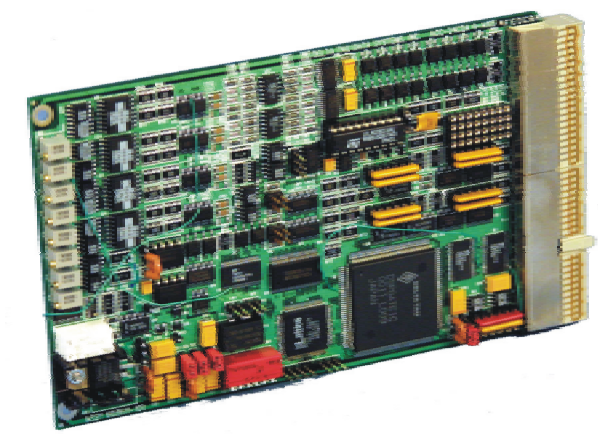
# USER MANUAL

# Accessory 24C2A



Compact UBUS 4-Axis Analog Servo Card

4Ax-603611-xUxx

October 15, 2003

DELTA TAU
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# INTRODUCTION

## Overview

The Acc-24C2A Axis Expansion Board is a single-slot module providing the interface circuitry for four axes, either analog interface for torque or velocity mode amplifiers or pulse and direction output for stepper motor drives. It has a slave Compact-UBUS interface on its J1 connector and the servo interface signals are on the J2 connector. Opto isolation is maintained between the analog circuitry and the digital circuitry to isolate the main axis flags.

The Acc-24C2A is part of the CPCI family of expansion cards and these accessory cards are designed to plug into an industrial CPCI rack system. The information from these accessories is passed directly to either the UMAC Turbo CPCI CPU via the high speed Compact UBUS. Other Compact UBUS interface cards include the following:

**Acc-11C:** General purpose 96-point I/O card with short circuit protection
Up to eight Acc-24C2A boards can be connected to one UMAC Turbo CPCI system, providing up to 32 additional channels of servo interface circuitry. The Acc-24C2A board contains no processor; it has one highly integrated 4-channel PMAC2-style Servo IC with the buffering circuitry and connectors around them. Some new features added to the family of Acc-24C2A breakout boards include:

- Loss of encoder circuit
- 5V to 24V Flag inputs
- Pulse and direction outputs for stepper systems or MLDTs
- 12-bit ADC option

## Features

The Acc-24C2A board can be used with any UMAC Turbo CPCI, interfacing through the Compact UBUS.

The Acc-24C2A supports a wide variety of servo and stepper interfaces:

- Analog +/-10V velocity commands
- Analog +/-10V torque commands
- Sinusoidal analog +/-10V phase current commands
- Pulse-and-direction commands
- Eight 12-bit ADC inputs

## Board Configuration

An Acc-24C2A comes standard with one Servo IC providing four servo interface channels, which are brought out on the P2 connectors on the backside of the Compact UBUS backplane board. Each channel of servo interface circuitry includes the following:

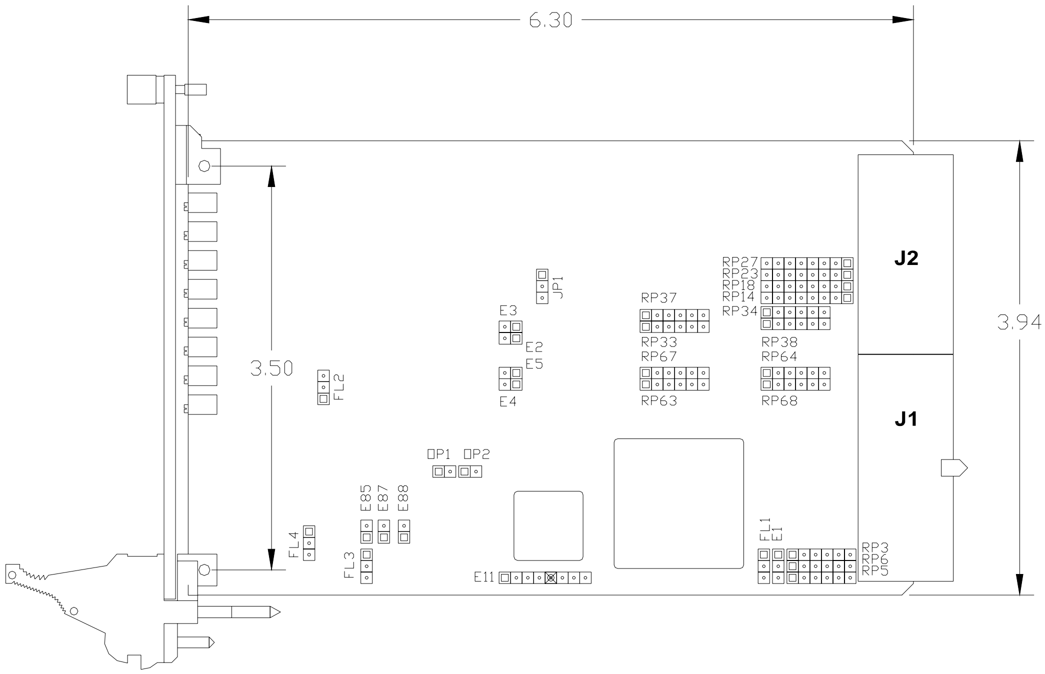
- Two output command signal sets, configurable as either:
  - One pulse-and-direction
  - Two DAC outputs
- Three-channel differential/single-ended encoder input
- Sixteen input flags, 4 Amplifier enable outputs

## Acc-24C2A Power Supply Requirements

The following table lists the power requirements for the Acc-24C2A.

| Product | 5V | 12V for DACs | -12V for DACs |
|---|---|---|---|
| Acc-24C2A | 1000mA | 400mA | 400mA |

# BOARD LAYOUT



# E-POINT JUMPER SETTINGS

## Acc-24C2A (Channels* 1, 2, 3, 4)

| Jumper | Config. | Description | Default |
|---|---|---|---|
| E1 | 1-2-3 | Jump 1-2 for UMAC MACRO CPCI (receive servo and phase clock)<br>Jump 2-3 for UMAC Turbo CPCI (source servo and phase clock) | Factory set |
| E2 | 1-2 | No Jumper for TTL Level input for CHU1, CHV1, CHW1, CHT1<br>Jumper 1-2 for DIR1+,DIR1-, PUL1+, PUL1- for stepper mode | No jumper |
| E3 | 1-2 | No Jumper for TTL Level input for CHU2, CHV2, CHW2, CHT2<br>Jumper 1-2 for DIR2+,DIR2-, PUL2+, PUL2- for stepper mode | No jumper |
| E4 | 1-2 | No Jumper for TTL Level input for CHU3, CHV3, CHW3, CHT3<br>Jumper 1-2 for DIR3+,DIR3-, PUL3+, PUL3- for stepper mode | No jumper |
| E5 | 1-2 | No Jumper for TTL Level input for CHU4, CHV4, CHW4, CHT4<br>Jumper 1-2 for DIR4+,DIR4-, PUL4+, PUL4- for stepper mode | No jumper |
| E85 | 1-2 | Jump 1-2 for Backplane Supplied +15V<br>No Jumper for External Supplied +15V | Jump 1-2 |
| E87 | 1-2 | Jump 1-2 for Backplane Supplied AGND<br>No Jumper for External Supplied AGND | Jump 1-2 |
| E88 | 1-2 | Jump 1-2 for Backplane Supplied -15V<br>No Jumper for External Supplied -15V | Jump 1-2 |
| OPT1 | 1-2 | For factory use only | |
| OPT2 | 1-2 | For factory use only | |
| *The channels refer to the Servo IC associated with the Acc-24C2A board. For example, an eight-axis application would have two Acc-24C2As. The first Acc-24C2A would have axes 1-4 and the second Acc-24C2A would contain axes 5-8. | | | |

# HARDWARE SETUP

## Switch Configuration

### UMAC Turbo CPCI Address DIP Switch S1

S1, S1-3, S1-4 are used to address the Acc-24C2A as shown in the table below.

| S1-1 | S1-3 | S1-4 | Board No. | IC No. | I-Var. Range | Base Address |
|---|---|---|---|---|---|---|
| ON | ON | ON | 1 | 2 | I7200 | $078200 |
| OFF | ON | ON | 2 | 3 | I7300 | $078300 |
| ON | OFF | ON | 3 | 4 | I7400 | $079200 |
| OFF | OFF | ON | 4 | 5 | I7500 | $079300 |
| ON | ON | OFF | 5 | 6 | I7600 | $07A200 |
| OFF | ON | OFF | 6 | 7 | I7700 | $07A300 |
| ON | OFF | OFF | 7 | 8 | I7800 | $07B200 |
| OFF | OFF | OFF | 8 | 9 | I7900 | $07B300 |

S1-2, S1-5, and S1-6 are used to determine whether the Acc-24C2A is communicating to a UMAC Turbo CPCI.

| S1-2 | S1-5 | S1-6 | Function |
|---|---|---|---|
| ON | ON | ON | UMAC Turbo CPCI Use |

## Acc-24C2A Clock Settings

The Phase Clock and Servo Clock must be configured on each Acc-24C2A base board to ensure proper operation. Each system can have only one source for the servo and phase clocks and jumpers must be set appropriately to avoid a timing conflict and a watchdog condition. There are two methods to set the phase clock and servo clock for the Acc-24C2A: UMAC Turbo MACRO CPCI Setup.

### UMAC CPCI Clock Setup for Acc-24C2A

Starting in Turbo firmware version 1.937, the firmware will set the clock settings for the Acc-24C2A cards in the Compact UBUS automatically. The user will have to set jumper E1 from 2 to 3 for all of the Acc-24C2As plugged into the Compact UBUS to enable this feature. At power up, the firmware will know that all of the cards are in the auto configuration setup and will assign the card with the lowest base address setting (usually $78200) the task of sourcing the clocks by setting variable I19 to the appropriate register. Initially, the clocks will be set the factory default servo update cycle and phase clock cycle.

### UMAC MACRO CPCI Clock Setup for Acc-24C2A

To manually set up the clock sources UMAC MACRO CPCI, set the Acc-24C2As to receive the phase and servo clock (E1 set 1-2).

## Resistor Pack Configuration

### Termination Resistors Packs

The Acc-24C2A provides sockets for termination resistors on differential input pairs coming into the board. As shipped, there are no resistor packs in these sockets. If these signals are brought long distances into the Acc-24C2A board and ringing at signal transitions is a problem, SIP resistor packs may be mounted in these sockets to reduce or eliminate the ringing.

All termination resistor packs are the types that have independent resistors (no common connection) with each resistor using two adjacent pins.

## Encoder Loss Resistor Packs

The Acc-24C2A also provides an encoder loss circuit to detect if the quadrature signals are valid. To activate this feature the user must reverse the resistor pack from its default configuration.

## Limit/Flag Voltage Level Resistor Packs

The Acc-24C2A limit and flag circuits also give the user the flexibility to wire in standard 12V to 24V limits and flags or they could wire in 5V level limits and flags on a channel basis (each Acc-24C2 has 4 channels). The default is set for the standard 12V to 24V inputs but if the resistor pack is added to the circuit, the card can read 5V inputs.

**Channel Specific Resistor Packs**

| Channel #1 | Channel #2 | Channel #3 | Channel #4 | SIP | Description |
|---|---|---|---|---|---|
| RP33 | RP34 | RP63 | RP64 | 2.2KΩ | Reverse resistor pack for encoder loss feature (for differential encoders only) |
| RP37 | RP38 | RP67 | RP68 | 220Ω | Termination resistor to reduce ringing (not installed by default). |
| RP14 | RP18 | RP23 | RP27 | 1KΩ | Install for 5V limits (not installed by default). |

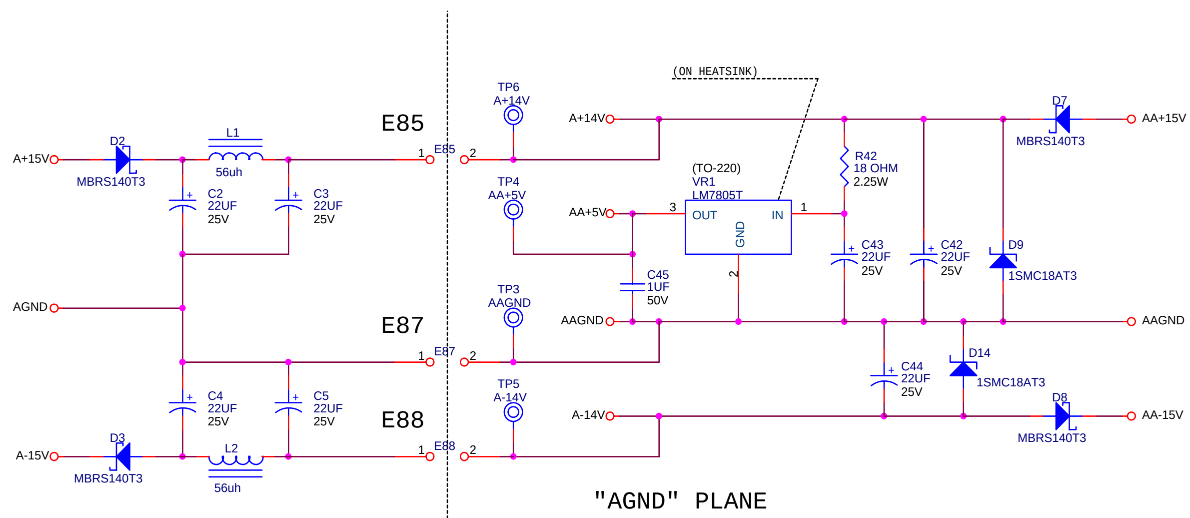
**Compact UBUS Specific Resistor Packs**

| Resistor Pack | SIP | Description |
|---|---|---|
| RP3 | 110Ω | Terminator for line receivers (always installed) |
| RP5 | 220Ω | Terminator (not installed, only used for non-CPCI Bus) |
| RP6 | 2.2 KΩ | Biasing resistor in pull down mode for non-terminating backplane (always installed) |

## Opto-Isolation Considerations

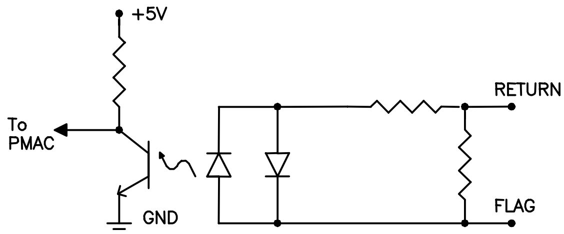
As shipped from the factory, the Acc-24C2A obtains its power from the Compact UBUS Backplane. Using this type of setup will defeat opto isolation since the analog ground plane will be tied directly to the digital ground plane.

If the user wants to optically isolate the analog ground plane from the digital ground plane, they will have to connect an external power supply the AA+15V, AA-15V, and AAGND inputs on the Acc-24C2A. Also, remove the E85, E87, and E88 jumpers to isolate the external power from the Compact UBUS power supplies.

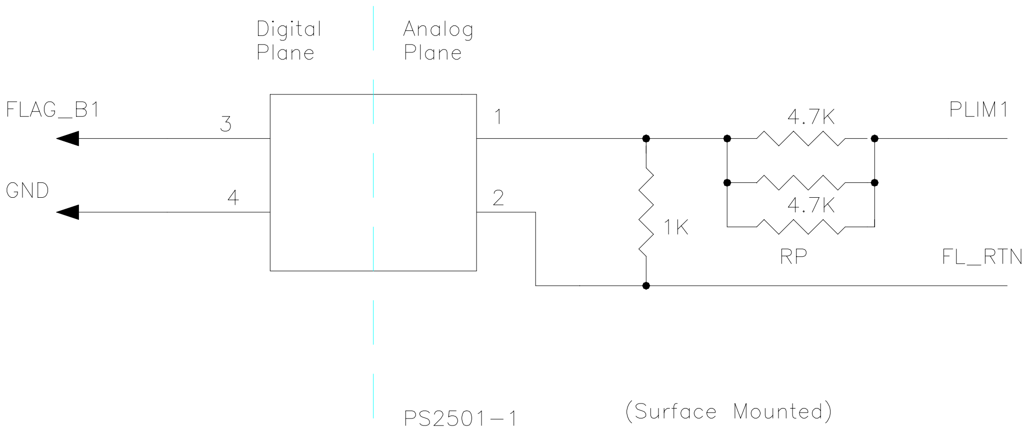


## Limit/Flag Circuit

The Acc-24C2A allows the user to use sinking or sourcing position limits and flags to the controller. The optoisolator IC used is a PS2701 photo transistor output type. This IC allows the current to flow from return to flag (sinking) or from flag to return (sourcing).

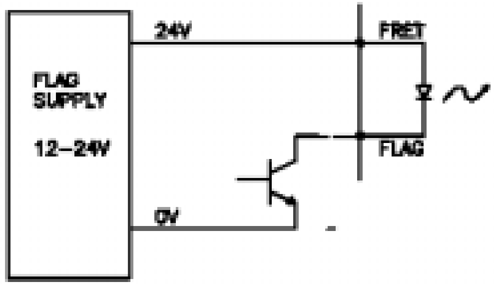



A sample of the positive limit circuit is shown below. The 4.7K resistor packs used will allow 12-24V flag inputs. If 0V to 5V voltage flags are used, then a 1KΩ resistor pack (RP) can be placed in either RP45 or RP46 (please refer to the Resistor Pack description section of this manual). If the user does add these resistor packs, all flags (±Limits, Home, User, and amplifier fault) will be referenced from 0V to 5V.

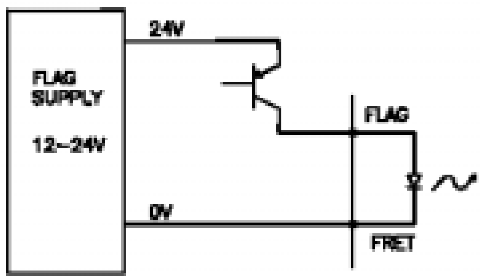


## Connecting Limits/Flags to the Acc-24C2A

The following diagrams illustrate the sinking and sourcing connections to an Acc-24C2A. For this example we are assuming the use of 12-24V flags.



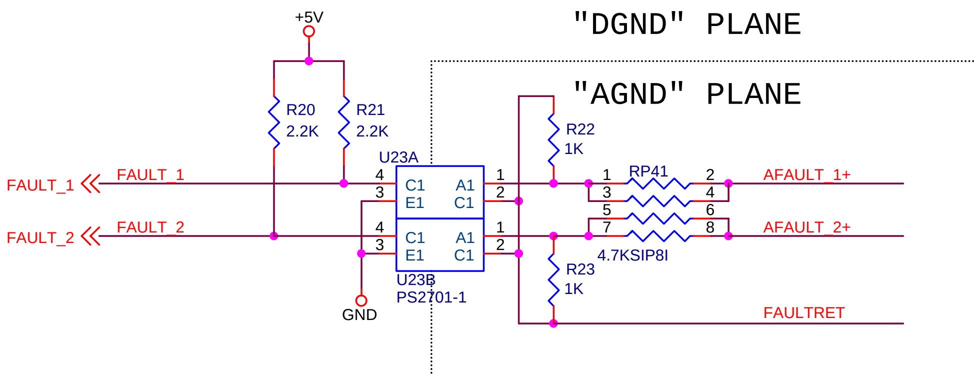

Sinking, Separate Supply




Sourcing, Separate Supply

## Amplifier Fault Circuit

The amplifier fault circuit for the Acc-24C2A is functionally the same circuit as the limits and flag circuit.




For single ended amplifier fault inputs, typically the AFAULT+ would be the actual signal input from the amplifier and the AFAULT- can be considered the reference.

**Single Ended Amplifier Fault Inputs**

| AFault+ | AFault- | Input Type |
|---|---|---|
| 0V | +12V to 24V | Sinking – Low True |
| 12V to 24V | 0V | Sourcing – High True |

## Loss of Encoder Circuit

The encoder-loss detection circuitry works only for differential incremental encoders. In proper operation, the digital states of the complementary inputs for a channel (e.g. A and A/) should always be opposite: when one is high, the other is low. If for some reason, such as a cable connection coming undone, one or more of the signal lines is no longer driven, pull-up resistors on the input line pull and hold the signal high.

The encoder-loss detection circuitry uses exclusive-or (XOR) gates on each complementary pair to detect whether the signals are in the same or opposite states. These results are combined to produce a single encoder-loss status bit that the processor can read.

This technique requires that both signal lines of the pair have pull-up resistors. Note that this is not the default configuration of a PMAC as it is shipped. The complementary lines (A/ and B/) are pulled to 2.5V in a voltage-divider configuration as shipped to be able to accept both single-ended and normal differential inputs. This must be changed to a pull-up configuration which involves reversing a socketed resistor pack on the Acc-24C2A.

**Acc-24C2A Discrete On-board Logic with UMAC Turbo CPCI**

| Channel | Resistor Pack | Status Bit Address (Even-Numbered Servo IC)* | Status Bit Address (Odd-Numbered Servo IC)* | Status Bit Name | Bit Error State |
|---|---|---|---|---|---|
| 1 | RP43 | Y:$07xF08,5 | Y:$07xF0C,5 | QL_1- | 0 |
| 2 | RP48 | Y:$07xF09,5 | Y:$07xF0D,5 | QL_2- | 0 |
| 3 | RP44 | Y:$07xF0A,5 | Y:$07xF0E,5 | QL_3- | 0 |
| 4 | RP49 | Y:$07xF0B,5 | Y:$07xF0F,5 | QL_4- | 0 |
| *The x digit in this hex address matches the value (8, 9, A, or B) in the fourth digit from the right in the board's own base address (e.g. $079200). If alternate addressing of Servo ICs is used (e.g. Servo IC 2*), add $20 to these addresses. | | | | | |

## Position Compare Port Driver IC

As with the other PMAC controllers, the UMAC Turbo CPCI has the high-speed position compare outputs allowing the user to fire an output based on position. This circuit will fire within 100 nsec of reaching the desired position. The position compare output port on the Acc-24C2A and its Option 1 daughter card have a socketed driver IC in a 8-pin DIP socket at component U27. This IC gives the user a fast CMOS driver.

The following table lists the properties of each driver IC:

| Part | # of Pins | Max Voltage and Current | Output Type | Max Frequency | E11, E12 Setting |
|---|---|---|---|---|---|
| DS75451N | 8 | 5V, 10 mA | Totem-Pole (CMOS) | 5 MHz | 1-2 |

# UMAC TURBO CPCI SOFTWARE SETUP

## Servo IC Configuration I-Variables

Turbo PMAC2 I-variables in the range I7200 – I7999 control the configuration of the Servo ICs. The hundred's digit represents the number of the Servo IC (2 to 9) in the system.

### Servo IC Numbering

The number m of the Servo IC on the Acc-24C2A board is dependent on the addressing of the board with DIP switches S1-1, S1-3, and S1-4, which place the board as the 1st through eighth external device:

- First Acc-24C2A: Servo IC 2 (channels 1-4)
- Second Acc-24C2A: Servo IC 3 (channels 5-8)
- Third Acc-24C2A: Servo IC 4 (channels 9-12)
- Fourth Acc-24C2A: Servo IC 5 (channels 13-16)
- Fifth Acc-24C2A: Servo IC 6 (channels 17-20)
- Sixth Acc-24C2A: Servo IC 7 (channels 21-24)
- Seventh Acc-24C2A: Servo IC 8 (channels 25-28)
- Eighth Acc-24C2A: Servo IC 9 (channels 29-32)

### Servo Channel Numbering

Each Servo IC has four channels of servo interface circuitry. The ten's digit n of the I-variable configuring the IC represents the channel number on the IC (n = 1 to 4). For example, Channel 1 of the Standard Servo IC on the first Acc-24C2A is configured by variables I7210 – I7219. These channel-specific I-variables are represented generically as I7mn0 – I7mn9, where m represents the Servo IC number (0 – 9) and n represents the IC channel number (1 – 4).

The Channels 1 – 4 on the Standard Servo IC of an Acc-24C2A correspond to Channels 1 – 4, respectively, on the Acc-24C2A board itself.

I-variables in the I7000s for which the ten's digit is 0 (Channel 0) affect all four channels of the PMAC2-style Servo IC on the Acc-24C2A. These multi-channel I-variables are represented generically as I7m00 – I7m09.

### Multi-Channel I-Variables

There are several multi-channel I-variables that must be set up properly for proper operation of the Acc-24C2A in a Turbo PMAC system. The most important are:

- **I7m07: Servo IC m Phase/Servo Clock Direction:** This variable should be set to 0 the Acc-24CPCI generating the clocks and set to 3 for the Acc-24C2As receiving the clocks. The setting I7m07 is setup automatically by the UMAC Turbo CPCI firmware.
- **I7m00: Servo IC m MaxPhase/PWM Frequency Control:** Typically, this will be set to the same value as the variable that controls the system clocks: I7200 on UMAC Turbo CPCI. If a different PWM frequency is desired, or the Acc-24C2A then the following constraint should be observed in setting this variable:

$$\frac{2 * PWMFreq(kHz)}{PhaseFreq} = \{Integer\}$$

- **I7m01: Servo IC m Phase Clock Frequency Control:** Even though the IC is receiving an external phase clock (see I7m07, above), it is usually best to create the same internal phase clock frequency in the Servo IC. This yields the following constraint:

$$I7m00 * (I7m01 + 1) = I7200 * (I7201 + 1) \quad \text{\{UMAC Turbo CPCI\}}$$

  Solving for I7m01, we get

$$I7m01 = \frac{I7200 * (I7201 + 1)}{I7m00} - 1 \qquad \{\text{UMAC Turbo CPCI}\}$$

If I7m00 is the same as I7200, I7m01 will be the same as I7201

- **I7m02: Servo IC m Servo Clock Frequency Control:** Even though the IC is receiving an external servo clock (see I7m07, above), usually it is best to create the same internal servo clock frequency in the Servo IC. This means that I7m02 for the IC should be set the same as I7202 on a UMAC Turbo CPCI.
- **I7m03: Servo IC m Hardware Clock Frequency Control:** The hardware clock frequencies for the Servo IC should be set according to the devices attached to it. There is no reason for these frequencies to be the same between ICs. There is seldom a reason to change this value from the default.

## Single-Channel I-Variables

The single-channel setup I-variables for Channel n of Servo IC m work the same on an Acc-24C2A as they do on a standard Turbo PMAC2 itself. Each Servo IC has four channels n, numbered 1 to 4. For the first (standard) Servo IC on the Acc-24C2A, the channel numbers 1 – 4 on the Servo IC are the same as the channel numbers 1 – 4 on the board. The most important variables are:

- **I7mn0: Servo IC m Channel n Encoder Decode Control:** Typically, I7mn0 is set to 3 or 7 for x4 quadrature decode, depending on which way is up. If the channel is used for open-loop stepper drive, I7mn0 is set to 8 to accept internal pulse-and-direction or to 0 to accept external pulse-and-direction (e.g. from an Acc-8S). It is set to 12 if the channel is used for MLDT feedback.
- **I7mn2: Servo IC m Channel n Capture Control:** I7mn2 determines whether the encoder index channel, an input flag, or both, are used for the capture of the encoder position.
- **I7mn3: Servo IC m Channel n Capture Flag Select:** I7mn3 determines which input flag is used for encoder capture, if one is used.
- **I7mn6: Servo IC m Channel n Output Mode Select:** I7mn6 determines whether the A and B outputs are DAC or PWM, and whether the C output is PFM (pulse-and-direction) or PWM. Typically, it is set to 0 for 3-phase PWM, or to 3 for DACs and PFM.

## Encoder Conversion Table I-Variables

To use feedback or master position data from an Acc-24C2A, entries must be added to the encoder conversion table (ECT) using I-variables I8000 – I8191 to address and process this data. The default conversion table in the Turbo PMAC does not contain these entries; it only contains entries for the eight channels on board the Turbo PMAC.

Usually, the position data obtained through an Acc-24C2A board is an incremental encoder feedback, and occasionally an A/D converter feedback from the ADC option on this card.

The ECT entries for Acc-24C2A incremental encoder channels are shown in the following table:

| Encoder Channel # | 1st and 2nd Acc-24C2A | 3rd and 4th Acc-24C2A | 5th and 6th Acc-24C2A | 7th and 8th Acc-24C2A |
|---|---|---|---|---|
| Channel 1 | $m78200 | $m79200 | $m7A200 | $m7B200 |
| Channel 2 | $m78208 | $m79208 | $m7A208 | $m7B208 |
| Channel 3 | $m78210 | $m79210 | $m7A210 | $m7B210 |
| Channel 4 | $m78218 | $m79218 | $m7A218 | $m7B218 |
| Channel 5 | $m78300 | $m79300 | $m7A300 | $m7B300 |
| Channel 6 | $m78308 | $m79308 | $m7A308 | $m7B308 |
| Channel 7 | $m78310 | $m79310 | $m7A310 | $m7B310 |
| Channel 8 | $m78318 | $m79318 | $m7A318 | $m7B318 |

The first hexadecimal digit in the entry, represented by m in the table, is a 0 for the most common 1/T timer-based extension of digital incremental encoders; it is an 8 for the parallel-data extension of analog incremental encoders; it is a C for no extension of an incremental encoder.

## Motor Addressing I-Variables

For a Turbo PMAC motor to use the servo interface circuitry of the Acc-24C2A, several of the addressing I-variables for the motor must contain the addresses of registers in the Acc-24C2A, or the addresses of encoder conversion table registers containing data processed from the Acc-24C2A. These I-variables can include:

- **Ixx02: Motor xx Command Output Address:** Ixx02 tells Turbo PMAC where to write its command outputs for Motor xx. If Acc-24C2A is to create the command signals, Ixx02 must contain the address of the register.

The following table shows the address of the 'A' output register for each channel of each Acc-24C2A. These addresses can be used for single analog outputs, double analog outputs, or direct PWM outputs.

| Acc-24C2A Register: Board No. and Channel | Address / Ixx02 Value | UMAC Turbo CPCI | Acc-24C2A Register: Board No. and Channel | Address / Ixx02 Value | UMAC Turbo CPCI |
|---|---|---|---|---|---|
| 1st Acc-24C2A DAC/PWM1A | $078202 | I102 | 5th Acc-24C2A DAC/PWM1A | $07A202 | I1702 |
| 1st Acc-24C2A DAC/PWM2A | $07820A | I202 | 5th Acc-24C2A DAC/PWM2A | $07A20A | I1802 |
| 1st Acc-24C2A DAC/PWM3A | $078212 | I302 | 5th Acc-24C2A DAC/PWM3A | $07A212 | I1902 |
| 1st Acc-24C2A DAC/PWM4A | $07821A | I402 | 5th Acc-24C2A DAC/PWM4A | $07A21A | I2002 |
| 2nd Acc-24C2A DAC/PWM1A | $078302 | I502 | 6th Acc-24C2A DAC/PWM1A | $07A302 | I2102 |
| 2nd Acc-24C2A DAC/PWM2A | $07830A | I602 | 6th Acc-24C2A DAC/PWM2A | $07A30A | I2202 |
| 2nd Acc-24C2A DAC/PWM3A | $078312 | I702 | 6th Acc-24C2A DAC/PWM3A | $07A312 | I2302 |
| 2nd Acc-24C2A DAC/PWM4A | $07831A | I802 | 6th Acc-24C2A DAC/PWM4A | $07A31A | I2402 |
| 3rd Acc-24C2A DAC/PWM1A | $079202 | I902 | 7th Acc-24C2A DAC/PWM1A | $07B202 | I2502 |
| 3rd Acc-24C2A DAC/PWM2A | $07920A | I1002 | 7th Acc-24C2A DAC/PWM2A | $07B20A | I2602 |
| 3rd Acc-24C2A DAC/PWM3A | $079212 | I1102 | 7th Acc-24C2A DAC/PWM3A | $07B212 | I2702 |
| 3rd Acc-24C2A DAC/PWM4A | $07921A | I1202 | 7th Acc-24C2A DAC/PWM4A | $07B21A | I2802 |
| 4th Acc-24C2A DAC/PWM1A | $079302 | I1302 | 8th Acc-24C2A DAC/PWM1A | $07B302 | I2902 |
| 4th Acc-24C2A DAC/PWM1A | $07930A | I1402 | 8th Acc-24C2A DAC/PWM2A | $07B30A | I3002 |
| 4th Acc-24C2A DAC/PWM2A | $079312 | I1502 | 8th Acc-24C2A DAC/PWM3A | $07B312 | I3102 |
| 4th Acc-24C2A DAC/PWM4A | $07931A | I1602 | 8th Acc-24C2A DAC/PWM4A | $07B31A | I3202 |

If the C output register for a given Acc-24C2A and channel is used (primarily for pulse and direction output), simply add 2 to the address shown in the above table. For example, on the first Acc-24C2A, output register 1C is at address $078204.

**Ixx03: Motor xx Position-Loop Feedback Address**

**Ixx04: Motor xx Velocity-Loop Feedback Address**

**Ixx05: Motor xx Master Position Address**

Usually, the Ixx03, Ixx04, and Ixx05 variables contain the address of a processed position value in the encoder conversion table, even when the raw data comes from the Acc-24C2A. The first line of the encoder conversion table is at address $003501; the last line is at address $0035C0.

**Ixx10: Motor xx Power-On Position Address:** Ixx10 tells the Turbo PMAC where to read absolute power-on position, if any. Typically, the only times Ixx10 will contain the address of an Acc-24C2A register is if the position is obtained from an A/D converter from the Acc-24C2A, or if it is obtained from an MLDT (e.g. Temposonics™) sensor excited directly from an Acc-24C2A.

The following table shows the possible values of Ixx10 for MLDT timer registers:

**Ixx10 for Acc-24C2A MLDT Timer Registers (Ixx95=$170000)**

| MLDT Timer Channel # | 1st and 2nd Acc-24C2A | 3rd and 4th Acc-24C2A | 5th and 6th Acc-24C2A | 7th and 8th Acc-24C2A |
|---|---|---|---|---|
| Channel 1 | $078200 | $079200 | $07A200 | $07B200 |
| Channel 2 | $078208 | $079208 | $07A208 | $07B208 |
| Channel 3 | $078210 | $079210 | $07A210 | $07B210 |
| Channel 4 | $078218 | $079218 | $07A218 | $07B218 |
| Channel 5 | $078300 | $079300 | $07A300 | $07B300 |
| Channel 6 | $078308 | $079308 | $07A308 | $07B308 |
| Channel 7 | $078310 | $079310 | $07A310 | $07B310 |
| Channel 8 | $078318 | $079318 | $07A318 | $07B318 |

- **Ixx24: Motor xx Flag Mode:** Ixx24 defines how to read and use the flags for Motor xx that are in the register specified by Ixx25. Ixx24 is a set of independent control bits. There are two bits that must be set correctly to use a flag set on an Acc-24C2A.

  Bit 0 of Ixx24 must be set to 1 to tell the Turbo PMAC that this flag set is in a Type 1 PMAC2-style Servo IC. Bit 18 of Ixx24 must be set to 0 to tell the Turbo PMAC that this flag set is not transmitted over a MACRO ring. Other bits of Ixx24 may be set as desired for a particular application.

- **Ixx25: Motor xx Flag Address:** Ixx25 tells Turbo PMAC where to access its flag data for Motor xx. If Acc-24C2A is interfaced to the flags, Ixx25 must contain the address of the flag register in Acc-24C2A. The following table shows the address of the flag register for each channel of each Acc-24C2A.

| Acc-24C2A Register: Board No. and Channel | Address / Ixx25 Value | UMAC Default for: | Acc-24C2A Register: Board No. and Channel | Address / Ixx25 Value | UMAC Default for: |
|---|---|---|---|---|---|
| 1st Acc-24C2A Flag Set 1 | $078200 | I125 | 5th Acc-24C2A Flag Set 1 | $07A200 | I1725 |
| 1st Acc-24C2A Flag Set 2 | $078208 | I225 | 5th Acc-24C2A Flag Set 2 | $07A208 | I1825 |
| 1st Acc-24C2A Flag Set 3 | $078210 | I325 | 5th Acc-24C2A Flag Set 3 | $07A210 | I1925 |
| 1st Acc-24C2A Flag Set 4 | $078218 | I425 | 5th Acc-24C2A Flag Set 4 | $07A218 | I2025 |
| 2nd Acc-24C2A Flag Set 1 | $078300 | I525 | 6th Acc-24C2A Flag Set 1 | $07A300 | I2125 |
| 2nd Acc-24C2A Flag Set 2 | $078308 | I625 | 6th Acc-24C2A Flag Set 2 | $07A308 | I2225 |
| 2nd Acc-24C2A Flag Set 3 | $078310 | I725 | 6th Acc-24C2A Flag Set 3 | $07A310 | I2325 |
| 2nd Acc-24C2A Flag Set 4 | $078318 | I825 | 6th Acc-24C2A Flag Set 4 | $07A318 | I2425 |
| 3rd Acc-24C2A Flag Set 1 | $079200 | I925 | 7th Acc-24C2A Flag Set 1 | $07B200 | I2525 |
| 3rd Acc-24C2A Flag Set 2 | $079208 | I1025 | 7th Acc-24C2A Flag Set 2 | $07B208 | I2625 |
| 3rd Acc-24C2A Flag Set 3 | $079210 | I1125 | 7th Acc-24C2A Flag Set 3 | $07B210 | I2725 |
| 3rd Acc-24C2A Flag Set 4 | $079218 | I1225 | 7th Acc-24C2A Flag Set 4 | $07B218 | I2825 |
| 4th Acc-24C2A Flag Set 1 | $079300 | I1325 | 8th Acc-24C2A Flag Set 1 | $07B300 | I2925 |
| 4th Acc-24C2A Flag Set 2 | $079308 | I1425 | 8th Acc-24C2A Flag Set 2 | $07B308 | I3025 |
| 4th Acc-24C2A Flag Set 3 | $079310 | I1525 | 8th Acc-24C2A Flag Set 3 | $07B310 | I3125 |
| 4th Acc-24C2A Flag Set 4 | $079318 | I1625 | 8th Acc-24C2A Flag Set 4 | $07B318 | I3225 |

- **Ixx81: Motor xx Power-On Phase Position Address:** Ixx81 tells Turbo PMAC2 where to read absolute power-on position for motor phase commutation, if any. Typically, it will contain the address of an Acc-24C2A register for only two types of absolute phasing sensors: hall-effect commutation sensors (or their optical equivalents) connected to the U, V, and W input flags on an Acc-24C2A channel.

  The following table contains the possible settings of Ixx81 for hall sensor absolute position with an Acc-24C2A:

**Turbo PMAC Ixx81 Acc-24C2A Hall Phasing Settings**

**(Ix91=$800000 - $FF0000)**

| Hall Flag Channel # | 1st and 2nd Acc-24C2A | 3rd and 4th Acc-24C2A | 5th and 6th Acc-24C2A | 7th and 8th Acc-24C2A |
|---|---|---|---|---|
| Channel 1 | $078200 | $079200 | $07A200 | $07B200 |
| Channel 2 | $078208 | $079208 | $07A208 | $07B208 |
| Channel 3 | $078210 | $079210 | $07A210 | $07B210 |
| Channel 4 | $078218 | $079218 | $07A218 | $07B218 |
| Channel 5 | $078300 | $079300 | $07A300 | $07B300 |
| Channel 6 | $078308 | $079308 | $07A308 | $07B308 |
| Channel 7 | $078310 | $079310 | $07A310 | $07B310 |
| Channel 8 | $078318 | $079318 | $07A318 | $07B318 |

The following table contains the possible settings of Ixx81 to read the encoder counters for Yaskawa absolute encoders:

**Turbo PMAC Ixx81 Acc-24C2A Encoder Register Settings**

**(Ix91=$480000 - $580000)**

| Encoder Register Channel # | 1st and 2nd Acc-24C2A | 3rd and 4th Acc-24C2A | 5th and 6th Acc-24C2A | 7th and 8th Acc-24C2A |
|---|---|---|---|---|
| Channel 1 | $078201 | $079201 | $07A201 | $07B201 |
| Channel 2 | $078209 | $079209 | $07A209 | $07B209 |
| Channel 3 | $078211 | $079211 | $07A211 | $07B211 |
| Channel 4 | $078219 | $079219 | $07A219 | $07B219 |
| Channel 5 | $078301 | $079301 | $07A301 | $07B301 |
| Channel 6 | $078309 | $079309 | $07A309 | $07B309 |
| Channel 7 | $078311 | $079311 | $07A311 | $07B311 |
| Channel 8 | $078319 | $079319 | $07A319 | $07B319 |

- **Ixx82: Motor xx Current Feedback Address:** Ixx82 tells Turbo PMAC where to get its current-loop feedback every phase update cycle. If Ixx82 is set to 0, Turbo PMAC does not perform current-loop calculations for Motor xx.

The following table shows the possible values of Ixx82 for Acc-24C2 ADC register pairs:

**Turbo PMAC Ixx82 Acc-24C2A ADC Register Settings**

| ADC Register Channel # | 1st and 2nd Acc-24C2A | 3rd and 4th Acc-24C2A | 5th and 6th Acc-24C2A | 7th and 8th Acc-24C2A |
|---|---|---|---|---|
| Channel 1 | $078206 | $079206 | $07A206 | $07B206 |
| Channel 2 | $07820E | $07920E | $07A20E | $07B20E |
| Channel 3 | $078216 | $079216 | $07A216 | $07B216 |
| Channel 4 | $07821E | $07921E | $07A21E | $07B21E |
| Channel 5 | $078306 | $079306 | $07A306 | $07B306 |
| Channel 6 | $07830E | $07930E | $07A30E | $07B30E |
| Channel 7 | $078316 | $079316 | $07A316 | $07B316 |
| Channel 8 | $07831E | $07931E | $07A31E | $07B31E |

- **Ixx83: Motor xx Phase Position Address:** Ixx83 tells Turbo PMAC where to get its commutation position feedback every phase update cycle. Usually, this contains the address of an encoder phase position register.

The following table shows the possible values of Ixx83 for Acc-24C2A encoder phase position registers:

**Turbo PMAC Ixx83 Acc-24C2A Encoder Register Settings**

| Encoder Register Channel # | 1st and 2nd Acc-24C2A | 3rd and 4th Acc-24C2A | 5th and 6th Acc-24C2A | 7th and 8th Acc-24C2A |
|---|---|---|---|---|
| Channel 1 | $078201 | $079201 | $07A201 | $07B201 |
| Channel 2 | $078209 | $079209 | $07A209 | $07B209 |
| Channel 3 | $078211 | $079211 | $07A211 | $07B211 |
| Channel 4 | $078219 | $079219 | $07A219 | $07B219 |
| Channel 5 | $078301 | $079301 | $07A301 | $07B301 |
| Channel 6 | $078309 | $079309 | $07A309 | $07B309 |
| Channel 7 | $078311 | $079311 | $07A311 | $07B311 |
| Channel 8 | $078319 | $079319 | $07A319 | $07B319 |

## UMAC Turbo CPCI Example Setups

The following section will show the user how to quickly setup the key variables for a DAC output system and for a combination torque mode (DAC) and stepper motor (PFM) system.

For these examples, the factory defaults for the other variables will allow the user to command DAC outputs and PFM outputs with a low true Amplifier Fault and ±Limits plugged in. If this is not the case then Ixx24 will have to be modified. The PID gains will also have to be modified for optimum closed loop control

**Example A: 4-axis DAC outputs from base address $078200 (servo IC2)**
For this type of system, the user will have to make sure I7mn6 is set for DAC output mode. Remember, UMAC Turbo has three outputs per channel (CHnA, CHnB, and CHnC)

```
I7216=3         ;CH1A and CH1B ouputs will be DAC and CH1C output will be PFM
I7226=3         ;CH2A and CH2B ouputs will be DAC and CH2C output will be PFM
I7236=3         ;CH3A and CH3B ouputs will be DAC and CH3C output will be PFM
I7246=3         ;CH4A and CH4B ouputs will be DAC and CH4C output will be PFM
```

**Example B: 2-axis PFM outputs and 2-axes PFM from base address $078200 (servo IC2). Assume DAC outputs on channels 1 and 2 and PFM outputs on channels 3** and **4. Jumpers E1A through C2AD must be jumpered on Acc-24C2A Option 1 only.**

For this type of system, the user will have to make sure I7mn6 is set for DAC and PFM output mode.

```
I7216=3         ;CH1A and CH1B ouputs will be DAC and CH1C output will be PFM
I7226=3         ;CH2A and CH2B ouputs will be DAC and CH2C output will be PFM
I7236=3         ;CH3A and CH3B ouputs will be DAC and CH3C output will be PFM
I7246=3         ;CH4A and CH4B ouputs will be DAC and CH4C output will be PFM

I102=$078202  ;Command output  to CH1A address (default) for DAC
I202=$07820A  ;Command output  to CH2A address (default) for DAC
I302=$078214  ;Command output  to CH3C address (default address + 2) for Stepper
I402=$07821C  ;Command output  to CH4C address (default address +2) for Stepper
```

# MLDT FEEDBACK SETUP

The Acc-24C2A can provide direct interface to magnetostrictive linear displacement transducers (MLDTs) through its encoder connectors. This interface is for MLDTs with an external excitation format (often called RS-422 format) because of the signal levels, because the Acc-24C2A provides the excitation pulse, and receives the echo pulse, both with RS-422 signal formats.

This section provides basic information for using MLDTs with the Acc-24C2A.

## MLDT Hardware Setup of the Acc-24C2A

The Acc-24C2A must be set up to output the differential pulse on what is normally the T and W input flags on the encoder connector. This is done by putting jumpers on E-points (E2, E3, E4, E5) for the corresponding channel on the Acc-24C2A. These jumpers are OFF by default.

The PULSE+ (high during the pulse) and PULSE- (low during the pulse) outputs from the encoder connector are connected to the differential pulse inputs on the MLDT. The echo pulse differential outputs from the MLDT are connected to the CHA+ and CHA- input pins on the same encoder connector.

If the MLDT uses RPM format, in which there is a brief start echo pulse, and a brief stop echo pulse, the + output from the MLDT should be connected to the CHA+ input on the Acc-24C2A, and the - output should be connected to the CHA- input.

If the MLDT uses DPM format, in which there is a single long echo pulse, with the delay to the trailing edge measuring the position, the + output from the MLDT should be connected to the CHA- input on the Acc-24C2A, and the - output should be connected to the CHA+ input.

## MLDT Software Setup of the UMAC Turbo CPCI

When the Acc-24C2A is used for MLDT feedback in a UMAC Turbo CPCI system, a few I-variables must be set up properly.

### Hardware Setup I-Variables for Servo IC m

- **I7m03 (PFM Clock Frequency):** In almost all cases, the clock frequency driving the pulse-generation circuitry for all channels on Servo IC m can be left at its default value of 9.83 MHz (0.102 µsec). Few people will need to change I7m03, which also controls other clock signals, from its default value of 2258.
- **I7m04 (PFM Pulse Width):** The pulse width, set by I7m04 in units of PFM clock cycles must be set long enough for the MLDT to see, and long enough to contain the rising edge of the RPM start echo pulse, or the rising edge of the single DPM echo pulse. For example, if this edge can come up to 2 µsec after the start of the excitation pulse, and the PMAC clock cycle is at its default of about 0.1 µsec, then I7m04 must be set at least to 20.
- **I7mn6 (Output Format Select):** For Servo IC m Channel n to be used for MLDT feedback, I7mn6 must be set to 1 or 3 for the C sub-channel to be used for PFM-format output. On an Acc-24C2A, I7mn6 must then be set to 3 for the A and B sub-channels to be used for DAC-format output.
- **I7mn0 (MLDT Feedback Select):** For Servo IC m Channel n to be used for MLDT feedback, I7mn0 must be set to 12. In this mode, the pulse timer is cleared on the output pulse, and latched on the echo pulse, counting in between at 117.96 MHz.

### Conversion Table Processing I-Variables

The pulse timer for Servo IC m Channel n holds a number proportional to the time and therefore the position. This must be processed in the conversion table before it can be used by the servo loop. It is best to use the filtered parallel data conversion, a 3-line entry in the table (three consecutive I-variables.

- **Line 1 (Method and Address):** This 24-bit value (6 hex digits) should begin with a 3 (filtered parallel data) followed by the address of the timer register. The possible values for this line are shown in the following table:

**Encoder Conversion Table Parallel Filtered Data Format 1st Line**

For Acc-24C2A Boards with Servo IC m Channel n

| Acc-24 # | Servo IC # | Channel 1 | Channel 2 | Channel 3 | Channel 4 |
|---|---|---|---|---|---|
| 1 | 2 | $378200 | $378208 | $378210 | $378218 |
| 2 | 3 | $378300 | $378308 | $378310 | $378318 |
| 3 | 4 | $379200 | $379208 | $379210 | $379218 |
| 4 | 5 | $379300 | $379308 | $379310 | $379318 |
| 5 | 6 | $37A200 | $37A208 | $37A210 | $37A218 |
| 6 | 7 | $37A300 | $37A308 | $37A310 | $37A318 |
| 7 | 8 | $37B200 | $37B208 | $37B210 | $37B218 |
| 8 | 9 | $37B300 | $37B308 | $37B310 | $37B318 |

- **Line 2 (Width and Start):** This 24-bit value should be set to $013000 to specify the use of 19 bits ($013) starting at bit 0.
- **Line 3 (Max Change):** This 24-bit value should be set to a value slightly greater than the maximum true velocity ever expected, expressed in timer LSBs per servo cycle. With a typical MLDT, the 117.96 MHz timer LSB represents 0.024 mm (0.00094 inches); the default servo cycle is 0.442 msec.

The result of this conversion is in the X-register of the third line. Any functions using this value should address this register. For example, if this were the first entry in the table, which starts at $003501, the result would be in X:$003503.

## Motor I-Variables

- **Ixx03 (Position Loop Feedback Address):** To use the result of the conversion table for position-loop feedback for Motor xx, Ixx03 should contain the address of the result register in the conversion table - $003503 in the above example.
- **Ixx04 (Velocity Loop Feedback Address):** To use the result of the conversion table for velocity-loop feedback for Motor xx, Ixx04 should contain the address of the result register in the conversion table - $003503 in the above example.
- **Ixx05 (Master Position Address):** To use the result of the conversion table for the master position for Motor xx, Ixx05 should contain the address of the result register in the conversion table - $003503 in the above example.
- **Ixx10 and Ixx95 (Power-On Position Address and Format):** To use the MLDT for absolute power-on position for Motor xx, Ixx95 should be set to $180000 (up to 24 bits of parallel Y-data) and Ixx10 should be set to the address of the timer register used:

**Ixx10 for Acc-24C2A MLDT Timer Registers (Ixx95=$180000)**

| Acc-24 # | Servo IC # | Channel 1 | Channel 2 | Channel 3 | Channel 4 |
|---|---|---|---|---|---|
| 1 | 2 | $078200 | $078208 | $078210 | $078218 |
| 2 | 3 | $078300 | $078308 | $078310 | $078318 |
| 3 | 4 | $079200 | $079208 | $079210 | $079218 |
| 4 | 5 | $079300 | $079308 | $079310 | $079318 |
| 5 | 6 | $07A200 | $07A208 | $07A210 | $07A218 |
| 6 | 7 | $07A300 | $07A308 | $07A310 | $07A318 |
| 7 | 8 | $07B200 | $07B208 | $07B210 | $07B218 |
| 8 | 9 | $07B300 | $07B308 | $07B310 | $07B318 |

- **Ixx80 (Power-On Mode):** Set Ixx80 to 4 to delay the absolute power-on position read until the pulse-output frequency can be set.
- **Ixx81 and Ixx91 (Power-On Phase Position Address and Format):** Occasionally the MLDT is used to establish an absolute phase reference position for Turbo-PMAC-commutated motors. In this case, Ixx81 and Ixx91 are set to the same values as Ixx10 and Ixx95, respectively (see above).

## Pulse Output Frequency

The pulse-output frequency is established by assigning an M-variable to the C sub-channel command register, and writing a value to that M-variable after every power-up/reset. The suggested M-variable for the Motor xx using this register is:

Mxx07->Y:{address},8,16,S

where **`{address}`** is specified according to the following table:

**Mxx07 for Acc-24C2A MLDT Pulse-Output Registers**

| Acc-24 # | Servo IC # | Channel 1 | Channel 2 | Channel 3 | Channel 4 |
|---|---|---|---|---|---|
| 1 | 2 | $078204 | $07820C | $078214 | $07821C |
| 2 | 3 | $078304 | $07830C | $078314 | $07831C |
| 3 | 4 | $079204 | $07920C | $079214 | $07921C |
| 4 | 5 | $079304 | $07930C | $079314 | $07931C |
| 5 | 6 | $07A204 | $07A20C | $07A214 | $07A21C |
| 6 | 7 | $07A304 | $07A30C | $07A314 | $07A31C |
| 7 | 8 | $07B204 | $07B20C | $07B214 | $07B21C |
| 8 | 9 | $07B304 | $07B30C | $07B314 | $07B31C |

The frequency of the pulse output should produce a period just slightly longer than the longest expected response time for the echo pulse. For MLDTs, the response time is approximately 0.35 μsec/mm (9 μsec/inch). On an MLDT 1500 mm (~60 in) long, the longest response time is approximately 540 μsec; a recommended period between pulse outputs for this device is 600 μsec, for a frequency of 1667 Hz.

To produce the desired pulse output frequency, the following formula can be used (assuming a 16-bit M-variable definition):

$$OutputFreq(kHz) = \frac{Mxx07}{65{,}536} PFMCLK\_Freq(kHz)$$

or:

$$Mxx07 = 65{,}536 * \frac{OutputFreq(kHz)}{PFMCLK\_Freq(kHz)}$$

To produce a pulse output frequency of 1.667 kHz with the default PFMCLK frequency of 9.83 MHz, we calculate:

$$Mxx07 = 65{,}536 * \frac{1.667}{9{,}380} \cong 11$$

To write this value to the register, a power-on PLC routine is suggested; this can be done also with on-line commands from the host computer. Sample PLC code to do this for Channel 1, using the above example value, is:

```
OPEN PLC 1                    ; PLC 1 is first program to execute
CLEAR
  M107=11                     ; Set pulse frequency
  CMD"$*"                     ; Absolute Position Read
DISABLE PLC 1                 ; So will not execute again
CLOSE
```

# 12-BIT ADC OPTION

The 12-bit ADC option on the Acc-24C2A allows the user to read analog input signals for the purpose of either closed loop servo feedback or general purpose monitoring. The Analog-to-Digital Converter (ADC) unit used in Acc-24C2A is the ADS7861 2 + 2 channel simultaneous 12-bit device manufactured by Burr-Brown. These devices have 12-bit resolution with ± 1/2 LSB linearity specification. For more details of the ADC chips please refer to the data sheet published by the manufacturer.

The data from the ADCs on the Acc-24C2A is not software supported in the Servo IC (GATE 1C). A description of the on-board ADCs will be added when the new version of the Servo IC (GATE 1D) is released.

# PINOUT DESCRIPTION

**P2 Connector**

| Row | A | B | C | D | E |
|---|---|---|---|---|---|
| 22 | DACA1+ | DACA2+ | A+12/15V | DACA3+ | DACA4+ |
| 21 | DACA1- | DACA2- | AGND | DACA3- | DACA4- |
| 20 | DACB1+ | DACB2+ | A-12/15V | DACB3+ | DACB4+ |
| 19 | DACB1- | DACB2- | AGND | DACB3- | DACB4- |
| 18 | AENA1+ | AENA2+ | AENARET | AENA3+ | AENA4+ |
| 17 | FAULT1 | FAULT2 | FAULTRET | FAULT3 | FAULT4 |
| 16 | FRET1 | FRET2 | ADCA1 | FRET3 | FRET4 |
| 15 | HOME1 | HOME2 | ADCB1 | HOME3 | HOME4 |
| 14 | PLIM1 | PLIM2 | ADCA2 | PLIM3 | PLIM4 |
| 13 | MLIM1 | MLIM2 | ADCB2 | MLIM3 | MLIM4 |
| 12 | USER1 | USER2 | ADCA3 | USER3 | USER4 |
| 11 | DIR1+/U1 | DIR2+/U2 | ADCB3 | DIR3+/U3 | DIR4+/U4 |
| 10 | DIR1-/V1 | DIR2-/V2 | ADCA4 | DIR3-/V3 | DIR4-/V4 |
| 9 | PUL1+/W1 | PUL2+/W2 | ADCB4 | PUL3+/W3 | PUL4+/W4 |
| 8 | PUL1-/T1 | PUL2-/T2 | GND | PUL3-/T3 | PUL4-/T4 |
| 7 | EQU1 | EQU2 | GND | EQU3 | EQU4 |
| 6 | ENCC1+ | ENCC2+ | GND | ENCC3+ | ENCC4+ |
| 5 | ENCC1- | ENCC2- | GND | ENCC3- | ENCC4- |
| 4 | ENCB1+ | ENCB2+ | +5V | ENCB3+ | ENCB4+ |
| 3 | ENCB1- | ENCB2- | +5V | ENCB3- | ENCB4- |
| 2 | ENCA1+ | ENCA2+ | +5V | ENCA3+ | ENCA4+ |
| 1 | ENCA1- | ENCA2- | +5V | ENCA3- | ENCA4- |

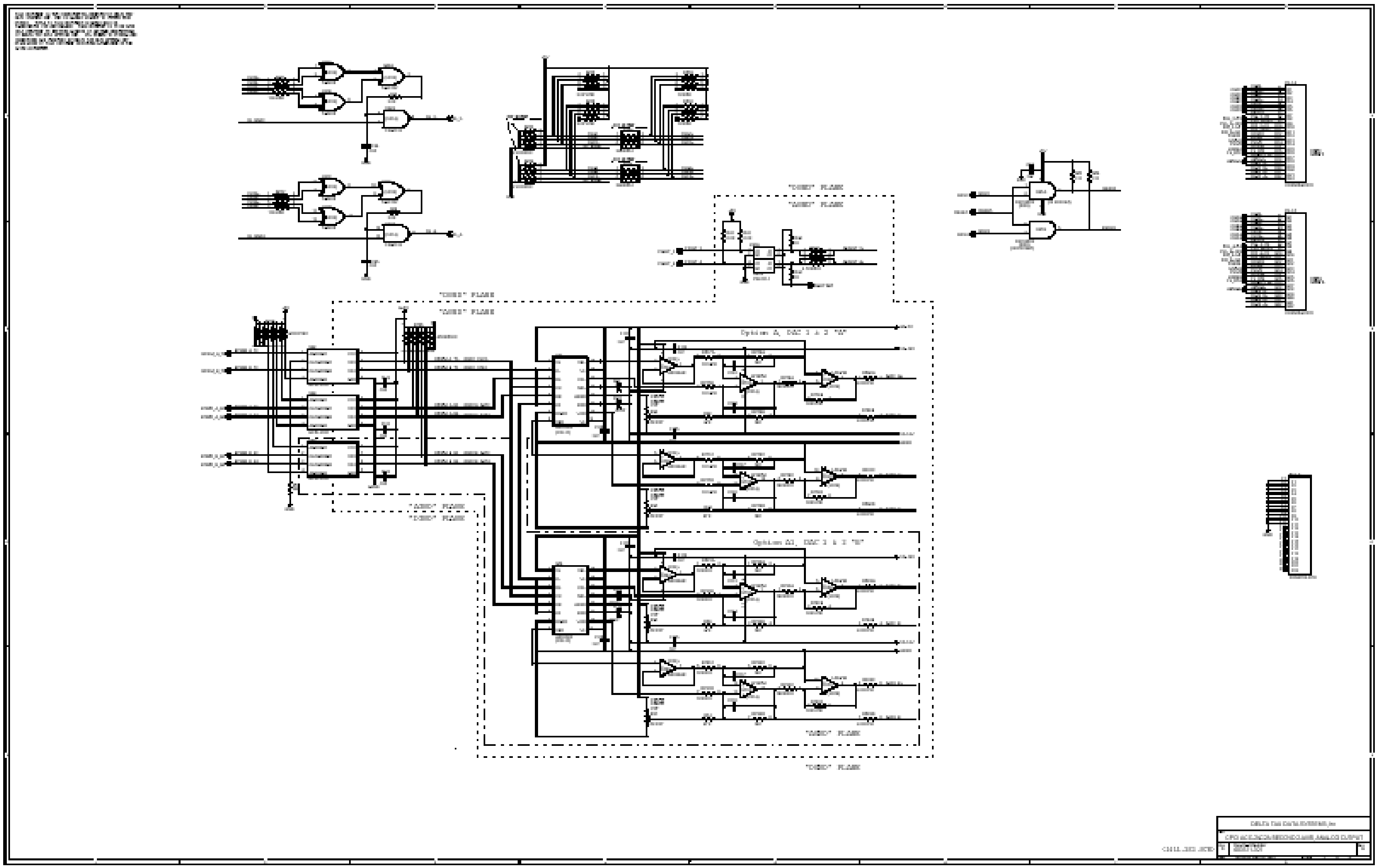
**Notes:**

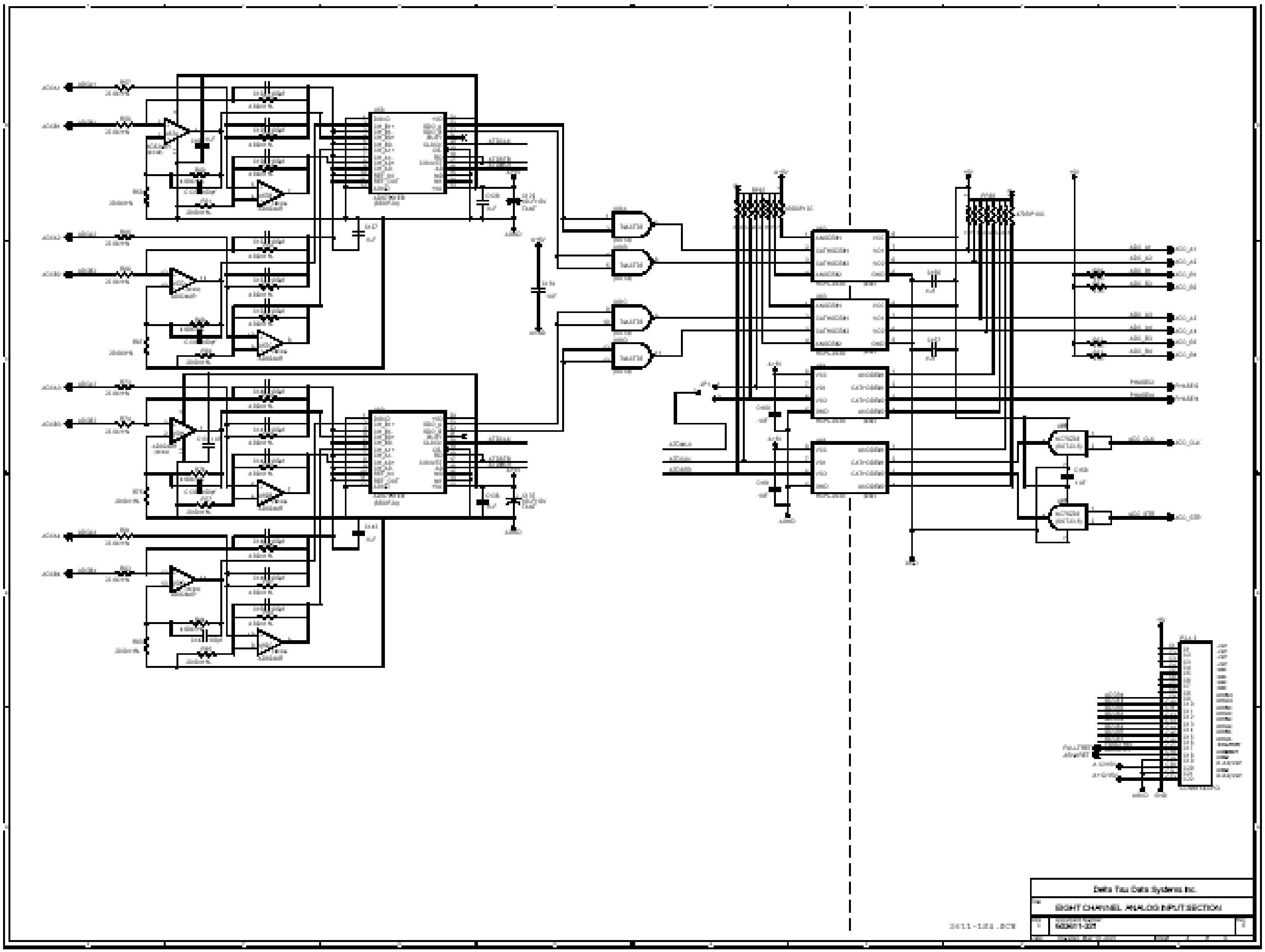
1. Signals in Rows 19 to 22, and ADC pins, are referenced to AGND (analog ground), optically isolated from the digital circuits.
2. Signals in Rows 1 to 11 (except ADCs) are referenced to GND (digital ground).
3. The signal AENARET is the return signal for the 4 isolated AENAn outputs.
4. Each signal FRETn is the return signal for optically isolated sinking/sourcing inputs HOMEn, PLIMn, MLIMn, and USERn. Each set of these four inputs is isolated from all other circuits on the board.
5. The signal FAULTRET is the return for the four optically isolated sinking/sourcing FAULTn inputs. Typically, these inputs will be ultimately referenced to AGND.
6. Outer columns Z and F are all shield pins.
7. Each channel has a jumper to permit the output of Pulse and Direction signals on what would otherwise be T, U, V, and W supplementary input flags (rows 12 to 15).

***Note:***

Row 22 is physically the top row with the cards in normal orientation.

# SCHEMATICS




Delta Tau Data Systems Inc.
EIGHT CHANNEL ANALOG INPUT SECTION