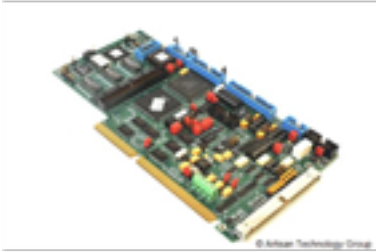
Delta Tau Mini-PMAC

ISA Programmable Multi-Axis Controller



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HARDWARE MANUAL

MINI-PMAC

Programmable Multi-Axis Controller

4Ax-602812-xHxx

September 17, 2003

DELTA TAU
Data Systems, Inc.
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All Delta Tau Data Systems, Inc. motion controller products, accessories, and amplifiers contain static sensitive components that can be damaged by incorrect handling. When installing or handling Delta Tau Data Systems, Inc. products, avoid contact with highly insulated materials. Only qualified personnel should be allowed to handle this equipment.

In the case of industrial applications, we expect our products to be protected from hazardous or conductive materials and/or environments that could cause harm to the controller by damaging components or causing electrical shorts. When our products are used in an industrial environment, install them into an industrial electrical cabinet or industrial PC to protect them from excessive or corrosive moisture, abnormal ambient temperatures, and conductive materials. If Delta Tau Data Systems, Inc. products are exposed to hazardous or conductive materials and/or environments, we cannot guarantee their operation.

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INTRODUCTION

The Mini-PMAC is an inexpensive, compact 2-axis version of the PMAC(1) family.

It can be used in a PC ISA slot as a half-sized board (230 mm, 9" long), or it can be used standalone, with serial communications for setup and/or application control.

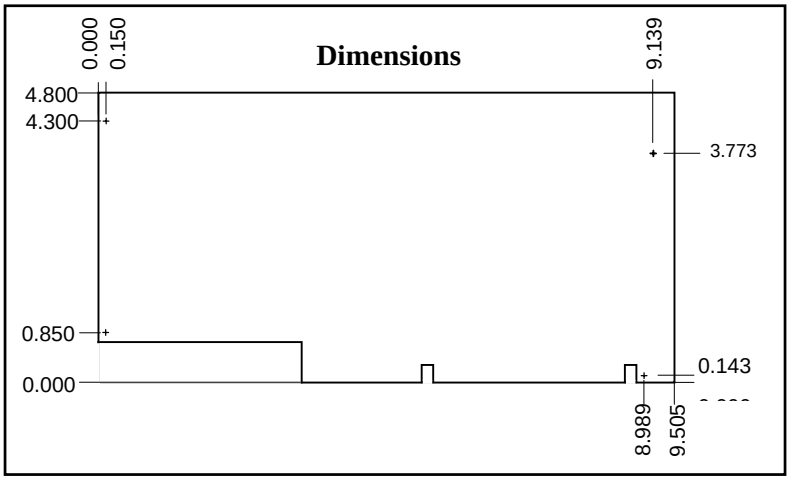
Programs for the Mini-PMAC, both motion and PLC, are 100% compatible with other versions of PMAC. However, there are several features unique to the Mini-PMAC:

1. There are only two output digital-to-analog converters: DAC1 and DAC2 (DAC3 and DAC4 do not exist). Both have differential outputs. The two analog outputs on the Mini-PMAC can be used as velocity or torque commands for separate axes, or as phase current commands for a single axis commutated by the card. However, there are 4 incremental encoder interfaces that can be used for feedback or master positions. Two of these may alternately be used to process analog voltages through optional on-board V/F converters.
2. There is no JPAN control panel port. There are no digital inputs dedicated to the functions of this port on other PMACs. To obtain equivalent functions, general-purpose inputs would have to be used along with a PLC program reading these inputs. Handwheel encoder(s) may be brought in through the JMACH port. WIPER input(s) may be brought in through the JAUX port if option 15 is purchased.
3. The memory mapping of the general-purpose digital I/O is different from other versions of the PMAC. Different M-variable definitions are required for these I/Os on the Mini-PMAC (see below).
4. There is no bus interrupt capability. There is no programmable interrupt controller (PIC) on board. Therefore, it is not possible to read interrupt status registers over the bus in polled format.
5. The serial port is RS-232 only. There is no on-board or optional capability to use RS-422 format. There is no daisychaining capability for a Mini-PMAC with other PMACs of any type on a single serial line.
6. Dual-ported RAM (Option 2M) is an on-board option that must be factory-installed. The Mini-PMAC cannot use the separate Option 2 DPRAM board.
7. The JTHW multiplexer port outputs are not as powerful as on other PMACs. There should be no more than 1 meter (3 ft.) of cable to any device on the port, instead of the 3 meters (10 ft.) on other PMACs. Anything longer should use the ACC-35A driver board.
8. There are no jumpers to control the open-circuit voltage of the complementary inputs. Instead, there are reversible socketed SIP resistor packs. At the factory, these are configured to tie the complementary lines to 2.5V. Reversed, they will tie the complementary lines to 5V.
9. There is no JXIO connector to provide clock signals to mating connectors on ACC-24P or ACC-8D Option 8 boards. If either of these boards is used with the Mini-PMAC, a custom cable should be made to connect the DCLK signal on the Mini-PMAC J7 port to both the DCLK and SCLK inputs on the ACC-24P JXIO port, or the SCLK input on the ACC-8D Option 8 JXIO port.
10. The HMFLn, PLIMn, and MLIMn flag inputs on the Mini-PMAC can accept signals from both sourcing and sinking drivers. If the A+15V on JMACH is used to supply the flag isolators through E89 and E90, only sinking drivers can be used. But, if pin 13 on J8 (JAUX) is used to supply the isolators, a +12V to +24V supply can be used for sinking drivers, or a 0V supply can be used for sourcing drivers.
11. The Mini-PMAC has an interlock circuit that drops out the +/-15V supplies to the analog outputs through a fail-safe relay if any supply on PMAC is lost.

12. If Option 15 is purchased, the Mini-PMAC has the capability for 2 on-board voltage-to-frequency (V/F) converters. These may be used for 2 "Wiper" analog inputs, or to convert the 2 analog outputs to pulse trains for stepper-type drives. The V/F converters can each take an input of 0-10V referenced to AGND. The pulse trains can be tied into encoder channels 3 or 4 for counting. (It is also possible, but more expensive, to use the first two channels of the off-board ACC-8D Option 2 board.)

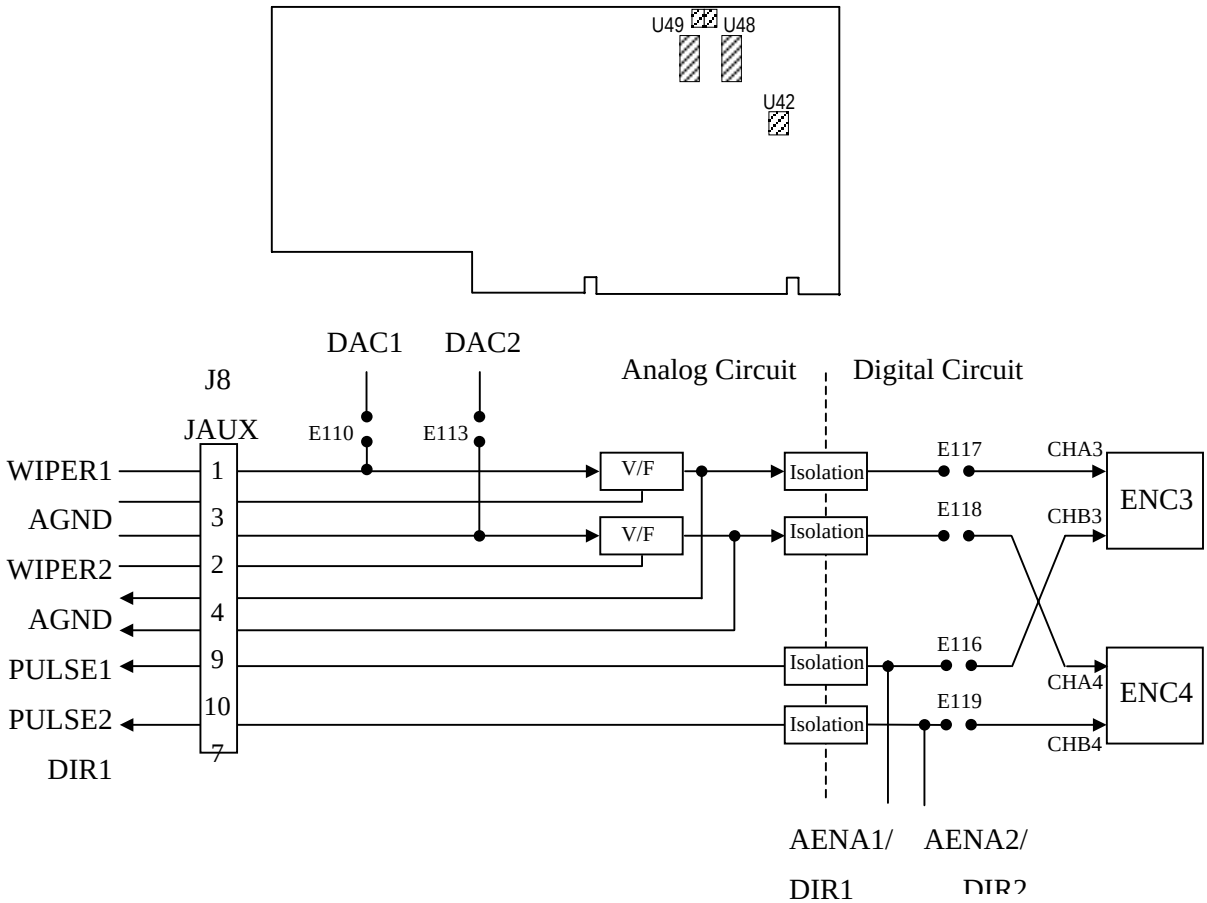
Features

- Motorola DSP 56002 Digital Signal Processor
- 2 output digital-to-analog (DAC) converters
- 4 full encoder channels
- 16 General Purpose I/O, OPTO-22 compatible
- Multiplexer port for expanded I/O
- Overtravel limit, home, fault amplifier enable flags
- Display port for LCD and VFD displays
- Optional on-board dual-ported RAM
- Optional 2 on-board V to F converters
- Optional On-Board Stepper control
- ISA Bus and/or RS-232 Control
- Stand-Alone Operation
- G-Code Command Processing for CNC
- Linear and Circular Interpolation
- 256 motion programs capacity
- Asynchronous PLC program capability
- Rotating buffer for large programs
- 36-bit position range (+/- 64 billion counts)
- 16-bit DAC Output Resolution
- "S-curve" Acceleration and Deceleration
- Cubic Trajectory Calculations, Splines
- Electronic gearing



THE OPTIONAL VOLTAGE TO FREQUENCY CONVERTER

When the Mini-PMAC Option 15 is ordered, the following components are installed on-board at the factory:



Configuration as Analog Input with a 0-100 kHz Frequency Range

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON

Software configuration to be typed on the terminal window:

```
WY$0724,$400722,1280  ;Timebase Encoder Conversion entry for Input #1
WY$0726,$400723,1280  ;Timebase Encoder Conversion entry for Input #2
I910=4                ;Encoder channel 3 for pulse-and-direction decode
                      ; (Input #1)
I915=4                ;Encoder channel 4 for pulse-and-direction decode
                      ; (Input #2)
M34->X:$0725,24       ;Result of the analog conversion. The range of
                      ; M34 is from 0 to the I10 value, proportional to
                      ;the 0-10 Volts range on the analog input #1.
M35->X:$0727,24       ;Result of the analog conversion. The range of
                      ; M35 is from 0 to the ;I10 value, proportional
                      ; to the 0-10 Volts range on the analog input #2.
```

Configuration as Analog Input with a 0-2 MHz Frequency Range

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON
E34 - E37: Encoder Sampling Clock Frequency Control									
E34A	E34	E35	E36	E37	SCLK Clock Frequency				
ON	OFF	OFF	OFF	OFF	19.6608 MHz				

Software configuration to be typed on the terminal window:

```
WY$0724,$40722,64     ;Timebase Encoder Conversion entry for Input #1
WY$0726,$40723,64     ;Timebase Encoder Conversion entry for Input #2
I911=1                ;Encoder 3 digital delay filter disabled
                      ; (bypassed)
I916=1                ;Encoder 4 digital delay filter disabled
                      ; (bypassed)
I910=4                ;Encoder channel 3 for pulse-and-direction decode
                      ; (Input #1)
I915=4                ;Encoder channel 4 for pulse-and-direction decode
                      ; (Input #2)
M34->X:$0725,24       ;Result of the analog conversion. The range of
                      ; M34 is from 0 to the I10 value, proportional to
                      ; the 0-10 Volts range on the analog input #1.
M35->X:$0727,24       ;Result of the analog conversion. The range of
                      ; M35 is from 0 to the I10 value, proportional to
                      ; the 0-10 Volts range on the analog input #2.
```

General Configuration for Step and Direction Outputs

- Set the appropriate jumpers as shown in the diagrams below.
- Wire the PULSEn and AENAn/DIRn open-collector outputs on the JAUX connector to the stepper drive inputs, with AGND as the reference.
- Tie the DACn output to the WIPERn input by putting the jumper ON.
- Select the desired frequency range with the two jumpers for the channel.
- If true open-loop operation is desired, tie the PULSEn output to the CHAm input with the jumper, and tie the AENAn/DIRn output to the CHBm input; otherwise leave these jumpers OFF.
- If true open-loop operation is desired, set up the encoder channel for pulse-and-direction decode by setting I910 or I915 to 4; otherwise, use as normal for real encoder feedback.
- If true open-loop operation is desired and the 0-2 MHz frequency range is selected, set I911=1 or I916=1. This will disable the digital delay filter for Encoder 3 or Encoder 4, respectively.
- Put the PMAC output channel in magnitude-and-direction mode by setting bit 16 of Ix02 to 1, and bit 16 of Ix25 to 1
- Choose the appropriate simulated or real encoder for the motor's feedback loop by setting Ix03 and Ix04 to the address in the conversion table of the proper encoder channel. Assuming the default conversion table, the value is $0720 for ENC1, $0721 for ENC2, $0722 for ENC3, and $0723 for ENC4.
- If the simulated feedback is used, set Ix30 to 550,000 for 100 kHz max.; or Ix30 to 27,500 for 2 MHz max. Set Ix31 to 0, Ix32 to 1000, Ix33 to 0, and Ix35 to 0. If real feedback is used, tune the motor as you would for a velocity-mode amplifier.

Jumper configuration for step and direction output 0-100 kHz frequency range and pseudo-feedback (no external encoder connected).

Jumpers Setting									
Input 1					**Input 2**				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

Jumper configuration for step and direction output 0-2 MHz frequency range and pseudo-feedback (no external encoder connected).

Jumpers Setting									
Input 1					**Input 2**				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON
E34 - E37: Encoder Sampling Clock Frequency Control									
E34A	E34	E35	E36	E37	SCLK Clock Frequency				
ON	OFF	OFF	OFF	OFF	19.6608 MHz				

Jumper configuration for step and direction output 0-100 kHz frequency range and external encoder feedback connected.

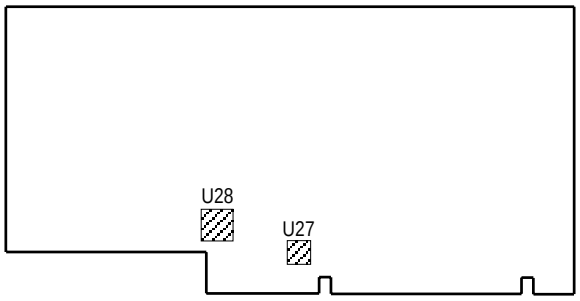
Jumpers Setting									
Input 1					**Input 2**				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF

Jumper configuration for step and direction output, 0-2 MHz frequency range and external encoder feedback connected.

Jumpers Setting									
Input 1					**Input 2**				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF

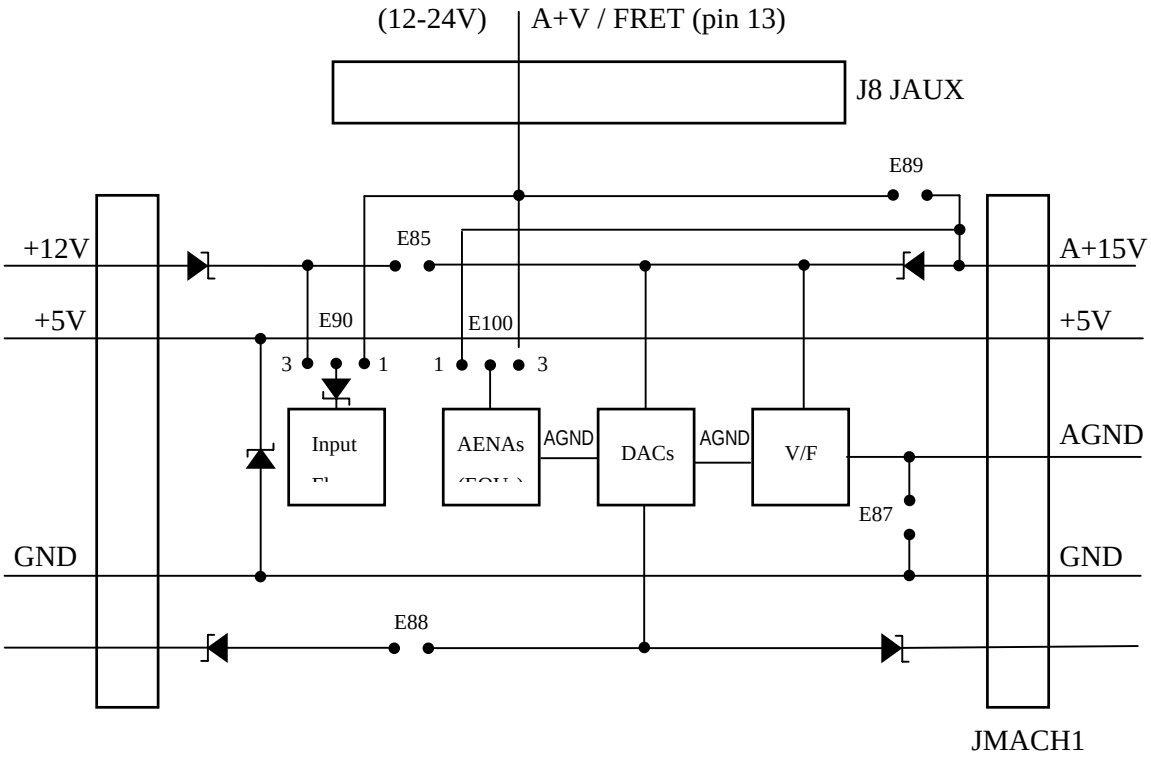
THE OPTIONAL DUAL-PORTED RAM

When the Mini-PMAC Option 2 is ordered, the following components are installed on-board at the factory:



See the PMAC Dual-Ported RAM User's Manual for more information.

MINI-PMAC(1) ANALOG & FLAG POWER SUPPLY



INPUT AND OUTPUT MAPPING (MINI-PMAC ONLY)

Y:$FFC0 J1 (JDISP) Outputs

0	DB0	Display Data0	(J1-8)
1	DB1	Display Data1	(J1-7)
2	DB2	Display Data2	(J1-10)
3	DB3	Display Data3	(J1-9)
4	DB4	Display Data 4	(J1-12)
5	DB5	Display Data 5	(J1-11)
6	DB6	Display Data 6	(J1-14)
7	DB7	Display Data 7	(J1-13)

Y:$FFC1 J3 (JTHW) Inputs

0	DAT0	THW DATA 0	(J3-3)
1	DAT1	THW DATA 1	(J3-5)
2	DAT2	THW DATA 2	(J3-7)
3	DAT3	THW DATA 3	(J3-9)
4	DAT4	THW DATA 4	(J3-11)
5	DAT5	THW DATA 5	(J3-13)
6	DAT6	THW DATA 6	(J3-15)
7	DAT7	THW DATA 7	(J3-17)

Y:$FFC2 J3 (JTHW) Outputs

0	SEL0	THW SELECT 0	(J3-4)
1	SEL1	THW SELECT 1	(J3-6)
2	SEL2	THW SELECT 2	(J3-8)
3	SEL3	THW SELECT 3	(J3-10)
4	SEL4	THW SELECT 4	(J3-12)
5	SEL5	THW SELECT 5	(J3-14)
6	SEL6	THW SELECT 6	(J3 16)
7	SEL7	THW SELECT 7	(J3 18)

Y:$FFC3 J5 (JOPTO) Inputs

0	MI1	MACHINE INPUT 1	(J5-15)
1	MI2	MACHINE INPUT 2	(J5-13)
2	MI3	MACHINE INPUT 3	(J5-11)
3	MI4	MACHINE INPUT 4	(J5-9)
4	MI5	MACHINE INPUT 5	(J5-7)
5	MI6	MACHINE INPUT 6	(J5-5)
6	MI7	MACHINE INPUT 7	(J5-3)
7	MI8	MACHINE INPUT 8	(J5-1)

Y:$FFC4 J5 (JOPTO) Outputs

0	MO1	MACHINE OUTPUT 1 (J5-31)
1	MO2	MACHINE OUTPUT 2 (J5-29)
2	MO3	MACHINE OUTPUT 3 (J5-27)
3	MO4	MACHINE OUTPUT 4 (J5-25)
4	MO5	MACHINE OUTPUT 5 (J5-23)
5	MO6	MACHINE OUTPUT 6 (J5-21)
6	MO7	MACHINE OUTPUT 7 (J5-19)
7	MO8	MACHINE OUTPUT 8 (J5-17)

Y:$FFC5 Dedicated Use

0	ENA422	Serial Enable
1	RS	Display Control
2	R/W	Display Control
3	E	Display Control
4	E44	Jumper E44
5	E45	Jumper E45
6	E46	Jumper E46
7	E47	Jumper E47

Y:$FFC6 Dedicated Use

0	E48	Jumper E48
1	E49	Jumper E49
2	E50	Jumper E50
3	E51	Jumper E51
4	PWR_GUD-	Power Supply Detect
5	(Reserved for future use)	
6	(Reserved for future use)	
7	(Reserved for future use)	

LED INDICATORS

The Mini-PMAC has four LED indicators.

D1 (green)	When the green LED is lit, this indicates that power is applied to the +5V input.
D2 (red)	When the red LED is lit, this indicates that the watchdog timer has tripped and shut down the PMAC.
D3 (yellow)	The yellow LED located beside the red and green LEDs, when lit, indicates that the phase-locked loop that multiplies the CPU clock frequency from the crystal frequency on the Option CPU is operational and stable. This indicator is for diagnostic purposes only.
D15 (green)	The Mini-PMAC has an interlock circuit that drops out the +/-15V supplies to the analog outputs through a fail-safe relay if any supply on PMAC is lost. In this case, the green LED D15 will be off.

SUGGESTED I/O M-VARIABLE DEFINITIONS (MINI-PMAC ONLY)

General Purpose Inputs and Outputs (Mini-PMAC only)

```
M1->Y:$FFC4,0,1             ; Machine Output 1
M2->Y:$FFC4,1,1             ; Machine Output 2
M3->Y:$FFC4,2,1             ; Machine Output 3
M4->Y:$FFC4,3,1             ; Machine Output 4
M5->Y:$FFC4,4,1             ; Machine Output 5
M6->Y:$FFC4,5,1             ; Machine Output 6
M7->Y:$FFC4,6,1             ; Machine Output 7
M8->Y:$FFC4,7,1             ; Machine Output 8
M9->Y:$FFC4,0,8,U           ; Machine Outputs 1-8 treated as byte
M11->Y:$FFC3,0,1            ; Machine Input 1
M12->Y:$FFC3,1,1            ; Machine Input 2
M13->Y:$FFC3,2,1            ; Machine Input 3
M14->Y:$FFC3,3,1            ; Machine Input 4
M15->Y:$FFC3,4,1            ; Machine Input 5
M16->Y:$FFC3,5,1            ; Machine Input 6
M17->Y:$FFC3,6,1            ; Machine Input 7
M18->Y:$FFC3,7,1            ; Machine Input 8
M19->Y:$FFC3,0,8,U          ; Machine Inputs 1-8 treated as byte
```

Thumbwheel Port Bits (Can be Used as General-Purpose I/O)

(These definitions are valid for Mini-PMAC only)

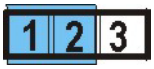
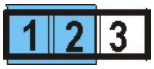
```
M40->Y:$FFC2,0,1            ; SEL0 Output
M41->Y:$FFC2,1,1            ; SEL1 Output
M42->Y:$FFC2,2,1            ; SEL2 Output
M43->Y:$FFC2,3,1            ; SEL3 Output
M44->Y:$FFC2,4,1            ; SEL4 Output
M45->Y:$FFC2,5,1            ; SEL5 Output
M46->Y:$FFC2,6,1            ; SEL6 Output
M47->Y:$FFC2,7,1            ; SEL7 Output
M48->Y:$FFC2,0,8,U          ; SEL0-7 Outputs treated as a byte
M50->Y:$FFC1,0,1            ; DAT0 Input
M51->Y:$FFC1,1,1            ; DAT1 Input
M52->Y:$FFC1,2,1            ; DAT2 Input
M53->Y:$FFC1,3,1            ; DAT3 Input
M54->Y:$FFC1,4,1            ; DAT4 Input
M55->Y:$FFC1,5,1            ; DAT5 Input
M56->Y:$FFC1,6,1            ; DAT6 Input
M57->Y:$FFC1,7,1            ; DAT7 Input
M58->Y:$FFC1,0,8,U          ; DAT0-7 Inputs treated as a byte
```

E-POINT JUMPER DESCRIPTIONS

E1 - E2: Machine Output Supply Voltage Configure

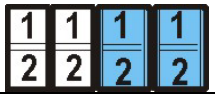
WARNING

The jumper setting must match the type of driver IC, or damage to the IC will result.

E-Point & Physical Layout	Location	Description	Default
E1 		Jump pin 1 to 2 to apply +V (+5V to 24V) to pin 11 of "U30" (should be ULN2803A for sink output configuration). JOPTO "MACHINE" outputs M01-M08. Jump pin 2 to 3 to apply GND to pin 11 of "U30" (should be UDN2981A for source output configuration). Also, see E2.	1-2 Jumper installed
E2 		Jump pin 1 to 2 to apply GND to pin 10 of "U30" (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply +V (+5V to 24V) to pin 10 of "U30" (should be UDN2981A for source output configuration). Also, see E1.	1-2 Jumper installed

E3 - E6: Servo Clock Frequency Control

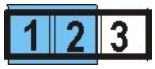
The servo clock (which determines how often the servo loop is closed) is derived from the phase clock (see E29 - E33 and E98) through a "divide-by-N" counter. Jumpers E3 through E6 control this dividing function.

E3	E4	E5	E6	Servo Clock Frequency	Default & Physical Layout E3 E4 E5 E6 
ON	ON	ON	ON	= Phase Clock Divided by 1	
OFF	ON	ON	ON	= Phase Clock Divided by 2	
ON	OFF	ON	ON	= Phase Clock Divided by 3	
OFF	OFF	ON	ON	= Phase Clock Divided by 4	Only E5 and E6 On
ON	OFF	ON	ON	= Phase Clock Divided by 5	
OFF	ON	OFF	ON	= Phase Clock Divided by 6	
ON	OFF	OFF	ON	= Phase Clock Divided by 7	
OFF	OFF	OFF	ON	= Phase Clock Divided by 8	
ON	ON	ON	OFF	= Phase Clock Divided by 9	
OFF	ON	ON	OFF	= Phase Clock Divided by 10	
ON	OFF	ON	OFF	= Phase Clock Divided by 11	
OFF	OFF	ON	OFF	= Phase Clock Divided by 12	
ON	ON	OFF	OFF	= Phase Clock Divided by 13	
OFF	ON	OFF	OFF	= Phase Clock Divided by 14	
ON	OFF	OFF	OFF	= Phase Clock Divided by 15	
OFF	OFF	OFF	OFF	= Phase Clock Divided by 16	

The setting of I-Variable I10 should be adjusted to match the servo interrupt cycle time set by E98, E3–E6, E29–E33, and the master clock frequency. I10 holds the length of a servo interrupt cycle, scaled so that 8,388,608 equals one millisecond. Since I10 has a maximum value of 8,388,607, the servo interrupt cycle time should always be less than a millisecond (unless you want to make your basic unit of time on PMAC something other than a millisecond). If you wish a servo sample time for a motor of greater than one millisecond, the sampling may be slowed in software for that motor with variable Ix60.

Approximate servo frequency may be measured by typing successive “RX0” commands in a PMAC terminal window to read the servo cycle counter, with the carriage return characters for the two commands hit exactly ten seconds apart. To obtain the servo frequency in kHz, take the difference of the two responses and divide by 10,000.

E7: Machine Input Source/Sink Control

E-Point & Physical Layout	Location	Description	Default
E7 		Jump pin 1 to 2 to apply +5V to input reference resistor sip pack; this will bias MI1 to MI8 inputs to +5V for "OFF" state; input must then be grounded for "ON" state. Jump pin 2 to 3 to apply GND to input reference resistor sip pack; this will bias MI1 to MI8 inputs to GND for "OFF" state; input must then be pulled up for "ON" state (+5V to +24V).	1-2 Jumper installed

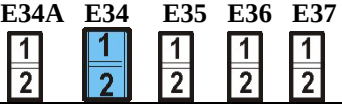
E17A-E17D: Amplifier-Enable/Direction Polarity Control

E-Point & Physical Layout	Location	Description	Default
E17A 		Jump 1-2 for high TRUE AENA1. Remove jumper for low TRUE AENA1	No jumper installed
E17B 		Jump 1-2 for high TRUE AENA2. Remove jumper for low TRUE AENA2	No jumper installed
E17C 		Jump 1-2 for high TRUE AENA1. Remove jumper for low TRUE AENA1	No jumper installed
E17D 		Jump 1-2 for high TRUE AENA2. Remove jumper for low TRUE AENA2	No jumper installed
Low-true enable is the fail-safe option with the default sinking (open-collector) ULN2803A output driver IC in U50. If U50 is replaced with a UDN2981A sourcing driver IC (and E101 and E102 are changed), high-true enable is the fail-safe option.			

E29 - E33: Phase Clock Frequency Control

E29	E30	E31	E32	E33	E33A	Phase Clock Freq. E98@1-2	Phase Clock Freq. E98@2-3	Default & Physical Layout
ON	OFF	OFF	OFF	OFF	OFF	2.26 kHz	1.13 kHz	
OFF	ON	OFF	OFF	OFF	OFF	4.52 kHz	2.26 kHz	E31 ON
OFF	OFF	ON	OFF	OFF	OFF	9.04 kHz	4.52 kHz	
OFF	OFF	OFF	ON	OFF	OFF	18.07 kHz	9.04 kHz	
OFF	OFF	OFF	OFF	ON	OFF	36.14 kHz	18.07 kHz	
OFF	OFF	OFF	OFF	OFF	ON	72.28 kHz	36.14 kHz	
Jumpers E29 through E33A control the speed of the phase clock, and, indirectly, the servo clock, which is divided down from the phase clock (see E3 - E6). No more than 1 of these 6 jumpers may be on at a time.								

E34 - E37: Encoder Sampling Clock Frequency Control

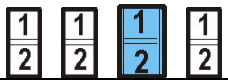
E34A	E34	E35	E36	E37	SCLK Clock Frequency 19.6608 MHz Master Clock	Default & Physical Layout E34A E34 E35 E36 E37 
ON	OFF	OFF	OFF	OFF	19.6608 MHz	
OFF	ON	OFF	OFF	OFF	9.8304 MHz	E34 On
OFF	OFF	ON	OFF	OFF	4.9152 MHz	
OFF	OFF	OFF	ON	OFF	2.4576 MHz	
OFF	OFF	OFF	OFF	ON	1.2288 MHz	

Jumpers E34 - E37 control the encoder-sampling clock (SCLK) used by the gate array ICs. No more than 1 of these 5 jumpers may be on at a time.

E39: Reset-From-Bus Enable

E-Point & Physical Layout	Location	Description	Default
E39 		Jump pin 1 to 2 to allow Mini-PMAC to derive its reset from the PC backplane. Remove jumper to allow Mini-PMAC to power up in normal way; PCbus hardware reset will not reset Mini-PMAC; also not needed for standalone operation.	No jumper

E44 - E47: Communications Control

Baud Rate Control "E" Points				Baud Rate			Default & Physical Layout
E44	E45	E46	E47	20 MHz Flash CPU (OPT 4A)	Standard CPU, 40 MHz Flash CPU (Opt 5A)	60 MHz Flash CPU (Opt 5B)	E44 E45 E46 E47 
ON	ON	ON	ON	Disabled	Disabled	Disabled	
OFF	ON	ON	ON	300	600	900	
ON	OFF	ON	ON	400*	800*	1200	
OFF	OFF	ON	ON	600	1200	1800	
ON	ON	OFF	ON	800*	1600*	2400	
OFF	ON	OFF	ON	1200	2400	3600	
ON	OFF	OFF	ON	1600*	3200*	4800	
OFF	OFF	OFF	ON	2400	4800	7200	
ON	ON	ON	OFF	3200*	6400*	9600	Opt 5B
OFF	ON	ON	OFF	4800	9600	14400	Standard, Opt 5A
ON	OFF	ON	OFF	6400*	12800*	19200	
OFF	OFF	ON	OFF	9600	19200	28800	Opt 4A
ON	ON	OFF	OFF	12800*	25600*	38400	
OFF	ON	OFF	OFF	19200	38400	57600	
ON	OFF	OFF	OFF	25600*	51200*	76800	
OFF	OFF	OFF	OFF	38400	76800	115200	

Jumpers E44 - E47 control what baud rate to use for serial communications. Any character received over the bus causes PMAC to use the bus for its standard communications. The serial port is disabled if "E"-points E44-E47 are all on.
These jumpers are read only at power-up/reset to set the baud rate at that time.
* Non-standard baud rate

E48: RAM Wait State Control (Standard CPU)

CPU Operational Frequency

E-Point & Physical Layout	Location	Description	Default
E48 		Battery-backed RAM version: Jump pin 1 to 2 for zero wait-state RAM operation; remove jumper for one wait-state RAM access. Flash-backed RAM version: Jump pin 1 to 2 for 60 MHz CPU operation; remove jumper for 40 MHz CPU operation; don't care on 20 MHz CPU operation	No jumper installed (standard) No jumper installed (Opt 5A); jumper installed (Opt 5B); don't care (Opt 4A).
Note: It may be possible to operate a board with 40 MHz components (Option 5A) at 60 MHz under some conditions by changing the setting of jumper E48. However, this operates the components outside of their specified operating range, and proper execution of PMAC under these conditions is not guaranteed. PMAC software failure is possible under these conditions, and this can lead to very dangerous machine failure. Operation in this mode is done completely at the user's own risk; Delta Tau can accept no responsibility for the operation of PMAC or the machine under these conditions.			

E49: Serial Communications Parity Control

E-Point & Physical Layout	Location	Description	Default
E49 		Jump pin 1 to 2 for NO serial parity; remove jumper for ODD serial parity	Jumper installed

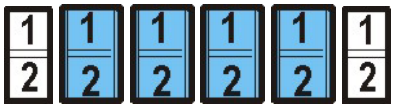
E50: Earom Save Enable/Disable

E-Point & Physical Layout	Location	Description	Default
E50 		Jump pin 1 to 2 to enable save to EAROM or flash memory; remove jumper to disable save to EAROM or flash memory	Jumper installed

E51: Normal/Re-Initializing Power-Up

E-Point & Physical Layout	Location	Description	Default
E51 		Jump pin 1 to 2 to re-initialize on power-up/reset; remove jumper for NORMAL power-up/reset	No jumper installed

E66 - E71: Bus Base Hardware Address

E-Point & Physical Layout	Location	Description	Default
E66 E67 E68 E69 E70 E71 		E66 - Bit 9 PC bus base address E67 - Bit 8 PC bus base address E68 - Bit 7 PC bus base address E69 - Bit 6 PC bus base address E70 - Bit 5 PC bus base address E71 - Bit 4 PC bus base address On = 0 Off = 1	E67-E70 installed
These jumpers work with E91 & E92 to set the base address of Mini-PMAC on the PC bus. See the PC bus addressing below for details on how to set these jumpers.			

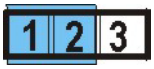
E85, E87, E88: Analog Power Source Configuration

E-Point & Physical Layout	Location	Description	Default
E85 		Jump pin 1 to pin 2 to allow analog +V to come from digital side -- P1 or TB1 -- ties amplifier and Mini-PMAC power supply together, defeats opto-isolation. Remove jumper to keep analog +V separate from digital +12V. **Note:** If E85 is changed, E88 and E87 must also be changed. Also, see E90.	No jumper
E87 		Jump pin 1 to pin 2 to tie analog common AGND to digital common GND -- defeats opto-isolation. Remove jumper to keep AGND and GND separate. **Note:** If E87 is changed, E85 and E88 must also be changed. Also, see E90.	No jumper
E88 		Jump pin 1 to pin 2 to allow analog -V to come from digital side -- P1or TB1 – ties amplifier and Mini-PMAC power supply together, defeats opto-isolation. Remove jumper to keep analog -V separate from digital -12V. **Note:** If E88 is changed, E85 and E87 must also be changed. Also, see E90.	No jumper

E89: Amplifier-Supplied Switch Pull-Up Enable

E-Point & Physical Layout	Location	Description	Default
E89 		Jump pin 1 to 2 to allow "A+V" on J8 (JAUX) pin 13, to tie to "A+15V" on J11 (JMACH1) pin 59. Remove jumper to permit separate voltage supply from A+V for input flags (+12V to +24V for sinking drivers, 0V for sourcing drivers). This jumper must be installed to allow "A+15V" to power the "OPTO" switch sensor inputs (including limits) from the same OPTO-power supply that powers the amplifier output stage. Also, see E90.	Jumper installed

E90: Host-Supplied Switch Pull-Up Enable

E-Point & Physical Layout	Location	Description	Default
E90 		Jump pin 1 to 2 to allow "A+V/FRET" on J8 pin 13 and/or J11 pin 59 (also see E89), to power "OPTO" switch sensor inputs (including limits). Jump pin 2 to 3 to allow "+12V" from DC bus connector P1-pin B09 to power "OPTO" switch sensor inputs (including limits). Optical isolation is then lost. Also, see E85, E87, E88 and PMAC opto-isolation diagram.	1-2 Jumper installed

E91 - E92: Bus Base Address Select (High Bits)

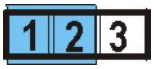
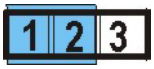
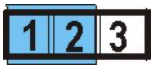
E-Point & Physical Layout	Location	Description	Default
E91 E92 		E91 - Bit 11 PC bus base address E92 - Bit 10 PC bus base address On = 0 Off = 1	Jumper installed
These jumpers work with E66 - E71 to set the base address of Mini-PMAC on the PC bus. See the PC bus addressing below for details on how to set these jumpers.			

E98: DAC/ADC Clock Frequency Control

E-Point & Physical Layout	Location	Description	Default

E98 		Jump 1-2 to provide a 2.45 MHz DCLK signal to DACs and ADCs. Jump 2-3 to provide a 1.23 MHz DCLK signal to DACs and ADCs. Important for high accuracy A/D conversion on ACC-28A boards. **Note:** This also divides the phase and servo clock freq. in half. See E29-E33, E3-E6	1-2 Jumper installed

E101 - E102: Amplifier Enable Output Configure

E-Point & Physical Layout	Location	Description	Default
E100 		Jump pin 1 to 2 to apply A+15V from J11 pin 59 to pin 1 of E101, pin 3 of E102, and FAULT input flag return. This makes U50 AENA/ EQU / PULSE / DIR / FEFCO driver IC work from analog A+15V supply. Jump pin 2 to 3 to apply A+V (12-24V) from J8 pin 13 to pin 1 of E101, pin 3 of E102, and FAULT input flag return. This makes U50 AENA / EQU / PULSE / DIR / FEFCO driver IC work from separate A+V (12-24V) supply. (This cannot be used when A+V is brought from digital side through E85.)	1-2 Jumper installed
E101 		Jump pin 1 to 2 to apply A+15V/A+V (as set by E100) to pin 11 of "U50" AENAn & EQUn driver IC (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply GND to pin 11 of "U50" (should be UDN2981A for source output configuration).	1-2 Jumper installed
E102 		Jump pin 1 to 2 to apply GND to pin 11 of "U50" AENAn & EQUn (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply A+15V/A+V (as set by E100) to pin 11 of "U50" (should be UDN2981A for source output configuration).	1-2 Jumper installed

E103 - E104: CPU/Watchdog Control Jumpers

E-Point & Physical Layout	Location	Description	Default
E103 		Jump pin 1 to 2 to disable Watchdog timer (for test purposes only.). Remove jumper to enable Watchdog timer.	No jumper installed
E104 		Jump pin 1 to 2 to BOOT from host port. Remove jumper to BOOT from PROM IC (normal operation).	No jumper installed
E105 	Present on -102 and newer boards only	Jump pin 1 to 2 to program on-board logic (for factory use only). Remove jumper for normal operation of board	No jumper installed

E110 - E115: V/F Converter Configuration

(Voltage-to-Frequency Converter Option [OPT 15] Required)

E-Point & Physical Layout	Location	Description	Default
E110 		Jump pin 1 to 2 to tie DAC1 output to WIPER1 input. Remove jumper to keep lines separate.	No jumper installed
E111 		Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 1st V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 1st V/F converter.	No jumper installed
E112 		Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 1st V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 1st V/F converter.	No jumper installed
E113 		Jump pin 1 to 2 to tie DAC2 output to WIPER2 input. Remove jumper to keep lines separate.	No jumper installed
E114 		Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 2nd V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 2nd V/F converter.	No jumper installed
E115 		Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 2nd V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 2nd V/F converter.	No jumper installed

E116 - E119: V/F Converter Configuration

(Voltage-to-Frequency Converter Option [OPT 15] Required)

E-Point & Physical Layout	Location	Description	Default
E116 		Jump pin 1 to 2 to tie AENA1/DIR1 output to CHB3 input Remove jumper to keep lines separate.	No jumper installed
E117 		Jump pin 1 to 2 to tie PULSE1 output to CHA3 input Remove jumper to keep lines separate.	No jumper installed
E118 		Jump pin 1 to 2 to tie PULSE2 output to CHA4 input Remove jumper to keep lines separate.	No jumper installed
E119 		Jump pin 1 to 2 to tie AENA2/DIR2 output to CHB4 input Remove jumper to keep lines separate.	No jumper installed

HOST PC-AT I/O ADDRESS MAP

Hex Range	Dec Range	Usage
000-01F	0-31	DMA Controller 1 8237A-5
020-03F	32-63	Interrupt Controller 1 8259A
040-05F	64-67	Timer 8254-2
060-06F	96-111	8042 (Keyboard)
070-07F	112-127	Real-time clock, NMI mask
080-09F	128-159	DMA Page Registers
0A0-0BF	160-191	Interrupt Controller 2 8259A
0C0-0DF	192-223	DMA Controller 2 8237A-5
0F0-0FF	240-255	Math CO processor
1F0-1F8	496-504	Fixed Disk
200-20F	512-527	Game Control
210-217	528-535	Expansion Unit (usually open)
278-27F	632-639	Parallel Printer: LPT2
2B0-2DF	688-735	Alternate EGA
2F8-2FF	760-767	Asynchronous Common: COM2
300-31F	768-799	Prototype Card (usually open)
360-36F	864-879	PC Network
378-37F	888-895	Parallel Printer: LPT1
380-38F	896-911	SDLC Communications 2
390-393	912-915	Cluster
3A0-3A9	928-937	SDLC Communications 1
3B0-3BF	944-959	IBM Monochrome Display/Printer
3C0-3CF	960-975	Enhanced Graphics Adapter
3D0-3DF	976-991	Color/Graphics
3F0-3F7	1000-1015	Diskette Controller
3F8-3FF	1016-1023	Asynchronous Common: COM1
x2E1		GPIB Adapter
x390-x393		Cluster Adapter
It is highly recommended that the above address space segment not be used for Mini-PMAC host base address unless the "Usage" column indicates "Usually Open."		

MINI-PMAC JUMPER BUS ADDRESS SETUP

Jumpers E91, E92, E66, E67, E68, E69, E70, and E71 on the Mini-PMAC determine the base address of the card in the I/O space of the host PC's expansion bus. Together, they form a binary number that specifies the 16 consecutive addresses on the bus where the card can be found.

The jumpers form the base address in the following fashion:

Jumper	E91	E92	E66	E67	E68	E69	E70	E71
Bit #	11	10	9	8	7	6	5	4
Dec Value	2048	1024	512	256	128	64	32	16
Hex Value	800	400	200	100	80	40	20	10

If a jumper is ON, the value it contributes to the base address is ZERO.

If a jumper is OFF, the value it contributes to the base address is given in the table above.

On both the PMAC-PC and the PMAC-Lite, the jumpers are physically arranged in the same order that they are presented in the above table.

From Jumper Configuration to Address

To determine the address specified by a given jumper configuration, use the following formula:

(Decimal)

Address = 2048*E91 + 1024*E92 + 512*E66 + 256*E67 + 128*E68 + 64*E69 + 32*E70 + 16*E71

(Hexadecimal)

Address = $800*E91 + $400*E92 + $200*E66 + $100*E67 + $80*E68 + $40*E69 + $20*E70 + $10*E71

In each case, Exx = 1 if the jumper is OFF; Exx = 0 if the jumper is ON.

Example: On a PMAC card, the jumpers are in the following configuration:

E91	E92	E66	E67	E68	E69	E70	E71
ON	ON	OFF	OFF	ON	ON	ON	ON

The address can be computed as:

Decimal Address = 0 + 0 + 512 + 256 + 0 + 0 + 0 + 0 = 768
Hex Address = 0 + 0 + $200 + $100 + 0 + 0 + 0 + 0 = $300

From Address to Jumper Configuration

Once an I/O address on the PC expansion port has been selected, the following procedure can be used for setting the address jumpers:

1. Convert the address to a 3-digital hexadecimal value ($000 to $FFF, representing 0 to 4095). If the value does not fit in this range, you will not be able to set PMAC for this address. Make sure the last digit is 0; only addresses divisible by 16 are permitted as PMAC base addresses.

2. Take the first hex digit and convert it to binary. The binary digits represent bits 11 through 8 of the base address. Assign each binary digit to jumpers as follows:

Bit #	11(MSB)	10	9	8(LSB)
Jumper	E91	E92	E66	E67
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

3. Take the second hex digit and convert it to binary. The binary digits represent bits 7 through 4 of the base address. Assign each binary digit to jumpers as follows:

Bit #	7(MSB)	6	5	4(LSB)
Jumper	E68	E69	E70	E71
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

Example: You wish to set up the card to be at base address 992 decimal on the PC expansion bus.

1. 992 decimal is equal to 3E0 hexadecimal
2. The first digit of 3 is binary 0011. This sets E91 ON, E92 ON, E66 OFF, E67 OFF.
3. The second digit of E is binary 1110. This sets E68 OFF, E69 OFF, E70 OFF, E71 OFF.

MINI-PMAC MATING CONNECTORS

This section lists several options for each connector. Choose an appropriate one for your application. (See attached "PMAC mating connector" sketch for typical connection.)

J1 (JDISP)/Display Port

1. 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0
   Qty. 2 - T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley stan. flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J3 (JTHW)/Multiplexer Port

1. 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 qty. 2 - T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley stan. flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J4 (JRS232)/Serial Communications

1. 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 qty. 2 - T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley stan. flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J5 (JOPT)/OPTO I/O

1. 34-pin female flat cable connector Delta Tau P/N 014-R00F34-0K0 qty. 2 - T&B Ansley P/N 609-3441
2. 171-34 T&B Ansley stan. flat cable stranded 34 wire
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J7 (JS1)/A-D Inputs 1-4

1. 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 qty. 2 - T&B Ansley P/N 609-1641-16
2. 171-16 T&B Ansley stan. flat cable stranded 16 wire
3. PHOENIX varioface module type FLKM 16 (male pins) P/N 22 81 03 4

J8 (JAUX)/Auxiliary I/O

1. 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 qty. 2 - T&B Ansley P/N 609-1641-16
2. 171-16 T&B Ansley stan. flat cable stranded 16 wire
3. PHOENIX varioface module type FLKM 16 (male pins) P/N 22 81 03 4

J9 (JEXP)/Expansion

1. 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0 qty. 2 - T&B Ansley P/N 609-5041
2. 171-50 T&B Ansley stan. flat cable stranded 50-wire
3. Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9 used for daisy chaining acc-14 I/0, -23 A and D connectors -24 expansion

J11 (JMACH)/Machine Connector

1. 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0 qty. 2 - T&B Ansley P/N 609-6041 available as ACC 8P or 8D
2. 171-60 T&B Ansley stan. flat cable stranded 60 wire

3. Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note

Normally, J11 is used with ACC-8P or 8D with Option P, which provides complete terminal strip fan-out of all connections.

TB1 (JPWR)

1. 4-pin terminal block

P1 (PC BUS)

62-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000F62-SCO qty. 1 Viking P/N 3KH 31/9 JN12 card edge connection Pierced solder eyelets.

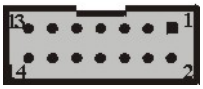
P2 (AT BUS)

36-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000 F36-SCO qty.1 Viking P/N 3KH 18/9 JN12 card edge connection Pierced solder eyelets.

CONNECTOR PINOUTS

Headers

J1 JDISP (14-Pin Header)

Front View 

Pin #	Symbol	Function	Description	Notes
1	Vdd	Output	+5V Power	Power Supply Out
2	Vss	Common	PMAC Common	
3	Rs	Output	Read Strobe	TTL Signal Out
4	Vee	Output	Contrast Adjust. VEE	0 to +5 VDC *
5	E	Output	Display Enable	High is Enable
6	R/W	Output	Read or Write	TTL Signal Out
7	DB1	Output	Display Data 1	
8	DB0	Output	Display Data 0	
9	DB3	Output	Display Data 3	
10	DB2	Output	Display Data 2	
11	DB5	Output	Display Data 5	
12	DB4	Output	Display Data 4	
13	DB7	Output	Display Data 7	
14	DB6	Output	Display Data 6	

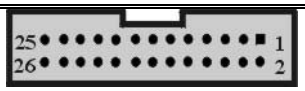
The JDISP connector is used to drive the 2 line x 24 character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (ACC. 12C) display unit. The DISPLAY command may be used to send messages and values to the display.

See Also:

Program Commands; DISPLAY
Accessories; ACC-12, ACC16D
Memory Map; Y:$0780 - $07D1

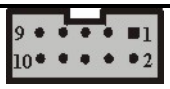
Note: There is no J2 (JPAN) control panel connector on Mini-PMAC.

* Controlled by potentiometer R4

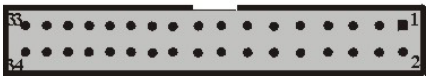
J3 JTHW (26-Pin Header)			**Front View** 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data Input from Thumbwheel Switches
4	SEL0	Output	Select-0 Output	Scanner Output for reading TW Switches
5	DAT1	Input	Data-1 Input	Data Input from Thumbwheel Switches
6	SEL1	Output	Select-1 Output	Scanner Output for reading TW Switches
7	DAT2	Input	Data-2 Input	Data Input from Thumbwheel Switches
8	SEL2	Output	Select-2 Output	Scanner Output for reading TW Switches
9	DAT3	Input	Data-3 Input	Data Input from Thumbwheel Switches
10	SEL3	Output	Select-3 Output	Scanner Output for reading TW Switches
11	DAT4	Input	Data-4 Input	Data Input from Thumbwheel Switches
12	SEL4	Output	Select-4 Output	Scanner Output for reading TW Switches
13	DAT5	Input	Data-5 Input	Data Input from Thumbwheel Switches
14	SEL5	Output	Select-5 Output	Scanner Output for reading TW Switches
15	DAT6	Input	Data-6 Input	Data Input from Thumbwheel Switches
16	SEL6	Output	Select-6 Output	Scanner Output for reading TW Switches
17	DAT7	Input	Data-7 Input	Data Input from Thumbwheel Switches
18	SEL7	Output	Select-7 Output	Scanner Output for reading TW Switches
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	N.C.	N.C.	No Connection	
22	GND	Common	PMAC Common	
23	N.C.	N.C.	No Connection	
24	GND	Common	PMAC Common	
25	+5V	Output	+5Vdc Supply	Power Supply Out
26	INIT/	Input	PMAC Reset	Low is "Reset"

The JTHW multiplexer port provides eight inputs and eight outputs at TTL levels. While these I/O can be used in unmultiplexed form for 16 discrete I/O points, most users will utilize PMAC software and accessories to use this port in multiplexed form to greatly multiply the number of I/O that can be accessed on this port. In multiplexed form, some of the SELn outputs are used to select which of the multiplexed I/O are to be accessed.
See also:

I/O and Memory Map Y:$FFC1, Y:$FFC2
Suggested M-variables M40 - M58
M-variable formats TWB, TWD, TWR, TWS
ACC-8D Opt 7, ACC-8D Opt 9, ACC-18, ACC-34x, NC Control Panel

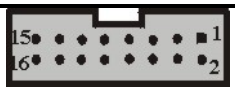
J4 JRS232 (10-Pin Header)			**Front View** 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	N.C.		No Connect	
2	DTR	Bidirectional	Data Term Ready	Tied to "DSR"
3	TXD/	Input	Receive Data	Host Transmit Data
4	CTS	Input	Clear to Send	Host Ready Bit
5	RXD/	Output	Send Data	Host Receive Data
6	RTS	Output	Request to Send	PMAC Ready Bit
7	DSR	Bidirectional	Data set Ready	Tied to "DTR"
8	N.C.		No Connect	
9	GND	Common	PMAC Common	
10	+5V	Output	+5VDC Supply	Power Supply Out
The JRS232 connector provides the Mini-PMAC with the ability to communicate serially with an RS232 port. This connector cannot be used for daisychain interconnection of multiple PMAC's See Also: Serial Communications				

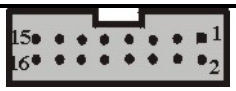
J5 JOPT (34-Pin Connector)

Front View 

Pin #	Symbol	Function	Description	Notes
1	MI8	Input	Machine Input 8	Low is true
2	GND	Common	PMAC Common	
3	MI7	Input	Machine Input 7	Low is true
4	GND	Common	PMAC Common	
5	MI6	Input	Machine Input 6	Low is true
6	GND	Common	PMAC Common	
7	MI5	Input	Machine Input 5	Low is true
8	GND	Common	PMAC Common	
9	MI4	Input	Machine Input 4	Low is true
10	GND	Common	PMAC Common	
11	MI3	Input	Machine Input 3	Low is true
12	GND	Common	PMAC Common	
13	MI2	Input	Machine Input 2	Low is true
14	GND	Common	PMAC Common	
15	MI1	Input	Machine Input 1	Low is true
16	GND	Common	PMAC Common	
17	MO8	Output	Machine Output 8	If Sinking Out Low True; If Source Out High True
18	GND	Common	PMAC Common	
19	MO7	Output	Machine Output 7	If Sinking Out Low True; If Source Out High True
20	GND	Common	PMAC Common	
21	MO6	Output	Machine Output 6	If Sinking Out Low True; If Source Out High True
22	GND	Common	PMAC Common	
23	MO5	Output	Machine Output 5	If Sinking Out Low True; If Source Out High True
24	GND	Common	PMAC Common	
25	MO4	Output	Machine Output 4	If Sinking Out Low True; If Source Out High True
26	GND	Common	PMAC Common	
27	MO3	Output	Machine Output 3	If Sinking Out Low True; If Source Out High True
28	GND	Common	PMAC Common	
29	MO2	Output	Machine Output 2	If Sinking Out Low True; If Source Out High True
30	GND	Common	PMAC Common	
31	MO1	Output	Machine Output 1	If Sinking Out Low True; If Source Out High True
32	GND	Common	PMAC Common	
33	+V	I/O	+V Power I/O	+V = +5V TO +24V +5V Out from PMAC, +5 to +24V in from external source, Diode Isolation from PMAC
34	GND	Common	PMAC Common	

This connector provides means for eight general-purpose inputs and eight general-purpose outputs. Inputs and outputs may be configured to accept or provide either +5V or +24V signals. Outputs can be made sourcing with an IC (U11 to UDN2981) and jumper (E1 & E2) change. E7 controls whether the inputs are pulled up or down internally. Outputs are rated to 100mA per line.

J7 JS1 (16- Pin Header)			**Front View** 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	DCLK	Output	D to A, A to D Clock	DAC and ADC Clock for Channel 1, 2, 3, 4
2	BDATA1	Output	D to A Data	DAC Data for Channel 1, 2, 3, 4
3	ASEL0/	Output	Chan. Select Bit 0	Select for Channel 1, 2, 3, 4
4	ASEL1/	Output	Chan. Select Bit 1	Select for Channel. 1, 2, 3, 4
5	CNVRT01	Output	A to D Convert	ADC Convert Sig. Channel 1, 2, 3, 4
6	ADCIN1	Input	A to D Data	ADC Data for Channel 1, 2, 3, 4
7	OUT1/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17)
8	OUT2/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17)
9	OUT3/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17)
10	OUT4/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17)
11	AFLT1+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
12	AFLT2+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
13	AFLT3+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
14	AFLT4+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
15	+5V	Output	+5V Supply	Power Supply Out
16	GND	Common	PMAC Common	
This connector is used to communicate with an Accessory 28 A/D converter board. It can also be used to build a digital amplifier interface. All signals are referenced to the digital common GND.				

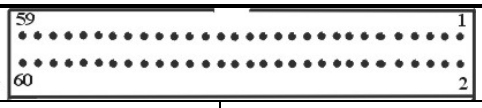
J8 JAUX (16-Pin Header)			**Front View** 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	WIPER1	Input	0-10V Analog Input	1, 2
2	WIPER2	Input	0-10V Analog Input	1, 2
3	AGND	Common	Analog/Flag Common	
4	AGND	Common	Analog/Flag Common	
5	EQU1/	Output	Encoder 1 Position Compare	3
6	EQU2/	Output	Encoder 2 Position Compare	3
7	AENA1/ DIR1	Output	Amp. 1 Enable/Direction	3,4,5
8	AENA2/ DIR2	Output	Amp. 2 Enable/Direction	3,4,5
9	PULSE1	Output	Channel 1 Pulse Command	1,3
10	PULSE2	Output	Channel 2 Pulse Command	1,3
11	FEFCO/	Output	Watchdog Output	3
12	AGND	Common	Analog/Flag Common	
13	A+V/FRET	Input	Flag Supply Volt	6
14	A-15V	I/O	Analog Minus Supply	
15	N.C.		No Connect	
16	N.C.		No Connect	

This connector provides auxiliary signals for the Mini-PMAC, including analog inputs, position compare outputs, pulse-and-direction outputs, and a flag supply/return voltage. All signals are referenced to AGND, isolated from the 5V digital circuitry.

Notes:

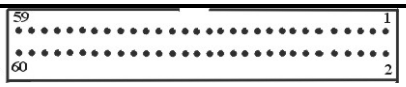
1. Requires Option 15 V/F Converters be installed to use.
2. WIPER1 is tied to DAC1 if jumper E110 is installed; WIPER2 is tied to DAC2 if jumper E113 is installed.
3. Open-collector sinking output in standard configuration (ULN2803A in U50); Can be replaced with sourcing driver (UDN2981A) in U50 socket; 100 mA per point sinking/sourcing capability.
4. Function of this signal determined by Ix02 and Ix25.
5. Can be tied to Encoder 3 or 4 feedback with jumpers (see E111, E112, E114, E115).
6. With jumper E89 ON, tied to A+15V from J11 pin 59; with E89 OFF and E90 at 1-2, can be separate +12V to +24V for input flags (HMFLn, PLIMn, MLIMn) with sinking drivers, or 0V for input flags with sourcing drivers.

J11 JMACH (60-Pin Header)

Top View 

Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For Encoders, 1
2	+5V	Output	+5V Power	For Encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC3	Input	Encoder C Channel Positive	2
6	CHC4	Input	Encoder C Channel Positive	2
7	CHC3/	Input	Encoder C Channel Negative	2,3
8	CHC4/	Input	Encoder C Channel Negative	2,3
9	CHB3	Input	Encoder B Channel Positive	2
10	CHB4	Input	Encoder B Channel Positive	2
11	CHB3/	Input	Encoder B Channel Negative	2,3
12	CHB4/	Input	Encoder B Channel Negative	2,3
13	CHA3	Input	Encoder A Channel Positive	2
14	CHA4	Input	Encoder A Channel Positive	2
15	CHA3/	Input	Encoder A Channel Negative	2,3
16	CHA4/	Input	Encoder A Channel Negative	2,3
17	CHC1	Input	Encoder C Channel Positive	2
18	CHC2	Input	Encoder C Channel Positive	2
19	CHC1/	Input	Encoder C Channel Negative	2,3
20	CHC2/	Input	Encoder C Channel Negative	2,3
21	CHB1	Input	Encoder B Channel Positive	2
22	CHB2	Input	Encoder B Channel Positive	2
23	CHB1/	Input	Encoder B Channel Negative	2,3
24	CHB2/	Input	Encoder B Channel Negative	2,3
25	CHA1	Input	Encoder A Channel Positive	2
26	CHA2	Input	Encoder A Channel Positive	2
27	CHA1/	Input	Encoder A Channel Negative	2,3
28	CHA2/	Input	Encoder A Channel Negative	2,3
29	N.C.		No Connect	
30	N.C.		No Connect	
31	N.C.		No Connect	
32	N.C.		No Connect	
33	EQU1/	Output	Position Compare 1	6
34	EQU2/	Output	Position Compare 2	6
35	N.C.		No Connect	
36	N.C.		No Connect	
37	N.C.		No Connect	
38	N.C.		No Connect	
39	N.C.		No Connect	

J11 JMACH (60-Pin Header) -Continued

Top View 

Pin #	Symbol	Function	Description	Notes
40	N.C.		No Connect	
41	N.C.		No Connect	
42	N.C.		No Connect	
43	DAC1	Output	Analog Out Positive 1	4
44	DAC2	Output	Analog Out Positive 2	4
45	DAC1/	Output	Analog Out Negative 1	4,5
46	DAC2/	Output	Analog Out Negative 2	4,5
47	AENA1/DIR1	Output	Amplifier-Enable/Dir. 1	6
48	AENA2/DIR2	Output	Amplifier-Enable/Dir. 2	6
49	FAULT1	Input	Amplifier-Fault 1	7
50	FAULT2	Input	Amplifier-Fault 2	7
51	MLIM1	Input	Negative End Limit 1	8,9
52	MLIM2	Input	Negative End Limit 2	8,9
53	PLIM1	Input	Positive End Limit 1	8,9
54	PLIM2	Input	Positive End Limit 2	8,9
55	HMFL1	Input	Home-Flag 1	10
56	HMFL2	Input	Home-Flag 2	10
57	FEFCO/	Output	Watchdog Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	
60	A-15V	Input	Analog -15V Supply	

The J11 connector is used to connect PMAC to the servo amps, flags, and encoders.

Notes:

1. In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.
2. Referenced to digital common (GND). Maximum of + 12V permitted between this signal and its complement.
3. If not used, leave this input floating (i.e. digital single-ended encoders).
4. + 10V, 10mA max, referenced to analog common (AGND).
5. Leave floating if not used. Do not tie to AGND. In this case, AGND is the return line.
6. Functional polarity controlled by jumper(s) E17. Sinking/sourcing nature of output control by IC type in U50 socket (default sinking) and E101/E102 configuration. Choice between AENA and DIR use controlled by Ix02 and Ix25.
7. Functional polarity controlled by variable Ix25. Must be conducting to AGND (sinking driver) to produce a '0' in PMAC software. Pull-up is to A+15V or A+V (12-24V) as determined by E100. Automatic fault function can be disabled with Ix25.
8. Pins marked PLIMn should be connected to switches at the positive end of travel. Pins marked MLIMn should be connected to switches at the negative end of travel.
9. Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.
10. Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

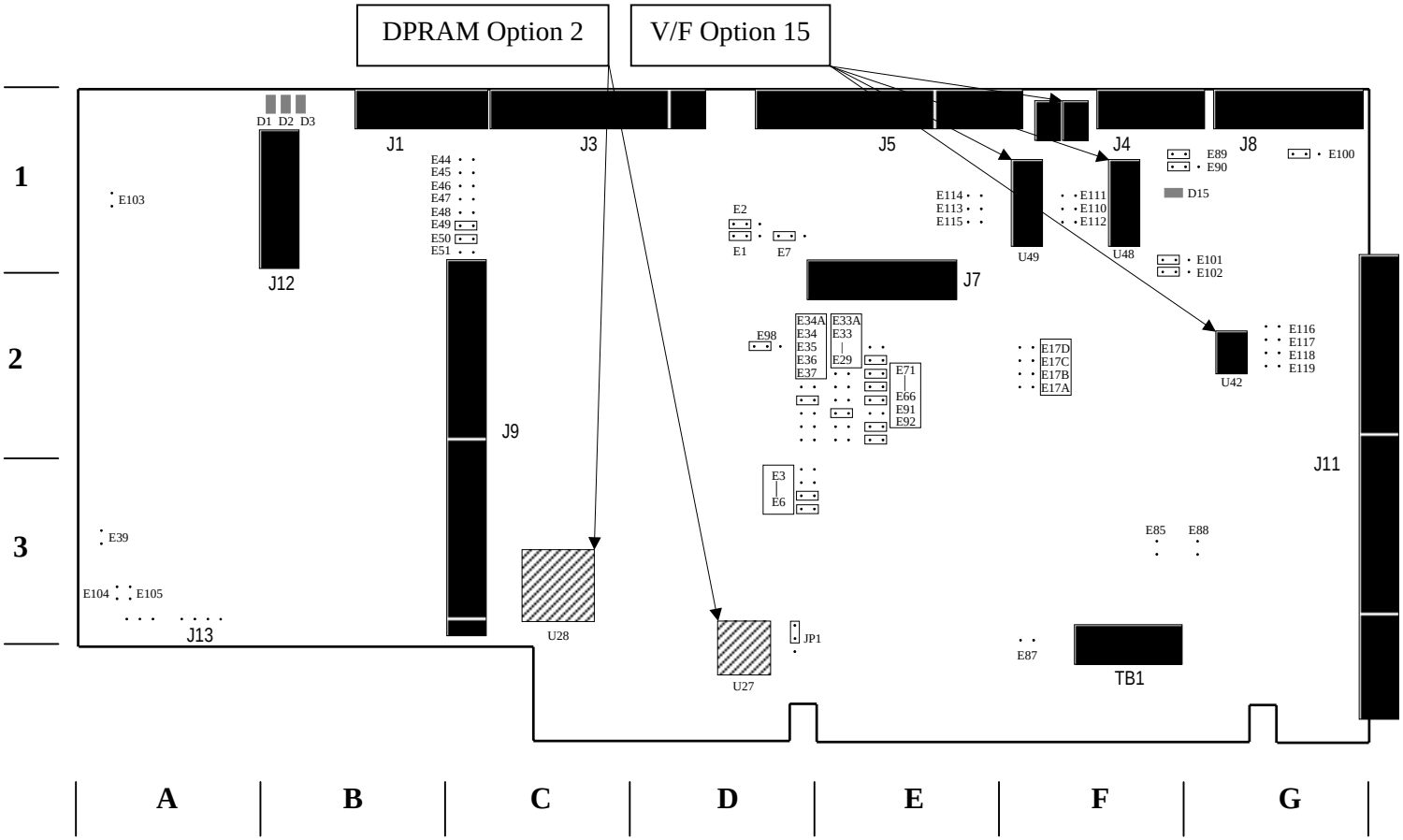
Terminal Block

TB1 (JPWR) (4-Pin Terminal Block)				Top View
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	GND	Common	Digital Ground	
2	+5V	Input	+5V Supply	Reference to digital ground
3	+12V	Input	+12V to +15V Supply	Reference to digital ground
4	-12V	Input	-12V to -15V Supply	Reference to digital ground

This terminal block may be used as an alternative power supply connector if PMAC-Lite is not installed in a PC-bus. The +5V powers the digital electronics. If jumpers E85, E87, and E88 are installed, the +12V and -12V power the analog output stage (this defeats the optical isolation on PMAC).

If you desire to keep the optical isolation between the digital and analog circuits on PMAC, you must provide analog power (+/-12V to +/-15V & AGND) through the JMACH connector, instead of the bus connector or this terminal block.

MINI-PMAC JUMPERS AND CONNECTORS LAYOUT



E1	D1	**E7**	D1	**E30**	E2	**E35**	D2	**E46**	C1	**E66**	E2	**E85**	F3	**E92**	E2	**E104**	A3	**E114**	E1
E2	D1	**E17A**	F2	**E31**	E2	**E36**	D2	**E47**	C1	**E67**	E2	**E87**	F3	**E98**	D2	**E105**	A3	**E115**	E1
E3	D3	**E17B**	F2	**E32**	E2	**E37**	D2	**E48**	C1	**E68**	E2	**E88**	G3	**E100**	G1	**E110**	F1	**E116**	G2
E4	D3	**E17C**	F2	**E33**	E2	**E39**	A3	**E49**	C1	**E69**	E2	**E89**	G1	**E101**	F1	**E111**	F1	**E117**	G2
E5	D3	**E17D**	F2	**E33A**	E2	**E44**	C1	**E50**	C1	**E70**	E2	**E90**	G1	**E102**	F1	**E112**	F1	**E118**	G2
E6	D3	**E29**	E2	**E34A**	D2	**E45**	C1	**E51**	C1	**E71**	E2	**E91**	E2	**E103**	A1	**E113**	E1	**E119**	G2
				E34	D2														