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ASTRONICS
TEST SYSTEMS

Talon Instruments™

SR192A

SR101A
Timing Set Module
Reference Manual

Publication No. SRMM921 Rev. B



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Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.



This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.
2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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DOCUMENT CHANGE HISTORY

Revision	Date	Description of Change
A	10/14/2009	Document Control Legacy Release.
B	10/14/2009	Added TS_CLK linked and master/slave frequency min/max specification.
B	09/24/2014	Per ECN05558, rebranded to Astronics Test Systems.

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1 Introduction

The SR192A digital test module is a modular VXI stimulus/response system. The SR192A baseboard is a two slot, “C” size module which houses up to 12 I/O modules. I/O modules are designed to provide either 8 or 16 stimulus/response channels for a total of 96 or 192 channels. Modules provide many logic options such as fixed or variable voltage, single ended or differential. Some of the current I/O modules are listed below:

- SR125A - 16 channel single ended TTL.
- SR124A - 8 channel single ended TTL or differential RS485/422 per pin.
- SR126A - 8 channel differential LVDS.
- SR214A - 16 channel single ended variable voltage (+7V to -5V).

Multiple SR192A’s may be linked in a master/slave configuration to provide up to 1152 channels in a single VXI 13-slot chassis.

This manual is for the SR101A Timing module. The function of the SR101A Timing Module is to provide all the timing and control for the SR192A I/O modules when executing a stimulus/response operation or emulating a bus interface. After being programmed and commanded to start, the SR101A can generate output signals to the UUT, test input signals from the UUT, generate memory address and control signals for the SR192A I/O modules, and finally examine the results from the I/O modules.

Each SR192A may have one or two SR101A modules installed . The first is always installed into the TSA timing module slot and the second optionally installed into the TSB timing module slot. TSA controls up to six I/O modules, channels 1-96. TSB controls up to six I/O modules, channels 97-192. The Timing modules may operate independently or may be synchronized with one another. Additionally, Timing modules from different SR192A’s may be synchronized together through the J7 master/slave front panel connector.

The layout of this manual is in five sections described below:

1. Introduction	This section
2. Specifications	SR101A electrical and environmental specifications
3. Jumpers/Installation	Description of the jumpers and installation of the SR101A
4. Functional Description	SR101A functional description
5. Operation	SR101A Operation

In addition, two appendices are included:

A. Glossary of Terms	Definition of terms used in this manual
B. Function Code Map	SR101A Function Codes

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2 Specifications

The following sections list the specifications of the SR101A timing module.

2.1 Timing Generator

Timing Sets

Number 16

Number of Cells per Timing Set

Maximum 256
Minimum
TS_CLK <= 50MHz 2
TS_CLK > 50MHz 4
Note: Each cell can output half-phase timing

Timing Set I/O Control Signals

Assert/Return Signal .....STIM_LOAD
Output Enable/Input Strobe .....TSES1 - TSES6
Pattern Increment .....MA_INC

Timing Set User Signals

Front Panel Outputs .....TSOUT1 - TSOUT6

Test Input Wait Conditions

Two Test Inputs (TEST1, TEST2) selected from the following 8 choices
TSINP1, TSINP2, TSINPM, CHTSA, CHTSB, CHT2A, CHT2B, TRIG
Test Conditions (wait for...)
TEST1/TEST2 Low, High, Rising Edge, Falling Edge, Delay A/B, Error, Compare, None
Delay Minimum .....0 TS_CLKs
Delay Maximum .....65535 TS_CLKS
Note: Test Conditions can be programmed in any cell except edge tests, which cannot be done in the last cell or two consecutive cells

Wait Timeout

Minimum 0-Disabled
Maximum .....65536 TS_CLKS
Note: Timeout disabled for Delay and Compare tests.

2.2 Word Generator

Sequence

Number of Subsequences Minimum 1
Number of Subsequences Maximum 4096
Sequence Loop Minimum .....1 (Single)
Sequence Loop Maximum 65536
Continuous Execution .....Yes

Sequence Steps

Number of Timing Cycles 1
Number of I/O Transfers Minimum 1
Number of I/O Transfers Maximum 262144
Sequence Step Loop Minimum 1
Sequence Step Loop Maximum 65536

Sequence Step Conditional Jump/Gosub Test Conditions

TEST1/TEST2 .....High, Low, Rising Edge, Falling Edge
ERROR .....True
Jump Enable .....True
Timeout .....True
Jump to: .....Jump Seq. or Vector Seq.

2.3 Electrical

Timing/Sequence Clock (TS_CLK)

Clock Generator
Maximum Frequency .....100 MHz
Minimum Frequency .....8 Hz
Accuracy .....50 ppm
Resolution .....4 digits
Jitter .....30 ps rms, typ.

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Front Panel CLOCK IN SMA (Optional)
- Maximum Frequency ..... 100 MHz
- Minimum Frequency ..... 8 Hz

Front Panel J8
- Maximum Frequency ..... 50 MHz
- Minimum Frequency ..... 8 Hz

Linked TSA/TSB
- Maximum Frequency ..... 80 MHz
- Minimum Frequency ..... 8 Hz

Master/Slave Mode
- Maximum Frequency ..... 55 MHz
- Minimum Frequency ..... 8 Hz

2.4 Timing Characteristics

The SR101A is a module that operates within the SR192A system. Refer to the SR192A Timing Reference Manual for the timing characteristics of the SR192A system.

2.5 Environmental

Temperature Range

Operating ..... 0° C to +50° C
Storage ..... -40° C to +71° C (RH not controlled)

Altitude

Operating ..... Sea level to 10,000 ft.
Storage ..... Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C ..... not controlled
+11°C to +30°C ..... 95+/-5%RH
+31°C to +40°C ..... 75+/-5%RH
+41°C to +50°C ..... 45+/-5%RH

2.6 Size

Dimension

4.93 cm x 22.61 cm (1.94” x 8.9”)

Weight

0.057 kg (2.0 oz)

2.7 Power Requirements

The power requirements listed in table 2-1 are for a single SR101A.

Voltage	Peak Current	Dynamic Current	Note
+5V	0.75A	0.66A	-
-5.2V	0	0	-
-2V	0	0	-
+12V	0	0	-
-12V	0	0	-
+24V	0	0	-
-24V	0	0	-
V+	0	0	-

Table 2-1 SR101A Power Requirements

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3 Jumpers/Installation

Figure 3-1below is a locator diagram for connectors on the SR101A.

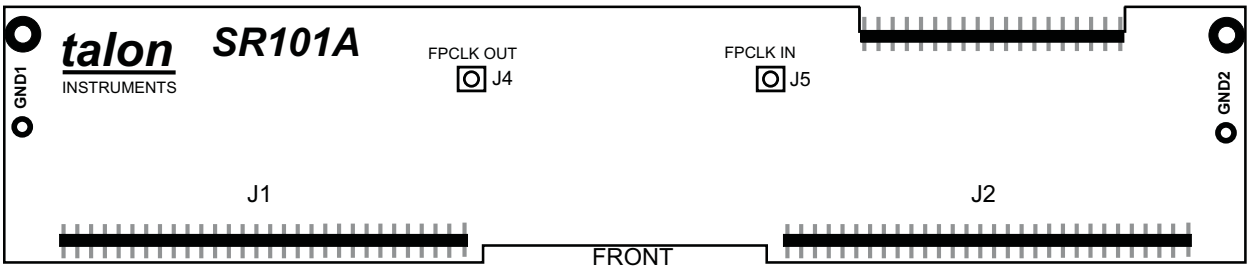


Figure 3-1 Test Point/Jumper Locations

3.1 Test Point Description

The SR101A provides numerous programmable test points for internal. None of the points are usable by customers. Connector J4 of TSA is connected to the front panel CLKOUTA SMA via coax cable. If TSB is installed, its J4 is connected to the front panel CLKOUTB SMA via coax cable.

J5 may be used to provide an input clock by connecting the CLKOUTA or CLKOUTB coax cable to connector J5.

3.2 Installation

Each SR192A baseboard can house up to two timing modules. Timing modules are installed in baseboard slots TSA and TSB. See Figure 3-2.

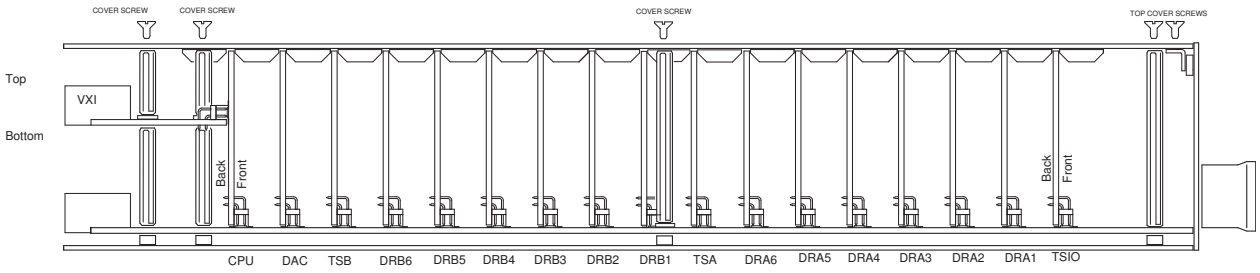


Figure 3-2 SR192A baseboard Side View

The SR192A Series includes an intermodule bus board(s) across the top of the I/O modules and the timing modules to provide an interconnect path. The front intermodule bus board (P/N 20580-001) has resistors installed in positions R1, R2 and R3. The rear intermodule module bus board (P/N 20580-002)

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has resistors installed in positions R7, R8 and R9, see Figure 3-4. If only one timing module is installed then 20580-002 must be installed in the front position.

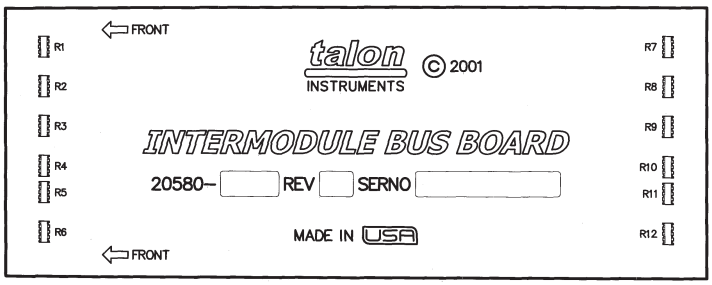


Figure 3-4 Intermodule Bus Board

The intermodule Bus Boards are installed as illustrated in Figure 3-3

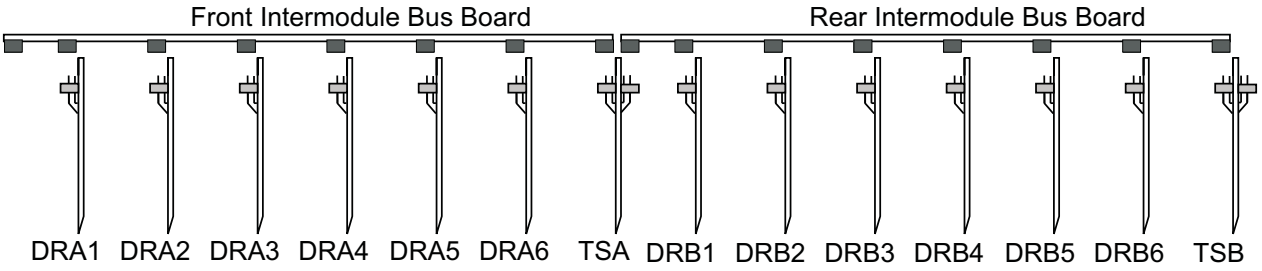


Figure 3-3 Intermodule Bus Board Installation

Follow these steps to add or replace a timing module:

Step 1. Remove SR192A from the chassis and take to an ESD safe area.

Step 2. Remove top cover screws, refer to figure 3-2.

Step 3. Remove the Intermodule Bus Board(s).

Step 4. If replacing a timing module, remove it by grasping at each corner and gently rocking forward and back while pulling it away from the baseboard. Disconnect the coax cable by pulling straight out.

Step 5. Reconnect the coax cable to J4 of timing module first. Insert the new timing module in the TSA or TSB slots, Figure 3-2, by lining up the J1 and J2 connectors with the baseboard connectors and gently pushing down. All SR192A modules are keyed along with the associated baseboard connectors. If the module cannot be inserted, check for bent pins and make sure the module is installed in the proper baseboard slot.

CAUTION

Although the modules and the associated mating connectors have been keyed, it is possible to force a module into an incorrect slot.

Step 6. Reinstall the Intermodule Bus Board(s). The front board overhangs by one connector (see Figure 3-3), the module installed in DRA1 (ascertain the bus board connectors are all aligned and gently press downward).

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4 Functional Description

The SR192A I/O modules are controlled through the SR192A timing modules. Control signals are generated by the timing module which allow the I/O modules to output stimulus data and record response data while the timing module is running. When the timing module is not running, the CPU module or VXI controller can program or query the stimulus/response memories.

The SR101A is comprised of two synchronous state machines referred to as the TIMING GENERATOR and the WORD/PATTERN GENERATOR. The state machines are controlled by the SEQUENCE CONTROLLER.

Figure 4-1 depicts the SR101A signal relationship to other components of the SR192A.

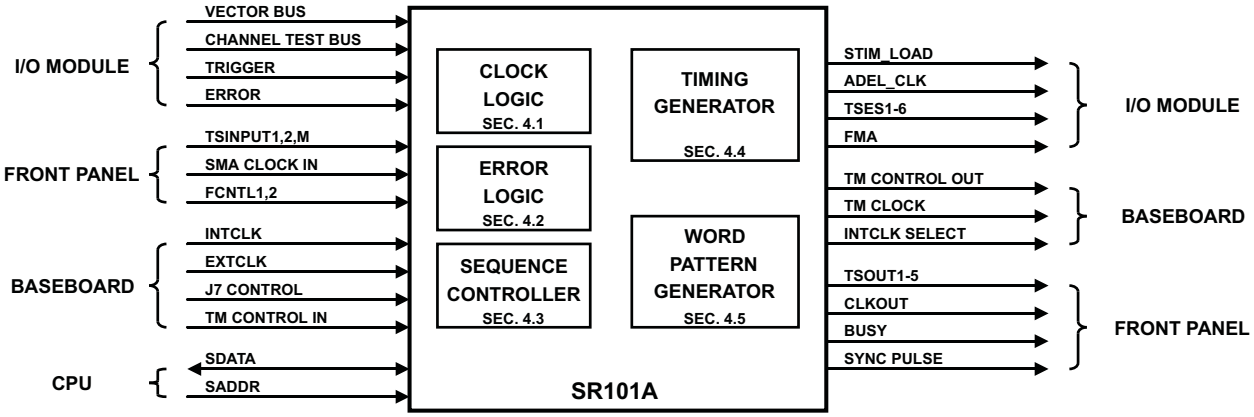


Figure 4-1 SR101A Block Diagram

The following list describes the functional blocks shown in figure 4-1 above.

1. CLOCK LOGIC — The registers that generates/selects the timing module clocks.
2. ERROR LOGIC — The memories and registers that record I/O module error addresses and count.
3. SEQUENCE CONTROLLER — The memories and registers that define and control the sequence steps. Each sequence step selects and controls the timing and word pattern generators.
4. TIMING GENERATOR — The memories and registers that define and control the timing sets. Each timing set generates control signals for the I/O modules and word pattern generator.
5. WORD PATTERN GEN. — The memory and registers that generates the word/pattern address (FMA) for the I/O modules. Each FMA selects a unique pattern in the I/O modules stimulus/response memory.

The following list describes the signals shown in figure 4- above.

1. VECTOR BUS — A four bit vector word used by the sequence controller to select a new sequence step.
2. CHANNEL TEST BUS — A two bit bus used by the sequence controller and timing generator as test input signals.
3. TRIGGER — Registered signal from the I/O modules which indicates that the current response data matches the trigger register. This signal is used by the sequence controller and timing generator as a test input signal.
4. ERROR — Registered signal from the I/O modules which indicates that the response data did not match the expect and mask data when the input strobe occurred. This signal is used by the error logic as well as the sequence controller and timing generator as a test input signal.
5. TSINPUT1,2,M — Front panel signals used by the sequence controller and timing generator as test input signals.
6. SMA CLOCK IN — Front panel signal used by the clock logic as a clock selection (optional).
7. FCNTL1,2 — Front panel signals used to control the I/O module stimulus/response logic as well as the error logic.
8. INTCLK — Baseboard selected internal clock (TM CLOCK or PGMCLK) used by the clock logic.
9. EXTCLK — Baseboard selected external clock (EXTCLK1, EXTCLK2 or EXTCLKM) used by the clock logic.
10. J7 CONTROL — J7 master/slave control signals (START, STOP and TSSYNC).
11. TM CONTROL IN — Link input control signals (START, STOP andTSSYNC).
12. SDATA — Either the baseboard CPU or VXI data bus used to program/query the SR101A.
13. SADDR — Either the baseboard CPU or VXI address bus used to program/query the SR101A.
14. STIM_LOAD — Timing generator signal used to control the I/O modules stimulus logic.
15. ADEL_CLK — Timing generator signal generated to delay the I/O modules response record window.
16. TSES1-6 — Timing generator signals used to control the I/O module stimulus/response logic as well as the error logic.

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17. FMA	Field Memory Address. While running the FMA is generated by the word pattern generator and broadcast to all the I/O modules to select a new stimulus word. While not running the FMA is either the baseboard CPU or VXI address bus used to program/query the I/O modules.
18. TM CONTROL OUT	Link output control signals (START, STOP and TSSYNC).
19. TM CLOCK	Timing Module Clock used by the clock logic.
20. INTCLK SELECT	Internal Clock Select bit used by the clock logic.
21. TSOUT1-5	Timing generator front panel output signals used for DUT handshake/control.
22. CLKOUT	Selected timing generator master clock routed to the front panel.
23. BUSY	Signal from the sequence controller indicating that a sequence is running.
24. SYNC PULSE	User programmable pulse active for selected pattern used for triggering external equipment or logic.

The following sections describe the five logic elements of the SR101A.

4.1 Clock Logic

The SR101A clock logic is used to select the master timing/sequence clock (TS_CLK). The TS_CLK can be set to the following sources:

- On board clock generator.
- Timing Module A Clock.
- Timing Module B Clock.
- External Clock One (EXTCLK1) from the J8 Connector.
- External Clock Two (EXTCLK2) from the J8 Connector.
- Front Panel Clock Input (SMA CLOCK) from the SMA Connector.
- Programmable Clock (PGMCLK) from the SR210 Module.
- Master/Slave Clock (EXTCLKM) from the J7 Connector.

The TS_CLK source is programmed via selectors located on both the SR192A baseboard as well as the SR101A timing module.

Figure 4-2 illustrates the baseboard clock logic block diagram.

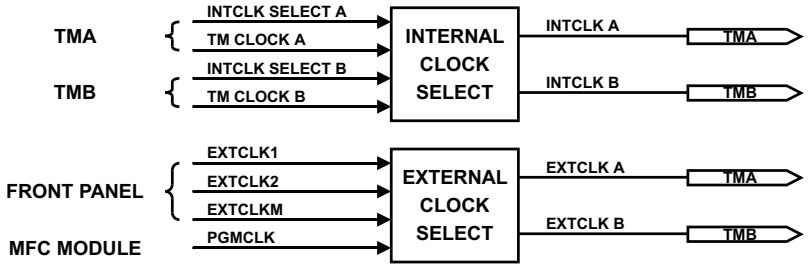


Figure 4-2 baseboard Clock Logic Block Diagram

Figure 4-3 illustrates the timing module clock logic block diagram.

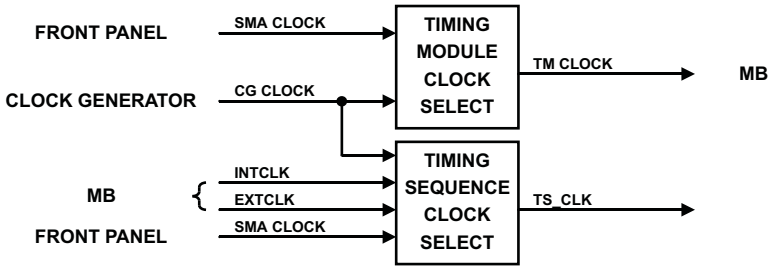


Figure 4-3 Timing Module Clock Logic Block Diagram

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4.2 Error Logic

The SR101A error logic is comprised of an error counter and pattern address memory. The error memory is 18 bits wide and records the FMA (pattern address) when an error occurs. The error memory only records the first 1024 errors. The error counter can count up to 256K errors.

Figure 4-4 illustrates the error logic.

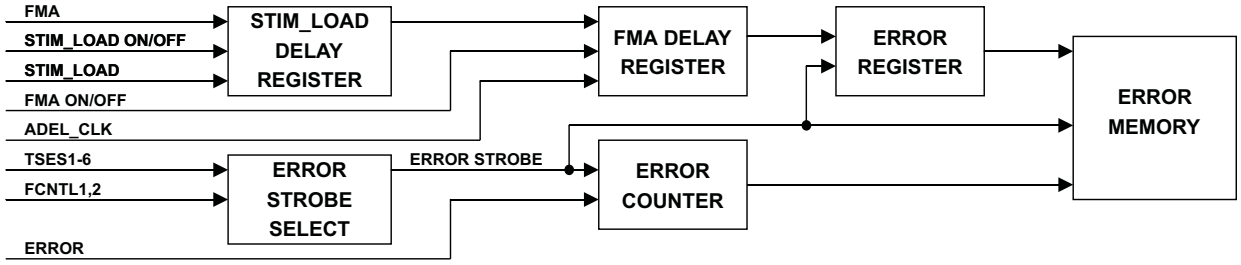


Figure 4-4 Error Logic Block Diagram

The following list describes the signals shown in figure 4-4 above.

1. FMA — Field Memory Address. While running the FMA is generated by the word pattern generator and broadcast to all the I/O modules to select a new stimulus word.
2. STIM_LOAD ON/OFF — Control signal that enables/disables the STIM_LOAD DELAY REGISTER.
3. STIM_LOAD — Timing generator signal used to control the I/O modules stimulus logic. The rising edge will register the FMA bus if the STIM_LOAD DELAY is enabled.
4. TSES1-6 — Timing generator signals used to control the I/O module stimulus/response logic as well as the error logic.
5. FCNTL1,2 — Front panel signals used to control the I/O module stimulus/response logic as well as the error logic.
6. FMA ON/OFF — Control signal that enables/disables the FMA DELAY REGISTER.
7. ADEL_CLK — Timing generator signal generated to delay the I/O modules response record window. The rising edge will register the bus from the STIM_LOAD DELAY REGISTER if the FMA DELAY is enabled.
8. ERROR STROBE — Control signal from the ERROR STROBE SELECT. The rising edge performs the following functions:
   A. Registers the bus from the FMA DELAY REGISTER
   B. Increments the ERROR COUNTER if ERROR true.
   C. Generate the write pulse to the ERROR MEMORY.
9. ERROR — Signal from the I/O modules that indicates a real time error.

The error counter allows the user to query a single register to determine whether a response error has occured during the previous pattern burst.

4.3 Sequence Controller

The SR101A sequence controller allows the user to execute a timing set with one or more word pattern addresses (table). A timing set matched with a table is called a sequence step. The user can program from 1 to 4096 sequence steps. In addition to linking a timing set with a table, the sequence controller also allows the user to define jump conditions and perform looping.

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Figure 4-5 below illustrates the sequence controller block diagram.

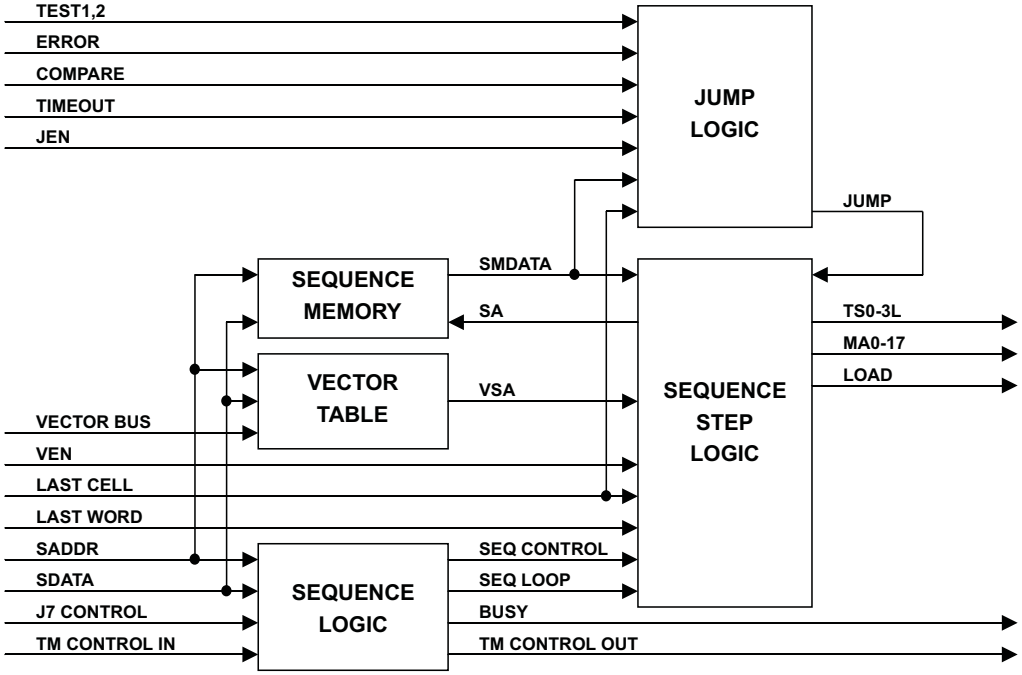


Figure 4-5 Sequence Controller Block Diagram

The following list describes the functional blocks shown in figure 4-5 above.

1. SEQUENCE MEMORY — The sequence memory is 4K deep memory array that controls the timing generator and word pattern generator. The sequence memory is addressed by a 12 bit counter generated by the sequence logic (SA). Sequence memory contains the following data:
   1. 1WSEQ (1 word sequence flag)
   2. LSTSEQ (Last sequence flag)
   3. SUB0 (Return to IDLE flag)
   4. SUBRTN (Subroutine jump flag)
   5. LOOP (Sequence step loop count)
   6. JC0-3 (Jump code)
   7. UJUMP (Unconditional jump flag)
   8. JSA0-11 (Jump sequence address)
   9. TS (Step timing set select)
   10. MA (Step pattern memory address)
2. VECTOR TABLE — The vector table contains sixteen locations that the user can program with a vector jump location. The sixteen locations can be addressed by any of the 192 I/O channels. The vector jump address can be enabled by the VEN control signal to allow sequence jumps based on up to four I/O channel input levels.
3. SEQUENCE LOGIC — The sequence logic selects the control source as well as controlling the sequence loop count. The sequence control is comprised of three signals:
   1. START (Starts the pattern burst).
   2. STOP (Stops an active pattern burst).
   3. SYNC (Synchronizes the master/slave and linked modes).

   The J7 CONTROL bus is selected for master/slave mode. The TM CONTROL is selected for linked mode.
4. JUMP LOGIC — During each sequence step, a jump instruction can be programmed for one of several conditions. The result of the instruction can cause the sequence step jump to the specified sequence address or continue to the next sequential step. The jump conditions are described below:
   1. TEST1 (HIGH, LOW, RISING, FALLING)
   2. TEST2 (HIGH, LOW, RISING, FALLING)

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3. ERROR
4. COMPARE
5. TIMEOUT - Timing cell test timed out.
6. JEN Flag
7. Unconditional
8. No Jump

5. SEQUENCE STEP LOGIC — The step logic provides the timing generator the timing set number (TS0-3) and the word generator the memory address (MA0-17). The sequence step logic provides the next address to the sequences memory based on the current sequence memory data as well as the following control signals:
   1. LAST CELL (Timing Generator last cell flag).
   2. LAST WORD (Word Generator last word flag).
   3. VEN (Word Generator vector enable flag).
   4. JEN (Word Generator jump enable flag).
   5. JUMP (Jump Logic jump flag).

The following list describes the signals shown in figure 4-5 above.

1. TEST1,2 — Two programmable signals used by the jump logic.
2. ERROR — Registered signal from the I/O modules which indicates that the response data did not match the expect and mask data when the input strobe occurred. This signal is used by the jump logic.
3. COMPARE — Inverted error signal from the I/O modules which indicates that the response data matched the expect and mask data when the input strobe occurred. This signal is used by jump logic.
4. TIMEOUT — Flag from the timing generator that indicates a cell test timeout occurred.
5. JEN — Flag used by the jump logic as a qualifier for during a jump step.
6. SADDR — Either the baseboard CPU or VXI address bus used to program/query the SR101A.
7. SDATA — Either the baseboard CPU or VXI data bus used to program/query the SR101A.
8. VECTOR BUS — A four bit vector word used by the vector table to select a new sequence step.
9. VEN — Flag used by the sequence step logic as a qualifier for the vector bus during a jump step.
10. LAST CELL — Signal programmed in the cell memory used to clock the sequence step and jump logic.
11. LAST WORD — Flag used to signal the end of a sequence step.
12. J7 CONTROL — J7 master/slave control signals (START, STOP and TSSYNC).
13. TM CONTROL IN — Link input control signals (START, STOP and TSSYNC).
14. SMDATA — Sequence memory data.
15. SA — Sequence memory address from the sequence step logic.
16. VSA — Sequence jump address from the vector table.
17. SEQ CONTROL — Selected control bus signals (START, STOP and TSSYNC).
18. SEQ LOOP — Sequenc loop control flag.
19. TM CONTROL OUT — Link output control signals (START, STOP and TSSYNC).
20. JUMP — Flag that indicates a jump true condition.
21. TS0-3 — Timing set select from sequence control.
22. MA0-17 — Signals to the word generator that defines a starting pattern memory address for a sequence step.

4.4 Timing Generator Logic

The SR101A timing generator allows the user to program the signals used by the I/O modules to control the stimulus/response timing. The timing generator also allows the user to generate and test handshake signals required by the DUT.

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Figure 4-6 below shows the block diagram of the timing generator logic.

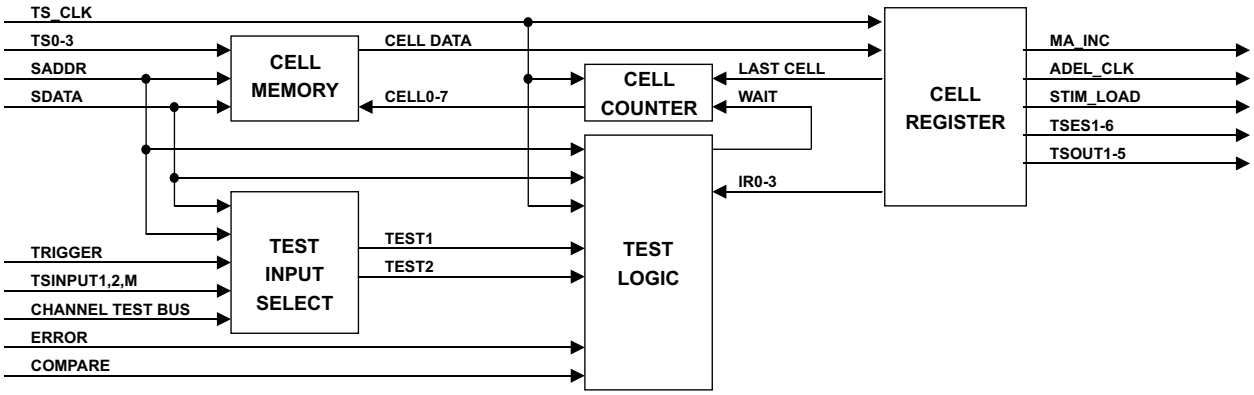


Figure 4-6 Timing Generator Block Diagram

The following list describes the functional blocks shown in figure 4-6 above.

1. CELL MEMORY — The contents of the cell memory controls the timing generator state machine as well as the word generator clock, SR192A I/O module control signals and user defined timing outputs. Each memory location is a timing generator state. The cell memory is segmented into the following address groups:
   1. TS0-TS3: Sixteen timing sets selected by the Sequence Controller.
   2. CELL0-7:256 timing cells
2. TEST INPUT SELECT — Select which Test Inputs will be used for TEST1 and TEST2.
3. CELL COUNTER — The cell counter generates the lower eight address lines (CELL0-7) to the cell memory. The counter is cleared to zero by a feedback signal programmed into the cell memory called LAST CELL. The counter can be stopped by a signal generated by the test logic called WAIT.
4. TEST LOGIC — Within each cell, a test instruction can be programmed for one of several conditions. The result of the test can cause the timing state machine to either stop (WAIT) or continue to the next timing cell. The test conditions are described below:
   1. TEST1 (HIGH, LOW, RISING, FALLING)
   2. TEST2 (HIGH, LOW, RISING, FALLING)
   3. ERROR
   4. COMPARE
   5. DELAY A or B DONE - Delay counter done signal
   6. No test

   The TSOUT and TSES signals can be programmed to be active during a WAIT cell by using half phase timing.
5. CELL REGISTER — The contents of the cell memory are registered and clocked by the same signal that generates the lower eight addresses. The signals are described below:
   1. ADEL_CLK (I/O Module Response Address Delay Clock).
   2. STIM_LOAD (I/O Module Stimulus Load Clock).
   3. TSES1-6 (I/O Module Enables/Strobes).
   4. TSOUT1-5 (User Defined Outputs).
   5. IR0-3 (Test Logic Instruction Register)
   6. LAST CELL (Cell Counter Clear Control and Word Generator Load Control)

The following list describes the signals shown in figure 4-6 above.

1. TS_CLK — This signal is the timing generator system clock. Every rising edge of the TS_CLK causes a new timing generator state, called a CELL. The minimum resolution of a timing generator cell is the period of the TS_CLK.
2. TS0-3 — Timing set select from sequence control.
3. SADDR — Either the baseboard CPU or VXI address bus used to program/query the SR101A.
4. SDATA — Either the baseboard CPU or VXI data bus used to program/query the SR101A.
5. TRIGGER — Registered signal from the I/O modules which indicates that the current response data matches the trigger register. This signal is used by the sequence controller and timing generator as a test input signal.
6. TSINPUT1,2,M — Front panel signals used by the sequence controller and timing generator as a test input signals.

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7.	CHANNEL TEST BUS	A two bit bus used by the sequence controller and timing generator as a test input signal.
8.	ERROR	Registered signal from the I/O modules which indicates that the response data did not match the expect and mask data when the input strobe occurred. This signal is used by the sequence controller and timing generator as a test input signal.
9.	COMPARE	Registered signal from the I/O modules which indicates that the response data matched the expect and mask data when the input strobe occurred. This signal is used by the sequence controller and timing generator as a test input signal.
10.	CELL DATA	Data from the cell memory that defines the levels of the cell register outputs.
11.	CELL0-7	Output of the cell counter that increments through the timing set memory.
12.	TEST1,2	Two programable signals used by the test logic for timing set handshakes.
13.	LAST CELL	Signal programmed in the cell memory used to clear the cell counter and increment the word generator.
14.	WAIT	Signal generated by the test logic used to stop the cell counter. This signal allows the user to generate handshake control of the timing sets.
15.	IR0-3	Signals programmed in the cell memory that selectes a timing set test instruction.
16.	MA_INC	Signal programmed in the cell memory that increments the word generator prior to the last cell.
17.	ADEL_CLK	Signal programmed in the cell memory to delay the I/O modules response record window.
18.	STIM_LOAD	Signal programmed in the cell memory used to control the I/O modules stimulus/response logic as well as the error logic.
19.	TSES1-6	Signals programmed in the cell memory used to control the I/O modules stimulus/response logic as well as the error logic.
20.	TSOUT1-5	Signals programmed in the cell memory used for DUT handshake/control.

4.5 Word Pattern Generator Logic

The SR101A word pattern generator provides the address to the I/O modules stimulus/response memories. It also provides flags to the sequence controller (LAST WORD, VEN, JEN) as well as the user (SYNC PULSE).

Figure 4-7 below is the block diagram for the word pattern generator.

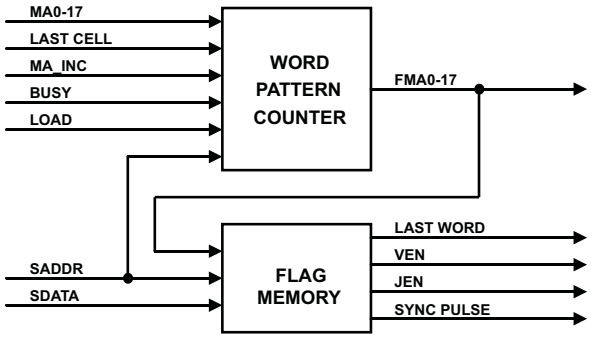


Figure 4-7 Word Generator Block Diagram

The following list describes the functional blocks shown in figure 4-7 above.

1.	WORD PATTERN COUNTER	The word pattern counter generates the I/O module stimulus/response address (FMA0-17). The counter is loaded by a signal from the sequence controller called LOAD. The counter increments with every LAST CELL or MA_INC signal from the timing generator. When the BUSY signal is false the SADDR bus is passed through to the FMA bus so the VXI backplane or CPU can program/query the I/O modules.
2.	FLAG MEMORY	The contents of the flag memory are used by the sequence controller as well as providing a sync output to the user.

The following list describes the signals shown in figure 4-7 above.

1.	MA0-17	Signals from the sequence controller that selects a starting pattern memory address for a sequence step.
2.	LAST CELL	Signal that indicates the timing generator is in the last cell of a timing set. The word pattern counter is incremented during the last cell.
3.	MA_INC	Signal from the timing generator used to increment the word pattern counter prior to the last cell.
4.	BUSY	Signal from the sequence controller that indicates whether pattern sequence is active (running).
5.	LOAD	Signal from the sequence controller that loads a new count into the word pattern counter.
6.	SADDR	Either the baseboard CPU or VXI address bus used to program/query the SR101A.
7.	SDATA	Either the baseboard CPU or VXI data bus used to program/query the SR101A.
8.	FMA0-17	Field Memory Address. While running, the FMA is generated by the word pattern counter and broadcast to all the I/O modules to select a new stimulus word. While not run-

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	ning, the FMA is either the baseboard CPU or VXI address bus used to program/query the I/O modules.
9. LAST WORD	Flag used by the sequence controller to signal the end of a sequence step.
10. VEN	Flag used by the sequence controller as a qualifier for the vector bus during a jump step.
11. JEN	Flag used by the sequence controller as a qualifier for during a jump step.
12. SYNC PULSE	Flag routed to the front panel.

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Appendix A Glossary of Terms

A16/A24/A32	The VXI address is segmented into three separate areas by a group of VXI signals called the address modifiers (AM0-AM5). These three areas are called A16, A24 and A32. Every VXI module is mapped into 64 bytes of the A16 memory. VXI modules, in addition, may request additional memory map space in the A24 or A32 space. The SR192A maps all the Timing and I/O modules registers into the A24/A32 space.
ADEL_CLK	Address Delay Clock. This signal, generated by the timing generator, clocks the response address delay register on the I/O modules.
CELL	A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK.
CHANNEL TEST	Allows any channel of the installed I/O modules to be used as a test input (TEST1 or TEST2).
ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
FCNTL1/2	Front panel input signals (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FMA	Field Memory Address. This group of signals is generated by the word generator and broadcast to the I/O modules. The FMA directly selects the stimulus/response memory word.
FUNCTION CODE(FC)	Each module in a SR192A is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module.
HALF PHASE TIMING	The ability to generate signals that are one-half the period of the TS_CLK. Typically used to enhance the performance of serial operations or to format output data.
HANDSHAKE	Process used to synchronize data to/from a UUT utilizing SR101A timing module test inputs and timing outputs.
I/O MODULE	Any Stimulus/Response modules for the SR192A.
JEN	JUMP ENABLE enables a jump condition on one or more words of a table.
JUMP	A “jump” occuring during the execution of a step causes the execution of this step to cease and the execution of another sequence step to begin.
LINKED MODE	TSA and TSB operating synchronously.
MA_INC	The memory address (FMA) is always incremented at start of each timing cycle (First Cell). The “MA_INC” signal may be used to increment the FMA in later timing cells. The FMA will be incremented at the beginning of the next cell after the “MA_INC”. “MA_INC” can be programmed in every other cell except the last two cells.

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MASTER MODE	Two or more SR192A's operating synchronously.
RESPONSE	The response data of the SR192A is comprised of EXPECT, MASK and RECORD memories.
SADDR	The address bus from the VXI Backplane.
SDATA	The data bus from the VXI Backplane.
SEQUENCE	A sequence is an ordered list of stimulus/response actions consisting of one or more sequence steps.
SEQUENCE STEP	A sequence step is a single element of a sequence. A sequence step selects a timing set, table, loop count, jump condition and control flags.
STIM_LOAD	Timing module control signal that loads the data from the stimulus memory into the output registers. The rising edge of this control signal also registers the stimulus address (FMA) when the output register delay is enabled. The falling edge performs the Data Format function if enabled.
STIMULUS	The stimulus data of the SR192A is determined by the OUTPUT and TRISTATE memory data, output enables, output mode and output format.
TABLE	A table isa defined number of STIMULUS/RESPONSE words. It is located within a specific range of FMA addresses. The FMA range is broadcast to all the I/O modules connected to the timing module.
TEST1, 2	Two test inputs that can be selected from the TSINPUTs, CHANTEST signals or TRIGGER.
TIMING MODULE	An SR192A plug-in module that controls stimulus/response timing and sequencing.
TIMING SET	A timing set is the structure that is created that defines the stimulus/response timing. Sixteen timing sets can be defined of 2-256 cells.
TRANSFER	See WORD.
TS_CLK	Timing Set Clock. This signal clocks the timing generator. Each cell is one period of the TS_CLK.
TSES1...6	General purpose Timing Set signals that can be used to enable stimulus drivers, enable mode functions, strobe data into registers or strobe response data into memory.
TSINPUT1/2	Front panel test input signal. Each timing module has two test input signals available, TEST1 and TEST2. Either TSINPUT signal may be routed to TEST1 or TEST2 for Timing Set or Sequence Control.
TSINPUTM	The TSINPUT1A signal which is synchronized by the clock and used in Linked or Master/Slave operations.
TSOUT1..5	Timing Set Output One through Five. General purpose output signals generated by the timing module.
UUT	Unit Under Test
VECTOR	A collection of up to four input channels whose High/Low states define a vector with up to sixteen values (one value for each combination of the input levels).

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VECTOR BUS	The vector bus is an intermodule bus that connects all of the Series A I/O modules with the associated timing module(s). This bus allows the user to route any channel input to any of the four vector bus lines. The Timing Module allows the user to jump to a sequence address where the four vector bus signals address a LUT to determine the jump address.
VEN	VECTOR ENABLE enables a jump condition which has a JEN to jump to a sequence based on a vector value generated by the I/O modules.
WORD	A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192A.

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Appendix B SR101A Function Code Map

Each SR192A module is assigned a base address in the A24/A32 memory. This base address along with a four bit function code gives each module 4MB of register space.

The following sections describes each of the SR101A function code definitions.

1 Timing Set Memory (FC0)

The timing set memory is organized into sixteen 512 x 16 bit arrays called a timing set. Figure B-1 illustrates the timing set memory offsets.

TS0 (IDLE)	BASE + 0h
TS1	BASE + 400h
TS2	BASE + 800h
TS3	BASE + C00h
TS4	BASE + 1000h
TS5	BASE + 1400h
TS6	BASE + 1800h
TS7	BASE + 1C00h
TS8	BASE + 2000h
TS9	BASE + 2400h
TS10	BASE + 2800h
TS11	BASE + 2C00h
TS12	BASE + 3000h
TS13	BASE + 3400h
TS14	BASE + 3800h
TS15	BASE + 3C00h

Figure B-1 Timing Set Memory Offsets

Every two consecutive memory locations is referred to as a cell. Each timing set can be programmed from 2 to 256 cells. A new timing cell is output for every “TS_CLK”. Figure B-2 describes the “TS_CLK” to timing cell relationship.

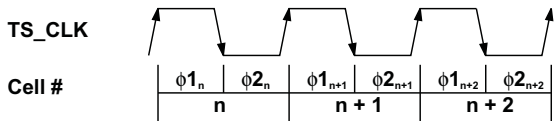


Figure B-2 Timing Set Memory Bits

Table B-1 shows the bit definitions for both words of a timing cell.

Word 1 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC-1	IR1	IR0	$TSO5_1$	$TSO4_1$	$TSO3_1$	$TSO2_1$	$TSO1_1$	$ES6_1$	$ES5_1$	$ES4_1$	$ES3_1$	$ES2_1$	$ES1_1$	ADC_1	SL_1
Word 2 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAI	IR3	IR2	$TSO5_2$	$TSO4_2$	$TSO3_2$	$TSO2_2$	$TSO1_2$	$ES6_2$	$ES5_2$	$ES4_2$	$ES3_2$	$ES2_2$	$ES1_2$	ADC_2	SL_2

Table B-1 Timing Cell Bit Definitions

Field/Bit Definition:

SL_1	“STIM_LOAD” phase 1.
ADC_1	“ADEL_CLK” phase 1.
$ES1_1$	“TSEN/STR1” phase 1.

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$ES2_1$	“TSEN/STR2” phase 1.
$ES3_1$	“TSEN/STR3” phase 1.
$ES4_1$	“TSEN/STR4” phase 1.
$ES5_1$	“TSEN/STR5” phase 1.
$ES6_1$	“TSEN/STR6” phase 1.
$TS01_1$	“TSOUT1” phase 1.
$TS02_1$	“TSOUT2” phase 1.
$TS03_1$	“TSOUT3” phase 1.
$TS04_1$	“TSOUT4” phase 1.
$TS05_1$	“TSOUT5” phase 1.
IR0	Instruction Register bit 0, see note 2 below.
IR1	Instruction Register bit 1, see note 2 below.
LC	Last cell flag, see note 3.
SL_1	“STIM_LOAD” phase 2.
ADC_2	“ADEL_CLK” phase 2.
$ES1_2$	“TSEN/STR1” phase 2.
$ES2_2$	“TSEN/STR2” phase 2.
$ES3_2$	“TSEN/STR3” phase 2.
$ES4_2$	“TSEN/STR4” phase 2.
$ES5_2$	“TSEN/STR5” phase 2.
$ES6_2$	“TSEN/STR6” phase 2.
$TS01_2$	“TSOUT1” phase 2.
$TS02_2$	“TSOUT2” phase 2.
$TS03_2$	“TSOUT3” phase 2.
$TS04_2$	“TSOUT4” phase 2.
$TS05_2$	“TSOUT5” phase 2.
IR2	Instruction Register bit 2, see note 2 below.
IR3	Instruction Register bit 3, see note 2 below.
MAI	Memory address increment, see note 4 below.

Notes:

1 All signals active high. Write to word 1 loads register. Write to word 2 loads register and programs memory.

2. The four bit instruction register (IR0 through IR3) are decoded as follows:

IR3	IR2	IR1	IR0	Instruction
0	0	0	0	Wait until “TEST1” low
0	0	0	1	Wait until “TEST1” high
0	0	1	0	Wait until “TEST1” rising edge
0	0	1	1	Wait until “TEST1” falling edge
0	1	0	0	Wait until “TEST2” low
0	1	0	1	Wait until “TEST2” high
0	1	1	0	Wait until “TEST2” rising edge
0	1	1	1	Wait until “TEST2” falling edge
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Wait until delay A done
1	1	0	0	Wait until delay B done
1	1	0	1	Wait on error
1	1	1	0	Wait until compare
1	1	1	1	No Test

3. The last cell bit is programed high one cell prior to the actual last cell.
4. Increments the memory address to the I/O modules.

2 Sequence Memory (FC1)

The sequence memory is organized into an array of 16K by 16 bit memory.

Every four consecutive memory locations is referred to as a subsequence. A sequence can be programmed from 1 to 4096 subsequences.

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Table B-2 shows the bit definitions for all four words of a subsequence.

Word 1 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSLOOP															
Word 2 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FMA_LSB															
Word 3 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	1WS	JSA												FMA_MSB	
Word 4 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU				LSEQ	SRTN	SUB0	UJMP	JCODE				TS			

Table B-2 Sequence Memory Bit Definitions

Field/Bit Definition:

SSLOOP	Subsequence loop count (1 - 65536, load count - 1).
FMA_LSB	Lower 16 bits of the table address to output.
FMA_MSB	Upper 2 bits of the table address to output.
JSA	Jump sequence address, see note 2.
1WS	One word table flag.
TS	Timing set number.
JCODE	Jump code, see note 3.
UJMP	Unconditional jump flag.
SUB0	Jump to subsequence address 0.
SRTN	Jump gosub flag, see note 4.
LSEQ	Last subsequence flag.

Notes:

1. Each write loads directly into its portion of the sequence memory.
2. If a jump condition is true and “VEN” is set in function code five than the next subsequence address will be defined by the vector table (function code nine). If “VEN” is not set then the next subsequence address will be the “JSA” value. If no jump condition is true than the next consecutive subsequence will execute until the LSEQ flag is true.
3. The four bit jump register is decoded as follows:

JEN (FC5)	UJMP	JCODE				Jump Instruction
		Bit 3	Bit 2	Bit 1	Bit 0	
1	0	0	0	0	0	Jump if “TEST1” low
1	0	0	0	0	1	Jump if “TEST1” high
1	0	0	0	1	0	Jump if “TEST1” rising edge
1	0	0	0	1	1	Jump if “TEST1” falling edge
1	0	0	1	0	0	Jump if “TEST2” low
1	0	0	1	0	1	Jump if “TEST2” high
1	0	0	1	1	0	Jump if “TEST2” rising edge
1	0	0	1	1	1	Jump if “TEST2” falling edge
1	0	1	0	0	0	Reserved
1	0	1	0	0	1	Reserved
1	0	1	0	1	0	Reserved
1	0	1	0	1	1	Reserved
1	0	1	1	0	0	Jump if error true
1	0	1	1	0	1	Jump if timeout true
1	0	1	1	1	0	Jump if JEN
X	0	1	1	1	1	No jump
X	1	X	X	X	X	Unconditional jump
0	0	X	X	X	X	No jump

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4. If a jump condition is true and “SRTN” is true then the jump subsequence will execute and return to the next word of this subsequence.

3 Sequence Loop Count Register (FC2)

This function code programs the sequence loop count register. The timing sequence can be looped continuous or from 1 to 65536 times, see Figure B-3 below.

LOOP LSW	**BASE + 0h**
LOOP MSW	**BASE + 2h**

Figure B-3 Loop Count Register

Table B-3 shows the bit definition for the sequence loop count.

LOOP LSW Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
LOOP MSW Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU															SC

Table B-3 Sequence Loop Count Bit Difinition

Field/Bit Definition:

COUNT	Loop count value (0 to 65536, load “count - 1”).
SC	Single/continuous (0 = continuous, 1 = single).

Notes:

None

4 Timing Set Delay Registers (FC3)

Two timing set delay registers can be programmed. Each delay can be programmed from 0 (no delay) to 65535 (65535 delays). Each delay is measured in TS_CLK periods. Figure B-4 illustrates the function code three register mapping.

DELAY 'A'	**BASE + 0h**
DELAY 'B'	**BASE + 2h**

Figure B-4 Timing Cell Delay Register Bit Definiton

Table B-4 shows the bit definition of the delay registers.

DELAY LSW Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAYA															
DELAY MSW Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAYB															

Table B-4 Delay Register Bit Definition

Field/Bit Definition:

DELAYA	Delay ‘A’ value (0 - 65535, 0 = no delay).
DELAYB	Delay ‘B’ value (0 - 65535, 0 = no delay).

Notes:

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None

5 Timing Set Timout Register (FC4)

The timeout register is a sixteen bit register and can be programmed from 1 to 65536 clocks before a timeout is generated during a WAIT on input. The timeout can also be disabled. Figure B-5 illustrates the function code four register mapping.

TIMEOUT LSW	**BASE + 0h**
TIMEOUT MSW	**BASE + 2h**

Figure B-5 Timing Set Timeout Register Mapping

Table 5-5 shows the bit definition of the timeout registers.

TIMEOUT LSW Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMEOUT															
TIMEOUT MSW Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															EN

Table B-5 Timeout Register Bit Definition

Field/Bit Definition:

TIMEOUT	Timeout count value (1 - 65536, load “count - 1”).
EN	Timeout enable (0 = disabled, 1 = enabled).

Notes:

None

6 Sync/Test Enable Memory (FC5)

The sync/test enable memory contains the last word, sync, jump and vector flags.

Table B-6 shows the bit definition of the sync/test enable memory.

Sync/Test Enable Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
See note 1								NU			ALW	VEN	JEN	SYNC	LW

Table B-6 Sync/Test Enable Memory Bit Definition

Field/Bit Definition:

LW	Last word flag (0 = next FMA is not last word, 1 = next FMA is last word).
SYNC	Sync output (0 = no sync, 1 = sync output, see note 2).
JEN	Jump Enable (0 = no jump, 1 = jump).
VEN	Vector Enable (0 = not a vectored jump, 1 = do a vectored jump)
ALW	Alternate last word flag (0 = next FMA is not last word, 1 = next FMA is last word). See note 3

Notes:

1. Upper byte cannot be programmed.
2. The sync output is active low on the J8 connector.
3. Refer to FC8 on how the ALW is selected.

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7 First Sequence Register (FC6)

The first sequence register holds the sequence address to be executed when the next start occurs. Table B-7 shows the bit definition of the first sequence register.

Sync/Test Enable Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU				SEQADDR											

Table B-7 First Sequence Bit Definition

Field/Bit Definition:

SEQADDR Sequence address (0 to 4095).

Notes:

None

8 Control/Status Registers (FC7)

The control/status registes are used to configure/query the following SR101A features:

1. Clock control
2. Signal Control
3. Error memory control
4. Timing Set Status
5. Sequence Status
6. Memory Address
7. Error Count

Figure B-6 illustrates function code seven register map.

CLOCK CONTROL	**BASE + 0h**
SIGNAL CONTROL	**BASE + 2h**
ERROR MEMORY CONTROL	**BASE + 4h**
TIMING SET STATUS	**BASE + 6h**
SEQUENCE STATUS	**BASE + 8h**
MEMORY ADDRESS	**BASE + Ah**
ERROR COUNT	**BASE + Ch**

Figure B-6 Control/Status Register Map

The following sections describe of the function code seven control/status registers.

8.1 Clock Control Register (FC7:0x0)

The clock control register is used to program the SR101A clock selection.
Table B-8 shows the bit definition of the clock control register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
J8 CLOCK OUT SEL		SMA CLOCK OUT SEL		TME	NU	MBCLKOUT		NU	CGDTB			CLKSEL			

Table B-8 Clock Control Bit Definition

Field/Bit Definition:

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CLKSEL	Clock select, see note 1.
CGDTB	Clock generator divide timebase, see note 2.
MBCLKOUT	Clock select for linked or M/S operation, see note 3.
TME	TSINPUTM edge (0 = rising, 1 - falling)

Notes:

1. The four bit clock select decode is listed below:

Bit 3	Bit 2	Bit 1	Bit 0	Clock Source
0	0	0	0	TSA Clock
0	0	0	1	TSB Clock
0	1	0	0	Clock Generator (CG)
1	0	0	0	SMACLKIN
1	0	1	0	Inverted SMACLKIN
1	1	0	0	Selected external clock
1	1	1	0	Inverted selected external clock

2. The three bit clock generator divide timebase decode is listed below:

Bit 6	Bit 5	Bit 4	Clock Source
0	0	0	X1
0	0	1	X10
0	1	0	X100
0	1	1	X1,000
1	0	0	X10,000
1	0	1	X100,000
1	1	0	X1,000,000
1	1	1	X10,000,000

3. The two bit baseboard clock output select decode is listed below:

Bit 9	Bit 8	Clock Source
0	0	None (low)
0	1	Clock Generator
1	0	SMACLKIN
1	1	Inverted SMACLKIN

4. SMA CLOCK OUT SEL

Bit 13	BIT 12	Clock Source
0	0	None (low)
0	1	Clock Generator
1	0	Selected Clock
1	1	Selected Clock Inverted

5. J8 CLOCK OUT SEL

Bit 15	Bit 14	Clock Source
0	0	None (low)
0	1	Clock Generator
1	0	Selected Clock
1	1	Selected Clock Inverted

8.2 Signal Control Register (FC7:0x2)

The signal control register is used to program the SR101A signal selection.
Table B-9 shows the bit definition of the signal control register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM	DTSA	CTRLSEL		JSSEL				VGS	T2SEL			NU	T1SEL		

Table B-9 Signal Control Bit Definition

Field/Bit Definition:

T1SEL	Test 1 signal select, see note 1.

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T2SEL	Test 2 signal select, see note 1.
VGS	Vector group select (0 = A, 1 = B).
JSSEL	Jump strobe signal select, see note 2.
CTRLSEL	Control signal select, see note 3.
CSE	Control signal edge (0 = rising, 1 = falling)
DTSA	Designates TSA if linked (1 = TSA, 0 = TSB)
DM	Designates Master if in Master/Slave mode (1 = Master TS, 0 = other TS)

Notes:

1. The three bit test signal select decode is listed below:

Bit 2,6	Bit 1,5	Bit 0,4	Test Signal Source
0	0	0	TSINPUT1
0	0	1	TSINPUT2
0	1	0	TSINPUTM
0	1	1	CHT1A
1	0	0	CHT2A
1	0	1	CHT1B
1	1	0	CHT2B
1	1	1	TRIGGER

2. The four bit jump strobe select decode is listed below:

Bit 11	Bit 10	Bit 9	Bit 8	Strobe Source
0	0	0	0	TSEN/STR1
0	0	0	1	TSEN/STR2
0	0	1	0	TSEN/STR3
0	0	1	1	TSEN/STR4
0	1	0	0	TSEN/STR5
0	1	0	1	TSEN/STR6
0	1	1	0	FCNTL1
0	1	1	1	FCNTL2
1	X	X	X	none

3. The two bit synchronization control select decode is listed below:

Bit 13	Bit 12	Control Source
0	0	Independent
0	1	Linked
1	0	Master/slave

8.3 Error Memory Control Register (FC7:0x4)

The error memory control register is used to program the SR101A error memory logic.
Table B-10 shows the bit definition of the error memory control register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU										AD	ORD	NU	EMSSEL		

Table B-10 Error Memory Control Bit Definition

Field/Bit Definition:

EMSSEL	Error memory strobe select, see note 1.
ORD	Output register delay (0 = disabled, 1 = enabled).
AD	Address delay (0 = disabled, 1 = enabled).

Notes:

2. The three bit error memory strobe select decode is listed below:

Bit 2	Bit 1	Bit 0	Strobe Source
0	0	0	TSEN/STR1
0	0	1	TSEN/STR2
0	1	0	TSEN/STR3
0	1	1	TSEN/STR4

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1	0	0	TSEN/STR5
1	0	1	TSEN/STR6
1	1	0	FCNTL1
1	1	1	FCNTL2

8.4 Timing Set Status Register (FC7:0x6)

The timing set status register is used to query the SR101A timing set status.
Table B-11 shows the bit definition of the timing set status register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CERR	SA	IDLE	WAIT	TS				CELL							

Table B-11 Timing Set Status Bit Definition

Field/Bit Definition:

CELL	Current cell number (0 to 255).
TS	Current timing set number (0 to 15).
WAIT	Waiting for test input handshake (0 = no wait, 1 = waiting).
IDLE	Idle mode flag (0 = not idle, 1 = idle active).
SA	Sequence active flag (0 = not active, 1 = active).
CERR	External clock error flag (0 = no error, 1 = selected external clock < CG/256

Notes:

1. Read only register.

8.5 Sequence Status Register (FC7:0x8)

The sequence status register is used to query the SR101A sequence status.
Table B-12 shows the bit definition of the sequence status register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECMSB		MAMSB		SEQ											

Table B-12 Sequence Status Bit Definition

Field/Bit Definition:

SEQ	Current sequence address (0 to 4095).
MAMSB	Memory address bits 17 and 16, see note 2.
ECMSB	Error count bits 17 and 16, see note 2.

Notes:

1. Read only register.
2. The memory address and error counter registers are 18 bits wide. The upper two bits of each register are stored in this register.

8.6 Memory Address Register (FC7:0xA)

The memory address register is used to query the SR101A memory address.

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Table B-15 shows the bit definition of the memory address register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MALSB															

Table B-15 Memory Address Bit Definition

Field/Bit Definition:

MALSB Current memory address bits 0 to 15 (0 to 65535), see note 2.

Notes:

1. Read only register.
2. The memory address is 18 bits wide. The following equation illustrates how to form the 18 bit memory address:

   MSB = data at address 8h of function code 7.
   LSB = data at address Ah of function code 7.
   FMA = (MSB & 3000h) << 4 + LSB

8.7 Error Count Register (FC7:0xC)

The error count register is used to query the SR101A error count.

Table B-13 shows the bit definition of the error count register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECLSB															

Table B-13 Error Count Bit Definition

Field/Bit Definition:

ECLSB Error counter bits 0 to 15 (0 to 65535), see note 2.

Notes:

1. Read only register.
2. The error counter is 18 bits wide. The following equation illustrates how to form the 18 error count:

   MSB = data at address 8h of function code 7.
   LSB = data at address Ch of function code 7.
   FMA = (MSB & C000h) << 2 + LSB

9 Run Control (FC8)

This register is used to control the timing and sequence execution.

Table B-14 shows the bit definition of the run control register.

Sync/Test Enable Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		LMSS	LLS	PL	ALWS	CERR	FDI	REC	DW	CW	SYNC	STOP	RUN	IDLE	RST

Table B-14 Run Control Bit Definition

Field/Bit Definition:

RST Resets the SR101A to the standby mode (1 = execute, 0 = no action).
IDLE Starts the SR101A in idle mode (1 = execute, 0 = no action)

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RUN	Starts the first sequence (1 = execute, 0 = no action)
STOP	Stops the currently running sequence (1 = execute, 0 = no action)
SYNC	Generates a sync pulse (1 = execute, 0 = no action)
CW	Generates a single pulse to clear a wait in one test/delay cell (1 = execute, 0 = no action)
DW	Disables test/delay cells (1 = disable, 0 = enable)
REC	Reset error counter (1 = reset, 0 = no action)
FDI	Forces Data from FMA = 0 to be output during Idle (1 = enable, 0 = disable)
CERR	Duplicate of External Clock Error flag in FC7
ALWS	Alternate Last Word Select (1 = selects the ALW bit in the Sync/Test Enable Memory, 0 = selects normal LW bit), see FC5
PL	Pre-load the Sync/Test Enable Memory with all zeros, see note 4
LLS	Lost Link Sync, see note 7
LMSS	Lost Master/Slave Sync, see note 8

Notes:

1. Bits 9, 12 and 13 are read only..
2. An IDLE command must be given before a RUN command.
3. Bits 1 thru 5 are synchronized with the selected clock. These bits may be read back to see if the command has executed. If the clock is slow (or there's no clock) a "1" will indicate that the command has not yet executed.
4. Bit 11 may be read. If a "1" is present, the command has not yet executed or is not finished (takes ~40ms to zero out the memory).
5. Bit 6, 8 and 10 are Read/Write
6. Bits 0,7,14 and 15 will always read zero.
7. A LLS is only meaningful if the both timing modules are installed and linked, see FC7.
8. A LMSS is only meaningful if the timing modules are setup for Master/Slave, see FC7.

10 Vector Jump Lookup Table (FC9)

The vector jump lookup table allows the user to program a sequence address for each of the sixteen possible vector codes from the I/O modules.

Figure B-7 illustrates the vector jump lookup table address map.

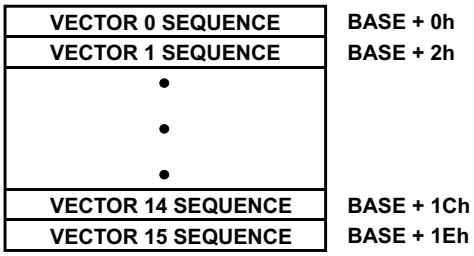


Figure B-7 Vector Jump Lookup Table Address Map

Table B-16 shows the bit definition of the vector jump lookup table registers.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU				SEQ											

Table B-16 Vector Jump Lookup Table Bit Definition

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Field/Bit Definition:

SEQ Sequence address to jump to if the vector enable bit is set in FC5.

Notes:

1. None.

11 Standby Register (FC10)

The standby register is used to define the timing set output signal levels when in standby. Table B-17 shows the bit definition of the standby register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU			TS05	TS04	TS03	TS02	TS01	ES6	ES5	ES4	ES3	ES2	ES1	ADC	SL

Table B-17 Standby Register Bit Definition

Field/Bit Definition:

SL Output level of STIM_LOAD during the standby state.
ADC Output level of ADEL_CLK during the standby state.
ES1 Output level of ENAB/STR1 during the standby state.
ES2 Output level of ENAB/STR2 during the standby state.
ES3 Output level of ENAB/STR3 during the standby state.
ES4 Output level of ENAB/STR4 during the standby state.
ES5 Output level of ENAB/STR5 during the standby state.
ES6 Output level of ENAB/STR6 during the standby state.
TS01 Output level of TSOUT1 during the standby state.
TS02 Output level of TSOUT1 during the standby state.
TS03 Output level of TSOUT1 during the standby state.
TS04 Output level of TSOUT1 during the standby state.
TS05 Output level of TSOUT1 during the standby state.

Notes:

1. Typically SL thru ES6 would be set to “0”.

12 Clock Generator Registers (FC11)

The clock generator registers allow the user to program the frequency of the internal clock generator. Figure B-8 illustrates the seven clock registers.

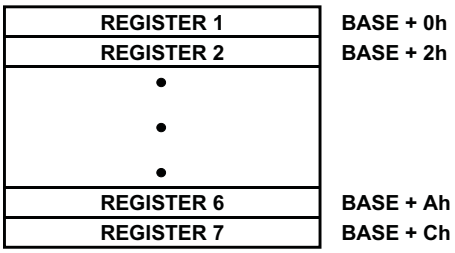


Figure B-8 Clock Generator Control Register Memory Map

12.1 Clock Generator Register 1 (FC11:0x0)

Register 1 is initialized on power up to hex B0F0 and should not be modified.

12.2 Clock Generator Register 2 (FC11:0x2)

Register 2 is initialized on power up to hex 0F00 and should not be modified.

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12.3 Clock Generator Register 3 (FC11:0x4)

Register 3 programs the reference clock selection and power down bit., post divide value and the lower 8 bits of the feedback divide value.

Table B-19 shows the bit definition of the clock generator register 3.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PD	RS	0	0	1	1	1	1	1	0	1	0	0	0

Table B-19 Clock Generator Register 3 Bit Definition

Field/Bit Definition:

RS	Reference Select (1 = external, 0 = internal)
PD	Power down (1 = power down, 0 = normal)

Notes:

1. A 20MHz clock reference would be applied to the SMA CLKIN (option).

12.4 Clock Generator Register 4 (FC11:0x6)

Register 4 programs the post divide value and the lower 8 bits of the feedback divide value.

Table B-18 shows the bit definition of the clock generator register 4.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEEDBACK 7:0								0	0	0	0	PD1		PD0	

Table B-18 Clock Generator Register 4 Bit Definition

Field/Bit Definition:

PD0	Post Divide Zero, see note 1.
PD1	Post Divide One, see note 2.
FEEDBACK 7:0	Lower eight bits of the feedback divide value.

Notes:

1. The two bit post divide zero decode is listed below:

Bit 1	Bit 0	Divide
0	0	1
0	1	2
1	0	4
1	1	8

1. The two bit post divide one decode is listed below:

Bit 3	Bit 2	Divide
0	0	1
1	0	5

12.5 Clock Generator Register 5 (FC11:0x8)

Register 5 programs the upper 6 bits of the feedback divide value.

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Table B-21 shows the bit definition of the clock generator register 5.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	0	1	0	FEEDBACK 13:8					

Table B-21 Clock Generator Register 5 Bit Definition

Field/Bit Definition:

FEEDBACK 13:8 upper six bits of the feedback divide value.

Notes:

1. Frequency - FEEDBACK/1000 *20MHz (min = 80, max = 230MHz)

12.6 Clock Generator Register 6 (FC11:0xA)

Register 6 programs the reference clock selection and the course tune value.

Table B-20 shows the bit definition of the clock generator register 6.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CTUNE				0	0	0	0	XREF			0

Table B-20 Clock Generator Register 6 Bit Definition

Field/Bit Definition:

XREF External reference setting (0 = internal, 7 = external)
CTUNE Course tune.

Notes:

1. None

12.7 Clock Generator Register 7 (FC11:0xC)

Register 7 is a write only register decode that starts the parallel to serial download into the clock generator.

13 Clock Delay Registers (FC12)

The clock delay registers allow the user to program a delay value for external clock input, SMA clock output and J8 clock output.

Figure B-9 illustrates the clock delay registers memory map.

EXTERNAL CLOCK INPUT	**BASE + 0h**
SMA CLOCK OUTPUT	**BASE + 2h**
J8 CLOCK OUTPUT	**BASE + 4h**
EXTERNAL CLOCK LUT	**BASE + (40h - 7Eh)**
SMA CLOCK LUT	**BASE + (80h - BEh)**
J8 CLOCK LUT	**BASE + (C0h - FEh)**

Figure B-9 Clock Delay Register Memory Map

13.1 External Clock Input Delay Register (FC12:0x0)

The external clock input delay register allows the user to program a delay value for the selected external input clock.

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Table B-24 shows the bit definition of the external clock input register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	INDEX					RAWDATA									

Table B-24 External Clock Input Delay Bit Definition

Field/Bit Definition:

RAWDATA	Raw clock input delay value (S = 0)
INDEX	Lookup clock input delay address (S = 1)
S	Select (0 = Raw value, 1 = Lookup value)

Notes:

None

13.2 SMA Clock Output Delay Register (FC12:0x2)

The SMA output clock output delay register allows the user to program a delay value for the SMA clock output.

Table B-23 shows the bit definition of the SMA clock output register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	INDEX					RAWDATA									

Table B-23 SMA Clock Output Delay Bit Definition

Field/Bit Definition:

RAWDATA	Raw SMA clock output delay value (S = 0)
INDEX	Lookup SMA clock output delay address (S = 1)
S	Select (0 = Raw value, 1 = Lookup value)

Notes:

None

13.3 J8 Clock Output Delay Register (FC12:0x4)

The J8 clock output delay register allows the user to program a delay value for the J8 clock output.

Table B-22 shows the bit definition of the J8 clock output register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	INDEX					RAWDATA									

Table B-22 J8 Clock Output Delay Bit Definition

Field/Bit Definition:

RAWDATA	Raw clock input delay value (S = 0)
INDEX	Lookup clock input delay address (S = 1)
S	Select (0 = Raw value, 1 = Lookup value)

Notes:

None

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13.4 External Clock Input Delay LUT (FC12:0x40-0x7E)

The external clock input delay LUT registers allow the user to select a preprogrammed delay value for the selected external clock.

The 32 registers are preprogrammed for delays from 0ns (offset 40_h) to +20ns (offset 66_h).

Table B-27 shows the bit definition of the external clock input lookup table.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LUTVAL									

Table B-27 External Clock Input Lookup Table Bit Definition

Field/Bit Definition:

LUTVAL Raw clock input delay value (S = 0)

Notes:

None

13.5 SMA Clock Output Delay LUT (FC12:0x80-0xBE)

The external clock input delay lookup registers allow the user to select a preprogrammed delay value for the selected external clock.

The 32 registers are preprogrammed for delays from 0ns (offset 40_h) to +20ns (offset 66_h).

Table B-26 shows the bit definition of the SMA clock output lookup table.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LUTVAL									

Table B-26 SMA Clock Output Lookup Table Bit Definition

Field/Bit Definition:

LUTVAL Raw clock input delay value (S = 0)

Notes:

None

13.6 J8 Clock Output Delay LUT (FC12:0xC0-0xFE)

The external clock input delay lookup registers allow the user to select a preprogrammed delay value for the selected external clock.

The 32 registers are preprogrammed for delays from 0ns (offset 80_h) to +20ns (offset $A6_h$).

Table B-25 shows the bit definition of the J8 clock output lookup table .

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LUTVAL									

Table B-25 J8 Clock Output Lookup Table Bit Definition

Field/Bit Definition:

LUTVAL Raw clock input delay value (S = 0)

Notes:

None

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14 Error Memory (FC13)

The error memory contains the first 1024 memory addresses that generate an error.
Figure B-11 illustrates the error memory mapping.

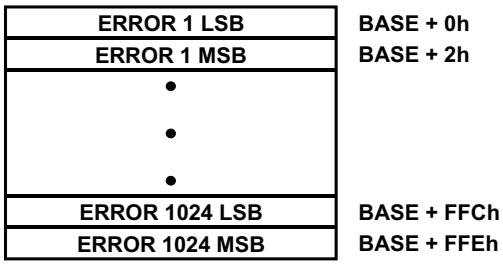


Figure B-11 Error Memory Mapping

Table B-28 shows the bit definition of the error memory.

Word 1 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
Word 1 Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														ADDR[17:16]	

Table B-28 Error Memory Bit Definition

Field/Bit Definition:

ADDR[15:0] Lower 16 bits of the error address.
ADDR[17:16] Upper 2 bits of the error address.

Notes:

None

15 BIT Registers (FC14)

The Function Code reads and writes Built in Test (BIT) registers. These registers are not for user applications.

16 ID/Revision Registers (FC15)

The ID registers contain a unique module id code as well as the module version and revision status.

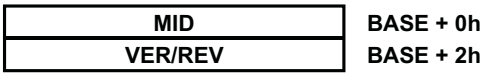


Figure B-10 ID Register Mapping

16.1 Module ID Register (FC15:0x0)

The module id register allows the user to query whether a timing module is installed or not.

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Table B-30 shows the bit definition of the module id register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	MID							NU	MID						

Table B-30 Module ID Register Bit Definition

Field/Bit Definition:

MID Module ID value (A_h/10)

Notes:

None

16.2 Module Version/Revision Register (FC15:0x2)

The version and revision register contains the timing module assembly information.

Table B-29 shows the bit definition of the version/revision register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Revision							

Table B-29 Version/Revision Register Bit Definition

Field/Bit Definition:

Revision Current revision of the firmware for the SR101A
Version Current version of the firmware for the SR101A

Notes:

None

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