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PM603/PM604 Processor/Memory Mezzanine Module and RAM104 DRAM Memory Module User's Manual

PM603A/UM3

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Preface

This manual provides both general and functional descriptions of the product along with connector pin assignments and specifications for the PM603 and PM604 Processor/Memory Mezzanine Modules and the RAM104 DRAM Memory Module used in MVME160*x* Single Board Computers (SBCs).

The information contained in this manual applies to the MVME1603-0*xx* and MVME1604-0*xx* boards, as well as the following PM603, PM604, and RAM104 models:

PM603-001a	PM603-011a	PM603-021a		PM604-001a	PM604-011a	RAM104-001a
PM603-002a	PM603-012a	PM603-022a	PM603-032a	PM604-002a	PM604-012a	RAM104-002a
PM603-003a	PM603-013a	PM603-023a	PM603-033a	PM604-003a	PM604-013a	RAM104-003a
PM603-004a	PM603-014a	PM603-024a	PM603-034a	PM604-004a	PM604-014a	RAM104-004a

This manual is intended for anyone who designs OEM systems, supplies additional capability to existing compatible systems, or works in a lab environment for experimental purposes. It is important to note that a basic knowledge of computers and digital logic is assumed.

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Printed in the United States of America
February 1999

Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must be plugged into an approved three-contact electrical outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

To prevent serious injury, use extreme caution when handling, testing, and adjusting this equipment. Dangerous voltages, capable of causing death are present.

All Motorola printed wiring boards (PWBs) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

WARNING

This equipment generates, uses, and can radiate electro-magnetic energy. It may cause or be susceptible to electro-magnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

If any modifications are made to the product, the modifier assumes responsibility for radio frequency interference issues. Changes or modifications not expressly approved by Motorola Computer Group could void the user's authority to operate the equipment.

European Notice: Board products with the **CE** marking comply with the EMC Directive (89/336/EEC). Marking a system with the **CE** symbol indicates compliance of that Motorola system to the applicable directives of the European Community. A system with the **CE** marking meets or exceeds the following technical standards:

EN55022 (CISPR 22): Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment. Tested to Equipment Class B.

EN50082-1, 1992: Electromagnetic Compatibility -- Generic Immunity Standard, Part 1: Residential, Commercial and Light Industry.

IEC801-2: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements.

IEC801-3: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 3: Radiated Electromagnetic Field Requirements.

IEC801-4: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 4: Electrical Fast Transient/Burst Requirements.

The product also fulfills EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

In accordance with European Community directives, a "Declaration of Conformity" has been made and is on file at Motorola, Inc. - Computer Group, 27 Market Street, Maidenhead, United Kingdom, SL6 8AE.

This board product was tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a **CE**-marked system will maintain the required EMC/safety performance.

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Contents

CHAPTER 1 Description

Introduction 1-1
Features 1-1
Model Designations 1-2
General Description 1-3
Functional Description 1-5
MPC603 Processor 1-5
MPC604 Processor 1-5
MPC105 PCI Bridge/Memory Controller 1-7
EEPROM/Flash 1-7
DRAM 1-8
Control and Status Registers 1-9
CPU Configuration Register 1-9
DRAM Size Register 1-10
Memory Maps 1-12
Installation 1-12
ESD Precautions 1-12
Installation of PM603/PM604 on MVME160x 1-13
Installation of RAM104 on PM603/PM604 1-15

CHAPTER 2 Connector Pin Assignments

Introduction 2-1
Optional RISCWatch Header (J1) 2-1
CPU Connector (J2) 2-2
DRAM Expansion Connectors (J3 and J4) 2-6
Connector to MVME160x Main Module (J5) 2-8

APPENDIX A Related Documentation

Motorola Computer Group Documents A-1
Manufacturers' Documents A-3
Related Specifications A-8

APPENDIX B Specifications

Specifications B-1
Cooling Requirements B-3
EMC Compliance B-4

GLOSSARY

Abbreviations, Acronyms, and Terms GL-1

FIGURES

Figure 1-1. Block Diagram of RAM104 and PM603/PM604 on Base Board 1-4
Figure 1-2. Block Diagram of PM603/PM604 1-6
Figure 1-3. Installing PM603 or PM604 on MVME160x 1-14
Figure 1-4. Installing RAM104 on PM603 or PM604 1-16

TABLES

Table 1-1. PM603, PM604, and RAM104 Model Designations 1-2
Table 1-2. Clock Frequencies Supported by PM603/PM604 1-7
Table 1-3. Minimum ROMFAL and ROMNAL Values 1-8
Table 2-1. RISCWatch Header J1 2-1
Table 2-2. CPU Connector Pin Assignments (J2) 2-2
Table 2-3. Pin Assignments for Connector J4 2-6
Table 2-4. Pin Assignments for Connector J3 2-7
Table 2-5. Pin Assignments for Connector J5 2-8
Table A-1 Motorola Computer Group Documents A-1
Table A-2. Manufacturers' Documents A-3
Table A-3. Related Specifications A-8
Table B-1. PM603/PM604 Specifications B-1
Table B-2. RAM104 Specifications B-2

Description 1

Introduction

This chapter provides information on the PM603 and PM604 Processor/Memory mezzanine modules and the RAM104 DRAM Memory mezzanine modules. These are add-on modules intended for use with the MVME160*x* base boards. In addition, product specifications, cooling requirements, and EMC compliance data are provided in Appendix B.

Note Although both the PM603 and PM604 are discussed in this manual, the PM604 is only available as a part of a factory configured MVME160x bundle. It is no longer available as a stand-alone part number.

Features

- MPC603 superscalar 32-bit or 64-bit RISC microprocessor operating at 200 MHz (PM603);
  - or -
  MPC604 superscalar 32-bit or 64-bit RISC microprocessor operating at 133 MHz (PM604)
- Optional 256 KB of level 2 (L2) secondary cache memory
- 8MB to 64MB shared DRAM on the PM603 or PM604. An additional 8MB to 64MB DRAM may be added as a RAM104 mezzanine that plugs into the PM603 or PM604
- Two 32-pin sockets that can accommodate a total of 1MB Flash memory
- Onboard debugger/monitor and diagnostic firmware for use with the MVME160*x*
- PPC/PCI bridge/memory controller (MPC105 chip)
- 32-bit PCI local bus interface

Model Designations

The PM603 and RAM104 are available in several models as shown in Table 1-1.

Table 1-1. PM603, PM604, and RAM104 Model Designations

Model Number	Speed	Major Differences
PM603-032	200 MHz	MPC603 MPU, 16MB DRAM, 256KB L2 cache
PM603-033	200 MHz	MPC603 MPU, 32MB DRAM, 256KB L2 cache
PM603-034	200 MHz	MPC603 MPU, 64MB DRAM, 256KB L2 cache
RAM104-001a		8 MB DRAM
RAM104-002a		16 MB DRAM
RAM104-003a		32 MB DRAM
RAM104-004a		64 MB DRAM

General Description

The RAM104 is a DRAM Memory module that plugs into the PM603 and PM604 Processor/Memory mezzanine modules that plug into the MVME160*x* Single Board Computers (refer to Figure 1-1).

For the processor/memory module, you initially have the choice of PowerPC 603 or PowerPC 604 with 8 to 64MB of DRAM. There is no parity or ECC protection on the DRAM. The memory is divided into two banks, but not interleaved. This supports read and write bursts of 8-4-4-4. The processor module also has sockets for 1MB of Flash.

The MPC105 bridge/memory controller provides the bridge between the PowerPC microprocessor bus and the PCI local bus. The memory is kept on the processor bus to get the optimum performance from the designs. Electrically, the processor/memory module is a PCI connection. The form factor, however, is unique to this design so as to optimize every square millimeter.

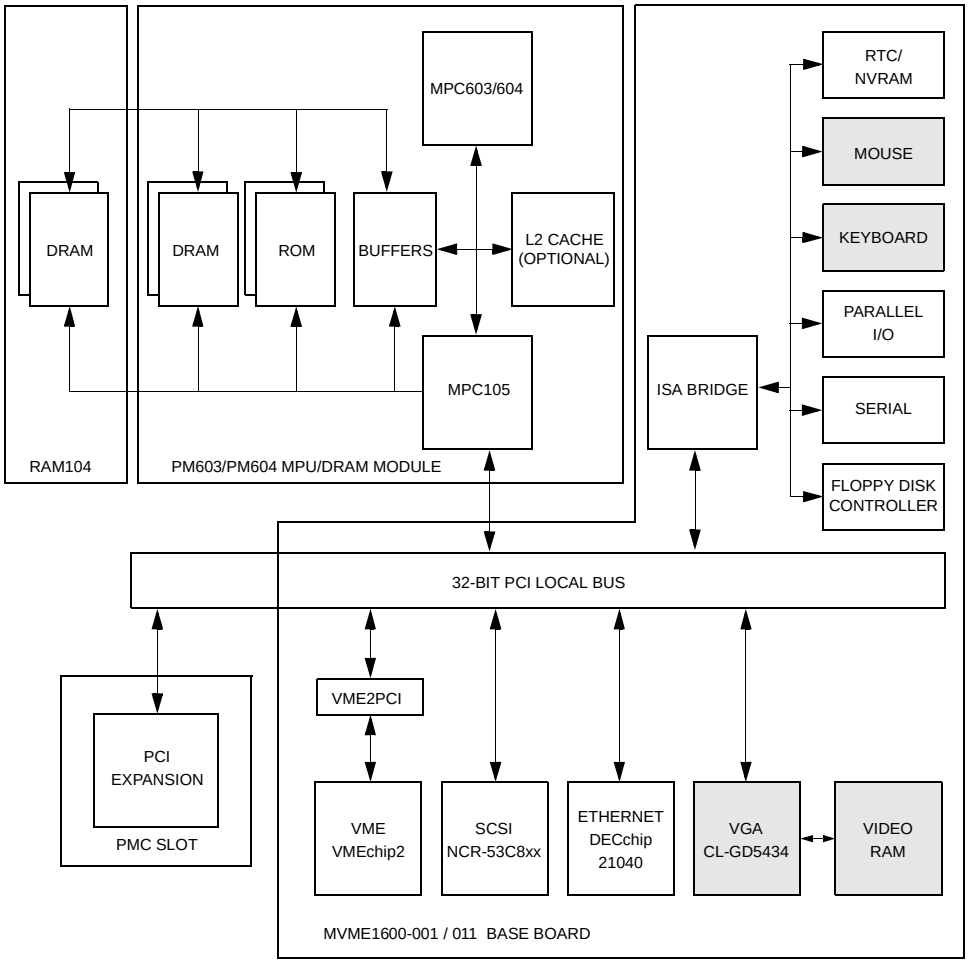
The PM604 modules have a heatsink on the PowerPC 604 that does extend into the next VME slot, so MVME1604 boards have double wide front panels.

Memory can be added to the processor/memory module to expand the memory capacity. RAM104 modules of 8, 16, 32, or 64MB are available for memory expansion. These have only DRAMs and bypass capacitors on them. Adding the memory module on the processor/memory module means that now the stack is three boards high. The PM603 on an MVME160*x* still maintains a single VME slot space with the stacking. It does enter the buffer space that is specified for clearance between cards, but it does not extend beyond the inter-board separation plane.

The onboard monitor/debugger (PPCBug), resides in the Flash memory chips that plug into the two 32-pin sockets(1 MB total, 2 banks 512K x 8). The PPCBug provides:

- boot loader and extensive onboard diagnostics
- single line assembler & disassembler
- configuration save and restore through NVRAM
- remote boot capability

The PM603 and PM604 Processor/Memory mezzanine modules plug into the MVME160*x* Single Board Computers.



NOTES : 1. SHADED BOXES ARE MVME1600-001 FEATURES ONLY.
2. SCSI CONTROLLER IS NCR-53C825 ON MVME1600-001, NCR-53C810 ON -011.

11186.00 9606

Figure 1-1. Block Diagram of RAM104 and PM603/PM604 on Base Board

The complete assembled MVME160*x* runs with software such as Motorola's VMEexec.

The MVME160*x*-00*y* requires a transition module such as an MVME760 to connect it to Ethernet, parallel, and/or serial peripherals. The MVME160x-01*y* requires an MVME712M to connect it to SCSI, Ethernet, parallel, and/or serial peripherals.

Functional Description

The following sections describe the PM603, PM604, and RAM104 in detail. Figure 1-2 is a block diagram of the PM603/PM604.

MPC603 Processor

The PowerPC 603™ (MPC603) microprocessor offers workstation-level performance packed into a low-power, low-cost design ideal for embedded real-time control and monitoring applications. It is a 32-bit or 64-bit (here used as 64-bit) processor with 16KB or 32KB onchip cache (8KB/16KB data cache and 8KB/16KB instruction cache).

The MPC603 has internal clock PLL that supports internal operation at 1x, 2x, 3x, and 4x the SYSCLK frequency. Refer to the chip user's manual listed in Appendix A for further information.

MPC604 Processor

The PowerPC 604™ (MPC604) microprocessor is a high-velocity engine for sophisticated control and mid-range servers. It is a 32-bit or 64-bit (here used as 64-bit) processor with 32KB onchip cache (16KB data cache and 16KB instruction cache).

The MPC604 has internal clock PLL that supports internal operation at 1x, 1.5x, 2x, and 3x the SYSCLK frequency. Refer to the chip user's manual listed in Appendix A for further information.

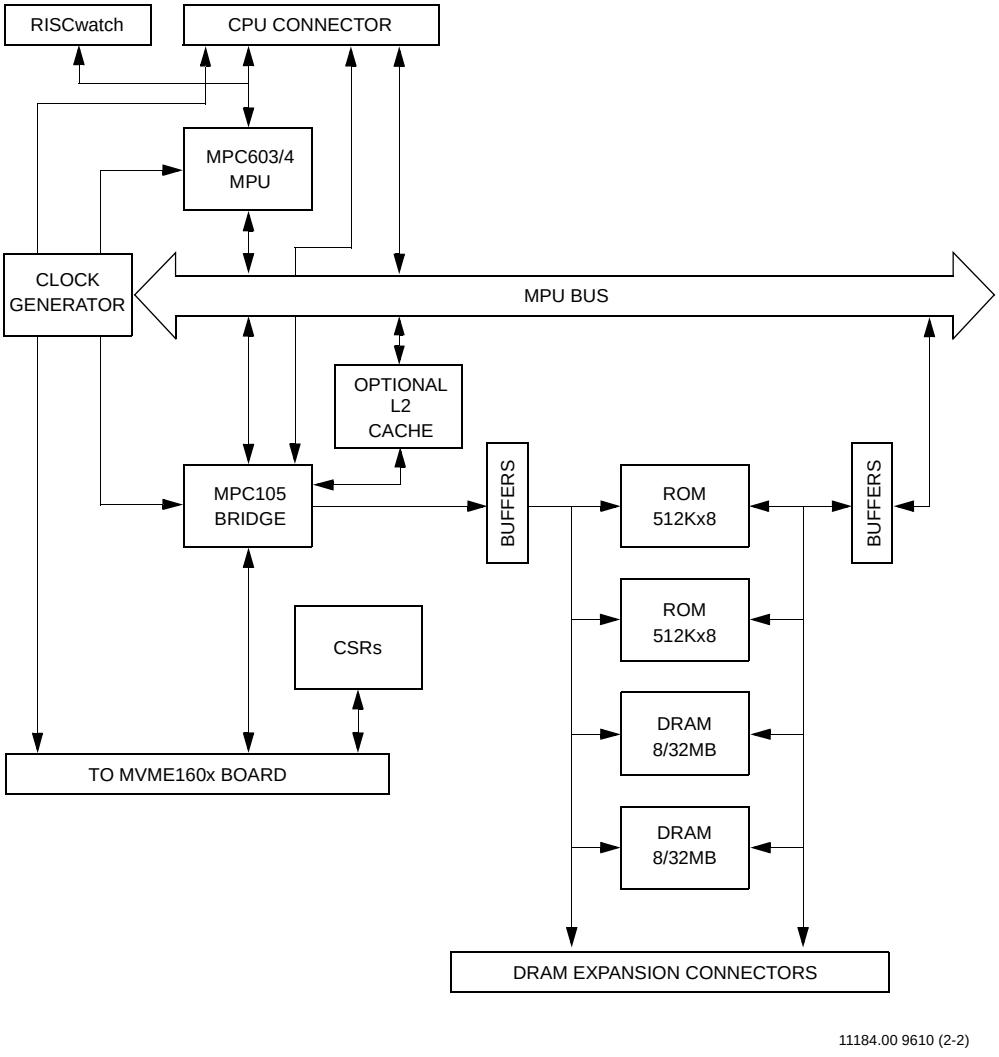


Figure 1-2. Block Diagram of PM603/PM604

MPC105 PCI Bridge/Memory Controller

The Motorola MPC105 device provides the necessary interface between the MPC603/604 processor, the EEPROM/Flash, the DRAM, and the PCI local bus. The MPC105 supports various PowerPC processor external bus frequencies up to 66 MHz and PCI frequencies up to 33 MHz. The following table summarizes the clock frequencies supported by the PM603/PM604:

Table 1-2. Clock Frequencies Supported by PM603/PM604

Processor Type	Internal Processor Speed	Processor External Bus Speed	Processor Clock PLL	MPC105 Internal Clock Frequency	MPC105 External Clock Frequency	MPC105 Clock PLL	PCI Bus Frequency
MPC603	66 MHz	66 MHz	1x	66 MHz	33 MHz	2x	33 MHz
MPC603	100 MHz	50 MHz	2x	50 MHz	25 MHz	2x	25 MHz
MPC603	200 MHz	66 MHz	3x	66 MHz	33 MHz	2x	33 MHz
MPC604	100 MHz	66 MHz	1.5x	66 MHz	33 MHz	2x	33 MHz
MPC604	133 MHz	66 MHz	2x	66 MHz	33 MHz	2x	33 MHz

The MPC105 asserts Machine Check Interrupt (MCP_) to the processor upon detecting a high level on NMI. Refer to *Interrupt Support*s in the *MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide* for additional information.

EEPROM/Flash

Two 32-pin PLCC/CLCC sockets contain the Flash chips. Chip speed is 150 ns. This memory is organized as two banks, each 512K x 8, giving 1MB total memory. 64-bit read or write access takes 80 clock cycles when using a 66 MHz bus clock. The two EEPROM/Flash banks are 8-bit ports controlled by the MPC105. The MPC105 performs byte alignment for write accesses (in Flash configuration) and also packs bytes for 16-bit, 32-bit, and 64-bit read accesses to the EEPROM/Flash area. The Flash memory is onboard programmable.

Because 512Kx8 Flash and EEPROM PLCC devices have different pinouts, zero-ohm resistors are provided for hard-wired configuration. The default hard-wired configuration is for Flash. The onboard monitor/debugger and diagnostic firmware, PPCBug, resides in the Flash chips.

For EEPROM/Flash speed of 150 ns, software must not program ROMFAL and ROMNAL in the MPC105 device with values lower than the following minimum values for various processor external clock frequencies (hardware does not support the burst which NAL is used for):

Table 1-3. Minimum ROMFAL and ROMNAL Values

Processor External Bus Speed	ROMFAL Minimum Value	ROMNAL Minimum Value
25 MHz	4	0
33 MHz	5	0
40 MHz	6	0
50 Mhz	8	0
66 MHz	10	0

DRAM

The MVME160*x* supports 8MB to 128MB of non-interleaved DRAM. 8MB to 64MB of 64-bit DRAM is located on the same module (PM603 or PM604) as the processor. It is in one bank (8MB or 32MB) or two banks (16MB or 64MB), not interleaved, in 300 mil TSOP Type II packaging. An additional 8MB to 64MB of DRAM may be added as a RAM104-*xxx* memory mezzanine module that is plugged into the processor/memory module. This second memory module stacks on the processor/memory module and still fits in a single 0.8 inch VMEbus slot (on the PM603 only; the PM604 has a double-wide front panel and takes two VMEbus slots because of its heatsink). Locating all memory on mezzanine module(s) allows for cost effective field upgrades.

No parity or ECC protection is presently provided for the DRAM.

The DRAM data bus is 64 bits wide, and its address bus is 32 bits wide. Single cycle read or write accesses take 8 clock cycles each. Burst mode read or write accesses, using a 66 MHz bus clock signal, take 8-4-4-4 cycles.

Control and Status Registers

The CPU Configuration Register and the DRAM Size Register are on the PM603/PM604 mezzanine modules. These registers are accessible in ISA I/O space. Note that in the OPER row, R = read only bit, R/W = read or write bit, and W = write only bit.

Resistors on the RAM104 DRAM Memory module are read as part of the DRAM Size Register.

The other control and status registers are on the MVME160*x* main module. These registers are accessible in ISA I/O space. Refer to the *MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide* for further information.

CPU Configuration Register

The CPU Configuration Register provides the configuration information about the PM603/PM604 module. This register resides on the PM603/PM604 mezzanine module, but actual decoding is done by the MVME160*x* board.

REG	CPU Configuration Register - 0800 (hex)							
BIT	SD7	SD6	SD5	SD4	SD3	DS2	SD1	SD0
FIELD	CPUTYPE				CKM1	CKM0	L2P1	L2P0
OPER	R				R	R	R	R
RESET	0001 (binary)				N/A	N/A	N/A	N/A

L2P1-L2P0L2 Cache Present. These bits are defined as follows:

L2P1	L2P0	L2 Cache Size
0	0	512KB
0	1	256KB
1	0	1MB
1	1	L2 Cache Not Present

CKM1-CKM0 Clocking Configuration. These bits reflect the clocking configuration of the PM603/PM604. The encoding for these bits is as follows:

CKM1	CKM0	PCI Bus Clock	CPU External Bus Clock
0	0	33 MHz	33 MHz
0	1	20 MHz	40 MHz
1	0	25 MHz	50 MHz
1	1	33 MHz	66 MHz

CPUTYPE CPU Type. These four bits reflect the CPU type information. For the MVME160*x*, this field is hard wired to 0001 (binary).

DRAM Size Register

The DRAM Size Register is an 8-bit register providing the DRAM size information. Banks 0 and 1 are on the PM603/PM604; Banks 2 and 3 reside on the RAM104 DRAM add-on module. This register resides on the PM603/PM604 module but the actual address decoding is done by the MVME160*x* board.

REG	DRAM Size Register - 0804 (hex)							
BIT	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
FIELD	B2/B3 ASYM_	B2/B3 SIZ2	B2/B3 SIZ1	B2/B3 SIZ0	B0/B1 ASYM_	B0/B1 SIZ2	B0/B1 SIZ1	B0/B1 SIZ0
OPER	R	R	R	R	R	R	R	R
RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

SIZ2 - SIZ0 DRAM Size. These bits provide the DRAM size information for the four banks of DRAM supported by the PM603/PM604. The encoding for these size bits is as follows:

B0/B1 (B2/B3)			DRAM Size	
SIZ2	**SIZ1**	**SIZ0**	**Bank 0 (Bank 2)**	**Bank 1 (Bank 3)**
0	1	1	32 MB (See note)	32 MB (See note)
0	1	0	8 MB	Not Present
0	0	1	32 MB	Not Present
0	0	0	128MB	Not Present
1	1	1	Not Present	Not Present
1	1	0	8 MB	8 MB
1	0	1	32 MB	32 MB
1	0	0	128 MB	128 MB

Note This is for the new 192-MB DRAM mezzanine, used only on the MVME1604-026 and -036 boards. When this mezzanine is used, all six 32-MB banks are populated. It is available only as a factory feature and not as an upgrade option.

ASYM_ Asymmetric Refresh Mode. When cleared, this bit indicates that the DRAM devices installed for Bank 0 and Bank 1 (Bank 2 and Bank 3) have more row address bits than column address bits. This bit is used to determine how to program the MPC105 chip appropriately. Note that, at this time, only the 4M x 4 DRAM devices (32MB banks) have this option. For 4M x4 DRAM, the asymmetric refresh mode is also referred to as the 4K refresh mode. For these devices, there would be 12 row addresses and 10 column addresses.

Memory Maps

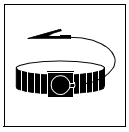
Refer to the *MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide* for memory maps of the PM603 or PM604 processor/memory mezzanine module (and, optionally, the RAM104 memory mezzanine module) as installed on the MVME160*x*. These include maps from the viewpoint of the processor, PCI local bus, and VMEbus.

Installation

The following instructions tell how to install the PM603/PM604 on an MVME160*x* single board computer, and how to install the RAM104 memory mezzanine module on the PM603/PM604 processor/memory mezzanine module.

Refer to the *MVME1603/MVME1604 Single Board Computer Installation and Use* manual for instructions on how to install the MVME160*x* into a backplane or system.

ESD Precautions



Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component on a grounded, static-free surface (if a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available locally) that is attached to an unpainted metal part of the system chassis.

Installation of PM603/PM604 on MVME160*x*

To install a PM603 or PM604 mezzanine on an MVME160*x* module, refer to Figure 1-3 and perform the following steps:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove the chassis or system cover(s) as necessary to gain access into the VMEmodule.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the MVME160*x* from its VMEbus card slot and place it on a clean and adequately protected working surface (preferably an ESD mat) with connectors P1 and P2 (opposite edge of the module from the front panel) facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage the circuits.

4. Place the PM603 or PM604 mezzanine module on top of the MVME160*x*, with the cutout corner at the upper right. Connector J5 at the bottom edge of the PM603 or PM604 should connect smoothly with its corresponding connector on the MVME160*x*.

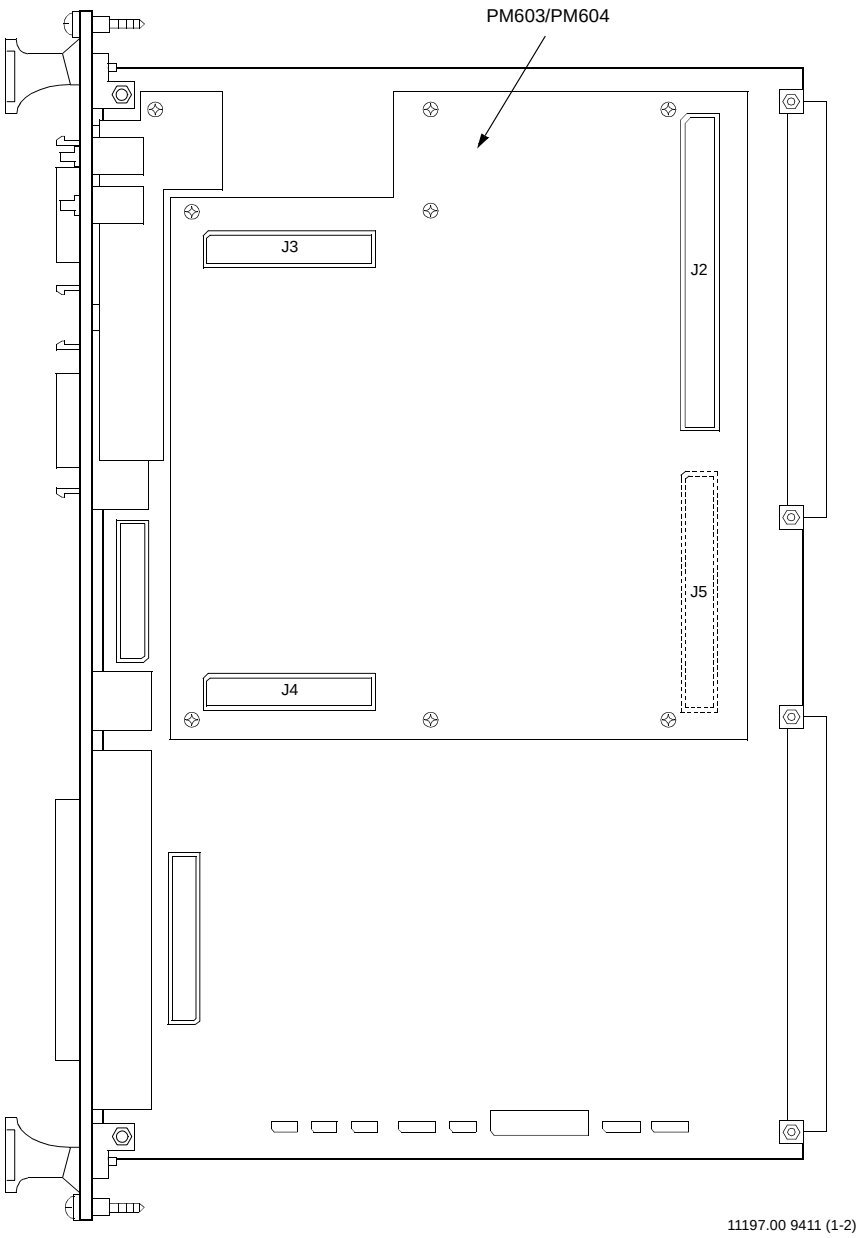


Figure 1-3. Installing PM603 or PM604 on MVME160*x*

5. Align the standoffs on the MVME160*x* board with the holes at the edges of the PM603 or PM604 mezzanine, install the phillips-head screws through the holes in the mezzanine and the spacers. Tighten the screws.
6. Install the MVME160*x* assembly in its proper card slot. Ensure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.
7. Replace the chassis or system cover(s) and connect the system to the AC or DC power source. Turn the equipment power on.

Installation of RAM104 on PM603/PM604

The RAM104 DRAM mezzanine mounts on top of the PM603 or PM604 processor/memory mezzanine. To install a RAM104 mezzanine, refer to Figure 1-4 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

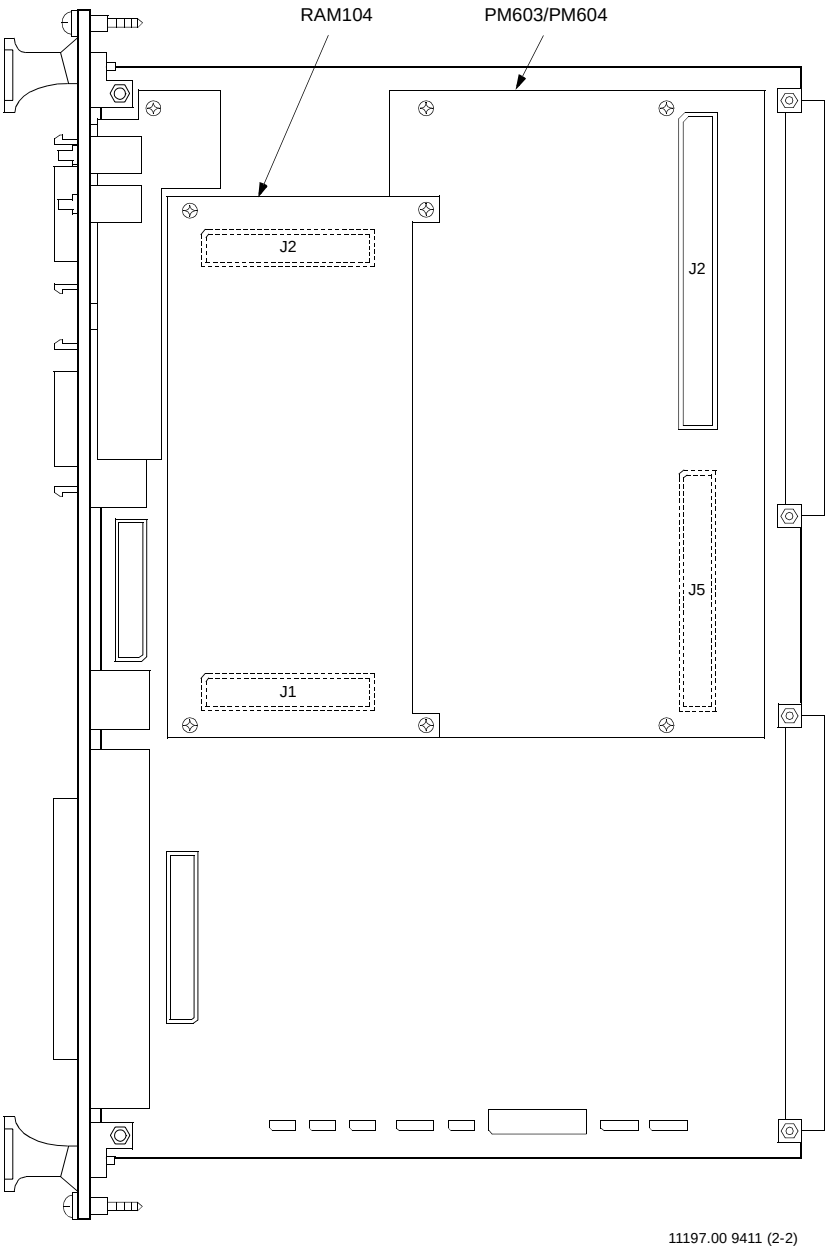


Figure 1-4. Installing RAM104 on PM603 or PM604

3. Carefully remove the MVME160*x* from its VMEbus card slot and place it on a clean and adequately protected working surface (preferably an ESD mat), component side up, with the front panel facing you, and the PM603/PM604 corner cutout at the lower left. Note that the ESD mat should be on a firm surface which does not bow.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

4. Remove four short phillips-head screws from either side of J3/J4 connectors.
5. Pick up the RAM104 mezzanine module, and note the positions of the male guide pins on the RAM104 connectors J1 and J2 at its left and right edges. Also note the positions of the female guide pins on the PM603/PM604 connectors. Align the RAM104 connectors, J2 and J1, with the corresponding connectors J3 and J4 on the PM603/PM604, without actually setting the RAM104 on the PM603/PM604.
6. Set the RAM104 mezzanine module on top of the connectors on the PM603 or PM604 mezzanine. Do NOT press the boards together yet.
7. Visually verify that the male guide pins on the RAM104 connectors are aligned with the female guide pins on the PM603/PM604 connectors. You can only see the guide pins from the sides. Do NOT press the boards together yet.

Caution

Failure to properly align the connectors on the RAM104 and the PM603/PM604 may result in damage to the module's components.

8. Place your thumbs on the top side of the RAM104 mezzanine module (in the middle of and behind each connector, J1 and J2). Press the mezzanine down with both thumbs until the RAM104 and the PM603/PM604 click together.
9. Visually verify that the connectors are fully seated. Connectors J2 and J1 at the left and right edges of the RAM104 should be connected with the corresponding connectors J3 and J4 on the PM603/PM604.
10. Install two long phillips-head screws through the holes at the bottom corners of the RAM104 module and into the standoffs on the MVME160*x*. Install two similar screws in the top (tabbed) corners of the RAM104. Tighten the screws.
11. Reinstall the MVME160*x* assembly in its proper card slot. Be sure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.
12. Replace the chassis or system cover(s) and reconnect the system to the AC or DC power source. Turn the equipment power on.

Connector Pin Assignments 2

Introduction

This chapter provides connector pin assignments for all connectors on the PM603/PM604 boards and the RAM104 board.

Optional RISCWatch Header (J1)

Signals are routed to the pin locations for a 16-pin male 2x8 header J1 (not provided) for connecting to the RISCWatch 603 processor interface. The pin assignment for this header is shown in Table 2-1.

Table 2-1. RISCWatch Header J1

Header J1 Pin No.	MPC603 Pin No. (240-pin QFP)	MPC603 I/O	Signal Name	Resistor
1	198	OUT	TDO	10K pullup
2				
3	199	IN	TDI	10K pullup
4	202	IN	TRST_	220-ohm pulldown
5				
6			3.3V	1K series
7	201	IN	TCK	10K pullup
8				
9	200	IN	TMS	10K pullup
10				
11	189	IN	SRESET_	10K pullup
12				
13	214	IN	HRESET_	10K pullup

Table 2-1. RISCWatch Header J1 (Continued)

Header J1 Pin No.	MPC603 Pin No. (240-pin QFP)	MPC603 I/O	Signal Name	Resistor
14			KEY	
15	216	OUT	CHECKSTOP_	10K pullup
16			GND	

Note QACK_ signal on the MPC603 has a 1K-ohm pull-down resistor to allow the MPC603 processor to enter the state required for reading and writing SCAN string data.

CPU Connector (J2)

This 190-pin SMT connector with a center row of power and ground pins is used to provide access to the processor bus (MPU bus) and some MPC105 signals. This CPU connector may be used to add L2 cache or to upgrade the processor.

Pin numbers and signal mnemonics for J2 are shown in Table 2-2.

Table 2-2. CPU Connector Pin Assignments (J2)

1	PA0		PA1	2
3	PA2		PA3	4
5	PA4		PA5	6
7	PA6		PA7	8
9	PA8		PA9	10
11	PA10		PA11	12
13	PA12		PA13	14
15	PA14		PA15	16
17	PA16		PA17	18
19	PA18	GND	PA19	20

Table 2-2. CPU Connector Pin Assignments (J2) (Continued)

21	PA20		PA21	22
23	PA22		PA23	24
25	PA24		PA25	26
27	PA26		PA27	28
29	PA28		PA29	30
31	PA30		PA31	32
33	PA_PAR0		PA_PAR1	34
35	PA_PAR2		PA_PAR3	36
37	APE*		RSRV*	38
39	PD0		PD1	40
41	PD2		PD3	42
43	PD4		PD5	44
45	PD6		PD7	46
47	PD8		PD9	48
49	PD10		PD11	50
51	PD12		PD13	52
53	PD14		PD15	54
55	PD16		PD17	56
57	PD18	+5V	PD19	58
59	PA20		PD21	60
61	PD22		PD23	62
63	PD24		PD25	64
65	PD26		PD27	66
67	PD28		PD29	68
69	PD30		PD31	70
71	PD32		PD33	72
73	PD34		PD35	74
75	PD36		PD37	76
77	PD38		PD39	78
79	PD40		PD41	80

Table 2-2. CPU Connector Pin Assignments (J2) (Continued)

81	PD42		PD43	82
83	PD44		PD45	84
85	PD46		PD47	86
87	PD48		PD49	88
89	PA50		PD51	90
91	PD52		PD53	92
93	PD54		PD55	94
95	PD56	GND	PD57	96
97	PD58		PD59	98
99	PD60		PD61	100
101	PD62		PD63	102
103	PDPAR0		PDPAR1	104
105	PDPAR2		PDPAR3	106
107	PDPAR4		PDPAR5	108
109	PDPAR6		PDPAR7	110
111	No Connection		No Connection	112
113	DPE*		DBDIS*	114
115	TT0		TSIZ0	116
117	TT1		TSIZ1	118
119	TT2		TSIZ2	120
121	TT3		TC0	122
123	TT4		TC1	124
125	CI*		TC2	126
127	WT*		CSE0	128
129	GLOBAL*		CSE1	130
131	SHARED*		DBWO*	132
133	AACK*	+3.3V	TS*	134
135	ARTY*		XATS*	136
137	DRTY*		TBST*	138
139	TA*		No Connection	140

Table 2-2. CPU Connector Pin Assignments (J2) (Continued)

141	TEA*		No Connection	142
143	No Connection		DBG*	144
145	No Connection		DBB*	146
147	No Connection		ABB*	148
149	TCLK_OUT		CPUGNT*	150
151	L2PRSNT0*		CPUREQ*	152
153	L2ADSC*		IBCINT*	154
155	L2BAA*		MCHK*	156
157	L2DIRTYI*		SMI*	158
159	L2DIRTYO*		CKSTPI*	160
161	L2DOE*		CKSTPO*	162
163	L2DWE1*		HALTED (N/C)	164
165	L2HIT*		TLBISYNC*	166
167	L2TALE		TBEN	168
169	L2TALOE*		SUSPEND*	170
171	L2TOE*	GND	DRVMOD0	172
173	L2TWE*		DRVMOD1 (N/C	174
175	L2TV		NAPRUN (N/C	176
177	L2PRSNT1*		QREQ*	178
179	SRESET*		QACK*	180
181	HRESET*		CPUTDO	182
183	GND		CPUTDI	184
185	CPUCLK1		CPUTCK	186
187	CPUCLK2		CPUTMS	188
189	CPUCLK3		CPUTRST*	190

2

DRAM Expansion Connectors (J3 and J4)

J3 and J4 are two 100-pin SMT connectors on the PM603/PM604 Processor/Memory mezzanine that interface with J2 and J1 (respectively) on the RAM104 add-on DRAM mezzanine. Pin assignments for connectors J3 and J4 are shown in Tables 2-3 and 2-4.

Table 2-3. Pin Assignments for Connector J4

1	GND	MA_BB0	2	51	GND	BCASB7*	52
3	MA_BB1	MA_BB2	4	53	BMD0	GND	54
5	MA_BB3	GND	6	55	GND	BMD1	56
7	GND	MA_BB4	8	57	BMD2	GND	58
9	MA_BB5	MA_BB6	10	59	GND	BMD3	60
11	MA_BB7	GND	12	61	BMD4	GND	62
13	GND	MA_BB8	14	63	GND	BMD5	64
15	MA_BB9	MA_BB10	16	65	BMD6	+5V	66
17	MA_BB11	GND	18	67	+5V	BMD7	68
19	GND	BWEB2*	20	69	BMD8	GND	70
21	BRASB0*	GND	22	71	GND	BMD9	72
23	GND	BRASB1*	24	73	BMD10	+5V	74
25	BRASB2*	GND	26	75	+5V	BMD11	76
27	GND	BRASB3*	28	77	BMD12	GND	78
29	BRASB4*	GND	30	79	GND	BMD13	80
31	GND	BRASB5*	32	81	BMD14	+5V	82
33	BRASB6*	GND	34	83	+5V	BMD15	84
35	GND	BRASB7*	36	85	BMD16	GND	86
37	BCASB0*	GND	38	87	GND	BMD17	88
39	GND	BCASB1*	40	89	BMD18	+5V	90
41	BCASB2*	GND	42	91	+5V	BMD19	92
43	GND	BCASB3*	44	93	BMD20	GND	94
45	BCASB4*	GND	46	95	GND	BMD21	96
47	GND	BCASB5*	48	97	BMD22	+5V	98
49	BCASB6*	GND	50	99	+5V	BMD23	100

Table 2-4. Pin Assignments for Connector J3

1	BWEB3*	GND	2	51	GND	BMD48	52
3	GND	BMD24	4	53	BMD49	GND	54
5	BMD25	GND	6	55	GND	BMD50	56
7	GND	BMD26	8	57	BMD51	+3.3V	58
9	BMD27	GND	10	59	+3.3V	BMD52	60
11	GND	BMD28	12	61	BMD53	GND	62
13	BMD29	GND	14	63	GND	BMD54	64
15	GND	BMD30	16	65	BMD55	+3.3V	66
17	BMD31	GND	18	67	+3.3V	BMD56	68
19	GND	BMD32	20	69	BMD57	GND	70
21	BMD33	GND	22	71	GND	BMD58	72
23	GND	BMD34	24	73	BMD59	+3.3V	74
25	BMD35	GND	26	75	+3.3V	BMD60	76
27	GND	BMD36	28	77	BMD61	GND	78
29	BMD37	GND	30	79	GND	BMD62	80
31	GND	BMD38	32	81	BMD63	+3.3V	82
33	BMD39	GND	34	83	+3.3V	BDP0	84
35	GND	BMD40	36	85	BDP1	BDP2	86
37	BMD41	GND	38	87	BDP3	GND	88
39	GND	BMD42	40	89	GND	BDP4	90
41	BMD43	GND	42	91	BDP5	BDP6	92
43	GND	BMD44	44	93	BDP7	+3.3V	94
45	BMD45	GND	46	95	+3.3V	No Conn.	96
47	GND	BMD46	48	97	B3SIZ0	B3SIZ1	98
49	BMD47	GND	50	99	B4SIZ0	B4SIZ1	100

2

Connector to MVME160*x* Main Module (J5)

The PM603/PM604 Processor/Memory mezzanine module interfaces with the MVME160*x* main module through a 152-pin AMP Mictor SMT connector. This connector provides power to the PM603/PM604 module and the PCI interface between the two boards. The PCI clocks are received from the PM603/PM604 module which determines the PCI frequency of operation.

Pin numbers and signal mnemonics for J5 are shown in Table 2-7.

Table 2-5. Pin Assignments for Connector J5

1	PCICLK1		PCICLK2	2
3	PCICLK3		PCICLK4	4
5	GND		GND	6
7	CKSTOP*		CPULED*	8
9	IBCINT*		ABORT*	10
11	LANINT*		VME2PCIINT*	12
13	SCSIINT*		GRINT*	14
15	PMCIRQ*		KBIRQ	16
17	MOUSEIRQ		COM1IRQ	18
19	COM2IRQ	GND	PARPTIRQ	20
21	CIO_IRQ*		SCC_IRQ*	22
23	FLPYIRQ*		IRQ_B*	24
25	SMI*		SRESET*	26
27	NMI		LBRESET*	28
29	TBEN		PURESET*	30
31	TCK		TDO1	32
33	TDI1		TMS	34
35	PMCP*		TRST*	36
37	PMCREQ*		PMCGNT*	38
39	ISA_MSTR*		FLSHREQ*	40
41	SD7		FLSHACK*	42
43	SD6		Reserved	44

Table 2-5. Pin Assignments for Connector J5 (Continued)

45	SD5		RAMCFG*	46
47	SD4		CPUCNFG*	48
49	SD3		X_IOR*	50
51	SD2		X_IOW*	52
53	SD1		SA1	54
55	SD0		SA0	56
57	–12V	+5V	+12V	58
59	SERR*		PERR*	60
61	SDONE		LOCK*	62
63	SBO*		DEVSEL*	64
65	GND		GND	66
67	IRDY*		TRDY*	68
69	FRAME*		STOP*	70
71	GND		GND	72
73	PCIGNT*		ACK64*	74
75	PCIREQ*		REQ64*	76
77	Reserved		PAR	78
79	CBE0*		CBE1*	80
81	CBE2*		CBE3*	82
83	AD0		AD1	84
85	AD2		AD3	86
87	AD4		AD5	88
89	AD6		AD7	90
91	AD8		AD9	92
93	AD10		AD11	94
95	AD12	GND	AD13	96
97	AD14		AD15	98
99	AD16		AD17	100
101	AD18		AD19	102
103	AD20		AD21	104
105	AD22		AD23	106
107	AD24		AD25	108

Table 2-5. Pin Assignments for Connector J5 (Continued)

109	AD26		AD27	110
111	AD28		AD29	112
113	AD30		AD31	114
115	PCI_RESV5		PAR64	116
117	CBE4*		CBE5*	118
119	CBE6*		CBE7*	120
121	AD32		AD33	122
123	AD34		AD35	124
125	AD36		AD37	126
127	AD38		AD39	128
129	AD40		AD41	130
131	AD42		AD43	132
133	AD44	+3.3V	AD45	134
135	AD46		AD47	136
137	AD48		AD49	138
139	AD50		AD51	140
141	AD52		AD53	142
143	AD54		AD55	144
145	AD56		AD57	146
147	AD58		AD59	148
149	AD60		AD61	150
151	AD62		AD63	152

Related Documentation A

Motorola Computer Group Documents

This product has an installation and use manual. This manual along with additional product documentation may be ordered by using any of the following methods

Note If you need additional information about this product, you may also want to order one or more of the documents listed throughout this appendix.

- Contacting your local Motorola sales office.
- Accessing the World Wide Web site **http//: www.mcg.mot.com** (listed on the back cover of this and other MCG manuals) and selecting “Product Literature”.
- (USA and Canada only) - Contacting the Literature Center via phone or FAX at the numbers listed under *Product Literature* at MCG’s World Wide Web site (above).

Any supplements issued for a specific revision of a manual or guide are furnished with that document. The “type” and “revision level” of a specific manual are indicated by the last three characters of the document number, such as “/IH2” (the second revision of an installation manual); a supplement bears the same number as a manual but has two additional characters that indicate the revision level of the supplement, for example “/IH2A1” (the first supplement to the second edition of the installation manual).

Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
MVME1603/MVME1604 Single Board Computer Installation and Use*	V1600-1A/IH
MVME1603/MVME1604 Single Board Computer Programmer’s Reference Guide*	V1600-1A/PG
PM603/PM604 Processor/Memory Mezzanine Module and RAM104 DRAM Memory Module User’s Manual*	PM603A/UM

Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
PPCBug Firmware Package User's Manual (Parts 1 and 2)*	PPCBUGA1/UM PPCBUGA2/UM
PPC1Bug Diagnostics Manual*	PPC1DIAA/UM
MVME712M Transition Module and P2 Adapter Board User's Manual	MVME712M/D
MVME760 Transition Module User's Manual	VME760A/UM
SIM705 Serial Interface Module Installation Guide	SIM705A/IH

Note Motorola documents marked with a * in the above list can be purchased as a set under part number **LK-V1600-1**.

Manufacturers' Documents

Table A-2 lists the manufacturers' data sheets and other useful manuals. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

To further assist your development effort, Motorola has collected some of the non-Motorola documents in this list from the suppliers. This bundle can be ordered as part number **68-PCIKIT**.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
PowerPC 603™ RISC Microprocessor Technical Summary Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430	MPC603/D
PowerPC 603™ RISC Microprocessor User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC603UM/AD MPR603UMU-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PowerPC 604™ RISC Microprocessor User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC604UM/AD MPR604UMU-01
MPC105 PCI Bridge/Memory Controller User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430	MPC105UM/AD
PowerPC™ Microprocessor Family: The Programming Environments Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/AD MPRPPCFPE-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Alpine™ VGA Family - CL-GD543X Technical Reference Manual Third Edition Cirrus Logic, Inc. (or nearest Sales Office) 3100 West Warren Avenue Fremont, California 94538-6423 Telephone: (510) 623-8300 FAX: (510) 226-2180	GD543X-TRM-003 (part number 385439-003)
DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-N0752-72
PC87303VUL (Super I/O™ Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87303VUL
PC87323VF (Super I/O™ Sidewinder) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87323VF

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
M48T18 CMOS 8K x 8 TIMEKEEPER™ SRAM Data Sheet SGS-Thomson Microelectronics Group Marketing Headquarters (or nearest Sales Office) 1000 East Bell Road Phoenix, Arizona 85022 Telephone: (602) 867-6100	M48T18
DS1643 Nonvolatile Timekeeping RAM Data Manual Dallas Semiconductor 4401 South Beltwood Parkway Dallas, Texas 75244-3292	DS1643/ DS1643LPM
82378 System I/O (SIO) PCI-to-ISA Bridge Controller Intel Corporation Literature Sales P.O. Box 7641 Mt. Prospect, Illinois 60056-7641 Telephone: 1-800-548-4725	290473-003
SYM 53CXX (was NCR 53C8XX) Family PCI-SCSI I/O Processors Programming Guide Symbios Logic Inc. 1731 Technology Drive, suite 600 San Jose, CA95110 Telephone: (408) 441-1080 Hotline: 1-800-334-5454	J10931I
SCC (Serial Communications Controller) User's Manual (for Z85230 and other Zilog parts) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8293-02

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification and User's Manual (in Z8000® Family of Products Data Book) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8319-00
CS4231 Parallel Interface, Multimedia Audio Codec Data Sheet Crystal Semiconductor Corporation 4210 South Industrial Drive P.O. Box 17847 Austin, Texas 78744-7847 Telephone: 1-800-888-5016 Telephone: (512) 445-7222 FAX: (512) 445-7581	DS111PP4
CSB4231/4248 Evaluation Board Data Sheet Crystal Semiconductor Corporation 4210 South Industrial Drive P.O. Box 17847 Austin, Texas 78744-7847 Telephone: 1-800-888-5016 Telephone: (512) 445-7222 FAX: (512) 445-7581	DS111DB4
Award Classic KB42 Keyboard Controller Firmware for the National Semiconductor PC87323VUL-IAB SuperI/O™ Device Award Software International, Inc. Sales and Marketing 777 E. Middlefield Road Mountain View, California 94043 Telephone: (415) 968-4433	Award Classic KB42

Related Specifications

Table A-3 lists the product's related specifications. The appropriate source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
ANSI Small Computer System Interface-2 (SCSI-2), Draft Document Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181	X3.131.1990
ANSI Std X3T9.2, 1994 AT Attachment Interface for Disk Drives Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181	ANSI X3.221
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE Standard 1284
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386 Draft 2.0

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1 Draft 2.0
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02
VME64 Specification VITA (VMEbus International Trade Association) 7825 E. Gelding Drive, Suite 104 Scottsdale, Arizona 85260-3415 Telephone: (602) 951-8866 FAX: (602) 951-0720 **NOTE:** An earlier version of this specification is available as: Versatile Backplane Bus: VMEbus Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333 OR Microprocessor system bus for 1 to 4 byte data Bureau Central de la Commission Electrotechnique Internationale 3, rue de Varembé Geneva, Switzerland	ANSI/VITA 1-1994 ANSI/IEEE Standard 1014-1987 IEC 821 BUS

Specifications

This appendix provides general specifications for the PM603, PM604, and the RAM104.

- Specifications for the PM603 and PM604 are listed in Table B-1.
- Specifications for the RAM104 are listed in Table B-2.

Table B-1. PM603/PM604 Specifications

Characteristics	Specifications
Power requirements (Processor/Memory mezzanine module only)	+3.3 Vdc (± 2.5%), 0.8 A typ., 1.2 A max. (for PM603 @ 66 MHz); 1.0 A typ., 1.5 A max. (for PM603 @ 100 MHz) 2.7 A typ., 4.2 A max. (for PM604 @ 100 MHz) 3.4 A typ., 4.8 A max. (for PM604 @ 133 MHz) +5 Vdc (± 2.5%), 1.5 A typ., 2.2 A max. (for PM603 @ 66 MHz); 1.6 A typ., 2.3 A max. (for PM603 @ 100 MHz) 1.5 A typ., 2.2 A max. (for PM604 @ 100 MHz) 1.6 A typ., 2.3 A max. (for PM604 @ 133 MHz)

B

Table B-1. PM603/PM604 Specifications (Continued)

Characteristics	Specifications
Operating temperature (refer to *Cooling Requirements* section)	0° to 55° C at point of exit of forced air (approximately 490 LFM)
Storage temperature	-40° to +85° C
Relative humidity	5% to 90% (non-condensing)
Physical dimensions (Processor/Memory mezzanine module only) Width Depth Height	 144 mm (5.63 inches) 133 mm (5.2 inches) 15.0 mm (0.59 inches) (maximum, PM603) 25.4 mm (1.0 inches) (maximum, PM604)

Table B-2. RAM104 Specifications

Characteristics	Specifications
Power requirements (DRAM Memory module only)	+5 Vdc (± 2.5%), 1.0 A typical, 1.5 A max.
Operating temperature (refer to *Cooling Requirements* section)	0° to 55° C at point of exit of forced air (approximately 490 LFM)
Storage temperature	-40° to +85° C
Relative humidity	5% to 90% (non-condensing)
Physical dimensions (DRAM Memory module only) Width Depth Thickness (PWB only)	 119 mm (4.70 inches) 64 mm (2.50 inches) 2.03 mm (0.080 inches)

Cooling Requirements

The Motorola RAM104 DRAM Memory module is specified, designed, and tested to operate reliably when mounted on a PM603 or PM604 Processor/Memory mezzanine module (which is itself mounted on an MVME160*x* board) with an incoming air temperature range from 0° to 55° C (32° to 131° F) with forced air cooling at a velocity typically achievable by using a 100 CFM axial fan.

Temperature qualification is performed in a standard Motorola VMEsystem chassis. Twenty-five watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 100 CFM per fan, is placed directly under the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55° C with increased airflow.

It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

B

EMC Compliance

The RAM104 was mounted on a PM603 or PM604, which was mounted on an MVME1603 or MVME1604 Single Board Computer, which was tested in an EMC-compliant chassis and meets the requirements for EN55022 Class B equipment. Compliance was achieved under the following conditions:

- Shielded cables on all external I/O ports.
- Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

Glossary

Abbreviations, Acronyms, and Terms

This Glossary defines some of the abbreviations, acronyms, and key terms used in this document.

10base-5	See thick Ethernet.
10base-2	See thin Ethernet.
10base-T	See twisted-pair Ethernet.
ACIA	**A**synchronous **C**ommunications **I**nterface **A**dapter
AIX	**A**dvanced **I**nteractive e**X**ecutive (IBM version of UNIX)
architecture	The main overall design in which each individual hardware component of the computer system is interrelated. The most common uses of this term are 8-bit, 16-bit, or 32-bit architectural design systems.
ASCII	**A**merican **S**tandard **C**ode for **I**nformation **I**nterchange. This is a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to 8-bits to encode a total of 256 alphanumeric and control characters.
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
AUI	**A**ttachment **U**nit **I**nterface
BBRAM	Battery Backed-up Random Access Memory
bi-endian	Having big-endian and little-endian byte ordering capability.
big-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.
BIOS	**B**asic **I**nput/**O**utput **S**ystem. This is the built-in program that controls the basic functions of communications between the processor and the I/O (peripherals) devices. Also referred to as ROM BIOS.

BitBLT	**Bit** Boundary **BL**ock **T**ransfer. A type of graphics drawing routine that moves a rectangle of data from one area of display memory to another. The data specifically need not have any particular alignment.
BLT	**BL**ock **T**ransfer
board	The term more commonly used to refer to a PCB (printed circuit board). Basically, a flat board made of nonconducting material, such as plastic or fiberglass, on which chips and other electronic components are mounted. Also referred to as a circuit board or card.
bpi	**b**its **p**er **i**nch
bps	**b**its **p**er **s**econd
bus	The pathway used to communicate between the CPU, memory, and various input/output devices, including floppy and hard disk drives. Available in various widths (8-, 16-, and 32-bit), with accompanying increases in speed.
cache	A high-speed memory that resides logically between a central processing unit (CPU) and the main memory. This temporary memory holds the data and/or instructions that the CPU is most likely to use over and over again and avoids accessing the slower hard or floppy disk drive.
CAS	**C**olumn **A**ddress **S**trobe. The clock signal used in dynamic RAMs to control the input of column addresses.
CD	**C**ompact **D**isc. A hard, round, flat portable storage unit that stores information digitally.
CD-ROM	**C**ompact **D**isk **R**ead-**O**nly **M**emory
CFM	**C**ubic **F**eet per **M**inute
CISC	**C**omplex-**I**nstruction-**S**et **C**omputer. A computer whose processor is designed to sequentially run variable-length instructions, many of which require several clock cycles, that perform complex tasks and thereby simplify programming.
CODEC	**CO**der/**DEC**oder

Color Difference (CD) The signals of (R-Y) and (B-Y) without the luminance (-Y) signal. The Green signals (G-Y) can be extracted by these two signals.

Composite Video Signal (CVS/CVBS) Signal that carries video picture information for color, brightness and synchronizing signals for both horizontal and vertical scans. Sometimes referred to as “Baseband Video”.

cpi **c**haracters **p**er **i**nch

cpl **c**haracters **p**er **l**ine

CPU **C**entral **P**rocessing **U**nit. The master computer unit in a system.

DCE **D**ata **C**ircuit-terminating **E**quipment.

DLL **D**ynamic **L**ink **L**ibrary. A set of functions that are linked to the referencing program at the time it is loaded into memory.

DMA **D**irect **M**emory **A**ccess. A method by which a device may read or write to memory directly without processor intervention. DMA is typically used by block I/O devices.

DOS **D**isk **O**perating **S**ystem

dpi **d**ots **p**er **i**nch

DRAM **D**ynamic **R**andom **A**ccess **M**emory. A memory technology that is characterized by extreme high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.

DTE **D**ata **T**erminal **E**quipment.

ECC **E**rror **C**orrection **C**ode

ECP **E**xtended **C**apability **P**ort

EEPROM **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down.

EISA (bus) **E**xtended **I**ndustry **S**tandard **A**rchitecture (bus) (IBM). An architectural system using a 32-bit bus that allows data to be transferred between peripherals in 32-bit chunks instead of 16-bit or 8-bit that most systems use. With the transfer of larger bits of information, the machine is able to perform much faster than the standard ISA bus system.

EPP **E**nhanced **P**arallel **P**ort

EPROM	**E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written once (per erasure cycle) and read many times.
ESCC	**E**nhanced **S**erial **C**ommunication **C**ontroller
ESD	**E**lectro-**S**tatic **D**ischarge/Damage
Ethernet	A local area network standard that uses radio frequency signals carried by coaxial cables.
FDC	**F**loppy **D**isk **C**ontroller
FDDI	**F**iber **D**istributed **D**ata **I**nterface. A network based on the use of optical-fiber cable to transmit data in non-return-to-zero, invert-on-1s (NRZI) format at speeds up to 100 Mbps.
FIFO	**F**irst-**I**n, **F**irst-**O**ut. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.
firmware	The program or specific software instructions that have been more or less permanently burned into an electronic component, such as Read-Only Memory (ROM) or Erasable Programmable Read-Only Memory (EPROM).
frame	One complete television picture frame consists of 525 horizontal lines with the NTSC system. One frame consists of two fields.
graphics controller	On EGA and VGA, a section of circuitry that can provide hardware assist for graphics drawing algorithms by performing logical functions on data written to display memory.
HAL	**H**ardware **A**bstraction **L**ayer. The lower level hardware interface module of the Windows NT operating system. It contains platform specific functionality.
hardware	A computing system is normally spoken of as having two major components: hardware and software. Hardware is the term used to describe any of the physical embodiments of a computer system, with emphasis on the electronic circuits (the computer) and electromechanical devices (peripherals) that make up the system.
HCT	**H**ardware **C**onformance **T**est. A test used to ensure that both hardware and software conform to the Windows NT interface.

I/O	**I**nput/**O**utput
IBC	PCI/**I**SA **B**ridge **C**ontroller
IDE	**I**ntelligent **D**evice **E**xpansion
IEEE	**I**nstitute of **E**lectrical and **E**lectronics **E**ngineers
interlaced	A graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. The advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware. It also may make it possible to display a resolution that would otherwise be impossible on given hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a few scanlines high.
IQ Signals	Similar to the color difference signals (R-Y) (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.
ISA (bus)	**I**ndustry **S**tandard **A**rchitecture (bus). The de facto standard system bus for IBM-compatible computers until the introduction of VESA and PCI. Used in the reference platform specification. (IBM)
ISASIO	**ISA S**uper **I**nput/**O**utput device
ISDN	**I**ntegrated **S**ervices **D**igital **N**etwork. A standard for digitally transmitting video, audio, and electronic data over public phone networks.
LAN	**L**ocal **A**rea **N**etwork
LED	**L**ight-**E**mitting **D**iode
LFM	**L**inear **F**eet per **M**inute
little-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.
MBLT	**M**ultiplexed **BL**ock **T**ransfer
MCA (bus)	**M**icro **C**hannel **A**rchitecture
MCG	**M**otorola **C**omputer **G**roup

MFM	**M**odified **F**requency **M**odulation
MIDI	**M**usical **I**nstrument **D**igital **I**nterface. The standard format for recording, storing, and playing digital music.
MPC	**M**ultimedia **P**ersonal **C**omputer
MPC105	The PowerPC-to-PCI bus bridge chip developed by Motorola for the Ultra 603/Ultra 604 system board. It provides the necessary interface between the MPC603/MPC604 processor and the Boot ROM (secondary cache), the DRAM (system memory array), and the PCI bus.
MPC601	Motorola's component designation for the PowerPC 601 microprocessor.
MPC603	Motorola's component designation for the PowerPC 603 microprocessor.
MPC603e	Motorola's component designation for the PowerPC 603e microprocessor.
MPC604	Motorola's component designation for the PowerPC 604 microprocessor.
MPU	**M**icro**P**rocessing **U**nit
MTBF	**M**ean **T**ime **B**etween **F**ailures. A statistical term relating to reliability as expressed in power on hours (poh). It was originally developed for the military and can be calculated several different ways, yielding substantially different results. The specification is based on a large number of samplings in one place, running continuously, and the rate at which failure occurs. MTBF is not representative of how long a device, or any individual device is likely to last, nor is it a warranty, but rather, of the relative reliability of a family of products.
multisession	The ability to record additional information, such as digitized photographs, on a CD-ROM after a prior recording session has ended.
non-interlaced	A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, and is usually said to have a more pleasing appearance.

nonvolatile memory	A memory in which the data content is maintained whether the power supply is connected or not.
NTSC	**N**ational **T**elevision **S**tandards **C**ommittee (USA)
NVRAM	**N**on-**V**olatile **R**andom **A**ccess **M**emory
OEM	**O**riginal **E**quipment **M**anufacturer
OMPAC	**O**ver - **M**olded **P**ad **A**rray **C**arrier
OS	**O**perating **S**ystem. The software that manages the computer resources, accesses files, and dispatches programs.
OTP	**O**ne-**T**ime **P**rogrammable
palette	The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 or 256 simultaneous colors out of 262,144.
parallel port	A connector that can exchange data with an I/O device eight bits at a time. This port is more commonly used for the connection of a printer to a system.
PCI (local bus)	**P**eripheral **C**omponent **I**nterconnect (local bus) (Intel). A high-performance, 32-bit internal interconnect bus used for data transfer to peripheral controller components, such as those for audio, video, and graphics.
PCMCIA (bus)	**P**ersonal **C**omputer **M**emory **C**ard **I**nternational **A**ssociation (bus). A standard external interconnect bus which allows peripherals adhering to the standard to be plugged in and used without further system modification.
PDS	**P**rocessor **D**irect **S**lot
physical address	A binary address that refers to the actual location of information stored in secondary storage.
PIB	**P**CI-to-**I**SA **B**ridge
pixel	An acronym for picture element, and is also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.
PLL	**P**hase-**L**ocked **L**oop
PMC	**P**CI **M**ezzanine **C**ard

POWER — **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC architecture (IBM)

PowerPC™ — The trademark used to describe the **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC microprocessor architecture for **P**ersonal **C**omputers developed by the IBM Corporation. PowerPC is superscalar, which means it can handle more than one instruction per clock cycle. Instructions can be sent simultaneously to three types of independent execution units (branch units, fixed-point units, and floating-point units), where they can execute concurrently, but finish out of order. PowerPC is used by Motorola, Inc. under license from IBM.

PowerPC 601™ — The first implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 256-entry buffer and a 32KB unified (instruction and data) cache. It provides a 64-bit data bus and a separate 32-bit address bus. PowerPC 601 is used by Motorola, Inc. under license from IBM.

PowerPC 603™ — The second implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 64-entry buffer and an 8KB (instruction and data) cache. It provides a selectable 32-bit or 64-bit data bus and a separate 32-bit address bus. PowerPC 603 is used by Motorola, Inc. under license from IBM.

PowerPC 603e™ — A variant of the second implementation of the PowerPC family of microprocessors. This CPU incorporates a faster clock (100MHz) and 256KB L2 cache. PowerPC 603e is used by Motorola, Inc. under license from IBM.

PowerPC 604™ — The third implementation of the PowerPC family of microprocessors. PowerPC 604 is used by Motorola, Inc. under license from IBM.

PowerPC Reference Platform (PRP) — A specification published by the IBM Power Personal Systems Division which defines the devices, interfaces, and data formats that make up a PRP-compliant system using a PowerPC processor.

PowerStack™ RISC PC (System Board)
A PowerPC-based computer board platform developed by the Motorola Computer Group. It supports Microsoft's Windows NT and IBM's AIX operating systems.

PRP See PowerPC Reference Platform (PRP).

PRP-compliant See PowerPC Reference Platform (PRP).

PRP Spec See PowerPC Reference Platform (PRP).

PROM **P**rogrammable **R**ead-**O**nly **M**emory

PS/2 **P**ersonal **S**ystem/**2** (IBM)

QFP **Q**uad **F**lat **P**ackage

RAM **R**andom-**A**ccess **M**emory. The temporary memory that a computer uses to hold the instructions and data currently being worked with. All data in RAM is lost when the computer is turned off.

RAS **R**ow **A**ddress **S**trobe. A clock signal used in dynamic RAMs to control the input of the row addresses.

Reduced-Instruction-Set Computer (RISC)
A computer in which the processor's instruction set is limited to constant-length instructions that can usually be executed in a single clock cycle.

RFI **R**adio **F**requency **I**nterference

RGB The three separate color signals: **R**ed, **G**reen, and **B**lue. Used with color displays, an interface that uses these three color signals as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

RISC See Reduced Instruction Set Computer (RISC).

ROM **R**ead-**O**nly **M**emory

RTC **R**eal-**T**ime **C**lock

SBC **S**ingle **B**oard **C**omputer

SCSI **S**mall **C**omputer **S**ystems **I**nterface. An industry-standard high-speed interface primarily used for secondary storage. SCSI-1 provides up to 5 Mbps data transfer.

SCSI-2 (Fast/Wide)	An improvement over plain SCSI; and includes command queuing. Fast SCSI provides 10 Mbps data transfer on an 8-bit bus. Wide SCSI provides up to 40 Mbps data transfer on a 16- or 32-bit bus.
serial port	A connector that can exchange data with an I/O device one bit at a time. It may operate synchronously or asynchronously, and may include start bits, stop bits, and/or parity.
SIM	**S**erial **I**nterface **M**odule
SIMM	**S**ingle **I**nline **M**emory **M**odule. A small circuit board with RAM chips (normally surface mounted) on it designed to fit into a standard slot.
SIO	**S**uper **I/O** controller
SMP	**S**ymmetric **M**ulti**P**rocessing. A computer architecture in which tasks are distributed among two or more local processors.
SMT	**S**urface **M**ount **T**echnology. A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.
software	A computing system is normally spoken of as having two major components: hardware and software. Software is the term used to describe any single program or group of programs, languages, operating procedures, and documentation of a computer system. Software is the real interface between the user and the computer.
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SSBLT	**S**ource **S**ynchronous **BL**ock **T**ransfer
standard(s)	A set of detailed technical guidelines used as a means of establishing uniformity in an area of hardware or software development.
SVGA	**S**uper **V**ideo **G**raphics **A**rray (IBM). An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 800 x 600 pixels.

Teletext One way broadcast of digital information. The digital information is injected in the broadcast TV signal, VBI, or full field, The transmission medium could be satellite, microwave, cable, etc. The display medium is a regular TV receiver.

thick Ethernet (10base-5)
An Ethernet in which the physical medium is a double shielded, 50-ohm coaxial cable capable of carrying data at 10 Mbps for a length of 500 meters (also referred to as thicknet).

thin Ethernet (10base-2)
An Ethernet in which the physical medium is a single-shielded, 50-ohm RG58A/U coaxial cable capable of carrying data at 10 Mbps for a length of 185 meters (also referred to as AUI or thinnet).

twisted-pair Ethernet (10base-T)
An Ethernet in which the physical medium is an unshielded pair of entwined wires capable of carrying data at 10 Mbps for a maximum distance of 185 meters.

UART **U**niversal **A**synchronous **R**eceiver/**T**ransmitter

UV **U**ltra**V**iolet

UVGA **U**ltra **V**ideo **G**raphics **A**rray. An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

Vertical Blanking Interval (VBI)
The time it takes the beam to fly back to the top of the screen in order to retrace the opposite field (odd or even). VBI is in the order of 20 TV lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

VESA (bus) **V**ideo **E**lectronics **S**tandards **A**ssociation (or VL bus). An internal interconnect standard for transferring video information to a computer display system.

VGA **V**ideo **G**raphics **A**rray (IBM). The third and most common monitor standard used today. It provides up to 256 simultaneous colors and a screen resolution of 640 x 480 pixels.

virtual address	A binary address issued by a CPU that indirectly refers to the location of information in primary memory, such as main memory. When data is copied from disk to main memory, the physical address is changed to the virtual address.
VL bus	See **V**ESA **L**ocal bus (VL bus).
VMEchip2	MCG second generation VMEbus interface ASIC (Motorola)
VME2PCI	MCG ASIC that interfaces between the PCI bus and the VMEchip2 device.
volatile memory	A memory in which the data content is lost when the power supply is disconnected.
VRAM	**V**ideo (Dynamic) **R**andom **A**ccess **M**emory. Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.
Windows NT™	The trademark representing **Windows N**ew **T**echnology, a computer operating system developed by the Microsoft Corporation.
XGA	E**X**tended **G**raphics **A**rray. An improved IBM VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.
Y Signal	Luminance. This determines the brightness of each spot (pixel) on a CRT screen either color or B/W systems, but not the color.

Index

A

abbreviations, acronyms, and terms GL-1
ambient air temperature B-3

B

block diagram
    PM603/PM604 1-6
    RAM104 and PM603/PM604
    on base board 1-4

C

cables B-4
CFM (cubic feet per minute) B-3
clock frequencies supported by
        PM603/PM604 1-7
conductive chassis rails B-4
connector pin assignments 2-1
connector J5 to MVME160x 2-8
control and status registers 1-9
cooling requirements B-3
CPU
    configuration register 1-9
    connector (J2) 2-2
    connector (J2)pin assignments 2-2
cubic feet per minute (CFM) B-3

D

description 1-1
DRAM 1-8
    expansion connectors (J3 & J4) 2-6
    size register 1-10

E

EEPROM/Flash 1-7
ESD
    precautions 1-12

F

EMC compliance B-4
features 1-1
forced air cooling B-3
functional description 1-3, 1-5

G

general description 1-3
Glossary GL-1

I

installation 1-12
installing/installation
    PM603/PM604 on MVME160x 1-13
    RAM104 on PM603/PM604 1-15
    PM603 or PM604 on MVME160x 1-14
    RAM104 on PM603 or PM604 1-16
introduction 1-1, 2-1

J

J1 2-1
J2 2-2
J4 2-6
J5 2-8

L

linear feet per minute (LFM) B-3

M

machine check interrupt (MCP_) 1-7
manufacturers' documents A-3
memory maps 1-12
minimum ROMFAL & ROMNAL values 1-8
model designations 1-2
models, PM603/PM604/RAM104 3
MPC105 1-7
    PCI bridge/memory controller 1-7
MPC603 processor 1-5
MPC604 processor 1-5

O

optional RISCWatch header (J1) 2-1

P

pin assignments
    connector J4 2-6
    connector J3 2-7
PM603/PM604
    models 3
    model designations 1-2
    specifications B-1

R

RAM104
    models 3
    model designations 1-2
    specifications B-2
related specifications A-8
RF emissions B-4
RISCWatch 603 processor interface
    header J1 2-1

S

shielded cables (see also cables) B-4
specifications B-1

INDEX

PM603/PM604 Processor/Memory Mezzanine Module and RAM104 DRAM Memory Module User's Manual

34 pages
1/8" spine

® ™

36 - 84 pages
3/16" & 1/4" spine

PM603/PM604 Processor/Memory Mezzanine and RAM104 DRAM Memory User's Manual

86 - 100 pages
5/16" spine

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102 - 180 pages
3/8" - 1/2" spine

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182 - 308 pages
5/8" - 1 1/8" spine
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