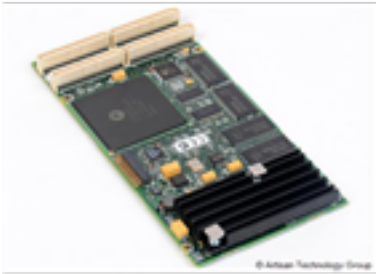
Motorola PPMC750-1141

Processor PCI Mezzanine Card



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PPMC750 Extended Processor PMC Module Installation and Use Manual

PPMC750XTA/IH1

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Computer Group
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Preface

This manual provides both general and functional descriptions of the product along with connector pin assignments and specifications for the PPMC750 Extended Processor PMC Module.

The information contained in this manual applies to the PPMC750 Extended Processor PMC Module, referred to in this manual as PPMC750-2xxx, and applying to the following model configurations:

Model Number	CPU/Speed	Major Differences
PPMC750-2141	750, 233MHz	64MB DRAM, 1M L2 Cache, 9M Flash, Extended Size (1.5 times standard width), ECC
PPMC750-2251	750, 350MHz	128MB DRAM, 1M L2 Cache, 9M Flash, Extended Size (1.5 times standard width), ECC

In addition, two optional assemblies are available with either model:

Model Number	Description
PPMC-CABLE-001	PPMC750-2xxx Debug Cable
PPMC750-DEV-1	PPMC750-2xxx Development Kit for the Front Panel

This manual is intended for anyone who designs OEM systems, supplies additional capability to existing compatible systems, or works in a lab environment for experimental purposes. It is important to note that a basic knowledge of computers and digital logic is assumed.

Printed in the United States of America
November 1999

Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must be plugged into an approved three-contact electrical outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

To prevent serious injury, use extreme caution when handling, testing, and adjusting this equipment. Dangerous voltages, capable of causing death are present.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

WARNING

This equipment generates, uses, and can radiate electro-magnetic energy. It may cause or be susceptible to electro-magnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

If any modifications are made to the product, the modifier assumes responsibility for radio frequency interference issues. Changes or modifications not expressly approved by Motorola Computer Group could void the user's authority to operate the equipment.

CE

European Notice: Board products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 (CISPR 22)	Radio Frequency Interference, Class A
EN50082-1	Electromagnetic Immunity

WARNING

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may be required to take adequate measures.

This board product was tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

For minimum RF emissions, it is essential that you implement the following conditions:
1. Install shielded cables on all external I/O ports.
2. Connect conductive chassis rails to earth ground to provide a path for connecting shields to earth ground.
3. Tighten all front panel screws.

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Contents

List of Figures

List of Tables

Preparation and Installation

1

Introduction

This chapter provides a brief description of the PPMC750-2xxx Extended Processor PMC Module, and instructions for preparing and installing the hardware including the optional SDRAM memory mezzanine module.

In this manual, the name PPMC750-2xxx refers to all models of the PPMC750-2xxx series boards, unless otherwise specified. These are add-on modules intended for use with any host carrier board that will accept the extended version of the PMC or PPMC module.

PPMC750-2xxx Description

The PPMC750-2xxx is an extended form factor version of the PPMC750 Processor PCI Mezzanine Card (PPMC) board (refer to the VITA-32-199x Processor PMC Standard for Processor PCI Mezzanine cards for more information). The width of the PPMC750-2xxx is extended to 1.5 times the normal width to 111 mm. It is based on the PowerPC MPC750 processor and the Hawk PCI-Host bridge/system memory controller.

The standard PPMC750 features include 1MB of L2 cache, one bank of SDRAM (32MB to 128MB) onboard, 8MB of FLASH, and an optional SDRAM memory expansion capability.

In addition to the standard PPMC750 features, the PPMC750-2xxx features 1MB of socketed FLASH, a 10/100TX Ethernet channel, a 190-pin Mictor debug connector, and a serial port debug connector.

Four 64-pin PMC connectors on the PPMC750-2xxx are used to connect the PPMC750-2xxx to the host board. A 10-pin right angle header located on the primary side of the board provides an interface to the async serial port. A 16-pin header provides access to the processor JTAG/COP port. A 190-pin Mictor connector located on the secondary side of the board

provides debug access to the processor bus. The Serial port and JTAG/COP interfaces, along with the ABORT_L signal, are also routed to the PMC P14 connector for carrier board access.

The PPMC750-2xxx contains a 140-pin AMP connector installed on the secondary side of the board to provide a receptacle for the memory expansion capability. The presence of this connector increases the side two component height measurement and places it outside the standard PMC height.

Monarch and Non-Monarch PPMCs

The traditional concept of host/master and slave/target processors changes with the inception of the PPMC because the arbiter or clock source, traditionally located on the host board, does not reside on the PPMC750-2xxx. The VITA 32 specification defines the terms Monarch and Non-monarch to refer to these two modes of operation for PPMCs. A Monarch PPMC is defined as the main PCI bus PPMC (or CPU) that performs PCI bus enumeration at power-up or reset and acts as the PCI interrupt handler. The Non-monarch is a slave/target processor that does not perform bus enumeration and does not service PCI interrupts but may generate a PCI interrupt to the host processor.

A system may have one Monarch PPMC750-2xxx and/or one or more Non-monarch PPMC750-2xxxs, creating a loosely coupled multiprocessing system. A PPMC750-2xxx operating as a Monarch may be mated to a carrier board with slave processors, PCI and other I/O devices. A PPMC750-2xxx operating as a Non-monarch may be installed on a carrier with a host processor and other PCI devices, such as an MVME2400 or an MCPN750 board. Different versions of PPCBUG or other operating systems may be required for a PPMC750-2xxx board operating as a Non-monarch versus the monarch mode.

The PPMC750-2xxx software is configured to operate as either a Monarch or Non-monarch by reading the state of the MONARCH# pin on the PPMC750-2xxx. This pin is either grounded or left open on the carrier board to enable the desired mode of operation. Refer to the MONARCH# signal explanation on page 3-14 of this manual for more information.

Carrier Board Requirements

A carrier board must provide the standard PCI interface, including 3.3V and 5V power, PCI address/control, a PCI clock, and a PCI arbiter REQ/GNT pair. Refer to the VITA-32-199x spec. The carrier board must also ground the MONARCH# pin to enable the Monarch operating mode. Leaving the MONARCH# pin open will enable the Non-monarch mode.

System Enclosure

The system enclosure requirements are determined by the configuration and architecture of the baseboard (either VME, CompactPCI, or custom), and requires two slots for both the baseboard and the attached PPMC750-2xxx (in a VME or CompactPCI chassis).

Overview of Start-Up Procedures

The following table lists the things you will need to do before you can use this board, and tells where to find the information you need to perform each step. Be sure to read this entire chapter and read all Caution and Warning notes before beginning.

Table 1-1. Start-Up Overview

What you need to do ...	Refer to ...	On page ...
Unpack the hardware.	***Unpacking the PPMC750-2xxx Hardware***	1-5
Make any settings or adjustments on the PPMC750-2xxx module.	***Preparing the PPMC750-2xxx Hardware***	1-5
	PPMC750-2xxx Configuration Considerations	1-5
Prepare any other optional devices or equipment you will be using.	For more information on optional devices and equipment, refer to the documentation provided with that equipment.	
Install the PPMC750-2xxx on the baseboard.	***Installation of a PPMC750-2xxx on a VME or CompactPCI board***	1-9

Table 1-1. Start-Up Overview (Continued)

What you need to do ...	Refer to ...	On page ...
Install the Optional Memory Mezzanine on the PPMC750-2xxx.	***Install of Optional SDRAM Mezzanine on the PPMC750-2xxx***	1-13
Connect any other optional devices or equipment you will be using.	***Connector Pin Assignments***	4-1
	For more information on optional devices and equipment, refer to the documentation provided with that equipment.	
Power up the system.	***Status Indicators***	2-3
	You may also wish to obtain the ***PPCBug Diagnostics Manual***, listed in Appendix A, ***Ordering Related Documentation***.	A-1
Examine the environmental parameters and make any changes needed.	***ENV - Set Environment***	6-3
	You may also wish to obtain the ***PPCBug Firmware Package User's Manual***, listed in Appendix A, ***Ordering Related Documentation***.	A-1
Program the PPMC750-2xxx module and PMCs as needed for your applications.	***Preparing the PPMC750-2xxx Hardware***	1-2, 1-6
	You may also wish to obtain the ***PPMC750-2xxx Programmer's Reference Guide***, listed in Appendix A, ***Ordering Related Documentation***.	A-1

Unpacking the PPMC750-2xxx Hardware

Note If the shipping carton(s) is/are damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton(s). Refer to the packing list(s) and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Caution Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

Preparing the PPMC750-2xxx Hardware

To produce the desired configuration and ensure proper operation of the PPMC750-2xxx, you may need to carry out certain modifications before and after installing the modules.

The following paragraphs discuss the preparation of the PPMC750-2xxx hardware components prior to installing them into a chassis and connecting them.

PPMC750-2xxx Configuration

The PPMC750-2xxx provides software control over most options; by setting bits in control registers after installing the PPMC750-2xxx in a system, you can modify its configuration. The PPMC750-2xxx control registers are described in the *PPMC750-2xxx Processor PMC Module Programmer's Reference Guide* as listed in the table *Motorola Computer Group Documents* in Appendix A, *Ordering Related Documents.*

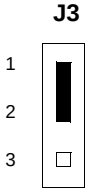
Figure 1-1 illustrates the placement of connectors, headers and jumpers on the PPMC750-2xxx. The PPMC750-2xxx has been factory tested and is shipped with the configurations described in the following sections. It contains a factory-installed debug monitor, PPCBug, which operates with those factory settings.

Flash Bank Selection (J3)

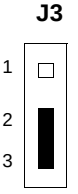
The PPMC750-2xxx board has provision for 1MB of socketed Flash memory and 8MB of soldered Flash memory.

The FLASH is organized into two banks: Bank A and Bank B. Bank A is 8Mbytes and 16-bits wide. Bank B is the 1MByte of socketed FLASH and is also 16-bits wide (XU1 and XU2). Both banks are shipped from the factory with PPCBug programmed in the first 1MByte.

To direct the reset vector to Flash Bank A, place a jumper across header J3 pins 1 and 2. To direct the reset vector to Flash Bank B, place a jumper across header J3 pins 2 and 3.



Flash Bank A Enabled (8MB, Soldered)



Flash Bank B Enabled (1MB, Sockets)
(Factory Configuration)

Note If no jumper is installed, the reset vector defaults to Bank A.

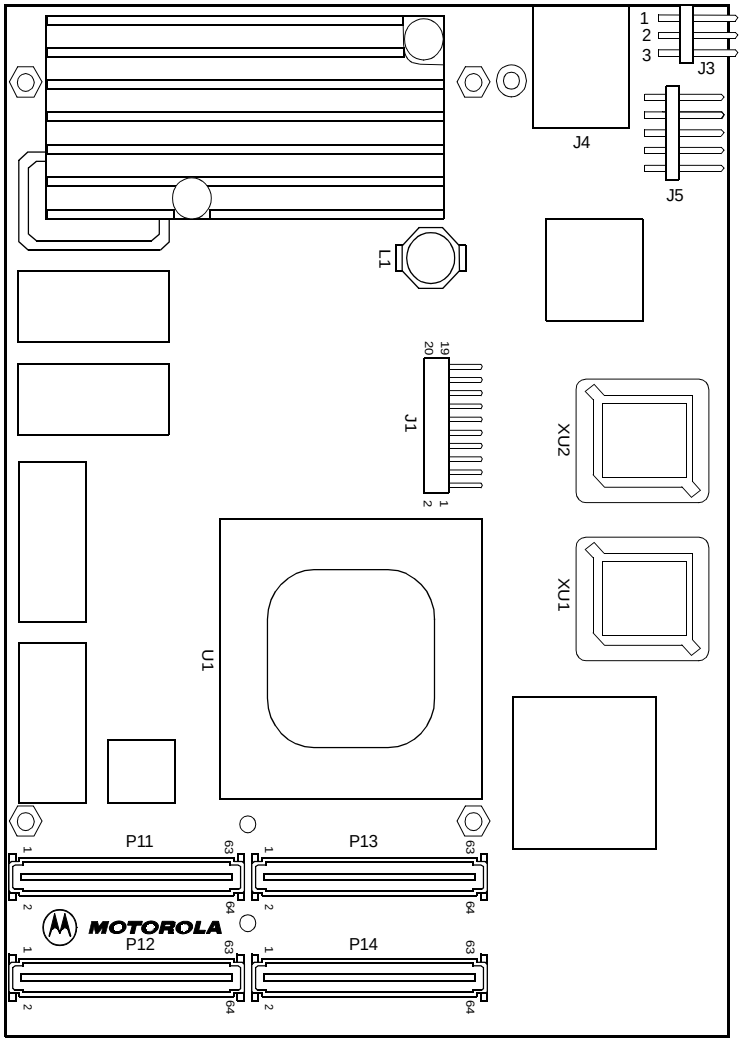


Figure 1-1. PPMC750-2xxx Headers, Connectors and Components (Top View)

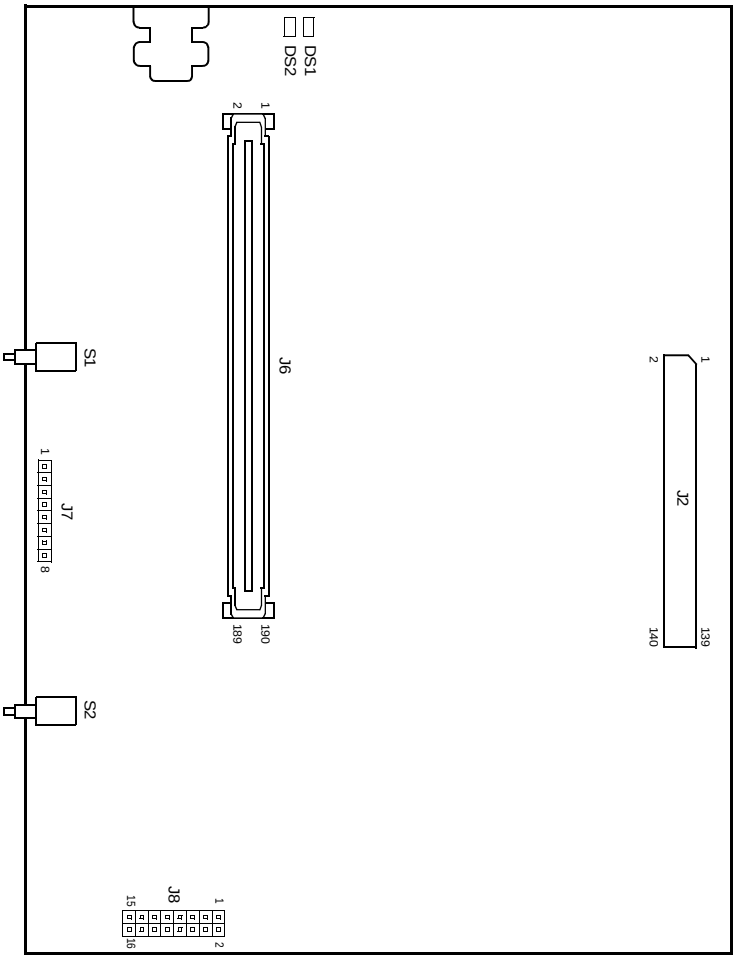


Figure 1-2. PPMC-2xxx Headers, Connectors and Components (Bottom View)

Installation

The following instructions tell how to install the PPMC750-2xxx on a typical VME or CompactPCI single board computer, and how to install the optional memory mezzanine module on the PPMC750-2xxx.

ESD Precautions

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component on a grounded, static-free surface (if a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available locally) that is attached to an unpainted metal part of the system chassis.

Installation of PPMC750-2xxx on a VME or CompactPCI Board

To install a PPMC750-2xxx mezzanine on an VMEmodule or CompactPCI board, refer to Figure 1-2 and perform the following steps:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove the chassis or system cover(s) as necessary to gain access to the VMEmodule or CompactPCI board.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the VMEmodule or CompactPCI board from its card slot and place it on a clean and adequately protected working surface (preferably an ESD mat) with the backplane connectors facing you.
4. If you are planning on using the optional PPMC750-2xxx Development Kit, install the kit (Kit #PPMC750-DEV-1 - note: some assembly of the kit hardware may be required) in the second PMC slot I/O connector area. Attach the DB9 serial port adapter cable to the bezel DB9 cutout area. Refer to Figure 1-3.

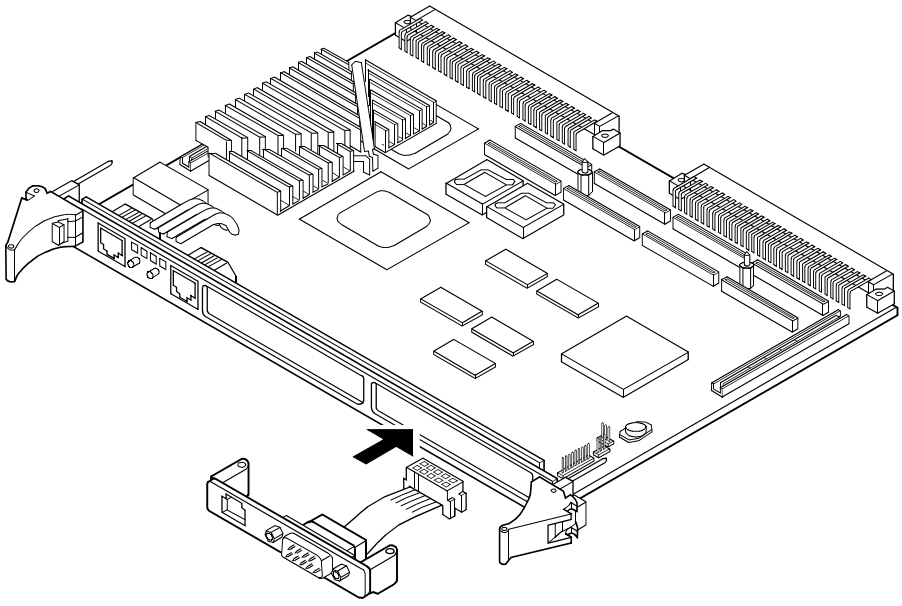


Figure 1-3. PPMC750-2xxx Development Kit Placement

Caution

Avoid touching areas of integrated circuitry; static discharge can damage the circuits.

5. Place the PPMC750-2xxx mezzanine module on top of the VMEmodule, or CompactPCI board, with the four PMC connectors on the PPMC750-2xxx aligned with the four corresponding connectors on the baseboard. Connectors P11, P12, P13, and P14 at the bottom edge of the PPMC750-2xxx should connect smoothly with the corresponding connectors on the VMEmodule or CompactPCI board. The RJ45 ethernet connector should line up with the cut out in the bezel.

6. Attach the other end of the serial port adapter cable to the 2x5 header (J5) on the PPMC750-2xxx. Make sure the pin 1 lines up on both connectors.

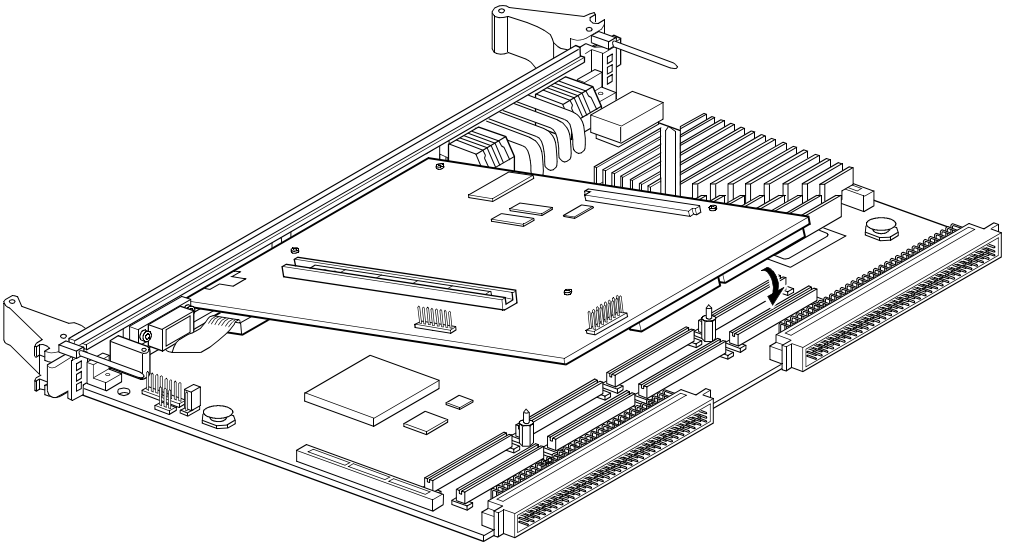


Figure 1-4. Installing a PPMC750-2xxx on a VMEmodule

7. Align the standoffs on the PPMC750-2xxx mezzanine with the VMEmodule or CompactPCI board, install the phillips-head screws through the holes in the base board and the spacers. Tighten the screws.

8. Install the VME or CompactPCI assembly in its proper card slot. Ensure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.

Notes When the PPMC750-2xxx is installed on a VME or CompactPCI board, the total assembly violates the single board height limit. The adjacent VME or CompactPCI slot must be left vacant for proper installation and system use.

9. Replace the chassis or system cover(s) and connect the system to the AC or DC power source. Turn the equipment power on.

Installation of Optional SDRAM Mezzanine on PPMC750-2xxx

The optional SDRAM mezzanine mounts on the backside (side 2) of the PPMC750-2xxx processor module. To install an SDRAM mezzanine, refer to Figure 1-3 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodule or CompactPCI board.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

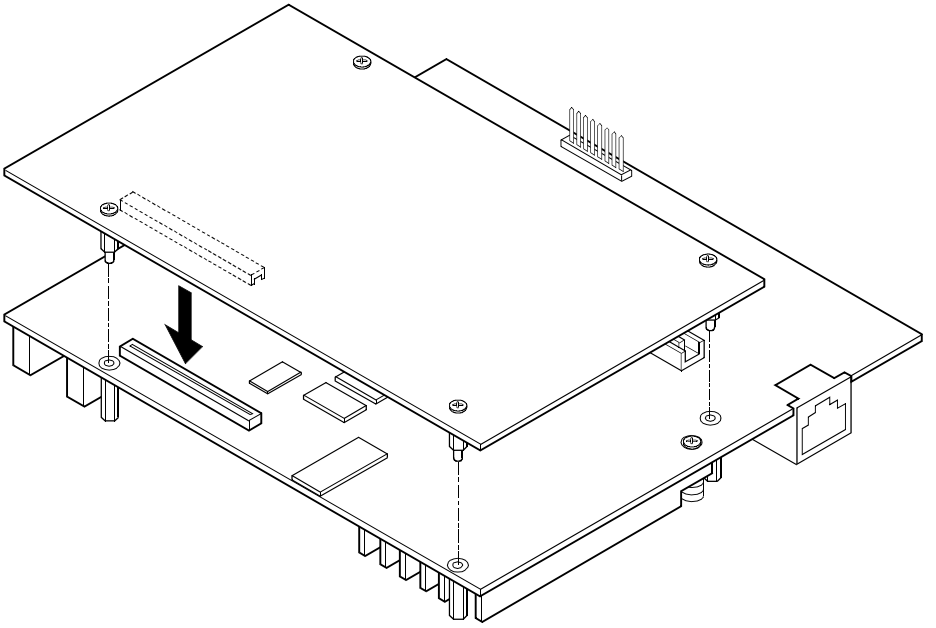


Figure 1-5. Installing SDRAM Mezzanine on PPMC750-2xxx

3. Carefully remove the VME or CompactPCI board, with the PPMC750-2xxx installed, from its card slot and place it on a clean and adequately protected working surface (preferably an ESD mat), component side up, with the front panel facing you. Note that the ESD mat should be on a firm surface which does not bow.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

4. Remove four short phillips-head screws attached to the four standoffs, from the side of the PPMC750-2xxx facing up. Do not remove the PPMC750-2xxx from the carrier board.
5. Pick up the SDRAM mezzanine module, and note the position of the SDRAM connector P1. Also note the position of the PPMC750-2xxx J2 connector. Align the SDRAM connector, P1, with the corresponding connector J2 on the PPMC750-2xxx, without actually setting the SDRAM on the PPMC750-2xxx.
6. Set the SDRAM mezzanine module on top of the corresponding connector on the PPMC750-2xxx mezzanine. Do NOT press the boards together yet.
7. Visually verify that the four screw/standoffs on the SDRAM mezzanine are aligned with the four standoff holes on the PPMC750-2xxx. Do NOT press the boards together yet.

Caution

Failure to properly align the connectors on the SDRAM and the PPMC750-2xxx may result in damage to the module's components.

8. Place your thumbs on the top side of the SDRAM mezzanine module (in the middle of and behind the connector, P1). Press the mezzanine down with both thumbs until the SDRAM and the PPMC750-2xxx click together.
9. Visually verify that the connector is fully seated and the four mezzanine screw/standoffs are protruding through the PPMC750-2xxx PWB and into the standoffs.
10. Tighten the four phillips-head screws at the four corners of the SDRAM module and into the standoffs on the VME or CompactPCI board.
11. Reinstall the VME or CompactPCI assembly in its proper card slot. Be sure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.

Notes When the combined PPMC750-2xxx and memory mezzanine is installed on a VME or CompactPCI board, the total assembly violates the single board height limit. In these situations, the adjacent VME or CompactPCI slot must be left vacant for proper installation and system use.

12. Replace the chassis or system cover(s) and reconnect the system to the AC or DC power source. Turn the equipment power on.

Operating Instructions 2

Introduction

This chapter provides information about powering up the PPMC750-2xxx system, and functionality of the status indicators, and I/O ports on the PPMC750-2xxx module.

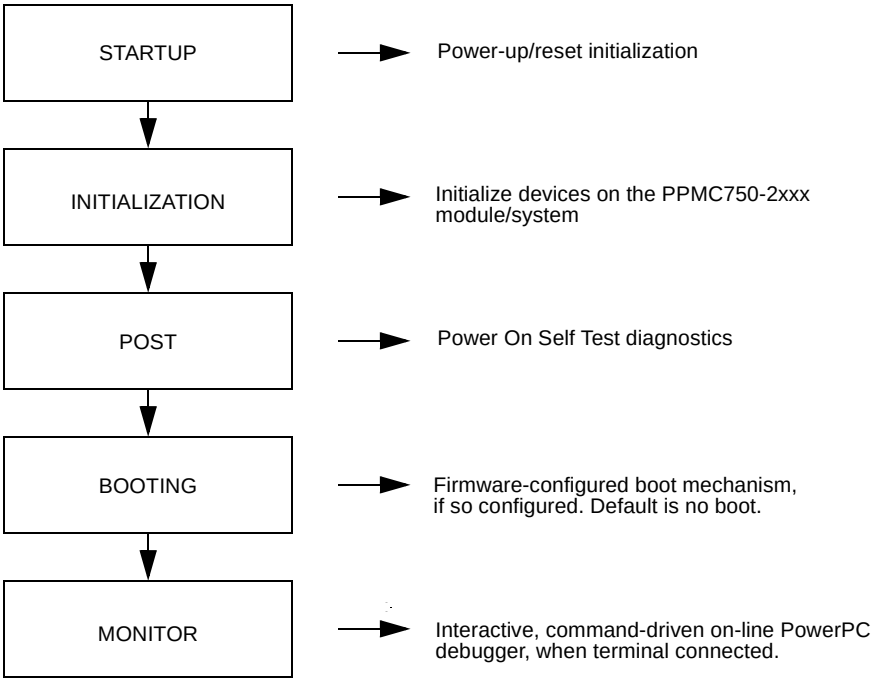
Applying Power

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. The MPU, hardware and firmware initialization process is performed by the PPCBug firmware at power-up or system reset. The firmware initializes the devices on the PPMC750-2xxx module in preparation for booting the operating system.

The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system. Refer to Chapter 6 for further information about modifying defaults.

The following flowchart shows the basic initialization process that takes place during PPMC750-2xxx system start-ups.

For further information on PPCbug, refer to Chapter 5, *PPCBug*, or to the PPCBug documentation listed in Appendix A.



PPMC750-2xxx

The status indicators (LEDs), and the Debug Serial port of the PPMC750-2xxx are described in the following sections.

Status Indicators

There are two LED (light-emitting diode) status indicators located on the secondary side of thePPMC750-2xxx : **BFL** and **CPU**.

BFL (DS1)

The *yellow* **BFL** LED indicates board failure; lights when the BRDFAIL* signal line is active.

CPU (DS2)

The *green* **CPU** LED indicates CPU activity; lights when the DBB* (Data Bus Busy) signal line on the processor bus is active.

DEBUG Serial Port

A three wire Debug serial RS232 port (TXD, RXD, GND) is available on the 0.1”, 10-pin right-angle header (J5) located on the primary side of the PPMC750-2xxx. Refer to Figure 2-1 for pin definitions. A J5 to DB9 adapter cable is provided in the front bezel kit.

The **DEBUG** port may be used for connecting a terminal to the PPMC750-2xxx to serve as the firmware console for the factory installed debugger, PPCBug. The port is configured as follows:

- 8 bits per character
- 1 stop bit per character
- Parity disabled (no parity)
- Baud rate = 9600 baud (default baud rate at power-up)

After power-up, the baud rate of the **DEBUG** port can be reconfigured by using the debugger’s Port Format (**PF**) command. Refer to Chapters 5 and 6 for information about PPCBug.

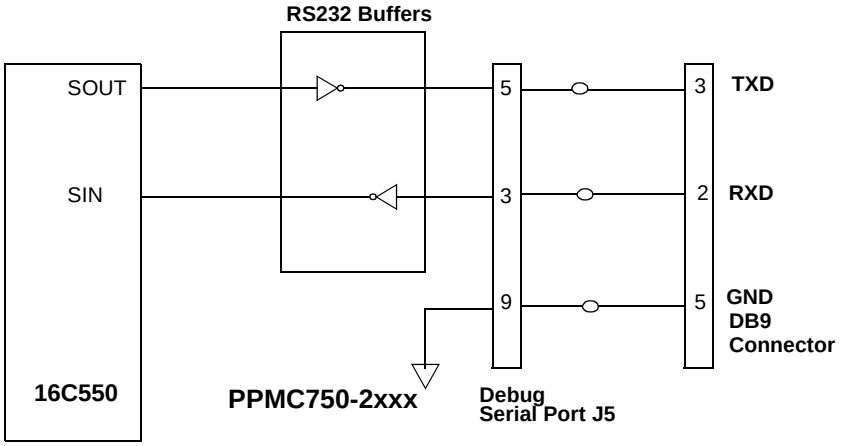


Figure 2-1. PPMC750-2xxx DEBUG Serial Port Configuration

RESET and ABORT Switches

The PPMC750-2xxx contains switches to support RESET and ABORT debug functions. The RESET switch is located at S1 and can be used to reset the entire PPMC750-2xxx module. The ABORT switch is located at S2 and can be used to generate an ABORT interrupt. These switches are not populated on the standard product.

Functional Description 3

Introduction

This chapter describes the PPMC750-2xxx Processor PMC Module on a block diagram level. The *General Description* provides an overview of the PPMC750-2xxx, followed by a detailed description of several blocks of circuitry. Figure 3-1 shows a block diagram of the overall board architecture.

Detailed descriptions of other PPMC750-2xxx blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide* (part number PPMC750XTA/PG). Refer to it for a functional description of the PPMC750-2xxx in greater depth.

Features

The following table summarizes the features of the PPMC750-2xxx processor module.

Table 3-1. PPMC750-2xxx Features

Feature	Description
Processor	Single MPC750 Processor Core Frequency up to 350 MHz Bus Clock Frequencies up to 100 MHz. Address and data bus parity
L2 Cache	1MB back side L2 Cache using pipeline burst-mode SRAMS Data bus parity
FLASH	Bank A: 8 MB Soldered on-board using two 32 Mbit devices. Bank B: 1 MByte of socketed FLASH Bank A/B select jumper.
Peripheral Support	10BaseT/100BaseTx interface with RJ45 connector

Table 3-1. PPMC750-2xxx Features (Continued)

Feature	Description
SDRAM	Double-Bit-Error detect, Single-Bit-Error correct across 72 bits Single bank of 16-bit wide devices onboard provide 32MB,64MB, or 128MB SDRAM. Optional memory mezzanine adds 32MB to 512MB of SDRAM.
Memory Controller	Hawk's SMC (System Memory Controller).
PCI Host Bridge	Hawk's PHB (PCI Host Bridge).
Interrupt Controller	Hawk's MPIC (Multi-Processor Interrupt Controller).
PCI Interface	32/64-bit Data 33MHz 3.3V/5V universal signaling interface P11, P12, P13 and P14 PMC connectors Address/data parity per PCI specification
Form Factor	1.5 width, standard length PMC (111mm x 149 mm) with 10mm board-to-board stacking height. Tall (20mm) side 2 component height due to debug connectors Height above carrier board: 21mm with debug connectors
SROM	Three 256x8 I^2C SROMs for Vital Product Data, user configuration data, and memory SPD
Debug Support	Standard 10-pin header for RS-232 serial port Standard RISCwatch header for processor JTAG/COP Interface RESET and ABORT switches 190-pin Mictor connector for processor bus monitoring Signals routed to 2mm header and PMC connector P14

General Description

The PPMC750-2xxx is a processor PMC module based on Motorola's PowerPlus II architecture. It consists of the MPC750 processor and L2 backside cache, the Hawk System Memory Controller (SMC)/PCI Host Bridge (PHB) ASIC, 9MB of FLASH memory, 32MB to 512MB of additional ECC-protected SDRAM plug-in memory expansion capability, and a debug serial port.

The PPMC750-2xxx module interfaces to the host board PCI bus via the PMC P11, P12, P13 and P14 connectors which provides a 64-bit PCI interface between the host board and the PPMC750-2xxx. The PPMC750-2xxx module draws +5V and +3.3V through the PMC connectors. The onboard Processor Core Power Supply derives the core voltage from the +5V power. The clock generator derives all of the required onboard clocks from the PCI clock input on P11.

The PPMC750-2xxx module has headers onboard to support module debug. These headers provides the interface to the debug serial RS-232 port and an interface to the MPC750 processor JTAG/COP port.

The PPMC750-2xxx module can function as a system controller (Monarch) for the host board or as a slave processor (Non-monarch) PMC, depending on the state of the MONARCH# signal from the PMC connector. When configured as the Monarch, the PPMC750-2xxx will enumerate the PCI bus as well as monitor and service the four PCI interrupts.

The block diagram for the PPMC750-2xxx module is shown in the figure on the next page.

Block Diagram

Figure 3-1 is a block diagram of the PPMC750-2xxx's overall architecture.

MPC750 Processor

The PPMC750-2xxx can be ordered with a 233MHz or a 350MHz PowerPC MPC750 processor chip.

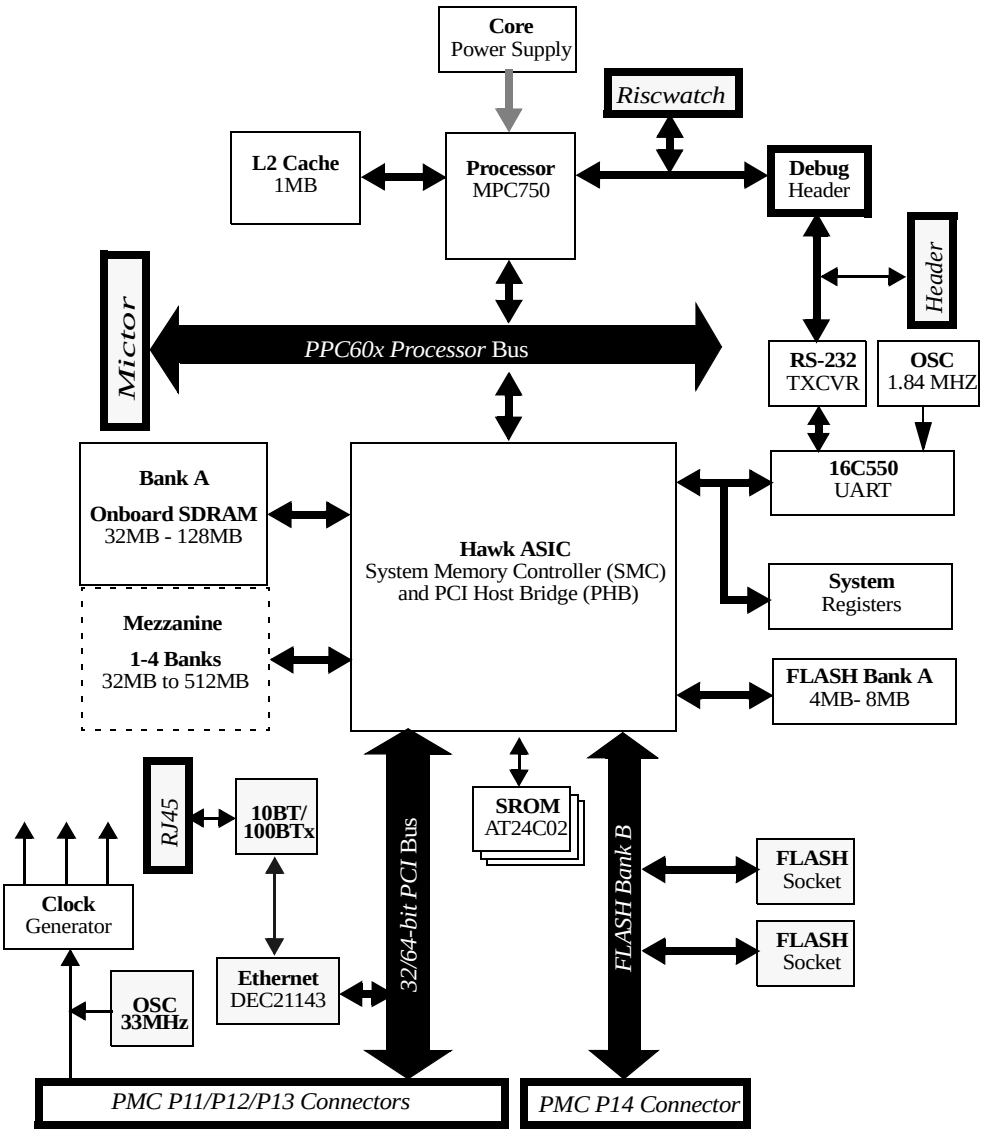


Figure 3-1. PPMC750-2xxx Block Diagram

L2 Cache

The PPMC750-2xxx uses a back-side L2 cache structure via the MPC750 processor chip. MPC750 L2 cache is implemented with an onchip 2-way set-associative tag memory and external direct-mapped synchronous SRAMs for data storage. The external SRAMs are accessed through a dedicated 72-bit wide (64 bits of data and 8 bits of parity) L2 cache port. The MPC750 processor supports 256KB, 512KB or 1MB of L2 cache SRAMs. The L2 cache can operate in copyback or writethru modes and supports system cache coherency through snooping. Data parity generation and checking can be disabled by programming the MPC750 accordingly. Refer to the MPC750 Data Sheet for additional information.

Hawk ASIC

The Hawk ASIC provides the bridge function between the PPC60X bus, the system memory, and the PCI Local Bus. The PCI interface provides 32 bit addressing and 64 bit data. PCI 64 bit addressing (dual address cycle) is not supported.

There are four programmable map decoders for each direction to provide flexible address mappings between the PowerPC and the PCI Local Bus. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for additional information and programming details.

The Hawk ASIC contains arbiters for the PPC bus and the PCI bus. The PPC arbiter will be used to arbitrate between the processor and the Hawk PPC bus master for ownership of the PPC bus. The MPC750 processor is connected to the Hawk arbiter CPU0_REQ/CPU0_GNT signal pair (XARB3/XARB0).

The Hawk PCI bus arbiter is disabled. PCI bus arbitration must be provided by the carrier board.

The Hawk ASIC also provides an MPIC Interrupt Controller to handle various interrupt sources. The interrupt sources include the four MPIC Timer Interrupts, the Watchdog timer 1 interrupt, the four PCI interrupts from the PMC connector, the two software interprocessor interrupts, and the UART interrupt. The PPMC750-2xxx can generate an interrupt to the

host processor on any of PMC interrupt lines INTA#-INTD# by activating the Processor 1 interrupt output from MPIC. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for additional information and programming details.

FLASH Memory

The PPMC750-2xxx supports two banks of FLASH memory. Bank A is soldered onboard FLASH while Bank B is on board socketed FLASH.

Important: If the PPMC750-2xxx is installed on a PPMCBASE board, either the PPMC750-2xxx socketed FLASH, or the PPMCBASE board socketed FLASH must be removed. Both banks of socketed FLASH must not be installed during simultaneous operation.

Onboard Bank A FLASH

The PPMC750-2xxx contains one bank of 16-bit FLASH memory onboard. Bank A consists of two AMD (AM29DL323C) 3.3 volt, FBGA devices configured to operate in byte-wide mode. The total size of the Bank A FLASH is 8Mbytes.

Onboard Bank B FLASH

The PPMC750-2xxx contains two 32-pin PLCC sockets that can be populated with 1MB of FLASH memory using AMD AM29LV040B or equivalent devices. This FLASH memory appears as FLASH Bank B to the Hawk chip. Only 8-bit writes are supported for this bank.

The reset vector may be sourced by either Bank A or Bank B depending on the state of Hawk ***rom_b_rv*** control bit. When the ***rom_b_rv*** bit is cleared, address range FFF00000-FFFFFFFF maps to Bank A. When ***rom_b_rv*** bit is set, it maps to Bank B. An onboard jumper (J3) is provided to set the desired state of the ***rom_b_rv*** bit.

Note If the PPMC750-2xxx is installed on a PPMCBASE board, the state of the FLASH Bank jumper on the Base board (J29) overrides the state of the FLASH Bank jumper on the PPMC750-2xxx (J3).

Ethernet Interface

The PPMC750-2xxx provides an Ethernet interface via the DEC21143 device. This device, along with a Level One LXT970A PHY device, 20 and 25MHz oscillators, and a Pulse H002 transformer, implements a 10BaseT/100BaseTX autoselect ethernet interface. The Ethernet interface is routed to an RJ45 connector located at the front panel of the board.

Every board is assigned an Ethernet Station Address. The address is $08003E2XXXXX, where XXXXX is the unique number assigned to the board. In addition, the Ethernet address is stored in the configuration area of the Microwire serial ROM attached to the 21143.

Serial Port Connector

The PPMC750-2xxx provides a standard 10-pin header interface to the 16C550 serial ERS232 port. This header will support a standard ribbon cable interface to a DB9 connector provided in the front bezel kit (PPMC750-DEV-1). Refer to the Connector Pin Assignment chapter for specific pinout information.

Mictor Debug Connector

The PPMC750-2xxx contains a 190-pin Mictor debug connector to provide logic analyzer access to the processor bus. Refer to the Connector Pin Assignment chapter for specific pinout information.

ECC Memory

The PPMC750-2xxx supports one bank of ECC SDRAM onboard and up to four additional banks of SDRAM on an optional memory mezzanine.

Onboard SDRAM

The PPMC750-2xxx onboard ECC SDRAM memory, Bank A, consists of one bank of five, 16-bit wide, 3.3V SDRAM devices in 54-pin TSOPII packages. The total onboard memory size can be 32MB, 64MB or 128MB depending on the memory type used. Refer to the following table for memory options. The SDRAM memory is controlled by the Hawk ASIC which provides single-bit error correction and double-bit error detection. ECC is calculated over 72-bits. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for additional information and programming details. The SDRAM memory bus operates at the same speed as the processor bus.

Table 3-2. Onboard SDRAM Memory Size Options

Bank A SDRAM Memory Size	Device Size	Device Organization	Number of Devices
32 Mbytes	64 Mbit	4Mx16	5
64 Mbytes	128 Mbit	8Mx16	5
128 Mbytes	256 Mbit	16Mx16	5

Optional Memory Mezzanines

The PPMC750-2xxx also contains a memory expansion connector that permits installation of a memory mezzanine card. The memory mezzanine connector provides signals to support from one to four additional banks of SDRAM on the mezzanine. The memory mezzanine will support two banks of 9 devices and two banks of 5 devices as shown in Figure 3-2.

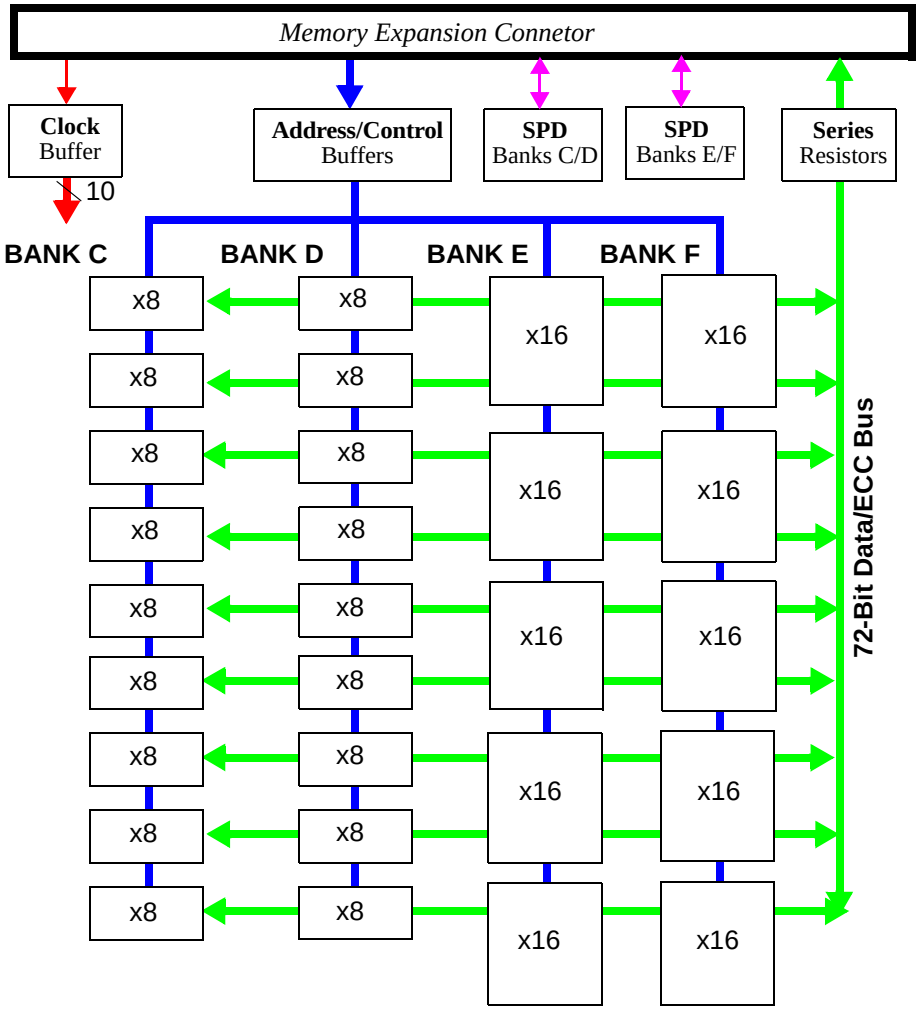


Figure 3-2. Memory Mezzanine Block Diagram

The memory mezzanine will have one or two SPD SROMs installed depending on the number of memory banks installed; one for banks C and D and one for banks E and F. Each SROM is a 3.3V, 256 x 8, Serial EEPROM device (AT24C02) used for Serial Presence Detect (SPD) memory configuration information.

The memory mezzanine has a MPC952 PLL clock driver implemented as a zero delay buffer. This buffers the SDRAM clock from the PPMC750-2xxx and creates 10 low skew clock outputs to drive the SDRAM devices on the mezzanine.

The address and control lines are buffered with flow-thru buffers and the data lines are terminated with 10 ohm series resistors. Refer to the following table for memory size options per bank. Note that since there is only one SPD SROM for Banks C/D and one for Banks E/F, the bank pairs must use the same memory device if both banks are populated.

Table 3-3. Mezzanine SDRAM Memory Size Options

Mezzanine SDRAM Memory Size	Device Size	Device Organization	Number of Devices	Banks Installed
32 Mbytes	64 Mbit	4Mx16	5	E
64 Mbytes	64 Mbit	8Mx8	9	C
128 Mbytes	64 Mbit	8Mx8	18	C & D
256 Mbytes	128 Mbit	16Mx8	18	C & D
512 Mbytes	256 Mbit	32Mx8	18	C & D
768 Mbytes	256 Mbit	32Mx8	18	C, D
		16Mx16	10	E, F

SROM

The PPMC750-2xxx module contains three 3.3V, 256 x 8, Serial EEPROM devices (AT24C02) onboard. One Serial EEPROM provides for Vital Product Data (VPD) storage of the module hardware configuration, one may be programmed with user defined configuration data, and the other provides for Serial Presence Detect (SPD) memory configuration information. The Serial EEPROM's are accessed through the I^2C port in the Hawk ASIC.

The I^2C port is also routed to the memory expansion connector and to pins on the P14 PMC User I/O connector. The interface to the memory expansion connector allows the processor to determine the configuration of the memory mezzanine. The connection to the PMC connector provides a means to interface to an optional configuration SROM on the carrier board. This will allow the PPMC750-2xxx, operating as the System Controller, to determine configuration information from the host board. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for SROM device address assignments and additional system configuration information.

System Registers

The PPMC750-2xxx System Registers include the Status, Module Fail, Module Reset and PCI Interrupt registers which provide module control and status information. Refer to the *PPMC750-2xxx Programmer's Reference Guide* (PPMC750XTA/PG) for additional details.

Timers

Timers on the PPMC750-2xxx board are provided by the Hawk ASIC. These timers are described in the following two subsections.

32-Bit Timers

Four 32-bit timers are provided by Hawk (MPIC) that may be used for system timing or to generate periodic interrupts. Each timer is driven by a divide-by-eight prescaler which is synchronized to the PPC processor

clock. For a 66.66 MHz processor bus, the timer frequency would be 8.33 MHz. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for additional information and programming details on these timers.

Watchdog Timers

The Hawk ASIC contains two Watchdog timers, WDT1 and WDT2. Each timer is functionally equivalent but independent. These timers will continuously decrement until they reach a count of 0 or are reloaded by software. The time-out period is programmable from 1 microsecond up to 32 minutes. If the timer count reaches 0, a timer output signal will be asserted. The output of Watchdog Timer 1 is routed to an MPIC interrupt. The output of Watchdog Timer 2 is logically ORed onboard to provide a hard reset. The onboard reset logic will provide a minimum 140 millisecond hard reset when the Watchdog Timer 2 output is asserted.

Following a device reset, WDT1 is enabled with a default time-out of 8 seconds and WDT 2 is enabled with a default time-out of 16 seconds. Each timer must be disabled or reloaded by software to prevent a time-out. Software may reload a new timer value or force the timer to reload a previously loaded value. To disable or load/reload a timer requires a two step process. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for additional timer details. PPCBug disables these timers during initialization.

Interrupt Routing and Generation

External interrupts routed to the Hawk MPIC include the four PCI interrupts INTA#-INTD#, four host board interrupts from PMC connector P14, the UART interrupt and the output from Watchdog Timer 1. The PPMC750-2xxx has the ability to generate any one of the PCI interrupts INTA#-INTD# by asserting the Processor 1 interrupt output from MPIC. The desired PCI interrupt is selected by programming the PCI Interrupt Select register in the System Register space. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for the register description and interrupt assignments.

Asynchronous Serial Port

The PPMC750-2xxx module contains one 16C550C UART device for use as a serial debug port. This serial port is wired as an RS-232 interface to the serial debug header. An onboard 1.8432 MHz oscillator provides the baud rate clock for the UART. The UART is accessed through the Hawk External Register Set interface. Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for more information.

Clock Generator

The PPMC750-2xxx module clock generator uses an MPC972 PLL clock driver to provide the clocks for the processor, the Hawk ASIC and the SDRAMs. All clocks are referenced to the PCI clock input on PMC connector P11.

The processor core and bus speeds listed in this document are based on a 33.33 MHz PCI bus clock input. For the 350 MHz processor version, the clock generator uses a 3x multiplier to generate the processor and memory bus clocks (100 MHz). For the 233 MHz version, a 2x multiplier is used (66 MHz processor bus).

Processor Core Power Supply

The PPMC750-2xxx uses a switching regulator to generate the processor core voltage from the +5V input. The processor core power supply provides 2.6V for the 233 MHz processor version and 2.05V for the 350 MHz processor version.

PCI Interface

The PMC750 module contains four EIA-E700 AAAB connectors which provide a 32/64-bit PCI interface to an IEEE P1386.1 PMC or VITA 32-199x PPMC compliant carrier board. Connectors P11-P13 provide the 32/64-bit PCI interface while P14 provides an I/O path from the module to the host board. Signals routed to P14 include the I2C bus, the RS-232 debug port, the processor JTAG/COP and the Bank B FLASH.

PCI bus pullup resistors required by the PCI Revision 2.1 Specification, including 64-bit expansion signals, must be supplied by the carrier board. This is required if the PPMC750-2xxx is operating as a Monarch or Non-monarch.

The following special function PMC pins, as defined by the VITA 32-199x PPMC specification, are implemented on the PPMC750-2xxx as described in the following sections.

PRESENT# Signal

The PRESENT# signal on the PPMC750-2xxx module is grounded to indicate to the carrier board that the module is installed.

MONARCH# Signal

The MONARCH# input signal allows the carrier board to enable the monarch controller features on the PPMC750-2xxx module. The PPMC750-2xxx will pullup the MONARCH# signal. If the carrier board grounds this pin, the PPMC750-2xxx module will operate as a monarch and provide system initialization and PCI interrupt handling. If the carrier leaves MONARCH# floating, the PPMC750-2xxx will operate as a non-monarch.

INTA#-INTD# Signals

The four PCI interrupt signals are routed to MPIC external interrupt inputs so that they can be monitored by the processor when the PPMC750-2xxx is operating in the Monarch mode. In the non-monarch mode, the PPMC750-2xxx can generate an interrupt to the host board processor on any one PCI interrupt INTA#-INTD# by activating the Processor 1 interrupt output from MPIC. Refer to the interrupt section of the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for interrupt assignments.

M66EN Signal

The M66EN pin is grounded on the PPMC750-2xxx to request that the carrier board operate at 33 MHz.

RESETOUT_L Signal

The PPMC RESETOUT_L output signal (P12-60) provides a means for the PPMC750-2xxx to reset the carrier board. The active low open drain RESETOUT_L signal is active whenever the PPMC750-2xxx power-up reset, Watchdog Timer 2 reset, software generated Module reset or Debug switch reset is active. The PMC PCI reset input signal will not generate RESETOUT_L.

PCI Signaling Voltage Level

The PPMC750-2xxx module is a universal PMC module which will operate with 3.3V or 5V signaling levels. The PMC VIO pins supply the voltage to the Hawk PCI interface clamp diode voltage pins allowing the PCI interface to operate at either voltage level.

Note The PCI clock input signal is a 3.3V only input.

ABORT# and RESET# Switches

The PPMC750-2xxx provides ABORT# and RESET# switches for debug purposes. The ABORT# switch (S2) is connected to the MPIC to generate an interrupt and the RESET# switch (S1) is ORed with the board reset logic.

On-Board LED's

The PPMC750-2xxx module provides two LEDs mounted on side 2 of the module for status: CPU and FAIL.

- The green CPU LED is lit when the DBB# signal of processor bus is active.
- The yellow FAIL LED is lit when the MODFAIL signal line is active (software controlled).

Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for details of the MODFAIL register.

Memory Maps

Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for memory maps of the PPMC750-2xxx processor module and the optional SRAM memory mezzanine module. The PPMC750-2xxx is a derivative of the PowerPlus II Single Board Computer (SBC) family.

Connector Pin Assignments

4

Introduction

This chapter provides connector pin assignments for all connectors on the PPMC750-2xxx board.

Memory Expansion Connector

The 140-pin AMP 0.6mm Free Height receptacle is used to provide memory expansion capability. This receptacle includes common ground contacts that mate with standard AMP plug assemblies or AMP GIGA plug assemblies with ground plates. This connector is installed on the secondary side (side 2) of the module for memory expansion capability. The pin assignments for this connector are as follows:

Table 4-1. J2 Memory Expansion Connector Pin Assignments

	J2		
1	GND*	GND*	**2**
3	DQ00	DQ01	**4**
5	DQ02	DQ03	**6**
7	DQ04	DQ05	**8**
9	DQ06	DQ07	**10**
11	+3.3V	+3.3V	**12**
13	DQ08	DQ09	**14**
15	DQ10	DQ11	**16**
17	DQ12	DQ13	**18**
19	DQ14	DQ15	**20**
21	GND*	GND*	**22**
23	DQ16	DQ17	**24**

Table 4-1. J2 Memory Expansion Connector Pin Assignments

25	DQ18	DQ19	**26**
27	DQ20	DQ21	**28**
29	DQ22	DQ23	**30**
31	+3.3V	+3.3V	**32**
33	DQ24	DQ25	**34**
35	DQ26	DQ27	**36**
37	DQ28	DQ29	**38**
39	DQ30	DQ31	**40**
41	GND*	GND*	**42**
43	DQ32	DQ33	**44**
45	DQ34	DQ35	**46**
47	DQ36	DQ37	**48**
49	DQ38	DQ39	**50**
51	+3.3V	+3.3V	**52**
53	DQ40	DQ41	**54**
55	DQ42	DQ43	**56**
57	DQ44	DQ45	**58**
59	DQ46	DQ47	**60**
61	GND*	GND*	**62**
63	DQ48	DQ49	**64**
65	DQ50	DQ51	**66**
67	DQ52	DQ53	**68**
69	+3.3V	+3.3V	**70**
71	DQ54	DQ55	**72**
73	DQ56	DQ57	**74**
75	DQ58	DQ59	**76**
77	DQ60	DQ61	**78**
79	GND*	GND*	**80**

Table 4-1. J2 Memory Expansion Connector Pin Assignments

81	DQ62	DQ63	**82**
83	CKD00	CKD01	**84**
85	CKD02	CKD03	**86**
87	CKD04	CKD05	**88**
89	+3.3V	+3.3V	**90**
91	CKD06	CKD07	**92**
93	BA0	BA1	**94**
95	A00	A01	**96**
97	A02	A03	**98**
99	GND*	GND*	**100**
101	A04	A05	**102**
103	A06	A07	**104**
105	A08	A09	**106**
107	A10	A11	**108**
109	+3.3V	+3.3V	**110**
111	A12	C0_CS_L	**112**
113	No Connect	D0_CS_L	**114**
115	WE_L	E0_CS_L	**116**
117	RAS_L	F0_CS_L	**118**
119	GND*	GND*	**120**
121	CAS_L	SDA	**122**
123	DQMB0	SCL	**124**
125	DQMB1	DQMB2	**126**
127	DQMB3	DQMB4	**128**
129	+3.3V	+3.3V	**130**
131	DQMB5	DQMB6	**132**
133	DQMB7	CLKEN (+3.3V)	**134**

Table 4-1. J2 Memory Expansion Connector Pin Assignments

135	GND	Reserved	136
137	CLK	Reserved	138
139	GND*	GND*	140

*Common GND pins mate to GIGA assembly with ground plate.

PCI Mezzanine Card (PMC) Connectors

There are four 64-pin EIA E700 AAAB SMT connectors (P11, P12, P13, and P14) on the PPMC750-2xxx to provide the 32/64-bit PCI interface and optional I/O interface to the host board. The P14 connect provide an interface to the Bank B FLASH and I2C bus along with a secondary interface to the serial port and the JTAG/COP port. The pin assignments are as follows.

Table 4-2. PMC Connector P11 Pin Assignments

	P11		
1	TCK	-12V (not used)	**2**
3	GND	INTA#	**4**
5	INTB#	INTC#	**6**
7	PRESENT#	+5V	**8**
9	INTD#	Not Used	**10**
11	GND	Not Used	**12**
13	CLK	GND	**14**
15	GND	GNT#	**16**
17	REQ#	+5V	**18**
19	VIO	AD31	**20**
21	AD28	AD27	**22**
23	AD25	GND	**24**
25	GND	C/BE3#	**26**

Table 4-2. PMC Connector P11 Pin Assignments

27	AD22	AD21	**28**
29	AD19	+5V	**30**
31	VIO	AD17	**32**
33	FRAME#	GND	**34**
35	GND	IRDY#	**36**
37	DEVSEL#	+5V	**38**
39	GND	LOCK#	**40**
41	SDONE# (not used)	SBO# (not used)	**42**
43	PAR	GND	**44**
45	VIO	AD15	**46**
47	AD12	AD11	**48**
49	AD09	+5V	**50**
51	GND	C/BE0#	**52**
53	AD06	AD05	**54**
55	AD04	GND	**56**
57	VIO	AD03	**58**
59	AD02	AD01	**60**
61	AD00	+5V	**62**
63	GND	REQ64#	**64**

Table 4-3. PMC Connector P12 Pin Assignments

	P12		
1	+12V (not used)	TRST#	**2**
3	TMS	TDO	**4**
5	TDI	GND	**6**
7	GND	Not Used	**8**
9	Not Used	Not Used	**10**
11	MOT_RSVD	+3.3V	**12**

Table 4-3. PMC Connector P12 Pin Assignments

13	RST#	MOT_RSVD	**14**
15	+3.3V	MOT_RSVD	**16**
17	Not Used	GND	**18**
19	AD30	AD29	**20**
21	GND	AD26	**22**
23	AD24	+3.3V	**24**
25	IDSEL	AD23	**26**
27	+3.3V	AD20	**28**
29	AD18	GND	**30**
31	AD16	C/BE2#	**32**
33	GND	IDSELB	**34**
35	TDRY#	+3.3V	**36**
37	GND	STOP#	**38**
39	PERR#	GND	**40**
41	+3.3V	SERR#	**42**
43	C/BE1#	GND	**44**
45	AD14	AD13	**46**
47	M66EN	AD10	**48**
49	AD08	+3.3V	**50**
51	AD07	REQB_L	**52**
53	+3.3V	GNTB_L	**54**
55	MOT_RSVD	GND	**56**
57	MOT_RSVD	MOT_RSVD	**58**
59	GND	RESETOUT_L	**60**
61	ACK64#	+3.3V	**62**
63	GND	MONARCH#	**64**

MOT_RSVD = Motorola Reserved pin

Table 4-4. PMC Connector P13 Pin Assignments

	P13		
1	Not Used	GND	**2**
3	GND	C/BE7#	**4**
5	C/BE6#	C/BE5#	**6**
7	C/BE4#	GND	**8**
9	VIO	PAR64	**10**
11	AD63	AD62	**12**
13	AD61	GND	**14**
15	GND	AD60	**16**
17	AD59	AD58	**18**
19	AD57	GND	**20**
21	VIO	AD56	**22**
23	AD55	AD54	**24**
25	AD53	GND	**26**
27	GND	AD52	**28**
29	AD51	AD50	**30**
31	AD49	GND	**32**
33	GND	AD48	**34**
35	AD47	AD46	**36**
37	AD45	GND	**38**
39	VIO	AD44	**40**
41	AD43	AD42	**42**
43	AD41	GND	**44**
45	GND	AD40	**46**
47	AD39	AD38	**48**
49	AD37	GND	**50**
51	GND	AD36	**52**

Table 4-4. PMC Connector P13 Pin Assignments

53	AD35	AD34	**54**
55	AD33	GND	**56**
57	VIO	AD32	**58**
59	Not Used	Not Used	**60**
61	Not Used	GND	**62**
63	GND	Not Used	**64**

Table 4-5. PMC Connector P14 Pin Assignments

	P14		
1	I2CSDA	I2CSCL	**2**
3	TXD	RXD	**4**
5	CPUTDI	CPUTDO	**6**
7	CPUTRST_L	GND	**8**
9	GND	BANKB_SEL	**10**
11	CPUTCK	CPUTMS	**12**
13	SRESET_L	CPURST_L	**14**
15	CHKSTPO_L	FLASHOE_L	**16**
17	FLASHUWE_L	FLASHCS_L	**18**
19	FLASHLWE_L	FLASHALE_L	**20**
21	FLASHBA0	FLASHDBOE_L	**22**
23	FLASHBA1	GND	**24**
25	GND	FLASHRA0	**26**
27	FLASHRA1	FLASHRA2	**28**
29	FLASHRA3	FLASHRA4	**30**
31	FLASHRA5	FLASHRA6	**32**
33	FLASHRA7	FLASHRA8	**34**
35	FLASHRA9	FLASHRA10	**36**
37	FLASHRA11	FLASHRA12	**38**

Table 4-5. PMC Connector P14 Pin Assignments

39	No Connect	GND	**40**
41	GND	ABORT_L	**42**
43	HOSTINT0	HOSTINT1	**44**
45	HOSTINT2	HOSTINT3	**46**
47	FLASHRD0	FLASHRD1	**48**
49	FLASHRD2	FLASHRD3	**50**
51	FLASHRD4	FLASHRD5	**52**
53	FLASHRD6	FLASHRD7	**54**
55	FLASHRD8	GND	**56**
57	GND	FLASHRD9	**58**
59	FLASHRD10	FLASHRD11	**60**
61	FLASHRD12	FLASHRD13	**62**
63	FLASHRD14	FLASHRD15	**64**

Signal Description for P14

I2CSDA:	I2C bus serial data
I2CSCL:	I2C bus clock
TXD:	RS232 serial port transmit data
RXD:	RS232 serial port receive data
CPUTDI:	Processor Riscwatch TDI
CPUTDO:	Processor Riscwatch TDO
CPUTRST_L:	Processor Riscwatch Test Reset
CPUTCK:	Processor Riscwatch Test Clock
CPUTMS:	Processor Riscwatch Test Mode Select
SRESET_L:	Processor Riscwatch Soft Reset
CPURST_L:	Processor Riscwatch CPU Reset

CHKSTPO_L:	Processor Riscwatch CPU Checkstop Out
BANKB_SEL:	FLASH Bank B reset vector select
FLASHOE_L:	FLASH Output Enable
FLASHUWE_L:	FLASH Upper Byte Write Enable
FLASHLWE_L:	FLASH Lower Byte Write Enable
FLASHCS_L	FLASH Bank B Chip Select
FLASHALE_L	FLASH Address Latch Enable
FLASHDBOE_L	FLASH (optional) Data Buffer Output Enable
FLASHBA(0:1)	FLASH address lines
FLASHRA(0:12)	FLASH address lines
FLASHRD(0:15)	FLASH data lines
ABORT_L	ABORT interrupt
HOSTINT(0:3)	Host interrupts to PPMC750-2xxx MPIC

Debug Header

A 2mm, 20-pin right-angle header located on side 1 of the PPMC750-2xxx provides an alternate interface to the async serial port, the processor JTAG/COP port, along with the RESET# and ABORT# signals. The Serial port and JTAG/COP interfaces, along with the ABORT_L signal, are also routed to the PMC P14 connector for carrier board access. The pin assignments for this header are as follows.

Table 4-6. J1 Debug Header Pin Assignments

	J1		
1	CPUTDO	RSVD	**2**
3	CPUTDI	CPUTRST_L	**4**
5	RSVD	PULLUP	**6**
7	CPUTCK	RSVD	**8**
9	CPUTMS	RSVD	**10**
11	SRESET_L	DEBUGINT_L	**12**
13	CPURST_L	GND	**14**
15	CKSTPO_L	GND	**16**
17	RESET_L	ABORT_L	**18**
19	TXD	RXD	**20**

Signal Description for J1

TXD:	RS232 serial port transmit data
RXD:	RS232 serial port receive data
CPUTDI:	Processor Riscwatch TDI
CPUTDO:	Processor Riscwatch TDO
CPUTRST_L:	Processor Riscwatch Test Reset
CPUTCK:	Processor Riscwatch Test Clock

CPUTMS:	Processor Riscwatch Test Mode Select
SRESET_L:	Processor Riscwatch Soft Reset
CPURST_L:	Processor Riscwatch CPU Reset
CHKSTPO_L:	Processor Riscwatch CPU Checkstop out
PULLUP	1K Pullup to 3.3V for Riscwatch probe
ABORT_L	ABORT interrupt
DEBUGINT_L	Debug Interrupt input
RESET_L	Debug Reset input
RSVD	Reserved pins. Do not connect any signals to these pins.

Mictor Debug Connector

One 190-pin Mictor connector with center row of power and ground pins is used to provide access to the Processor Bus and some miscellaneous signals. The pin assignments for this connector are as follows:

Table 4-7. J6 Mictor Debug Connector Pin Assignments

	J6			
1	PA0	GND	PA1	**2**
3	PA2		PA3	**4**
5	PA4		PA5	**6**
7	PA6		PA7	**8**
9	PA8		PA9	**10**
11	PA10		PA11	**12**
13	PA12		PA13	**14**
15	PA14		PA15	**16**
17	PA16		PA17	**18**
19	PA18		PA19	**20**
21	PA20		PA21	**22**
23	PA22		PA23	**24**
25	PA24		PA25	**26**
27	PA26		PA27	**28**
29	PA28		PA29	**30**
31	PA30		PA31	**32**
33	PAPAR0		PAPAR1	**34**
35	PAPAR2		PAPAR3	**36**
37	APE#		RSRV#	**38**

Table 4-7. J6 Mictor Debug Connector Pin Assignments (Continued)

39	PD0	**+5V**	PD1	**40**
41	PD2		PD3	**42**
43	PD4		PD5	**44**
45	PD6		PD7	**46**
47	PD8		PD9	**48**
49	PD10		PD11	**50**
51	PD12		PD13	**52**
53	PD14		PD15	**54**
55	PD16		PD17	**56**
57	PD18		PD19	**58**
59	PA20		PD21	**60**
61	PD22		PD23	**62**
63	PD24		PD25	**64**
65	PD26		PD27	**66**
67	PD28		PD29	**68**
69	PD30		PD31	**70**
71	PD32		PD33	**72**
73	PD34		PD35	**74**
75	PD36		PD37	**76**

Table 4-7. J6 Mictor Debug Connector Pin Assignments (Continued)

77	PD38	**GND**	PD39	**78**
79	PD40		PD41	**80**
81	PD42		PD43	**82**
83	PD44		PD45	**84**
85	PD46		PD47	**86**
87	PD48		PD49	**88**
89	PA50		PD51	**90**
91	PD52		PD53	**92**
93	PD54		PD55	**94**
95	PD56		PD57	**96**
97	PD58		PD59	**98**
99	PD60		PD61	**100**
101	PD62		PD63	**102**
103	PDPAR0		PDPAR1	**104**
105	PDPAR2		PDPAR3	**106**
107	PDPAR4		PDPAR5	**108**
109	PDPAR6		PDPAR7	**110**
111				**112**
113	DPE#		DBDIS#	**114**

Table 4-7. J6 Mictor Debug Connector Pin Assignments (Continued)

115	TT0	**+3.3V**	TSIZ0	**116**
117	TT1		TSIZ1	**118**
119	TT2		TSIZ2	**120**
121	TT3			**122**
123	TT4			**124**
125	CI#			**126**
127	WT#			**128**
129	GLOBAL#			**130**
131	SHARED#		DBWO#	**132**
133	AACK#		TS#	**134**
135	ARTY#		XATS#	**136**
137	DRTY#		TBST#	**138**
139	TA#			**140**
141	TEA#			**142**
143			DBG#	**144**
145			DBB#	**146**
147			ABB#	**148**
149	TCLK_OUT		CPUGNT0#	**150**
151			CPUREQ0#	**152**

Table 4-7. J6 Mictor Debug Connector Pin Assignments (Continued)

153		**GND**	INT0#	**154**
155	CPUGNT1#		MCHK0#	**156**
157	INT1#/WDT1TO#		SMI#	**158**
159			CKSTPI#	**160**
161	L2BR#		CKSTPO#	**162**
163	L2BG#		HALTED	**164**
165	L2CLAIM#		TLBISYNC#	**166**
167			TBEN	**168**
169				**170**
171				**172**
173				**174**
175			NAPRUN	**176**
177	SRESET1#		QREQ#	**178**
179	SRESET0#		QACK#	**180**
181	RWCPURST_L		TDO	**182**
183	GND		TDI	**184**
185	CPUCLK		TCK	**186**
187	CPUCLK		TMS	**188**
189	CPUCLK		TRST#	**190**

Ethernet Connector

The 10BaseT/100BaseTx Connector is an RJ45 connector located on the front of the PPMC750-2xxx module. The pin assignments for this connector are as follows:

Table 4-8. J4 10BaseT/100BaseTx Connector Pin Assignments

	J4
1	TD+
2	TD-
3	RD+
4	AC Terminated
5	AC Terminated
6	RD-
7	AC Terminated
8	AC Terminated

Serial Port Connector

A standard 2x5 0.1” right angle header is located on the PPMC750-2xxx to provide the interface to the serial port. The pin assignments for this connector is as follows:

Table 4-9. J5 Serial Port Connector Pin Assignments

	J5		
1	NC	NC	2
3	RXD	NC	4
5	TXD	NC	6
7	NC	NC	8
9	GND	NC	10

RISCwatch Header

The PPMC750-2xxx provides a standard 2x8 0.1” header for the RISCwatch interface. The pin assignments for this header are as follows:

Table 4-10. J8 RISCwatch Header Pin Assignments

	J8		
1	CPUTDO	No Connect	**2**
3	CPUTDI	CPUTRST_L	**4**
5	No Connect	PULLUP	**6**
7	CPUTCK	No Connect	**8**
9	CPUTMS	No Connect	**10**
11	SRESET_L	No Connect	**12**
13	CPURST_L	VOID	**14**
15	CKSTPO_L	GND	**16**

FLASH Bank Select Jumper

A 0.1 inch, 3-pin header located on the PPMC750-2xxx controls the state of the of Hawk ***rom_b_rv*** bit during power up. Placing the jumper between pins 1 and 2 will select FLASH Bank A. Placing the jumper between pins 2 and 3 will select FLASH Bank B. The pin assignments for this header are as follows:

Table 4-11. J3 FLASH Bank Select Header

	J3
1	GND
2	BANKB_SEL
3	+3.3V

Note If the PPMC750-2xxx is installed on a PPMCBASE board, the state of the FLASH Bank jumper on the Base board (J29) overrides the state of the FLASH Bank jumper on the PPMC750-2xxx (J3).

PPCBug Overview

The PPCBug firmware is the layer of software just above the hardware. The firmware provides the proper initialization for the devices on the PPMC750-2xxx module upon power-up or reset.

This chapter describes the basics of PPCBug and its architecture, describes the monitor (interactive command portion of the firmware) in detail, and gives information on actually using the PPCBug debugger and the special commands. A complete list of PPCBug commands appears at the end of the chapter.

Chapter 6 contains information about the CNFG and ENV commands, system calls, and other advanced user topics.

For full user information about PPCbug, refer to the *PPCBug Firmware Package User's Manual* and the *PPCBug Diagnostics Manual,* listed in the *Related Documentation* appendix.

PPCBug Basics

The PowerPC debug firmware, PPCBug, is a powerful evaluation and debugging tool for systems built around the Motorola PowerPC microcomputers. Facilities are available for loading and executing user programs under complete operator control for system evaluation.

PPCBug provides a high degree of functionality, user friendliness, portability, and ease of maintenance.

It achieves good portability and comprehensibility because it was written entirely in the C programming language, except where necessary to use assembler functions.

PPCBug includes commands for:

- Display and modification of memory

- Breakpoint and tracing capabilities
- A powerful assembler and disassembler useful for patching programs
- A self-test at power-up feature which verifies the integrity of the system

PPCBug consists of three parts:

- A command-driven, user-interactive *software debugger*, described in the *PPCBug Firmware Package User's Manual*. It is hereafter referred to as "the debugger" or "PPCBug".
- A command-driven *diagnostics package* for the PPMC750-2xxx hardware, hereafter referred to as "the diagnostics." The diagnostics package is described in the *PPCBug Diagnostics Manual.*
- A *user interface* or *debug*/*diagnostics monitor* that accepts commands from the system console terminal.

When using PPCBug, you operate out of either the *debugger directory* or the *diagnostic directory.*

- If you are in the debugger directory, the debugger prompt `PPC6-Bug>` is displayed and you have all of the debugger commands at your disposal.
- If you are in the diagnostic directory, the diagnostic prompt `PPC6-Diag>` is displayed and you have all of the diagnostic commands at your disposal as well as all of the debugger commands.

Because PPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. When you enter a command, PPCBug executes the command and the prompt reappears. However, if you enter a command that causes execution of user target code (e.g., **GO**), then control may or may not return to PPCBug, depending on the outcome of the user program.

Memory Requirements

PPCBug requires a maximum of 768KB of read/write memory (i.e., DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB ($04000000) of read/write memory will place the PPCBug memory page at locations $03F40000 to $03FFFFFF.

PPCBug Implementation

PPCBug is written largely in the C programming language, providing benefits of portability and maintainability. Where necessary, assembly language has been used in the form of separately compiled program modules containing only assembler code. No mixed-language modules are used.

Physically, PPCBug is contained in two on-board Flash devices that together provide 8MB of storage. The executable code is checksummed at every power-on or reset firmware entry, and the result (which includes a precalculated checksum contained in the Flash devices), is verified against the expected checksum.

MPU, Hardware, and Firmware Initialization

The debugger performs the MPU, hardware, and firmware initialization process. This process occurs each time the PPMC750-2xxx is reset or powered up. The steps below are a high-level outline; not all of the detailed steps are listed.

1. Sets MPU.MSR to known value.
2. Invalidates the MPU's data/instruction caches.
3. Clears all segment registers of the MPU.
4. Clears all block address translation registers of the MPU.
5. Initializes the MPU-bus-to-PCI-bus bridge device.
6. Calculates the external bus clock speed of the MPU.

7. Delays for 750 milliseconds.
8. Determines the CPU base board type.
9. Sizes the local read/write memory (i.e., DRAM).
10. Initializes the read/write memory controller. Sets base address of memory to $00000000.
11. Retrieves the speed of read/write memory.
12. Initializes the read/write memory controller with the speed of read/write memory.
13. Retrieves the speed of read only memory (i.e., Flash).
14. Initializes the read only memory controller with the speed of read only memory.
15. Enables the MPU's instruction cache.
16. Copies the MPU's exception vector table from $FFF00000 to $00000000.
17. Verifies MPU type.
18. Enables the superscalar feature of the MPU (superscalar processor boards only).
19. Verifies the external bus clock speed of the MPU.
20. Determines the debugger's console/host ports, and initializes the PC16550A.
21. Displays the debugger's copyright message.
22. Displays any hardware initialization errors that may have occurred.
23. Checksums the debugger object, and displays a warning message if the checksum failed to verify.
24. Displays the amount of local read/write memory found.
25. Verifies the configuration data that is resident in NVRAM, and displays a warning message if the verification failed.

26. Calculates and displays the MPU clock speed, verifies that the MPU clock speed matches the configuration data, and displays a warning message if the verification fails.
27. Displays the BUS clock speed, verifies that the BUS clock speed matches the configuration data, and displays a warning message if the verification fails.
28. Probes PCI bus for supported network devices.
29. Probes PCI bus for supported mass storage devices.
30. Initializes the memory/IO addresses for the supported PCI bus devices.
31. Executes Self-Test, if so configured. (Default is no Self-Test.)
32. Extinguishes the board fail LED, if Self-Test passed, and outputs any warning messages.
33. Executes boot program, if so configured. (Default is no boot.)
34. Executes the debugger monitor (i.e., issues the `PPC6-Bug>` prompt).

Using PPCBug

PPCBug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `PPC6-Bug` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `PPC6-Diag` prompt appears on the screen, the debugger is ready to accept diagnostics commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the Return or Enter key. This allows you to correct entry errors, if necessary, with the control characters described in the *PPCBug Firmware Package User's Manual*, Chapter 1.

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example **GO**) then control may or may not return to the debugger, depending on what the user program does. For example, if a breakpoint has

been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine RETURN (described in the *PPCBug Firmware Package User's Manual*, Chapter 5). For more about this, refer to the **GD**, **GO**, and **GT** command descriptions in the *PPCBug Firmware Package User's Manual*, Chapter 3.

A debugger command is made up of the following parts:

- The command name, either uppercase or lowercase (e.g., **MD** or **md**).
- Any required arguments, as specified by command.
- At least one space before the first argument. Precede all other arguments with either a space or comma.
- One or more options. Precede an option or a string of options with a semicolon (**;**). If no option is entered, the command's default option conditions are used.

Debugger Commands

The individual debugger commands are listed in the following table. The commands are described in detail in the *PPCBug Firmware Package User's Manual*, Chapter 3.

Note You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax for a particular command by entering **HE** and the command mnemonic, as listed below.

Table 5-1. Debugger Commands

Command	Description
AS	One Line Assembler
BC	Block of Memory Compare
BF	Block of Memory Fill
BI	Block of Memory Initialize
BM	Block of Memory Move
BR	Breakpoint Insert
NOBR	Breakpoint Delete
BS	Block of Memory Search
BV	Block of Memory Verify
CACHE	Modify Cache State
CM	Concurrent Mode
NOCM	No Concurrent Mode
CNFG	Configure Board Information Block
CS	Checksum
CSAR	PCI Configuration Space READ Access
CSAW	PCI Configuration Space WRITE Access
DC	Data Conversion
DS	One Line Disassembler
DU	Dump S-Records
ECHO	Echo String
ENV	Set Environment
FORK	Fork Idle MPU at Address
FORKWR	Fork Idle MPU with Registers
GD	Go Direct (Ignore Breakpoints)
GEVBOOT	Global Environment Variable Boot
GEVDEL	Global Environment Variable Delete

Table 5-1. Debugger Commands (Continued)

Command	Description
GEVDUMP	Global Environment Variable(s) Dump
GEVEDIT	Global Environment Variable Edit
GEVINIT	Global Environment Variable Initialization
GEVSHOW	Global Environment Variable(s) Display
GN	Go to Next Instruction
G, GO	Go Execute User Program
GT	Go to Temporary Breakpoint
HE	Help
IDLE	Idle Master MPU
IOC	I/O Control for Disk
IOI	I/O Inquiry
IOP	I/O Physical (Direct Disk Access)
IOT	I/O Teach for Configuring Disk Controller
IRD	Idle MPU Register Display
IRM	Idle MPU Register Modify
IRS	Idle MPU Register Set
LO	Load S-Records from Host
MA	Macro Define/Display
NOMA	Macro Delete
MAE	Macro Edit
MAL	Enable Macro Listing
NOMAL	Disable Macro Listing
MAR	Load Macros
MAW	Save Macros
MD, MDS	Memory Display
MENU	System Menu
M, MM	Memory Modify
MMD	Memory Map Diagnostic
MS	Memory Set
MW	Memory Write
NAB	Automatic Network Boot

Table 5-1. Debugger Commands (Continued)

Command	Description
NAP	Nap MPU
NBH	Network Boot Operating System, Halt
NBO	Network Boot Operating System
NIOC	Network I/O Control
NIOP	Network I/O Physical
NIOT	Network I/O Teach (Configuration)
NPING	Network Ping
OF	Offset Registers Display/Modify
PA	Printer Attach
NOPA	Printer Detach
PBOOT	Bootstrap Operating System
PF	Port Format
NOPF	Port Detach
PFLASH	Program FLASH Memory
PS	Put RTC into Power Save Mode
RB	ROMboot Enable
NORB	ROMboot Disable
RD	Register Display
REMOTE	Remote
RESET	Cold/Warm Reset
RL	Read Loop
RM	Register Modify
RS	Register Set
RUN	MPU Execution/Status
SD	Switch Directories
SET	Set Time and Date
SROM	SROM Examine/Modify
SYM	Symbol Table Attach
NOSYM	Symbol Table Detach
SYMS	Symbol Table Display/Search
T	Trace

Table 5-1. Debugger Commands (Continued)

Command	Description
TA	Terminal Attach
TIME	Display Time and Date
TM	Transparent Mode
TT	Trace to Temporary Breakpoint
VE	Verify S-Records Against Memory
VER	Revision/Version Display
WL	Write Loop

Caution Although a command to allow the erasing and reprogramming of Flash memory is available to you, keep in mind that reprogramming any portion of Flash memory will erase everything currently contained in Flash, including the PPCBug debugger.

Note NVRAM is located in Flash bank A on the PPMC750-2xxx board.

Diagnostic Tests

The PPCBug hardware diagnostics are intended for testing and troubleshooting the PPMC750-2xxx module.

In order to use the diagnostics, you must switch to the diagnostic directory. You may switch between directories by using the **SD** (Switch Directories) command. You may view a list of the commands in the directory that you are currently in by using the **HE** (Help) command.

If you are in the debugger directory, the debugger prompt `PPC6-Bug>` displays, and all of the debugger commands are available. Diagnostics commands cannot be entered at the `PPC6-Bug>` prompt.

If you are in the diagnostic directory, the diagnostic prompt `PPC6-Diag>` displays, and all of the debugger and diagnostic commands are available.

PPCBug's diagnostic test groups are listed in Table 5-2. Note that not all tests are performed on the PPMC750-2xxx. Using the **HE** command, you can list the diagnostic routines available in each test group. Refer to the *PPCBug Diagnostics Manual* for complete descriptions of the diagnostic routines and instructions on how to invoke them.

Table 5-2. Diagnostic Test Groups

Test Group	Description
CL1283*	Parallel Interface (CL1283) Tests*
DEC**	DEC21x43 Ethernet Controller Tests
HAWK	HAWK Tests
ISABRDGE**	PCI/ISA Bridge Tests
KBD8730x*	PC8730x Keyboard/Mouse Tests*
L2CACHE	Level 2 Cache Tests
NCR**	NCR 53C8xx SCSI-2 I/O Processor Tests
PAR8730x*	Parallel Interface (PC8730x) Test*
UART	Serial Input/Output Tests
PCIBUS	PCI/PMC Generic Tests
RAM	Local RAM Tests
RTC*	MK48Txx Timekeeping Tests
SCC*	Serial Communications Controller (Z85C230) Tests*
VGA54xx**	VGA Controller (GD54xx) Tests
VME3**	VME3 (Universe) Tests
Z8536*	Z8536 Counter/Timer Tests*

Notes You may enter command names in either uppercase or lowercase.

Some diagnostics depend on restart defaults that are set up only in a particular restart mode. Refer to the documentation on a particular diagnostic for the correct mode.

Test Sets marked with an asterisk (*) are not available on the PPMC750-2xxx.

** PCI devices that are detected will be tested.

* Represent Non-PCI devices that depend on the VPD SROM to determine if a device is expected to be present. These devices are not on the PPMC750-2xxx, but could reside on a carrier board.

Modifying the Environment

6

Overview

You can use the factory-installed debug monitor, PPCBug, to modify certain parameters contained in the PPMC750-2xxx's Non-Volatile RAM (NVRAM). NVRAM is located in the last 32K of Flash Bank A on the PPMC750-2xxx.

- The Board Information Block in NVRAM contains various elements concerning operating parameters of the hardware. Use the PPCBug command **CNFG** to change those parameters.
- Use the PPCBug command **ENV** to change configurable PPCBug parameters in NVRAM.

The **CNFG** and **ENV** commands are both described in the *PPCBug Firmware Package User's Manual*. Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **CNFG** and **ENV** that is specific to the PPCBug debugger, along with the parameters that can be configured with the **ENV** command.

CNFG - Configure Board Information Block

Use this command to display and configure the Board Information Block, which is resident within the NVRAM. The board information block contains various elements detailing specific operational parameters of the PPMC750-2xxx. The board structure for the PPMC750-2xxx is as shown in the following example:

```
Board (PWA) Serial Number     = "MOT00xxxxxxx   "
Board Identifier              = "PPMC750-2xxx   "
Artwork (PWA) Identifier      = "01-w3512FxxC   "
MPU Clock Speed               = "350            "
Bus Clock Speed               = "100            "
Ethernet Address              = 08003E20xxxx
Primary SCSI Identifier       = "07"
System Serial Number          = "nnnnnnn        "
System Identifier             = "Motorola PPMC750"
License Identifier            = "nnnnnnnn "
```

The parameters that are quoted are left-justified character (ASCII) strings padded with space characters, and the quotes (") are displayed to indicate the size of the string. Parameters that are not quoted are considered data strings, and data strings are right-justified. The data strings are padded with zeroes if the length is not met.

The Board Information Block is factory-configured before shipment. There is no need to modify block parameters unless the NVRAM is corrupted.

Refer to the *PPMC750 Extended Processor PMC Module Programmer's Reference Guide (PPMC750XTA/PG)* for the actual location and other information about the Board Information Block.

Refer to the *PPCBug Firmware Package User's Manual* for a description of **CNFG** and examples.

ENV - Set Environment

Use the **ENV** command to view and/or configure interactively all PPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PPCBug Firmware Package User's Manual* for a description of the use of **ENV**. Additional information on registers are contained in your *PPMC750 Extended Processor PMC Module Programmer's Reference Guide*.

Listed and described below are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

Configuring the PPCBug Parameters

The parameters that can be configured using **ENV** are:

```
Bug or System environment [B/S] = B?
```

B Bug is the mode where no system type of support is displayed. However, system-related items are still available. (Default)

S System is the standard mode of operation, and is the default mode if NVRAM should fail. System mode is defined in the *PPCBug Firmware Package User's Manual*.

```
Field Service Menu Enable [Y/N] = N?
```

Y Display the field service menu.

N Do not display the field service menu. (Default)

```
Probe System for Supported I/O Controllers [Y/N] = Y?
```

Y Accesses will be made to the appropriate system buses (e.g., VMEbus, local MPU bus) to determine the presence of supported controllers. (Default)

N Accesses will not be made to the VMEbus to determine the presence of supported controllers.

```
Auto-Initialize of NVRAM Header Enable [Y/N] = Y?
```

Y NVRAM (PReP partition) header space will be initialized automatically during board initialization, but only if the PReP partition fails a sanity check. (Default)

N NVRAM header space will not be initialized automatically during board initialization.

```
Network PReP-Boot Mode Enable [Y/N] = N?
```

Y Enable PReP-style network booting (same boot image from a network interface as from a mass storage device).

N Do not enable PReP-style network booting. (Default)

```
SCSI Bus Reset on Debugger Startup [Y/N] = N?
```

Y Local SCSI bus is reset on debugger setup.

N Local SCSI bus is not reset on debugger setup. (Default)

```
Primary SCSI Bus Negotiations Type [A/S/N] = A?
```

A Asynchronous SCSI bus negotiation. (Default)

S Synchronous SCSI bus negotiation.

N None.

```
Primary SCSI Data Bus Width [W/N] = N?
```

W Wide SCSI (16-bit bus).

N Narrow SCSI (8-bit bus). (Default)

```
Secondary SCSI identifier = 07?
```

Select the identifier. (Default = 07.)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Enable [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* global environment variable (GEV).

N Do not give boot priority to devices listed in the *fw-boot-path* GEV. (Default)

Note When enabled, the GEV (Global Environment Variable) boot takes priority over all other boots, including Autoboot and Network Boot.

```
NVRAM Bootlist (GEV.fw-boot-path) Boot at power-up only [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* GEV at power-up reset only.

N Give power-up boot priority to devices listed in the *fw-boot-path* GEV at any reset. (Default)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Abort Delay = 5?
```

The time in seconds that a boot from the NVRAM boot list will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Auto Boot Enable [Y/N]   = N?
```

Y The Autoboot function is enabled.

N The Autoboot function is disabled. (Default)

```
Auto Boot at power-up only [Y/N] = N?
```

Y Autoboot is attempted at power-up reset only.

N Autoboot is attempted at any reset. (Default)

```
Auto Boot Scan Enable [Y/N]   = Y?
```

Y If Autoboot is enabled, the Autoboot process attempts to boot from devices specified in the scan list (e.g., FDISK/CDROM/TAPE/HDISK). (Default)

N If Autoboot is enabled, the Autoboot process uses the Controller LUN and Device LUN to boot.


```
Auto Boot Scan Device Type List = FDISK/CDROM/TAPE/HDISK?
```

This is the listing of boot devices displayed if the Autoboot Scan option is enabled. If you modify the list, follow the format shown above (uppercase letters, using forward slash as separator).

```
Auto Boot Controller LUN   = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Auto Boot Device LUN    = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape devices currently supported by PPCBug. (Default = $00)

```
Auto Boot Partition Number = 00?
```

Which disk "partition" is to be booted, as specified in the PowerPC Reference Platform (PRP) specification. If set to zero, the firmware will search the partitions in order (1, 2, 3, 4) until it finds the first "bootable" partition. That is then the partition that will be booted. Other acceptable values are 1, 2, 3, or 4. In these four cases, the partition specified will be booted without searching.

```
Auto Boot Abort Delay = 7?
```

The time in seconds that the Autoboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 7 seconds)

```
Auto Boot Default String [NULL for an empty string] = ?
```

You may specify a string (filename) which is passed on to the code being booted. The maximum length of this string is 16 characters. (Default = null string)

```
ROM Boot Enable [Y/N] = N?
```

Y	The ROMboot function is enabled.
N	The ROMboot function is disabled. (Default)

```
ROM Boot at power-up only [Y/N] = Y?
```

Y	ROMboot is attempted at power-up only. (Default)
N	ROMboot is attempted at any reset.

```
ROM Boot Abort Delay = 5?
```

The time in seconds that the ROMboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
ROM Boot Direct Starting Address = FFF00000?
```

The first location tested when PPCBug searches for a ROMboot module. (Default = $FFF00000)

```
ROM Boot Direct Ending Address = FFFFFFFC?
```

The last location tested when PPCBug searches for a ROMboot module. (Default = $FFFFFFFC)

```
Network Auto Boot Enable [Y/N] = N?
```

Y The Network Auto Boot (NETboot) function is enabled.

N The NETboot function is disabled. (Default)

```
Network Auto Boot at power-up only [Y/N] = N?
```

Y NETboot is attempted at power-up reset only.

N NETboot is attempted at any reset. (Default)

```
Network Auto Boot Controller LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of network controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Device LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of network controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Abort Delay = 5?
```

The time in seconds that the NETboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Network Auto Boot Configuration Parameters Offset (NVRAM) =
00001000?
```

The address where the network interface configuration parameters are to be saved/retained in NVRAM; these parameters are the necessary parameters to perform an unattended network boot. A typical offset might be $1000, but this value is application-specific. (Default = $00001000)

Caution

If you use the **NIOT** debugger command, these parameters need to be saved somewhere in the offset range $00001000 through $000016F7. The **NIOT** parameters do not exceed 128 bytes in size. The setting of this ENV pointer determines their location. If you have used the same space for your own program information or commands, they will be overwritten and lost.

You can relocate the network interface configuration parameters in this space by using the **ENV** command to change the Network Auto Boot Configuration Parameters Offset from its default of $00001000 to the value you need to be clear of your data within NVRAM.

Note This number is still an offset within NVRAM. However, the NVRAM image for Bug is stored at the end of Flash Bank A (in the last 32K).

```
Memory Size Enable [Y/N] = Y?
```

Y	Memory will be sized for Self Test diagnostics. (Default)
N	Memory will not be sized for Self Test diagnostics.

```
Memory Size Starting Address = 00000000?
```

The default Starting Address is $00000000.

```
Memory Size Ending Address = 02000000?
```

The default Ending Address is the calculated size of local memory. If the memory start is changed from $00000000, this value will also need to be adjusted.

```
DRAM Speed in NANO Seconds = 60?
```

The default setting for this parameter will vary depending on the speed of the DRAM memory parts installed on the board. The default is set to the slowest speed found on the available banks of DRAM memory.

```
ROM First Access Length (0 - 31) = 10?
```

This is the value programmed into the“ROMFAL” field (Memory Control Configuration Register 8: bits 23-27) to indicate the number of clock cycles used in accessing the ROM. The lowest allowable ROMFAL setting is $00; the highest allowable is $1F. The value to enter depends on processor speed; refer to Chapter 1 or Appendix B for appropriate values. The default value varies according to the system’s bus clock speed.

Note ROM First Access Length is not applicable to the PPMC750-2xxx. The configured value is ignored by PPCBug.

```
ROM Next Access Length (0 - 15) = 0?
```

The value programmed into the“ROMNAL” field (Memory Control Configuration Register 8: bits 28-31) to represent wait states in access time for nibble (or burst) mode ROM accesses. The lowest allowable ROMNAL setting is $0; the highest allowable is $F. The value to enter depends on processor speed; refer to Chapter 1 or Appendix B for appropriate values. The default value varies according to the system’s bus clock speed.

Note ROM Next Access Length is not applicable to the PPMC750-2xxx. The configured value is ignored by PPCBug.

```
DRAM Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O DRAM parity is enabled upon detection. (Default)

A DRAM parity is always enabled.

N DRAM parity is never enabled.

Note This parameter (above) also applies to enabling ECC for DRAM.

```
L2 Cache Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O L2 Cache parity is enabled upon detection. (Default)

A L2 Cache parity is always enabled.

N L2 Cache parity is never enabled.

```
PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?
```

Initializes the PIRQx (PCI Interrupts) route control registers in the IBC (PCI/ISA bus bridge controller). The **ENV** parameter is a 32-bit value that is divided by 4 to yield the values for route control registers PIRQ0/1/2/3. The default is determined by system type.

Note LED/Serial Startup Diagnostic Codes: these codes can be displayed at key points in the initialization of the hardware devices. Should the debugger fail to come up to a prompt, the last code displayed will indicate how far the initialization sequence had progressed before stalling. **Due to limitations imposed by storing the ENV parameters in Flash, the Serial Startup codes are disabled for PPMC750-2xxx.** The codes are enabled by an **ENV** parameter:

```
Serial Startup Code Master Enable [Y/N]=N?
```

A line feed can be inserted after each code is displayed to prevent it from being overwritten by the next code. This is also enabled by an **ENV** parameter:

```
Serial Startup Code LF Enable [Y/N]=N?
```

The list of LED/serial codes is included in the section on *MPU, Hardware, and Firmware Initialization* in Chapter 1 of the *PPCBug Firmware Package User's Manual*.

Related Documentation A

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office,
- Visiting MCG's World Wide Web literature site, http://www.mcg.mot.com/literature

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Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
PPMC750 Extended Processor Programmer's Reference Guide	PPMC750XTA/PG
MVME2400-Series SBC Programmer's Reference Guide	V2400A/PG
MVME2400-Series SBC Installation and Use	V2400A/IH
MCPN750 SBC Installation and Use	MCPN750A/IH
MCPN750 SBC Programmer's Reference Guide	MCPN750A/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPCBug Diagnostics Manual	PPCDIAA/UM

Manufacturers' Documents

Table A-2 lists the manufacturers' data sheets and other useful manuals. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
MPC750™ RISC Microprocessor Technical Summary Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC750/D
MPC750™ RISC Microprocessor User's Manual Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC750UM/AD MPR604UMU-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Family: The Programming Environments Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/AD MPRPPCFPE-01
Texas Instruments TI16C550C Asynchronous Communications Element - March 1994. Revised March 1997 Texas Instruments P.O. Box 655303 Dallas, TX 75265	SLLS177C
ATMEL Nonvolitile Memory Data Book Atmel Corporation 2325 Orchord Parkway San Jose, CA 95131 Telephone: (408) 441-0311 FAX: (408) 436-4300 Website: http://www.atmel.com	AT24C04
AM29DL32xC 32 Mbit CMOS 3.0 Volt-only, Simultaneous Operation FLASH Memory AMD One AMD Place Sunnyvale, CA 94088-3453 www.amd.com	21524 Rev B, Oct 98

Related Specifications

Table A-3 lists the product's related specifications. The appropriate source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02
Proposed Standard Physical and Environmental Layers for PCI Processor Mezzanine Cards: PPMC VITA Standards Organization 7825 E. Gelding Dr. Suite 104 Scottsdale, AZ 85260 www.vita.com	VITA32 Draft 0.3

Specifications

This appendix provides general specifications, including mechanical, electrical and temperature, for the PPMC750-2xxx and the memory mezzanine.

Mechanical Characteristics

The mechanical outline of the PPMC750-2xxx module is defined as a 1.5x wide, standard length PMC module (111mm x 149mm x 10mm stacking height). The side 2 component height of the PPMC750-2xxx, without the optional memory mezzanine connector or memory mezzanine, will conform to the standard side 2 height dimension (3.5mm). The PPMC750-2xxx with the memory mezzanine will fit within the tall PMC envelope (20 mm). See Table B-1.

Electrical Characteristics

The voltage requirements and estimated power consumption for the PPMC750-2xxx are shown in the table on the following page.

Airflow Requirements

The PPMC750-2xxx module requires a minimum air flow of 490 LFM when operating at 55 degrees C ambient temperature.

B

Table B-1. PPMC750-2xxx Specifications

Characteristics	Specifications
+3.3Vdc (±5%)	(for MPC750 @ 350MHz/100MHz bus) 1.3A, typical 1.9A, max (for MPC750 @ 233MHz/66MHz bus) 1.0A, typical 1.5A, max
+5.0Vdc (±5%)	(for MPC750 @ 350MHz/100MHz bus) 1.3A, typical 1.9A, max (for MPC750 @ 233MHz/66MHz bus) 1.8A, typical 2.7A, max
Operating temperature (refer to Cooling Requirements section)	0^{o} to 55^{o} C at point of exit of forced air
Storage Temperature	-40^{o} to $+85^{o}$ C
Relative Humidity	5% to 90% (non-condensing)
Physical Dimensions (DRAM Memory module only)	Width: 74mm (2.91 inches) Length: 149mm (5.87 inches) Height (above carrier): 21mm (0.83”)

Table B-2. PPMC Memory Mezzanine Specifications

Characteristics	Specifications
Power requirements (DRAM Memory module only)	(for MPC750 @ 350MHz/100MHz bus) 3.3Vdc (±5%) (@ 100MHz bus) 32MB: 300mA typical, 450mA max 64MB: 400mA typical, 600mA max 128MB: 500mA typical, 750mA max
Operating temperature (refer to Cooling Requirements section)	0^{o} to 55^{o} C at point of exit of forced air
Storage Temperature	-40^{o} to $+85^{o}$ C
Relative Humidity	5% to 90% (non-condensing)
Physical Dimensions (DRAM Memory module only)	Width: 74mm (2.91 inches) Length: 145.8mm (5.74 inches) PPMC750-2xxx height above carrier: 18.8mm (0.74 in)

B

Cooling Requirements

The PPMC750-2xxx module is specified, designed, and tested to operate reliably when mounted on a carrier board with an incoming air temperature range from 0° to 55° C (32° to 131° F) with forced air cooling at a velocity typically achievable by using a 100 CFM axial fan.

Temperature qualification is performed in a standard Motorola VMEsystem chassis. Thirty-six watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of two axial fans, rates at 100 CFM per fan, is placed directly under the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed in order to exercise the board under test. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55° C with increased airflow.

It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

EMC Compliance

The PPMC750-2xxx is an add-on module meant to be used in conjunction with standard VME or CompactPCI baseboard applications. As such, it is the responsibility of the OEM to meet the regulatory guidelines as determined by their application.

The PPMC750-2xxx has been tested in conjunction with a standard MCG baseboard and chassis for CE certification and meets the requirements for EN55022 Class A equipment. Compliance was achieved under the following conditions:

- Shielded cables on all external I/O ports.
- Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

PPMC750-2xxx VPD Reference Information

C

Vital Product Data (VPD) Introduction

The Vital Product Data (VPD) portion of on-board memory contains static board build information, which is typically used for board initialization, configuration, and verification. The PPMC750-2xxx VPD is stored in the board's SROM and contains local hardware configuration information. The data in the VPD portion of the SROM consists of a header section, followed by contiguous formatted data packets. The header section consists of eye-catcher and size fields, and the data packets consist of identifier, data length and data content fields.

The header section begins with an eye-catcher field that can be used to verify the existence of an initialized VPD SROM (an EEPROM CRC packet is also used to verify the integrity of the VPD content). The size field contains the total number of bytes assigned to the VPD portion of the SROM.

Each packet begins with a unique identifier field that defines the content and data structures of the packet's data section. The data length field contains the size of the data section in bytes which is also added to the data section base address to locate the starting address of the following VPD packet. Different data section lengths are sometimes used to denote different revision levels or array sizes for packets of a particular identifier. Packets must be contiguous, but may be placed in any order. The termination packet identifier marks the end of the VPD and must immediately follow the last valid packet. Common VPD packets include assigned ethernet address, board serial number, processor internal/external clock frequency, processor identifier, connector population, and other packets.

Users may add additional data packets which are assigned to the user range of packet identifiers and adhere to the data structure described in this appendix. Although the addition of user packets is discouraged, one potential user packet application is the specification of field installed hardware modules.

The data listed in the following tables are for general reference information. The VPD identifies board information that may be useful during board initialization, configuration and verification.

VPD Definitions - Packet Types

The following table describes and lists the currently assigned packet identifiers. **Note: Additional packet identifiers may be added to this list as future versions of the VPD are released.**

Table C-1. VPD Packet Types

ID#	Size	Description	Data Type	Notes
00	N/A	Guaranteed Illegal	N/A	
01	Variable	Product Identifier (e.g., “PPMC750”, “MCP750”, “MVME2400”, “PPMC750-2xxx”, “PPMCBASE,” etc.)	ASCII	1
02	Variable	Factory Assembly Number (e.g., “01-W3512F01x”, etc.)	ASCII	1
03	Variable	Serial Number (e.g., “3383185”, etc.)	ASCII	1
04	10	Product Configuration Options Data The data in this packet further describes the board configuration (e.g., header population, I/O routing, etc.). Its exact contents is dependent upon the product configuration/type. A following table describes this packet.	Binary	
05	04	MPU Internal Clock Frequency in Hertz (e.g., 350,000,000 decimal, etc.)	Integer (4-byte)	2
06	04	MPU External Clock Frequency in Hertz (e.g., 100,000,000 decimal, etc.). This is also called the local processor bus frequency.	Integer (4-byte)	2
07	04	Reference Clock Frequency in Hertz (e.g., 32,768 decimal, etc.). This value is the frequency of the crystal driving the OSCM.	Integer (4-byte)	2
08	06	Ethernet Address (e.g., 08003E26A475, etc.)	Binary	3, 4
09	Variable	MPU Type (e.g., 601, 602, 603, 604, 750, 801, 821, 823, 860, 860DC, 860DE, 860DH, 860EN, 860MH, etc.)	ASCII	1
0A	04	EEPROM CRC This packet is optional. This packet would be utilized in environments where CRC protection is required. When computing the CRC this field (i.e., 4 bytes) is set to zero. This CRC only covers the range as specified the size field.	Integer (4-byte)	2

Table C-1. VPD Packet Types (Continued)

ID#	Size	Description	Data Type	Notes
0B	0C	FLASH Memory Configuration A table found later in this document further describes this packet.	Binary	
0C	TBD	VLSI Device Revisions/Versions	Binary	
0D	04	Host PCI-Bus Clock Frequency in Hertz (e.g., 33,333,333 decimal, etc.)	Integer (4-byte)	2
0E	0F	L2 Cache Configuration A table found later in this document further describes this packet.	Binary	
0F	04	VPD Revision. A table found later in this section further describes this packet.	Binary	
10-BF		Reserved		
C0-FE		User Defined An example of a user defined packet could be the type of LCD panel connected in an MPC821 based application.		
FF	N/A	Termination Packet (follows the last initialized data packet)	N/A	

Notes:

1. Data size varies, depending on the product configuration/type.
2. Integer values are formatted/stored in big-endian byte ordering.
3. This packet may be omitted if the ethernet interface is non-existent, or the ethernet interface has an associative SROM (e.g., DEC21x4x).
4. This packet may contain an additional byte following the address data. This additional byte indicates the ethernet interface number and is specified in applications where the host product supports multiple ethernet interfaces. For each ethernet interface present, the instance number is incremented by one starting with zero.

VPD Definitions - Product Configuration Options Data

The product configuration options data packet consists of a binary bit field. The first bit of the first byte is bit 0 (i.e., PowerPC bit numbering). An option is present when the assigned bit is a one. the following table further describes the product configuration options VPD data packet:

Table C-2. MCG Product Configuration Options Data

Bit Number	Bit Mnemonic	Bit Description
0	PCO_PCI0_CONN1	PCI/PMC bus 0 connector 1 present
1	PCO_PCI0_CONN2	PCI/PMC bus 0 connector 2 present
2	PCO_PCI0_CONN3	PCI/PMC bus 0 connector 3 present
3	PCO_PCI0_CONN4	PCI/PMC bus 0 connector 4 present
4	PCO_PCI1_CONN1	PCI/PMC bus 1 connector 1 present
5	PCO_PCI1_CONN2	PCI/PMC bus 1 connector 2 present
6	PCO_PCI1_CONN3	PCI/PMC bus 1 connector 3 present
7	PCO_PCI1_CONN4	PCI/PMC bus 1 connector 4 present
8	PCO_ISA_CONN1	ISA bus connector 1 present
9	PCO_ISA_CONN2	ISA bus connector 2 present
10	PCO_ISA_CONN3	ISA bus connector 3 present
11	PCO_ISA_CONN4	ISA bus connector 4 present
12	PCO_EIDE1_CONN1	IDE/EIDE device 1 connector 1 present
13	PCO_EIDE1_CONN2	IDE/EIDE device 1 connector 2 present
14	PCO_EIDE2_CONN1	IDE/EIDE device 2 connector 1 present
15	PCO_EIDE2_CONN2	IDE/EIDE device 2 connector 2 present
16	PCO_ENET1_CONN	Ethernet device 1 connector present
17	PCO_ENET2_CONN	Ethernet device 2 connector present
18	PCO_ENET3_CONN	Ethernet device 3 connector present
19	PCO_ENET4_CONN	Ethernet device 4 connector present
20	PCO_SCSI1_CONN	SCSI device 1 connector present
21	PCO_SCSI2_CONN	SCSI device 2 connector present
22	PCO_SCSI3_CONN	SCSI device 3 connector present
23	PCO_SCSI4_CONN	SCSI device 4 connector present
24	PCO_SERIAL1_CONN	Serial device 1 connector present

Table C-2. MCG Product Configuration Options Data (Continued)

Bit Number	Bit Mnemonic	Bit Description
25	PCO_SERIAL2_CONN	Serial device 2 connector present
26	PCO_SERIAL3_CONN	Serial device 3 connector present
27	PCO_SERIAL4_CONN	Serial device 4 connector present
28	PCO_FLOPPY_CONN1	Floppy device connector 1 present
29	PCO_FLOPPY_CONN2	Floppy device connector 2 present
30	PCO_PARALLEL1_CONN	Parallel device 1 connector present
31	PCO_PARALLEL2_CONN	Parallel device 2 connector present
32	PCO_PMC1_IO_CONN	PMC slot 1 I/O connector present
33	PCO_PMC2_IO_CONN	PMC slot 2 I/O connector present
34	PCO_USB0_CONN	USB channel 0 connector present
35	PCO_USB1_CONN	USB channel 1 connector present
36	PCO_KEYBOARD_CONN	Keyboard connector present
37	PCO_MOUSE_CONN	Mouse connector present
38	PCO_VGA1_CONN	VGA device 1 connector present
39	PCO_SPEAKER_CONN	Speaker connector present
40	PCO_VME_CONN	VME backplane connector present
41	PCO_CPCI_CONN	Compact PCI backplane connector present
42	PCO_ABORT_SWITCH	Abort switch present
43	PCO_BDFAIL_LIGHT	Board fail light present
44	PCO_SWREAD_HEADER	Software readable header present
45	PCO_MEMMEZ_CONN	Memory mezzanine connector present
46	PCO_PCI0_EXP_CONN	PCI bus 0 expansion connector present
47		Reserved for future configuration options
48	PCO_DIMM1_CONN	DIMM slot 1 connector present
49	PCO_DIMM2_CONN	DIMM slot 2 connector present
50	PCO_DIMM3_CONN	DIMM slot 3 connector present
51	PCO_DIMM4_CONN	DIMM slot 4 connector present
52-127		Reserved for future configuration options

VPD Definitions - FLASH Memory Configuration Data

The FLASH memory configuration data packet consists of byte fields which indicate the size/organization/type of the FLASH memory array. The following table(s) further describe the FLASH memory configuration VPD data packet.

Table C-3. FLASH Memory Configuration Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	2	FMC_MID	Manufacturer's Identifier (FFFF = Undefined/Not-Applicable)
02	2	FMC_DID	Manufacturer's Device Identifier (FFFF = Undefined/Not-Applicable)
04	1	FMC_DDW	Device Data Width (e.g., 8-bits, 16-bits)
05	1	FMC_NOD	Number of Devices/Sockets Present
06	1	FMC_NOC	Number of Columns (Interleaves)
07	1	FMC_CW	Column Width in Bits This will always be a multiple of the device's data width.
08	1	FMC_WEDW	Write/Erase Data Width The FLASH memory devices must be programmed in parallel when the write/erase data width exceeds the device's data width.
09	1	FMC_BANK	Bank Number of FLASH Memory Array: 0 = A, 1 = B
0A	1	FMC_SPEED	ROM Access Speed in Nanoseconds
0B	1	FMC_SIZE	Total Bank Size (Should agree with the physical organization above): 00=256K, 01=512K, 02=1M, 03=2M, 04=4M, 05=8M

A product may contain multiple FLASH memory configuration packets.

VPD Definitions - L2 Cache Configuration Data

The L2 cache configuration data packet consists of byte fields that show the size, organization, and type of the L2 cache memory array. The following table(s) further describe the L2 cache memory configuration VPD data packet.

Table C-4. L2 Cache Configuration Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	2	L2C_MID	Manufacturer's Identifier (FFFF = Undefined/Not-Applicable)
02	2	L2C_DID	Manufacturer's Device Identifier (FFFF = Undefined/Not-Applicable)
04	1	L2C_DDW	Device Data Width (e.g., 8-bits, 16-bits, 32-bits, 64-bits, 128-bits)
05	1	L2C_NOD	Number of Devices Present
06	1	L2C_NOC	Number of Columns (Interleaves)
07	1	L2C_CW	Column Width in Bits This will always be a multiple of the device's data width.
08	1	L2C_TYPE	L2 Cache Type: 00 - Arthur Backside 01 - External 02 - In-Line
09	1	L2C_ASSOCIATE	Associative Microprocessor Number (If Applicable)
0A	1	L2C_OPERATIONMODE	Operation Mode: 00 - Either Write-Through or Write-Back (S/W Configurable) 01 - Either Write-Through or Write-Back (H/W Configurable) 02 - Write-Through Only 03 - Write-Back Only

C

Table C-4. L2 Cache Configuration Data (Continued)

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
0B	1	L2C_ERROR_DETECT	Error Detection Type: 00 - None 01 - Parity 02 - ECC
0C	1	L2C_SIZE	L2 Cache Size (Should agree with the physical organization above): 00 - 256K 01 - 512K 02 - 1M 03 - 2M 04 - 4M
0D	1	L2C_TYPE_BACKSIDE	L2 Cache Type (Backside Configurations): 00 - Late Write Sync, 1nS Hold, Differential Clock, Parity 01 - Pipelined Sync Burst, 0.5nS Hold, No Differentia Clock, Parity 02 - Late Write Sync, 1nS Hold, Differential Clock, No Parity 03 - Pipelined Sync Burst, 0.5nS Hold, No Differential Clock, No Parity
0E	1	L2C_RATIO_BACKSIDE	L2 Cache Core to Cache Ration (Backside Configurations): 00 - Disabled 01 - 1:1 (1) 02 - 3:2 (1.5) 03 - 2:1 (2) 04 - 5:2 (2.5) 05 - 3:1 (3)

A product may contain multiple L2 cache configuration packets.

VPD Definitions - VPD Revision Data

The VPD revision data packet consists of byte fields that indicate the type, version, and revision of the vital product data. The following table(s) further describe the VPD revision data packet.

Table C-5. VPD Revision Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	1	VR_TYPE	Vital Product Data Type: 00 - Processor board VPD 01 - Baseboard (non-processor) VPD 02 - Transition module VPD
01	1	VR_ARCH	Vital Product Data Architecture Revision (currently at 2)
02	1	VR_BUILD	Vital Product Data Board Build Revision (starts at 0)
03	1	VR_REASON	Vital Product Data Revision Flags: 00 - Initial release

A product must have exactly one VPD revision packet.

C

SROM_CRC.C

```
/*
 * srom_crc - generate CRC data for the passed buffer
 * description:
 * This function's purpose is to generate the CRC for the
 * passed buffer.
 * call:
 *    argument #1 = buffer pointer
 *    argument #2 = number of elements
 * return:
 *    CRC data
 */
unsigned int
srom_crc(elements_p, elements_n)
register unsigned char *elements_p; /* buffer pointer */
register unsigned int elements_n;   /* number of elements */
{
   register unsigned int crc;
   register unsigned int crc_flipped;
   register unsigned char cbyte;
   register unsigned int index, dbit, msb;

   crc = 0xffffffff;
   for (index = 0; index < elements_n; index++) {
      cbyte = *elements_p++;
      for (dbit = 0; dbit < 8; dbit++) {
         msb = (crc >> 31) & 1;
         crc <<= 1;
         if (msb ^ (cbyte & 1)) {
            crc ^= 0x04c11db6;
            crc |= 1;
         }
         cbyte >>= 1;
      }
   }
crc_flipped = 0;
   for (index = 0; index < 32; index++) {
      crc_flipped <<= 1;
      dbit = crc & 1;
      crc >>= 1;
      crc_flipped += dbit;
   }
   crc = crc_flipped ^ 0xffffffff;
   return (crc);
}
```

Calculation of Checksum for the Configuration Information

Table C-6. Config. Parameters for the PPMC750-2xxx

	Parameters
Start Location in Flash	0x7F9EF8
Structure Size	0xF7
Checksum Location	Start + 0xF7 = 0x7F9FEF
Offset ending with the following should be programmed on to U26 0, 1, 2, 3 8, 9, A, B	U26
Offset ending with the following should be programmed on to U26 4, 5, 6, 7 C, D, E, F	U25

```
struct brdi_cnfg {
  char version[4];     /* version of this structure in ascii */
  char serial[12];     /* board serial number in ascii */
  char id[16];         /* board identifier in ascii */
  char pwa[16];        /* pwa identifier in ascii */
  char reserved_1[4];  /* reserved */
  char ethernet[6];    /* ethernet address */
  char reserved_2[2];  /* reserved */
  char lscsiid[2];     /* local scsi identifier (address of host) */
  char speed_mpu[3];   /* MPU speed in megahertz (i.e. '150' = 150Mhz) */
  char speed_bus[3];   /* BUS speed in megahertz (i.e. '075' = 75Mhz) */
  char system_sn[16];  /* system serial number in ascii */
  char system_id[31];  /* system identifier in ascii */
  char license_id[9];  /* license identifier in ascii */
  char reserved[123];  /* reserved for future expansion */
  char cksum;          /* checksum of this structure */
};
```

Figure C-1. Config. Structure for the CNFG Area

The following code in 'C' is the checksum function for the configuration area.

```
/* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
 *
 * cssect - checksum section
 * description:
 *      This component's purpose is to checksum the buffer pointed to
 *      by the buffer pointer.
 * notes:
 * call:
 *      argument #1 = buffer (section) to checksum
 *      argument #2 = number of bytes in buffer
 * return:
 *      0xXX            = checksum
 */
UCHAR
cssect(nvram_ptr, count)
register UCHAR *nvram_ptr;        /* NVRAM buffer pointer */
register UINT count;              /* count, number of bytes */
{
   register UCHAR y, isum, sum;
   for (sum = 0; count; count--) {
      y = *nvram_ptr++;
      isum = sum + y;
      if ((isum < y) || (isum < sum)) isum += 1;
      sum = isum;
   }
   return (sum);                  /* return calculated checksum */
```

Figure C-2. Config. Checksum Calculation Code

Ethernet SROM Contents for PPMC750-2xxx Boards

The following table describes and lists the contents of the Ethernet SROM which is programmed onto the raw PPMC750-2xxx part number 51NW9637H66. Note: not part of VPD SROM.

C

Table C-7. Ethernet SROM Configuration Contents for 01-W3512Fxxr*

OFFSET	VALUE	DESCRIPTION
00 (0x00)	57	SubSystem Vendor ID lower byte - Optional and manufacturer defined Eye-Catcher (“MOTOROLA”) **Note: Lowest CRC byte for the calculation of CRC**.
01 (0x01)	10	SubSystem Vendor ID upper byte - Optional and manufacturer defined.
02 (0x02)	56	SubSystem ID lower byte - Optional and manufacturer defined.
03 (0x03)	34	SubSystem ID upper byte - Optional and manufacturer defined.
04 (0x04)	00	Pointer to Card Bus (if supported - must be zero if not supported)
05 (0x05)	00	Pointer byte 2
06 (0x06)	00	Pointer byte 3
07 (0x07)	00	Pointer byte 4
08 (0x08)	00	ID_Reserved1 (8 bytes).
09 (0x09)	00	ID_Reserved1 byte 2
10 (0x0a)	00	ID_Reserved1 byte 3
11 (0x0b)	04	ID_Reserved1 byte 4
12 (0x0c)	00	ID_Reserved1 byte 5
13 (0x0d)	02	ID_Reserved1 byte 6
14 (0x0e)	00	ID_Reserved1 byte 7
15 (0x0f)	00	ID_Reserved1 byte 8
16 (0x10)	13	ID_BLOCK_CRC - CRC of bytes in offsets 00-15
17 (0x11)	00	ID_Reserved2
18 (0x12)	03	SROM format Version “Version 3”.
19 (0x13)	01	Number of controllers sharing this SROM
20 (0x14)	08	MAC address byte 1
21 (0x15)	00	MAC address byte 2
22 (0x16)	3e	MAC address byte 3
23 (0x17)	xx	MAC address byte 4 - defined at ATE
24 (0x18)	xx	MAC address byte 5 - defined at ATE

Table C-7. Ethernet SROM Configuration Contents for 01-W3512Fxxr* (Continued)

OFFSET	VALUE	DESCRIPTION
25 (0x19)	xx	MAC address byte 6 - defined at ATE
26 (0x1a)	0e	Controller Device number (this should be PCE DEVSEL for chip). This is the device ID for PCI configuration cycles to this device.
27 (0x1b)	1e	Offset to controller leaf information (0x1e = byte 30d)
28 (0x1c)	00	Offset to controller lead information MSB
29 (0x1d)	00	Controller offset list NULL terminator (Must be zero)
30 (0x1e)	00	**Controller 1 Info lead start**: LSB of driver last connection type (AutoSense 0x0800)
31 (0x1f)	08	MSB of connection type (AutoSense 0x0800)
32 (0x20)	01	Media Count - 1 media supported by this device (TP).
33 (0x21)	93	Format/Length (Extended Format 13 bytes long)
34 (0x22)	03	Block Type (0x03 = MII PHY chips only)
35 (0x23)	00	PHY number (index of the PHY controlled by this block)
36 (0x24)	00	GPR Sequence Length
37 (0x25)	03	Reset Sequence Length
38 (0x26)	01	Reset Sequence (0801, 0000, 0001)
39 (0x27)	08	
40 (0x28)	00	
41 (0x29)	00	
42 (0x2a)	01	
43 (0x2b)	00	
44 (0x2c)	00	Media Capabilities (0x7800) - 100Tx-FD/HD 10T-FD/HD
45 (0x2d)	78	Media Capabilities MSB
46 (0x2e)	e0	Nway advertisement 100Tx-FD/HD, 10T-FD/HD
47 (0x2f)	01	Nway advertisement MSB
48 (0x30)	00	Full duplex map - in order to support Full Duplex these bits
49 (0x31)	50	in Media capabilities mask are to be written. 100/10FD bits.
50 (0x32)	00	Transmit Threshold Bit Map - these bits describe which media
51 (0x33)	18	capabilities mask are to be written. (100 base medium only)

Table C-7. Ethernet SROM Configuration Contents for 01-W3512Fxxr* (Continued)

OFFSET	VALUE	DESCRIPTION
52 (0x34)	00	MII Connector Interrupt
53 (0x35)	00	
:	:	
125 (0x7d)	00	
126 (0x7e)	yy	Lower CRC byte - CRC for entire SROM (Refer to
127 (0x7f)	yy	Upper CRC byte

Note *This data will change to reflect the specific configuration of the corresponding board assembly number to which it applies.

VPD SROM Contents for PPMC750 (01-W3512Fxx) Boards

The following tables describe the variable and static contents of the VPD that is programmed onto the PPMC750's raw part number 51NW9637L49. Table B-7 contains the variable data and Table B-8 contains the static data.

Table C-8. Variable VPD Contents Specifications for 01-W3512Fxx

Offset	01-W3512F02	01-W3512F07
Field Description: Product Identifier (Packet ASCII)		
26 (0x1a)	32	32
27 (0x1b)	31	32
28 (0x1c)	34	35
29 (0x1d)	31	31
Field Description: Assembly Number (Packet ASCII)		
41 (0x29)	30	30
42 (0x2a)	32	37
43 (0x2b)	xx	xx
Field Description: L2 Cache Configuration (Packet Binary)		
120 (0x78)	03	04

Table C-9. Static VPD SROM Configuration Specifications for 01-W3512Fxx

Offset	Value	Field Type	Description
00 (0x00)	4D	ASCII	Eye-Catcher ("MOTOROLA") Note: Starting byte for the calculation of CRC
01 (0x01)	4F		
02 (0x02)	54		
03 (0x03)	4F		
04 (0x04)	52		
05 (0x05)	4F		
06 (0x06)	4C		

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Table C-9. Static VPD SROM Configuration Specifications for 01-W3512Fxx (Continued)

Offset	Value	Field Type	Description
07 (0x07)	41		
08 (0x08)	01	BINARY	Size of VPD area in bytes. The size is viewed as logical, it is not the size of the EEPROM.
09 (0x09)	00		
10 (0x0a)	0F	PACKET BINARY	VPD Revision
11 (0x0b)	04		
12 (0x0c)	00		
13 (0x0d)	02		
14 (0x0e)	00		
15 (0x0f)	00		
16 (0x10)	01	PACKET ASCII	Product Identifier [**PPMC750-xxxx]. Refer to the previous table for 'xx' values.**
17 (0x11)	0C		
18 (0x12)	50		
19 (0x13)	50		
20 (0x14)	4D		
21 (0x15)	43		
22 (0x16)	37		
23 (0x17)	35		
24 (0x18)	30		
25 (0x19)	2D		
26 (0x1a)	xx		
27 (0x1b)	xx		
28 (0x1c)	xx		
29 (0x1d)	xx		
30 (0x1e)	02	PACKET ASCII	Factory Assembly Number [**01-W3512Fxx*]**
31 (0x1f)	0C		
32 (0x20)	30		

Table C-9. Static VPD SROM Configuration Specifications for 01-W3512Fxx (Continued)

Offset	Value	Field Type	Description
33 (0x21)	31		
34 (0x22)	2D		
35 (0x23)	57		
36 (0x24)	33		
37 (0x25)	35		
38 (0x26)	31		
39 (0x27)	32		
40 (0x28)	46		
41 (0x29)	xx		To be filled in at ATE. Refer to the previous table for the ‘xx’ values.
42 (0x2a)	xx		
43 (0x2b)	xx		
44 (0x2c)	03		
45 (0x2d)	07		
46 (0x2e)	xx		
47 (0x2f)	xx		
48 (0x30)	xx		
49 (0x31)	xx		
50 (0x32)	xx		
51 (0x33)	xx		
52 (0x34)	xx		
53 (0x35)	04	PACKET BINARY	Product Configuration Options Data.
54 (0x36)	10		
55 (0x37)	80		
56 (0x38)	00		
57 (0x39)	80		
58 (0x3A)	80		
59 (0x3B)	80		
60 (0x3C)	34		
61 (0x3D)	00		

Table C-9. Static VPD SROM Configuration Specifications for 01-W3512Fxx (Continued)

Offset	Value	Field Type	Description
62 (0x3E)	00		
63 (0x3F)	00		
64 (0x40)	00		
65 (0x41)	00		
66 (0x42)	00		
67 (0x43)	00		
68 (0x44)	00		
69 (0x45)	00		
70 (0x46)	00		
71 (0x47)	09	PACKET ASCII	MPU Type [750]
72 (0x48)	03		
73 (0x49)	37		
74 (0x4A)	35		
75 (0x4B)	30		
76 (0x4C)	0B	PACKET BINARY	FLASH Memory Configuration (Bank A)
77 (0x4D)	0C		
78 (0x4E)	00		
79 (0x4F)	01		
80 (0x50)	00		
81 (0x51)	50		
82 (0x52)	08		
83 (0x53)	02		
84 (0x54)	02		
85 (0x55)	08		
86 (0x56)	08		
87 (0x57)	00		
88 (0x58)	78		
89 (0x59)	05		

Table C-9. Static VPD SROM Configuration Specifications for 01-W3512Fxx (Continued)

Offset	Value	Field Type	Description
90 (0x5A)	0B	PACKET BINARY	FLASH Memory Configuration (Bank A)
91 (0x5B)	0C		
92 (0x5C)	FF		
93 (0x5D)	FF		
94 (0x5E)	FF		
95 (0x5F)	FF		
96 (0x60)	08		
97 (0x61)	02		
98 (0x62)	02	:	:
99 (0x63)	08		
100 (0x64)	08		
101 (0x65)	01		
102 (0x66)	78		
103 (0x67)	02		
104 (0x68)	OE	PACKET BINARY	L2 Cache Configuration. Refer to the previous table for ‘xx’ values.
105 (0x69)	OF		
106 (0x6A)	FF		
107 (0x6B)	FF		
108 (0x6C)	FF		
109 (0x6D)	FF		
110 (0x6E)	20		
111 (0x6F)	02		
112 (0x70)	02		
113 (0x71)	20		
114 (0x72)	00		
115 (0x73)	00		
116 (0x74)	00		
117 (0x75)	01		
118 (0x76)	02		

Table C-9. Static VPD SROM Configuration Specifications for 01-W3512Fxx (Continued)

Offset	Value	Field Type	Description
119 (0x77)	01		
120 (0x78)	xx		
121 (0x79)	0A	PACKET INTEGER	EPPROM CRC When computing the CRC, this field (i.e., 4 bytes) is set to zero. This CRC only covers the range as Integer (4-byte). Refer to the section on CRC calculation preceeding this table for more information. **Note: Starting byte for the calculation of CRC = 00. End byte for the calculation of CRC = 255**
122 (0x7A)	04		
123 (0x7B)	xx		CRC to be filled in at ATE
124 (0x7C)	xx		
125 (0x7D)	xx		
126 (0x7E)	xx		
127 (0x7F)	FF	BINARY	Reserved for future expansion.
:	:		
255 (0xFF)	FF		Reserved for future expansion Note: End byte for the calculation of CRC

Config. Contents for 01-W3512Fxxr* Boards

The following tables describe and list the static, as well as variable contents of the Config. data to be programmed onto Raw Part number 51NW9655D34 and is arranged in the following order:

Table C-10 contains only the variable contents of Config. Flash Contents for 01-W3512Fxx* boards.

Table C-11 contains only the static contents of Config. Flash Contents for 01-W3512Fxx* boards.

Note This data is not static, each board must be assigned a unique ID.
The last 3 characters of the Factory Assembly Number should be programmed at ATE.
The method that ATE uses to program the Serial Number and other unique per board Config. packet types requires that this packet be located in an absolute fixed location. For this reason, the Serial Number packet shall have a fixed size and shall immediately follow.

Table C-10. Variable Config. Flash Contents for 01-W3512Fxx

Offset	01-W3512F02	01-W3512F07
Field Description: Product Identifier in ASCII (16 bytes)		
8363792 (0x7F9F10)	32	32
8363793 (0x7F9F11)	31	32
8363794 (0x7F9F12)	34	35
8363795 (0x7F9F13)	31	31
Field Description: PWA Identifier in ASCII (16 bytes)		
8363809 (0x7F9F21)	30	30
8363810 (0x7F9F22)	32	37
8363811 (0x7F9F23)	xx	xx
Field Description: MPU Speed in megahertz in ASCII (3 bytes) [xxx MHz]		
8363830 (0x7F9F36)	32	33
8363831 (0x7F9F37)	33	35
8363832 (0x7F9F38)	33	30
Field Description: BUS Speed in megahertz in ASCII (3 bytes) [xxx MHz]		
8363833 (0x7F9F39)	30	31
8363834 (0x7F9F3A)	36	30
8363835 (0x7F9F3B)	37	30

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Table C-11. Static Config. Flash Image Contents 01-W3512xx* Boards

Part No.	OffSet		HEX Value	Description
U26	8363768	0x7F9EF8	30	Version of this Structure in ASCII (4 bytes)
	8363769	0x7F9EF9	33	
	8363770	0x7F9EFA	30	
	8363771	0x7F9EFB	30	
U25	8363772	0x7F9EFC	xx	**** Board Serial Number - (12 bytes) - Filled in at ATE**
	8363773	0x7F9EFD	xx	
	8363774	0x7F9EFE	xx	
	8363775	0x7F9EFF	xx	
U26	8363776	0x7F9F00	xx	
	8363777	0x7F9F01	xx	
	8363778	0x7F9F02	xx	
	8363779	0x7F9F03	20	
U25	8363780	0x7F9F04	20	
	8363781	0x7F9F05	20	
	8363782	0x7F9F06	20	
	8363783	0x7F9F07	20	
U26	8363784	0x7F9F08	50	Board Identifier in ASCII (16 bytes) [**PPMC750-xxxx**] **Refer to the previous table for 01-W3512Fxx* assemblies for "xx" values**
	8363785	0x7F9F09	50	
	8363786	0x7F9F0A	4D	
	8363787	0x7F9F0B	43	

Table C-11. Static Config. Flash Image Contents 01-W3512xx* Boards (Continued)

U25	8363788	0x7F9F0C	37	
	8363789	0x7F9F0D	35	
	8363790	0x7F9F0E	30	
	8363791	0x7F9F0F	2D	
U26	8363792	0x7F9F10	xx	
	8363793	0x7F9F11	xx	
	8363794	0x7F9F12	xx	
	8363795	0x7F9F13	xx	
U25	8363796	0x7F9F14	20	
	8363797	0x7F9F15	20	
	8363798	0x7F9F16	20	
	8363799	0x7F9F17	20	
U26	8363800	0x7F9F18	30	PWA Identifier in ASCII (16 bytes) **Refer to the previous table for 01-W3512Fxx* assemblies for "xx" values**
	8363801	0x7F9F19	31	
	8363802	0x7F9F1A	2D	
	8363803	0x7F9F1B	57	
U25	8363804	0x7F9F1C	33	
	8363805	0x7F9F1D	35	
	8363806	0x7F9F1E	31	
	8363807	0x7F9F1F	32	
U26	8363808	0x7F9F20	46	
	8363809	0x7F9F21	xx	
	8363810	0x7F9F22	xx	
	8363811	0x7F9F23	xx	

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Table C-11. Static Config. Flash Image Contents 01-W3512xx* Boards (Continued)

U25	8363812	0x7F9F24	20	
	8363813	0x7F9F25	20	
	8363814	0x7F9F26	20	
	8363815	0x7F9F27	20	
U26	8363816	0x7F9F28	55	Reserved (4 bytes)
	8363817	0x7F9F29	55	
	8363818	0x7F9F2A	55	
	8363819	0x7F9F2B	55	
U25	8363820	0x7F9F2C	xx	****Ethernet Address NOT ASCII (6 bytes) - Filled in at ATE.**
	8363821	0x7F9F2D	xx	
	8363822	0x7F9F2E	xx	
	8363823	0x7F9F2F	xx	
U26	8363824	0x7F9F30	xx	
	8363825	0x7F9F31	xx	
	8363826	0x7F9F32	55	Reserved (2 bytes)
	8363827	0x7F9F33	55	
U25	8363828	0x7F9F34	30	Local SCSI Identifier in ASCII (2 bytes) **[07]**
	8363829	0x7F9F35	37	
	8363830	0x7F9F36	xx	MPU Speed in megahertz in ASCII (3 bytes) **Refer to the previous table for 01-W3512xx* assemblies for "xx" values**
	8363831	0x7F9F37	xx	

Table C-11. Static Config. Flash Image Contents 01-W3512xx* Boards (Continued)

U26	8363832	0x7F9F38	xx	
	8363833	0x7F9F39	xx	BUS speed in megahertz in ASCII (bytes) **Refer to the previous table for 01-W3512xx* assemblies for "xx" values**
	8363834	0x7F9F3A	xx	
	8363835	0x7F9F3B	xx	
U25	8363836	0x7F9F3C	30	System Serial Number in ASCII (16 bytes)
	8363837	0x7F9F3D	20	
	8363838	0x7F9F3E	20	
	8363839	0x7F9F3F	20	
U26	8363840	0x7F9F40	20	
	8363841	0x7F9F41	20	
	8363842	0x7F9F42	20	
	8363843	0x7F9F43	20	
U25	8363844	0x7F9F44	20	
	8363845	0x7F9F45	20	
	8363846	0x7F9F46	20	
	8363847	0x7F9F47	20	
U26	8363848	0x7F9F48	20	
	8363849	0x7F9F49	20	
	8363850	0x7F9F4A	20	
	8363851	0x7F9F4B	20	
U25	8363852	0x7F9F4C	30	System Identifier in ASCII (31 bytes)
	8363853	0x7F9F4D	20	
	8363854	0x7F9F4E	20	
	8363855	0x7F9F4F	20	

C

Table C-11. Static Config. Flash Image Contents 01-W3512xx* Boards (Continued)

U26	8363856	0x7F9F50	20	
	8363857	0x7F9F51	20	
	8363858	0x7F9F52	20	
	8363859	0x7F9F53	20	
U25	8363860	0x7F9F54	20	
	8363861	0x7F9F55	20	
	8363862	0x7F9F56	20	
	8363863	0x7F9F57	20	
U26	8363864	0x7F9F58	20	
	8363865	0x7F9F59	20	
	8363866	0x7F9F5A	20	
	8363867	0x7F9F5B	20	
U25	8363868	0x7F9F5C	20	
	8363869	0x7F9F5D	20	
	8363870	0x7F9F5E	20	
	8363871	0x7F9F5F	20	
U26	8363872	0x7F9F60	20	
	8363873	0x7F9F61	20	
	8363874	0x7F9F62	20	
	8363875	0x7F9F63	20	
U25	8363876	0x7F9F64	20	
	8363877	0x7F9F65	20	
	8363878	0x7F9F66	20	
	8363879	0x7F9F67	20	

Table C-11. Static Config. Flash Image Contents 01-W3512xx* Boards (Continued)

U26	8363880	0x7F9F68	20	
	8363881	0x7F9F69	20	
	8363882	0x7F9F6A	20	
	8363883	0x7F9F6B	xx	**License Identifier in ASCII (9 bytes). **Filled in (Board Serial Number) at ATE**
U25	8363884	0x7F9F6C	xx	
	8363885	0x7F9F6D	xx	
	8363886	0x7F9F6E	xx	
	8363887	0x7F9F6F	xx	
U26	8363888	0x7F9F70	xx	
	8363889	0x7F9F71	xx	
	8363890	0x7F9F72	20	
	8363891	0x7F9F73	20	
U25	8363892	0x7F9F74	00	Reserved for future expansion (123 bytes)
	8363893	0x7F9F75	00	
	8363894	0x7F9F76	00	
	8363895	0x7F9F77	00	
U26	8363896	0x7F9F78	00	
	8363897	0x7F9F79	00	
	8363898	0x7F9F7A	00	
	8363899	0x7F9F7B	00	
U25	8363900	0x7F9F7C	00	
	:	:	:	:

Table C-11. Static Config. Flash Image Contents 01-W3512xx* Boards (Continued)

U26	8364010	0x7F9FEA	00	
	8364011	0x7F9FEB	00	
	8364012	0x7F9FEC	00	
	8364013	0x7F9FED	00	
U25	8364014	0x7F9FEE	00	Reserved for future expansion (123 bytes)
U25	8364015	0x7F9FEF	xx	**Checksum of this structure (1 byte). Filled in at ATE.

SPD Contents for 01-W3512Fxx* Boards

The following tables describe and list the static, as well as variable contents of the SPD to be programmed onto Raw Part number 51NW9655L49 and is arranged in the following order: Table C-12 contains only variable contents of SPD for 01-W3512Fxx*, Table C-13 contains static contents of SPD for 01-W3512Fxx* boards.

The 64MB SDRAM and the 128MB SDRAM are identified as follows:

- **64MB SDRAM** - (for 01-W3512F02 boards) SPD for 64megabytes using one bank of five 16-bit wide, 128megabit KM4116S803T-GL devices (51NW9655D88). These have a CAS Latency of 3 at 10ns clk cycle. CL3 affects byte 23 decimal. In this case its a c0 meaning CL of 2 requires 12ns.
- **128MB SDRAM** - (for 01-W3512F07 boards) SPD for 128megabyte using one bank of five 16-bit wide, 256megabit KM416S16230AT-GL devices (51NW9655D68). These have a CAS Latency of 3 at 10ns clk cycle. CL3 affects byte 23 decimal. In this case it is a c0 meaning CL of 2 requires 12ns.

Notes

Table C-12. Variable SPD Contents for 01-W3512Fxx*

Assembly No.	01-W3512F02	01-W3512F07
SDRAM Part Number	51NW9655D88	51NW9655D68*
Offset		
03 (0x03)	0C	0D
04 (0x04)	09	09
09 (0x09)	A0	A0
23 (0x17)	C0	C0
24 (0x18)	70	70
28 (0x1c)	14	14
30 (0x1e)	32	32
31 (0x1f)	10	20
63 (0x3F)	BD	CE

1. This will typically be programmed as 128 Bytes
2. This will typically be programmed as 256 Bytes
3. High order bit defines if assembly requires “redundant” addressing (if set to “1”, redundant addressing is required)
4. From datasheet
5. High order bit is Self Refresh “flag”. If set to “1”, the assembly supports self refresh.
6. The JEDEC spec specifies that these bytes are optional for 66MHz applications. If they are not included, then the SPD revision level (byte 62) is set at revision 1 (01h). . .

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Table C-13. Static SPD SROM Configuration for 01-W3512Fxx*

OFFSET	VALUE	FIELD TYPE	DESCRIPTION
00 (0x00)	80		Number of Serial PD Bytes written during module production. **Refer to Note 1**.
01 (0x01)	08		Total Number of Bytes in Serial PD Device. **Refer to Note 2.**
02 (0x02)	04		Fundamental Memory Type (FPM, EDO, SDRAM
03 (0x03)	xx		Number of Row Addresses on this assembly **Refer to Note 3**. **Refer to the previous tables for "xx" values.**
04 (0x04)	xx		Number of Column Addresses on this assembly. **Refer to the previous tables for "xx" values.**
05 (0x05)	01		Number of DIMM Banks
06 (0x06)	48		Data Width of this assembly
07 (0x07)	00		---as above---
08 (0x08)	01		Voltage Interface Level of this assembly
09 (0x09)	xx		SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X. **Refer to Note 4**. **Refer to the previous tables for "xx" values.**
10 (0x0a)	60		SDRAM Access from Clock.
11 (0x0b)	02		DIMM configuration type (Non-parity, Parity or ECC)
12 (0x0c)	00		Refresh Rate/Type Refer to Notes 4, 5
13 (0x0d)	10		Primary SDRAM Width
14 (0x0e)	10		Error Checking SDRAM Width
15 (0x0f)	01		SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back Random Column Access
16 (0x10)	8F		SDRAM Device Attributes: Burst Lengths Supported
17 (0x11)	04		SDRAM Device Attributes: Number of Banks on SDRAM Device. **Refer to Note: 4**

Table C-13. Static SPD SROM Configuration for 01-W3512Fxx* (Continued)

OFFSET	VALUE	FIELD TYPE	DESCRIPTION
18 (0x12)	06		SDRAM Device Attributes: CAS Latency. **Refer to Note 4.**
19 (0x13)	01		SDRAM Device Attributes: CS Latency. **Refer to Note 4.**
20 (0x14)	01		SDRAM Device Attributes: Write Latency. **Refer to Note 4**.
21 (0x15)	00		SDRAM Module Attributes
22 (0x16)	0E		SDRAM Device Attributes: General. **Refer to Note: 4.**
23 (0x17)	xx		Minimum Clock Cycle at CLX-1. **Refer to Note 4. Refer to the previous tables for "xx" values.**
24 (0x18)	xx		Maximum Data Access Time (t AC) from Clock at CLX-1. **Refer to Note 4. Refer to the previous tables for "xx" values.**
25 (0x19)	00		Minimum Clock Cycle at CLX-2. **Refer to Note 4.**
26 (0x1a)	00		Maximum Data Access Time (t AC) from Clock at CLX-2. **Refer to Note 4.**
27 (0x1b)	14		Minimum Row Precharge Time (t RP). **Refer to Note 4.**
28 (0x1c)	xx		Minimum Row Active to Row Active delay (t RRD). **Refer to Note 4. Refer to the previous table for "xx" values.**
29 (0x1d)	14		Minimum RAS to CAS delay (t RCD). **Refer to Note 4.**
30 (0x1e)	xx		Minimum RAS Pulse width (t RAS). **Refer to Note 4. Refer to the previous tables for "xx" values.**
31 (0x1f)	xx		Module Bank Density
32 (0x20)	20		Address and Command Setup Time Before Clock. **Refer to Note: 6.**

Table C-13. Static SPD SROM Configuration for 01-W3512Fxx* (Continued)

OFFSET	VALUE	FIELD TYPE	DESCRIPTION
33 (0x21)	10		Address and Command Hold Time After Clock. **Refer to Note: 6.**
34 (0x22)	20		Data Input Setup Time Before Clock. **Refer to Note: 6.**
35 (0x23)	10		Data Input Hold Time After Clock. **Refer to Note: 6.**
36 (0x24)	FF		Reserved for future expansion
:	:	:	:
61 (0x3D)	FF		
62 (0x3E)	12		SPD Revision
63 (0x3F)	xx		**Checksum for bytes 0-62. Refer to the previous tables for "xx" values.**
64 (0x40)	FF		Reserved for future expansion
:	:		
255 (0xFF)	FF		

Index

D

E

F

G

H

INDEX

INDEX

INDEX

R

S

T

INDEX

U

V

PPMC750 Extended Processor PMC Module Installation and Use