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PENT/CPCI-731
Reference Guide

P/N 211604 Edition 1.2
May 2000

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List of Tables and Figures

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Using This Manual

This section does not provide information on the product, but on standard features of the manual itself:

- Its structure
- Special layout conventions
- Related documents

Audience of the Manual

This *Reference Guide* is intended for hard- and software developers installing and integrating the PENT/CPCI-731 into their systems.

Overview of the Manual

This *Reference Guide* provides a comprehensive hardware and software guide to your board.

Note: **Please take a moment to examine the "Table of Contents" to see how this documentation is structured. This will be of value to you when looking for information in the future.**

It includes:

- Brief overview of the PENT/CPCI-731: see section 2 "Introduction" on page 5.
- Installation instructions for powering up the board: see section 3 "Installation" on page 9. It includes the default configuration (switches and the like), initialization, connector pinouts, and the BIOS details.
- Block diagram relating the most important components and a description of the PENT/CPCI-731 specific registers: section 4 "Hardware" on page 33.

Data Sheets

It is assumed that the PENT/CPCI-731 is integrated into systems at the operating system level. Therefore, no data sheets are provided in this *Reference Guide*. Nevertheless, all data sheets of the most important board components are listed below. They can be found on the respective company's webpage.

- BIOS flash - 1Mx8, 28F008S5, 28F800B5 (developer.intel.com)
- CPU - Intel Pentium II

  Intel Pentium II Processor Mobile Module: Mobile Module Connector 2 (MMC-2) (developer.intel.com)

  Intel Architecture Software Developer's Manual; Volume 1: Basic Architecture, Volume 2: Instruction Set Reference Manual, Volume 3: System Programming Guide
- EIDE, PCI-to-ISA bridge, USB - 82371AB (82371EB) (developer.intel.com)
- Ethernet - 82559 (developer.intel.com)
- Hardware monitor - W83781D (http://www.winbond.com)
- Host-to-PCI bridge - 82443BX (developer.intel.com)
- IDE flash disk - SanDisk FlashChipset, SDFCSTB-128-366 (www.sandisk.com)
- I^2C bus - "The I^2C-bus and how to use it (including specifications)" (http://www.philips.com)
- Keyboard, PS2 mouse, COM1, COM2, LPT1, floppy - National PC87309 SuperI/O (www.national.com)
- PCI-to-PCI bridge - 21150 (developer.intel.com)
- PCI-to-PCI bridge - 21554 (developer.intel.com)
- Synchronous DRAM - Hitachi/Micron/Mitsubishi 8Mx8 (M5M4V64S30A) (www.halsp.hitachi.com)

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Table a History of Manual Publication

Edition	Date	Description
1.0	December 1999	First Print
1.1	January 2000	Corrected Forced Air Flow in **table 4 “Environmental Requirements of the PENT/CPCI-731” on page 9**; corrected table 19 “NMI Control Register” on page 51; editorial changes
1.2	May 2000	Corrected IRQ settings in table 29 “Hot Swap ENUM Register” on page 67; changed SW2-3 to ON in table 6 “PENT/CPCI-731 Switch Settings” on page 14; editorial changes

Table b Fonts, Notations and Conventions

Notation	Description
	All numbers are decimal numbers except when used with the following notations:
`0000.0000`$_{16}$	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets. Note the dot marking the 4th (to its right) and 5th (to its left) digit.
`0000`$_{8}$	Same for octal numbers (digits are 0 through 7)
`0000`$_{2}$	Same for binary numbers (digits are 0 and 1)
`Program`	Typical character format used for names, values, and the like. It is used to indicate when to type literally the same word. Also used for on-screen output.
Variable	Typical character format for words that represent a part of a command, a programming statement, or the like, and that will be replaced by an applicable value when actually applied.

Icons for Ease of Use: Safety Notes and Tips & Tricks

There are three levels of safety notes used in this manual which are described below in brief by displaying a typical layout example.

Be sure to always read and follow the safety notes of a section first – before acting as documented in the other parts of the section.

Danger

Dangerous situation: injuries to people and severe damage to objects possible.

Caution

Possibly dangerous situation: no injuries to people but damage to objects possible.

Note: **No danger encountered. Pay attention to important information marked using this layout.**

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1 Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PENT/CPCI-731. For your protection, follow all warnings and instructions found in the following text.

General

This *Reference Guide* provides the necessary information to install and handle the PENT/CPCI-731. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. In case you need additional information, ask your Force Computers representative.

The PENT/CPCI-731 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, uninstall or maintain the PENT/CPCI-731. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Hot Swap

The PENT/CPCI-731 provides hot-swap support, i.e. it may be installed in or removed from a powered system supporting hot swap. Never install or uninstall the board in a system under hot-swap conditions unless the hot-swap or high-availability platform is used and the system documentation explicitly includes appropriate guidelines. For detailed information on the hot-swap support and the relevant safety notes, see “Hot Swap” on page 12. All of the following safety notes refer to the installation and uninstallation of the board in a non-powered system.

Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before installing or uninstalling the board, read section 3 “Installation” on page 9.**
- **Before touching integrated circuits, ensure that you are working in an ESD safe environment.**

- **Before installing or uninstalling the board in a CompactPCI rack:**
  - **– Check all installed boards for steps that have to be taken before turning off the power.**
  - **– Take those steps.**
  - **– Finally turn off the power.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**
- **Ensure that the board is connected to the CompactPCI backplane via all assembled connectors and that power is available on all power pins.**

CompactPCI

The PENT/CPCI-731 is a peripheral (or non host) board. Therefore:

- **Plug the PENT/CPCI-731 only into a peripheral slot of a CompactPCI system.**
- **Never plug the PENT/CPCI-731 into another slot of a CompactPCI system or into a system rack other than a CompactPCI system.**
- **Ensure that the board is connected to the CompactCI backplane via all its connectors, and that power is available on all power pins.**
- **When operating the board in areas of strong electro-magnetic radiation, ensure that the board is:**
  - **– Bolted on the CompactPCI rack**
  - **– Shielded by enclosure**

Hard Disk Limitation

If the PENT/CPCI-731/HD-AccKit is installed on the PENT/CPCI-731, the operating temperature and the shock and vibration values are limited by the hard disk environmental requirements. For details, refer to the Installation Guide of the PENT/CPCI-731/HD-AccKit.

Power Consumption

The total maximal power consumption per PMC slot at +/–12 V, 5 V, and 3.3 V level must not exceed 7.5 W (total over all used voltages).

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Operation

- **While operating the board ensure that the environmental and power requirements as given in table 4 “Environmental Requirements of the PENT/CPCI-731” on page 9 and table 5 “Typical 5 V and 3.3 V Power Requirements” on page 10 are met.**

EMC

- **If boards are integrated into open systems, always cover empty slots.**
- **The front panel of the PENT/CPCI-731 provides one cutout for a PMC module. If the board is shipped without the module installed, the front-panel cutout is covered by a blind panel to ensure proper EMC shielding. To ensure proper EMC shielding, always operate the PENT/CPCI-731 with the blind panel or with a PMC module installed.**

Expansion

- **Check the total power consumption of all components installed (see the technical specification of the respective components). For the total power consumption of the PENT/CPCI-731, see table 5 “Typical 5 V and 3.3 V Power Requirements” on page 10.**
- **Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).**
- **Only replace components or system parts with those recommended by Force Computers. In case you use components other than those recommended by Force Computers, you are fully responsible for the impact on EMC/Safety and the eventually changed functionality of the product.**

IOBP

The IOBP-CPCI-731 is especially designed for the base board of the PENT/CPCI-731. Do not use any other I/O panels on the PENT/CPCI-731.

Environment

Always dispose of used batteries and/or old boards according to your country’s legislation.

Battery

The board is designed to be maintenance-free. However, note that a Lithium battery is installed on the board. The battery provides a data retention of five years summing up all periods of actual battery use. Therefore, Force Computers assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare part handling.

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is already installed.**
- **If the battery is covered by a PMC module on slot 1 or a memory module, the module must be removed first.**
- **Use an appropriate tool to remove the battery from its holder to avoid possible damage to the PCB or the battery holder.**
- **When installing the new battery ensure that the '+' on top of the battery stays at the top and therefore is visible when viewing the board from its component side. If necessary reinstall the PMC or memory module in its correct position.**

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2 Introduction

The PENT/CPCI-731 is a 6U CompactPCI computer based on the Intel Pentium II/III CPU and is a CompactPCI non host or I/O board. It requires the space of one slot. All PENT/CPCI-731 PCI buses are 32-bit wide and operate at 33 MHz PCI bus frequency.

The PENT/CPCI-731 is designed to run with Windows NT Version 4.0. or higher, VxWorks and LynxOS.

2.1 Features and Products

The PENT/CPCI-731 features include:

- Mobile module based on Intel Pentium II/III CPU
- CompactPCI I/O slot functionality
- Inrush current protection and full hot swap support
- Two PMC slots for I/O extensions, both supporting the front panel I/O and I/O via CompactPCI connector
- Synchronous DRAM (SDRAM) with ECC support running at 66/100 MHz clock frequency
- 10/100 BaseT Ethernet available via CompactPCI connector (IOBP-CPCI-731)
- On-board 16 MByte IDE flash disk
- One MByte flash BIOS, 8-bit wide
- Two RS-232 serial interfaces with 115 KBaud maximum data rate and 16-byte deep FIFO
  - COM1 available on front-panel and CompactPCI connector J3
  - COM2 available on CompactPCI connector J3

- One IEEE 1284 compatible parallel interface LPT with ECP (Extended Capabilities Port) and EPP (1.7/1.9) support available at the CompactPCI connector
- Two USB interfaces, available at CompactPCI connector J3
- Floppy controller, compatible with PC8477 which contains a superset of NECuPD72065B and N82077, accessible via CompactPCI connector J4
- IDE controller with primary and secondary EIDE support, the primary IDE interface accessible via on-board connector, the primary and secondary via CompactPCI connector J4 and J5
- Motorola 146818 compatible real time clock and CMOS RAM for storing factory settings, both RTC and RAM with battery backup
- Two 82C37A compatible DMA controllers
- Two 82C29 compatible interrupt controllers
- 8254 compatible 3-channel timer
- PS/2 keyboard and mouse controller, 8042 compatible, available on front-panel and CompactPCI connector J5
- Software-controllable, scalable watchdog, which controls the CPU activity and causes a RESET or an NMI in case of malfunction
- Program-readable vintage registers for board information protocol (BIP)
- Additional front-panel features include:
  - RESET key which can be disabled via switch or software, the RESET signal is available on the CompactPCI connector.
  - Two LEDs for network link and activity, LED for signaling access to devices connected to IDE, latter both also user available for user applications
  - 2x PMC front-panel I/O

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Factory Options, Upgrades and Accessories

The PENT/CPCI-731 has been designed to cost-effectively support a wide range of hardware requirements. Therefore a number of factory options and accessory kits are available. These are the following:

- Intel Pentium II based mobile module with 266/333 MHz, Pentium III based mobile module with 500 MHz internal frequency
- On-board SDRAM capacity: up to 256 MByte
- On-board IDE flash disk and its capacity: 16 MByte
- On-board 2,5” IDE hard disk drive
- PMC VGA card
- Memory module: up to 512MByte capacity.

For a list of upgrades and accessories, see table 3 “Excerpt from the PENT/CPCI-731 Ordering Information” on page 8. The upgrades and accessories available depend on the variant of the PENT/CPCI-731 under consideration.

The following table gives an excerpt from the PENT/CPCI-731 specification:

Table 1 Specification of the PENT/CPCI-731

Additional Features	Optional on-board IDE flash disk, 16 MByte, PIO mode 1
Board Form Factor	6HE, 4TE
CompactPCI Interface	32 bit with 33 MHz, PCI Specification Rev. 2.1., 3.3/5 V level
EIDE	PIO mode 4 via rear I/O
Environmental conditions	See **table 4 “Environmental Requirements of the PENT/CPCI-731” on page 9**
Ethernet	Twisted-pair, 10/100 Mbit, according to IEEE802.3, via rear I/O
Firmware	Phoenix BIOS, see section 3.6 “BIOS” on page 19
Floppy DiskIinterface	PC-AT floppy, e.g. 360 KByte, 720 KByte, 1.2 MByte, 1.44 MByte, 2.88 MByte, via rear I/O
Inrush Current Protection	Protected/switched: +5 V, +3.3 V, switched: VIO, +12 V, -12 V
Keyboard/Mouse Port	PS/2 compatible
L2 Cache	512 KByte/256 KByte depending on Processor
Main Memory	Up to 768 MByte (depending on selected memory option) with ECC
Parallel I/O	IEEE 1284, ECP, EPP modes via rear I/O

Table 1 Specification of the PENT/CPCI-731 (cont.)

PMC Slots	2 for 32 bit with 33 MHz PMC modules, PCI Specification Rev. 2.1, 5 V and 3.3 V level (assembly option)
Power Consumption	See **table 5 "Typical 5 V and 3.3 V Power Requirements" on page 10**
Processor	Pentium II with 266/333 MHz or higher, Pentium III with 500 MHz
Serial I/O	2x, RS232 level, max. rate 115.2 KBaud
USB Port	2x, via rear I/O

Data Sheets

For a list of data sheets see the front matter of this manual.

Ordering Information

Due to the flexible design, the PENT/CPCI-731 is available in several variants as well as in several memory and speed options. Consult your local sales representative to confirm availability of specific combinations. The following table explains the general product nomenclature.

Table 2 Product Nomenclature

PENT/CPCI-731/*ddd-ppp*-L*ccc-u*			
ddd = MByte DRAM	*ppp* = Processor type	L*ccc* = 2nd level cache	*u* = MByte IDE flash disk
128 =128 MByte 256 =256 MByte	333 = Intel Pentium II 333 MHz	L512 = 256 KByte	16 = 16MByte

The following table is an excerpt from the PENT/CPCI-731 data sheet. For current information ask your local Force Computers representative.

Table 3 Excerpt from the PENT/CPCI-731 Ordering Information

Product Name	**Description**
PENT/CPCI-731/…	
…/128-266-L512-0	Intel Pentium II 266 MHz with 128MByte main memory, 512 KByte 2nd level cache, no flash disk
…/256-333-L256-16	Intel Pentium II 333 MHz with 256MByte main memory, 256 KByte 2nd level cache, 16 MByte flash disk

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3 Installation

Before installing or dismounting the board, refer to section 1 “Safety Notes” on page 1.

3.1 Installation Prerequisites and Requirements

Note: **Before powering up check the items described in the following list.**

- Check this section for installation prerequisites and requirements concerning the PENT/CPCI-731
- Check the consistency of the current switch settings (see section 3.2 “Switch Settings” on page 14)
- Check section 3.7 “Upgrades and Accessories” on page 29 for installation prerequisites and requirements concerning PENT/CPCI-731 accessories, like e.g. a PMC module

Caution

If the PENT/CPCI-731/HD-AccKit is installed on the PENT/CPCI-731, operating temperature, shock and vibration values are limited by the hard disk environmental requirements. For details, refer to the Installation Guide of the PENT/CPCI-731/HD-AccKit .

Table 4 Environmental Requirements of the PENT/CPCI-731

	Operating	**Non-operating**
Temperature	0°C to +55°C	–40°C to +85°C
Forced Air Flow (in LFM = Linear Feet per Minute)	300 LFM	–
Temperature Change	+/– 0.5°C/min	+/– 1°C/min
Relative Humidity	5% to 95% non-condensing at +40°C	5% to 95% non-condensing at +40°C
Altitude	–300 m to +3,000 m	–300 m to +13,000 m

Table 4 Environmental Requirements of the PENT/CPCI-731 (cont.)

	Operating	Non-operating
Vibration **10 to 15 Hz** **15 to 150 Hz**	 2 mm amplitude 2 g	 5 mm amplitude 5 g
Shock	5 g/11 ms halfsine	15 g/11 ms halfsine
Free Fall	100 mm/3 axis	1,200 mm/all edges and corners (packed state)

These environmental values must be tested and proven in the used system configuration. These conditions refer to the surroundings of the board within the user environment. Operating temperatures refer to the temperature of the air circulating around the board and not to the actual component temperature. To ensure that the operating conditions are met, forced air cooling is required within the chassis environment.

Power Requirements

The board's +/– 12 V power requirements depend on the PMC modules installed. The PENT/CPCI-731 provides a limited current at the PMC supply pins.

Caution

The total maximal power consumption per PMC slot at +/–12 V, 5 V, and 3.3 V level must not exceed 7.5 W (total over-all used voltages).

Typical 5 V and 3.3 V power requirements of the PENT/CPCI-731 are given in the following table:

Table 5 Typical 5 V and 3.3 V Power Requirements

PENT/CPCI-731 (no Memory Board, PMC Module Installed)	+5 V	+3.3 V
PENT/CPCI-731/256-333-L256-16	1.8 A	1.7 A

Keyboard, Mouse, USB

Make sure that the lengths of the keyboard/mouse cable and of the USB cable do not exceed 3m each and that the two cables are installed apart from other cables.

Floppy Disk Connector

The floppy disk connector is assembled to provide BIOS field upgrade ability of the PENT/CPCI-731 if no IOBP-CPCI-731 is available.

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IDE Devices

The PENT/CPCI-731 provides a primary and a secondary IDE interface for connecting up to four IDE devices. An on-board flash disk may be provided at the primary IDE interface as a factory option (see below). A hard disk can be connected to the primary IDE port via the on-board connector using the PENT/CPCI-731/HD-AccKit. If two devices are connected to an IDE interface, one device has to be the master, the other has to be the slave. If only one drive is connected to an IDE interface, that device must be set as master.

Due to the nature of IDE some further limitations apply:

- There can be up to three connectors on each ribbon cable connected to the primary or secondary PENT/CPCI-731 IDE interface. Thereby, up to two IDE devices per ribbon cable can be connected to a PENT/CPCI-731 IDE interface.
- Never connect more than two devices to the primary or secondary PENT/CPCI-731 IDE interface.
- Before connecting IDE devices to an IDE interface, do the following:
  - Check for IDE devices already connected to the IDE interface.
  - Decide which IDE device should be master and which should be slave. If only one IDE device is connected to an IDE interface, this device must be master.
  - Configure the device which you want to connect.
  - Ribbon cable length must not exceed 0.45 m (18 inches).

At the first boot after connecting an IDE device use the according menu in Setup to modify the BIOS parameters appropriately (see section 3.6.1 “Booting Up and Entering Configuration Utilities (e.g. BIOS Setup)” on page 21 <F2>).

If the PENT/CPCI-731 is provided without on-board flash disk, up to four hard disks can be connected to the PENT/CPCI-731 via the IOBP-CPCI-731 and on-board connector.

IDE Flash Disk (Factory Option)

If the PENT/CPCI-731 is provided with an on-board flash disk connected to its primary IDE interface, a hard disk can be connected as second device to the primary IDE interface. This can be done by either assembling the PENT/CPCI-731/HD-AccKit or via an IOBP-CPCI-731 board. The flash disk can be enabled or disabled via switch SW1-3 (see “Switch Settings” on page 14).
If the flash disk is enabled and a second device is connected to the primary IDE interface, any of the two devices can be the master while the other is the slave. The flash disk is set to master or slave mode via switch SW1-4. If the flash disk is disabled, the second device at the primary IDE interface must be the master.

For the IDE flash disk a data endurance of 300,000 erase/program cycles per logical sector is guaranteed.

EMC

The PENT/CPCI-731 front panel provides two cutouts to enable the installation of PMC modules. If the PENT/CPCI-731 is shipped without modules installed, the front-panel cutouts are covered by blind panels to ensure proper EMC shielding.

Note: **To ensure proper EMC shielding, check the items described in the following list.**

- Always operate a PENT/CPCI-731:
  - With the blind panels for the PENT/CPCI-731 front panel installed
  - With the modules installed
- If the PENT/CPCI-731 is upgraded with PMC modules, ensure that the blind panels are stored in a safe place to be used again when uninstalling the upgrades.

Hot Swap

The PENT/CPCI-731 provides full Hot Swap functionality. This, however, does only cover the CPCI interface of connector J1 and J2. If I/O devices are used at the connectors J3, J4 and J5 (e.g. via IOBP-CPCI-731), refer to the respective documentation of these signals and interfaces for hot swap capability.

Location Overview

Figure 1 highlights the location of the important base board components.

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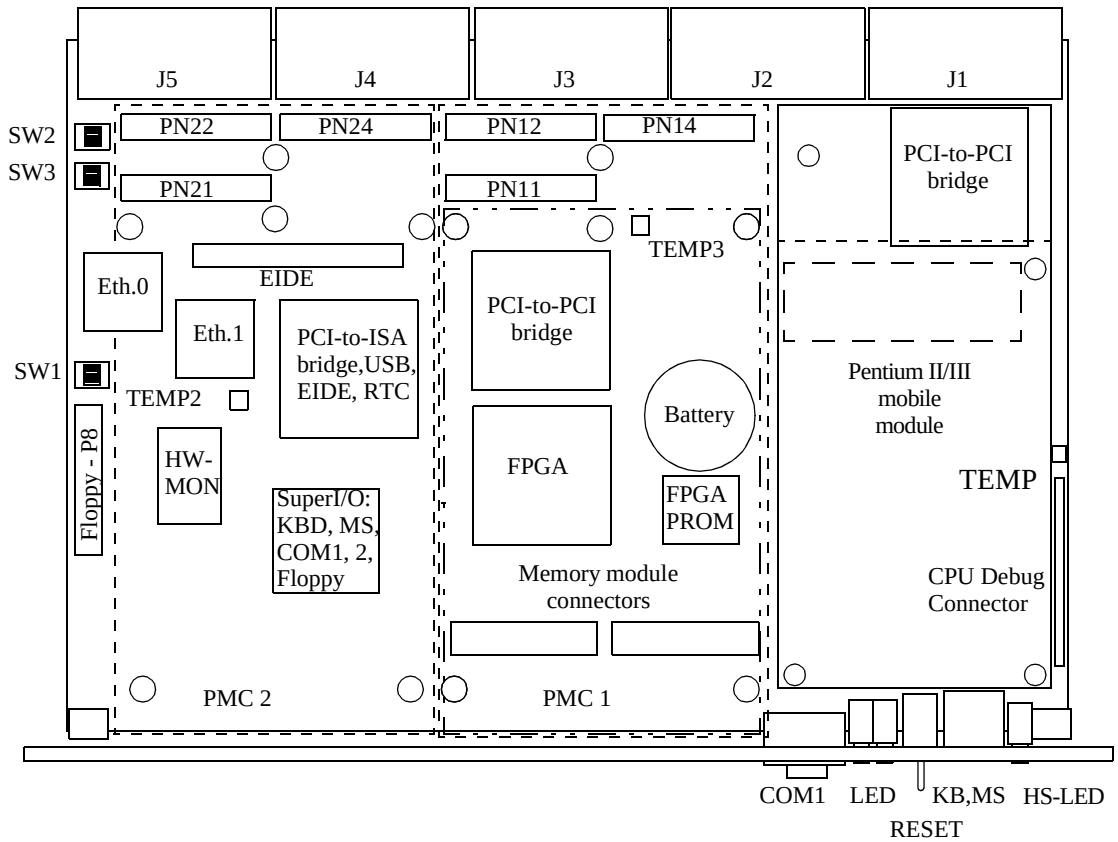
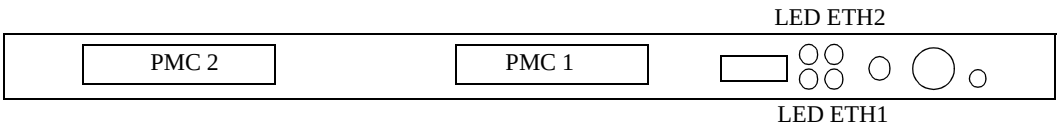
Figure 1 Location Diagram of the PENT/CPCI-731 (Schematic)

Top



Front panel



3.2 Switch Settings

The PENT/CPCI-731 is configurable via three micro switches. The switches are located on the left-hand side of the base board seen from the front panel (see “Location Diagram of the PENT/CPCI-731 (Schematic)” on page 13).

Table 6 PENT/CPCI-731 Switch Settings

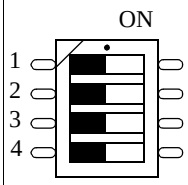
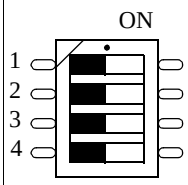
Name and Default Setting		Description
	SW1-1 OFF	I2C USER EEPROM write protection OFF = Write protected ON = Write enabled
	SW1-2 OFF	Boot Block write protection OFF = Write enabled ON = Write protected
	SW1-3 OFF	Flash disk enable (see “IDE Flash Disk (Factory Option)” on page 11) = Flash disk disabled ON = Flash disk enabled
	SW1-4 OFF	Flash Disk Master/Slave (boot enable) OFF = Primary IDE slave ON = Primary IDE master
	SW2-1 OFF	FPGA Download source OFF = via EEPROM ON = via Download Cable
	SW2-2 OFF	FPGA Init Select OFF = Lower 64KB ON = Upper 64KB
	SW2-3 ON	12V Supervising OFF = Enabled ON = Disabled
	SW2-4 OFF	Reset Key OFF = Enabled ON = Disabled

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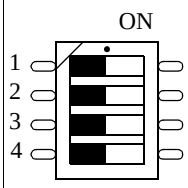
Table 6 PENT/CPCI-731 Switch Settings (cont.)

Name and Default Setting		Description
	SW3-1 OFF	FPGA Spare Switch
	SW3-2 OFF	FPGA Spare Switch
	SW3-3 OFF	FPGA Spare Switch
	SW3-4 OFF	FPGA Spare Switch

3.3 Front-Panel Keys and LEDs

The following front-panel keys and LEDs are provided on the PENT/CPCI-731:

– RESET Key — Mechanical reset key: When enabled via switch SW2-4 (see “Switch Settings” on page 14) and toggled, it instantaneously affects the system board by generating a reset. The reset behavior of the board (reset source, destructive-, non destructive reset) is fully configurable via registers (refer to “Reset and Watchdog” on page 45 for details). A reset is performed when the RESET key is pushed to the active position. RESET is held active until the key is back in the inactive position. For information on how to disable the key, see “Switch Settings” on page 14.

– LED 1,2 — Per default the U1 signals Board Power and U2 signals IDE activity. These LEDs are fully software programmable by means of a register. Possible LED status: Green, red, or off.

– LED ETH1 — Ethernet 1 active, link LED: signals status of Ethernet Interface 1. Possible LED status:

- LED is illuminated when properly connected to an Ethernet Network.
- LED flashes during network access.

– LED ETH2 — Ethernet 2 active, link LED: signals status of ethernet interface 2. Possible LED status:

- LED is illuminated when properly connected to an Ethernet Network.
- LED flashes during network access.

3.4 Front Panel Connectors

In addition to its CompactPCI interface (see section 3.5 “CompactPCI Interface” on page 16) the PENT/CPCI-731 provides one keyboard or mouse connector and one serial interface connector. The following figures show the pinouts.

Figure 2 KBD/MS **– Keyboard and Mouse Connector Pinout**

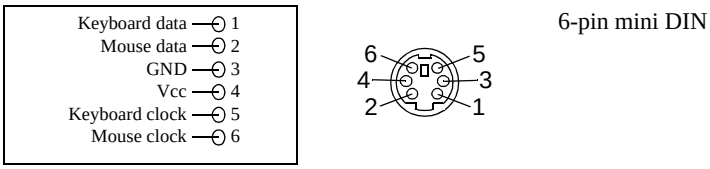
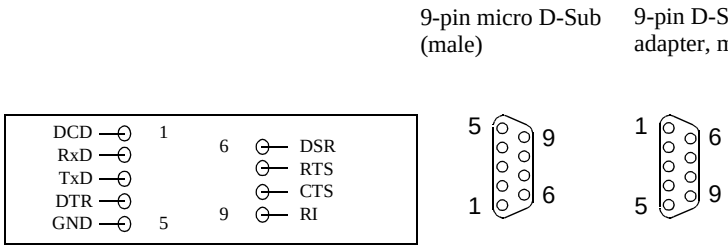


Figure 3 COM1 **Connector Pinout**



3.5 CompactPCI Interface

The PENT/CPCI-731 is a CompactPCI system peripheral board. The PCI bus supports a 32-bit data bus width with a frequency of 33 MHz.

The interfaces available on the CompactPCI interface can be routed to interface-dependent standard connectors via the IOBP-CPCI-731 (see page 19).

Signaling Level

Due to the hot swap capability and compliance to the CompactPCI Hot Swap Specification 2.1, the PENT/CPCI-731 board can only be used in a 5V system. A 5V key within the CPCI P1 Connector prevents the board from being installed in a non 5V System.

Hot Swap

The PENT/CPCI-731 provides full hot swap functionality signals of the CPCI connectors J1 and J2. If I/O devices are used at the connectors J3, J4 and J5 (e.g. via IOBP-CPCI-731), refer to the respective documentation for hot swap capability.

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J1 and J2

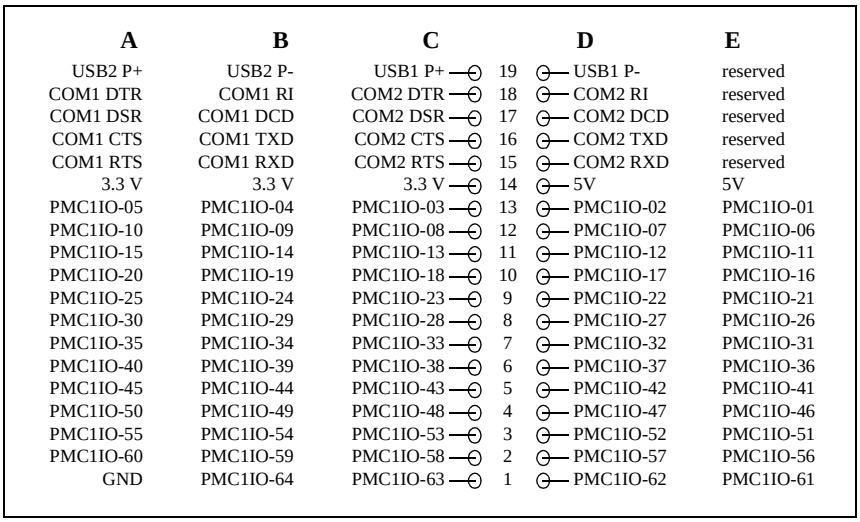
The J1 and J2 connectors implement the CompactPCI 64-bit connector pinout as specified by the CompactPCI specification. Therefore, this manual only documents the pinout of the J3, J4 and J5 connectors.

J3

The following interfaces are available via the PENT/CPCI-731 CompactPCI J3 connector (the designations used in the following pinout are given in brackets):

- USB 1 (`USB1`), USB 2 (`USB2`), COM 1 (`COM1`), COM 2 (`COM2`)
- PMC Slot 1 I/O signals (`PMC1IO`)

Figure 4 CompactPCI J3 Connector Pinout



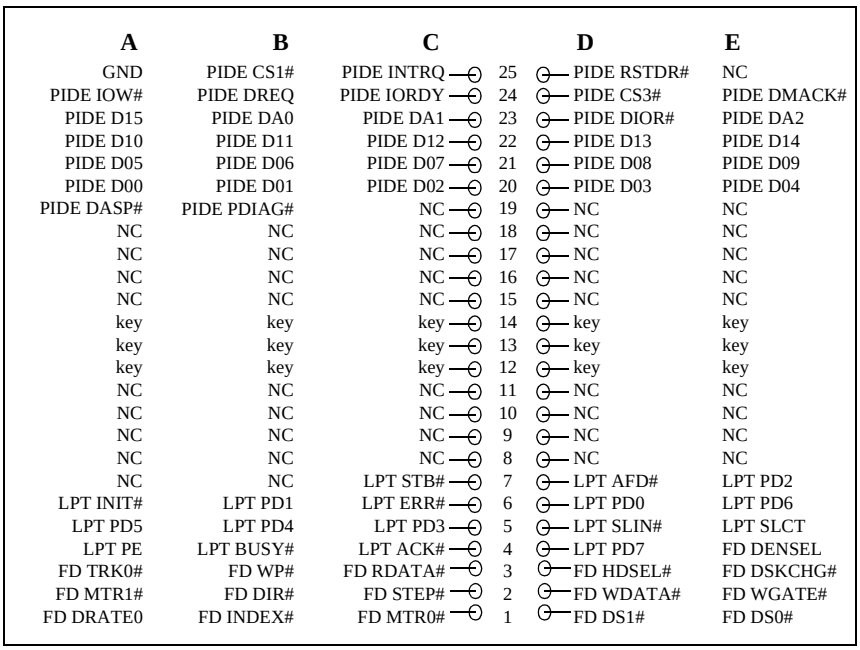
A	B	C		D	E
USB2 P+	USB2 P-	USB1 P+	19	USB1 P-	reserved
COM1 DTR	COM1 RI	COM2 DTR	18	COM2 RI	reserved
COM1 DSR	COM1 DCD	COM2 DSR	17	COM2 DCD	reserved
COM1 CTS	COM1 TXD	COM2 CTS	16	COM2 TXD	reserved
COM1 RTS	COM1 RXD	COM2 RTS	15	COM2 RXD	reserved
3.3 V	3.3 V	3.3 V	14	5V	5V
PMC1IO-05	PMC1IO-04	PMC1IO-03	13	PMC1IO-02	PMC1IO-01
PMC1IO-10	PMC1IO-09	PMC1IO-08	12	PMC1IO-07	PMC1IO-06
PMC1IO-15	PMC1IO-14	PMC1IO-13	11	PMC1IO-12	PMC1IO-11
PMC1IO-20	PMC1IO-19	PMC1IO-18	10	PMC1IO-17	PMC1IO-16
PMC1IO-25	PMC1IO-24	PMC1IO-23	9	PMC1IO-22	PMC1IO-21
PMC1IO-30	PMC1IO-29	PMC1IO-28	8	PMC1IO-27	PMC1IO-26
PMC1IO-35	PMC1IO-34	PMC1IO-33	7	PMC1IO-32	PMC1IO-31
PMC1IO-40	PMC1IO-39	PMC1IO-38	6	PMC1IO-37	PMC1IO-36
PMC1IO-45	PMC1IO-44	PMC1IO-43	5	PMC1IO-42	PMC1IO-41
PMC1IO-50	PMC1IO-49	PMC1IO-48	4	PMC1IO-47	PMC1IO-46
PMC1IO-55	PMC1IO-54	PMC1IO-53	3	PMC1IO-52	PMC1IO-51
PMC1IO-60	PMC1IO-59	PMC1IO-58	2	PMC1IO-57	PMC1IO-56
GND	PMC1IO-64	PMC1IO-63	1	PMC1IO-62	PMC1IO-61

J4

The following interfaces are available via the PENT/CPCI-731 CompactPCI J4 connector (the designations used in the following pinout are given in brackets):

- Primary IDE (`PIDE`)
- LPT (`LPT`), Floppy Disk (`FD`)

Figure 5 CompactPCI J4 Connector Pinout



A	B	C		D	E
GND	PIDE CS1#	PIDE INTRQ	25	PIDE RSTDR#	NC
PIDE IOW#	PIDE DREQ	PIDE IORDY	24	PIDE CS3#	PIDE DMACK#
PIDE D15	PIDE DA0	PIDE DA1	23	PIDE DIOR#	PIDE DA2
PIDE D10	PIDE D11	PIDE D12	22	PIDE D13	PIDE D14
PIDE D05	PIDE D06	PIDE D07	21	PIDE D08	PIDE D09
PIDE D00	PIDE D01	PIDE D02	20	PIDE D03	PIDE D04
PIDE DASP#	PIDE PDIAG#	NC	19	NC	NC
NC	NC	NC	18	NC	NC
NC	NC	NC	17	NC	NC
NC	NC	NC	16	NC	NC
NC	NC	NC	15	NC	NC
key	key	key	14	key	key
key	key	key	13	key	key
key	key	key	12	key	key
NC	NC	NC	11	NC	NC
NC	NC	NC	10	NC	NC
NC	NC	NC	9	NC	NC
NC	NC	NC	8	NC	NC
NC	NC	LPT STB#	7	LPT AFD#	LPT PD2
LPT INIT#	LPT PD1	LPT ERR#	6	LPT PD0	LPT PD6
LPT PD5	LPT PD4	LPT PD3	5	LPT SLIN#	LPT SLCT
LPT PE	LPT BUSY#	LPT ACK#	4	LPT PD7	FD DENSEL
FD TRK0#	FD WP#	FD RDATA#	3	FD HDSEL#	FD DSKCHG#
FD MTR1#	FD DIR#	FD STEP#	2	FD WDATA#	FD WGATE#
FD DRATE0	FD INDEX#	FD MTR0#	1	FD DS1#	FD DS0#

J5

The following interfaces are available via the PENT/CPCI-731 CompactPCI J5 connector (the name used in the following pinout is given in brackets):

- Secondary IDE (`SIDE`)
- Keyboard (`KBD`), PS2 mouse (`MS`)
- Ethernet 1 (`ETH1`)
- Ethernet 2 (`ETH2`)
- PMC Slot 2 I/O signals (`PMC2IO`)

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Figure 6 **CompactPCI J5 Connector Pinout**

A	B	C		D	E
ETH1 TX +	ETH1 RX +	KBD DAT	22	SIDE INTR	SIDE RSTDR#
ETH1 TX -	ETH1 RX -	KBD CLK	21	SIDE DACK#	SIDE CS1#
GND	AUXVCC	RESET IN	20	SIDE IORDY	SIDE CS3#
ETH2 TX +	ETH2 RX +	MS DAT	19	SIDE IOW#	SIDE DREQ
ETH2 TX -	ETH2 RX -	MS CLK	18	SIDE IOR#	SIDE A2
GND	AUXVCC	SIDE D15	17	SIDE A0	SIDE A1
SIDE D10	SIDE D11	SIDE D12	16	SIDE D13	SIDE D14
SIDE D05	SIDE D06	SIDE D07	15	SIDE D08	SIDE D09
SIDE D00	SIDE D01	SIDE D02	14	SIDE D03	SIDE D04
PMC2IO-05	PMC2IO-04	PMC2IO-03	13	PMC2IO-02	PMC2IO-01
PMC2IO-10	PMC2IO-09	PMC2IO-08	12	PMC2IO-07	PMC2IO-06
PMC2IO-15	PMC2IO-14	PMC2IO-13	11	PMC2IO-12	PMC2IO-11
PMC2IO-20	PMC2IO-19	PMC2IO-18	10	PMC2IO-17	PMC2IO-16
PMC2IO-25	PMC2IO-24	PMC2IO-23	9	PMC2IO-22	PMC2IO-21
PMC2IO-30	PMC2IO-29	PMC2IO-28	8	PMC2IO-27	PMC2IO-26
PMC2IO-35	PMC2IO-34	PMC2IO-33	7	PMC2IO-32	PMC2IO-31
PMC2IO-40	PMC2IO-39	PMC2IO-38	6	PMC2IO-37	PMC2IO-36
PMC2IO-45	PMC2IO-44	PMC2IO-43	5	PMC2IO-42	PMC2IO-41
PMC2IO-50	PMC2IO-49	PMC2IO-48	4	PMC2IO-47	PMC2IO-46
PMC2IO-55	PMC2IO-54	PMC2IO-53	3	PMC2IO-52	PMC2IO-51
PMC2IO-60	PMC2IO-59	PMC2IO-58	2	PMC2IO-57	PMC2IO-56
TM_PRNT	PMC2IO-64	PMC2IO-63	1	PMC2IO-62	PMC2IO-61

IOBP-CPCI-731

The IOBP-CPCI-731 I/O panel is available as separate price list item for the PENT/CPCI-731. The I/O panel supports the following interfaces:

- Two Ethernet interfaces
- Keyboard
- Mouse
- Two USB interfaces
- Two serial interfaces
- Two parallel interfaces
- IDE interfaces (primary and secondary)
- Floppy interface

Caution

The IOBP-CPCI-731 is especially designed for the base board of the PENT/CPCI-731. Do not use any other I/O panels on the PENT/CPCI-731.

3.6 BIOS

The PENT/CPCI-731 is designed to run with Windows NT Version 4.0 in host mode. The initial boot-up procedure is performed by BIOS which provides the following features:

- Year 2000 support
- Upgradable via software utility
- PCI 2.1 compliant
- Plug-and-Play BIOS Specification Version 1.0A compliant (PnP)
- Flexible booting via Multiboot
- Advanced power management
- Two-level password control provided by system security
- Hardware setup via setup program:
  - For information on general system configuration via the system BIOS, see section 3.6.1 “Booting Up and Entering Configuration Utilities (e.g. BIOS Setup)” on page 21. Detailed on-line help is available for the system BIOS setup.
  - For information on option ROMs which may be implemented on other boards in the CompactPCI rack, see the respective board documentation.

  Using the setup program BIOS allocates and optimizes resources (memory, interrupts, etc.) for each of the hardware components (video, disk drives, etc.).
- Hardware initialization at boot: At power-on or reset, BIOS performs Power-On Self Test (POST) routines to test system resources. Afterwards it loads and starts the operating system.

  The POST performs the following tasks:
  - Run basic and limited RAM test
  - Conduct an inventory of the devices installed on the system board
  - Configure hard and floppy disks, keyboard, VGA, serial or parallel ports
  - Configure other devices installed on the system board, e.g. CD-ROM drives
  - Initialize hardware required for system board features such as plug-and-play and power management
  - Run Setup if requested

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3.6.1 Booting Up and Entering Configuration Utilities (e.g. BIOS Setup)

BIOS automatically starts during power up or reset:

<Esc> When pressing <Esc> BIOS continues with the POST screen until the end of POST. It then displays a boot selection menu.
For further information, see section 3.6.2 “The Boot Selection Menu” on page 22.

<F2> When pressing <F2> BIOS enters Setup.
BIOS provides the Setup program to configure the setting of a wide range of system board features. For example:

- `LPT`, `COM1` and `COM2` can be remapped via the advanced configuration option for integrated peripherals in BIOS Setup.
- The IDE devices can be configured via the main configuration options for primary and secondary IDE masters and slaves and via the advanced configuration option for integrated peripherals. This configuration capability is used for example at the first boot after connecting an IDE device.
- The floppy type can be configured via the respective main configuration options for diskettes. This configuration capability is used for example at the first boot after installing a floppy via the respective I/O panel (see note on the IOBP-CPCI-731 on page 19).

Note: **If you save the changes you made in Setup, the selections in the menus are stored in NVRAM (CMOS). The next time the system board boots, the BIOS configures the system according to the Setup selections stored in NVRAM (CMOS). If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the default values or try to change the selections that caused the boot to fail. If you get the default values, note that the displayed default values are not yet stored to be effective for the next boot. They are just loaded to be displayed. However, they are effective when the current boot-up procedure is resumed.**

Input Requests If the BIOS or an Option ROM (e.g. of an add-on card) requests keyboard input, you are prompted for entering the information. POST continues from there with the regular POST screen.

POST Error Whenever POST detects a non-fatal error, BIOS displays a message asking you to choose between boot continuation or error correction via Setup.

3.6.2 The Boot Selection Menu

The boot selection menu is used to rearrange the boot-order list or to enter Setup.

1. In order to override the existing boot sequence (for this boot only) select another boot device from the boot-order list.

   If the specified device does not load the operating system, BIOS reverts to the previous boot sequence.

2. In order to boot via the boot configuration options in Setup, enter Setup and change the device as described in the following section.

3. In order to continue with the previous boot sequence, press <Esc>.

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3.6.3 Boot Configuration in Setup

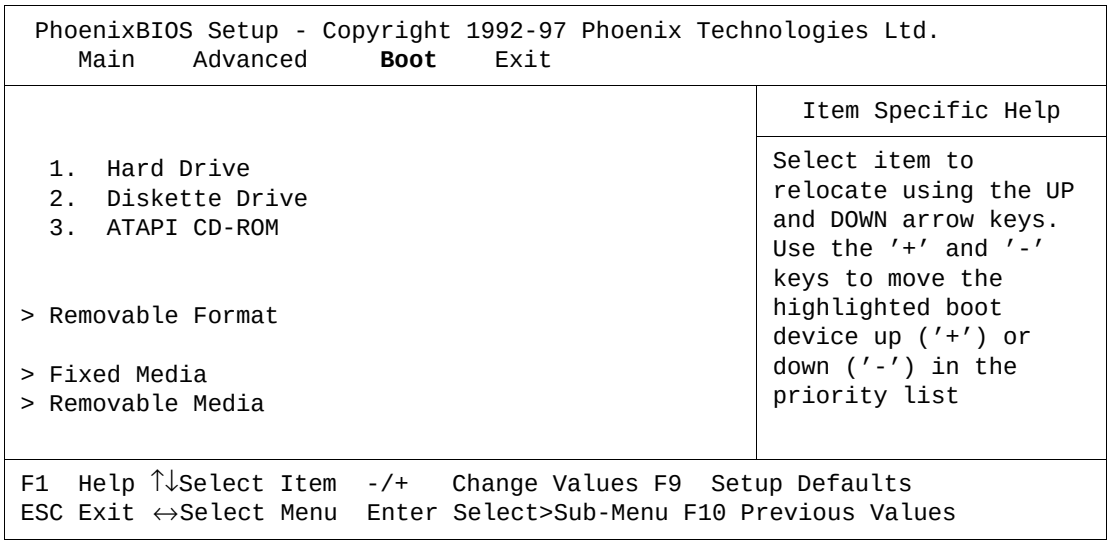
The order of the devices from which BIOS attempts to boot the operating system can be selected by the boot configuration options in Setup. During POST, BIOS tries the next one on the list if it is unsuccessful at booting from one device.

Each device listed represents the first of a group of devices if more than one device of this group is installed on the system. For example, if there is more than one hard disk drive, the displayed entry represents the first of such drives as specified in the boot configuration option for fixed media. The same applies to removable media.

The same options determine the order in which POST installs the devices and the operating system assigns device letters. BIOS supports up to two floppy devices, to which the operating system may assign, for example, drive letters A: and B:. C:, D:, E:, etc. are assigned to hard-disk drives.

Note: **There is not always an exact correspondence between the order specified in these menus and the letters assigned by the operating system. Many devices such as legacy Option ROMs support more than one device, to which can be assigned more than one letter. If you want the CD-ROM drive to have a letter coming before the hard drive, move it in front of the hard drive. The group of bootable add-in cards refers to devices with non-multiboot-compliant BIOS Option ROM from which you can boot the operating system.**

Figure 7 A Sample Setup Screen Showing the Boot Configuration Options



In the example above BIOS first attempts to boot in the following order:

1. `Hard Drive` - from hard disk
2. `Diskette Drive` - from floppy disk
3. `ATAPI CD-ROM` - from CD-ROM.

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3.6.4 Sample Start-up

The following figure shows a sample start-up message following the video BIOS message which displays the graphic card type and the video RAM size.

Figure 8 Sample Start-up Screen

```
PhoenixPICO BIOS Version 4.xx
Copyright 1985-1997 Phoenix Technologies Ltd., All Rights Reserved

FORCE COMPUTERS- CPCI-731 BIOS Revision 1.0

08/07/97 09:44:57
CPU = Intel(R) Mobile PentiumII processor 333 MHz
0000640K System RAM Passed
0255M Extended RAM Passed
0256K Cache SRAM Passed
System BIOS shadowed
Video BIOS shadowed
UMB upper limit segment address: F4B2
Fixed Disk 0: SunDisk SDP3B-16
ATAPI CD-ROM: TOSHIBA CD_ROM XM-5702B




Press <F2> to enter SETUP
```

Problems

The NVRAM (CMOS) values may have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in NVRAM (CMOS). BIOS detects such problems by verifying a so-called `System CMOS Checksum`.

If, during boot-up, BIOS detects a problem in the integrity of values stored in NVRAM (CMOS), it displays a message asking you to choose between boot continuation or entering Setup with the ROM default values already loaded into the menus.

Note: **After entering Setup with the ROM default values already loaded into the menus, it might be possible to restore some values as saved in NVRAM (CMOS) via the exit configuration option to load previous values. However, you should then try to fix the erroneous values which are causing BIOS problems.**

3.6.5 BIOS Messages

Note: **If your system fails after you made changes in the Setup menus, you may be able to correct the problem by entering Setup and restoring the original values. If your system displays one of the following messages, write down the message and contact Force Computers.**

- Extended RAM Failed at offset: nnnn
- Failing Bits: nnnn
- Keyboard controller error
- Parity Check 1 nnnn
- Parity Check 2 nnnn
- Real time clock error
- Shadow Ram Failed at offset: nnnn
- System cache error - Cache disabled
- System RAM Failed at offset: nnnn
- System timer error

Message Explanations

nnnn `Cache SRAM Passed`
nnnn is the amount of system cache in KBytes successfully tested.

`CD-ROM Drive Identified`
Autotyping identified CD-ROM Drive

`Diskette drive A error`
`Diskette drive B error`
Drive A: or B: is present but fails the BIOS POST diskette tests. Check to see that the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.

`Entering SETUP ...`
Starting Setup program.

`Extended RAM Failed at offset:` *nnnn*
Extended memory not working or not configured properly at offset *nnnn*.

nnnn `Extended RAM Passed`
nnnn being the amount of RAM in KBytes successfully tested.

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`Failing Bits: nnnn`
The hex number *nnnn* is a map of the bits at the RAM address (in system, extended, or shadow memory) which failed the memory test. Each `1` (one) in the map indicates a failed bit.

`Fixed Disk 0 Failure`
`Fixed Disk 1 Failure`
`Fixed Disk Controller Failure`
Fixed disk is not working or not configured properly. Check to see if fixed disk is attached properly. Run Setup to be sure the fixed-disk type is correctly identified.

`Fixed Disk 0...3 Identified`
Autotyping identified specified fixed disk.

`Incorrect Drive A type - run SETUP`
`Incorrect Drive B type - run SETUP`
Type of floppy drive not correctly identified in Setup.

`Invalid NVRAM media type`
Problem with NVRAM (CMOS) access.

`Keyboard controller error`
The keyboard controller failed test. You may have to replace the keyboard.

`Keyboard error`
Keyboard not working.

`Keyboard error nn`
BIOS discovered a stuck key and displays the scan code *nn* for the stuck key.

`Keyboard locked - Unlock key switch`
Unlock the system to proceed.

`Monitor type does not match CMOS - Run SETUP`
Monitor type not correctly identified in Setup.

`Operating system not found`
Operating system cannot be located on either drive A: or drive C:. Enter Setup and see if fixed disk and drive A: are properly identified.

`Parity Check 1 nnnn`
Parity error found in the system bus. BIOS attempts to locate the address *nnnn* and display it on the screen. If it cannot locate the address, it displays ????.

`Parity Check 2 nnnn`
Parity error found in the I/O bus. BIOS attempts to locate the address *nnnn* and display it on the screen. If it cannot locate the address, it displays ????.

`Press <F1> to resume, <F2> to Setup`
Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.

`Previous boot incomplete - Default configuration used`
Previous POST did not complete successfully. POST loads default values and offers to run Setup. If the failure was caused by incorrect values and they are not corrected, the next boot is likely to fail. On systems with control of wait states, improper Setup settings can also terminate POST and cause this error on the next boot. Run Setup and verify that the wait-state configuration is correct. This error is cleared the next time the system is booted.

`Real time clock error`
Real-time clock fails BIOS test. May require board repair.

`Resource allocation conflict on motherboard - Run Configuration Utility`
Run ISA or EISA Configuration Utility to resolve resource conflict.

`Shadow Ram Failed at offset:` *nnnn*
Shadow RAM failed at offset *nnnn* of the 64k block at which the error was detected.

nnnn `Shadow RAM Passed`
nnnn being the amount of shadow RAM in KBytes successfully tested.

`System BIOS shadowed`
System BIOS copied to shadow RAM.

`System cache error - Cache disabled`
RAM cache failed the BIOS test. BIOS disabled the cache.

`System CMOS checksum bad - run SETUP`
System NVRAM (CMOS) has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in NVRAM (CMOS). Run Setup and reconfigure the system either by getting the Default Values and/or making your own selections.

`System RAM Failed at offset:` *nnnn*
System RAM failed at offset *nnnn* in the 64k block at which the error was detected.

nnnn `System RAM Passed`
Where *nnnn* is the amount of system RAM in KBytes successfully tested.

`System timer error`
The timer test failed. Requires repair of system board.

`UMB upper limit segment address:` *nnnn*
Displays the address *nnnn* of the upper limit of upper memory blocks, indicating released segments of the BIOS which may be reclaimed by a virtual memory manager.

`Video BIOS shadowed`
Video BIOS successfully copied to shadow RAM.

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`Invalid System Configuration Data – run configuration utility`

Enter Setup and use the advanced configuration option to reset the configuration data (due to corrupted ESCD data).

3.7 Upgrades and Accessories

Apart from the extensions which are possible via the CompactPCI system, the PENT/CPCI-731 itself allows for an easy and cost-efficient way to adapt the board to the application's needs.

PMC Slot 1 — The PMC slot 1 can be used to install a standard PMC module with front-panel I/O and rear I/O onto the PENT/CPCI-731. The memory module option can only be installed on this location if no PMC is required on this slot. For further information, see section 3.7.1 "Installing a PMC Module" on page 31.

PMC Slot 2 — The PMC slot 2 can be used to install a standard PMC module with front-panel I/O and rear I/O onto the PENT/CPCI-731. A 2.5'' hard drive may be installed at the location of PMC slot 2 instead of a PMC Module. For further information, see section 3.7.1 "Installing a PMC Module" on page 31.

Memory Module — In addition to the local SDRAM of the PENT/CPCI-731 the memory module PENT/MEM-700 with SDRAM chips can be installed on the PENT/CPCI-731. The maximum possible memory size of the memory module is 512 MByte. This allows a maximum possible system memory of 768 MByte in total. For installation information, refer to the Installation Guide delivered together with the memory module.

HD-AccKit — The IDE hard disk accessory kit PENT/CPCI-731/HD-AccKit can be installed on PMC slot 2 of the PENT/CPCI-731 providing a local mass storage device. For installation information refer to the Installation Guide delivered together with the accessory kit.

IOBP-CPCI-731 — The IOBP-CPCI-731 provides access to the base board's CompactPCI user I/O interfaces via industry standard connectors. It is included in the rear I/O panel accessory kit for PENT/CPCI-731 base boards, containing the I/O panel itself and the cables.

VGA-AccKit — The VGA accessory kit PMC/VGA is a PMC based VGA card. It can be installed in one of the PMC slots of the PENT/CPCI-731.
For installation information refer to the Installation Guide delivered together with the VGA accessory kit.

BIOS-UpKit

The BIOS upgrade kit PENT/CPCI-731/BIOS-UpKit contains a DOS-formatted floppy disk with a BIOS upgrade file and upgrade utilities e.g. to reflect extended hardware support. For installation information refer to the `README` file contained on the floppy disk.

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3.7.1 Installing a PMC Module

The PENT/CPCI-731 provides two PMC slots. Both slots consist of three connectors identified as PNxx (see "Mounting Points for PMC Modules on the PENT/CPCI-731" on page 32) and support a 32-bit data bus width with a maximum frequency of 33 MHz. +/–12V are available at the PMC slots.

Note: **Slot 1 is only available if no memory module is installed and Slot 2 is only available if no hard drive is assembled.**

PMC Voltage Keys

The PCI bus uses a 5V or 3.3V voltage signal level on the PMC slots (factory option). The appropriate voltage keys prevent 3.3V PMC cards, or respective 5V PMC cards, from being plugged into the PMC slots.

Connector Configuration

The 32-bit PCI bus requires two PMC connectors. The third PMC connector connects additional user I/O signals of PMC slot 1 and 2 with the CompactPCI J3 and J5 connector.

Installation

In order to install a PMC module on a PMC slot, proceed as follows:

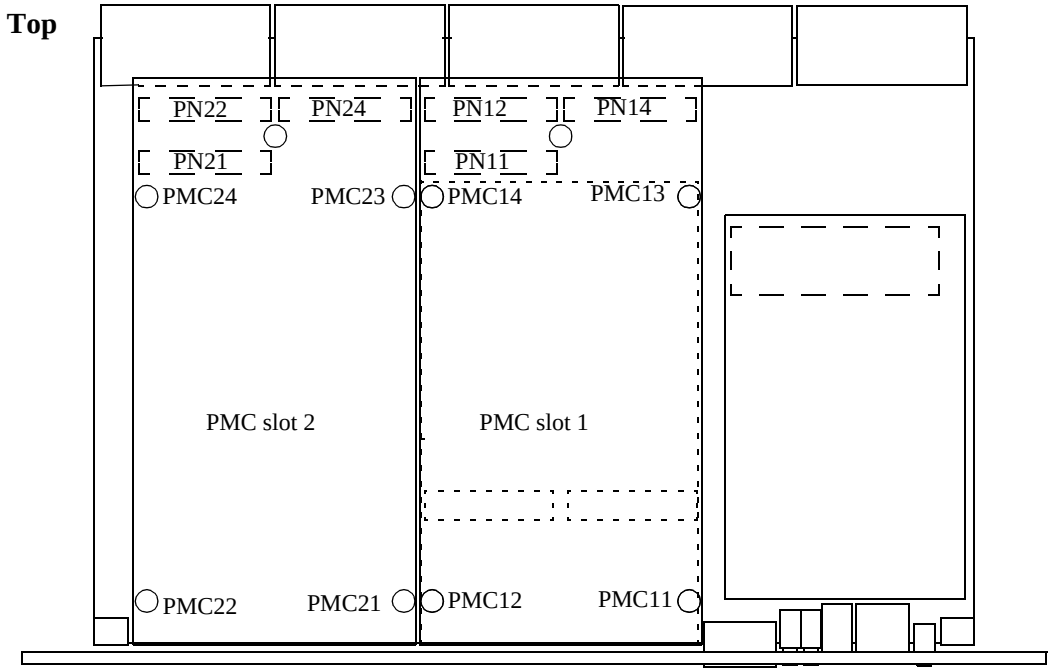
1. If PMC slot 1 is intended to be used, the memory module option cannot be used. If the space for PMC slot 1 is occupied by a memory module the memory module must be removed first.

   If PMC slot 2 is intended to be used, the on-board hard drive option cannot be used. If the space of PMC slot 2 is occupied by a hard drive the hard drive must be removed first.

2. Plug the PMC module on the connectors PN11, PN12 and PN14 for PMC slot 1 or PN21, PN22, and PN24 for PMC slot 2, so that the stand-offs of the module fit on the mounting holes PMC11…PMC14 or PMC21…PMC24 (see figure 9 "Mounting Points for PMC Modules on the PENT/CPCI-731" on page 32).

3. Fasten the PMC module onto the PENT/CPCI-731 with the four screws delivered together with the PMC module.

Figure 9 Mounting Points for PMC Modules on the PENT/CPCI-731



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4 Hardware

The PENT/CPCI-731 is a high performance CompactPCI platform. The I/O board is based on:

- Intel Pentium II/III Mobile Module
- PCI bus with 33 MHz clock frequency

Device Information

Wherever applicable, the PENT/CPCI-731 uses standard PC devices and related software to implement the features listed in section 2 “Introduction” on page 5. The following block diagram gives an overview on how those devices work together and which data paths they use.

Data Sheets

It is assumed that the PENT/CPCI-731 is integrated into systems at the operating system level. Therefore, no data sheets are provided in this *Reference Guide.* For a list of applicable data sheets, see the front matter of this manual.

Board Specific Registers

Following the block diagram for the PENT/CPCI-731, this section gives an overview on the I/O and memory maps and describes all PENT/CPCI-731 specific registers.

Figure 10 Block Diagramm

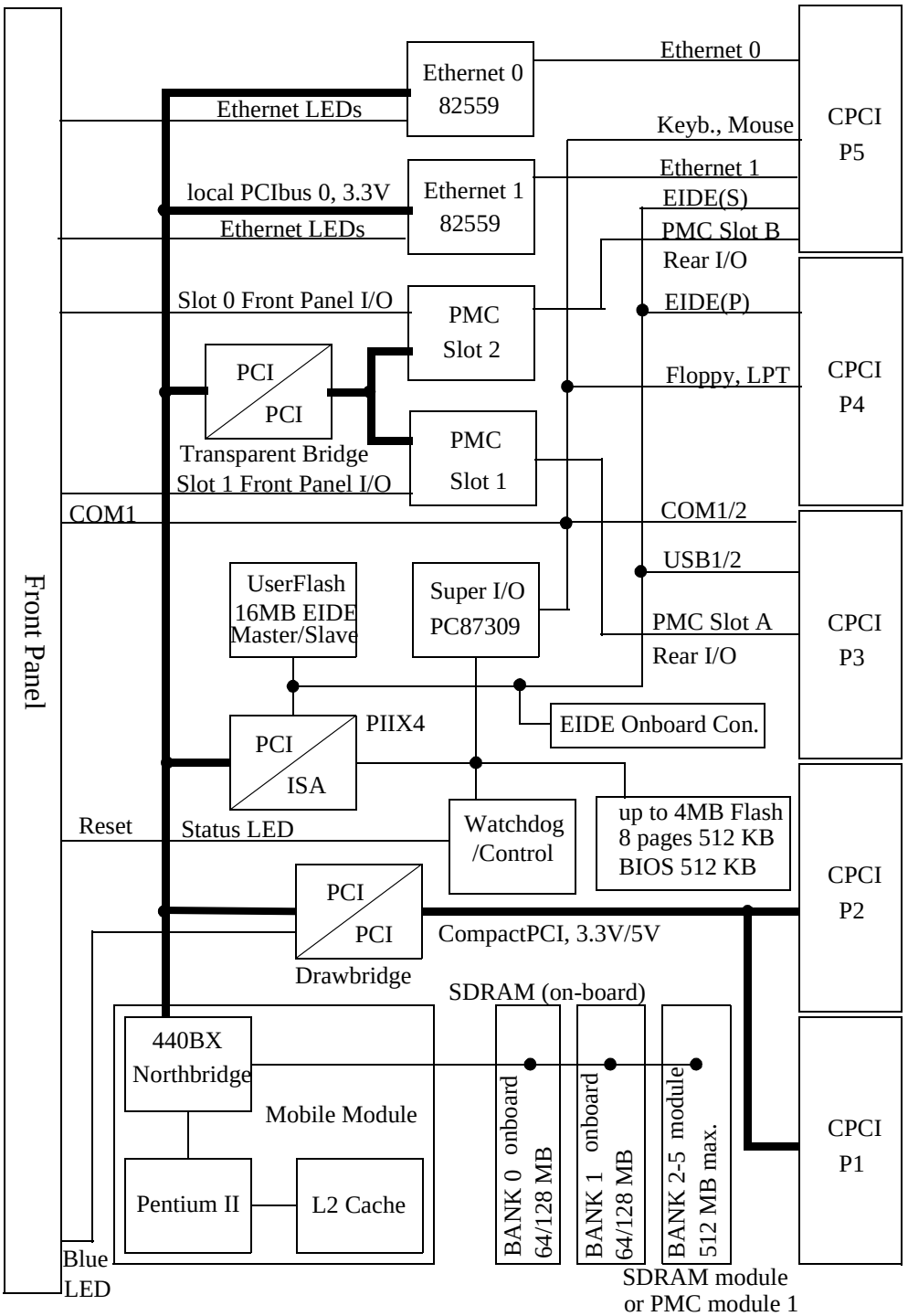

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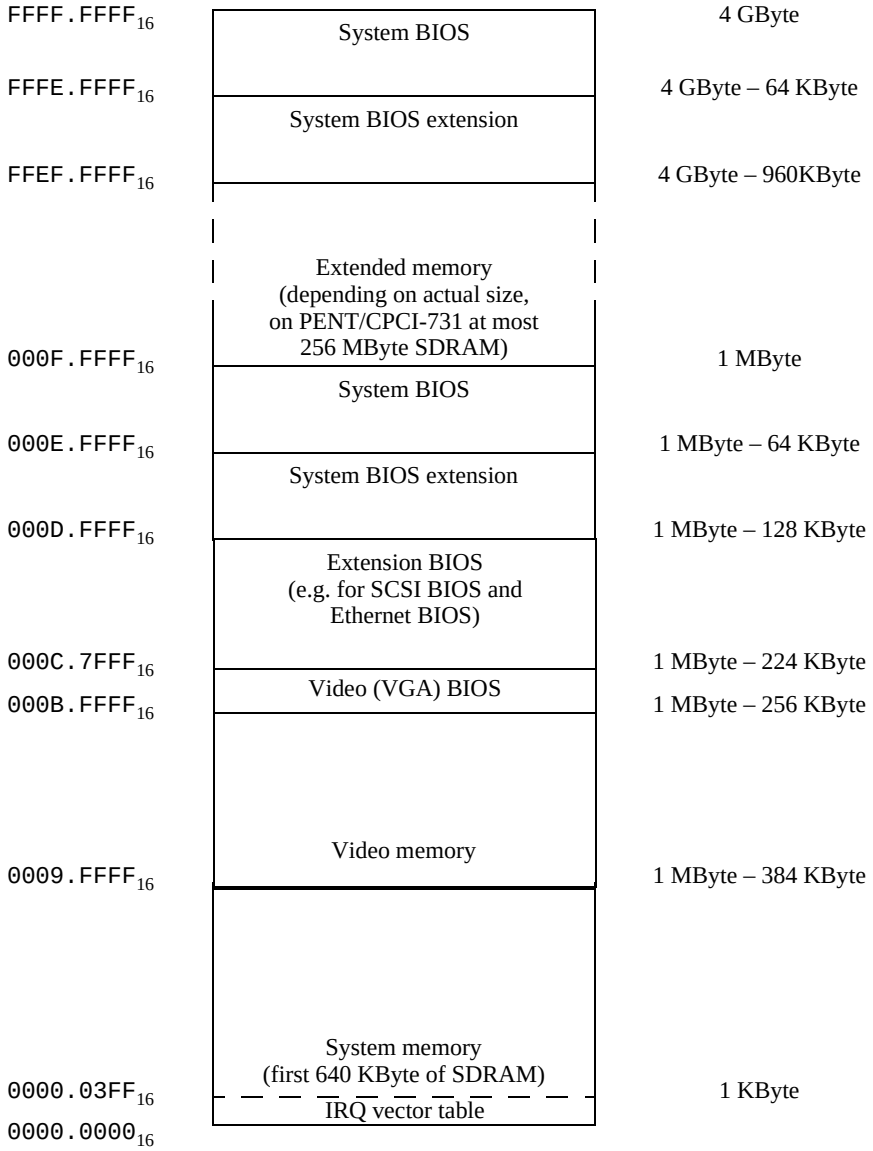
Table 7 I/O Map

I/O Address	Device ↓ EIDE, PCI-to-ISA bridge, USB: Intel 82371AB (82371EB) (developer.intel.com)	↓ Keyboard, PS2 mouse, COM1, COM2, LPT1, floppy: National PC87309 SuperI/O (www.national.com)	
0000_{16}…$001F_{16}$	x		DMA controller 1
0020_{16}…$003F_{16}$	x		Interrupt controller 1
0040_{16}…$005F_{16}$	x		Counter and timer
0060_{16}		x	Keyboard controller
0061_{16}	x		NMI status and control
0064_{16}		x	Keyboard controller
0070_{16}…0071_{16}	x		RTC and NMI mask
0080_{16}…$009F_{16}$	x		DMA page register
0100_{16}…$010F_{16}$		(x)	PENT/CPCI-731-specific registers (partially implemented in separate FPGA)
$00A0_{16}$…$00BF_{16}$	x		Interrupt controller 2
$00C0_{16}$…$00DF_{16}$	x		DMA controller 2
$00E0_{16}$…$00FF_{16}$	n.a.		Coprocessor
0170_{16}…0177_{16}	x		Secondary EIDE / ATAPI
$01F0_{16}$…$01F7_{16}$	x		Primary EIDE / ATAPI
0295_{16}…0296_{16}	n.a.		Hardware monitor
$02F8_{16}$…$02FF_{16}$		x	COM2
$03BC_{16}$…$03BF_{16}$		x	LPT1
$03C0_{16}$…$03DA_{16}$	n.a.		Graphic controller
$03F2_{16}$…$03F7_{16}$		x	Floppy-EIDE / ATAPI
$03F8_{16}$…$03FF_{16}$		x	COM1

Figure 11 Memory Map



4.1 I²C-BUS

The PENT/CPCI-731 contains three serial busses which use the I²C serial protocol. Via these serial busses the CPU can access board status sensors (temperature, voltages), memory sizes etc.

4.1.1 Module Information I²C Bus

The PENT/CPCI-731 contains a serial EEPROM free for applications. The EEPROM has a size of 256 bytes.

Table 8 Module Information I²C bus

Device Name	Device Type	Function	Location	Address
Reserved	24C04	Reserved	Base board	1010000_2
	24C02		Memory module	1010011_2
MEEPROM3	24C02	Free for applications	Base board	1010010_2

4.1.2 System Management I²C Bus

This serial bus is used for the PC compatible serial devices which comply with the SBus specification from Intel. The bus contains the temperature sensor on the Pentium II/III Mobile Module, the hardware monitor chip W83781D, 1 SPD serial EEPROM for the first and second memory bank. If the memory module is installed, two SPD serial EEPROMs on the module are visible on this bus as well. They contain information for memory banks 2 to 5. The SPD serial EEPROMs are built with the 24C02 version.

Table 9 System Management I²C Bus

Device Name	Device Type	Function	Location	Address
SPDEEPROM1	24C02	Memory bank 0, 1 information	Base board	1010000_2
SPDEEPROM2	24C02	Memory bank 2, 3 information	Memory module	1010001_2
SPDEEPROM3	24C02	Memory bank 4, 5 information	Memory module	1010010_2

Table 9 System Management I^2C Bus

Device Name	Device Type	Function	Location	Address
TEMPSENSE1	MAX1617	Temperature sensor	Pentium II mobile module	1001110_2
HWMON	W83781D	Hardware monitor chip	Base board	0101101_2*)

*) Power-on default value, can be altered via software

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4.2 Board Specific Registers

This section specifies the different registers of the FPGA located on the PENT/CPCI-731 board. The FPGA contains all the special functions not provided by the standard PC architecture. The registers implemented in the FPGA are accessible via the ISA-Bus.

Table 10 Register on Page 1 Overview

ISA-BUS ADDRESS	Register on PAGE 1	Comment
100_{16}	LED control register	1)
101_{16}	Reserved	1)
102_{16}	Reserved	1)
103_{16}	Flash control register	1)
104_{16}	Watchdog timer register	1)
105_{16}	Watchdog retrigger address	1)
106_{16}	Hot Swap ENUM register	1)
107_{16}	Geographical address register	1)
108_{16}	I^2C-bus register	1)
109_{16}	Reset control register 1	1)
$10A_{16}$	Reset control register 2	1)
$10B_{16}$	NMI control register	1)
$10C_{16}h$	Software NMI/Reset register	1)
$10D_{16}$	Reset/NMI status register	1)
$10F_{16}$	FLAG register	1)

Table 11 Register on Page 2 Overview

ISA-BUS ADDRESS	Register on PAGE 2	Comment
103_{16}	PCI control register	1)
104_{16}	PCI Interrupt control register	1)
$10F_{16}$	Version register	1)

Table 12 Independent Register Overview 3

ISA-BUS ADDRESS	Register Independent of Page	Comment
$10E_{16}$	Lock and page register	2)

1) Register controlled by the lock feature and locked after power up.
2) Register is not controlled by the lock feature.

4.2.1 ISA-BUS Decoding

This section gives a description on how ISA bus decoding is performed.

4.2.1.1 BIOS/User Flash Paging

The PCI-to-ISA bridge provides a 512 KByte or a 1 MByte address window to access the BIOS on the ISA-BUS.

The FPGA allows the mapping of eight pages with a size of 512 KByte or four pages with a size of 1 MByte in the BIOS address range. Four 1 MByte flash devices are provided. The flash device selection is performed via register bits in the flash control register (page 40). The address range is determined with the register bit `RANGE.`

The following figure gives an overview on the address mapping:

Figure 12 Flash Device Address Mapping

4.2.1.2 Flash Control Register

The flash control register provides the following:

Boot Block Write Protection — The flash device 0 programmed with the standard PC BIOS contains a writeprotected boot block area. The write protection can be enabled/disabled via switch SW1-2 (see table 6 “PENT/CPCI-731 Switch Settings” on page 14).

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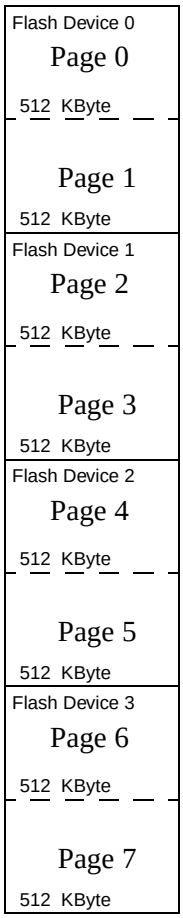
BIOS address range: 512 KByte



BIOS address range: 1 MByte

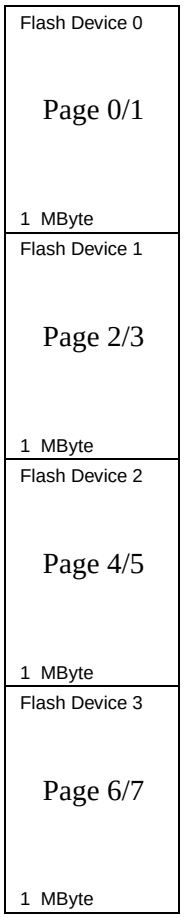


Table 13 Flash Control Register

Address: 0103_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
2 - 0	FLASH_SEL_0, FLASH_SEL_1, FLASH_SEL_2	Selects the flash device which is accessible in the BIOS address range.	r/w	= 000_2 (default) Flash device 0 is selected.
				= 001_2 Flash device 1 is selected.
				= 010_2 Flash device 2 is selected.
				= 011_2 Flash device 3 selected.
				= 100_2 FPGA Initialisation Flash is selected.
				= 101_2 reserved
				= 110_2 reserved
				= 111_2 reserved
3	RANGE	Selects the flash address range between 512 Kbyte and 1 Mbyte. The range must be equal to the BIOS address range configured in the South Bridge.	r/w	= 0 (default) Address range is 512 Kbyte. The A19 bit drives the FLASH_A19 address line.
				= 1 Address range is 1 Mbyte. The ISA-Bus address line ISA_SA[19]drives the FLASH_A19 signal.

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Table 13 Flash Control Register (cont.)

Address: 0103_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
4	A19	The A19 bit drives the address line FLASH_A19 of the selected flash devices directly and determines the 512 Kbyte page. If the RANGE bit is set to 1, the A19 bit has no function anymore and the FLASH_A19 is driven by the ISA-Bus address line ISA_SA[19].	r/w	= 0 The flash address line FLASH_A19 is driven low. The button 512 Kbyte page of one 1 Mbyte device is selected. The selected pages are 1, 3, 5, 7; depending on the setting of the FLASH_SEL[2…0] bits.
				= 1 (default) The flash address line FLASH_A19 is driven high. The top 512 Kbyte page of one 1 Mbyte device is selected. The selected pages are 0, 2, 4, 6; depending on the setting of the FLASH_SEL[2…0] bits.
5	A20	The A20 bit drives the address line FLASH_A20 of the flash devices directly. This bit has no function for using one Mbyte flash device.	r/w	= 0 The flash address line FLASH_A20 is driven low.
				= 1 (default) The flash address line FLASH_A20 is driven high.

Table 13 Flash Control Register (cont.)

Address: 0103_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
6	WE	WE selects between write protect and write enable mode of the flash memory devices.	r/w	= 0 The flash memory device is write protected.
				= 1 (default) The flash memory device is enabled for write access.
7	INIT_REQ	The INIT_REQ bit allows a software caused re-initialisation of the FPGA.	r/w	= 0 (default) The re-initialisation of the FPGA is disabled.
				= 1 Starts the re-initialisation directly after the write access.

4.2.2 I^2C Register

The I^2C Register is used for data transfer settings on the I^2C bus and provides acces to the program readable vintage registers for the base board and the memory modules.

Table 14 I^2C Register

Address: 0108_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
0	DIR	DIR specifies the direction of data transfer.	r/w	= 0 Data is written to the data line (drives the pulled-up data signal to low).
				= 1 (default) Data is read from the data line.

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Table 14 I²C Register (cont.)

Address: 0108_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
1	SCLK	Serial Clock line of the I^2C bus.	r/w	= 0 I2C_SCLK signal is driven low.
				= 1 (default) I2C_SCLK signal is driven high.
2	DATA_IN	DATA_IN stores the current value of the data line.	r	
7 - 3	Reserved		r/w	

4.2.3 Reset and Watchdog

The reset logic supports a destructive/ non destructive board reset for every reset source. Non destructive reset means that the contents of the main memory remains unchanged during the reset phase.

4.2.3.1 Reset Types

The FPGA supports the following two different reset types:

- Destructive Reset
- Non Destructive Reset

Destructive Reset

Independent of all register settings, the signal BRG_S_RST_N causes in all case a destructive reset if it is asserted via writing the reset register of the DEC 21554. This function is necessary to cause a destructive reset on a non-host configured board in a system which does not allow a FPGA register access anymore or to reset a single slave board without resetting the whole CompactPCI bus.

The PWR_FAIL_DET_N and WATCHDOG2 signals will also cause a destructive reset independent of all register settings.

4.2.3.2 NMI/Reset Sources

The following NMI/reset sources and functions are implemented.

Table 15 NMI/Reset Sources

Signal Name	Function	Reset Maskable	Reset Type		NMI Maskable	Comments
			Destructive	Non Destructive		
CPCI_RST_N	CompactPCI bus reset	x	x	x	x	External source, bidirectional
CPCI_PBRST_N	CompactPCI bus push button reset	x	x	x	x	External source
RESET_IN_P5	Reset input from P5	x	x	x	x	
SWITCH_RESET_N	Frontpanel reset key	x	x	x	x	
BRG_S_RST_N	This signal is controlled by the RESET register of the PCI-to-PCI bridge.	-	x	-	-	External sources, causes in any cases a destructive reset
PWR_FAIL_DET_N	Power fail detection form power up CPLD	-	x	-	-	
WDOG_1_N	Watchdog 1	x	x	x	x	Internal source
WDOG_2_N	Watchdog 2	x	x	-	-	
SOFT	Software	x	x	x	x	
SB	PCI-to-ISA bridge	NA	NA	NA	-	External source, causes only a NMI
RST_HW_MON_N	System control chip	NA	NA	NA	x	External source, causes only a NMI

- In the Reset control register 1 the NMI/reset sources can be enabled/disabled to cause a reset.
- The Reset control register 2 determines the reset type (destructive/non destructive).
- In the NMI control register, the NMI/reset source can be enabled/disabled to cause an NMI.

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Table 16 Possible NMI/Reset Configurations

Reset Mask Bit (Reset Configuration Register 1)	Reset Type Bit (Reset Configuration Register 2)	NMI Mask Bit (NMI Configuration Register)	NMI/Reset Source
1	Don’t care	1	disabLed
0	0	1	Causes a destructive reset (default)
0	1	1	causes a non destructive reset
1	Don’t care	0	Causes a NMI
0	0	0	Causes a NMI and after 1s a destructive reset
0	1	0	Causes a NMI and after 1s a non destructive reset

4.2.3.3 Reset Control Register 1

Table 17 Reset Control Register 1

Address: 0109_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
0	SWITCH_RST_MASK	Reset mask bit for the front-panel reset key	r/w	= 0 (default) The reset source is enabled.
				= 1 The reset source is disabled.
1	RST_IN_P5_MASK	Reset mask bit for the reset input from the P5 connector	r/w	= 0 (default) The reset source is enabled.
				= 1 The reset source is disabled.

Table 17 Reset Control Register 1 (cont.)

Address: 0109_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
2	CPCI_ PBRST_ MASK	Reset mask bit for CompactPCI bus push buttom reset.	r/w	= 0 (default) The reset source is enabled.
				= 1 The reset source is disabled.
3	CPCI_ RST_ MASK	Reset mask bit for the CompactPCI bus Reset.	r/w	= 0 (default) The reset source is enabled.
				= 1 The reset source is disabled.
4	WDOG1_ RST_ MASK	Reset mask bit for the watchdog 1 reset.	r/w	= 0 The reset source is enabled.
				= 1 (default) The reset source is disabled.
5	SOFT_ RST_ MASK	Reset mask bit for the software reset.	r/w	= 0 (default) The reset source is enabled.
				= 1 The reset source is disabled.
6	WDOG2_RST_ MASK	Reset mask bit for the watchdog 2 reset.	r/w	= 0 The reset source is enabled.
				= 1 (default) The reset source is disabled.
7	Reserved			

Note: **Invalid configuration if WDOG2_RST_MASK is enabled and WDOG1_RST_MASK is disabled.**

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4.2.3.4 Reset Control Register 2

Table 18 Reset Control Register 2

Address: $010A_{16}$ PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
0	SWITCH_RST_ TYPE	Specifies the reset type of the reset key.	r/w	= 0 (default) The reset source causes a destructive reset.
				= 1 The reset source causes a non destructive reset.
1	RST_IN_ P5_ TYPE	Specifies the reset type of the reset input from the P5 connector.	r/w	= 0 (default) The reset source causes a destructive reset.
				= 1 The reset source causes a non destructive reset.
2	CPCI_ PBRST_ TYPE	Specifies the reset type of the CompactPCI bus push button reset.	r/w	= 0 (default) The reset source causes a destructive reset.
				= 1 The reset source causes a non destructive reset.
3	CPCI_ RST_ TYPE	Specifies the reset type of the CompactPCI bus reset.	r/w	= 0 (default) The reset source causes a destructive reset.
				= 1 The reset source causes a non destructive reset.

Table 18 Reset Control Register 2 (cont.)

Address: $010A_{16}$ PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
5 - 4	WDOG1_ RST_ TYPE_0, WDOG1_ RST_ TYPE_1	Specifies the reset type of watchdog reset.	r/w	= 00_2 (default) The reset source causes a destructive reset. = 01_2 The reset source causes a non destructive reset. = 10_2 The reset source causes a NMI. = 11_2 reserved.
6	SOFT_ RST_ TYPE	Specifies the reset type of the software reset.	r/w	= 0 (default) The reset source causes a destructive reset.
				= 1 The reset source causes a non destructive reset.
7	Reserved			

4.2.3.5 Non Maskable Interrupt NMI

Every reset source is configured via the NMI control register to cause an NMI before asserting the reset signals. In addition to the described reset sources, the PCI-to-ISA bridge and the Hardware Monitor Chip may also cause an NMI. The PCI-to-ISA bridge NMI source is not maskable in the NMI control register. The time between the assertion of the CPU_NMI signal and the reset signals is fixed to 1 s.

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4.2.3.6 NMI Control Register

Table 19 NMI Control Register

Address: $010B_{16}$ PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
0	SWITCH_NMI_MASK	NMI mask bit for the reset key.	r/w	= 0 NMI is enabled.
				= 1 (default) NMI is disabled.
1	RST_IN_P5_NMI_MASK	NMI mask bit for the reset input of the P5 connector.	r/w	= 0 NMI is enabled.
				= 1 (default) NMI is disabled.
2	CPCI_PB_NMI_MASK	NMI mask bit for the CompactPCI bus push button reset.	r/w	= 0 NMI is enabled.
				= 1 (default) NMI is disabled.
3	CPCI_NMI_MASK	NMI mask bit for the CompactPCI bus reset.	r/w	= 0 NMI is enabled.
				= 1 (default) NMI is disabled.
4	WDOG_NMI_MASK	NMI mask bit for the watchdog. Note: These settings override the reset control register 2. If the NMI is disabled here no NMI will be generated even if bits 4 and 5 of the reset control register are programmed to 00_2.	r/w	= 0 NMI is enabled.
				= 1 (default) NMI is disabled.
5	SOFT_NMI_MASK	NMI mask bit for the software reset.	r/w	= 0 NMI is enabled.
				= 1 (default) NMI is disabled.

Table 19 NMI Control Register (cont.)

Address: $010B_{16}$ PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
6	HW_MON_NMI_ MASK	NMI mask bit for the Hardware Monitor Chip reset.	r/w	= 0 NMI is enabled.
				= 1 (default) NMI is disabled.
7		Reserved		

4.2.3.7 Reset/NMI Status Register

The Reset/NMI Status register allows the software to find out, what kind of reset source has been caused a NMI and/or a non-destructive reset and enables clearing all of its status bits via a write access to this register.

Table 20 Reset/NMI Status Register

Address: $010D_{16}$ PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
0	SWITCH_RST_STAT	Indicates whether the reset key has caused an NMI and/or reset since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI/reset has been caused.
				= 1 NMI/reset has been caused.
1	RST_IN_P5_ RST_STAT	Indicates whether the reset input of the P5 connector has caused an NMI/reset since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI/reset has been caused.
				= 1 NMI/reset has been caused.
2	CPCI_PBRST_STAT	Indicates whether the CompactPCI bus push button reset caused an NMI/reset since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI/reset has been caused.
				= 1 NMI/reset has been caused.

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Table 20 Reset/NMI Status Register

Address: $010D_{16}$ PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
3	CPCI_RST_STAT	Indicates whether the CompactPCI bus reset has caused an non destructive reset since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI/reset has been caused.
				= 1 NMI/reset has been caused.
4	WDOG_RST_STAT	Indicates whether the watchdog caused an non-destructive reset since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI/reset has been caused.
				= 1 NMI/reset has been caused.
5	SOFT_RST_STAT	Indicates whether the software caused an non destructive reset via the reset generation register since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI/reset has been caused.
				= 1 NMI/reset has been caused.
6	SB_NMI_STAT	Indicates whether the South Bridge caused an NMI since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI has been caused.
				= 1 NMI has been caused.
7	HW_MON_NMI_STAT	Indicates whether the hardware monitor chip caused an NMI since the last clearance of the status bits via a write access to the register.	r/w	= 0 (default) No NMI has been caused.
				= 1 NMI has been caused.

4.2.3.8 Software NMI/Reset

The software NMI/Reset can be caused by writing a *magic byte* to the Software NMI/Reset register.

4.2.3.9 Software NMI/Reset Register

Table 21 Software NMI/Reset Register

Address: $010C_{16}$ PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
7 - 0	SWRST[7…0]	A write access with the magic byte to this register can cause an NMI/reset, depending on the setting of the SOFT_RST_MASK bit in the reset control register 2 and the SOFT_NMI_MASK bit in the NMI control register.	w	= $0\ 1\ 0\ 1\ 0\ 1\ 0\ 1_2$ The reset source can cause an NMI/reset.
				≠ $0\ 1\ 0\ 1\ 0\ 1\ 0\ 1_2$ No NMI/reset will be generated.

4.2.3.10 Watchdog

The Watchdog can be configured according to the table “Possible NMI/Reset Configurations” on page 47. The watchdog timer starts running if the WDOG_RST_MASK bit in the reset control register 1 is set to 0. If not masked with the reset control register 1 the Watchdog 2 will assert a destructive reset 1 second after the watchdog 1 has set an NMI.

4.2.3.11 Watchdog Retrigger

A write access to the I/O address 0105_{16} retriggers the watchdog timer when the watchdog is enabled. This must be done at least in every time period specified in the watchdog timer register to prevent a watchdog time out.

4.2.3.12 Watchdog Timer

The FPGA input clock signal FPGA_CLK33 with f = 33.33MHz is used to implement the watchdog timer.

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Table 22 Watchdog Timer

DIV [3..0]Bit (Watchdog Control Register)	FPGA_CLK33 Divider 33,33 Mhz == 30,00 ns	Watchdog Timer
0000_2	2^{13} = 8192	245.760 us
0001_2	2^{14} = 16384	491.520 us
0010_2	2^{15} = 32768	983.040 us
0011_2	2^{16} = 65536	1.966 us
0100_2	2^{17} = 131072	3.932 ms
0101_2	2^{18} = 262144	7.864 ms
0110_2	2^{19} = 524288	15.729 ms
0111_2	2^{20} = 1048576	31.457 ms
1000_2	2^{21} = 2097152	62.915 ms
1001_2	2^{22} = 4194304	0.126 s
1010_2	2^{23} = 8388608	0.252 s
1011_2	2^{24} = 16777216	0.503 s
1100_2	2^{25} = 33554432	1.007 s
1101_2	2^{26} = 67108864	2.013 s
1110_2	2^{27} = 134217728	4.027 s
1111_2	2^{28} = 268435465	8.053 s

4.2.3.13 Watchdog Timer Register

Table 23 Watchdog Timer Register

Address: 0104_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
3-0	DIV[0…3]	Controls the retrigger period of the watchdog. The retrigger period is programmable from 245.760 us to 8.053 s in 16 steps.	r/w	= 0000_2 == 245.760 us
				= 0001_2 == 491.520 us
				= 0010_2 == 983.040 us
				= 0011_2 == 1.966 ms
				= 0100_2 == 3.932 ms
				= 0101_2 == 7.864 ms
				= 0110_2 == 15.729 ms
				= 0111_2 == 31.457 ms
				= 1000_2 == 62.915 ms
				= 1001_2 == 0.126 s
				= 1010_2 == 0.252 s
				= 1011_2 == 0.503 s
				= 1100_2 == 1.007 s
				= 1101_2 == 2.013 s
				= 1110_2 == 4.027 s

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Table 23 Watchdog Timer Register (cont.)

Address: 0104_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
				$= 1111_2$ == 8.053 s
7 -4		Reserved		

4.2.4 PCI Configuration and Interrupt, Operating Modes

The PENT/CPCI-731 is configurable to operate in as normal non-host (peripheral) board or in a special mode, the Interrupt and ENUM service mode.

4.2.4.1 Interrupt and Enum Service Mode

In this mode CompactPCI Interrupts and ENUM signals are serviced and the CompactPCI reset signal is driven. The interrupt routing is configurable independent of the currently active mode.

4.2.4.2 Signal Direction

Via the **PCI_DIR** bit of the PCI control register The PENT/CPCI-731 can be configured to cause or to receive CompactPCI interrupts, CompactPCI reset and Hot Swap CompactPCI ENUM. The inverted state of this bit is mirrored to the INT_LVT_DIR signal to control the direction of the CompactPCI signal buffer on the PENT/CPCI-731.

After power up the CPCI_SYSEN_N signal is sampled and the state is written in the PCI_DIR register bit. A low state means that the board is configured to provide the interrupt and enum service mode functionality and a high signal state configures the board to operate as a normal non-host board. The PCI_DIR bit could be overwritten after power up by software.

Table 24 Signal Direction

CompactPCI Signal	Interrupt and Enum Service Mode	Configuration as Non-Host
Interrupts CPCI_INT[D…A]_N	Input	Output

Table 24 Signal Direction (cont.)

CompactPCI Signal	Interrupt and Enum Service Mode	Configuration as Non-Host
Reset CPCI_RST_N	Output	Input
ENUM CPCI_ENUM_N	Input	Output

4.2.4.3 Interrupt Mask

Every CompactPCI Interrupt is maskable via the INTx_MASK bit in the PCI Control register, x = A, B, C, D.

4.2.4.4 Interrupt Routing

The interrupt routing from the CompactPCI to the local PCI bus, the interrupt routing from the primary side of the PCI-to-PCI bridge to the CompactPCI and the interrupt routing from the secondary side of the PCI-to-PCI bridge to the local PCI bus are selectable in the PCI interrupt control register.

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4.2.4.5 PCI Control Register

Table 25 PCI Control Register

Address: 0103_{16} PAGE 2				
Bit	**Value**	**Description**	**Access**	**Settings**
0	INTD_MASK	The CompactPCI bus interrupts are maskable independent of the setting of the PCI-Bus direction bit PCI_DIR. This is useful if more than one board in a system operates in the Interrupt and ENUM service mode to share the interrupt servicing. By default the non-host board drives no interrupts to the CompactPCI backplane, since the local processor serves all local interrupts. If the board is configured to use the Interrupt and ENUM service mode and is intended to serve interrupts the INTx_MASK bits must be set to 0.	r/w	= 0 The corresponding CompactPCI bus interrupt is not masked (enable).
				= 1 (default) The corresponding CompactPCI bus interrupt is masked (disabled).
1	INTC_MASK		r/w	= 0 The corresponding CompactPCI bus interrupt is not masked (enable).
				= 1 (default) The corresponding CompactPCI bus interrupt is masked (disabled).
2	INTB_MASK		r/w	= 0 The corresponding CompactPCI bus interrupt is not masked (enable).
				= 1 (default) The corresponding CompactPCI bus interrupt is masked (disabled).

Table 25 PCI Control Register (cont.)

Address: 0103_{16} PAGE 2				
Bit	**Value**	**Description**	**Access**	**Settings**
3	INTA_MASK		r/w	= 0 The corresponding CompactPCI bus interrupt is not masked (enable).
				= 1 (default) The corresponding CompactPCI bus interrupt is masked (disabled).

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Table 25 PCI Control Register (cont.)

Address: 0103_{16} PAGE 2				
Bit	**Value**	**Description**	**Access**	**Settings**
4	PCI_DIR	Selects the direction of the CompactPCI bus interrupt, reset and ENUM signals. The FPGA output signal INT_LVT_DIR mirrors the state of this bit. The bit state after power up depends on the CPCI_SYSEN_N signal. After power up this bit can be overwritten by software to enable the Interrupt and ENUM service mode.	r/w	= 0 The PENT/CPCI-731 provides the Interrupt and ENUM service mode and drives the signal INT_LVT_DIR low. The BRG_ENUM_R_N signal of the PCI-to-PCI bridge is masked and is not visible to the CompactPCI bus. The Hot Swap ENUM register is configured to detect the CPCI_ENUM_N assertion of other boards. The CPCI_RST_N signal is output.
				= 1 (default) The PENT/CPCI-731 provides non-host functionality and drives the signal INT_LVT_DIR high. The BRG_ENUM_R_N signal of the PCI-to-PCI bridge is unmasked and is visible to the CompactPCI bus. The Hot Swap ENUM register is disabled. The CPCI_RST_N signal is input.

Table 25 PCI Control Register (cont.)

Address: 0103_{16} PAGE 2				
Bit	**Value**	**Description**	**Access**	**Settings**
5	PCIDIR_MASK	Selects whether the PCI_DIR bit is programmable via software or determined by the CPCI_SYSEN_N signal.	r/w	= 0 The PCI_DIR bit is determined by the CPCI_SYSEN_N pin.
				= 1 (default) The user can write a 0 or 1 to the PCI_DIR bit to force the Interrupt and ENUM service mode or the normal non-host functionality.
7 - 6		Reserved		

4.2.4.6 PCI Interrupt Control Register

Table 26 PCI Interrupt Control Register

Address: 0104_{16} PAGE 2				
Bit	**Value**	**Description**	**Access**	**Settings**
1 - 0	PCI_INT [1…0]	Selects the interrupt routing between the Compact-PCI bus and the local PCI bus.	r/w	= 00_2 (default) L_PCI_INTA_N is routed to CPCI_INTA_N. L_PCI_INTB_N is routed to CPCI_INTB_N. L_PCI_INTC_N is routed to CPCI_INTC_N. L_PCI_INTD_N is routed to CPCI_INTD_N.
				= 01_2 L_PCI_INTA_N is routed to CPCI_INTB_N. L_PCI_INTB_N is routed to CPCI_INTC_N. L_PCI_INTC_N is routed to CPCI_INTD_N. L_PCI_INTD_N is routed to CPCI_INTA_N.

Table 26 PCI Interrupt Control Register (cont.)

Address: 0104_{16} PAGE 2				
Bit	**Value**	**Description**	**Access**	**Settings**
				= 10_2 L_PCI_INTA_N is routed to CPCI_INTC_N. L_PCI_INTB_N is routed to CPCI_INTD_N. L_PCI_INTC_N is routed to CPCI_INTA_N. L_PCI_INTD_N is routed to CPCI_INTB_N.
				= 11_2 L_PCI_INTA_N is routed to CPCI_INTD_N. L_PCI_INTB_N is routed to CPCI_INTA_N. L_PCI_INTC_N is routed to CPCI_INTB_N. L_PCI_INTD_N is routed to CPCI_INTC_N.

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Table 26 PCI Interrupt Control Register (cont.)

Address: 0104_{16} PAGE 2				
Bit	**Value**	**Description**	**Access**	**Settings**
3 - 2	SEC_INT [1…0]	Selects the interrupt routing between the secondary interrupt of the PCI-to-PCI bridge and the local PCI-Bus.	r/w	= 00_2 BRG_S_INT_N is routed to L_PCI_INTA_N. = 01_2 BRG_S_INT_N is routed to L_PCI_INTB_N. = 10_2 (default) BRG_S_INT_N is routed to L_PCI_INTC_N. = 11_2 BRG_S_INT_N is routed to L_PCI_INTD_N.
5 - 4	PRIM_INT [1…0]	Selects the interrupt routing between the secondary interrupt of the PCI-to-PCI bridge and the local PCI-Bus.	r/w	= 00_2 (default) BRG_P_INT_N is routed to CPCI_INTA_N. = 01_2 BRG_P_INT_N is routed to CPCI_INTB_N. = 10_2 BRG_P_INT_N is routed to CPCI_INTC_N. = 11_2 BRG_P_INT_N is routed to CPCI_INTD_N.
7 - 6		Reserved		

4.2.5 Geographical Addressing and Rear Transition Module

The state of the CompactPCI geographical address signals CPCI_GA[4…0] and the rear transition module present signal TM_RPNT are readable via the geographical address register bits.

4.2.5.1 Geographical Address

The state of the geographical address lines CPCI_GA[4…0] are directly readable via the register bits GA[4…0] of the geographical address register.

4.2.5.2 Rear Transition Module Detection

The TM_PRNT signal indicates if a rear transition module is assembled or not behind the corresponding CompactPCI slot.

Table 27 TM_PRNT Signal

TM_PRNT	Status of the Rear Transition Module
Low	Present
High	Not present

The signal state is readable in the register bit TM_PRNT in the geographical address register.

4.2.5.3 Geographical Address Register

Table 28 Geographical Address Register

Address: 0107_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
4 - 0	GA[4…0]	Mirrors the signal state of the geographical address lines.	r	
5	TM_PRNT	Mirrors the signal state of the rear transition module present signal TM_PRNT.	r	
7 - 6		Reserved		Set to 0

4.2.6 Hot Swap LED/Switch and ENUM

4.2.6.1 Hot Swap ENUM Register

Note: **The register is only enabled and accessible if the board operates in the interrupt and ENUM service mode.**

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The ENUM register has three major functions:

1. Detect the assertion of the CPCI_ENUM_R_N signal caused by other non-host boards.
2. Mask/unmask the BRG_ENUM_R_N signal from the on-board PCI-to-PCI bridge.
3. Support polling and interrupt mode to detect the assertion of the CPCI_ENUM_R_N signal.

Table 29 Hot Swap ENUM Register

Address: 0106_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
0	ENUM	ENUM shows the logic level of the CPCI_ENUM_R_N signal at the CompactPCI backplane.	r	= 0 CPCI_ENUM_R_N signal is asserted.
				= 1 CPCI_ENUM_R_N is not asserted.
1	MASK	MASK is used to mask the ENUM interrupt.	r/w	= 0 (default) The ENUM interrupt is masked and no interrupts will occur.
				= 1 The ENUM interrupt is unmasked and an interrupt will occur if the ENUM signal on the CompactPCI backplane is asserted.
2	IRQ	IRQ reflects the status of the interrupt line.	r/w	= 0 (default) The ISA-Bus IRQ is not asserted.
				= 1 The ISA-Bus IRQ level 11 is asserted if the ENUM signal goes active and the IRQ stays active until a write access to the register.
7-3		Reserved		Set to 0

4.2.7 LEDs

The FPGA controls two bicolor (red/green) LEDs. The LEDs are configurable as user LEDs and/or to show the primary and secondary IDE device access.

The LED 2 can be programmed as IDE-led. User LED 2 has no effect in that case.

4.2.7.1 LED Control Register

The LED control register specifies the status of the LEDs. The BIOS activates the IDE LED after booting.

Table 30 LED Control Register

Address: 0100_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
1 - 0	1_LEDSTAT [1…0]	1_LEDSTAT has to specify the status of the user LED on the PENT/CPCI-731's front panel.	r/w	= 00_2 (default) off
				= 01_2 red
				= 10_2 green
				= 11_2 off
3 - 2	2_LEDSTAT [1…0]	2_LEDSTAT has to specify the status of the user LED on the PENT/CPCI-731's front panel. The function of 2_LEDSTAT depends on the configuration of IDE_LEDSTAT.	r/w	= 00_2 (default) off
				= 01_2 red
				= 10_2 green
				= 11_2 off

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Table 30 LED Control Register (cont.)

Address: 0100_{16} PAGE 1				
Bit	**Value**	**Description**	**Access**	**Settings**
5 - 4	IDE_LEDSTAT [1…0]	IDE_LEDSTAT has to specify the color and the function of the IDE access LED on the PENT/CPCI-731's front panel.	r/w	= 00_2 (default) off
				= 01_2 Signals the IDE activity red.
				= 10_2 Signals the IDE activity green.
				= 11_2 reserved.
7 - 6		Reserved		set to 0

4.2.8 Additional Features

This section describes some additional features of the PENT/CPCI-731.

4.2.8.1 Register Lock and Page Function

The lock and page register enables or disables the read and write access to the protectable registers. The affected registers are listed in "Board Specific Registers" on page 39.

The read back value of a protected register is always FF_{16}, even the LOCK/UNLOCK register is read as FF_{16}, but is write accessible.

Table 31 Lock and Page Register

Address: $010E_{16}$ PageIndependent				
Bit	**Value**	**Description**	**Access**	**Settings**
2 - 0	B[2…0]	B[2…0] has to specify whether the protectable registers are unlocked or locked.	r/w	= 010_2 Unlocked the specific registers. ≠ 010_2 (default) Locked the specific registers.
3		reserved		

Table 31 Lock and Page Register (cont.)

Address: $010E_{16}$ PageIndependent				
Bit	**Value**	**Description**	**Access**	**Settings**
4	PAGE	The PAGE bit sets the access to the registers located in PAGE 1 or PAGE 2.	r/w	= 0 Registers located in PAGE 1 are accessible.
				= 1 Registers located in PAGE 2 are accessible.
7		Reserved		

Table 32 Flag Register

Address: $010F_{16}$ Page 1				
Bit	**Value**	**Description**	**Access**	**Settings**
0	FLAG	BIOS determines whether it should execute full POST or directly jump to an external boot loader located in a user flash.	r/w	= 0 Normal BIOS is carried out.
				= 1 BIOS jumps to an external bootloader.
7 - 1		Reserved		set to 0

4.2.8.2 Version Register

The version register provides the version of the FPGA software in BCD-code.

Table 33 Version Register

Address: $010F_{16}$ Page 2				
Bit	**Value**	**Description**	**Access**	**Settings**
3 - 0	x[3…0]	The most significant four bits specify the first number of the version.	r/w	
7 - 4	y [3…0]	The least significant four bits specify the second number of the version. The version can therefore be max. 99_d.	r/w	

4.2.9 Spare Configuration Switches

Four additional configuration switches are connected to the FPGA. These switches are currently unused and are reserved for features in the future.

Table 34 Configuration Switches

Switch	Position	CONF_SW_x_N Signal State
SW3-x	Off	High
SW3-x	On	Low

4.2.10 PMC Slot Identification

The PMC slot identification mechanism can be used to detect if a PCI bus compliant CMC module (i.e. PMC) is plugged on 1 of the PMC module sockets. There are four signals (BUSMODE4-BUSMODE1) which are used for the detect mechanism. BUSMODE2, 3, and 4 is a signal group which is generated by the PMC host. Each PMC socket has one BUSMODE1 signal which is pulled high on the host side. BUSMODE2, 3 and 4 are fixed to a certain logic level (001_2) by the PENT/CPCI-731 to indicate that the CMC host is capable of driving the PCI bus protocol. A CMC module which uses the PCI bus protocol (PMC) should drive the BUSMODE1 pin low to indicate to the host that it is capable of driving the PCI bus protocol.

Note: **The PENT/CPCI-731 accepts PMC cards which do not drive the BUSMODE1 pin low. Application software may use the detect mechanism described below to verify if a PMC card is installed.**

The BUSMODE1 signal of PMC slot 1 and 2 are connected to general purposes I/O pins of the PCI-to-PCI bridge (see table 35 “Busmode/GPIO Routing” on page 72). This bridge is used to connect the PMC slots to the local PCI bus of the PENT/CPCI-731. The general purpose I/O pins used to read the logic level of the BUSMODE1 signals must be configured as inputs (default setting).

The general purpose registers are accessible via the PCI configuration space of the Intel21150 PCI-to-PCI chip.

For a complete description of the general purpose I/O registers see the data sheet of the Intel21150 PCI-to-PCI chip.

Table 35 Busmode/GPIO Routing

General Purpose I/O Pin	GPIO0	GPEI1
PMC Slot	2	1

Table 36 General Purpose I/O Registers in Intel21150

Base Address	I/O Offset	Function
Via PCI configuration space, Intel21150	0x65	GPIO Output Data Register
	0x66	GPIO Output Enable Control Register
	0x67	GPIO Input Data Register

4.2.11 Hardware Monitor

The PENT/CPCI-731 contains a hardware monitor chip which monitors the local board voltages and temperatures. Thresholds can be programmed for the voltages. If one of the voltages is out of the predefined range the chip generates an alarm (external system management interrupt, EXTSMI). Monitored voltages are +5 V, +3.3 V, +12 V, -12 V and the two +2.5 V voltages from the mobile module which are used for the clock reference.

The maximum input voltage at the hardware monitor is 4.095 V except the 5V input. To measure the +/-12 voltages, the respective inputs are scaled with resistors. Software which sets up the hardware monitor must consider this scale.

The PENT/CPCI-731 has three temperature sensors located on top of the board. One is set closely to the CPU module, the other sensors are placed on cooler positions (see figure 1 “Location Diagram of the

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PENT/CPCI-731 (Schematic)" on page 13). Thresholds can be set for the three sensors to generate an alarm if the threshold temperature is reached.

The fan inputs (FANx) are disabled on the PENT/CPCI-731.

The hardware monitor can be addressed by either using the system management bus (SMB) via the PCI-to-ISA bridge or directly via CPU I/O cycles at the ISA bus.

A software (Winbond Hardware Doctor) is available on the delivery CD. It initializes the hardware monitor chip and provides a user interface under WinNT. The thresholds can be set and events can be masked or enabled for generating an alarm. For further information on the use of this software refer to the `readme` file on the CD.

Table 37 Monitored Board Voltages versus Hardware Monitor Voltage Inputs

Board Voltage	Voltage Input	Scale
+5V	+5VIN	1.0
Short to GND	-5VIN	None
+3.3V	+3.3VIN	1.0
+12V	+12VIN	0.26
-12V	-12VIN	-0.28
VCPUIO, 2.5V	VCOREA	1.0
VCLK, 2.5V	VCOREB	1.0

Table 38 Hardware Monitor Base Address

Base Address	PCI-to-ISA Chip select	Used Bus
295_{16},296_{16}	1	ISA
0101101_2	None	SMB

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Product Error Report

PRODUCT:	SERIAL NO.:
DATE OF PURCHASE:	ORIGINATOR:
COMPANY:	POINT OF CONTACT:
TEL.:	EXT.:
ADDRESS: PRESENT DATE:	
AFFECTED PRODUCT: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS	AFFECTED DOCUMENTATION: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS
ERROR DESCRIPTION:	

THIS AREA TO BE COMPLETED BY FORCE COMPUTERS:

DATE:

PR#:

RESPONSIBLE DEPT.: ❑ MARKETING ❑ PRODUCTION

ENGINEERING ➠ ❑ BOARD ❑ SYSTEMS

☞ Send this report to the nearest Force Computers headquarter listed on the back of the title page.