VMIC VMIVME-7588-841

Enhanced Pentium Processor-Based VMEbus CPU Module

Limited Availability
Used and in Excellent Condition

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VMIVME-7588

Enhanced Pentium Processor-Based VMEbus CPU

Product Manual

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
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RECORD OF REVISIONS

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(I/O man figure)

(Instant OPC wizard logo)

(IOWorks man figure)

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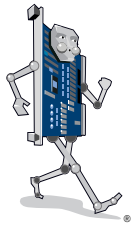

(I/O Man Figure)

(VMIC LOGO)

VME Microsystems International Corporation

RECORD OF REVISIONS

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VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

W A R N I N G

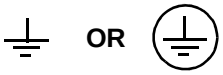
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

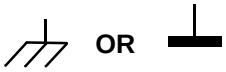
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



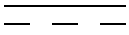
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

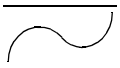


Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER

1

OVERVIEW

IN THIS CHAPTER:

SECTION 1 - INTRODUCTION TO THE VMIVME-7588

VMIC's VMIVME-7588 is a complete IBM PC/AT-compatible Pentium® processor-based computer with the additional benefits of Eurocard construction and full compatibility with the VMEbus Specification Rev. C.1. The VMIVME-7588 with advanced VMEbus interface, and RAM that is dual-ported to the VMEbus, is ideal for multiprocessor applications.

The CPU board functions as a standard PC/AT. It executes a PC/AT-type power-on self-test, then boots up MS-DOS®, Window 3.11, Windows 95®, Windows NT™, or any other PC/AT-compatible operating system. The PC/AT mode of the VMIVME-7588 is discussed in Chapter 3 of this manual.

Beyond the standard PC/AT-compatible CPU, the VMIVME-7588, when supplied with an optional PCI-to-VMEbus bridge, may also operate as a VMEbus controller and interact with other VMEbus modules.

The VMIVME-7588 may also be accessed as a VMEbus slave board. The VMEbus functions are available by programming the VMIVME-7588's PCI-to-VMEbus bridge according to the references defined in this manual or Volume II.

In this document suite, references made to the VMIVME-7588-003 or -004 apply to the PC/AT CPU board without the optional PCI-to-VMEbus

bridge. References made to the VMIVME-7588 without designating the VMEbus interface apply to the product in any format.

The VMIVME-7588 programmer may quickly and easily control all the VMEbus functions simply by linking to a library of VMEbus interrupt and control functions. This library is located in VMIC's VMISFT-9420 IOWorks Access software for Windows NT users.

SECTION 2 - ABOUT THIS MANUAL

Because this product bridges the traditionally divergent worlds of Intel-based PCs and Motorola-based VMEbus controllers, some confusion over "conventional" notation and terminology may exist. We have made every effort to make this manual consistent by adhering to conventions typical for the Motorola / VMEbus world; nevertheless, users in both camps should review the following notes:

- Hexadecimal numbers are listed Motorola-style, prefixed with a dollar sign: $F79, for example. By contrast, this same number would be signified 0F79H according to the Intel convention, or 0xF79 by many programmers. Less common are forms such as $F79_h$ or the mathematician's $F79_{16}$.
- An 8-bit quantity is termed a "byte," a 16-bit quantity is termed a "word," and a 32-bit quantity is termed a "longword." The Intel convention is similar, although their 32-bit quantity is more often called a "double-word".
- Motorola programmers should note that Intel processors have an I/O bus that is completely independent from the memory bus. Every effort has been made in the manual to clarify this by referring to registers and logical entities in I/O space by prefixing I/O addresses as such. Thus, a register at "I/O $140" is not the same as a register at "$140," since the latter is on the memory bus while the former is on the I/O bus.
- Intel programmers should note that addresses are listed in this manual using a linear, "flat-memory" model rather than the old segment:offset model associated with Intel Real Mode programming. Thus, a ROM chip at a segment:offset address of C000:0 will be listed in this manual as being at address $C0000. For reference, here are some quick conversion formulas:

Segment:Offset to Linear Address

Linear Address = (Segment × 16) + Offset

Linear Address to Segment:Offset

Segment = ((Linear Address ÷ 65536) – *remainder*) × 4096

Offset = *remainder* × 65536

Where *remainder* = the fractional part of (Linear Address ÷ 65536)

Note that there are many possible segment:offset addresses for a single location. The formula above will provide a unique segment:offset address by forcing the segment to an even 64 Kbyte boundary, for example, $C000, $E000, etc. When using this formula, make sure to round the offset calculation properly!

SECTION 3 - VMIVME-7588 PRODUCT OPTIONS

VMIC's VMIVME-7588 is built around three fundamental hardware configurations. These involve processor power, DRAM memory, and interface. The Pentium processor-based CPU is available in 133, 150, 166, and 200 MHZ versions, while the DRAM memory is available in 8, 16, 32, and 64 Mbyte capabilities. These options are subject to change based on emerging technologies and availability of vendor configurations.

The current details and the comprehensive list of options available with the VMIVME-7588 are defined in the *Device Specification Sheet* available from your VMIC representative.

The interface configuration includes the option to attach a VMEbus interface as well as the option to add two on-board Ethernet controller options to the standard 10Base2 Ethernet port.

The VMIVME-7588 VMEbus interface is provided by the PCI-to-VMEbus bridge mezzanine built around the Tundra Semiconductor Corporation Universe VMEbus interface chip. The Universe provides a reliable high-performance 64-bit VMEbus-to-PCI interface in one design. The functions and programming of the Universe based VMEbus are addressed in detail in Volume II of this manual.

The optional Ethernet mezzanine allows the user to add both 10BaseT and 100BaseTx Ethernet functions to the standard 10Base2 Ethernet port of the VMIVME-7588.

SECTION 4 - REFERENCES

For the most up-to-date physical description and specifications for the VMIVME-7588, please refer to:

VMIC specification number 800-007588-000

The following books references pertain to the Tundra Universe based bridge option available in the VMIVME-7588:

VMEbus Interface Components Manual
Tundra Semiconductor Corporation
603 March Rd.
Kanata, Ontario
Canada, K2K 2M5
(613) 592-0714
FAX (613) 592-1320

PCI Bus Interface and Clock Distribution Chips
PLX Technology, Inc.
625 Clyde Avenue
Mountain View, CA 94043
(415) 694-2800
(415) 960-0479

There are many books widely available on the subject of general PC/AT use and programming. Some reference sources which may be particularly helpful in using or programming the VMIVME-7588 include:

Pentium® Family User's Manual: Architecture and Programming Manual
and the ***Pentium® Family User's Manual: Data Book***
Intel Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641

Intel Triton II 82430HX
PCI Set Preliminary Data Sheet
Intel Folsom
FM4-41
1900 Prairie City Road
Folsom, CA 95630-9598

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
FAX (503) 234-6762

Programmers Guide to the AMIBIOS
American Megatrends, Inc.
6145-F Northbelt Parkway
Norcross, GA 30071

The VMIC VMEbus interrupt and control function software library references include for Windows NT:

VMISFT-9420 IOWorks Access User's Guide
Doc. No. 520-009420-910

For a detailed description and specification of the VMEbus, please refer to:

VMEbus Specification Rev. C.1
and The VMEbus Handbook
VITA
VMEbus International Trade Association
7825 East Gelding Drive
No. 104
Scottsdale, AZ 85260
(602) 951-8866
FAX: (602) 951-0720
Internet: http://www.vita.com

SECTION 5 - VMIVME-7588 FEATURES

The VMIVME-7588 performs all the functions of a standard IBM PC/AT motherboard with the following features:

- Two-slot VMEbus 6U size
- High-performance Intel P54C Pentium processor
  - Available in speeds from 133 to 200 MHz
  - Standard 16 Kbyte internal cache
- Low-power VRE 3.5V design
- Up to 64 Mbyte of DRAM
- 512 Kbyte Synchronous Burst SRAM External (L2) Cache
- 64-bit PCI SVGA video graphics accelerator
  - 2 Mbyte of video DRAM
  - Resolutions up to 1280 x 1024, noninterlaced, 256 colors, and 75 Hz refresh rate
- Battery-backed clock/calendar
- Front panel reset switch and indicators for hard drive activity, power, status, and miniature speaker

- On-board ports for keyboard, mouse, EIDE hard drive, floppy drive, Ethernet, video, serial, parallel I/O, and Ultra/Fast/Wide SCSI
- Front panel “vital sign” indicators (power, EIDE hard drive activity, VMEbus SYSFAIL, and Ethernet status)

The VMIVME-7588 also supports standard PC/AT I/O features such as those listed in Table 1-1 on page 1-8. Figure 1-1 on page 1-7 also shows a block diagram of the VMIVME-7588 emphasizing the I/O features, including the optional PCI-to-VMEbus bridge option.

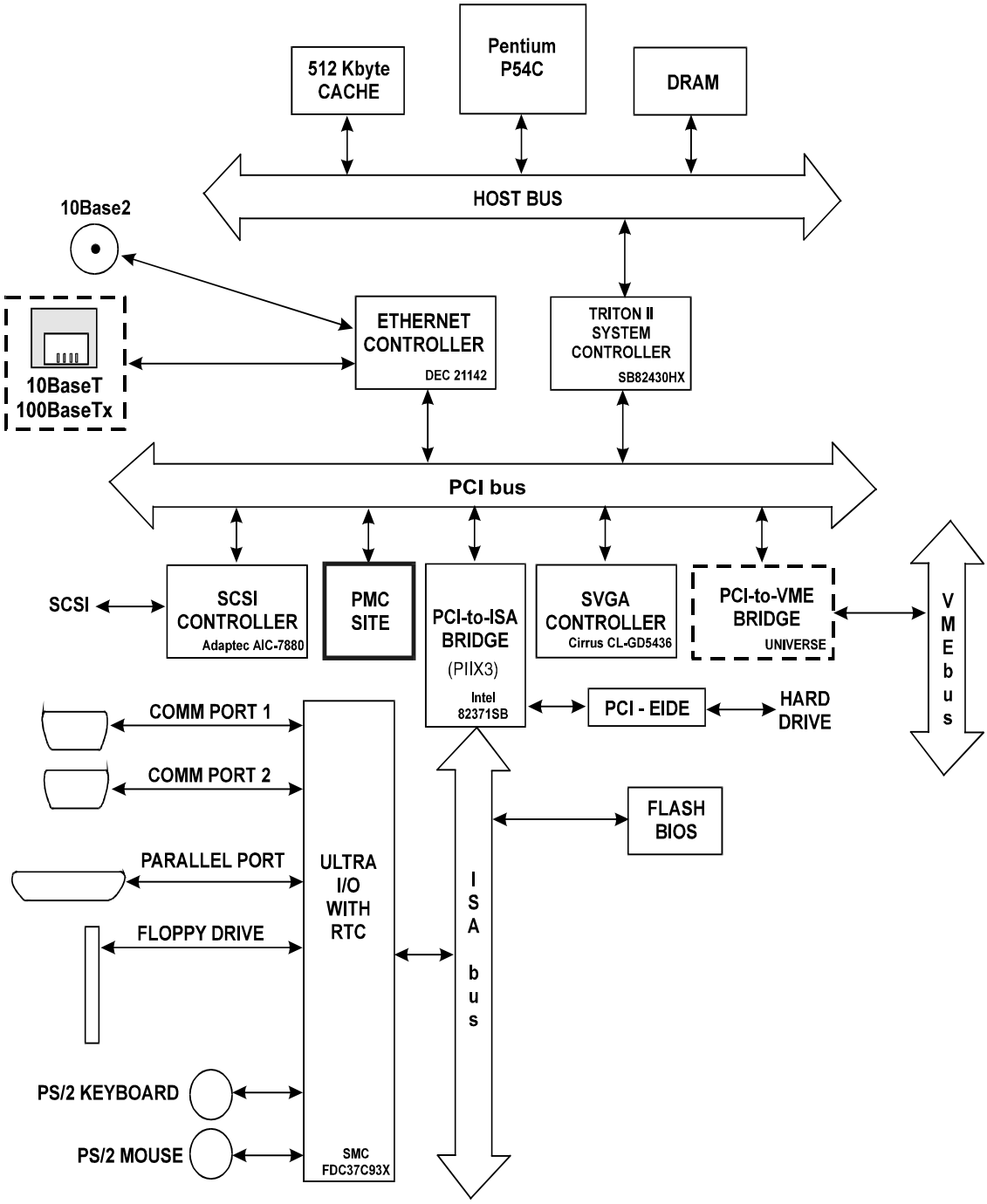


Figure 1-1 VMIVME-7588 Block Diagram

Table 1-1 PC/AT I/O Features

I/O FEATURE	IDENTIFIER	PHYSICAL ACCESS
Two Serial Ports (16550-compatible RS-232C)	COM1, COM2	Front Panel, DB-9 Male, RJ45 (RJ45 to DB-9 adaptor supplied)
One Parallel Port	LPT1	Front Panel DB25S (female)
AT-Style Keyboard Controller with PS/2-Style Adapter	KBD	Front Panel PS/2-Style Mini-DIN Circular (female)
PS/2-Style Mouse	MSE	Front Panel PS/2-Style Mini-DIN Circular (female)
Real-Time Clock/Calendar with Battery and Watchdog Timer	Date, Time	
Super VGA Video Controller with 2 Mbyte DRAM	Display	Front Panel DB15HD High Density (female)
Ethernet, 10BaseT, 10Base2 100BaseTx	Novell NE-2000 compatible	Front Panel BNC, RJ45
Floppy Disk Controller (two drive maximum)	Drives A, B	*34-pin Header Flat Cable Type
EIDE Fixed Disk Controller (two drive maximum)	Drives C, D	*40-pin Header Flat Cable Type
Ultra/Fast/Wide SCSI Controller	SCSI	Front Panel 68-Pin High Density Ultra Fast Wide SCSI
Hardware Reset	Cold Boot	Front Panel Pushbutton
IBM/PC Sound	Beep	Front Panel Speaker Port
LED Indicators	Power Status, Hard Drive Activity, and Ethernet Status	Front Panel

*Recommended length not to exceed 18”

SECTION 6 - VMEbus FEATURES

In addition to its PC/AT functions, the VMIVME-7588 has the following VMEbus features when purchased with the Universe based bridge option:

- Two-slot, 6U height VMEbus board
- Complete six-line Address Modifier (AM-Code) programmability
- 32-bit data interface with separate hardware byte/word swapping for master and slave accesses
- Support for VME64 multiplexed MBLT 64-bit VMEbus block transfers
- User-configured interrupter
- User-configured interrupt handler
- System Controller mode with programmable VMEbus arbiter (PRI, SGL, and RRS modes are supported)
- VMEbus BERR* bus error timer (software programmable)
- Slave access from the VMEbus to local RAM and mailbox registers
- Full-featured programmable VMEbus requester (ROR, RWD, and BCAP modes are supported)
- System Controller autodetection
- Complete VMEbus master access through five separate Protected-mode memory windows

Figure 1-2 shows the VMIVME-7588 functions in a typical VMEbus system. The VMIVME-7588 is a versatile double-board solution for VMEbus control with familiar PC/AT operation.

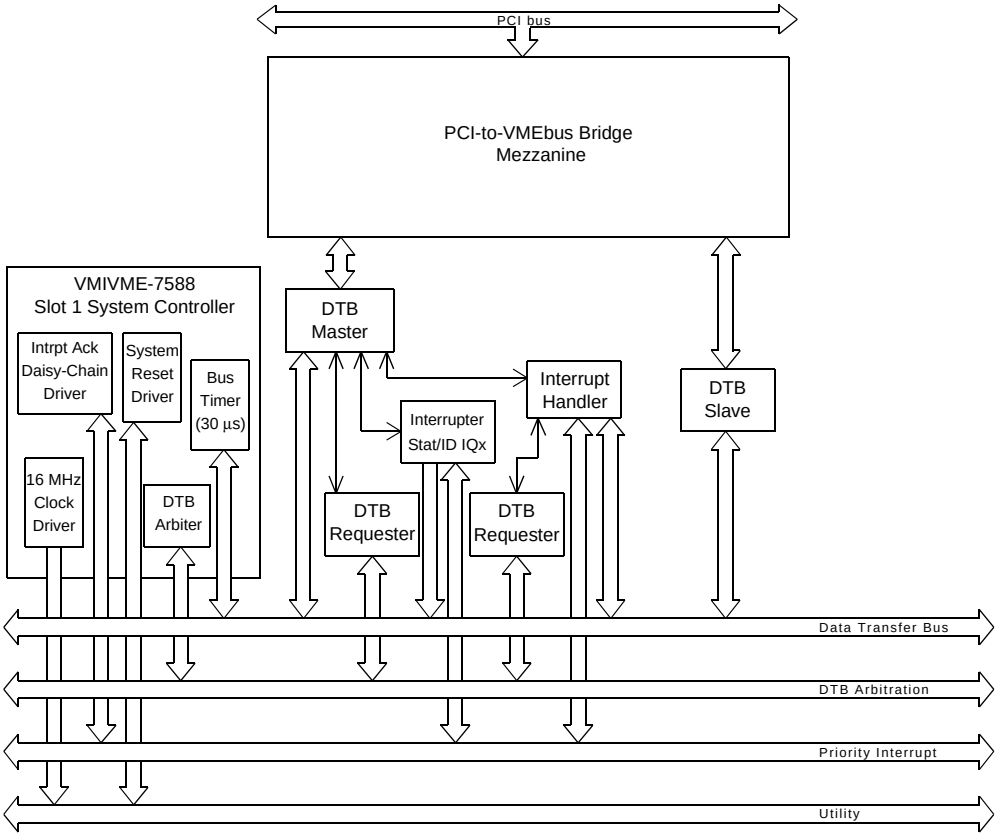


Figure 1-2 VMIVME-7588 VMEbus Functions

CHAPTER 2

INSTALLATION AND SETUP

IN THIS CHAPTER:

SECTION 1 - INTRODUCTION

This chapter describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup, and operation of the VMIVME-7588, the Pentium® processor-based VMEbus CPU, the PCI-to-VMEbus bridge option and the Tundra Universe-based interface.

SECTION 2 - UNPACKING PROCEDURES

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed

circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC Customer Service together with a request for advice concerning the disposition of the damaged item(s).

****
* CAUTION *
****

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. WHEN THE BOARD IS PLACED ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED.

SECTION 3 - HARDWARE SETUP

VMIVME-7588, The Pentium Processor-Based VMEbus CPU

The VMIVME-7588 is tested for system operation and shipped with factory-installed header jumpers. The physical location of the user-configurable jumpers and connectors for the CPU board are illustrated in Figure 2-1. The definitions of these jumpers and connectors are included in Table 2-1 through Table 2-5.

The physical location of the user-configurable jumpers and connectors for the I/O board are illustrated in Figure 2-2. The definitions of these jumpers and connectors are included in Table 2-6 through Table 2-11.

The default jumper condition of the VMIVME-7588 is expressed in Table 2-2 through Table 2-12 by bold text in the table cells.

****
* CAUTION *
****

ON THE CPU BOARD, THE SCSI JUMPER IS MODIFIED BY THE USER ONLY IF ULTRA SCSI OPERATION IS REQUIRED. ON THE I/O BOARD, THE COM PORT JUMPERS AND THE PASSWORD CLEAR JUMPER CAN BE MODIFIED BY THE USER.

ALL OTHER JUMPERS ARE FACTORY CONFIGURED AND SHOULD NOT BE MODIFIED BY THE USER.

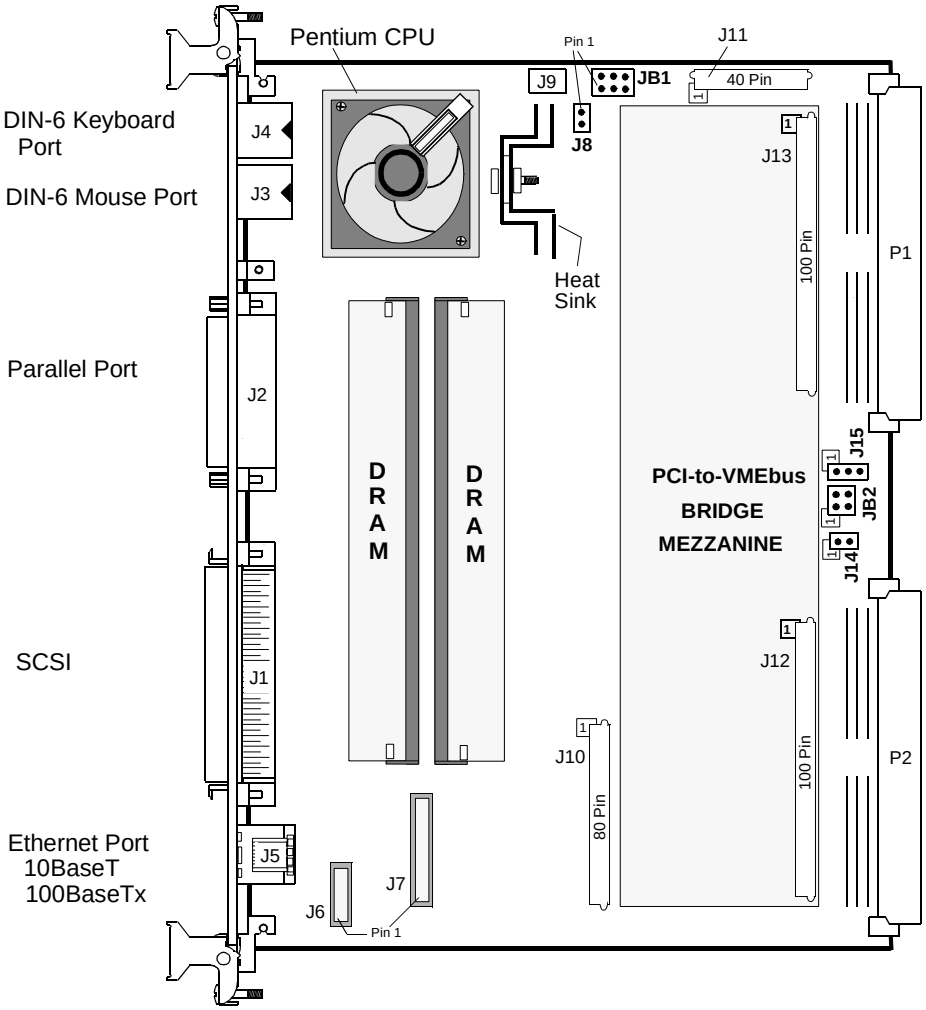


Figure 2-1 VMIVME-7588 CPU Board I/O Port and Jumper Locations

Table 2-1 CPU Board Connectors

Connector	Function
J1	SCSI Connector
J2	Parallel Port Connector
J3	PS/2 Mouse Connector
J4	PS/2 Keyboard Connector
J5	Ethernet Port: 10BaseT, 100BaseTx
J6, J7	100Mbyte Daughter Board Connectors
J9	CPU Fan Connector
J10, J11	I/O Board Connectors
J12, J13	PCI/VME Mezzanine Board Connectors
P1, P2	VME Connectors

NOTE:

MODIFYING THE RESERVED JUMPER IN TABLE 2-2 THROUGH TABLE 2-4 WILL VOID THE WARRANTY AND MAY DAMAGE THE UNIT.

Table 2-2 CPU Core / Bus Frequency Ratio - Jumper (JB1)

Speed Ratio	Jumper Setting
3 / 2 x	1-3, 2-4
2 x	3-5, 2-4
3 x	1-3, 4-6
5 / 2 x	3-5, 4-6

Table 2-3 CPU Bus Frequency Select - Jumpers (JB2 and J15)

CPU Bus Frequency (MHz)	Jumper JB2 1-2 Position	Jumper JB2 3-4 Position	Jumper J15 Position
66	Out	In	2-3
60	In	Out	1-2
50	In	In	2-3
Reserved	Out	Out	x

Table 2-4 CPU Voltage Select - Jumper (J8)

CPU Voltage	Jumper J8 1-2 Position
VR	Out
VRE	In

NOTE:

THE JUMPER SETTING IN TABLE 2-5, SCSI SPEED SELECT - JUMPER (J14), MAY REQUIRE MODIFICATION BASED UPON THE USER-DEFINED CONFIGURATION.

Table 2-5 SCSI Speed Select - Jumper (J14)

SCSI Speed	Jumper J14 1-2 Position
Ultra	Out
Fast	**In**

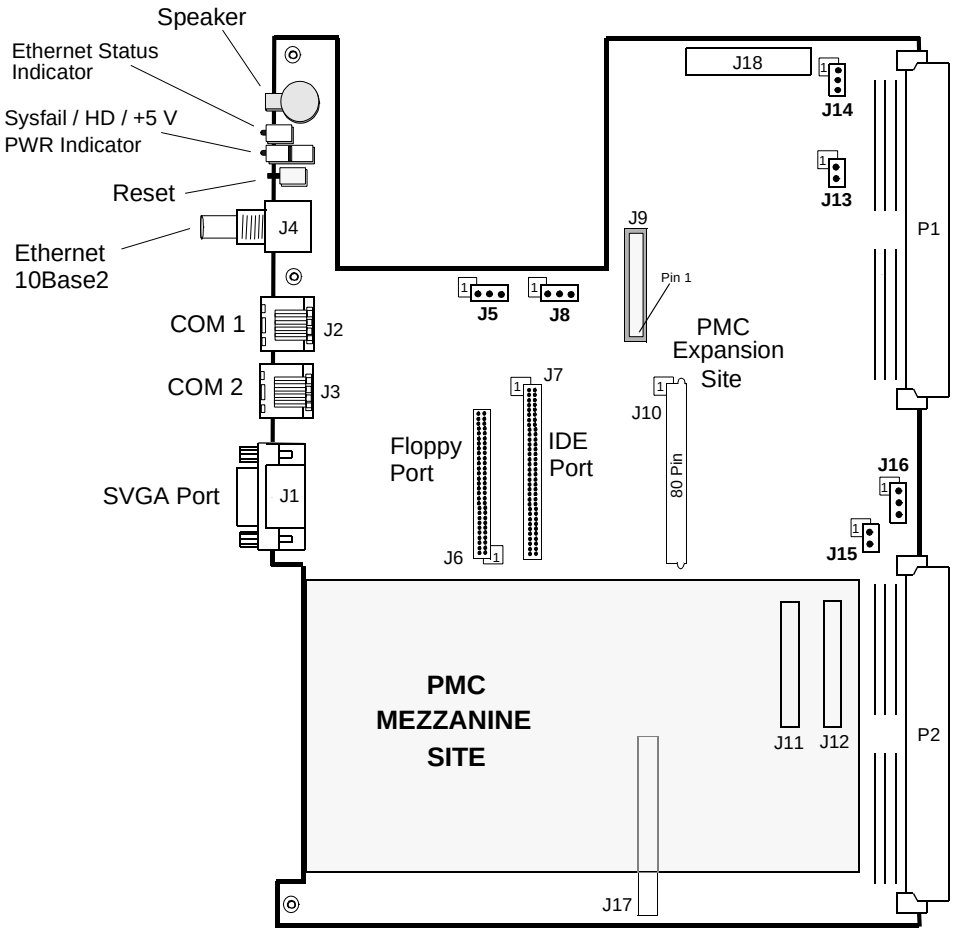


Figure 2-2 VMIVME-7588 I/O Board I/O Port Locations

Table 2-6 I/O Board Connectors

Connector	Function
J1	SVGA Connector
J3	COM 2 Connector
J2	COM 1 Connector
J4	10Base2 Connector
J6	Floppy Connector
J7	IDE Connector
J9	Port 80 Test Port Connector
J11, J12	PMC Connectors
J10	PMC Expansion Connector
J17, J18	CPU Board Connectors
P1, P2	VME Connectors

NOTE:

THE JUMPER SETTINGS IN TABLE 2-7 AND TABLE 2-8 MAY REQUIRE MODIFICATION BASED UPON THE USER-DEFINED CONFIGURATION.

Table 2-7 COM Port Status - Jumpers (J5 and J8)

Status Select	COM0 Jumper Position	COM1 Jumper Position
DCD	**1-2**	**1-2**
Ring Indicator	2-3	2-3

Table 2-8 Password Clear - Jumper (J13)

Password Clear	Jumper Position
Normal	**Out**
Clear Password	In

NOTE:

MODIFYING THE RESERVED JUMPER SETTINGS IN TABLE 2-9, TABLE 2-10, AND TABLE 2-11 WILL VOID THE WARRANTY AND MAY DAMAGE THE UNIT.

Table 2-9 Boot Block Select - Jumper (J14)

Boot Block	Jumper Position
Normal	**2-3**
Boot Block	1-2

Table 2-10 Reset Routing Select - Jumper (J15)

Reset Routing	Jumper Position
PCI -to- VME Bridge Installed	Out
No PCI -to- VME Bridge	IN

Table 2-11 PCI Clock Select - Jumper (J16)

PCI Clock	Jumper Position
33 / 30 MHz	2-3
25 MHz	1-2

VMIVME-7588, Tundra Universe Based PCI-to-VMEbus Bridge

The Tundra Universe based PCI-to-VMEbus bridge is tested for system operation and shipped with factory-installed header jumpers. The bridge is shipped with the CPU and I/O board as part of the VMIVME-7588. Figure 2-3 illustrates the physical location of the user-configurable jumpers and connectors on the bridge option. Table 2-12 lists each jumper designator, its function, and the factory-installed default configuration.

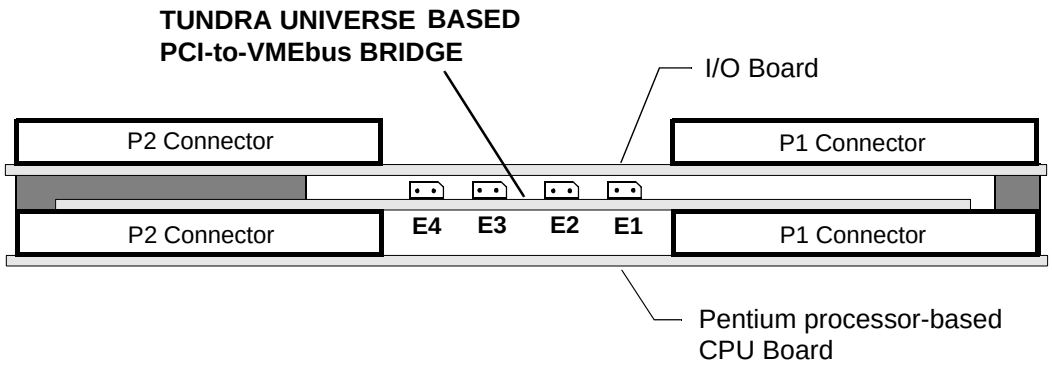


Figure 2-3 Jumper Locations on the Universe Based PCI-to-VMEbus Bridge (Rear View)

Table 2-12 Universe-Based PCI-to-VMEbus Bridge Jumper Functions and Factory Settings

JUMPER	FUNCTION	FACTORY SETTING
E1	Installed - Universe memory mapped Removed - Universe I/O mapped	Installed **(Should Not be Removed)**
E2	Installed - Receives VMEbus SYSRESET Removed - Does Not Receive	Installed
E3	Installed - Drives VMEbus SYSRESET Removed - Does not drive	Installed
E4	Installed - SYSFAIL Not asserted upon reset Removed - SYSFAIL Asserted upon reset	Installed

NOTE:

ANY OTHER JUMPER LOCATIONS ARE RESERVED FOR VMIC USE ONLY AND SHOULD NOT BE ALTERED FROM THE FACTORY DEFAULT SETTINGS.

SECTION 4 - INSTALLATION

The VMIVME-7588 conforms to the VMEbus physical specification for a 6U dual Eurocard (dual height, two-slot width). It can be plugged directly into any standard chassis accepting this type of board.

****
* CAUTION *
****

DO NOTE INSTALL OR REMOVE THE BOARD WHILE POWER IS APPLIED.

The following steps describe the VMIC recommended method for VMIVME-7588 installation and powerup:

1. Make sure power to the equipment is off.
2. If a drive module or other expansion module such as VMIC's VMIVME-7453 VMEbus Floppy / Hard Disk Module is to be used, connect it to the controller prior to board installation. Refer to the disk module manual. Recommended cable lengths of the floppy and EIDE are not to exceed 18".
3. Choose two chassis slots. The VMIVME-7588 must be attached to a dual P1 / P2 VMEbus backplane.

   If the VMIVME-7588 with the Universe-based PCI-to-VMEbus bridge is to be the VMEbus system controller, choose the first two VMEbus slots. If some other board is the VMEbus system controller, choose any slot *except* slot one. The Universe-based bridge requires no jumpers for enabling / disabling the system controller function.

   NOTE:

   THE VMIVME-7588 HAS AN OPERATING TEMPERATURE OF 0 TO 55 °C. IT IS ADVISABLE TO INSTALL BLANK PANELS OVER ANY EXPOSED VMEBUS SLOTS. THIS WILL ALLOW FOR BETTER AIR FLOW OVER THE VMIVME-7588 BOARD.

4. Insert the VMIVME-7588 and its attached expansion modules into the chosen VMEbus chassis slot (expansion modules should fill the slots immediately adjacent to the VMIVME-7588). While ensuring that the boards are properly aligned and oriented in the supporting board guides, slide the boards smoothly forward against the mating connector until firmly seated.

5. Connect all needed peripherals to the front panel. Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A. Minimally, a keyboard and a monitor are required if the user has not previously configured the system.
6. Apply power to the system. Several messages are displayed on the screen, including names, versions, and copyright dates for the various BIOS modules on the VMIVME-7588.
7. If a drive module was installed, the BIOS Setup program must be run to configure the drive types. The procedure varies according to the BIOS manufacturer. See Appendix C to properly configure the system.
8. If a drive module is present, install the operating system according to the manufacturer's instructions.

See Appendix B for instructions on installing VMIVME-7588 peripheral driver software during operating system installation.

SECTION 5 - FRONT PANEL CONNECTORS

Front panel connections for the parallel and video ports are typical for any PC/AT and clearly labeled. The keyboard and mouse connectors are standard mini-DIN PS/2 style connectors; an adapter is supplied to connect a keyboard with a larger connector to the VMIVME-7588. See Appendix A for connector pinouts and orientation.

SECTION 6 - LED STATUS DEFINITION

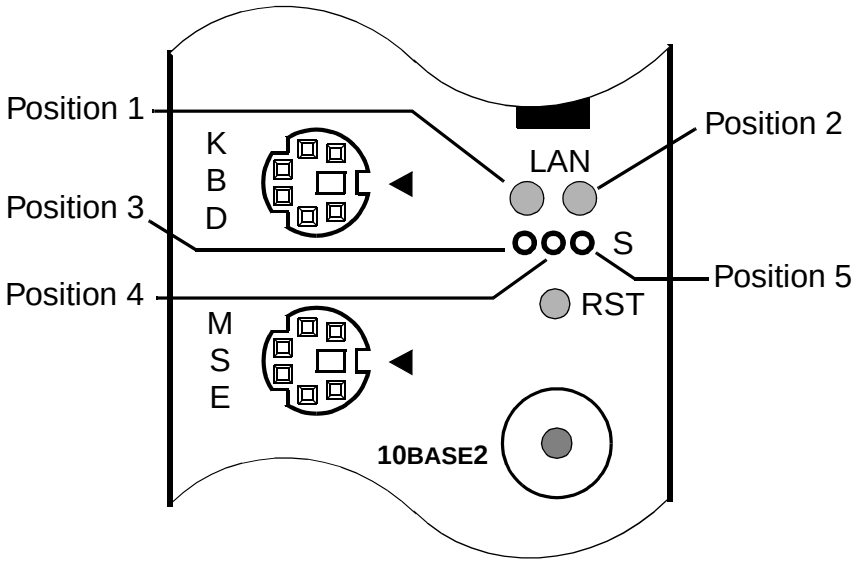


Figure 2-4 LED Position on the Front Panel

LED Definition

Position 1 - Ethernet Active - Indicates when the Ethernet is transmitting or receiving data.

Position 2 - Ethernet Link - *Yellow* indicates when the Ethernet is linked in 10BaseT or 10Base2 mode. *Green* indicates when the Ethernet is linked in 100BaseTx mode.

Position 3 - Power - Indicates when power is applied to the board.

Position 4 - Hard Drive Indicator - Indicates when hard drive activity is occurring.

Position 5 - SYSFAIL - Indicates when a VMEbus SYSFAIL is asserted.

SECTION 7 - PMC EXPANSION SITE

The PCI Mezzanine Card (PMC) site on the VMIVME-7588 allows expansion of the PCI bus for the use of such peripherals as the VMIPMC-5588 reflective memory board or other third-party PMC mezzanine boards. The PMC site on the VMIVME-7588 is attached to the primary (type 0) PCI bus.

The VMIVME-7588 supports Type I and Type II PMC specifications. Type I PMC specification allows the PMC board to extend through the front panel of the VMIVME-7588 for front panel connections and displays. The Type II PMC specification calls for the PMC board to be shorter than the Type I, thereby Enabling the PMC board to remain hidden behind the front panel of the VMIVME-7588. Figure 2-5 on page 2-12 shows where the two types of PMC expansion boards are mounted on the VMIVME-7588.

The PMC expansion site on the I/O board contains a keying pin that restricts the addition of a PMC board to a 5 V board only.

WARNING

THE PMC EXPANSION SITE ON THE VMIVME-7588 IS A 5 V SITE. DO NOT ATTEMPT TO PLACE A 3.3 V PMC BOARD IN THIS SITE. HARDWARE DAMAGE WILL OCCUR.

SECTION 8 - BIOS SETUP

The VMIVME-7588 has an on-board BIOS Setup program that controls many configuration options. These options are saved in a special nonvolatile, battery-backed memory chip and are collectively referred to as the board's "CMOS configuration." The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

The VMIVME-7588 is shipped from the factory with no hard drives configured in CMOS. The BIOS Setup program must be run to configure the specific drives attached.

Details of the VMIVME-7686 BIOS setup program are included in Appendix C.

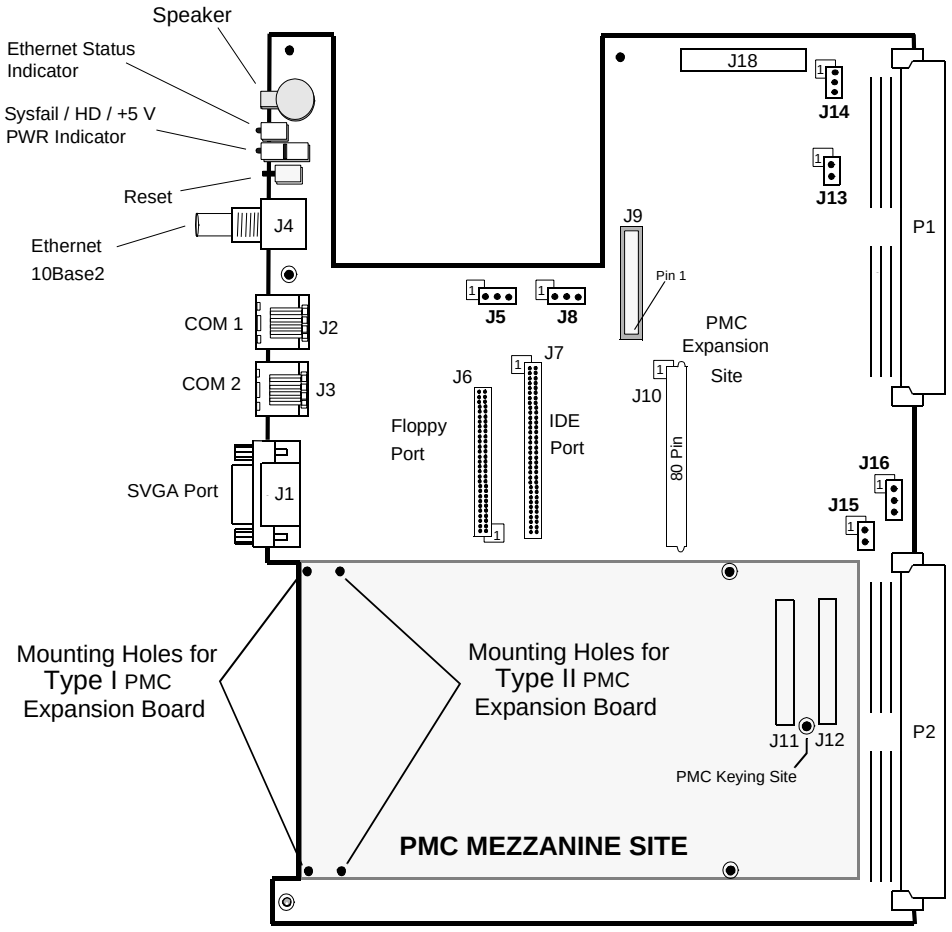


Figure 2-5 Type I and Type II PMC Expansion Mounting Sites on the I/O Board

CHAPTER

3

PC/AT FUNCTIONS

IN THIS CHAPTER:

SECTION 1 - CPU SOCKET

The VMIVME-7588 CPU socket is factory populated with a 133, 150, 166, or 200 MHz Pentium® processor. The CPU speed is a user-specified part of the VMIVME-7588 ordering information. The CPU speed is not user-upgradable. To change CPU speeds, contact customer service to receive a Return Material Authorization (RMA). For detailed information on the Pentium processor, please refer to the “Pentium Family User’s Manual.”

All CPU-associated jumpers are factory configured and should not be modified by the user. These configurations are outlined in this chapter.

SECTION 2 - PHYSICAL MEMORY

The VMIVME-7588 has two 72-pin SIMM sockets with options for factory-installed SIMM modules yielding a total of 8 Mbyte, 16 Mbyte, 32 Mbyte, 64 Mbyte, 128Mbyte, or 256 Mbyte as either parity or non-parity of DRAM. The memory modules are available in fast page mode rated at 70 ns or faster. Memory can be accessed as bytes, words, or longwords. Note that this memory is not user-upgradable. To upgrade this memory, contact VMIC's customer service to receive a Return Material Authorization (RMA).

All DRAM on the VMIVME-7588 is dual-ported to the VMEbus through the PCI-to-VME bridge. The memory is not only addressable by the local processor, but is also addressable through the VMEbus slave interface by another VMEbus master. Caution must be used when sharing memory between the local processor and the VMEbus to prevent a VMEbus master from overwriting the local processor's operating system.

The VMIVME-7588 includes both the system and video BIOS in a single 256 K x 8 FLASH.

The system portion of this ROM (at $E0000) is automatically shadowed, but for higher performance it is recommended that shadow RAM for the video BIOS be enabled from the Advanced CMOS Setup menu in BIOS Setup (see Appendix C).

SECTION 3 - MEMORY AND PORT MAPS

Memory Map - Tundra Universe-Based PCI-to-VMEbus Bridge

The memory map for the Tundra Universe-based interface (VMIVME-7588-xx0 and -xx1) is shown in Table 3-1. All systems share this same memory map, although a VMIVME-7588 with less than the full 64 Mbyte of DRAM does not fill the entire space reserved for On-Board Extended Memory.

Table 3-1 VMIVME-7588-xx0 and -xx1, Universe Based Interface Memory Address Map

MODE	MEMORY ADDRESS RANGE	SIZE	DESCRIPTION
PROTECTED MODE	$FFFF 0000 - $FFFF FFFF	64 Kbyte	ROM BIOS Image
	$0400 0000 - $FFFE FFFF	3.9 Gbyte	Unused *
	$0010 0000 -$03FF FFFF	63 Mbyte	Reserved for ** On-Board Extended Memory (not filled on all systems)
REAL MODE	$E0000 - $FFFFF	128 Kbyte	ROM BIOS
	$D0000 - $DFFFF	64 Kbyte	Unused
	$C8000 - $CFFFF	32 Kbyte	SCSI
	$C0000 - $C7FFF	32 Kbyte	Video ROM
	$A0000 - $BFFFF	128 Kbyte	Video RAM
	$00000 - $9FFFF	640 Kbyte	User RAM/DOS RAM

* This space can be used to set up Protected mode PCI-to-VMEbus windows (Also referred to as PCI slave images).

** This space can be allocated as shared memory (i.e. shared between Pentium processor-based CPU and the VMEbus master). Note, that if a PMC Card is loaded, the expansion BIOS may be placed in this area.

I/O Port Map

The Pentium processor-based CPU has special input/output instructions that access I/O peripherals residing in I/O addressing space (which is separate and distinct from memory addressing space). Locations in I/O address space are often referred to as *ports*. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00-A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU has an independent 64 Kbyte I/O address space which is accessible as bytes, words, or longwords.

Standard PC/AT hardware circuitry reserves only 1,024 bytes of I/O addressing space from I/O $000–$3FF for peripherals. All standard PC I/O peripherals such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers, and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly, so beware of adjusting these I/O ports directly.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 3-2.

Table 3-2 VMIVME-7588 I/O Address Map

I/O ADDRESS RANGE	SIZE IN BYTES	HARDWARE DEVICE	PC/AT FUNCTION
$000 - $00F	16		DMA Controller 1 (Intel 8237A Compatible)
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller (Intel 8259A Compatible)
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer (Intel 8254 Compatible)
$044 - $05F	30		Reserved
$060 - $064	5		Keyboard, Speaker, Eqpt. Config (Intel 8042 Compatible)
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock, NMI Mask
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20 / Fast Reset Register
$093	1		Reserved
$094	1	Super VGA Chip	POS102 Access Control Register
$095 - $09F	11		Reserved
$0A0 - $0A1	2		Slave Interrupt Controller (Intel 8259A Compatible)
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2 (Intel 8237A Compatible)
$0E0 - $16F	142		Reserved
$170 - $177	8	PIIX3	Secondary Hard Disk Controller
$178 - $1EF	120		**User I/O**
$1F0 - $1F7	8	PIIX3	Primary Hard Disk Controller
$1F8 - $277	128		**User I/O**

Table 3-2 VMIVME-7588 I/O Address Map (Continued)

I/O ADDRESS RANGE	SIZE IN BYTES	HARDWARE DEVICE	PC/AT FUNCTION
$278 - $27F	8	I/O Chip*	LPT2 Parallel I/O*
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	UART*	COM4 Serial I/O*
$2EF - $2F7	9		**User I/O**
$2F8 - $2FE	7	Ultra I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Ultra I/O Chip	Secondary Floppy Disk Controller
$378 - $37F	8	Ultra I/O Chip	LPT1 Parallel I/O
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	UART*	COM3 Serial I/O*
$3F0 - $3F7	8	Ultra I/O Chip	Primary Floppy Disk Controller
$3F8 - $3FE	7	Ultra I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF	1		Reserved

* While these I/O ports are reserved for the listed functions, they are not implemented on the VMIVME-7588. They are listed here to make the user aware of the standard PC/AT usage of these ports.

SECTION 4 - PC/AT INTERRUPTS

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 3-3 along with their functions. Table 3-4 on page 3-8 details the vectors in the interrupt vector table.

Table 3-3 PC/AT Hardware Interrupt Line Assignments

IRQ	AT FUNCTION	COMMENTS
NMI	Parity Errors (Must be enabled in BIOS Setup)	**Used by VMIVME-7588 VMEbus Interface**
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2 / COM4	
4	COM1 / COM3	
5	LPT2	Determined by BIOS
6	Floppy Controller	
7	LPT1	
8	Real-Time Clock	
9	Old IRQ2	SVGA or Network I/O
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Not Assigned	Determined by BIOS
13	Math Coprocessor	
14	AT Hard Drive	
15	Not Assigned	Determined by BIOS

Table 3-4 PC/AT Interrupt Vector Table

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, VMEbus Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Ethernet	General Protection Violation
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	LPT1 Parallel I/O	Unassigned
10	16		BIOS Video I/O	Coprocessor Error
11	17		Eqpt Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26	IRQ8	Real-Time Clock	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode

Table 3-4 PC/AT Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-71	103-113		Reserved by DOS	Same as Real Mode
72	114	IRQ10		
73	115	IRQ11		
74	116	IRQ12		
75	117	IRQ13		
76	118	IRQ14		
77	119	IRQ15		
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

The maskable interrupts are prioritized in hardware by the equivalent of two cascaded Intel 8259A Priority Interrupt Controller (PIC) chips. At boot-up time, the BIOS writes to each PIC an 8-bit vector that maps each Interrupt Request line (IRQx) to its corresponding interrupt vector in memory. Also at boot-up time, the correct 32-bit interrupt vector must be loaded at the right place in the interrupt table. Later, when the IRQx line is acknowledged, the CPU reads the 8-bit vector returned by the PIC, multiplies it by four to create an index into the interrupt table, then retrieves the 32-bit (segment:offset) pointer from the table. The CPU uses that pointer to branch to the interrupt service routine corresponding to the IRQx line.

The interrupt hardware implementation on the VMIVME-7588 is standard for computers built around the PC/AT architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

SECTION 5 - PCI INTERRUPTS

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal.

PCI defines one interrupt line for a single function device, such as a SCSI, and up to four interrupt lines for a multifunction device or connector, such as the PCI Mezzanine Card (PMC). For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 3-1 on page 3-12 depicts the VMIVME-7588 interrupt logic pertaining to VMEbus operations and the PMC mezzanine expansion card.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line or each may have its own (up to a maximum of four functions) or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the VMEbus interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

The PCI-to-VME Bridge has the capability of generating a Non-Maskable Interrupt (NMI) via the PCI SERR# line. The SERR interrupt is routed through certain logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable / disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable / enable all NMI sources. Table 3-5 and Table 3-6 describe the register bits that are used by the NMI.

Table 3-5 NMI Status Control Register Bit Description

NMI Status Control Register (I/O Address $061, Read/Write, Read Only)	
Bit 7	SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set bit 2 to 0 and then set it to 1. When writing to port $061, bit 7 must be 0.
Bit 2	PCI SERR# Enable (Read/Write) - 1 = Clear and Disable, 0 = Enable

Table 3-6 NMI Enable and Real-Time Clock Address Register Bit Description

NMI Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)	
Bit 7	NMI Enable - 1 = Disable, 0 = Enable

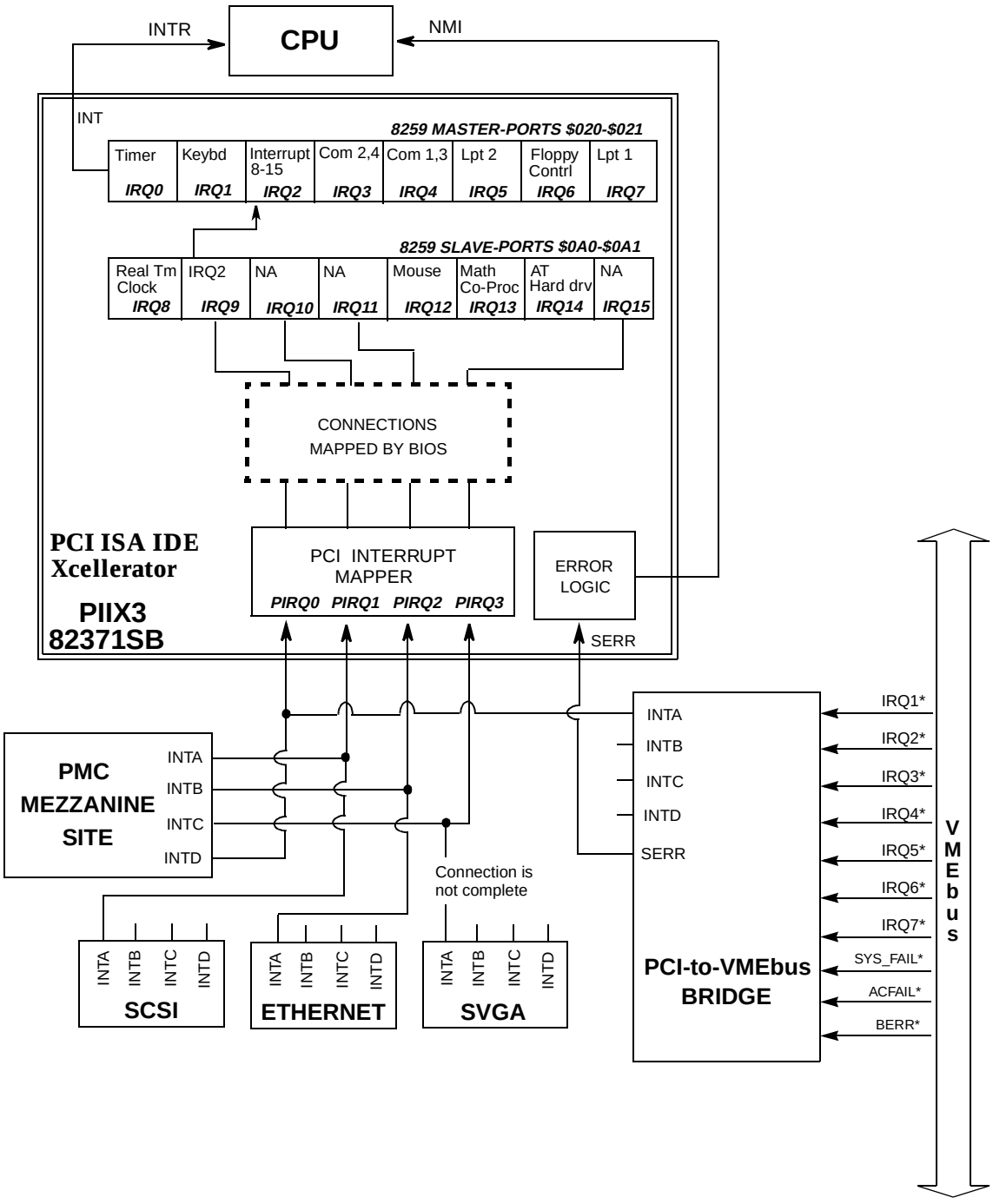


Figure 3-1 Connections for the PC Interrupt Logic Controller

SECTION 6 - I/O PORTS

The VMIVME-7588 incorporates the SMC Ultra-I/O chip. This chip provides the VMIVME-7588 with a standard floppy drive controller, two 16550 UART compatible serial ports, and one standard Centronics parallel port. The Intel PIIX 3 chip provides the standard EIDE hard drive interface. All ports are present in their standard PC/AT locations, using default interrupts.

SECTION 7 - VIDEO GRAPHICS ADAPTER

The monitor port on the VMIVME-7588 is controlled by a Cirrus Logic CL-GD5436 chip with 2 Mbyte video DRAM. The video controller chip is hardware and BIOS compatible with the IBM EGA and SVGA standards and also supports VESA high-resolution and extended video modes. Table 3-7 shows the graphics video modes supported by the Cirrus Logic video chip.

Table 3-7 Supported Graphics Video Resolutions

SCREEN RESOLUTION	MAXIMUM COLORS	REFRESH RATES
640 x 480	256, 64 K, 16 M	60 Hz, 72 Hz, 75 Hz
800 x 600	256, 64 K, 16 M + A	56 Hz, 60 Hz, 72 Hz, 75 Hz
1024 x 768 (Interlaced)	256, 32 K, 64 K	43.5 Hz (Interlaced to 87 Hz)
1024 x 768	256, 32 K, 64 K	60 Hz, 70 Hz, 75 Hz
1280 x 1024	16, 256	43 Hz
1280 x 1024	256	60 Hz, 72 Hz, 75 Hz

Note that not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 60 Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

The VMIVME-7588's processor has 32-bit access to video memory with no-wait states. Video I/O registers are accessed using PCI bus. In addition,

the Cirrus Logic video controller supports up to a 64 x 64 pixel hardware cursor.

Floppy disks supplied with the VMIVME-7588 contain video drivers for Windows and other popular programs and operating systems. Follow the instructions on the floppy disk label to install the drivers using an interactive installation program.

SECTION 8 - SCSI CONTROLLER

The Small Computer System Interface (SCSI) is provided on the VMIVME-7588. Both Fast Wide-SCSI and Ultra-SCSI are implemented on the VMIVME-7588 system using Adaptec's AIC-7880 PCI-based SCSI controller. The SCSI architecture supports 8-bit (narrow) or 16-bit (wide) SCSI, for external SCSI devices. Ultra-SCSI provides faster disk access than a traditional disk interface, supporting a synchronous transfer rate of up to 40 Mbyte per second. In this manual, the Ultra/Fast/Wide SCSI is generically referred to as SCSI.

Internally, the SCSI bus is actively terminated; therefore, there are no peripherals located on the internal SCSI bus. The SCSI bus does provide external expansion to accommodate single-ended Ultra or Fast Wide SCSI devices such as external peripherals, plotters, scanners, and CD-ROM drives. Up to 15 external SCSI devices can be accommodated. The external Fast SCSI bus must be terminated at the last external SCSI device with an active, single-ended terminator.

The cable from the external devices attaches to the VMIVME-7588 with a 68-pin Micro D-SUB connector. The cable can be a maximum of 19 feet 10 inches, and the recommended impedance is 90 Ω. The SCSI connector and pinout is shown in Appendix A.

Selection between Ultra and Fast SCSI operation is done by configuring the J14 jumper on the VMIVME-7588 CPU Board. Reference Figure 2-1 and Table 2-5 for board location and setting information. Also, the user must set the proper SCSI BIOS parameters as shown in Appendix D.

SECTION 9 - ETHERNET CONTROLLER

The network capability is provided by the Digital Semiconductor's 21142. This Ethernet controller is PCI bus based and is software configurable. The VMIVME-7588 supports 10Base2 Ethernet as a standard onboard interface with 10BaseT and 100BaseTx Ethernet options available on a plug and play mezzanine.

10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ-45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 meters from the wiring hub to the end node. The Ethernet 10BaseT connector is shown in Appendix A on page A-2.

10Base2

The VMIVME-7588 also supports the 10Base2 (thin Ethernet) type connector for the Ethernet. This type of Ethernet connection requires a thin (RG58) coaxial cable and has a maximum segment length of 185 meters.

100BaseTx

The VMIVME-7588 (-xx1 and -xx4) supports the 100BaseTx Ethernet. A network based on 100BaseTx standard uses unshielded twisted-pair cables. The RJ-45 connector is used with the 100BaseTx standard, and the 100BaseTx has a maximum length of 250 meters.

CHAPTER

4

MAINTENANCE

IN THIS CHAPTER:

SECTION 1 - MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

APPENDIX

A

CONNECTOR PINOUTS

IN THIS APPENDIX:

SECTION 1 - INTRODUCTION

The VMIVME-7588 PC/AT Compatible VMEbus Controller has several connectors for its many I/O ports. Figure A-1 on page A-2 and Figure A-2 on page A-3 show the locations of the connectors on the VMIVME-7588. Wherever possible, the VMIVME-7588 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a minimum of confusion.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a VMEbus chassis.

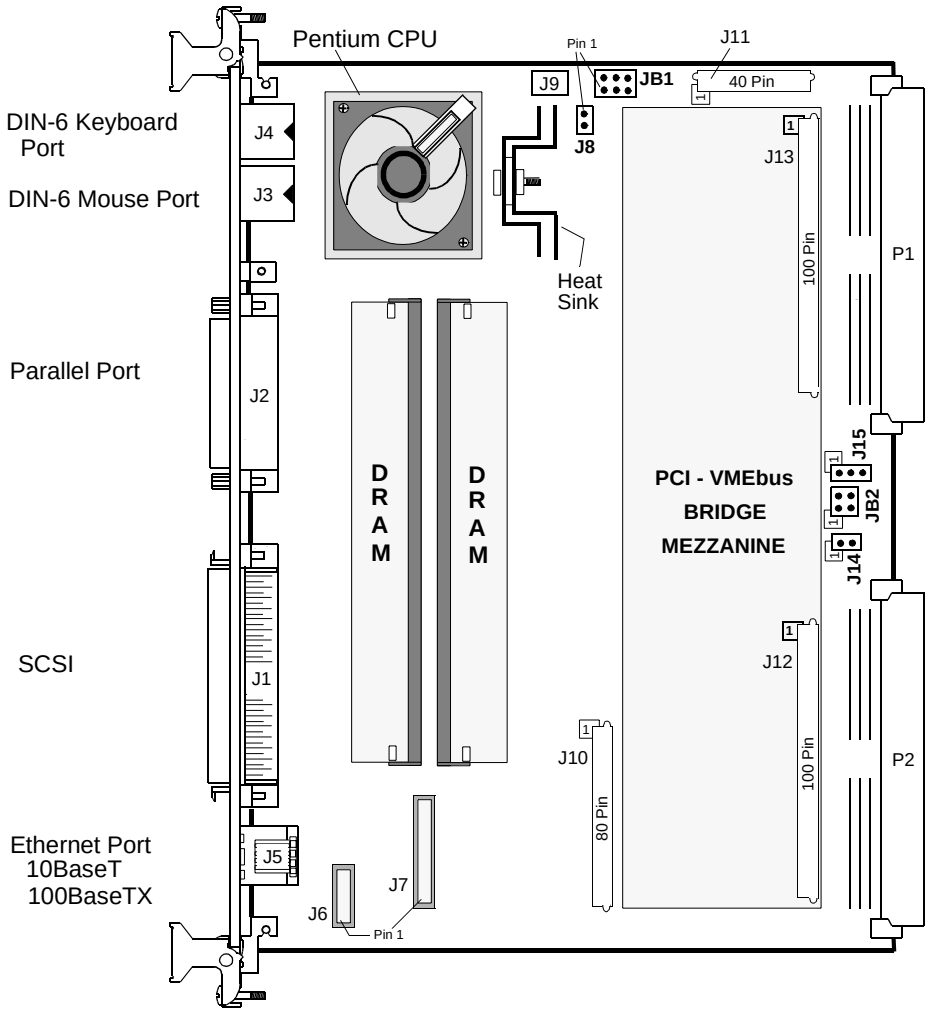


Figure A-1 VMIVME-7588 CPU Board Connector Locations

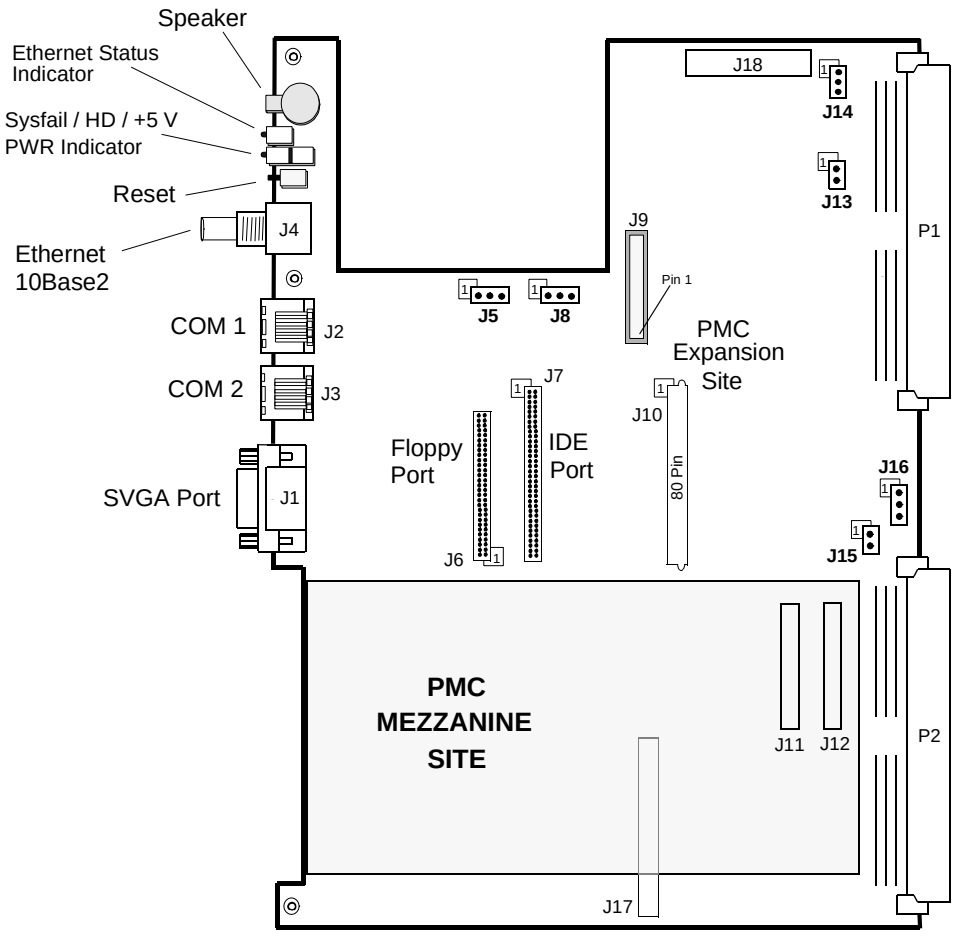


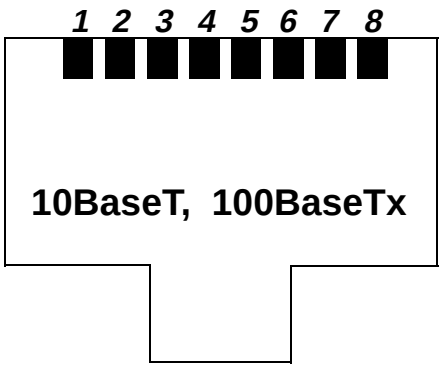
Figure A-2 VMIVME-7588 I/O Board Connector Locations

NOTE:

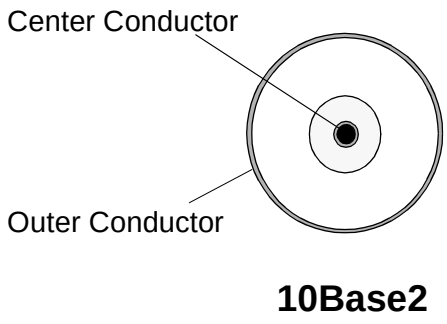
THE PMC EXPANSION CONNECTORS ARE NOT LOADED ON CERTAIN VERSIONS OF THE VMIVME-7588.

SECTION 2 - ETHERNET CONNECTOR PINOUT

The pinout diagram for the Ethernet 10BaseT, 100BaseTx, and 10Base2 connectors are shown in Figure A-3.



ETHERNET CONNECTOR (10BaseT, 100BaseTx)		
PIN	**Signal Name**	
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	NC	No Connection
5	NC	No Connection
6	RD-	Receive Data
7	NC	No Connection
8	NC	No Connection

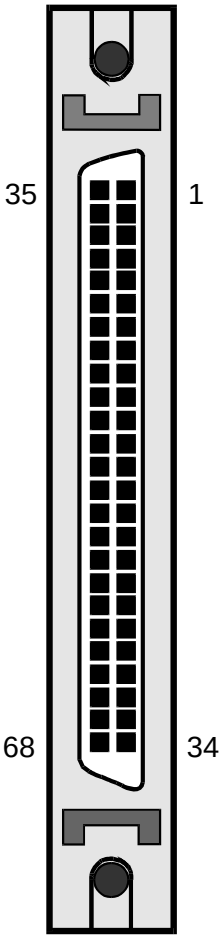


ETHERNET CONNECTOR (10Base2)	
PIN	**Signal Name**
Center Conductor	Data
Outer Conductor	Ground

Figure A-3 Ethernet Connector Pinout

SECTION 3 - SCSI CONNECTOR PINOUT

The SCSI connector is a 68-pin Micro D-SUB with a pinout illustrated in the following figure.

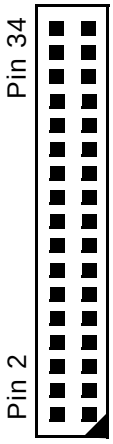


Pin	Signal Name	
1-16, 20-34, 49, 50, 54, 56	Ground	GND
40	Command Data Bus 0	SSCD0
41	Command Data Bus 1	SSCD1
42	Command Data Bus 2	SSCD2
43	Command Data Bus 3	SSCD3
44	Command Data Bus 4	SSCD4
45	Command Data Bus 5	SSCD5
46	Command Data Bus 6	SSCD6
47	Command Data Bus 7	SSCD7
48	Command Data Bus Parity	SSCDP#
17-18 51-52	Terminator Power	TERMPWR
55	Bus Attention	SATN#
57	Bus Busy	SBSY#
58	Bus Acknowledge	SACK#
59	Bus Reset	SRESET#
60	Bus Message	SMSG#
61	Bus Select	SSEL#
62	Bus Command	SCD#
63	Bus Request	SREQ#
64	Input/Output	SIO#
19, 53	No Connect	-
35	Data Bus 12	SSCD12
36	Data Bus 13	SSCD13
37	Data Bus 14	SSCD14
38	Data Bus 15	SSCD15
39	Data Bus Parity High	SSCDPH#
65	Data Bus 8	SSCD8
66	Data Bus 9	SSCD9
67	Data Bus 10	SSCD10
68	Data Bus 11	SSCD11

Figure A-4 SCSI Connector Pinout

SECTION 4 - FLOPPY DRIVE CONNECTOR PINOUT

The floppy drive connector is a dual-row 34-pin header connector. Pin 1 marks the beginning of the odd-numbered row. Most standard PC-compatible floppy disk drives use this pinout, which is shown in Figure A-5. The user should exercise caution to not misalign the floppy drive connector and cable.

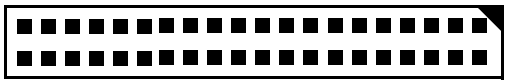


FLOPPY DRIVE CONNECTOR		
PIN	**DIRECTION**	**FUNCTION**
1		Ground
2	From Controller	Drive Density 0 (not connected on some controllers)
3		Ground
4		Reserved
5		Ground
6	From Controller	Drive Density 1 (not connected on some controllers)
7		Ground
8	From Drive	Index
9		Ground
10	From Controller	Motor Enable A
11		Ground
12	From Controller	Drive Select B
13		Ground
14	From Controller	Drive Select A
15		Ground
16	From Controller	Motor Enable B
17		Ground
18	From Controller	Step Motor Direction
19		Ground
20	From Controller	Step Pulse
21		Ground
22	From Controller	Write Data
23		Ground
24	From Controller	Write Enable
25		Ground
26	From Drive	Track 0
27		Ground
28	From Drive	Write Protect
29		Ground
30	From Drive	Read Data
31		Ground
32	From Controller	Select Head 1
33		Ground
34	From Drive	Disk Change

Figure A-5 Floppy Drive Connector Pinout

SECTION 5 - EIDE HARD DRIVE CONNECTOR PINOUT

Figure A-6 describes the pin assignment for the 40-pin EIDE / ATA hard drive header connector. Like the floppy header connector it has an odd-numbered row and an even-numbered row. The user should exercise caution to not misalign the hard drive connector and cable.



Pin 40 Pin 2

PIN	DIRECTION	DESCRIPTION	PIN	DIRECTION	DESCRIPTION
1	Out	Reset Drive	2	Out	Signal Ground
3	In/Out	Bidirectional Data 07	4	In/Out	Bidirectional Data 08
5	In/Out	Bidirectional Data 06	6	In/Out	Bidirectional Data 09
7	In/Out	Bidirectional Data 05	8	In/Out	Bidirectional Data 10
9	In/Out	Bidirectional Data 04	10	In/Out	Bidirectional Data 11
11	In/Out	Bidirectional Data 03	12	In/Out	Bidirectional Data 12
13	In/Out	Bidirectional Data 02	14	In/Out	Bidirectional Data 13
15	In/Out	Bidirectional Data 01	16	In/Out	Bidirectional Data 14
17	In/Out	Bidirectional Data 00	18	In/Out	Bidirectional Data 15
19	Out	Signal Ground	20	None	Unused, Keying Position
21		Reserved	22	Out	Signal Ground
23	Out	Write Strobe	24	Out	Signal Ground
25	Out	Read Strobe	26	Out	Signal Ground
27		Reserved	28	Out	Address Latch Enable
29		Reserved	30	Out	Signal Ground
31	In	Interrupt Request #14	32	In	16-bit Data Word Size
33	Out	Address Line #1	34	In	Diagnostic Test Passed
35	Out	Address Line #0	36	Out	Address Line #2
37	Out	Chip Select #0	38	Out	Chip Select #1
39	In	Slave/Activity Status	40	Out	Signal Ground

Figure A-6 EIDE Hard Drive Connector Pinout

SECTION 6 - PMC CONNECTOR PINOUT

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Figure A-7 shows the PMC connector and pinout. Table A-1 describes the pins and gives the respective name for each pin.

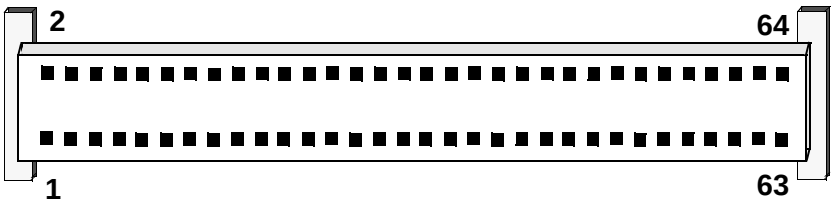


Figure A-7 PMC Connector

Table A-1 PMC Connector Pin Description

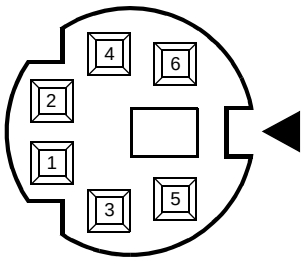
PMC CONNECTOR (J7)				PMC CONNECTOR (J8)			
LEFT SIDE		RIGHT SIDE		LEFT SIDE		RIGHT SIDE	
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	TCK	2	-12 V	1	+12 V	2	TRST#
3	GND	4	INTA#	3	TMS	4	TDO
5	INTB#	6	INTC#	5	TDI	6	GND
7	PRSNT1	8	+5 V	7	GND	8	NC
9	INTD#	10	NC	9	NC	10	NC
11	GND	12	NC	11	PRSNT2	12	+3.3 V
13	CLK	14	GND	13	RST#	14	GND
15	GND	16	GNT#	15	+3.3 V	16	GND
17	REQ#	18	+5 V	17	NC	18	GND
19	+5 V	20	AD[31]	19	AD[30]	20	AD[29]
21	AD[28]	22	AD[27]	21	GND	22	AD[26]
23	AD[25]	24	GND	23	AD[24]	24	+3.3 V
25	GND	26	C/BE3#	25	IDSEL	26	AD[23]
27	AD[22]	28	AD[21]	27	+3.3 V	28	AD[20]
29	AD[19]	30	+5 V	29	AD[18]	30	GND

Table A-1 PMC Connector Pin Description (Continued)

PMC CONNECTOR (J7)				PMC CONNECTOR (J8)			
LEFT SIDE		RIGHT SIDE		LEFT SIDE		RIGHT SIDE	
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
31	+5 V	32	AD[17]	31	AD[16]	32	C/BE2#
33	FRAME#	34	GND	33	GND	34	NC
35	GND	36	IRDY#	35	TRDY#	36	+3.3 V
37	DEVSEL#	38	+5 V	37	GND	38	STOP#
39	GND	40	LOCK#	39	PERR#	40	GND
41	SDONE	42	SB0#	41	+3.3 V	42	SERR#
43	PAR	44	GND	43	C/BE1#	44	GND
45	+5 V	46	AD[15]	45	AD[14]	46	AD[13]
47	AD[12]	48	AD[11]	47	GND	48	AD[10]
49	AD[9]	50	+5 V	49	AD[8]	50	+3.3 V
51	GND	52	C/BE0#	51	AD[7]	52	NC
53	AD[6]	54	AD[5]	53	+3.3 V	54	NC
55	AD[4]	56	GND	55	NC	56	GND
57	+5 V	58	AD[3]	57	NC	58	NC
59	AD[2]	60	AD[1]	59	GND	60	NC
61	AD[0]	62	+5 V	61	ACK64#	62	+3.3 V
63	GND	64	REQ64#	63	GND	64	NC

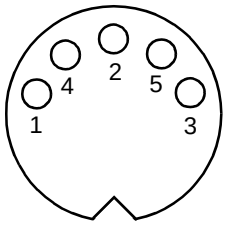
SECTION 7 - KEYBOARD CONNECTOR PINOUT

The keyboard connector is a standard 6-pin female mini-DIN PS/2 style connector shown in Figure A-8; an adapter is supplied to connect a keyboard with a larger PC/AT-style connector to the VMIVME-7588. The PC/AT-style connector pinout is shown in Figure A-9.



KEYBOARD CONNECTOR		
PIN	**DIR**	**FUNCTION**
1	In/Out	Data
2		Reserved
3		Ground
4		+5 V
5	Out	Clock
6		Reserved
Shield		Chassis Ground

Figure A-8 Keyboard Connector Pinout

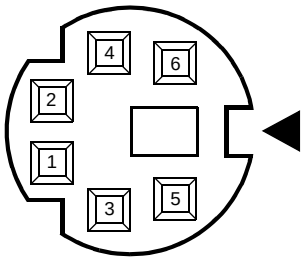


KEYBOARD CONNECTOR	
PIN	**FUNCTION**
1	+ Keyboard Clock (+5 VDC Signal Level)
2	+ Keyboard Data (+5 VDC Signal Level)
3	Free
4	Ground
5	+5 VDC

Figure A-9 PC/AT Keyboard Connector Pinout

SECTION 8 - MOUSE CONNECTOR PINOUT

The mouse connector is a standard 6-pin female mini-DIN PS/2 style connector shown in Figure A-10.

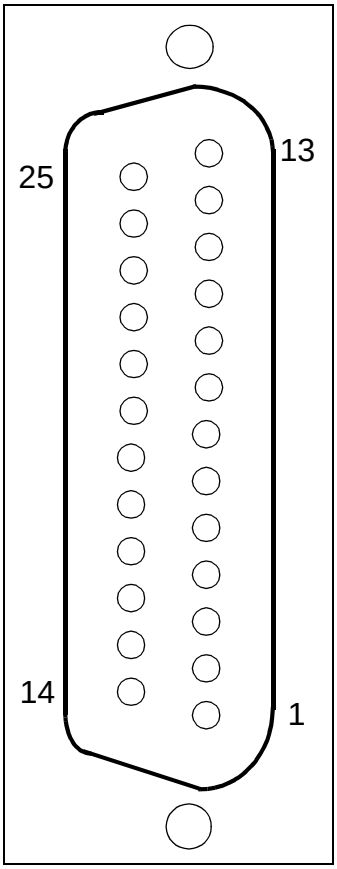


MOUSE CONNECTOR		
PIN	**DIR**	**FUNCTION**
1	In/Out	Data
2		Reserved
3		Ground
4		+5 V
5	Out	Clock
6		Reserved
Shield		Chassis Ground

Figure A-10 Mouse Connector Pinout

SECTION 9 - PARALLEL PORT CONNECTOR PINOUT

The printer port shown in Figure A-11 uses a D25 female connector typical of any PC / AT system.

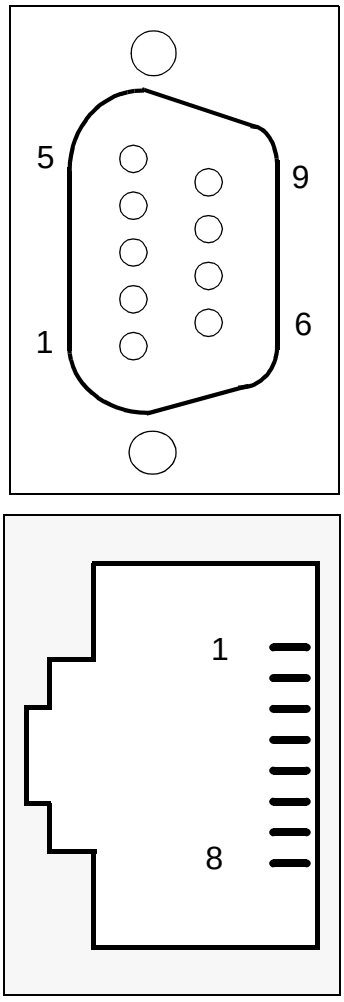


PARALLEL PORT CONNECTOR		
PIN	**DIRECTION**	**FUNCTION**
1	In/Out	Data Strobe
2	In/Out	Bidirectional Data D0
3	In/Out	Bidirectional Data D1
4	In/Out	Bidirectional Data D2
5	In/Out	Bidirectional Data D3
6	In/Out	Bidirectional Data D4
7	In/Out	Bidirectional Data D5
8	In/Out	Bidirectional Data D6
9	In/Out	Bidirectional Data D7
10	In	Acknowledge
11	In	Device Busy
12	In	Out of Paper
13	In	Device Selected
14	Out	Auto Feed
15	In	Error
16	Out	Initialize Device
17	In	Device Ready for Input
18		Signal Ground
19		Signal Ground
20		Signal Ground
21		Signal Ground
22		Signal Ground
23		Signal Ground
24		Signal Ground
25		Signal Ground
Shield		Chassis Ground

Figure A-11 Parallel Port Connector Pinout

SECTION 10 - SERIAL CONNECTOR PINOUT

Each standard RS-232 serial port connectors is either a D9 male as shown in the upper drawing in Figure A-12 or an RJ45 jack like the lower drawing in Figure A-12. The controller boards with RJ45 jacks are supplied with adapters to connect standard D9 serial peripherals. Because only eight of the nine RS-232 signals are brought out to the RJ45 connectors, the signal at pin 8 (pin 1 on the D9 adapter) is assigned to either the DCD signal or the RI signal, depending upon a jumper selection (see Chapter 2 for complete board jumper information).



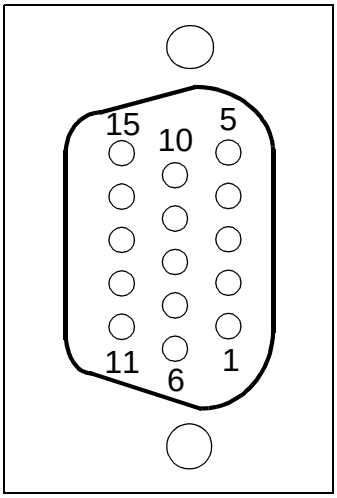
SERIAL COM PORT CONNECTORS				
D9 PIN	**RJ45 PIN**	**DIR**	**RS-232 SIGNAL**	**FUNCTION**
1*	1*	In	DCD	Data Carrier Detect
2	7	In	RX	Receive Data
3	6	Out	TX	Transmit Data
4	5	Out	DTR	Data Terminal Ready
5	8		GND	Signal Ground
6	4	In	DSR	Data Set Ready
7	3	Out	RTS	Request to Send
8	2	In	CTS	Clear to Send
9*	9*	In	RI	Ring Indicator
Shield	Shield			Chassis Ground

* RJ45 pin 1 is either assigned to the DCD or the RI signal, depending upon a jumper on the controller board. If the supplied RJ45-to-D9 adapter is being used, D9 pin 9 is not connected and D9 pin 1 is the DCD or RI signal from RJ45 pin 1.

Figure A-12 Serial Connector Pinouts

SECTION 11 - VIDEO CONNECTOR PINOUT

The video port uses a standard high-density D15 VGA connector. Figure A-13 shows the pinout.



VIDEO CONNECTOR		
PIN	**DIRECTION**	**FUNCTION**
1	Out	Red
2	Out	Green
3	Out	Blue
4		Reserved
5		Ground
6		Ground
7		Ground
8		Ground
9		Reserved
10		Ground
11		Reserved
12		Reserved
13	Out	Horizontal Sync
14	Out	Vertical Sync
15		Reserved
Shield		Chassis Ground

Figure A-13 Video Connector Pinout

SECTION 12 - VMEbus CONNECTOR PINOUT

Figure A-14 shows the location of the VMEbus P1 and P2 connectors and their orientation. Table A-2 shows the pin assignments for the VMEbus connectors. Note that only Row B of connector P2 is used; all other pins on P2 are reserved and should not be connected.

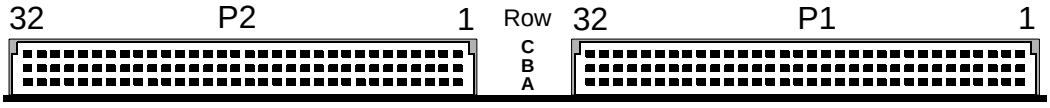


Figure A-14 VMEbus Connector Diagram

Table A-2 VMEbus Connector Pinout

PIN NUMBER	P1 ROW A SIGNAL	P1 ROW B SIGNAL	P1 ROW C SIGNAL	P2 ROW B SIGNAL
1	D00	BBSY	D08	+5 V
2	D01	BCLR	D09	GND
3	D02	ACFAIL	D10	Reserved
4	D03	BG0IN	D11	A24
5	D04	BG0OUT	D12	A25
6	D05	BG1IN	D13	A26
7	D06	BG1OUT	D14	A27
8	D07	BG2IN	D15	A28
9	GND	BG2OUT	GND	A29
10	SYSCLK	BG3IN	SYSFAIL	A30
11	GND	BG3OUT	BERR	A31
12	DS1	BR0	SYSRESET	GND
13	DS0	BR1	LWORD	+5 V
14	WRITE	BR2	AM5	D16
15	GND	BR3	A23	D17
16	DTACK	AM0	A22	D18
17	GND	AM1	A21	D19
18	AS	AM2	A20	D20
19	GND	AM3	A19	D21

Table A-2 VMEbus Connector Pinout (Continued)

PIN NUMBER	P1 ROW A SIGNAL	P1 ROW B SIGNAL	P1 ROW C SIGNAL	P2 ROW B SIGNAL
20	IACK	GND	A18	D22
21	IACKIN	SERCLK	A17	D23
22	IACKOUT	SERDAT	A16	GND
23	AM4	GND	A15	D24
24	A07	IRQ7	A14	D25
25	A06	IRQ6	A13	D26
26	A05	IRQ5	A12	D27
27	A04	IRQ4	A11	D28
28	A03	IRQ3	A10	D29
29	A02	IRQ2	A09	D30
30	A01	IRQ1	A08	D31
31	-12 V	+5 V STDBY	+12 V	GND
32	+5 V	+5 V	+5 V	+5 V

APPENDIX

B

SYSTEM DRIVER SOFTWARE

IN THIS APPENDIX:

SECTION 1 - INTRODUCTION

The VMIVME-7588 provides high performance video, SCSI, and Local Area Network (LAN) access by means of onboard PCI based adapters and associated software drivers. The PCI based video adapter used on the VMIVME-7588 is the Cirrus Logic 5436. Ultra / Fast / Wide SCSI operation is controlled by the onboard Adaptec 7880 PCI based SCSI adapter, while high performance LAN operation including 10Base2, 10BaseT, and 100BaseTx, is provided by the DEC 21142 ethernet controller chip.

To optimize performance of each of these PCI based subsytems, the VMIVME-7588 is provided with software drivers compatible with DOS, Windows for Workgroups Version 3.11, Windows 95, and Windows NT operating systems. The following paragraphs provide instructions for loading and installing the adapter software.

SECTION 2 - DRIVER SOFTWARE INSTALLATION

In order to properly use the SCSI and LAN adapters of the VMIVME-7588, the user must install the driver software provided as distribution diskettes with the unit. Detailed instructions for installation of the drivers during installation of Windows for Workgroups version 3.11, Windows 95, or Windows NT (Versions 3.5x and 4.0) operating systems described in the following sections.

SECTION 3 - WINDOWS FOR WORKGROUPS (VERSION 3.11)

1. Format and load the IDE hard drive with MS-DOS.
2. Begin installation of Windows for Workgroups 3.11, following the instruction provided by Microsoft for Express Setup. When you reach the 'WINDOWS FOR WORKGROUPS NETWORK SETUP' screen, it will show that 'NO NETWORK IS INSTALLED'.
3. The following steps will load the DEC ethernet drivers, and configure the DEC 21142 adapter.

NOTE:

IF YOU DO NOT REQUIRE LAN OPERATION CLICK THE MOUSE ON 'CONTINUE' AND SKIP STEPS 4. THROUGH 12., ELSE FROM THE MAIN 'NETWORK SETUP' SCREEN, CLICK THE MOUSE ON THE 'NETWORKS' BUTTON.

4. Under 'NETWORKS', click the mouse on the circle to install 'MICROSOFT WINDOWS NETWORK'.
5. Then Click the mouse on 'OK'.
6. The 'NETWORK SETUP SCREEN' appears again with the option for 'SHARING'. Click on 'SHARING' and choose the options that fit your system requirements by placing an x in the boxes shown. Then click on 'OK'.
7. Again at the 'NETWORK SETUP SCREEN', click on 'CONTINUE'.
8. Under 'ADD NETWORK ADAPTER' click the mouse on 'UNLISTED or UPDATED NETWORK ADAPTER'. Then click the mouse on 'OK'.

9. Insert the VMIVME-7588 distribution disk marked 320-500010-007 into drive A: and type: `A:\I386\WFW311\` then click the mouse on 'OK'.
10. Under 'UNLISTED' or 'UPDATED NETWORK ADAPTER', choose 'DEC PCI ETHERNET DC21142 BASED ADAPTER', then click the mouse on 'OK'.
11. Under 'MICROSOFT WINDOWS NETWORK NAMES' , enter the network names you want for computer name, group name, etc. Then click the mouse on 'OK'.
12. Windows for Workgroups should now continue with regular installation. During the remaining installation steps, use the full path name, A:\I386\WFW311\, whenever prompted for the DEC 21142 driver diskette.
13. After Windows for Workgroups installation is complete, you may choose to install the Adaptec SCSI drivers.

NOTE:

IF YOU DO NOT REQUIRE THE SCSI DRIVERS FOR OPERATION, PLEASE SKIP STEPS 14. THROUGH 18.

14. Insert the VMIVME-7588 Distribution diskette marked 320-500010-008 into drive A:
15. From the Windows file manager select 'RUN', and type `A:\SETUP` <ENTER>.
16. Under Adaptec EZ-SCSI 4.0 Setup Wizard, click on 'NEXT' then select 'SCAN ALL' by highlighting the circle and then click on 'NEXT'.
17. Then click on 'NEXT' again for each of the six following screens: 'SCSI DEVICE DETECTION' screen, 'SETUP OPTIONS' screen, 'CHOOSE DIRECTORY' screen, 'START COPYING FILES' screen, 'MODIFY CONFIG.SYS FILES' screen and 'INSTALLATION SUCCESSFUL' screen.
18. Then click on 'REBOOT' at the 'RESTARTING SYSTEM' screen.
19. The following steps will load the optional Cirrus Logic video drivers on to the hard drive. These drivers are not required for system operation, but can be installed to optimize video performance.

NOTE:

IF YOU DO NOT REQUIRE THE CIRRUS LOGIC VIDEO DRIVERS FOR OPERATION, PLEASE SKIP STEPS 20. THROUGH 32.

20. Insert the VMIVME-7588 Distribution diskette marked 320-500010-002 into drive A:
21. From the Program Manager Screen double click the mouse on the 'MAIN' icon.
22. Next double click the mouse on the 'MS-DOS' icon.
23. Type the following command: `A:WFWGBAT` <ENTER>.
24. This will make a directory on the C: drive named C:\CIRRUS\W311\, and copy the Cirrus Logic video drivers onto the C:\CIRRUS\W311\ directory. When the WINDOWS screen returns, remove the CIRRUS LOGIC diskette from drive A and return to the 'PROGRAM MANAGER WINDOW'.
25. From the 'PROGRAM MANAGER' window, click the mouse on 'FILE' and then click on 'RUN'.
26. Next, type `C:\CIRRUS\W311\INSTALL` and click on 'OK'.
27. In the 'INSTALL PROGRAM' window, click on 'CONTINUE'.
28. Then click 'CONTINUE' to select the default destination path and click 'INSTALL' in the 'VERIFY DESTINATION' window.
29. Select 'OK' in the 'SELECT A GROUP' window, then click 'OK' in the 'INSTALLATION' COMPLETE' window.
30. In the 'WINMODE' screen, adjust the monitor settings as required and then click on 'OK'.
31. Click the mouse on 'OK' to restart windows.
32. There will now be a 'VGA DISPLAY' icon in the 'PROGRAM MANAGER' window. In the 'VGA DISPLAY' window there will be a 'WINMODE' icon that will allow the user to adjust the VGA display.
33. In order for the network to be setup properly, it is necessary to setup the proper connection type for your system.

Since the Windows screen is present from step 23., proceed with the following steps to set your network connection type.

NOTE:

IF YOU ARE NOT RUNNING A NETWORK, PLEASE SKIP STEPS 34. THROUGH 38.

34. From the ‘PROGRAM MANAGER’ screen, double click on the ‘NETWORKS’ icon.
35. Then double click on ‘NETWORK SETUP’ icon.
36. Under ‘NETWORK SETUP’, double click on ‘DEC PCI ETHERNET DC21142 BASED ADAPTER’.
37. Under ‘ADVANCED NETWORK-ADAPTER SETTINGS’, choose ‘CONNECTION TYPE’ and choose the ‘CONNECTION TYPE VALUE’ needed for your system. Do not use ‘AUTO SENSE TYPE.’ Click on ‘SET’ and then ‘OK’.
38. Under ‘NETWORK SETUP’, click on ‘OK’. If the network connection type has changed, then click ‘OK’ at the next screen for the information message about ‘SYSTEM.INI’ and ‘PROTOCOL.INI’ and click on ‘RESTART COMPUTER’ for the new network settings to take effect.

The unit should now be configured for operation in the WINDOWS FOR WORKGROUPS 3.11 environment.

SECTION 4 - WINDOWS 95

1. Format the hard drive with MS-DOS.
2. Begin installation of Windows 95, following the instructions provided by the Windows 95 manual.
3. When you reach the 'WINDOWS 95 SETUP WIZARD SCREEN' choose 'TYPICAL' under 'SETUP OPTIONS' and then click on 'NEXT'.
4. When you reach the 'ANALYZING YOUR COMPUTER' screen, place an x in the box for 'NETWORK ADAPTER' and 'CD-ROM' if one is required, and then click on 'NEXT'.
5. Under the 'WINDOWS COMPONENTS SCREEN', select 'INSTALL THE MOST COMMON COMPONENTS' and then click on 'NEXT'.
6. Continue with the installation until Windows 95 is completely installed and has rebooted.

NOTE:

IF YOU DO NOT REQUIRE LAN OPERATION, SKIP STEPS 7. THROUGH 24.

7. From the main Windows 95 screen, click on 'START'.
8. Then click on 'SETTINGS' and then 'CONTROL PANEL'.
9. Double click on the 'SYSTEM' icon and select the 'DEVICE MANAGER' tab.
10. Double click on 'OTHER DEVICES' and then double click on 'PCI ETHERNET CONTROLLER'.
11. Select the 'DRIVER' tab and then select 'CHANGE DRIVER'.
12. In the 'SELECT HARDWARE TYPE' screen choose 'NETWORK ADAPTERS' and click on 'OK'.
13. Insert the Diskette marked 320-500010-007 into drive A:
14. In the 'SELECT DEVICE' window, click on 'HAVE DISK' and type `A:\I386\WIN95\` and then click on 'OK'.
15. Under 'SELECT DRIVERS' choose 'PCI FAST ETHERNET DEC21142 BASED ADAPTER' and then click on 'OK'.
16. Under 'PCI ETHERNET CONTROL PROPERTIES' select 'OK'. Then the system will prompt you for computer and workgroup

names. Type in the names you wish to use in the spaces shown and then choose 'CLOSE'.

17. Windows 95 will then prompt for diskettes. Follow all instructions.
18. At the 'SYSTEM PROPERTIES' window, click on 'OK'.
19. From 'CONTROL PANEL', double click on the 'NETWORK' icon.
20. Under 'NETWORK', click on 'FILE AND PRINT SHARING' and choose the appropriate items for your system then click on 'OK'.
21. Under the 'NETWORK' window, double click on 'PCI FAST ETHERNET DEC21142 BASED ADAPTER'.
22. Select the 'ADVANCED' folder tab. Then under 'PROPERTY' choose 'CONNECTION TYPE' and under value choose the appropriate value for your system and click on 'OK'. Do not use 'AUTO SENSE TYPE.'
23. At the 'NETWORK' window, click on 'OK'. When prompted, insert the diskettes needed to complete the network installation.
24. When the system prompts you to restart your computer, click on 'YES' for the network settings to take effect.

NOTE:

THERE ARE TWO METHODS FOR INSTALLING THE SCSI DRIVERS. IF YOU DO NOT REQUIRE THE SCSI DRIVERS FOR OPERATION, PLEASE SKIP STEPS 25. THROUGH 37., AND ALTERNATIVE STEPS A. THROUGH F.

25. This section describes how to update/install the aic78xx.mpd driver for Windows 95
26. Start Windows 95.
27. Click the 'START' button on the Windows 95 task bar, and then point to 'SETTINGS'.
28. Click the mouse on 'CONTROL PANEL'.
29. Double-click the mouse on the 'SYSTEM' icon.
30. On the 'DEVICE MANAGER' tab, click the plus sign next to the 'OTHER DEVICES' icon.
31. Double-click the yellow question mark labelled 'PCI SCSI BUS CONTROLLER'.

32. On the Driver tab, click 'CHANGE DRIVER'. You may be asked to select the hardware type; if asked to do so, select 'SCSI -CONTROLLER', then click on 'OK'.
33. Click the 'HAVE DISK' button and type `A:\win95` as the location to copy the manufacturer's file from.
34. Click the mouse on 'OK'.
35. Select the 7800 Family host adapter, and click 'OK'.
36. Click 'OK'. The driver is copied and scanned.
37. You must restart your computer for the changes to take effect. Click 'YES' to restart your computer.

Alternate SCSI Directions

The SCSI drivers may also be installed as follows:

A. From Windows 95, click the mouse on 'START', then 'SHUTDOWN'.
B. Select 'RESTART THE COMPUTER IN MS-DOS MODE', then click on 'YES'.
C. Wait for the C:\WINDOWS prompt, then insert the Diskette marked 320-500010-008 into drive A:
D. Type `A:` <ENTER>. Wait for the A:\ prompt, then type `INSTALL` <ENTER>.
E. Follow the instructions for default installation of the SCSI drivers.
F. When the installation is complete, remove the diskette from the drive, and press CTRL-ALT-DEL to reboot the computer.

NOTE:

THE FOLLOWING STEPS LOAD OPTIONAL CIRRUS LOGIC VIDEO DRIVERS FOR WINDOWS 95. THESE DRIVERS ARE NOT REQUIRED FOR SYSTEM OPERATION, BUT CAN BE USED TO OPTIMIZE VIDEO PERFORMANCE. IF YOU DO NOT REQUIRE THE CIRRUS LOGIC DRIVERS FOR OPERATION, PLEASE SKIP STEPS 38. THROUGH 47.

38. Click the mouse on 'START', then select 'PROGRAMS' and then select 'MS-DOS PROMPT'.

39. Insert the Cirrus Logic disk, 320-500010-004 into drive A and then type `A:w95bat`.
40. When Windows 95 returns remove the diskette from drive A:
41. Click the mouse on ‘START’ and then ‘SETTINGS’ then ‘CONTROL PANEL’.
42. Double click on the ‘SYSTEM’ icon and choose the ‘DEVICE MANAGER’ folder tab.
43. Double click on the ‘CIRRUS LOGIC’ entry and then select the ‘DRIVER’ folder tab.
44. In the ‘CIRRUS LOGIC PROPERTIES’ window, select ‘CHANGE DRIVER’.
45. In the ‘SELECT DEVICE’ window, double click on ‘HAVE DISK’, and then type: `C:\cirrus\win95\`.
46. Choose the ‘CIRRUS LOGIC 5436’ and then select ‘OK’.
47. At the ‘CIRRUS LOGIC PROPERTIES’ window, again choose ‘OK’ and when the prompted, select ‘YES’ to restart Windows 95.
48. The unit should now be properly configured for operation in Windows 95.

SECTION 5 - WINDOWS NT (VERSION 3.51)

1. Format the hard drive with MS-DOS.
2. Install the Windows NT boot disk in drive A, and reboot the computer.
3. When prompted, insert Windows NT Setup Disk 2 into drive A.
4. From the 'WELCOME TO SETUP' screen, press <ENTER> to set up Windows NT.
5. From the 'WINDOWS NT SETUP METHODS' screen, press 'C' for 'CUSTOM SETUP'.

****
*** CAUTION ***
****

IF EXPRESS SETUP IS CHOSEN, THE INSTALLATION PROCESS IS UNABLE TO DETECT THE MOST RECENT ADAPTEC HOST ADAPTER AND THE EMBEDDED DRIVER INCLUDED WITH WINDOWS NT WILL BE LOADED AND THE INSTALLATION PROCESS WILL FAIL.

6. When prompted, press 'S' to skip mass storage device detection. This allows the user to manually select the driver for your host adapter.
7. Since mass storage device detection was skipped in the previous step, Windows NT Setup displays <NONE> in the list of recognized devices. Press 'S' to configure additional SCSI adapters.
8. From the list of additional SCSI adapters, select 'OTHER (REQUIRES DISK PROVIDED BY A HARDWARE MANUFACTURER)', and press <ENTER>.
9. When prompted, insert the Adaptec 7800 Family Manager Set diskette, diskette #320-500010-009, into drive A and press <ENTER>.
10. The screen then displays the adapter drivers supported on the diskette. The 'ADAPTEC AHA-2940/AIC-78xx (PCI) NT v3.5x' driver is highlighted by default. Press <ENTER>.

NOTE:

IF YOU WANT TO ADD OTHER HOST ADAPTERS (THAT ARE NOT PART OF THE 78XX FAMILY), DO SO AT THIS TIME BY REPEATING STEPS 7. THROUGH 9. FOR EACH ADDITIONAL ADAPTER AND

INSERTING THE APPROPRIATE DISK PROVIDED BY THE HARDWARE MANUFACTURER

11. After all host adapters have been specified press <ENTER>.
12. When prompted inset Windows NT Setup Disk 3.
13. When prompted, press <ENTER> to install Windows NT from 'CD-ROM (RECOMMENDED)'.
14. At the next screen, verify that the computer information is correct and press 'ENTER'.
15. When prompted, press <ENTER> to install Windows NT on the highlighted partition or unpartitioned space.
16. At the next screen, press <ENTER> to select '*Leave the current file system intact (no changes).*'
17. Next, press <ENTER> to install Windows NT at the default location \WINNT 35.
18. At the next screen, press 'ESC' to skip the exhaustive hard drive examination.
19. When prompted, reinsert the ADAPTEC 7800 Family Manager Set diskette, diskette #320-500010-009, into drive A and press <ENTER>.
20. At the next screen, remove the floppy from drive A and press <ENTER> to restart the computer.
21. At the operating system screen, select Windows NT and press <ENTER>.
22. After step 21., press <ENTER> to continue with the Windows NT operating system setup. Follow the instructions given on screen and in the Windows NT installation documentation to continue with Windows NT setup.
23. The following steps will load the DEC ethernet drivers and configure the DEC 21142 adapter.
24. At the 'NETWORK ADAPTER CARD DETECTION' screen, select 'CONTINUE'.

NOTE:

IF YOU DO NOT REQUIRE LAN OPERATION, CLICK ON NO NETWORK AND THEN AT THE NEXT SCREEN CLICK ON OK. THEN SKIP STEPS 25. THROUGH 32.

25. At the 'ADD NETWORK ADAPTER' screen, scroll down the list to 'OTHER (REQUIRES DISK FROM MANUFACTURER)' and choose it by selecting 'CONTINUE'.
26. At the 'INSERT DISK SCREEN', type in the location of the drivers, A:\I386\WNT351\ .
27. From the OEM option, highlight 'DEC PCI FAST ETHERNET DC21142' and select 'OK'.
28. Continue with setup until you reach the next network setup screen below.
29. At the 'DEC DC21142 BASED ADAPTER SETUP', choose the appropriate connection type for your system and then select 'CONTINUE'.
30. At the next screen, choose the appropriate network protocal, (The default is 'NETBEUI TRANSPORT'.) and select 'CONTINUE'. Do not use 'AUTO SENSE TYPE.'
31. At the 'NETWORK SETTINGS' screen, choose 'OK'.
32. At the 'DOMAIN/WORKGROUP SETTINGS' screen, enter the appropriate workgroup and domain name and then click on 'OK'.

NOTE:

THE FOLLOWING STEPS WILL LOAD THE OPTIMAL VIDEO DRIVERS. THESE DRIVERS ARE NOT REQUIRED FOR SYSTEM OPERATION, BUT CAN BE INSTALLED TO OPTIMIZE VIDEO PERFORMANCE. IF YOU DO NOT REQUIRE THE CIRRUS LOGIC DRIVERS FOR OPERATION, PLEASE SKIP STEPS 34. THROUGH 46.

33. From the 'PROGRAM MANAGER' window, double click on the 'MAIN' icon.
34. Then double click on the 'MS-DOS' icon.
35. Insert disk 320-500010-003 into drive A.
36. Type `A:\wntbat` and press <ENTER>.
37. When Windows NT returns from the DOS prompt, double click the 'CONTROL PANEL' icon.
38. Then double click on 'DISPLAY'.
39. Under 'DISPLAY SETTINGS' screen, click on 'CHANGE DISPLAY TYPE'.
40. Under 'DISPLAY TYPE' window, click on 'CHANGE'.

41. Under ‘SELECT DEVICE’ window, click on ‘OTHER’ button.
42. Then type in the path name, `C:\CIRRUS\WNT\` and click on ‘OK’.
43. Highlight ‘CIRRUS LOGIC 256/64K/16M COLORS’ and click on ‘INSTALL’.
44. At the ‘INSTALLING DRIVERS’ screen, click on ‘YES’.
45. Under the ‘WINDOWS NT SETUP’ screen, verify the name C:\CIRRUS\WNT\ appears in the box and then click on ‘CONTINUE’.
46. The message window ‘INSTALLING DRIVERS’ appears letting you know that the drivers were successfully installed. Click on ‘OK’.
47. At the next screen, press ‘OK’ to restart.
48. Then press ‘RESTART NOW’. The unit should now be properly configured for Windows NT 3.51.

SECTION 6 - WINDOWS NT (Version 4.0)

Windows NT 4.0 includes drivers for the onboard LAN, SCSI, and video adapters. The following steps are required to configure the LAN for operation.

1. Follow the normal Windows NT 4.0 installation until you reach the ‘WINDOWS NT WORKSTATION SETUP’ window which states that ‘WINDOWS NT NEEDS TO KNOW HOW THIS COMPUTER SHOULD PARTICIPATE ON A NETWORK’.
2. Place a dot next to ‘THIS COMPUTER WILL PARTICIPATE ON A NETWORK’.
3. Place a check mark next to ‘WIRED TO THE NETWORK’ and then click on ‘NEXT’.
4. At the next screen, click on the ‘START SEARCH’ button. The DEC 21142 should appear in the ‘NETWORK ADAPTERS’ screen. After it appears, click on ‘NEXT’.
5. At the next screen, place a check mark in the box next to the appropriate protocol for your system and then click on next.
6. Then click on ‘NEXT’ again at the screen to install selected components.

7. At the ‘DEC DECCHIP 21142 BASED ADAPTER SETUP’ screen, choose the appropriate connection type for your system and then click on ‘NEXT’. Do not use ‘AUTO SENSE TYPE.’
8. At the next screen, click on ‘NEXT’ to start the network.
9. At the next screen, select whether you are going to participate in a workgroup or domain and then enter the appropriate WORKGROUP and DOMAIN information and click on ‘NEXT’.

The unit should now be configured for LAN operation under Windows NT 4.0.

APPENDIX

C

BASIC INPUT OUTPUT SYSTEM

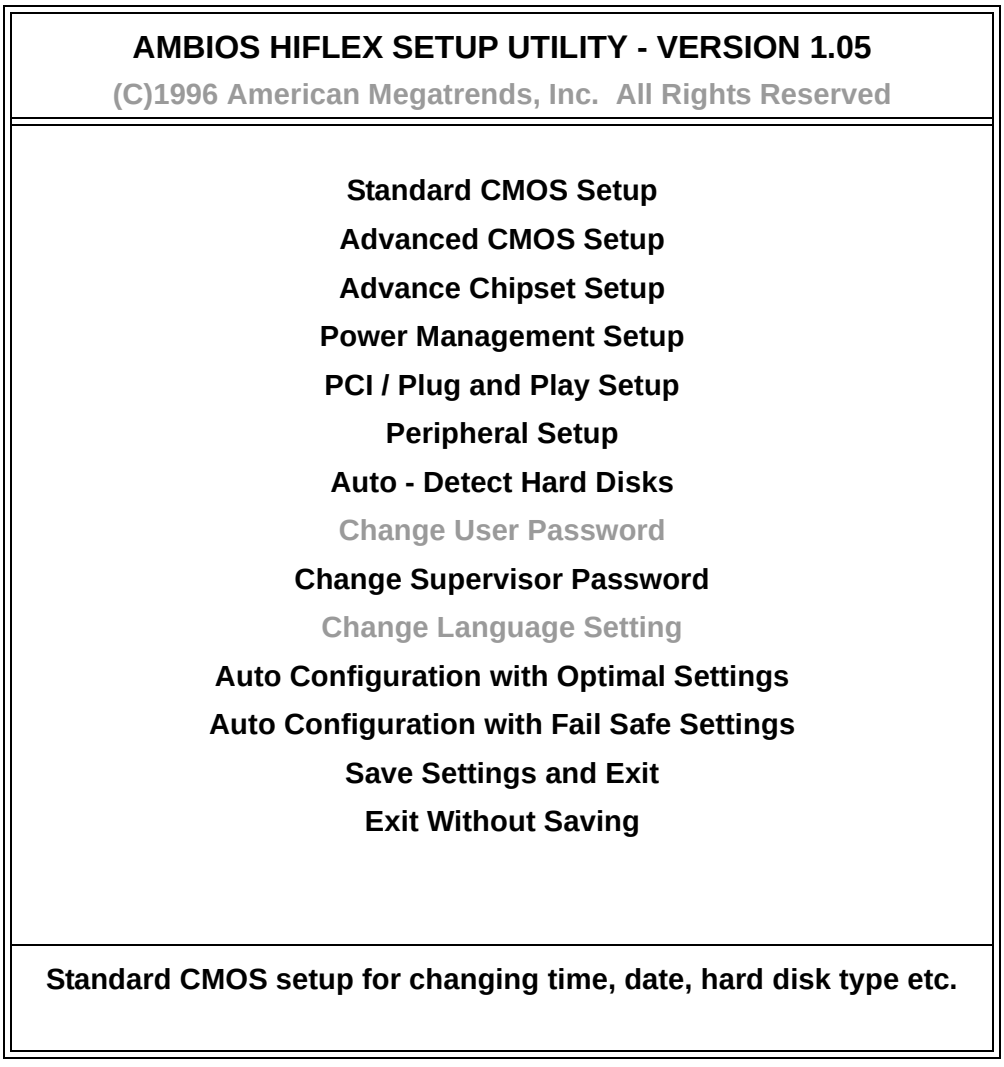
IN THIS APPENDIX:

The VMIVME-7588 has three types of BIOS contained in a single Flash Memory device: the AMI (system) BIOS, the Cirrus Logic CL-GD5436 SVGA BIOS, and the Adaptec SCSI BIOS. This appendix describes the menus and options associated with the AMI (system) BIOS.

SECTION 1 - SYSTEM BIOS SETUP UTILITY

During boot-time, continuously press the DEL key until the **AMBIOS Hiflex Setup Utility** screen is displayed. From this screen, the user can select any part of the AMI (system) BIOS that needs to be changed, such as floppy drive configuration or system memory.

Options available to the operator are designated with dark text in the following graphics. The parameters included are default values.



SECTION 2 - STANDARD CMOS SETUP

Selection of the first main menu item, the **Standard CMOS Setup**, allows the user to adjust the date and time in addition to defining the parameters and disk drives associated with the system.

Note that the values included for Date, Time, Floppy Drive and Pri Master are example values. The default values are 'Not Installed.'

AMBIOS SETUP - STANDARD CMOS SETUP

(C)1996 American Megatrends, Inc. All Rights Reserved

Date (mm/dd/yyyy): **Mon Nov 04, 1996**

Time (hh/mm/ss): **09:37:16**

Floppy Drive A: **1.44 MB 3 ½**

Floppy Drive B: **Not Installed**

	Type	Size	Cyln	Head	WPcom	Sec	LBA Mode	Blk Mode	PIO Mode	32Bit Mode
Pri Master :	User	1295	2633	16	65535	63	On	On	4	Off
Pri Slave :	Not Installed									
Sec Master :	Not Installed									
Sec Slave :	Not Installed									

Boot Sector Virus Protection **Disabled**

Month : Jan - Dec

Day : 01 - 31

Year : 1901 - 2099

ESC :Exit ↑↓ :Sel

PgUp/PgDn :Modify

F2/F3 :Color

Date / Time Configuration

The **Time** field displays the time in the 24-hour clock format. (For P.M., add 12 to the hour. Enter 4:30 P.M. as 16:30:00.)

Floppy Disk Drive Configuration

Floppy Drive A: Supports a 720 Kbyte 3.5-inch drive, a 1.44 Mbyte 3.5-inch drive, or a system without a floppy drive. The default setting is 1.44 Mbyte 3.5-inch.

Floppy Drive B: The system uses only one floppy drive, so the default setting is **Not Installed**.

Use the arrow keys to select the floppy drive type.

Master and Slave Disk Drive Configuration

The VMIVME-7588 has the capability of utilizing up to two hard disk drives. The conditions presented in the menu illustrate and example of a 1.3 Gigabyte hard drive. The default setting for the Primary Master is **Auto** and the default setting for the Primary Slave is **Not Installed**.

Boot Sector Virus Protection

Enabling this feature prohibits writes to the boot sector (Head 0, Track0, Sector 1). This feature only works for IDE devices and for I/O calls made through INT 13H. The default setting is **Disabled**.

SECTION 3 - ADVANCED CMOS SETUP

From the Main Menu, selecting the **Advanced CMOS Setup** option displays options to establish system preferences to customize the system operations.

AMBIOS SETUP - ADVANCED CMOS SETUP

Quick Boot	**Enabled**	**Available Options:**
BootUp Sequence	A:,C:,CDROM	Disabled
BootUp Num-Lock	Off	Enabled
Floppy Drive Swap	Disabled	
Mouse Support	Enabled	
Primary Display	VGA / EGA	
Password Check	Setup	
OS/2 Compatible Mode	Disabled	
CPU MicroCode Mode	Disabled	
Internal Cache	WriteBack	
External Cache	WriteBack	
System BIOS Cacheable	Enabled	
C000,16k Shadow	Cached	
C400,16k Shadow	Cached	
C800,16k Shadow	Disabled	
CC00,16k Shadow	Disabled	
D000,16k Shadow	Disabled	
D400,16k Shadow	Disabled	ESC :Exit ↑↓ :Sel
D800,16k Shadow	Disabled	PgUp/PgDn :Modify
DC00,16k Shadow	Disabled	F2/F3 :Color

Quick Boot

This feature, when Enabled, allows the system to boot without the presence of a keyboard; however, the Quick Boot does not check all of memory checked during a regular boot sequence. The default condition is **Enabled**.

Bootup Sequence

The BIOS Setup Program boots the system from the device selected in the **Bootup Sequence** option. The default setting enables the BIOS to boot the system from floppy disk drive A:, if unsuccessful, it will try to boot from hard disk drive C:, if again unsuccessful, it will then boot from CDROM. If the **Bootup Sequence** option is set to **C:, A:,CDROM:**, the system will attempt to boot from hard drive C: then from floppy drive A:, and finally from CDROM. The same procedure holds true if the **CDROM:, C:, A:** option is selected. Set this option to **A:, C:, CDROM:** to use the EISA Configuration Utility, AMI Flash Utility, diagnostics, and other utilities.

Bootup Num-Lock

The **Bootup Num-Lock** option enables the `Num Lock` option on the keyboard to be turned off when the system is powered on. This option allows use of the arrow keys on the numeric keypad. The BIOS defaults the Num-Lock option: **Off**.

Floppy Drive Swap

This option logically swaps floppy drives A: and B:, allowing the VMIVME-7588 to boot from B:.

Mouse Support

The **Mouse Support** option is used to enable or disable mouse support in the BIOS Setup program. The BIOS Setup program supports a PS/2-type mouse. If disabled, the mouse will not function in the BIOS Setup program. The default is **Enabled**.

Primary Display

This option configures the primary display subsystem in the computer. The settings include: Absent, VGA/EGA, CGA40x25, CGA80x25, and Mono. The default is **VGA/EGA**.

Password Check

When enabled, the **Password Check** option prevents unauthorized system boot-up or unauthorized use of BIOS Setup. The password check function is enabled by choosing **Always** or **Setup**. If **Always** is chosen, the prompt appears each time the system is powered on. If **Setup** is chosen, the prompt appears only when an attempt is made to enter the Setup program. The password feature is disabled by entering the **Change Password** option and entering a carriage return at the prompt for a new password. The default setting is **Setup**.

OS/2 Compatible Mode

The **OS/2 Compatible Mode** option allows the BIOS to configure the system to operate on IBM's OS/2 platform or any other operating system that does not support Plug and Play. The default setting is **Disabled** and should not be modified by the user.

CPU MicroCode Mode

The default setting is **Disabled** and should not be modified by the user.

Internal Cache

This option allows the user to select the type of internal cache algorithm to be used by the BIOS and the CPU. The selections include **Writeback**, **Write-Through**, or **Disabled**. The **Disabled** option allows the CPU to set the caching algorithm. The Optimal default setting and the Fail-Safe default setting is **Writeback**.

External Cache

This option allows the user to select the type of external cache algorithm to be used by the BIOS and the CPU. The selections include **Writeback**, **Write-Through**, or **Disabled**. The **Disabled** option allows the CPU to set the caching algorithm. The Optimal default setting and the Fail-Safe default setting is **Writeback**.

System BIOS Cacheable

When enabled, the **System BIOS Cacheable** option allows caching of the system BIOS. This option causes BIOS that has been shadowed from ROM to RAM using the **System ROM Shadow** option to be cached. Caching means that a block of data is stored in cache memory, providing faster access time and execution speed of the BIOS. The default setting is **Enabled**.

C000, 16 K Shadow and C400, 16 K Shadow

These options specify how the contents of the video ROM are handled. The default setting is **Disabled**.

C800, 16 K Shadow and CC00, 16 K Shadow

These options specify how the contents of the SCSI ROM are handled. The default setting is **Disabled**.

D000, 16 K Shadow, D400, 16K Shadow, D800, 16K Shadow, and DC00, 16 K Shadow

These options should remain at **Disabled** on the VMIVME-7588.

SECTION 4 - ADVANCED CHIPSET SETUP

AMBIOS SETUP - ADVANCED CHIPSET SETUP

Global Triton2 Enabled	**Enabled**	**Available Options:**
Shutdown to Port 92	**Disabled**	Disabled
Memory Hole	**Disabled**	Enabled
IRQ12/M Mouse Function	**Enabled**	
8Bit I/O Recovery Time (Sysclk)	**1**	
16Bit I/O Recovery Time (Sysclk)	**1**	
DRAM Timings	**60ns**	
Refresh Rate	66Mhz	
Turbo Read LeadOff	Disabled	
Read Burst Timing	x333	
Write Burst Timing	x333	
Fast RAS to CAS Delay (Clocks)	3	
LeadOff Timing	7/6/3/4	
Turbo Read Pipelining	Disabled	
Speculative LeadOff	Disabled	
Turn-Around Insertion	Disabled	
Memory Address Drive Strength	**8ma/8ma**	
TypeF DMA Buffer Control1	**Disabled**	
TypeF DMA Buffer Control2	**Disabled**	
NA Disable (NAD) for Ext Cache	**Enabled**	
Peer Concurrency	**Enabled**	
PCI 2.1 Passive Release Enable	**Enabled**	
Delayed Transaction Enable	**Disabled**	
North Bridge Retry Enable	**Enabled**	**ESC** :Exit ↑↓ :Sel
USB KeyBoard Support	**Disabled**	**PgUp/PgDn** :Modify
USB Passive Release Enable	**Enabled**	**F2/F3** :Color

From the Main Menu, select the Advanced Chipset Setup option to enable the modification of the core logic of the system to processor interface. This setup menu modifies the Triton II chipset memory and PCI control.

Global Triton2 Enabled

This value enables operation of the Triton2 Global Functions. The default setting is **Enabled** and should not be modified by the user.

Shutdown to Port 92

The menu item permits a faster version of the keyboard reset. The default setting is **Disabled** and should not be modified by the user.

Memory Hole

This option allows the user to select a memory hole. The settings are **Disabled**, **512-640 K**, or **15-16 M**. The default setting is **Disabled**.

IRQ12/M Mouse Function

This option should be set according to the mouse hardware implementation. The default setting is **Enabled**. The **Disabled** setting should be used if the mouse hardware uses IRQ12. Choose **Enabled** if a keyboard controller mouse interrupt is used.

8 bit I/O Recovery Time (SYSCLK)

This option specifies the length of a delay inserted between consecutive 8-bit I/O operations. Options include: disabled, 8, 6, 5, 4, 3, 2, and 1. The default setting is **1**.

16 bit I/O Recovery Time (SYSCLK)

This option specifies the length of a delay inserted between consecutive 16-bit I/O operations. Options include: disabled, 4, 3, 2, and 1. The default setting is **1**.

DRAM Timings

This option specifies the RAS access time for the DRAM used in the computer for system memory. Options include: Manual, 60ns, and 70ns. The default setting is **60ns**. Selection of the Manual setting activates the following menu items and allows them to be adjusted. However, these items are optimized to system specifications and should not be adjusted by the user.

Refresh Rate

The DRAM refresh rate is adjusted according to the frequency selected in this field. The field is configured based on system options and should not be adjusted by the user. Options include: 50Mhz, 60Mhz, 66Mhz. The default setting is **66Mhz**.

Turbo Read LeadOff

This option control the DRAM read lead off timing. The default setting is **Disabled**, and should not be modified by the user.

Read Burst Timing

This value controls the read burst transfer timing for DRAM access on the VMIVME-7588. The default setting is **x333**. This value should not be modified by the user.

Write Burst Timing

This value controls the write burst transfer timing for DRAM access. The default setting is **x333**, and should not be modified by the user.

Fast RAS to CAS Delay (Clocks)

This option specifies the number of system clock cycles between the assertion of the DRAM RAS and CAS Signals. The default value is **3** and should not be modified by the user.

LeadOff Timing

These values determine the DRAM page hit lead off timings. The default setting is **7/6/3/4**. These values should not be modified by the user.

Turbo Read Pipelining

This option controls the first input register in the DRAM data pipeline. The default setting is **Disabled** and should not be modified by the user.

Speculative LeadOff

This option defines when a DRAM read request is presented in relation to final memory target decoded by the TXC. The default setting is **Disabled** and should not be modified by the user.

Turn-Around Insertion

This option controls the extended turn around time for the memory controller buffers. The default setting is **Disabled** and should not be modified by the user.

Memory Address Drive Strength

This field controls the strength of the chipset output buffers that drive the DRAM address and control signals. The default value is **8ma/8ma** and should not be modified by the user.

TypeF DMA Buffer Control1

This option selects the operating mode of the on board DMA Controller1. The default setting is **Disabled** and should not be modified by the user.

TypeF DMA Buffer Control2

This option selects the operating mode of the on board DMA Controller2. The default setting is **Disabled** and should not be modified by the user.

NA Disable (NAD) for Ext Cache

The option selects the operating mode for the NA# Line. The default setting is **Disabled** and should not be modified by the user.

Peer Concurrency

When enabled, this option allows the CPU to run DRAM/L2 cycles when non-PHLD PCI Masters are running non-locked cycles targeting PCI peer devices. The default setting is **Enabled** and should not be modified by the user.

PCI 2.1 Passive Release Enable

This option enables PCI Rev. 2.1 Passive Release functions that provide a PCI bus release mechanism to meet required master latencies. The default setting is **Enabled** and should not be modified by the user.

Delay Transaction Enable

When enabled, this function will provide a delayed cycle completion mechanism to support PCI target devices that cannot complete PCI cycles as required by standard timing. The default setting is **Disabled** and should not be modified by the user.

North Bridge Retry Enable

This option enables PCI retry to/from the on board TXC controller chip. The default setting is **Enabled** and should not be modified by the user.

USB Keyboard Support

This option is not supported. The default setting is **Disabled** and should not be modified by the user.

USB Passive Release Enable

This option is not supported. The default setting is **Enabled** and should not be modified by the user.

SECTION 5 - POWER MANAGEMENT SETUP

From the **Main Menu**, selection of the **Power Management Setup** option enables the modification of the power management settings for the PCI interface items.

AMBIOS SETUP - POWER MANAGEMENT SETUP

Power Management/APM	**Disabled**	**Available Options:**
Instant-On Timeout (Minute)	Disabled	Disabled
Green PC Monitor Power State	Standby	Enabled
Video Power Down Mode	Disabled	
Hard Disk Power Down Mode	Disabled	
Hard Disk Time Out (Minute)	Disabled	
Standby Time Out (Minute)	Disabled	
Suspend Time Out (Minute)	Disabled	
Slow Clock Ratio	1:8	
Display Activity	Ignore	
IRQ3	Ignore	
IRQ4	Ignore	
IRQ5	Ignore	
IRQ7	Ignore	
IRQ9	Ignore	
IRQ10	Ignore	
IRQ11	Ignore	
IRQ12	Monitor	
IRQ13	ignore	**ESC** :Exit ↑↓ :Sel
IRQ14	Monitor	**PgUp/PgDn** :Modify
IRQ15	Ignore	**F2/F3** :Color

Power Management/APM

Set this option to **Enabled** to enable the Intel Triton II power management features and APM (Advanced Power Management). The default setting is **Disabled**.

Selection of the Enable value activates all of the following options except the **Instant-on Timeout**. Selection of the **Inst-On** option activates the **Instant-on Timeout** and the **Green PC Monitor Power State** only.

Instant-on Timeout (Minute)

This option specifies the length of a period of system inactivity while the computer is in full power on state. When this length of time expires, the BIOS takes the computer to a lower power consumption state, but the computer can return to full power instantly when any system activity occurs. Option settings range from 1 through 15 minutes. The default setting is **Disabled**.

Green PC Monitor Power State

This option specifies the power state that the green PC-compliant video monitor enters when the BIOS places it in a power savings state after the specified period of display inactivity has expired. The default setting is **Standby**, while other options include Suspend and Off.

Video Power Down Mode

This option specifies the power conserving state that the VESA VGA video subsystem enters after the specified period of display inactivity expires. The default setting is **Disabled**.

Hard Disk Power Down Mode

This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The default setting is **Disabled**.

Hard Disk Time Out (Minute)

This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters the power-conserving state specified in the **Hard Disk Power Down Mode** option. Option settings range from 1 through 15 minutes. The default setting is **Disabled**.

Standby Time Out (Minute)

This option specifies the length of a period of system inactivity while in full power-on state. When this length of time expires, the computer enters Standby power state. Option settings range from 1 through 15 minutes. The default setting is **Disabled**.

Suspend Time Out (Minute)

This option specifies the length of a period of system inactivity while in full power-on state. When this length of time expires, the computer enters Suspend power state. Option settings range from 1 through 15 minutes. The default setting is **Disabled**.

Slow Clock Ratio

This option specifies the speed at which the system clock runs in power-saving states. The settings are expressed as a ratio between the normal CPU clock speed and the CPU clock speed when the computer is in the power-conserving state. The default setting is **1:8**. Option settings include: 1:1, 1:2,1:4, 1:8, 1:16, 1:32, 1:64, and 1:128.

Display Activity

This option specifies if the BIOS is to monitor display activity for power conservation purposes. When this option is set to **Monitor** and there is no display activity for the length of time specified in the **Standby Timeout (Minutes)** option, the computer enters a power savings state. The default setting is **Ignore**.

IRQx

This option specifies whether the identified interrupt is to be monitored or ignored, while the unit is in power saving mode. The default condition for interrupts IRQ3 through IRQ11, IRQ13, and IRQ15 is **Ignore**, while IRQ12 and IRQ14 default to **Monitor**.

SECTION 6 - PCI / PLUG AND PLAY SETUP

From the **Main Menu**, select the **PCI / Plug and Play Setup** option to modify the basic PCI, Plug and Play, and ISA / EISA parameters.

AMBIOS SETUP - PCI / PLUG AND PLAY SETUP

Plug and Play Aware O/S	**No**	**Available Options:**
PCI Latency Time (PCI Clocks)	**64**	Disabled
PCI VGA Palette Snoop	**Disabled**	Enabled
PCI IDE BusMaster	**Disabled**	
OffBoard PCI IDE Card	**Auto**	
OffBoard PCI IDE Primary IRQ	Disabled	
OffBoard PCI IDE Secondary IRQ	Disabled	
DMA Channel 0	**PnP**	
DMA Channel 1	**PnP**	
DMA Channel 3	**PnP**	
DMA Channel 5	**PnP**	
DMA Channel 6	**PnP**	
DMA Channel 7	**PnP**	
IRQ3	**PCI/PnP**	
IRQ4	**PCI/PnP**	
IRQ5	**PCI/PnP**	
IRQ7	**PCI/PnP**	
IRQ9	**PCI/PnP**	
IRQ10	**PCI/PnP**	
IRQ11	**PCI/PnP**	
IRQ14	**PCI/PnP**	
IRQ15	**PCI/PnP**	**ESC** :Exit ↑↓ :Sel
Reserved Memory Size	**Disabled**	**PgUp/PgDn** :Modify
Reserved Memory Address	C8000	**F2/F3** :Color

Plug and Play Aware O/S

Set this option to **Yes** if the operating system is aware of and follows the Plug and Play specification. The default setting is **No**.

PCI Latency Timer (PCI Clocks)

This option specifies the latency timings (in PCI clocks) for all PCI devices on the PCI bus. Options include: 32, 64, 96, 128, 160, 192, 224, and 248. The default setting is **64**.

PCI VGA Palette Snoop

When this option is set to **Enabled**, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example: if there are two VGA devices in the computer (one PCI and one ISA) and if the **PCI VGA Palette Snoop** option is set to **Disabled**, then data read and written by the CPU is only directed to the PCI VGA device's palette registers. However, if the **PCI VGA Palette Snoop** option is set to **Enabled**, then data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both devices to be identical. The default setting is **Disabled**.

PCI IDE BusMaster

Set this option to **Enabled** to specify that the IDE controller on the PCI local bus includes a bus mastering capability. The default setting is **Disabled**.

OffBoard PCI IDE Card

This option specifies if an off-board PCI IDE controller adapter card is installed in the computer. The default setting is **Auto** and should not be modified by the user.

OffBoard PCI IDE Primary IRQ
OffBoard PCI IDE Secondary IRQ

These options specify the PCI interrupt used by the Primary (or Secondary) IDE channel on the off-board PCI IDE controller. The default setting is **Auto** and should not be modified by the user.

DMA Channel x

These options specify the operations of the internal DMA controllers. The options include the PnP and the ISA/EISA. The default setting for these options is **PnP.**

IRQx

These options specify the bus upon which the identified IRQ line is used. These options allow the user to reserve IRQs for legacy ISA adapter boards. The default setting for these options is **PCI/PnP.**

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter boards. options include: Disabled, 16k, 32k, and 64k. The default setting is **Disabled**.

Reserved Memory Address

This option specifies the beginning address (in hex) of the **Reserved Memory Size** defined in the previous option. The specified ROM memory area is reserved for use by legacy ISA adapter boards. The default setting is **C8000**.

SECTION 7 - PERIPHERAL SETUP

From the main menu, select the Peripheral Setup option to modify the Floppy disk controller, the serial ports, or the parallel port operational parameters.

AMBIOS SETUP - Peripheral Setup

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OnBoard FDC	**Auto**	**Available Options:**
OnBoard Serial Port1	**Auto**	Auto
OnBoard Serial Port2	**Auto**	Disabled
Serial Port2 Mode	**Standard**	Enabled
IR Transmission Mode	N/A	
Receiver Polarity	N/A	
Transmitter Polarity	N/A	
OnBoard Parallel Port	**Auto**	
Parallel Port Mode	**Normal**	
EPP Version	N/A	
Parallel Port IRQ	Auto	
Parallel Port DMA Channel	N/A	
OnBoard IDE	**Primary**	
		ESC :Exit ↑↓ :Sel
		PgUp/PgDn :Modify
		F2/F3 :Color

OnBoard FDC

This option enables the FDC (Floppy Drive Controller) on the motherboard. The default setting is **Auto**.

OnBoard Serial Port1

This option specifies the base I/O port address of serial port 1. Options include: Auto, Disable, 3F8h, 2F8h, 3E8h, and 2E8h. The default setting is **Auto**.

OnBoard Serial Port2

This option specifies the base I/O port address of serial port 2. Options include: Auto, Disable, 3F8h, 2F8h, 3E8h, and 2E8h. The default setting is **Auto**.

Serial Port2 Mode

This option specifies the base I/O port address of the parallel port. Options include: Standard, IrDA, and ASK IR. The default setting is **Standard**.

IR Transmission Mode

The default setting is **N/A**, but converts to Auto if the Serial Port2 Mode is changed.

Receiver Polarity

The default setting is **N/A**, but converts to Auto if the Serial Port2 Mode is changed.

Transmitter Polarity

The default setting is **N/A**, but converts to Auto if the Serial Port2 Mode is changed.

OnBoard Parallel Port

This option specifies the base I/O address of the parallel port. The default setting is **Auto**. Other options include: Disabled, 378, 278, and 3BC. The Disable selection inactivates the four lower level menu options that follow.

Parallel Port Mode

This option specifies the parallel port mode. The default setting is **Normal**. The settings include:

Normal The normal or output only parallel port mode is used.

EPP The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.

ECP The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Mbytes/sec. ECP provides symmetric bidirectional communication.

EPP Version

This parameter reflects the EPP version supported when EPP Parallel port mode is enabled. The default setting is **N/A** and should not be modified by the user.

Parallel Port IRQ

This parameter defines the interrupt request to be used during parallel port operation. The default setting is **Auto** and should not be modified by the user.

Parallel Port DMA Channel

This option is only available if the setting of the **Parallel Port Mode** option is **ECP**. The user can select the DMA channel that is to be used in conjunction with the **ECP** mode of the **Parallel Port Mode** option. The default setting is **N/A** and should not be modified by the user.

On Board PCI IDE

This option specifies the onboard Triton II IDE controller channels to be used. The default setting is **Primary** while other options include Disabled, Secondary, or Both.

SECTION 8 - AUTO-DETECT HARD DISK

Selection of this menu item presents to the user the first main menu item, the **Standard CMOS Setup**. Refer to “STANDARD CMOS SETUP” on C-3 for a detail description of the menu.

SECTION 9 - CHANGE USER PASSWORD

The VMIVME-7588 BIOS provides the capability of setting up two passwords, a supervisor and a user.

A change to the user password requires that the supervisor password be changed and that the system be rebooted. After the reboot, upon re-entering the BIOS main menu screen, (See “AMBIOS HIFLEX SETUP UTILITY - VERSION 1.05” on page C-2.) the menu setting for the **Change User Password** is sensitive to selection.

Selection of the menu item presents the following prompt for the user defined password. Enter the password and press `Enter`. The BIOS will then ask to confirm the password. If the confirmation password is entered correctly, then the new password will be set.

Enter new user password:

To disable the user password requires that the operator enter the current password and follow this with a single `Enter` key when prompted for the new password. The following message confirms the disable.

User password disabled, press any key to continue

The operator should note that the presentation of these password requests during bootup is dictated by the **Password Check** menu item found on the **Advanced CMOS Setup** menu. Refer to page C-7.

SECTION 10 - CHANGE SUPERVISOR PASSWORD

To change the supervisor password, select the menu item from the Setup Utility on page C-2. This will present the following prompt.

Enter the password and press `Enter`. The BIOS will then ask to confirm the password. If the confirmation password is entered correctly, then the new password will be set.

Enter new supervisor password: _

To disable the supervisor password requires that the operator enter the current password and follow this with a single `Enter` key when prompted for the new password. A message confirms the disable.

Presentation of the Supervisor password request during bootup is dictated by the **Password Check** menu item found on the **Advanced CMOS Setup** menu. Refer to page C-7.

SECTION 11 - AUTO CONFIGURATION WITH OPTIMAL SETTINGS

The **Optimal Settings** option loads the best-case BIOS values that optimize system performance. The system is delivered using the **Optimal Settings** BIOS values. After using the AMI Flash Utility to reprogram the system BIOS, select this option to ensure that the best-case values are being used. Selecting this option causes the following message to display. Select **Y** to load the optimal values.

Load high performance settings (Y / N) ? N

SECTION 12 - AUTO CONFIGURATION WITH FAIL SAFE SETTINGS

The **Fail-safe** BIOS Defaults option loads settings that are most likely to configure a workable computer when something is wrong. If you cannot boot the computer successfully, select the **Fail-safe** BIOS options and try to diagnose the problem after the computer boots. These settings do not provide optimal performance. If CMOS RAM becomes corrupt, the **Fail-safe** BIOS defaults load automatically. Selecting this option causes the following message to display. Select **Y** to load the optimal values.

Load failsafe settings (Y / N) ? N

SECTION 13 - SAVE SETTINGS AND EXIT

Selection of this menu option enables the user to exit the Setup Utility after saving the all previous made BIOS setting. A selection of **N** will send the user back to the main menu.

Save current settings and exit (Y / N) ? Y

SECTION 14 - EXIT WITHOUT SAVING

Selection of this menu option enables the user to exit the Setup Utility without saving the changes made to the BIOS settings. A selection of **N** will send the user back to the main menu. A selection of **Y** will cause the system to boot with the original BIOS settings.

Quit without saving (Y / N) ? N

APPENDIX

D

SCSI SELECTION UTILITY

IN THIS APPENDIX:

SECTION 1 - INTRODUCTION

The SCSI BIOS includes a configuration utility that enables users to change the VMIVME-7588 SCSI adapter settings. The utility lets users list the SCSI IDs of devices on the host adapter, format SCSI disk drives, and check drives for defects. This section describes the utility default and permitted settings, and the procedure for using the utility.

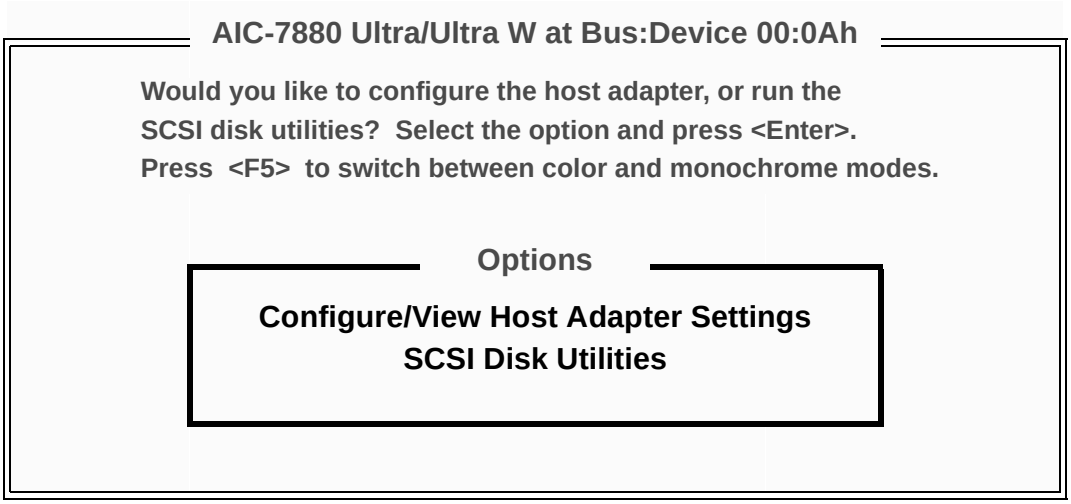
In this appendix, the VMIVME-7588 SCSI adapter will be referred to as the 'host adapter' or as the 'adapter.'

During boot-time, the Power-On Self Test (POST) software displays the message:

```
<<< Press <Ctrl><A> for SelectSCSI (TM) Utility! >>>
```

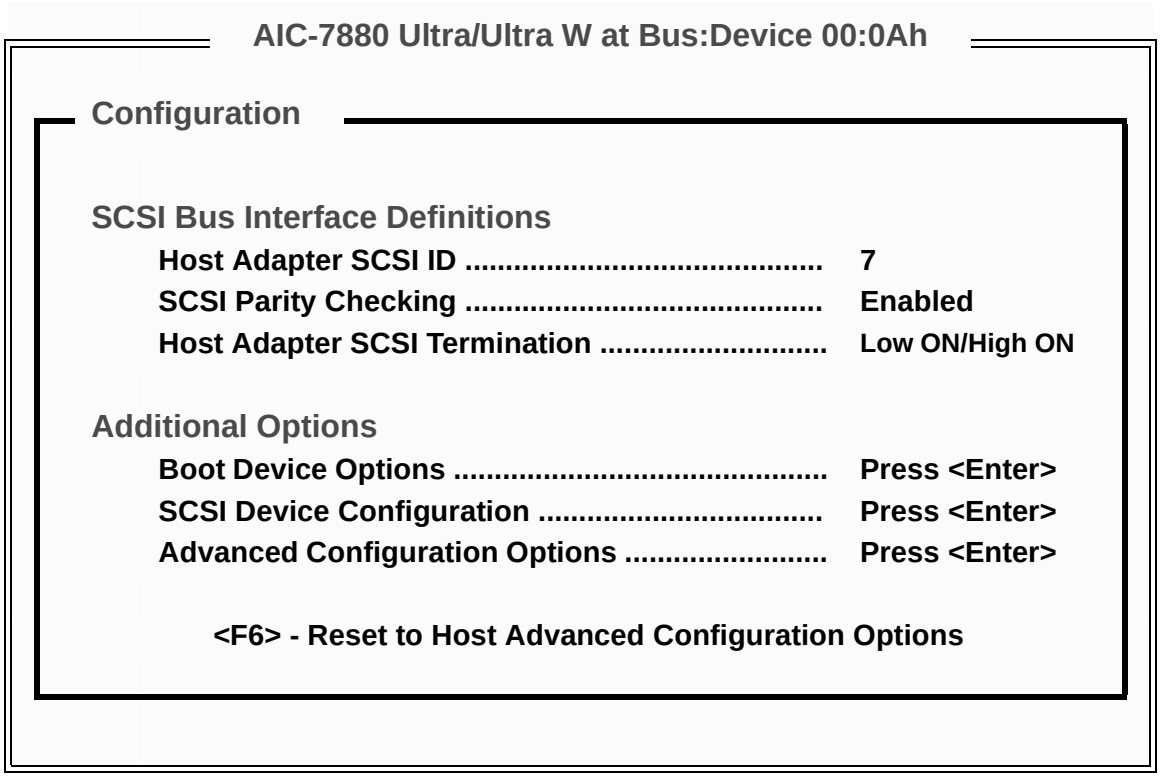
Initiating this key sequence presents to the operator the SCSI Selection Utility main menu which can be used to edit the Host Adapter Settings or the SCSI Disk Utility.

Options available to the operator are designated with dark text in the following graphics. The parameters included are default values.



SECTION 2 - CONFIGURE/VIEW HOST ADAPTER SETTINGS

Selection of the first main menu item, the **Configure/View Host Adapter Settings,** allows the user to adjust the SCSI Bus Interface Definitions.



SCSI Bus Interface Definitions

The SCSI bus Interface Definition default settings configure the unit for SCSI bus operation. The settings described here are for a host adapter SCSI ID, host adapter termination, and parity checking.

Host Adapter SCSI ID

Each device on the SCSI bus must have a unique SCSI ID. Allowable IDs include 0 through 7 on 8-bit adapters, and 0 through 15 on 16-bit adapters. The ID uniquely defines each SCSI device on the bus. The ID also

determines which device controls the bus when two or more devices try to use the bus at the same time. For 8-bit devices, ID 7 has the highest priority and ID 0 has the lowest priority. For 16-bit devices, the priority of IDs is 7-0, then 15-8: in this case, ID 7 has the highest priority and ID 8 has the lowest priority.

The Adapter has the highest priority on the SCSI bus, since each adapter (8- or 16-bit) is defaulted to SCSI ID of 7. Options range from 0 through 15.

SCSI Parity Checking

SCSI parity checking is used to verify the accuracy of data transfer on the SCSI bus for each adapter. If a device on the SCSI bus does not support SCSI parity, then disable the parity checking. Most SCSI devices support SCSI parity. The default setting is **Enabled.**

Host Adapter SCSI Termination

A set of resisters, called Terminators, must be either installed in or enabled on the first and last SCSI devices on each SCSI bus. Without termination, the devices will not operate properly. The adapter is usually the SCSI device at one end of the bus and will cause the termination to be enabled by default. On default, termination is enabled for the low byte (bits 0-7) and high byte (bits 8-15) of the SCSI bus. Refer to the following to set termination:

- Low ON / High ON (the default) - Adapter is at end of SCSI bus; the bus has only 8-bit devices or only 16-bit devices.
- Low ON / High ON - Adapter is at end of SCSI bus; the bus has 8-bit and 16-bit SCSI devices. Last device must be 16-bit and terminated.
- Low OFF / High OFF - Adapter is not at end of SCSI bus; the bus has only 16-bit SCSI devices.
- Low OFF / High ON - Adapter is not at end of SCSI bus; the bus has both 8-bit and 16-bit SCSI devices

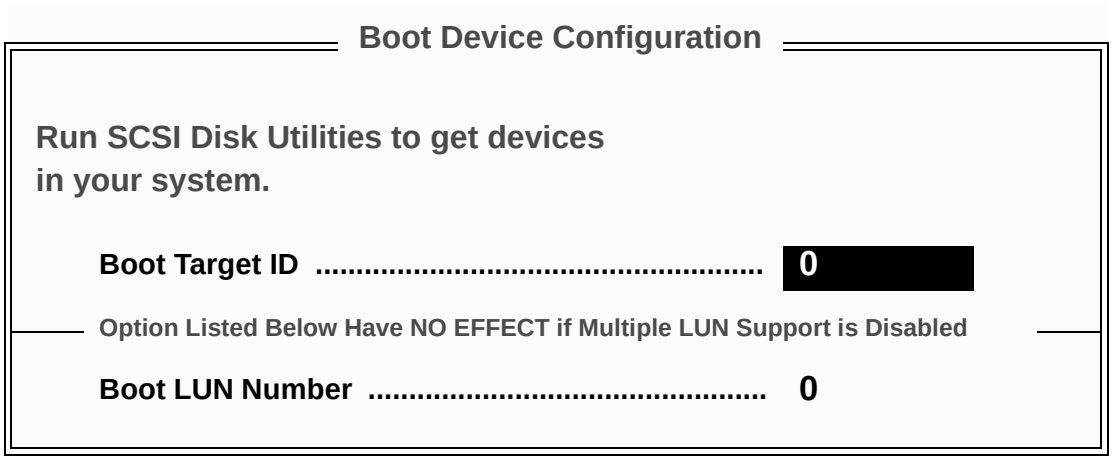
Additional Options

Boot Device Options

With the Boot Device options the user specifies the boot device. The default boot device is SCSI ID 0 and logical unit number (LUN) 0. To specify a different boot device, choose a different SCSI ID: ID 0 through 7 on 8-bit adapters, or ID 0 through 15 on 16-bit adapters. The Boot Target ID default is **0**.

The operator must also specify the boot logical unit number (LUN). If the boot device has multiple logical, units this LUN can be 0 through 7 (on 8-bit or 16-bit adapters).

The Boot LUN Number default is **0**.



SCSI Device Configuration

Each device on the SCSI bus requires configuration parameters that must be defined prior to device operation. These configuration parameters define how devices will transfer command and data information on the bus. The SCSI Device Configuration default options are shown in the menu illustration shown below.

SCSI Device Configuration

SCSI Device ID	#0	#1	#2	#3	#4	#5	#6	#7
Initiate Sync Negotiation	yes	yes	yes	yes	yes	yes	yes	yes
Maximum Sync Transfer Rate	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
Enable Disconnection	yes	yes	yes	yes	yes	yes	yes	yes
Initiate Wide Negotiation	yes	yes	yes	yes	yes	yes	yes	yes
Option Listed Below Have NO EFFECT if Multiple BIOS Support is Disabled								
Send Start Unit Command	no	no	no	no	no	no	no	no
SCSI Device ID	**#8**	**#9**	**#10**	**#11**	**#12**	**#13**	**#14**	**#15**
Initiate Sync Negotiation	yes	yes	yes	yes	yes	yes	yes	yes
Maximum Sync Transfer Rate	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
Enable Disconnection	yes	yes	yes	yes	yes	yes	yes	yes
Initiate Wide Negotiation	yes	yes	yes	yes	yes	yes	yes	yes
Option Listed Below Have NO EFFECT if Multiple BIOS Support is Disabled								
Send Start Unit Command	no	no	no	no	no	no	no	no

Initiate Sync Negotiation

Setting the Synchronous Negotiation to yes allows the SCSI adapter and its attached SCSI devices to transfer data in synchronous mode. Such transfer is faster than asynchronous data transfer.

The default setting is **Yes** causing the adapter to initiate synchronous negotiation with the SCSI device. Setting the value to *No* causes the adapter to not initiate synchronous negotiation; however, the adapter

always responds to synchronous negotiate if the SCSI device initiates it. If neither the adapter nor the SCSI device negotiates for synchronous data transfer, data is transferred in asynchronous mode.

The majority of SCSI devices support synchronous negotiation. If a device does not support synchronous negotiation, then the adapter automatically transfers the data in asynchronous mode.

Maximum Synchronous Transfer Rate

The maximum synchronous transfer rate that the adapter will negotiate is defined by this setting. The default rates of the transfer are defined in the above SCSI Device Configuration menu. The adapter automatically negotiates for the rate requested by the device. The default setting is **20.0** for all devices.

If the adapter is set to *not* negotiate for the synchronous data transfer, then the value selected is the maximum rate at which the adapter accepts data from the device during negotiation. This is standard SCSI protocol.

Enable Disconnection

This menu item defines whether the SCSI device may disconnect from the SCSI bus. The disconnect/reconnect function allows the adapter to perform other operations on the SCSI bus while the SCSI device is temporarily disconnected. The default setting is **Yes**, meaning that the SCSI device may disconnect.

The device may contain the logic to decide not to disconnect even if it is permitted by the adapter setting. This can be configured on the SCSI device. The SCSI device cannot disconnect from the SCSI bus when the Enable Disconnect is set to *No*.

The Enable Disconnection should be set to *yes* if the adapter connects to two or more SCSI devices. This will optimize SCSI bus performance. If the adapter connects to only one SCSI device, set the item to *No* to achieve better performance.

Initiate Wide Negotiation

Leave this option set to *yes*. The adapter will not attempt wide negotiation with 8-bit devices even if the bus is set to wide. This allows the adapter to initiate wide negotiation with 16-bit devices. The default setting is **Yes**.

Send Start Unit Command

This function serves to reduce the load on the computer's power supply. Enabling the option allows the adapter to turn on SCSI devices sequentially during boot-up. Specifically, the setting defines whether the adapter sends the Start Unit command to the SCSI device. This is the SCSI command 1B. The default settings is **No**.

The SCSI BIOS must be enabled before you can enable this option for the device.

If you enable the Send Start Unit Command for more than one SCSI device, the adapter sends the Start Unit command to the boot device as defined in the Boot Device Configuration menu (page D-5). After this device responds, Start Unit commands are sent to the additional devices, beginning with the device with the lowest SCSI ID. The boot time of the system is driven by the how long it takes to each drive to spin up.

Advanced Configuration Options

The SCSI BIOS includes advanced configuration setting. Users are discouraged from changing these options. The default settings are included in the following menu.

Advanced Configuration Options

Option Listed Below Have NO EFFECT if Multiple BIOS Support is Disabled

Host Adapter BIOS (Configuration Utility Reserves BIOS Space) ..	**Enable**
Support Removable Disks Under BIOS as Fixed Disks	**Boot only**
Extended BIOS Translation for DOS Drives > 1 GByte	**Enabled**
Display <Ctrl-A> Message During BIOS Initialization	**Enabled**
Multiple LUN Support	**Disabled**
Support for Ultra SCSI Speed	**Disabled**

Host Adapter BIOS

This setting enables or disables the SCSI BIOS. The BIOS must be enabled if you want the computer to boot from a SCSI hard disk drive connected to the adapter. The default setting is Enabled. All options on the Advanced Configuration Option menu are disabled with this option.

NOTE:

IF THE DEVICES ON THE SCSI BUS ARE CONTROLLED BY DEVICE DRIVERS THEN A BIOS FOR THESE IS NOT NECESSARY. THE SCSI BIOS CAN BE DISABLED TO FREE UP ABOUT 16 KBYTE OF MEMORY. THIS WILL ALSO REDUCE BOOT TIME BY 60 SECONDS.

Support Removable Disks Under BIOS as Fixed Disks

This option provides control of removable, media drives. The default is **Boot Only**. Selection options include:

Boot Only - The removable, media drive designated as the boot device is considered as a hard disk drive.

All Disks - The removable, media drives supported by the SCSI BIOS are considered as hard disk drives. There is no effect on drives under NetWare which automatically supports removable, media drives as fixed drives.

Disabled -No removable, media drives running under DOS are considered as hard disk drives. Driver software is necessary under these circumstances since the drives are not controlled by the BIOS.

Extended BIOS Translation for DOS Drives > 1 Gbyte

The SCSI BIOS includes an extended translation scheme that supports drives up to 8 Gbyte under MS-DOS. With this option enabled, drives managed by the BIOS use the extended translation if their formatted capacity is greater than 1 Gbyte. Standard translation is used on drives smaller than 1 Gbyte. The default is **Enabled**.

Back up disk drives before changing the translation scheme. All data is erased upon changing from one scheme to another.

Use the MS-DOS `fdisk` utility as normal to partition a disk larger than 1 Gbyte. The cylinder size increases to 8 Mbyte under extended translation; therefore, the partition size must be a multiple of 8 Mbyte. Requesting a size that is not a multiple of 8 Mbyte causes `fdisk` to round up to the nearest whole multiple of 8 Mbyte.

Display <Ctrl-A> Message During BIOS Initialization

The option controls the display of the boot prompt message:

```
Press <Ctrl><A> for SCSISelect (TM) Utility!
```

Designating the option as Enable causes the prompt to display during every computer boot. The default option is **Enabled**. The default option hot key sequence is <**Ctrl-A**>. This can be altered by editing the `absegs.inc` file.

Multiple LUN Support

This option allows the BIOS to support multiple logical units for any device. The default entry is **Disabled**.

Support For Ultra SCSI Speed

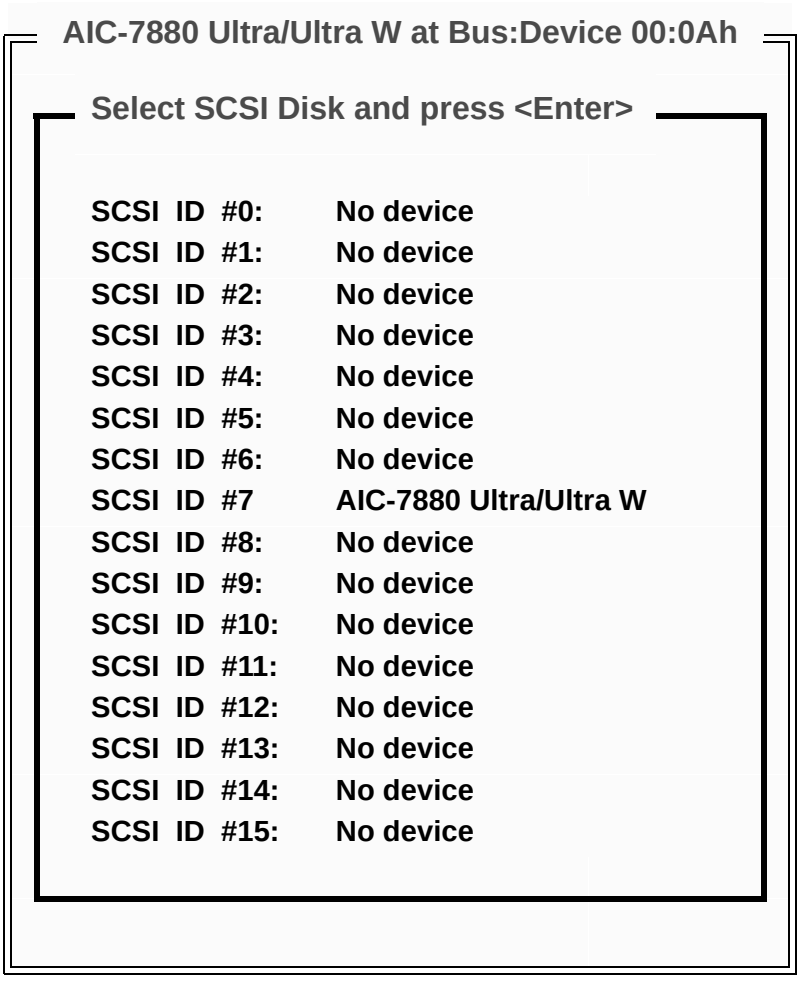
This option appears only if the BIOS is configured to include Ultra SCSI support. To support Ultra SCSI speeds, the option must be Enabled, and the Jumper J14 on the VMIVME-7588 CPU board must be open. The default entry is **Disabled** and the Jumper J14 is installed.

SECTION 3 - SCSI DISK UTILITIES

The SCSI Disk Utilities allow the users to perform disk setup and configuration operations. These operations include listing SCSI IDs of the devices on the host adapter, formatting SCSI disk drives, and checking drives for defects.

Select SCSI Disk

To list and select SCSI ID's of devices, select SCSI Disk Utilities from the main menu. This allows the user to view the list of current SCSI devices and their SCSI ID Number and insure that no duplicates are present.



Selection of a device allows the operator to format or verify the disk on the device.

Formatting a Disk

Most SCSI drives are preformatted; however, if formatting is necessary, the operator can use the SCSI BIOS to perform a low-level format on the drive. The formatting is compatible with most SCSI disk drives. The operating system's partitioning and high-level formatting utilities, such as MS-DOS `fdisk` and `format`, require that a disk have a low-level format. To format a disk:

- Select the device from the list of SCSI devices that you want to format.
- From the submenu that appears, select Format disk.
- At the confirmation prompt, select **Yes** to format, or **No** to cancel.

```
**************
*  CAUTION   *
*            *
**************
```

YOU CANNOT ABORT FORMATTING ONCE IT HAS STARTED.

Verifying a Disk

Using the Verify Disk option, the operator can scan a device for defects. If bad blocks are found by the utility, the operator is prompted to reassign them so they are not further used. To conduct a verify:

- Select the device from the list of SCSI devices that you want to Verify.
- From the submenu that appears, select Verify disk.
- At the confirmation prompt, select **Yes** to reassign the bad blocks, or **No** to not alter and leave as is.
- To abort the verification, press **Esc** at any time.

APPENDIX

E

Device Configuration: I/O and Interrupt Control

IN THIS APPENDIX:

SECTION 1 - INTRODUCTION

This appendix provides the user with the information needed to develop custom applications for the VMIVME-7588. The CPU board on the VMIVME-7588 is unique in that the BIOS can not be removed; it must be used in the initial boot cycle. A custom application, like a revised operating system for example, can only begin to operate after the BIOS has finished initializing the CPU. The VMIVME-7588 will allow the user to either maintain the current BIOS configuration or alter this configuration to be more user specific, but this alteration can only be accomplished after the initial BIOS boot cycle has completed.

When the VMIVME-7588 is powered on, control immediately jumps to the BIOS. The BIOS initiates a Power-on Self Test (POST) program which instructs the microprocessor to initialize system memory as well as the rest of the system. The BIOS establishes the configuration of all on-board devices by initializing their respective
I/O and Memory addresses and interrupt request lines. The BIOS then builds an interrupt vector table in main memory, which is used for interrupt handling. The default interrupt vector table and the default address map is described in Chapter 3 of this manual. Finally, the BIOS

jumps to the hard drive or floppy drive to execute the operating system's boot program. This is the point at which a custom operating system could take over control of the board and proceed with a custom configuration and/or custom application. A user application could override the configuration set by the BIOS and reconfigure the system or it could accept what the BIOS initialized.

There are two areas on the VMIVME-7588 with which the user must be familiar in order to override the initial BIOS configuration. These include the device addresses and the device interrupts. This appendix reviews the details of these addresses and interrupts, and provides a reference list for the individual devices used on the board.

The VMIVME-7588 utilizes the high performance Peripheral Component Interconnect (PCI) bus along with the Industrial Standard Architecture (ISA) bus. In general, the PCI bus is plug-and-play compatible. The components that are connected to the PCI bus are not always placed at a standard I/O or Memory address nor are they connected to a standard interrupt request line as is the case with ISA bus devices. These PCI bus devices are re-established by the BIOS meaning that these devices will not always be located at the same address or connected to the same interrupt request line every time the CPU is booted. This appendix lists the defaults that are found by powering-up a specific VMIVME-7588.

Functional Overview and References

The block diagram included in Figure E-1 on page E-3 illustrates the VMIVME-7588 emphasizing the I/O features, including the optional PCI-to-VMEbus bridge.

The circled number in the upper left corner of a function block references the appropriate data book necessary for the programming of the function block.

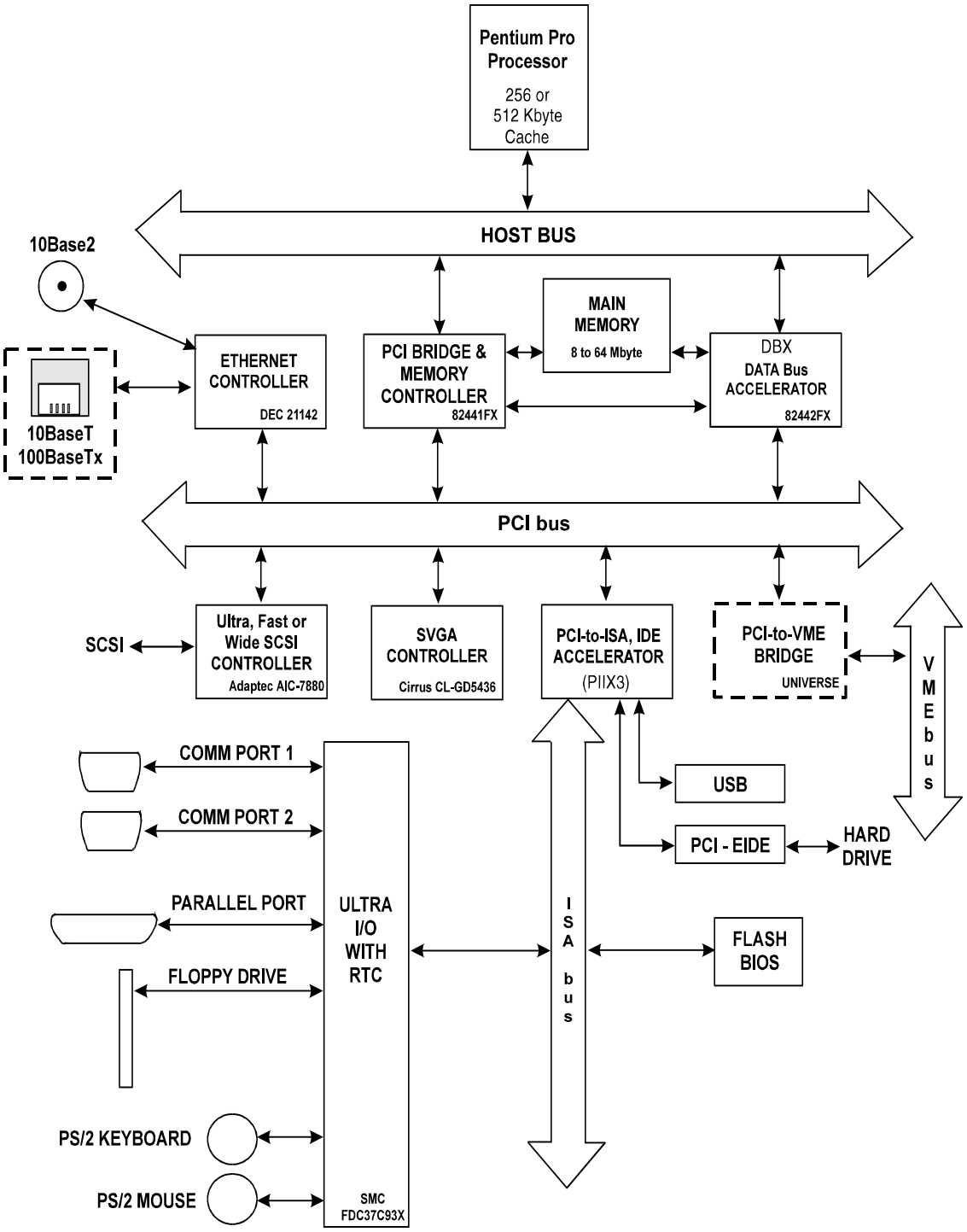


Figure E-1 VMIVME-7588 Block Diagram

Data Book References

1. Intel 82430HX PCIset Cache / Memory Subsystem
   82439HX System Controller (TXC)
   Intel Corporation
   2200 Mission College Boulevard
   P.O. Box 58119
   Santa Clara, CA 95052-8119

2. Intel 82430HX PCIset ISA Bridge
   82371FB PCI ISA IDE Xcellerator (PIIX3)
   Same: Intel Corporation

3. Adaptec AIC-7880 Ultra / Fast SCSI Host Adapter
   Adaptec, Inc.
   691 South Milpitas Boulevard
   Milpitas, CA 95035

4. Cirrus Logic Alpine VGA Family - CL-GD543X / '4X
   Technical Reference Manual, February 1995
   Cirrus Logic
   3100 West Warren Avenue
   Fremont, CA 94538
   (510) 623-8300

5. SMC FDC37C93X Plug-and-Play Compatible Ultra I / O Controller
   SMC Component Products Division
   300 Kennedy Drive
   Hauppauge, NY. 11788
   (516) 435-6000
   FAX (516) 231-6004

6. Digital Semiconductor 21142 10 / 100 Mb / s Ethernet LAN Controller
   Digital Equipment Corporation
   Maynard, Mass.
   1-800-332-2717

7. VMIVME-7588 User Manual
   500-007588-000 Product Manual
   500-007588-001 VMIVME-7588, Tundra Universe™-Based VMEbus
   Interface Option, Product Manual

8. PCI Local Bus Specification, Rev 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

9. ISA & EISA, Theory and Operation
Solari, Edward
Annabooks
15010 Avenue of Science, Suite 101
San Diego, CA 92128, USA
ISBN 0-929392 -15-9

SECTION 2 - DEVICE ADDRESS DEFINITION

The standard PC / AT architecture defines two distinctive types of address spaces for the devices and peripherals on the CPU board. These spaces have typically been named Memory address space and I / O address space. The boundaries for these areas are limited to the number of address bus lines that are physically located on the CPU board. The VMIVME-7588 has 32 address bus lines located on the board, thereby defining the limit of the address space as 4 gigabytes. The standard PC / AT architecture defines Memory address space from zero to 4 gigabytes and the separate I / O address space from zero to 64 kilobytes.

ISA Devices

The ISA devices on the VMIVME-7588 are configured by the BIOS at Boot-up and fall under the realm of the standard PC / AT architecture. They are mapped in I / O address space within standard addresses and their interrupts are mapped to standard interrupt control registers. However, all of the ISA devices with the exception of the real-time clock and the keyboard are re-locatable to almost anywhere within the standard 1 Kbyte of I / O address space. Table 1 on page E-7 defines the spectrum of addresses available for reconfiguration of ISA devices.

As previously stated, in the standard PC / AT system, all I / O devices are mapped in
I / O address space; however, one exception exists. The Dynamic Random Access Memory (DRAM) is addressed in Memory address space. The BIOS places DRAM at address zero and extends to the physical limit of the on-board DRAM.

Table E-1 ISA Device Mapping Configuration

DEVICE	MEMORY SPACE	I/O ADDRESS SPACE	PIC INTERRUPT OPTIONS	BYTE ADDRESS BOUNDARY	DEFAULT
Floppy	N/A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$3F0
Parallel Port	N/A	[0x100 - 0xFFC] [0x100 - 0xFF8]	IRQ1 - IRQ15	4 8	$378
Serial Port 1	N/A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$3F8
Serial Port 2	N/A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$2F8
Real Time Clock	Non - Relocatable				
Keyboard	Non - Relocatable				
Auxiliary I/O	N/A	- Primary I/O [0x000 - 0xFFF] - Secondary I/O [0x000 - 0xFFF]	IRQ1, IRQ3-IRQ15	1 1	

PCI Devices

PCI devices are fully configured under I/O and/or Memory address space. Table 1 describes the PCI bus devices that are on-board the VMIVME-7588 along with each device's configuration spectrum.

The PCI bus includes three physical address spaces. As with ISA bus, PCI bus supports Memory and I/O address space, but PCI bus includes an additional Configuration address space. This address space is defined to support PCI bus hardware configuration (refer to the PCI bus Specification for complete details on the configuration address space). PCI bus targets are required to implement Base Address registers in configuration address space to access internal registers or functions. The BIOS uses the Base Address register to determine how much space a device requires in a given address space and then assigns where in that space the device will reside. This functionality enables PCI devices to be located in either Memory or I/O address space.

Table E-2 PCI Device Mapping Configuration

DEVICE	MEMORY SPACE	I/O ADDRESS SPACE	PIC INTERRUPT OPTIONS	DEFAULT
SVGA	Anywhere	N/A	N/A	
SCSI	Anywhere	Anywhere	PCI Defined	
Universe** PCI-to-VMEbus Bridge	Anywhere	N/A	PCI Defined	
Ethernet	Anywhere	Anywhere	PCI Defined	

** refer to the VMIVME-7588-001 Users Manual

SECTION 3 - DEVICE INTERRUPT DEFINITION

PC/AT Interrupt Definition

The interrupt hardware implementation on the VMIVME-7588 is standard for computers built around the PC/AT architecture. The PC/AT evolved from the IBM PC/XT architecture. In the IBM PC/XT systems, only eight Interrupt Request (IRQ) lines exist, numbered from IRQ0 to IRQ7. These interrupt lines were included originally on a 8259A Priority Interrupt Controller (PIC) chip.

The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave 8259A PIC into the original master 8259A PIC. The interrupt line IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This master/slave architecture, the standard PC/AT interrupt mapping, is illustrated in Figure E-2 on page E-10 within the PCI-ISA Bridge PIIX3 82371FB section of the diagram.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin on the AT Expansion Bus (or ISA bus).

The BIOS defines the PC/AT interrupt line to be used by each device. The BIOS writes to each of the two cascaded 8259A PIC chips an 8-bit vector which maps each IRQx to its corresponding interrupt vector in memory.

ISA Device Interrupt Map

The VMIVME-7588 BIOS maps the IRQx lines to the appropriate device per the standard ISA architecture. Reference Figure E-2 on page E-10. This initialization operation can not be changed; however, a custom application could reroute the interrupt configuration after the BIOS has completed the initial configuration cycle.

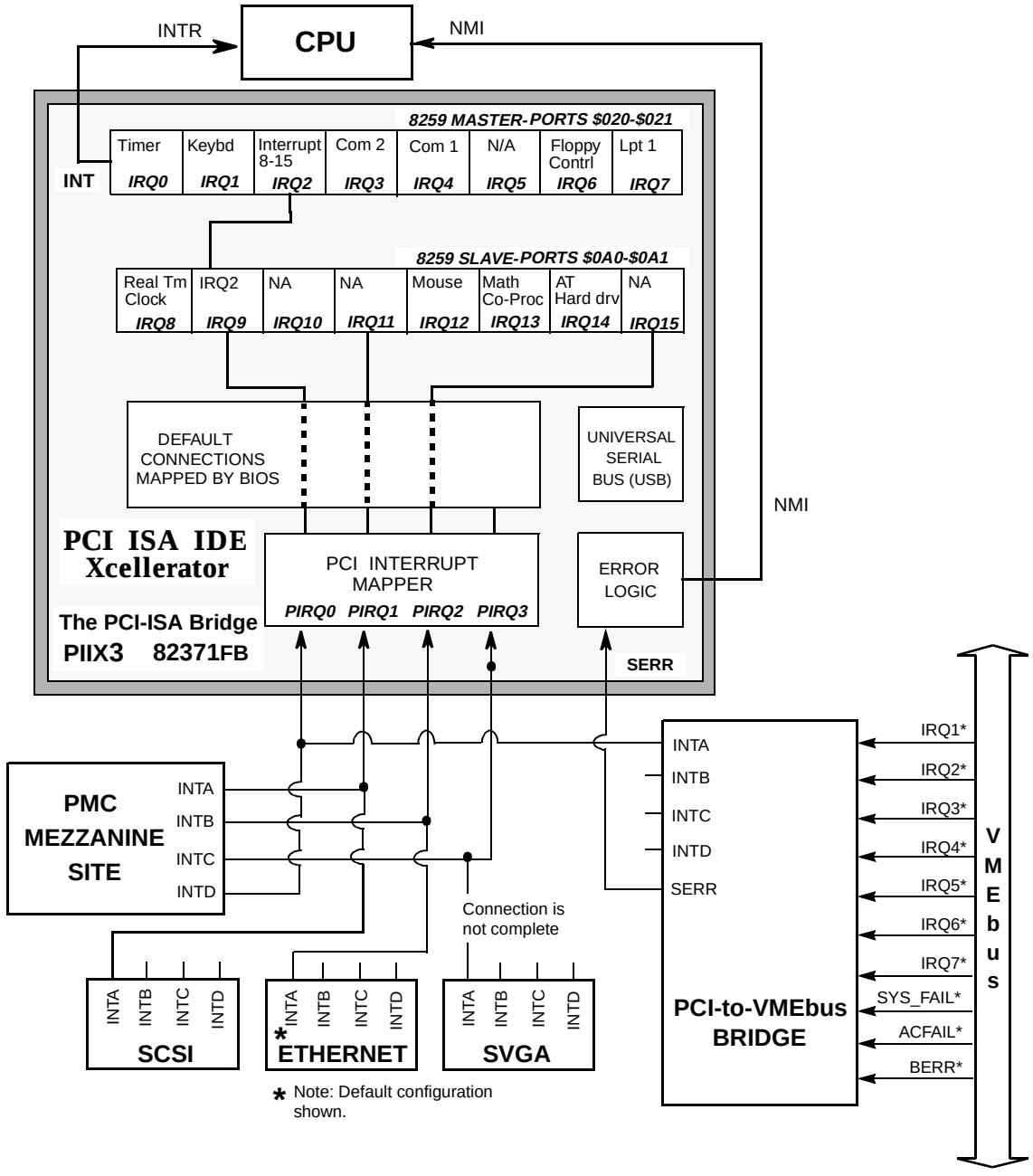


Figure E-2 BIOS Default Connections for the PC Interrupt Logic Controller

PCI Device Interrupt Map

The PCI bus based external devices include the PCI Mezzanine Card (PMC) mezzanine site, the SCSI-2 Controller, the PCI-to-VMEbus bridge, and the VGA reserved connection. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the PIIX3. This mapping is illustrated in Figure E-2 on page E-10 and is defined in Table 1.

The device PCI interrupt lines (INTA through INTD) that are present on each device *cannot* be modified.

Table E-3 Device PCI Interrupt Mapping by the BIOS

DEVICE	COMPONENT	VENDOR ID	DEVICE ID	CPU ADDRESS MAP ID SELECT	DEVICE PCI INTERRUPT	MOTHER-BOARD PCI INTERRUPT MAPPER	DATA BOOK REF. NO.	REVISION ID
PCI-VME Bridge Option: Tundra Universe™	Universe CA91C042	0x10E3	0x0	AD19	INTA	PIRQ0	7	N / A
	PLX PCI9060ES	0x114A	0x0001	AD20	N / A	N / A	7	N / A
PMC SITE	N / A	Board Specific	Board Specific	AD23	INTA	PIRQ1	N / A	N / A
	N / A	Board Specific	Board Specific	N / A	INTB	PIRQ2	N / A	N / A
	N / A	Board Specific	Board Specific	N / A	INTC	PIRQ3	N / A	N / A
	N / A	Board Specific	Board Specific	N / A	INTD	PIRQ0	N / A	N / A
PCI ISA Bridge	PIIX3 82371FB Function 00	0x8086	0x7000	AD18	N / A	N / A	2	N / A
SCSI Controller	Adaptec AIC-7880	0x9004	0x8078	AD21	INTA	PIRQ1	3	N / A
SVGA Controller	Cirrus CL-GD5436	0x1013	0x00B8	AD24	INTA**	PIRQ3**	4	N / A
Ethernet Controller	DEC 21142	0x1011	0x0019	AD22	INTA	PIRQ2	6	N / A
PCI IDE Controller	PIIX3 82371FB Function 01	0x8086	0x7010	AD18	N / A	N / A	2	N / A
Universal Serial Bus (USB)***	PIIX3 82371FB Function 02	0x8086	0x7020	AD18	INTD	PIRQ3	2	N / A
PCI Host Bridge	Intel 430 HX	0x8086	0x1250	N / A	N / A	N / A	1	N / A

* To access these parts use the revision number as the distinguishing factor.

** Not connected, for reference only

*** PIRQ3 interrupt is not enabled by the BIOS.

The motherboard accepts these PCI device interrupts through the PCI interrupt mapper function. The BIOS default maps the PCI Interrupt Request (PIRQx) external device lines to one of the available slave PIC Interrupt Request lines, IRQ(9, 10, 11, or 15). The BIOS default mapping of the PIRQx to the slave PIC is defined in Table 4.

Table E-4 Default PIRQx to IRQx BIOS Mapping

PCI INTx	PIC IRQx
PIRQ0	IRQ9
PIRQ1	IRQ11
PIRQ2	IRQ15

Using the interrupt steering registers of the 82371FB PIIX3, the user can override the BIOS defaults and map any of the PCI interrupts (PIRQ0-3) to any of the following PIC IRQx (ISA) interrupts: IRQ15, 14, 12-9, or 7-3.

****
* CAUTION *
****

IF PCI INTERRUPTS ARE REMAPPED BY THE USER, CARE MUST BE TAKEN TO INSURE THAT ALL ISA AND PCI FUNCTIONS THAT REQUIRE AN INTERRUPT ARE INCLUDED.

Index

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S

T

U

V