Ascor 3000-62

128 TTL I/O Compatible Driver VXI Module

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Model 3000-62
128 Channel TTL I/O
90400840

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Regulatory compliance information

This product complies with the essential requirements of the following applicable European Directives, and carries the CE mark accordingly.

89/336/EEC and 73/23/EEC	EMC Directive and Low Voltage Directive
EN61010-1 (1993)	Electrical Safety
EN61326-1 (1997)	EMC – Emissions and Immunity
Manufacturer's Name:	**Manufacturer's Address**
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Type of Equipment:	**Model Series Number**
Switching Module	3000-62

Declaration of Conformity on file. Contact Giga-tronics at the following;

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Record of Changes to This Manual

Use the table below to maintain a permanent record of changes to this document. Corrected replacement pages are issued as Technical Publication Change Instructions (TPCI). When you are issued a TPCI, do the following:

1. Insert the TPCI at the front of the manual binder.
2. Remove the pages from the manual binder that are noted in the TPCI.
3. Replace the page(s) removed in the previous step with the corrected page(s).
4. Record the changes in the table below.

TPCI Number	TPCI Issue Date	Date Entered	Comments

Revision History			
Revision	**Description of Change**	**Chg Order #**	**Approved By**
A	Initial Release 4/05		
B	Updated		
C	Reformatted 3/12		RCW

Contents

Chapter 1 **Introduction**

1.1 Safety and Manual Conventions

This manual contains conventions regarding safety and equipment usage as described below.

1.1.1 Product Reference

Throughout this manual, the term “Common Core Switching Platform, Series 8800” refers to all models of within the series, unless otherwise specified.

1.1.2 Personal Safety Alert

WARNING: Indicates a hazardous situation which, if not avoided, could result in death or serious injury.

1.1.3 Equipment Safety Alert

CAUTION: Indicates a situation which can damage or adversely affect the product or associated equipment.

1.1.4 Notes

Notes are denoted and used as follows:

NOTE: Highlights or amplifies an essential operating or maintenance procedure, practice, condition or statement.

1.1.5 Electrical Safety Precautions

Any servicing instructions are for use by service-trained personnel only. To avoid personal injury, do not perform any service unless you are qualified to do so.

For continued protections against fire hazard, replace the AC line fuse only with a fuse of the same current rating and type. Do not use repaired fuses or short circuited fuse holders.

Chapter 2 **Configuration Table**

OPTION 2 (L)

PL90400840
Assy90400840
MB PL85002350
Assy85002350
SCH85002350
DB PL85002360
Assy85002360
SCH85002360

OPTION 1 (A)

PL90400840-001
Assy90400840
MB PL85002350
Assy85002350
SCH85002350
DB PL85002370
Assy85002370
SCH85002370

STANDARD MODEL

PL90400840-002
Assy90400840-002
MB PL85002350
Assy85002350
SCH85002350
DB PL85002360
Assy85002360
PL85002360

OPTION3

PL90400840-003
Assy90400840-003
MB PL85002350
Assy85002350
SCH85002350
DB PL85002630
Assy85002630
SCH85002630

OPTION4

PL90400840-004
Assy90400840-004
MB PL85002350-001
Assy85002350-001
SCH85002350
DB PL85002890
Assy85002890
SCH85002890

Chapter 3 **Functional Description**

3.1 Introduction

This publication provides the necessary information for the maintenance and programming of the Model 3000-62 Digital I/O Module. This section provides general information and specifications.

3.2 General Description

The standard Model 3000-62 is a digital input/output module with 128 TTL driver channels terminated with 330/680 ohm terminators. The following options are available.:

Option 1: Optional daughterboard provides an additional 128 TTL channels terminated with 1K ohm resistors.

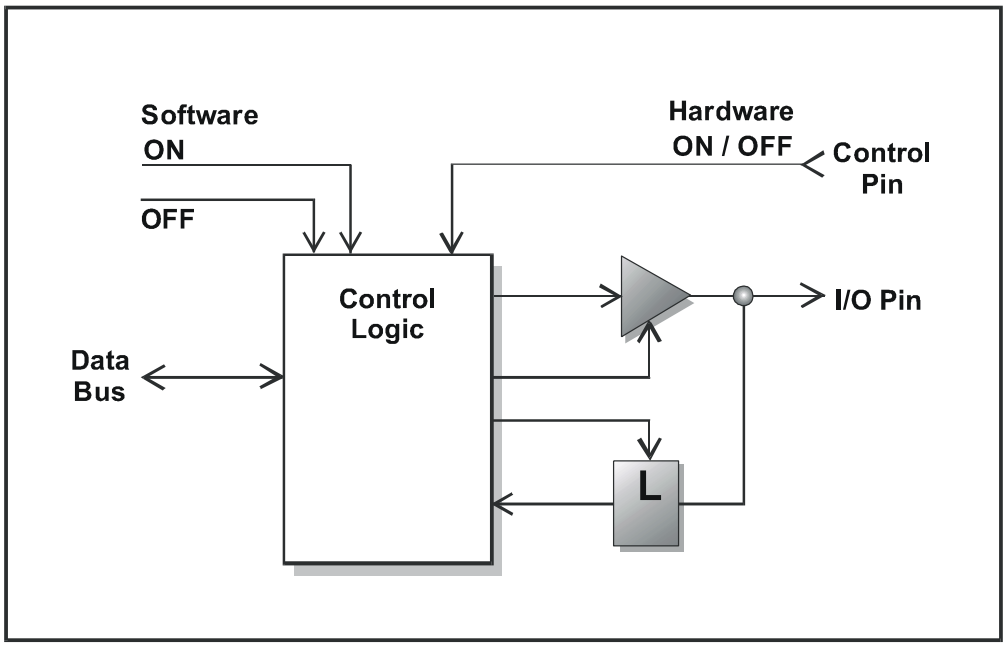
Option 2: Optional daughterboard provides 32 channels of CMOS, Differential, and Open Collector Drivers.

Option 3: Optional daughterboard provides 64 channels of Differential I/O.

Option 4: Optional daughterboard provides 128 high current relay drivers plus 16 TTL I/O channels.

Note: All options are mutually exclusive.

Chapter 4 Block Diagram



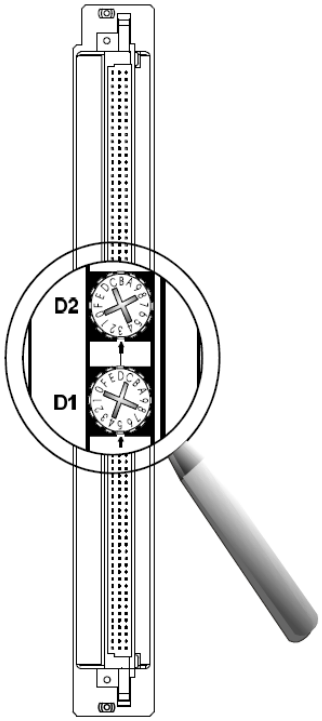
Typical Channel

Chapter 5 Controls and Indicators

The following controls and indicators are provided to select and display the functions of the ASCOR 3000-62 Module's operating environment.

5.1 VXI Logical Address

The Logical Address Switch is dual circular switches, D1 and D2 which are located at the rear of the module. The address can be set to any value between 1 and 255 (decimal) or 1 and FF (hexadecimal), (address 0 is reserved for the resource manager). However, the Module fully supports Dynamic Configuration as defined in ***Section F of the VXI specification,*** address 255 (FF) should be selected only if the Resource Manager also supports Dynamic Configuration.



5.2 LEDs

The following LEDs are visible at the Module's front panel to indicate the

status of the module's operation:

5.2.1 "BUS" LED

This green color LED is normally off and will flash on when the module is addressed by the system.

5.2.2 "PWR" LED

This red color LED is normally on when the Module is Powered up.

Chapter 6 **Internal Settings**

The following items are inside the module and can be reached by removing the side cover.

6.1 Fuse

The ASCOR VXI 3000-62 uses a 10 Amp fuse in the +5 Volt line and is located on the Mother Board (MB) assembly.

6.2 VXI_{bus} Interrupt Level Selection

The VXIbus interrupt level is set with three bits in the “3Eh” register.

See the section on “A16 ADDRESS SPACE REGISTER DESCRIPTION”.

The interrupt level is factory set to “no interrupt”.

Chapter 7 **Specifications**

Electrical:

Power Consumption:	+5Volts, 3.92 Amps, with all outputs HI-Z.
Fuse Rating:	7 Amps
DIFF IC DRIVER :	TI-AM26LS31-SM, MEETS RS-422 SPEC
O.C. IC DRIVER:	TI-SN74BCT760DW, Iol=64ma
CMOS IC DRIVER:	TI-SN74ABT16541DL, Iol=64ma,Ioh=32ma

Mechanical:

Thickness:	1.200 inches
Width:	10.317 inches
Length:	13.78 inches
Weight:	3 lbs.

Connectors:

Options 1, 2 & 3 (J1 through J4):	PCA connector: Airborn # WTB70PR7J
Mating connector:	Airborn # WTBXA70SAJTL
Installation Kit:	89800470 contains four mating connectors and four hoods.
Option 4 (J1 & J2):	
Mating connector:	Airborn # WTBXA70SAJTL.
Option 4 (J3 & J4):	
Mating connector:	Robinson Nugent # P50E100STG
Standard Model (J1 & J2):	
Mating connector:	Airborn # WTBXA70SAJTL.

Environmental Specifications

Temperature:	
Operating:	0º to 55ºC
Storage:	- 40º to 75ºC
Relative Humidity:	
Operating:	0 to 90% non-condensing
Storage:	0 to 95% non-condensing

Chapter 9 Register Map

The Model 3000-62 is VXI register based and supports VXIbus register maps.

Registers on the Model 3000-62 can be accessed by the following VXI system configurations:

- Slot 0 computers.
- Host computers with VXI-MXI
- Host computers with GPIB and GPIB-VXI slot 0 controllers.

The Model 3000-62 is not message based and does not support VXIbus communication protocols.

9.1 Module Registers

The Model 3000-62 registers control the motherboard and daughterboard. These registers are listed herein. The registers are controlled by a high-speed VXIMAX™ 16/32 VXIbus interface. Because of VXIMAX™, registers can be programmed as 16-bit or 32-bit words (in D16 or D32 mode) as desired, with no special configuration or upgrade procedures required.

9.2 Register Addresses

Module register address assignment is controlled by the Resource Manager. The Resource Manager sets the Offset (VXI Configuration) Register at A16 (06h offset) and this defines the A24/A32 Base Address. The unique A24/A32 Base Address is reassigned each time the Resource Manager initiates. This Base Address determines the address of each module register.

You can read the Offset Register at A16 (06h offset) to obtain the A24 Base Address. After reading the Offset Register, map the first (most significant) eight (8) bits of the Offset Register to the first eight (8) bits of the A24 Base Address. To obtain an A32 Base Address, map the first 16 bits of the Offset Register to the first 16 bits of the A32 Base Address. Set all other bits of either Base Address to zeroes.

To obtain the A16 Base Address, use the following formula:

A16 Base Address = C000h + (Logical Address x 64h)+49152

For purposes of interface library calls, the address of each register on the Model 3000-62 is the sum of the following:

	The A24/A32 Base Address.
	Offset of 8000h or 8100h (motherboard or daughterboard)
+	*The register number minus 1 times 2 or 4 (16-bit or 32-bit address factor); if the register number is 1 then no change*
=	*Module register address.*

9.3 Register Programming

The VXI Device registers start at an offset of 0h from the A16 Base Address and are programmed as 16-bit words. See Table 9-1 on page 17.

The registers that control the motherboard start at an offset of 8000h from the A24/A32 Base Address; the registers that control the daughterboard start at an offset of 8100h. Module registers can be accessed as either 16-bit or 32-bit words. Under 16-bit (D16) mode, address offsets increment by 2h. Under 32-bit (D32) mode, address offsets increment by 4h.

The tables that follow show the offsets and bit number for both methods. These tables are:

Table 9-2 on page 19 (motherboard)

Table 9-3 on page 38 (daughterboard PN 85002360 Option 2)

Table 9-4 on page 38, (daughterboard PN 85002370 Option 1), and

Table 9-5 on page 68, (daughterboard Option 4).

Write to VXI or module registers through your VXI controller.

Further explanations of the motherboard and daughterboard—or PN 85002370 Option 1-- module registers are under “

Motherboard and Daughterboard Registers" on page 75.

Table 9-1. VXI Device Registers, A16 Memory Map

Section 3VXI Configuration Registers			
Section ode:	**Section 5 6-bit**	*Section 6ID Register (read) / Logical Address Register (write)*	**Value:** *CFB5h or DFB5h*
Section ffset:	Section 8 0h	*A read of this 16-bit register provides device class, Address Space(s) used, and manufacturer ID. Preserve all bit values of this register–do not write–used by Resource Manager. For A24/32 Address Space, see "Description Motherboard" on page 75.*	
	Section 9 it	Section 10Bit Description	
	15–14	Section 11Device Class = 11b. The 3000-62 is register based.	
	13–12	Section 12Address Space = 00b. A16/A24 operational register address mode. = 01b. A16/A32 operational register address mode.	
	11–0	Section 13Manufacturer ID = FB5h. Unique ASCOR ID.	
Section ode:	**Section 1 6-bit**	*Section 16Device Type Register (read/write)*	**Value:** *7D1Ch or FD1Ch*
Section ffset:	Section 1 2h	*A read of this 16-bit register provides how much VMEbus memory required and unique model code. Preserve all bit values of this register–do not write–used by Resource Manager.*	
	Section 1 it	Section 20Bit Description	
	15–12	Section 21Required Memory = 7h. 64K bytes in A24 Address Space. = Fh. 64K bytes in A32 Address Space.	
	11–0	Section 22Model Code = D1Ch. Unique model code.	
Section ode:	**Section 2 6-bit**	*Section 25Status/Control Register (read/write)*	**Value:** *FFFCh*
Section ffset:	Section 2 4h	*A read of this 16-bit register provides whether A24/A32 Address Space is active. Set bit 0 on then off to reset the module. Preserve all other bit values of this register–used by the Resource Manager after power-on initialization and/or for dynamic configuration.*	
	Section 2 it	Section 29Bit Description	
	15	Section 30Custom Register Status = 1b. A24/A32 VMEbus registers enabled.	
	11–2	Not used. Variable. Normally all on.	
	1	Section 31Sysfail Inhibit status = 0b. Not inhibited.	
	0	Section 32Device Reset = 0b. Normal operational mode. = 1b. Resets the module to its power-on state. See instructions above.	

Table 9-1. VXI Device Registers, A16 Memory Map, *Continued*

Section 33VXI Configuration Registers, Continued			
Section ode:	***Section 6-bit***	*Section 36Offset Register (read/write)*	***Value:*** *00xxh-FFxxh*
Section ffset:	*Section 6h*	*A read of this 16-bit register allows you to determine the A24 or A32 Base Address.* Preserve all bit values of this register–do not write–*used by the Resource Manager.*	
	Section 39Scenario 1: A24 Address Space configured		
	Section 4 it	*Section 41Bit Description*	
	15–8	***Section 42Offset Value*** = *0h-FFh. First eight bits of A24 Base Address. If Offset Register is:*	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	x	x	x	x	x	x	x	x

The A24 Base Address is:

23	22	21	20	19	18	17	16	15	14	13	12
0	0	1	0	0	0	0	0	0	0	0	0

Section 4

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0

7–0	*Section 44Not used.*	
Section 45Scenario 2: A32 Address Space configured		
Section 4 it	*Section 47Bit Description*	
15–0	***Section 48Offset Value*** = *0h-FFFFh. First sixteen bits of A32 Base Address. If Offset Register is:*	

Example 5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The A32 Base Address is:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Sec

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Examp
Exar

Section 50VXI Device Class Dependent Registers and VXI Device Dependent Registers			
Section ode:	***Section 6-bit***	*Section 53*	***Value:*** *not applicable*
Section ffset:	*Section 8h-3Ch*	*Section 56These registers are not used (02h each).*	
Section ode:	***Section 6-bit***	*Section 59Control Register (read/write)*	***Value:*** *variable*
Section ffset:	*Section Eh*	*A read of this 16-bit register provides the IRQ level.* Preserve all other bit values of this register–*used by the Resource Manager.*	
	Section it	*Section 63Bit Description*	
	15–6	*Section 64Not used. All Off.*	
	5–3	***Section 65Module IRQ Level*** = *0h. Interrupt disabled (default).* = *1h-7h. Corresponds to IRQ Level of 1-7. This is the VXI interrupt number generated if the module makes an interrupt request.*	
	2–0	*Section 66Not used.*	

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map

Section ffset:	*Section 68800 0h–80FFh*	*Section 69Used by the motherboard, PN 85002350, TTL channels 1 - 128*
		Section 70Control Registers
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, TTL Channels 1–16.*
Section ffset:	*Section 000h*	*Section 000h*	Section 77
	Section it	*Section it*	*Section 80Bit Description*
	15	*15*	Section 81*Not used, mask off.*
	14	*14*	Section 82*Not used, mask off.*
	13	*13*	Section 83*Not used, mask off.*
	12	*12*	Section 84*Not used, mask off.*
	11	*11*	*Latch Status* *0 = unlatches* *1 = latched.*
	10	*10*	*Output Data Polarity;* *0 = true (default)* *1 = complement of data written to 0x8030*
	9	*9*	*Latch Mode* *0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8040*
	8	*8*	*Gate Control Mode* *0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity* *0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode* *0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable* *0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode* *0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode* *0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity* *0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode* *0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction* *0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8050, 0x8054, 0x8090, and 0x8094.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 85Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 17–32.*
Section ffset:	*Section 002h*	*Section 000h*		
	Section it	*Section it*	*Section 94Bit Description*	
	15	*31*	Section 95*Not used, mask off.*	
	14	*30*	Section 96*Not used, mask off.*	
	13	*29*	Section 97*Not used, mask off.*	
	12	*28*	Section 98*Not used, mask off.*	
	11	*27*	Section 99*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x8032*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8042*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8058, 0x805C, 0x8090, and 0x8094.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 85Control Registers, Continued			
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, TTL Channels 33–48.*
Section ffset:	*Section 004h*	*Section 004h*	
	Section it	*Section it*	*Section 108Bit Description*
	15	*15*	Section 109*Not used, mask off.*
	14	*14*	Section 110*Not used, mask off.*
	13	*13*	Section 111*Not used, mask off.*
	12	*12*	Section 112*Not used, mask off.*
	11	*11*	Section 113*Not used, mask off.*
	10	*10*	*Output Data Polarity;* *0 = true (default)* *1 = complement of data written to 0x8034*
	9	*9*	*Latch Mode* *0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8044*
	8	*8*	*Gate Control Mode* *0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity* *0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode* *0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable* *0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode* *0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode* *0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity* *0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode* *0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction* *0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8060, 0x8064, 0x8090, and 0x8094.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 85Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 49–64.*
Section ffset:	*Section 006h*	*Section 004h*		
	Section it	*Section it*	*Section 122Bit Description*	
	15	*31*	Section 123*Not used, mask off.*	
	14	*30*	Section 124*Not used, mask off.*	
	13	*29*	Section 125*Not used, mask off.*	
	12	*28*	Section 126*Not used, mask off.*	
	11	*27*	Section 127*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x8036*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8046*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8068, 0x806C, 0x8090, and 0x8094.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 85Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 65–80.*
Section ffset:	*Section 008h*	*Section 008h*		
	Section it	*Section it*	*Section 136Bit Description*	
	15	*15*	Section 137*Not used, mask off.*	
	14	*14*	Section 138*Not used, mask off.*	
	13	*13*	Section 139*Not used, mask off.*	
	12	*12*	Section 140*Not used, mask off.*	
	11	*11*	Section 141*Not used, mask off.*	
	10	*10*	*Output Data Polarity;*	*0 = true (default)* *1 = complement of data written to 0x8038*
	9	*9*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8048*
	8	*8*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8070, 0x8074, 0x8090, and 0x8094.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 85Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 81–96.*
Section ffset:	*Section 00Ah*	*Section 008h*		
	Section it	*Section it*	*Section 150Bit Description*	
	15	*31*	Section 151*Not used, mask off.*	
	14	*30*	Section 152*Not used, mask off.*	
	13	*29*	Section 153*Not used, mask off.*	
	12	*28*	Section 154*Not used, mask off.*	
	11	*27*	Section 155*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x803A*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x804A*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8078, 0x807C, 0x8090, and 0x8094.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 85Control Registers, Continued			
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, TTL Channels 97–112.*
Section ffset:	*Section 00Ch*	*Section 00Ch*	
	Section it	*Section it*	*Section 164Bit Description*
	15	*15*	Section 165*Not used, mask off.*
	14	*14*	Section 166*Not used, mask off.*
	13	*13*	Section 167*Not used, mask off.*
	12	*12*	Section 168*Not used, mask off.*
	11	*11*	Section 169*Not used, mask off.*
	10	*10*	*Output Data Polarity;* *0 = true (default)* *1 = complement of data written to 0x803C*
	9	*9*	*Latch Mode* *0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x804C*
	8	*8*	*Gate Control Mode* *0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity* *0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode* *0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable* *0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode* *0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode* *0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity* *0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode* *0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction* *0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8080, 0x8084, 0x8090, and 0x8094.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 85Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 113–128.*
Section ffset:	*Section 00Eh*	*Section 00Ch*		
	Section it	*Section it*	*Section 178Bit Description*	
	15	*31*	Section 179*Not used, mask off.*	
	14	*30*	Section 180*Not used, mask off.*	
	13	*29*	Section 181*Not used, mask off.*	
	12	*28*	Section 182*Not used, mask off.*	
	11	*27*	Section 183*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x803E*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x804E*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8088, 0x808C, 0x8090, and 0x8094.*

Example 8.

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 184Compare Mask Registers				
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:*	*Compare Mask Register, TTL Channels 1–16.*
Section ffset:	*Section 1 010h*	*Section 1 010h*		
	Section 1 it	*Section 1 it*	*Section 193Bit Description*	
	15–0	*15–0*	*Channels 16–1*	*0 = channel does not participate in compare (default)* *1 = channel participates in compare*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:*	*Compare Mask Register, TTL Channels 17–32.*
Section ffset:	*Section 1 012h*	*Section 1 010h*		
	Section 2 it	*Section 2 it*	*Section 202Bit Description*	
	15–0	*31–16*	*Channels 32–17*	*0 = channel does not participate in compare (default)* *1 = channel participates in compare*
Section ode:	***Section 26-bit***	***Section 22-bit***	*Register Description:*	*Compare Mask Register, TTL Channels 33–48.*
Section ffset:	*Section 2 014h*	*Section 2 014h*		
	Section 2 it	*Section 2 it*	*Section 211Bit Description*	
	15–0	*15–0*	*Channels 48–33*	*0 = channel does not participate in compare (default)* *1 = channel participates in compare*
Section ode:	***Section 26-bit***	***Section 22-bit***	*Register Description:*	*Compare Mask Register, TTL Channels 49–64.*
Section ffset:	*Section 2 016h*	*Section 2 014h*		
	Section 2 it	*Section 2 it*	*Section 220Bit Description*	
	15–0	*31–16*	*Channels 64–49*	*0 = channel does not participate in compare (default)* *1 = channel participates in compare*
Section ode:	***Section 26-bit***	***Section 22-bit***	*Register Description:*	*Compare Mask Register, TTL Channels 65–80.*
Section ffset:	*Section 2 018h*	*Section 2 018h*		
	Section 2 it	*Section 2 it*	*Section 229Bit Description*	
	15–0	*15–0*	*Channels 80–65*	*0 = channel does not participate in compare (default)* *1 = channel participates in compare*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section ode:	***Section 2 6-bit***	***Section 2 2-bit***	*Register Description:* *Compare Mask Register, TTL Channels 81–96.*
Section ffset:	*Section 2 01Ah*	*Section 2 018h*	
	Section 2 it	*Section 2 it*	*Section 238Bit Description*
	15–0	*31–16*	*Channels 96–81* — *0 = channel does not participate in compare (default)*; *1 = channel participates in compare*
Section ode:	***Section 2 6-bit***	***Section 2 2-bit***	*Register Description:* *Compare Mask Register, TTL Channels 97–112.*
Section ffset:	*Section 2 01Ch*	*Section 2 01Ch*	
	Section 2 it	*Section 2 it*	*Section 247Bit Description*
	15–0	*15–0*	*Channels 112–97* — *0 = channel does not participate in compare (default)*; *1 = channel participates in compare*

Section 248Compare Mask Registers, Continued

Section ode:	***Section 2 6-bit***	***Section 2 2-bit***	*Register Description:* *Compare Mask Register, TTL Channels 113–128.*
Section ffset:	*Section 2 01Eh*	*Section 2 01Ch*	
	Section 2 it	*Section 2 it*	*Section 257Bit Description*
	15–0	*31–16*	*Channels 128–113* — *0 = channel does not participate in compare (default)*; *1 = channel participates in compare*

Example 9.

Section 258Compare Pattern Registers

Section ode:	***Section 2 6-bit***	***Section 2 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 1–16.*
Section ffset:	*Section 2 020h*	*Section 2 020h*	
	Section 2 it	*Section 2 it*	*Section 267Bit Description*
	15–0	*15–0*	*Channels 16–1* — *0 or 1 Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 2 6-bit***	***Section 2 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 17–32.*
Section ffset:	*Section 2 022h*	*Section 2 020h*	
	Section 2 it	*Section 2 it*	*Section 276Bit Description*
	15–0	*31–16*	*Channels 32–17* — *0 or 1 Each bit is compared against the state of its corresponding channel.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 33–48.*
Section ffset:	*Section 024h*	*Section 024h*	
	Section it	*Section it*	*Section 285Bit Description*
	15–0	*15–0*	*Channels 48–33* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 49–64.*
Section ffset:	*Section 026h*	*Section 024h*	
	Section it	*Section it*	*Section 294Bit Description*
	15–0	*31–16*	*Channels 64–49* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 65–80.*
Section ffset:	*Section 028h*	*Section 028h*	
	Section it	*Section it*	*Section 303Bit Description*
	15–0	*15–0*	*Channels 80–65* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 81–96.*
Section ffset:	*Section 02Ah*	*Section 028h*	
	Section it	*Section it*	*Section 312Bit Description*
	15–0	*31–16*	*Channels 96–81* *0 or 1Each bit is compared against the state of its corresponding channel.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 313Compare Pattern Registers, Continued			
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 97–112.*
Section ffset:	*Section 3 02Ch*	*Section 3 02Ch*	
	Section 3 it	*Section 3 it*	*Section 322Bit Description*
	15–0	*15–0*	*Channels 112–97* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 113–128.*
Section ffset:	*Section 3 02Eh*	*Section 3 02Ch*	
	Section 3 it	*Section 3 it*	*Section 331Bit Description*
	15–0	*31–16*	*Channels 128–113* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section 332Output Data Registers			
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description:* *Output Data Register, TTL Channels 1–16.*
Section ffset:	*Section 3 030h*	*Section 3 030h*	
	Section 3 it	*Section 3 it*	*Section 341Bit Description*
	15–0	*15–0*	*Channels 16–1* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description:* *Output Data Register, TTL Channels 17–32.*
Section ffset:	*Section 3 032h*	*Section 3 030h*	
	Section 3 it	*Section 3 it*	*Section 350Bit Description*
	15–0	*31–16*	*Channels 32–17* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description:* *Output Data Register, TTL Channels 33–48.*
Section ffset:	*Section 3 034h*	*Section 3 034h*	
	Section 3 it	*Section 3 it*	*Section 359Bit Description*
	15–0	*15–0*	*Channels 48–33* *0 or 1Each bit corresponds to a channel.*

Example 10.

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Output Data Register, TTL Channels 49–64.*
Section ffset:	*Section 036*	*Section 034h*	
	Section it	*Section it*	*Section 368Bit Description*
	15–0	*31–16*	*Channels 64–49* *0 or 1Each bit corresponds to a channel.*

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Output Data Register, TTL Channels 65–80.*
Section ffset:	*Section 038h*	*Section 038h*	
	Section it	*Section it*	*Section 377Bit Description*
	15–0	*15–0*	*Channels 80–65* *0 or 1Each bit corresponds to a channel.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

			Section 378Output Data Registers, Continued
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description: Output Data Register, TTL Channels 81–96.*
Section ffset:	*Section 3 03Ah*	*Section 3 038h*	
	Section 3 it	*Section 3 it*	*Section 387Bit Description*
	15–0	*31–16*	*Channels 96–81 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description: Output Data Register, TTL Channels 97–112.*
Section ffset:	*Section 3 03Ch*	*Section 3 03Ch*	
	Section 3 it	*Section 3 it*	*Section 396Bit Description*
	15–0	*15–0*	*Channels 112–97 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 3 6-bit***	***Section 3 2-bit***	*Register Description: Output Data Register, TTL Channels 113–128.*
Section ffset:	*Section 4 03Eh*	*Section 4 03Ch*	
	Section 4 it	*Section 4 it*	*Section 405Bit Description*
	15–0	*31–16*	*Channels 128–113 0 or 1Each bit corresponds to a channel.*
			Section 406Input Data Registers
Section ode:	***Section 4 6-bit***	***Section 4 2-bit***	*Register Description: Input Data Register, TTL Channels 1–16. Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 4 040h*	*Section 4 040h*	
	Section 4 it	*Section 4 it*	*Section 415Bit Description*
	15–0	*15–0*	*Channels 16–1 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 4 6-bit***	***Section 4 2-bit***	*Register Description: Input Data Register, TTL Channels 17–32. Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 4 042h*	*Section 4 040h*	
	Section 4 it	*Section 4 it*	*Section 424Bit Description*
	15–0	*31–16*	*Channels 32–17 0 or 1Each bit corresponds to a channel.*

Example 11.

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section ode:	***Section 4 6-bit***	***Section 4 2-bit***	*Register Description: Input Data Register, TTL Channels 33–48.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 4 044h*	*Section 4. 044h*	
	Section 4 it	*Section 4. it*	*Section 433Bit Description*
	15–0	*15–0*	*Channels 48–33* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 4 6-bit***	***Section 4 2-bit***	*Register Description: Input Data Register, TTL Channels 49–64.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 4 046h*	*Section 4. 044h*	
	Section 4 it	*Section 4 it*	*Section 442Bit Description*
	15–0	*31–16*	*Channels 64–49* *0 or 1Each bit corresponds to a channel.*

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

			Section 443Input Data Register, Continued
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description: Input Data Register, TTL Channels 65–80.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 048h*	*Section 048h*	
	Section it	*Section it*	*Section 452Bit Description*
	15–0	*15–0*	*Channels 80–65* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description: Input Data Register, TTL Channels 81–96.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 04Ah*	*Section 048h*	
	Section it	*Section it*	*Section 461Bit Description*
	15–0	*31–16*	*Channels 96–81* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description: Input Data Register, TTL Channels 97–112.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 04Ch*	*Section 04Ch*	
	Section it	*Section it*	*Section 470Bit Description*
	15–0	*15–0*	*Channels 112–97* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description: Input Data Register, TTL Channels 113–128.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 04Eh*	*Section 04Ch*	
	Section it	*Section it*	*Section 479Bit Description*
	15–0	*31–16*	*Channels 128–113* *0 or 1Each bit corresponds to a channel.*
			Section 480Gate Control Registers
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description: Write only. Turn on gate, TTL Channels 1–16.*
Section ffset:	*Section 050h*	*Section 050h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description: Write only. Turn off gate, TTL Channels 1–16.*
Section ffset:	*Section 054h*	*Section 054h*	

Example 12.

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Register Description:*	*Write only. Turn on gate, TTL Channels 17–32.*
Section ffset:	*Section 058h*	*Section 058h*		

Section ode:	**Section 6-bit**	**Section 2-bit**	*Register Description:*	*Write only. Turn off gate, TTL Channels 17–32.*
Section ffset:	*Section 05Ch*	*Section 05Ch*		

Section ode:	**Section 6-bit**	**Section 2-bit**	*Register Description:*	*Write only. Turn on gate, TTL Channels 33–48.*
Section ffset:	*Section 060h*	*Section 060h*		

Section ode:	**Section 6-bit**	**Section 2-bit**	*Register Description:*	*Write only. Turn off gate, TTL Channels 33–48.*
Section ffset:	*Section 064h*	*Section 064h*		

Section ode:	**Section 6-bit**	**Section 2-bit**	*Register Description:*	*Write only. Turn on gate, TTL Channels 49–64.*
Section ffset:	*Section 068h*	*Section 068h*		

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section 523Gate Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, TTL Channels 49–64.*
Section ffset:	*Section 06Ch*	*Section 06Ch*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, TTL Channels 65–80.*
Section ffset:	*Section 070h*	*Section 070h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, TTL Channels 65–80.*
Section ffset:	*Section 074h*	*Section 074h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, TTL Channels 81–96.*
Section ffset:	*Section 078h*	*Section 078h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, TTL Channels 81–96.*
Section ffset:	*Section 07Ch*	*Section 07Ch*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, TTL Channels 97–112.*
Section ffset:	*Section 080h*	*Section 080h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, TTL Channels 97–112.*
Section ffset:	*Section 084h*	*Section 084h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, TTL Channels 113–128.*
Section ffset:	*Section 088h*	*Section 088h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, TTL Channels 113–128.*
Section ffset:	*Section 08Ch*	*Section 08Ch*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, all channels on motherboard.*
Section ffset:	*Section 090h*	*Section 090h*		

Example 14.

Table 9-2. Motherboard, PN 85002350, A24/A32 Memory Map, *Continued*

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, all channels on motherboard.*
Section ffset:	*Section 094h*	*Section 094h*	

Section ffset:	*Section 5918096 –80FF*	*Section 592Not used.*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map

Section ffset:	*Section 59481 00h–81FFh*	*Section 595Used by the daughterboard PN 85002360, Differential TTL channels 1 – 32 Open collector channels 1 – 32 CMOS channels 1 - 32*
		Section 596Control Registers
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, Differential TTL Channels 1–16.*
Section ffset:	*Section 100h*	*Section 100h*	Section 603
	Section it	*Section it*	*Section 606Bit Description*
	15	*15*	Section 607*Not used, mask off.*
	14	*14*	Section 608*Not used, mask off.*
	13	*13*	Section 609*Not used, mask off.*
	12	*12*	Section 610*Not used, mask off.*
	11	*11*	*Latch Status* *0 = unlatches* *1 = latched.*
	10	*10*	*Output Data Polarity;* *0 = true (default)* *1 = complement of data written to 0x8130*
	9	*9*	*Latch Mode* *0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8140*
	8	*8*	*Gate Control Mode* *0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity* *0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode* *0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable* *0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode* *0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode* *0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity* *0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode* *0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction* *0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8150, 0x8154, 0x8190, and 0x8194.*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section 611Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, Differential TTL Channels 17–32.*
Section ffset:	*Section 102h*	*Section 100h*		
	Section it	*Section it*	*Section 620Bit Description*	
	15	*31*	Section 621*Not used, mask off.*	
	14	*30*	Section 622*Not used, mask off.*	
	13	*29*	Section 623*Not used, mask off.*	
	12	*28*	Section 624*Not used, mask off.*	
	11	*27*	Section 625*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x8132*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8142*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8158, 0x815C, 0x8190, and 0x8194.*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section 611Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, Open Collector Channels 1–16.*
Section ffset:	*Section 104h*	*Section 104h*		
	Section it	*Section it*	*Section 634Bit Description*	
	15	*15*	Section 635*Not used, mask off.*	
	14	*14*	Section 636*Not used, mask off.*	
	13	*13*	Section 637*Not used, mask off.*	
	12	*12*	Section 638*Not used, mask off.*	
	11	*11*	Section 639*Not used, mask off.*	
	10	*10*	*Output Data Polarity;*	*0 = true (default)* *1 = complement of data written to 0x8134*
	9	*9*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8144*
	8	*8*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8160, 0x8164, 0x8190, and 0x8194.*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section 611Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, Open Collector Channels 17–32.*
Section ffset:	*Section 106h*	*Section 104h*		
	Section it	*Section it*	*Section 648Bit Description*	
	15	*31*	Section 649*Not used, mask off.*	
	14	*30*	Section 650*Not used, mask off.*	
	13	*29*	Section 651*Not used, mask off.*	
	12	*28*	Section 652*Not used, mask off.*	
	11	*27*	Section 653*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x8136*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8146*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8168, 0x816C, 0x8190, and 0x8194.*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section 611Control Registers, Continued

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, CMOS Channels 1–16.*
Section ffset:	*Section 108h*	*Section 108h*	
	Section it	*Section it*	*Section 662Bit Description*
	15	*15*	Section 663*Not used, mask off.*
	14	*14*	Section 664*Not used, mask off.*
	13	*13*	Section 665*Not used, mask off.*
	12	*12*	Section 666*Not used, mask off.*
	11	*11*	Section 667*Not used, mask off.*
	10	*10*	*Output Data Polarity;* *0 = true (default)* *1 = complement of data written to 0x8138*
	9	*9*	*Latch Mode* *0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8148*
	8	*8*	*Gate Control Mode* *0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity* *0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode* *0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable* *0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode* *0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode* *0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity* *0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode* *0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction* *0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8170, 0x8174, 0x8190, and 0x8194.*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section 611Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, CMOS Channels 17–32.*
Section ffset:	*Section 10Ah*	*Section 108h*		
	Section it	*Section it*	*Section 676Bit Description*	
	15	*31*	Section 677*Not used, mask off.*	
	14	*30*	Section 678*Not used, mask off.*	
	13	*29*	Section 679*Not used, mask off.*	
	12	*28*	Section 680*Not used, mask off.*	
	11	*27*	Section 681*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x813A*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x814A*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8178, 0x817C, 0x8190, and 0x8194.*

Example 15.

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section ffset:	*Section 68381 0Ch–810Eh*	*Section 684Not used.*	*Section 685*
		Section 686Compare Mask Registers	
Section ode:	***Section 6 6-bit***	***Section 6 2-bit***	*Register Description: Compare Mask Register, Differential TTL Channels 1–16.*
Section ffset:	*Section 6 110h*	*Section 6 110h*	
	Section 6 it	*Section 6 it*	*Section 695Bit Description*
	15–0	*15–0*	*Channels 16–1* — *0 = channel does not participate in compare (default); 1 = channel participates in compare*
Section ode:	***Section 6 6-bit***	***Section 6 2-bit***	*Register Description: Compare Mask Register, Differential TTL Channels 17–32.*
Section ffset:	*Section 7 112h*	*Section 7 110h*	
	Section 7 it	*Section 7 it*	*Section 704Bit Description*
	15–0	*31–16*	*Channels 32–17* — *0 = channel does not participate in compare (default); 1 = channel participates in compare*
Section ode:	***Section 7 6-bit***	***Section 7 2-bit***	*Register Description: Compare Mask Register, Open Collector Channels 1–16.*
Section ffset:	*Section 7 114h*	*Section 7 114h*	
	Section 7 it	*Section 7 it*	*Section 713Bit Description*
	15–0	*15–0*	*Channels 16–1* — *0 = channel does not participate in compare (default); 1 = channel participates in compare*
Section ode:	***Section 7 6-bit***	***Section 7 2-bit***	*Register Description: Compare Mask Register, Open Collector Channels 17–32.*
Section ffset:	*Section 7 116h*	*Section 7 114h*	
	Section 7 it	*Section 7 it*	*Section 722Bit Description*
	15–0	*31–16*	*Channels 32–17* — *0 = channel does not participate in compare (default); 1 = channel participates in compare*
Section ode:	***Section 7 6-bit***	***Section 7 2-bit***	*Register Description: Compare Mask Register, CMOS Channels 1–16.*
Section ffset:	*Section 7 118h*	*Section 7 118h*	
	Section 7 it	*Section 7 it*	*Section 731Bit Description*
	15–0	*15–0*	*Channels 16–1* — *0 = channel does not participate in compare (default); 1 = channel participates in compare*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section ode:	**Section 6-bit**	**Section 2-bit**	Register Description: Compare Mask Register, CMOS Channels 17–32.
Section ffset:	Section 11Ah	Section 118h	
	Section it	Section it	Section 740Bit Description
	15–0	31–16	Channels 32–17 — 0 = channel does not participate in compare (default); 1 = channel participates in compare

Section ffset:	Section 74281 1Ch–811Eh	Section 743Not used.	Section 744

Section 745Compare Pattern Registers

Section ode:	**Section 6-bit**	**Section 2-bit**	Register Description: Compare Pattern Register, Differential TTL Channels 1–16.
Section ffset:	Section 120h	Section 120h	
	Section it	Section it	Section 754Bit Description
	15–0	15–0	Channels 16–1 — 0 or 1 Each bit is compared against the state of its corresponding channel.

Section ode:	**Section 6-bit**	**Section 2-bit**	Register Description: Compare Pattern Register, Differential TTL Channels 17–32.
Section ffset:	Section 122h	Section 120h	
	Section it	Section it	Section 763Bit Description
	15–0	31–16	Channels 32–17 — 0 or 1 Each bit is compared against the state of its corresponding channel.

Section ode:	**Section 6-bit**	**Section 2-bit**	Register Description: Compare Pattern Register, Open Collector Channels 1–16.
Section ffset:	Section 124h	Section 124h	
	Section it	Section it	Section 772Bit Description
	15–0	15–0	Channels 16–1 — 0 or 1 Each bit is compared against the state of its corresponding channel.

Section ode:	**Section 6-bit**	**Section 2-bit**	Register Description: Compare Pattern Register, Open Collector Channels 17–32.
Section ffset:	Section 126h	Section 124h	
	Section it	Section it	Section 781Bit Description
	15–0	31–16	Channels 32–17 — 0 or 1 Each bit is compared against the state of its corresponding channel.

Example 16.

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section ode:	***Section 7 6-bit***	***Section 7 2-bit***	*Register Description: Compare Pattern Register, CMOS Channels 1–16.*
Section ffset:	*Section 7 128h*	*Section 7 128h*	
	Section 7 it	*Section 7 it*	*Section 790Bit Description*
	15–0	*15–0*	*Channels 16–1 0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 7 6-bit***	***Section 7 2-bit***	*Register Description: Compare Pattern Register, CMOS Channels 17–32.*
Section ffset:	*Section 7 12Ah*	*Section 7 128h*	
	Section 7 it	*Section 7 it*	*Section 799Bit Description*
	15–0	*31–16*	*Channels 32–17 0 or 1Each bit is compared against the state of its corresponding channel.*

Example 17.

Section ffset:	*Section 80181 2Ch–812Eh*	*Section 802Not used. Section 803*

Section 804Output Data Registers

Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description: Output Data Register, Differential TTL Channels 1–16.*
Section ffset:	*Section 8 130h*	*Section 8 130h*	
	Section 8 it	*Section 8 it*	*Section 813Bit Description*
	15–0	*15–0*	*Channels 16–1 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description: Output Data Register, Differential TTL Channels 17–32.*
Section ffset:	*Section 8 132h*	*Section 8 130h*	
	Section 8 it	*Section 8 it*	*Section 822Bit Description*
	15–0	*31–16*	*Channels 32–17 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description: Output Data Register, Open Collector Channels 1–16.*
Section ffset:	*Section 8 134h*	*Section 8 134h*	
	Section 8 it	*Section 8 it*	*Section 831Bit Description*
	15–0	*15–0*	*Channels 16–1 0 or 1Each bit corresponds to a channel.*

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description:* *Output Data Register, Open Collector Channels 17–32.*
Section ffset:	*Section 8 136*	*Section 8 134h*	
	Section 8 it	*Section 8 it*	*Section 840Bit Description*
	15–0	*31–16*	*Channels 32–17* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description:* *Output Data Register, CMOS Channels 1–16.*
Section ffset:	*Section 8 138h*	*Section 8 138h*	
	Section 8 it	*Section 8 it*	*Section 849Bit Description*
	15–0	*15–0*	*Channels 16–1* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description:* *Output Data Register, CMOS Channels 17–32.*
Section ffset:	*Section 8 13Ah*	*Section 8 138h*	
	Section 8 it	*Section 8 it*	*Section 858Bit Description*
	15–0	*31–16*	*Channels 32–17* *0 or 1Each bit corresponds to a channel.*
Section ffset:	*Section 860813Ch –813Eh*		*Section 861Not used.*
			Section 862Input Data Registers
Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description:* *Input Data Register, Differential TTL Channels 1–16.* *Note:* *This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 8 140h*	*Section 8 140h*	
	Section 8 it	*Section 8 it*	*Section 871Bit Description*
	15–0	*15–0*	*Channels 16–1* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description:* *Input Data Register, Differential TTL Channels 17–32.* *Note:* *This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 8 142h*	*Section 8 140h*	
	Section 8 it	*Section 8 it*	*Section 880Bit Description*
	15–0	*31–16*	*Channels 32–17* *0 or 1Each bit corresponds to a channel.*

Example 18.

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description: Input Data Register, Open Collector Channels 1–16.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 8 144h*	*Section 8 144h*	
	Section 8 it	*Section 8 it*	*Section 889Bit Description*
	15–0	*15–0*	*Channels 16–1 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 8 6-bit***	***Section 8 2-bit***	*Register Description: Input Data Register, Open Collector Channels 17–32.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 8 146h*	*Section 8 144h*	
	Section 8 it	*Section 8 it*	*Section 898Bit Description*
	15–0	*31–16*	*Channels 32–17 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 9 6-bit***	***Section 9 2-bit***	*Register Description: Input Data Register, CMOS Channels 1–16.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 9 148h*	*Section 9 148h*	
	Section 9 it	*Section 9 it*	*Section 907Bit Description*
	15–0	*15–0*	*Channels 16–1 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 9 6-bit***	***Section 9 2-bit***	*Register Description: Input Data Register, CMOS Channels 17–32.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 9 14Ah*	*Section 9 148h*	
	Section 9 it	*Section 9 it*	*Section 916Bit Description*
	15–0	*31–16*	*Channels 32–17 0 or 1Each bit corresponds to a channel.*

Example 19.

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section ffset:	*Section 918814Ch –814Eh*	*Section 919Not used.*
	Section 920Gate Control Registers	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, Differential TTL Channels 1–16.*
Section ffset:	*Section 150h*	*Section 150h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, Differential TTL Channels 1–16.*
Section ffset:	*Section 154h*	*Section 154h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, Differential TTL Channels 17–32.*
Section ffset:	*Section 158h*	*Section 158h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, Differential TTL Channels 17–32.*
Section ffset:	*Section 15Ch*	*Section 15Ch*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, Open Collector Channels 1–16.*
Section ffset:	*Section 160h*	*Section 160h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, Open Collector Channels 1–16.*
Section ffset:	*Section 164h*	*Section 164h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, Open Collector Channels 17–32.*
Section ffset:	*Section 168h*	*Section 168h*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn off gate, Open Collector Channels 17–32.*
Section ffset:	*Section 16Ch*	*Section 16Ch*		
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Write only. Turn on gate, CMOS Channels 1–16.*
Section ffset:	*Section 170h*	*Section 170h*		

Table 9-3. Daughterboard, PN 85002360 Option 2, A24/A32 Memory Map, *Continued*

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, CMOS Channels 1–16.*
Section ffset:	*Section 174h*	*Section 174h*	

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, CMOS Channels 17–32.*
Section ffset:	*Section 178h*	*Section 178h*	

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, CMOS Channels 17–32.*
Section ffset:	*Section 17Ch*	*Section 17Ch*	

Section ffset:	*Section 9948180 h–818Fh*	*Section 995Not used.*

Example 21.

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, all channels on daughterboard.*
Section ffset:	*Section 190h*	*Section 190h*	

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, all channels on daughterboard.*
Section ffset:	*Section 194h*	*Section 194h*	

Section ffset:	*Section 1009819 6–FFFF*	*Section 1010Not used.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map

Section ffset:	*Section 10128 100h–81FFh*	*Section 1013Used by the daughterboard PN 85002370, TTL channels 129 - 256*
		Section 1014Control Registers
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, TTL Channels 129–144.*
Section ffset:	*Section 100h*	*Section 100h*	Section 1021
	Section it	*Section it*	*Section 1024Bit Description*
	15	*15*	Section 1025*Not used, mask off.*
	14	*14*	Section 1026*Not used, mask off.*
	13	*13*	Section 1027*Not used, mask off.*
	12	*12*	Section 1028*Not used, mask off.*
	11	*11*	Section 1029*Not used, mask off.*
	10	*10*	*Output Data Polarity;* *0 = true (default)* *1 = complement of data written to 0x8130*
	9	*9*	*Latch Mode* *0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8140*
	8	*8*	*Gate Control Mode* *0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity* *0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode* *0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable* *0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode* *0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode* *0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity* *0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode* *0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction* *0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8150, 0x8154, 0x8190, and 0x8194.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1030Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 145–160.*
Section ffset:	*Section 102h*	*Section 100h*		
	Section it	*Section it*	*Section 1039Bit Description*	
	15	*31*	Section 1040*Not used, mask off.*	
	14	*30*	Section 1041*Not used, mask off.*	
	13	*29*	Section 1042*Not used, mask off.*	
	12	*28*	Section 1043*Not used, mask off.*	
	11	*27*	Section 1044*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x8132*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8142*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8158, 0x815C, 0x8190, and 0x8194.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1030Control Registers, Continued			
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, TTL Channels 161–176.*
Section ffset:	*Section 104h*	*Section 104h*	
	Section it	*Section it*	*Section 1053Bit Description*
	15	*15*	Section 1054*Not used, mask off.*
	14	*14*	Section 1055*Not used, mask off.*
	13	*13*	Section 1056*Not used, mask off.*
	12	*12*	Section 1057*Not used, mask off.*
	11	*11*	Section 1058*Not used, mask off.*
	10	*10*	*Output Data Polarity;* *0 = true (default)* *1 = complement of data written to 0x8134*
	9	*9*	*Latch Mode* *0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8144*
	8	*8*	*Gate Control Mode* *0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity* *0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode* *0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable* *0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode* *0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode* *0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity* *0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode* *0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction* *0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8160, 0x8164, 0x8190, and 0x8194.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1030Control Registers, Continued			
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Control Register, TTL Channels 177–192.*
Section ffset:	*Section 106h*	*Section 104h*	
	Section it	*Section it*	*Section 1067Bit Description*
	15	*31*	Section 1068*Not used, mask off.*
	14	*30*	Section 1069*Not used, mask off.*
	13	*29*	Section 1070*Not used, mask off.*
	12	*28*	Section 1071*Not used, mask off.*
	11	*27*	Section 1072*Not used, mask off.*
	10	*26*	*Output Data Polarity* — *0 = true (default)*; *1 = complement of data written to 0x8136*
	9	*25*	*Latch Mode* — *0 = data is not latched (default)*; *1 = data present at channel inputs is latched by gate until read at 0x8146*
	8	*24*	*Gate Control Mode* — *0 = software only control of this group (default)*; *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity* — *0 = sensitive to the leading edge of this group's gate (default)*; *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode* — *0 = interrupt on gate (default)*; *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable* — *0 = disable interrupt (default)*; *1 = enable interrupt*
	4	*20*	*'Return To' Mode* — *0 = quiescent low (default)*; *1 = quiescent high*
	3	*19*	*'Return To' Mode* — *0 = return to one/zero disabled (default)*; *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity* — *0 = recognizes low true external control (default)*; *1 = recognizes high true external control*
	1	*17*	*External Control Mode* — *0 = external signal treated as gate (default)*; *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.* — *0 = input only (default)*; *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8168, 0x816C, 0x8190, and 0x8194.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1030Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 193–208.*
Section ffset:	*Section 108h*	*Section 108h*		
	Section it	*Section it*	*Section 1081Bit Description*	
	15	*15*	Section 1082*Not used, mask off.*	
	14	*14*	Section 1083*Not used, mask off.*	
	13	*13*	Section 1084*Not used, mask off.*	
	12	*12*	Section 1085*Not used, mask off.*	
	11	*11*	Section 1086*Not used, mask off.*	
	10	*10*	*Output Data Polarity;*	*0 = true (default)* *1 = complement of data written to 0x8138*
	9	*9*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x8148*
	8	*8*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group*
	7	*7*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8170, 0x8174, 0x8190, and 0x8194.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1030Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 209–224.*
Section ffset:	*Section 10Ah*	*Section 108h*		
	Section it	*Section it*	*Section 1095Bit Description*	
	15	*31*	Section 1096*Not used, mask off.*	
	14	*30*	Section 1097*Not used, mask off.*	
	13	*29*	Section 1098*Not used, mask off.*	
	12	*28*	Section 1099*Not used, mask off.*	
	11	*27*	Section 1100*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x813A*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x814A*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8178, 0x817C, 0x8190, and 0x8194.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1030Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 225–240.*
Section ffset:	*Section 10Ch*	*Section 10Ch*		
	Section it	*Section it*	*Section 1109Bit Description*	
	15	*15*	Section 1110*Not used, mask off.*	
	14	*14*	Section 1111*Not used, mask off.*	
	13	*13*	Section 1112*Not used, mask off.*	
	12	*12*	Section 1113*Not used, mask off.*	
	11	*11*	Section 1114*Not used, mask off.*	
	10	*10*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x813C*
	9	*9*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x814C*
	8	*8*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*7*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*6*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*5*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*4*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*3*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*2*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*1*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*0*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8180, 0x8184, 0x8190, and 0x8194.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1030Control Registers, Continued				
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:*	*Control Register, TTL Channels 241–256.*
Section ffset:	*Section 10Eh*	*Section 10Ch*		
	Section it	*Section it*	*Section 1123Bit Description*	
	15	*31*	Section 1124*Not used, mask off.*	
	14	*30*	Section 1125*Not used, mask off.*	
	13	*29*	Section 1126*Not used, mask off.*	
	12	*28*	Section 1127*Not used, mask off.*	
	11	*27*	Section 1128*Not used, mask off.*	
	10	*26*	*Output Data Polarity*	*0 = true (default)* *1 = complement of data written to 0x813E*
	9	*25*	*Latch Mode*	*0 = data is not latched (default)* *1 = data present at channel inputs is latched by gate until read at 0x814E*
	8	*24*	*Gate Control Mode*	*0 = software only control of this group (default)* *1 = allow external control by way of the dedicated control line for this group.*
	7	*23*	*Gate Sensitivity*	*0 = sensitive to the leading edge of this group's gate (default)* *1 = sensitive to the trailing edge of this group's gate*
	6	*22*	*Interrupt Mode*	*0 = interrupt on gate (default)* *1 = interrupt on data match and gate*
	5	*21*	*Interrupt Enable*	*0 = disable interrupt (default)* *1 = enable interrupt*
	4	*20*	*'Return To' Mode*	*0 = quiescent low (default)* *1 = quiescent high*
	3	*19*	*'Return To' Mode*	*0 = return to one/zero disabled (default)* *1 = return to one/zero enabled*
	2	*18*	*External Control Polarity*	*0 = recognizes low true external control (default)* *1 = recognizes high true external control*
	1	*17*	*External Control Mode*	*0 = external signal treated as gate (default)* *1 = external signal treated as pulse; first pulse turns gate on and second pulse turns gate off*
	0	*16*	*Data Direction.*	*0 = input only (default)* *1 = permit group to drive data out. This is not the 3-state control. See external control description, bit 8 in this register, 0x8188, 0x818C, 0x8190, and 0x8194.*

Example 22.

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1129Compare Mask Registers

Section ode:	**Section 16-bit**	**Section 12-bit**	Register Description:	Compare Mask Register, TTL Channels 129–144.
Section ffset:	Section 110h	Section 110h		
	Section it	Section it	Section 1138Bit Description	
	15–0	15–0	Channels 144–129	0 = channel does not participate in compare (default) 1 = channel participates in compare

Section ode:	**Section 16-bit**	**Section 12-bit**	Register Description:	Compare Mask Register, TTL Channels 145–160.
Section ffset:	Section 112h	Section 110h		
	Section it	Section it	Section 1147Bit Description	
	15–0	31–16	Channels 160–145	0 = channel does not participate in compare (default) 1 = channel participates in compare

Section ode:	**Section 16-bit**	**Section 12-bit**	Register Description:	Compare Mask Register, TTL Channels 161–176.
Section ffset:	Section 114h	Section 114h		
	Section it	Section it	Section 1156Bit Description	
	15–0	15–0	Channels 176–161	0 = channel does not participate in compare (default) 1 = channel participates in compare

Section ode:	**Section 16-bit**	**Section 12-bit**	Register Description:	Compare Mask Register, TTL Channels 177–192.
Section ffset:	Section 116h	Section 114h		
	Section it	Section it	Section 1165Bit Description	
	15–0	31–16	Channels 192–177	0 = channel does not participate in compare (default) 1 = channel participates in compare

Section ode:	**Section 16-bit**	**Section 12-bit**	Register Description:	Compare Mask Register, TTL Channels 193–208.
Section ffset:	Section 118h	Section 118h		
	Section it	Section it	Section 1174Bit Description	
	15–0	15–0	Channels 208–193	0 = channel does not participate in compare (default) 1 = channel participates in compare

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section ode:	**Section 16-bit**	**Section 12-bit**	*Register Description:* *Compare Mask Register, TTL Channels 209–224.*
Section ffset:	*Section 11Ah*	*Section 1118h*	
	Section 1it	*Section 1it*	*Section 1183Bit Description*
	15–0	*31–16*	*Channels 224–209* — *0 = channel does not participate in compare (default)*; *1 = channel participates in compare*

Section ode:	**Section 16-bit**	**Section 12-bit**	*Register Description:* *Compare Mask Register, TTL Channels 225–240.*
Section ffset:	*Section 11Ch*	*Section 111Ch*	
	Section 1it	*Section 1it*	*Section 1192Bit Description*
	15–0	*15–0*	*Channels 240–225* — *0 = channel does not participate in compare (default)*; *1 = channel participates in compare*

Section 1193Compare Mask Registers, Continued

Section ode:	**Section 16-bit**	**Section 12-bit**	*Register Description:* *Compare Mask Register, TTL Channels 241–256.*
Section ffset:	*Section 11Eh*	*Section 111Ch*	
	Section 1it	*Section 1it*	*Section 1202Bit Description*
	15–0	*31–16*	*Channels 256–241* — *0 = channel does not participate in compare (default)*; *1 = channel participates in compare*

Example 23.

Section 1203Compare Pattern Registers

Section ode:	**Section 16-bit**	**Section 12-bit**	*Register Description:* *Compare Pattern Register, TTL Channels 129–144.*
Section ffset:	*Section 1120h*	*Section 1120h*	
	Section 1it	*Section 1it*	*Section 1212Bit Description*
	15–0	*15–0*	*Channels 144–129* — *0 or 1 Each bit is compared against the state of its corresponding channel.*

Section ode:	**Section 16-bit**	**Section 12-bit**	*Register Description:* *Compare Pattern Register, TTL Channels 145–160.*
Section ffset:	*Section 1122h*	*Section 1120h*	
	Section 1it	*Section 1it*	*Section 1221Bit Description*
	15–0	*31–16*	*Channels 160–145* — *0 or 1 Each bit is compared against the state of its corresponding channel.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 161–176.*
Section ffset:	*Section 124h*	*Section 124h*	
	Section it	*Section it*	*Section 1230Bit Description*
	15–0	*15–0*	*Channels 176–161* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 177–192.*
Section ffset:	*Section 126h*	*Section 124h*	
	Section it	*Section it*	*Section 1239Bit Description*
	15–0	*31–16*	*Channels 192–177* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 193–208.*
Section ffset:	*Section 128h*	*Section 128h*	
	Section it	*Section it*	*Section 1248Bit Description*
	15–0	*15–0*	*Channels 208–193* *0 or 1Each bit is compared against the state of its corresponding channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 209–224.*
Section ffset:	*Section 12Ah*	*Section 128h*	
	Section it	*Section it*	*Section 1257Bit Description*
	15–0	*31–16*	*Channels 224–209* *0 or 1Each bit is compared against the state of its corresponding channel.*

Section 1258Compare Pattern Registers, Continued

Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 225–240.*
Section ffset:	*Section 12Ch*	*Section 12Ch*	
	Section it	*Section it*	*Section 1267Bit Description*
	15–0	*15–0*	*Channels 240–225* *0 or 1Each bit is compared against the state of its corresponding channel.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Compare Pattern Register, TTL Channels 241–256.*
Section ffset:	*Section 12Eh*	*Section 12Ch*	
	Section it	*Section it*	*Section 1276Bit Description*
	15–0	*31–16*	*Channels 256–241* *0 or 1Each bit is compared against the state of its corresponding channel.*
			Section 1277Output Data Registers
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 129–144.*
Section ffset:	*Section 130h*	*Section 130h*	
	Section it	*Section it*	*Section 1286Bit Description*
	15–0	*15–0*	*Channels 144–129* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 145–160.*
Section ffset:	*Section 132h*	*Section 130h*	
	Section it	*Section it*	*Section 1295Bit Description*
	15–0	*31–16*	*Channels 160–145* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 161–176.*
Section ffset:	*Section 134h*	*Section 134h*	
	Section it	*Section it*	*Section 1304Bit Description*
	15–0	*15–0*	*Channels 176–161* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 177–192.*
Section ffset:	*Section 136*	*Section 134h*	
	Section it	*Section it*	*Section 1313Bit Description*
	15–0	*31–16*	*Channels 192–177* *0 or 1Each bit corresponds to a channel.*

Example 24.

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 193–208.*
Section ffset:	*Section 138h*	*Section 138h*	
	Section it	*Section it*	*Section 1322Bit Description*
	15–0	*15–0*	*Channels 208–193* *0 or 1Each bit corresponds to a channel.*

Section 1323Output Data Registers, Continued

Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 209–224.*
Section ffset:	*Section 13Ah*	*Section 138h*	
	Section it	*Section it*	*Section 1332Bit Description*
	15–0	*31–16*	*Channels 224–209* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 225–240.*
Section ffset:	*Section 13Ch*	*Section 13Ch*	
	Section it	*Section it*	*Section 1341Bit Description*
	15–0	*15–0*	*Channels 240–225* *0 or 1Each bit corresponds to a channel.*

Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description:* *Output Data Register, TTL Channels 241–256.*
Section ffset:	*Section 13Eh*	*Section 13Ch*	
	Section it	*Section it*	*Section 1350Bit Description*
	15–0	*31–16*	*Channels 256–241* *0 or 1Each bit corresponds to a channel.*

Example 25.

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

			Section 1351Input Data Registers
Section ode:	***Section 1 6-bit***	***Section 1 2-bit***	*Register Description: Input Data Register, TTL Channels 129–144.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 1 140h*	*Section 1. 140h*	
	Section 1 it	*Section 1. it*	*Section 1360Bit Description*
	15–0	*15–0*	*Channels 144–129 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 1 6-bit***	***Section 1 2-bit***	*Register Description: Input Data Register, TTL Channels 145–160.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 1 142h*	*Section 1. 140h*	
	Section 1 it	*Section 1. it*	*Section 1369Bit Description*
	15–0	*31–16*	*Channels 160–145 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 1 6-bit***	***Section 1 2-bit***	*Register Description: Input Data Register, TTL Channels 161–176.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 1 144h*	*Section 1. 144h*	
	Section 1 it	*Section 1. it*	*Section 1378Bit Description*
	15–0	*15–0*	*Channels 176–161 0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 1 6-bit***	***Section 1 2-bit***	*Register Description: Input Data Register, TTL Channels 177–192.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 1 146h*	*Section 1. 144h*	
	Section 1 it	*Section 1. it*	*Section 1387Bit Description*
	15–0	*31–16*	*Channels 192–177 0 or 1Each bit corresponds to a channel.*

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

			Section 1388Input Data Register, Continued
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description: Input Data Register, TTL Channels 193–208.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 148h*	*Section 148h*	
	Section it	*Section it*	*Section 1397Bit Description*
	15–0	*15–0*	*Channels 208–193* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description: Input Data Register, TTL Channels 209–224.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 14Ah*	*Section 148h*	
	Section it	*Section it*	*Section 1406Bit Description*
	15–0	*31–16*	*Channels 224–209* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description: Input Data Register, TTL Channels 225–240.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 14Ch*	*Section 14Ch*	
	Section it	*Section it*	*Section 1415Bit Description*
	15–0	*15–0*	*Channels 240–225* *0 or 1Each bit corresponds to a channel.*
Section ode:	***Section 16-bit***	***Section 12-bit***	*Register Description: Input Data Register, TTL Channels 241–256.* *Note: This is a real time read of the external data lines if the data is not latched.*
Section ffset:	*Section 14Eh*	*Section 14Ch*	
	Section it	*Section it*	*Section 1424Bit Description*
	15–0	*31–16*	*Channels 256–241* *0 or 1Each bit corresponds to a channel.*

Example 26.

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section 1425Gate Control Registers			
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 129–144.*
Section ffset:	*Section 150h*	*Section 150h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 129–144.*
Section ffset:	*Section 154h*	*Section 154h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 145–160.*
Section ffset:	*Section 158h*	*Section 158h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 145–160.*
Section ffset:	*Section 15Ch*	*Section 15Ch*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 161–176.*
Section ffset:	*Section 160h*	*Section 160h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 161–176.*
Section ffset:	*Section 164h*	*Section 164h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 177–192.*
Section ffset:	*Section 168h*	*Section 168h*	
Section 1468Gate Control Registers, Continued			
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 177–192.*
Section ffset:	*Section 16Ch*	*Section 16Ch*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 193–208.*
Section ffset:	*Section 170h*	*Section 170h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 193–208.*
Section ffset:	*Section 174h*	*Section 174h*	

Table 9-4. Daughterboard, PN 85002370 Option 1, A24/A32 Memory Map, *Continued*

Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 209–224.*
Section ffset:	*Section 178h*	*Section 178h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 209–224.*
Section ffset:	*Section 17Ch*	*Section 17Ch*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 225–240.*
Section ffset:	*Section 180h*	*Section 180h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 225–240.*
Section ffset:	*Section 184h*	*Section 184h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, TTL Channels 241–256.*
Section ffset:	*Section 188h*	*Section 188h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn off gate, TTL Channels 241–256.*
Section ffset:	*Section 18Ch*	*Section 18Ch*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, all channels on daughterboard.*
Section ffset:	*Section 190h*	*Section 190h*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Register Description:* *Write only. Turn on gate, all channels on daughterboard.*
Section ffset:	*Section 194h*	*Section 194h*	
Section ffset:	*Section 1536819 6–FFFF*		*Section 1537Not used.*

Example 28.

Table 9-5. Daughterboard, Option 4, A24/A32 Memory Map

Section ffset:	*Section 15398 100h–81FFh*		*Section 1540Used by the daughterboard Option 4, 128 Relay Driver Channels and Driver Static TTL I/0 1–16*	
Section ode:	***Section 6-bit***	***Section 2-bit***	*Note: Analog ground (shield) is on J3-83, 63, 43, 23, and 3. V reference (+12V) connection available at J3-81, 61, 41, 21, and 1.*	
Section ffset:	*Section 100h*	*Section 100h*		
	Section it	*Section it*	*Section 1549Connection*	Section 1550*Function*
	15	*15*	*J3-65*	*Drive 16*
	14	*14*	*J3-67*	*Drive 15*
	13	*13*	*J3-69*	*Drive 14*
	12	*12*	*J3-71*	*Drive 13*
	11	*11*	*J3-73*	*Drive 12*
	10	*10*	*J3-75*	*Drive 11*
	9	*9*	*J3-77*	*Drive 10*
	8	*8*	*J3-79*	*Drive 9*
	7	*7*	*J3-85*	*Drive 8*
	6	*6*	*J3-87*	*Drive 7*
	5	*5*	*J3-89*	*Drive 6*
	4	*4*	*J3-91*	*Drive 5*
	3	*3*	*J3-93*	*Drive 4*
	2	*2*	*J3-95*	*Drive 3*
	1	*1*	*J3-97*	*Drive 2*
	0	*0*	*J3-99*	*Drive 1*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Analog ground (shield) is on J3-83, 63, 43, 23, and 3. V reference (+12V) connection available at J3-81, 61, 41, 21, and 1.*	
Section ffset:	*Section 102h*	*Section 100h*		
	Section it	*Section it*	*Section 1559Connection*	Section 1560*Function*
	15	*31*	*J3-25*	*Drive 32*
	14	*30*	*J3-27*	*Drive 31*
	13	*29*	*J3-29*	*Drive 30*
	12	*28*	*J3-31*	*Drive 29*
	11	*27*	*J3-33*	*Drive 28*
	10	*26*	*J3-35*	*Drive 27*
	9	*25*	*J3-37*	*Drive 26*
	8	*24*	*J3-39*	*Drive 25*
	7	*23*	*J3-45*	*Drive 24*
	6	*22*	*J3-47*	*Drive 23*
	5	*21*	*J3-49*	*Drive 22*
	4	*20*	*J3-51*	*Drive 21*
	3	*19*	*J3-53*	*Drive 20*
	2	*18*	*J3-55*	*Drive 19*
	1	*17*	*J3-57*	*Drive 18*
	0	*16*	*J3-59*	*Drive 17*

Table 9-5. Daughterboard, Option 4, A24/A32 Memory Map, *Continued*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Analog ground (shield) is on J3-84, 64, 44, 24, and 4. V reference (+12V) connection available at J3-82, 62, 42, 22, and 2.*	
Section ffset:	*Section 104h*	*Section 104h*		
	Section it	*Section it*	*Section 1569Connection*	Section 1570*Function*
	15	*15*	*J3-86*	*Drive 48*
	14	*14*	*J3-88*	*Drive 47*
	13	*13*	*J3-90*	*Drive 46*
	12	*12*	*J3-92*	*Drive 45*
	11	*11*	*J3-94*	*Drive 44*
	10	*10*	*J3-96*	*Drive 43*
	9	*9*	*J3-98*	*Drive 42*
	8	*8*	*J3-100*	*Drive 41*
	7	*7*	*J3-5*	*Drive 40*
	6	*6*	*J3-7*	*Drive 39*
	5	*5*	*J3-9*	*Drive 38*
	4	*4*	*J3-11*	*Drive 37*
	3	*3*	*J3-13*	*Drive 36*
	2	*2*	*J3-15*	*Drive 35*
	1	*1*	*J3-17*	*Drive 34*
	0	*0*	*J3-19*	*Drive 33*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Analog ground (shield) is on J3-84, 64, 44, 24, and 4. V reference (+12V) connection available at J3-82, 62, 42, 22, and 2.*	
Section ffset:	*Section 106h*	*Section 104h*		
	Section it	*Section it*	*Section 1579Connection*	Section 1580*Function*
	15	*31*	*J3-46*	*Drive 64*
	14	*30*	*J3-48*	*Drive 63*
	13	*29*	*J3-50*	*Drive 62*
	12	*28*	*J3-52*	*Drive 61*
	11	*27*	*J3-54*	*Drive 60*
	10	*26*	*J3-56*	*Drive 59*
	9	*25*	*J3-58*	*Drive 58*
	8	*24*	*J3-60*	*Drive 57*
	7	*23*	*J3-66*	*Drive 56*
	6	*22*	*J3-68*	*Drive 55*
	5	*21*	*J3-70*	*Drive 54*
	4	*20*	*J3-72*	*Drive 53*
	3	*19*	*J3-74*	*Drive 52*
	2	*18*	*J3-76*	*Drive 51*
	1	*17*	*J3-78*	*Drive 50*
	0	*16*	*J3-80*	*Drive 49*

Table 9-5. Daughterboard, Option 4, A24/A32 Memory Map, *Continued*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Analog ground (shield) is on J4-83, 63, 43, 23, and 3. V reference (+12V) connection available at J4-81, 61, 41, 21, and 1.*	
Section ffset:	*Section 108h*	*Section 108h*		
	Section it	*Section it*	*Section 1589Connection*	Section 1590*Function*
	15	*15*	*J3-6*	*Drive 80*
	14	*14*	*J3-8*	*Drive 79*
	13	*13*	*J3-10*	*Drive 78*
	12	*12*	*J3-12*	*Drive 77*
	11	*11*	*J3-14*	*Drive 76*
	10	*10*	*J3-16*	*Drive 75*
	9	*9*	*J3-18*	*Drive 74*
	8	*8*	*J3-20*	*Drive 73*
	7	*7*	*J3-26*	*Drive 72*
	6	*6*	*J3-28*	*Drive 71*
	5	*5*	*J3-30*	*Drive 70*
	4	*4*	*J3-32*	*Drive 69*
	3	*3*	*J3-34*	*Drive 68*
	2	*2*	*J3-36*	*Drive 67*
	1	*1*	*J3-38*	*Drive 66*
	0	*0*	*J3-40*	*Drive 65*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Analog ground (shield) is on J4-83, 63, 43, 23, and 3. V reference (+12V) connection available at J4-81, 61, 41, 21, and 1.*	
Section ffset:	*Section 10Ah*	*Section 108h*		
	Section it	*Section it*	*Section 1599Connection*	Section 1600*Function*
	15	*31*	*J4-65*	*Drive 96*
	14	*30*	*J4-67*	*Drive 95*
	13	*29*	*J4-69*	*Drive 94*
	12	*28*	*J4-71*	*Drive 93*
	11	*27*	*J4-73*	*Drive 92*
	10	*26*	*J4-15*	*Drive 91*
	9	*25*	*J4-77*	*Drive 90*
	8	*24*	*J4-79*	*Drive 89*
	7	*23*	*J4-85*	*Drive 88*
	6	*22*	*J4-87*	*Drive 87*
	5	*21*	*J4-89*	*Drive 86*
	4	*20*	*J4-91*	*Drive 85*
	3	*19*	*J4-93*	*Drive 84*
	2	*18*	*J4-95*	*Drive 83*
	1	*17*	*J4-97*	*Drive 82*
	0	*16*	*J4-99*	*Drive 81*

Table 9-5. Daughterboard, Option 4, A24/A32 Memory Map, *Continued*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Analog ground (shield) is on J4-84, 64, 44, 24, and 4. V reference (+12V) connection available at J4-82, 62, 42, 22, and 2.*	
Section ffset:	*Section 10Ch*	*Section 10Ch*		
	Section it	*Section it*	*Section 1609Connection*	Section 1610*Function*
	15	*15*	*J4-25*	*Drive 112*
	14	*14*	*J4-27*	*Drive 111*
	13	*13*	*J4-29*	*Drive 110*
	12	*12*	*J4-31*	*Drive 109*
	11	*11*	*J4-33*	*Drive 108*
	10	*10*	*J4-35*	*Drive 107*
	9	*9*	*J4-37*	*Drive 106*
	8	*8*	*J4-39*	*Drive 105*
	7	*7*	*J4-45*	*Drive 104*
	6	*6*	*J4-47*	*Drive 103*
	5	*5*	*J4-49*	*Drive 102*
	4	*4*	*J4-51*	*Drive 101*
	3	*3*	*J4-53*	*Drive 100*
	2	*2*	*J4-55*	*Drive 99*
	1	*1*	*J4-57*	*Drive 98*
	0	*0*	*J4-59*	*Drive 97*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Analog ground (shield) is on J4-84, 64, 44, 24, and 4. V reference (+12V) connection available at J4-82, 62, 42, 22, and 2.*	
Section ffset:	*Section 10Eh*	*Section 10Ch*		
	Section it	*Section it*	*Section 1619Connection*	Section 1620*Function*
	15	*31*	*J4-86*	*Drive 128*
	14	*30*	*J4-88*	*Drive 127*
	13	*29*	*J4-90*	*Drive 126*
	12	*28*	*J4-92*	*Drive 125*
	11	*27*	*J4-94*	*Drive 124*
	10	*26*	*J4-96*	*Drive 123*
	9	*25*	*J4-98*	*Drive 122*
	8	*24*	*J4-100*	*Drive 121*
	7	*23*	*J4-5*	*Drive 120*
	6	*22*	*J4-77*	*Drive 119*
	5	*21*	*J4-99*	*Drive 118*
	4	*20*	*J4-111*	*Drive 117*
	3	*19*	*J4-13*	*Drive 116*
	2	*18*	*J4-15*	*Drive 115*
	1	*17*	*J4-17*	*Drive 114*
	0	*16*	*J4-19*	*Drive 113*

Table 9-5. Daughterboard, Option 4, A24/A32 Memory Map, *Continued*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Chassis ground is on J4-4, and 2. V reference (+12V) connection available at J4-16, 14, and 12.*	
Section ffset:	*Section 110h*	*Section 110h*		
	Section it	*Section it*	*Section 1629Connection (Signal, Digital Ground)*	Section 1630*Function*
	15	*15*	*J4-20, 18*	*TTL I/O 16 enable*
	14	*14*	*J4-24, 22*	*TTL I/O 15 enable*
	13	*13*	*J4-28, 26*	*TTL I/O 14 enable*
	12	*12*	*J4-32, 30*	*TTL I/O 13 enable*
	11	*11*	*J4-36, 34*	*TTL I/O 12 enable*
	10	*10*	*J4-40, 38*	*TTL I/O 11 enable*
	9	*9*	*J4-44, 42*	*TTL I/O 10 enable*
	8	*8*	*J4-48, 46*	*TTL I/O 9 enable*
	7	*7*	*J4-52, 50*	*TTL I/O 8 enable*
	6	*6*	*J4-56, 54*	*TTL I/O 7 enable*
	5	*5*	*J4-60, 58*	*TTL I/O 6 enable*
	4	*4*	*J4-64, 62*	*TTL I/O 5 enable*
	3	*3*	*J4-68, 66*	*TTL I/O 4 enable*
	2	*2*	*J4-72, 70*	*TTL I/O 3 enable*
	1	*1*	*J4-76, 74*	*TTL I/O 2 enable*
	0	*0*	*J4-80, 78*	*TTL I/O 1 enable*

Table 9-5. Daughterboard, Option 4, A24/A32 Memory Map, *Continued*

Section ode:	**Section 6-bit**	**Section 2-bit**	*Note: Chassis ground is on J4-4, and 2. V reference (+12V) connection available at J4-16, 14, and 12.*	
Section ffset:	*Section 112h*	*Section 110h*		
	Section it	*Section it*	*Section 1639Connection*	Section 1640*Function*
	15	*31*	*J4-20, 18*	*TTL I/O 16 data*
	14	*30*	*J4-24, 22*	*TTL I/O 15 data*
	13	*29*	*J4-28, 26*	*TTL I/O 14 data*
	12	*28*	*J4-32, 30*	*TTL I/O 13 data*
	11	*27*	*J4-36, 34*	*TTL I/O 12 data*
	10	*26*	*J4-40, 38*	*TTL I/O 11 data*
	9	*25*	*J4-44, 42*	*TTL I/O 10 data*
	8	*24*	*J4-48, 46*	*TTL I/O 9 data*
	7	*23*	*J4-52, 50*	*TTL I/O 8 data*
	6	*22*	*J4-56, 54*	*TTL I/O 7 data*
	5	*21*	*J4-60, 58*	*TTL I/O 6 data*
	4	*20*	*J4-64, 62*	*TTL I/O 5 data*
	3	*19*	*J4-68, 66*	*TTL I/O 4 data*
	2	*18*	*J4-72, 70*	*TTL I/O 3 data*
	1	*17*	*J4-76, 74*	*TTL I/O 2 data*
	0	*16*	*J4-80, 78*	*TTL I/O 1 data*
Section ffset:	*Section 1642811 4–FFFF*		*Section 1643Not used.*	

Example 29.

Chapter 10 Motherboard and Daughterboard **Registers**

10.1 Description Motherboard, PN 85002350

The motherboard consists of the VXI bus interface and 128 TTL I/O channels in eight 16-bit groups. Each group consists of driver circuitry to drive sixteen pins, a 16-bit transparent latch for reading the state of the sixteen pins, and control circuitry with five registers to control the behavior of each group.

The registers are paired to permit access to two 16-bit registers as a 32-bit register. The registers are located in the module's address space starting at offset 0x8000. In addition to the D16/D32 capability, configuration jumper J6 on the motherboard can be used to locate the module in the VXI A24 or A32 address spaces. The default is A32.

10.2 Description, Daughterboard, PN 85002360

PN 85002360 Option 2, 32 Differential, 32 Open-Collector, 32 CMOS

This daughterboard consists of 32 differential TTL I/O channels in two 16-bit groups, 32 open collector I/O channels in two 16-bit groups, and 32 CMOS I/O channels in two 16-bit groups. The modes of operation and the control circuitry are the same in each group and are described below. The difference is in the interface at the front panel pins. The differential channels have differential drivers and receivers, which consume two pins for each channel. The open-collector pins have a TTL compatible open-collector buffer, and the CMOS pins have a TTL compatible CMOS buffer.

10.3 Description, Daughterboard, PN 85002370

Option 1PN 85002370 Option 1, 128 TTL I/O

This daughterboard consists of 128 TTL I/O channels in eight 16-bit groups. The modes of operation and the control circuitry are the same in each group and are described below.

10.4 Description, Control Logic

There are five 16-bit registers for each group. At reset time all registers hold the value of 0x0. The five registers are:

Output Data. This register is written to by software and represents the data pattern the pins are to be driven to. If the output data polarity bit is set in the control register (register 5 below), the output data pattern will be the complement of the data written to this register.

Input Data. This register is read-only and represents the state of the pins. The data being read can be real-time or latched. If the data has been latched, the latched data is available to be read once. Subsequent reads are real-time until the data is latched again. Latch control is available as a bit in the control register (register 5 below).

Pattern. This register is written to with the data pattern to be compared against the input data (register 2 above) during the compare process.

Mask. This register is written to with a data pattern representing which of the 16 pins of input data (register 2 above) participate in the compare process.

Control. This register controls the mode of operation of the group.

10.5 The Gate

Within the control circuitry for each group is a gate signal. The gate is normally off, and is controlled by software or by hardware. Software controls the gate by way of 'on' and 'off' strobes. If an 'on' strobe is issued, the gate turns on. If an 'off' strobe is issued, the gate turns off. Hardware control of the gate is by way of the dedicated external input control line for the group. The control line is input only, TTL compatible, terminated with a 3 volt, 200 Ohm, Thevenin termination. The control line can be used to drive the gate directly, where line on means gate on, and line off means gate off. Or the control line can be used to pulse the gate on or off. In this mode the first pulse turns the gate on and the second pulse turns the gate off.

The gate is the heart of the control circuitry for the group. The data driven out is affected by the state of the gate, and activity can be generated at the edges of the gate (when the gate transitions on or off). Modes of operation will now be described and how the gate is involved.

Table 10-1. Modes of Operation

The modes of operation are controlled by turning control register bits on or off.

Default	The default condition is the reset state where all bits in the control register are low. The default is high impedance at the I/O pins, and read-only of the input data. The gate has no affect in this mode. The only activity that is possible is real-time reading of the state of the pins. Since the output drive is turned off, external data can be driven into the pins and read by software.
Output Drive Control	Setting bit 0 (LSB) HIGH will allow the output data to appear at the pins while the gate is on. When the gate is off the pins return to high impedance.

Return to Zero	Setting bit 3 high enables the 'return to' mode. Setting bit 4 low will cause all sixteen pins to be driven low while the gate is off. While the gate is on the pins are driven to what is stored in the output data register.
Return to One	Setting bit 3 high enables the 'return to' mode. Setting bit 4 high will cause all sixteen pins to be driven high while the gate is off. While the gate is on the pins are driven to what is stored in the output data register.
Latched Input Data	Setting bit 9 high permits input data to be latched. Setting bit 7 low will cause input data to be latched on the leading edge of the gate. Setting bit 7 high will cause input data to be latched on the trailing edge of the gate. If the data has been latched, the latched data is readable one time only. Subsequent reads are real-time until the data is latched again by a gate.
Interrupt Generation	Setting bit 5 high enables the group to generate interrupts based on the states of bits 6 and 7. Setting bit 6 low allows interrupts on every gate. Setting bit 6 high permits interrupts only if there is a gate and a data match between the input data, the pattern register, and the mask register. Setting bit 7 low allows interrupt generation on the leading edge of the gate. Setting bit 7 high allows interrupt generation on the trailing edge of the gate.
Pattern Matching	Data at the pins is constantly compared against the pattern and mask registers. If there is a match, an interrupt can be generated on the leading or trailing edge of the gate as described in "Interrupt Generation".
Comple-mented Output Data	Setting bit 10 will cause the data driven out to the pins to be the complement of the data stored in the output register.
External Control	Setting bit 8 high enables the external control line to control the gate. Bit 2 is used to permit the control circuitry to recognize a low-true or high-true signal on the external control line. Bit 1 low causes the gate to follow the external control signal; signal on means gate on and signal off means gate off. Bit 1 highs causes the gate to be pulsed on and off by the external control signal. In this mode, the first pulse in the external control signal will turn the gate on and a second pulse will turn the gate off. Bit 2 is employed to allow high-true or low-true pulses.

10.6 Register Programming Technique

The ASCOR module registers listed in Table 9-2 *on page 19 (motherboard),* Table 9-3 *on page 38 (daughterboard* PN 85002360 Option 2*) and* Table 9-4 *on page 38 (daughterboard* PN 85002370 Option 1*) are accessed under VXI A24/A32 Address Mode as 16-bit or 32-bit words. Since all 16 bits or 32 bits are programmed with a single write operation, care must be taken to preserve the state of bits that effect other functions. In order to avoid changing any other bits in a register use the following procedure:*

1. *Read the register first into memory.*

   Write only to the bit(s) in memory that you intend to change.

   Write the new value back to the register.

10.7 Register Programming Examples

In the examples, it is assumed that the module is assigned A32 space 0x20000000, and its Logical Address is 8.

Turn on TTL channels 1–16. The data pattern found at the 16 output pins is now 0xAAAA. Invert the data and the output data pattern is now 0x5555. Lastly, turn off (HI-Z) the group.

Section 1644A32 Write Address	*Section 1645 16 Data*	*Section 1646Comments*
0x20008000	*0x1*	*set the direction to out*
0x20008030	*0xAAAA*	*the data*
0x20008050	*don't care*	*output pins should be driving 0xAAAA*
0x20008000	*0x401*	*invert the data*
0x20008050	*don't care*	*output pins should be driving 0x5555*
0x20008054	*don't care*	*tri-state the group*

After writing to 0x20008050, read 0x20008040 to read the output pin state.

Drive TTL channels 1–16 low when the input control line is low, and high when the input control line is high.

Section 1647A32 Write Address	*Section 1648 16 Data*	*Section 1649Comments*
0x20008030	*0x0*	*the data*
0x20008000	*0x119*	*external control, return to one*

All 16 outputs should follow the external control line.

Modify 0 so that the external control line is treated as pulses. The first pulse drives the pins low and the second pulse drives them high.

Section 1650A32 Write Address	Section 1651 16 Data	Section 1652Comments
0x20008030	0x0	the data
0x20008000	0x11B	external control, return to one

The outputs should be high. When the control line goes low the outputs will go low. The outputs stay low until the control line goes low a second time.

Modify 0 so that on the trailing (rising) edge of the external control VXI interrupt #3 is generated.

Section 1653A16 Write Address	Section 1654 16 Data	Section 1655Comments
0xC23E	0xC	set interrupt to #3

Section 1656A32 Write Address	Section 1657 16 Data	Section 1658Comments
0x20008030	0x0	the data
0x20008000	0x1B9	external control, return to one interrupt on trailing edge of gate

The outputs should be high, waiting for the external control to go low. When the control line goes low, all 16 outputs go low. When the control line goes high, all 16 outputs go high and interrupt 3 is generated.

Set TTL channels 1–16 to input only. An interrupt is generated if TTL channel 1 goes high during the compare window.

Section 1659A16 Write Address	Section 1660I 16 Data	Section 1661Comments
0xC23E	0x10	set interrupt to #4

Section 1662A32 Write Address	Section 1663I 16 Data	Section 1664Comments
0x20008010	0x1	mask off all but channel 1
0x20008020	0x1	expect a one on channel 1
0x20008000	0x1E0	interrupt on trailing edge of gate if there was a data match

Assume at this point channel 1 is being driven low by some external source, and the external control line is being driven high. When the control line goes low compare is enabled. If channel 1 stays low the entire time and the control line goes high, no interrupt is generated. If channel 1 is driven high while the control line is low, interrupt 4 will be generated when the control line goes high.

Set TTL channels 1–16 to input only. The external control line is used to latch the state of the pins for later reading. An interrupt is generated to let the software know that there is latched data ready to read.

Section 1665A16 Write Address	Section 1666I 16 Data	Section 1667Comments
0xC23E	0x14	set interrupt to #5

Section 1668A32 Write Address	Section 1669I 16 Data	Section 1670Comments
0x20008000	0x3A4	high true external control, latch data and generate interrupt when external control goes low

Assume channels 1–16 are being driven to 0xFFFF and the external control is low. Next channels 1–16 are driven to 0xAA55 and the control line goes high. Next the control line goes low and moments later the channels return to 0xFFFF. At this point interrupt 5 is generated. Reading A32 address 0x20008040 will yield 0xAA55. Reading the same address again will yield 0xFFFF. The first read was latched data. The second read was the present state of channels 1–16.

Turn on TTL channels 1–128. Each group outputs different data. Next, turn all 128 channels off (HI-Z). Example uses 32-bit data.

Section 1671A32 Write Address	*Section 1672 32 Data*	*Section 1673Comments*
0x20008000	*0x00010001*	*set the direction to out, channels 1–32*
0x20008004	*0x00010001*	*set the direction to out, channels 33–64*
0x20008008	*0x00010001*	*set the direction to out, channels 65–96*
0x2000800C	*0x00010001*	*set the direction to out, channels 97–128*
0x20008030	*0x02020101*	*data, channels 1–32*
0x20008034	*0x08080404*	*data, channels 33–64*
0x20008038	*0x20201010*	*data, channels 65–96*
0x2000803C	*0x80804040*	*data, channels 97–128*
0x20008090	*don't care*	*all 128 pins should be driving*
0x20008094	*don't care*	*all 128 pins should be HI-Z*

10.8 General Programming Examples

Obtains the A24 Base Address using National Instruments NI-VXI GetDevInfo.

Procedure obtains the A24 Base Address using its base. The Logical Address is 5.

```
/* C code segment for obtaining the device's A24 Base Address */

int16     ret;
uint16    la        = 5;      /* Logical Address */
uint16    field     = 12;     /* Base of A24 address space */
uint32    baseA24;

/* Get the A24 Base Address */
ret = GetDevInfo (la, field, &baseA24);

/* Check for function error /
if (ret < 0)
          /* Error occurred during GetDevInfo. */;
```

Obtains the A32 Base Address using National Instruments NI-VXI GetDevInfo.

Procedure obtains the A32 Base Address using its base. The Logical Address is 5.

```
/* C code segment for obtaining the device's A32 Base Address */

int16     ret;
uint16    la        = 5;      /* Logical Address */
uint16    field     = 12;     /* Base of A32 address space */
uint32    baseA32;

/* Get the A32 Base Address */
ret = GetDevInfo (la, field, &baseA32);

/* Check for function error */
if (ret < 0)
          /* Error occurred during GetDevInfo.*/;
```

Writes to the first module register using National Instruments NI-VXI calls, A24 Address Mode, and 16-bit data.

Procedure writes the value 1000h to the first module register. The A24 Base Address is 200000h.

```
/* C code segment for writing the value 0x1000h to the first module */
/* Register, assuming an A24 Base Address of 200000h */

int16     ret;
uint16    accessparms    =2;  /* A24, Nonprivileged data access, */
                              /* Motorola Byte Order */

uint32    address;
uint16    width          =2;  /* width = word (16 bits) */
uint32    value32;

address = 0x208000;           /* A24 Base Address + first module  */
                              /* Register offset */
value32 = 0x1000;             /* Value to write to the first module */
                              /* Register */

/* Write to the First module register. */
ret = VXIout (accessparms, address, width, value32);

/* Check for write error. */
if (ret<0)
          /* Error occurred during write. */;
```

Writes to the first module register using VXIplug&play VISA calls, A24 Address Mode, and 16-bit data.

Procedure writes the value 2000h to the first module register. The variable, "vi" references the Logical Address.

```
/* C code segment for writing the value 0x2000 to the first module */
/* Register */

ViStatus       as3xxx_status;
ViSession      vi;                 /* vi from previous call to */
                                   /* as3xxx_init */
ViUlnt16       space=VI_A24_SPACE; /* A24 Address Space */
ViBusAddress   offset=0x8000;      /* first module register offset. */
ViUlnt16       value16;

value16 = 0x2000;                  /* Value to write to the first */
                                   /* module register */

/* Write to the first module register. */
as3xxx_status = ViOut16 (vi, space, offset, value16);

/* Check for write error. */
if (as3xxx_status < VI_SUCCESS)
          /* Error occurred during write. */;
```

Writes to the first module register using National Instruments NI-VXI calls, A32 Address Mode, and 32-bit data.

Procedure writes the value 10000h to the first module register. The A32 Base Address is 20000000h.

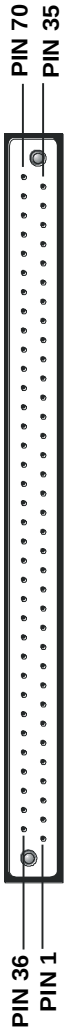
```
/* C code segment for writing the value 0x10000000 to the first */
/* module register, assuming an A32 Base Address of 20000000h */

int16     ret;
uint16    accessparms    =3;  /* A32, Nonprivileged data access, */
                              /* Motorola Byte Order */

uint32    address;
uint16    width          =4;  /* width = long word (32 bits) */
uint32    value32;

address = 0x20008000;          /* A32 Base Address + first module  */
                               /* register offset */
value32 = 0x10000;             /* Value to write to the first module */
                               /* register */

/* Write to the First module register. */
ret = VXIout (accessparms, address, width, value32);

/* Check for write error. */
if (ret<0)
          /* Error occurred during write. */;
```

Writes to the first module register using VXIplug&play VISA calls, A32 Address Mode, and 32-bit data.

Procedure writes a value to all bits of the first module register, assuming that A32 Address Space is configured. The variable, "vi" references the Logical Address.

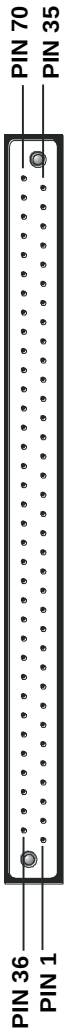
```
/* C code segment for writing the value 0x10000000 to the first */
/* module register */

ViStatus       as3xxx_status;
ViSession      vi;                 /* vi from previous call to */
                                   /* as3xxx_init */
ViUlnt16       space=VI_A32_SPACE; /* A32 Address Space */
ViBusAddress   offset=0x8000;      /* first module register offset. */
ViUlnt32       value32;

Value32 = 0x10000000;         /* Value to write to the first module */
                              /* register */

/* Write to the first module register. */
as3xxx_status = ViOut32 (vi, space, offset, value32);

/* Check for write error. */
if (as3xxx_status < VI_SUCCESS)
          /* Error occurred during write. */;
```

Table 11-1. Front Panel Connector Motherboard J1 Pin Signals



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
TTL_GATE_113_128	69	34	TTL_GATE_97_112
TTL_GATE_81_96	68	33	TTL_GATE_65_80
TTL128	67	32	TTL127
TTL126	66	31	TTL125
TTL124	65	30	TTL123
TTL122	64	29	TTL121
TTL120	63	28	TTL119
TTL118	62	27	TTL117
TTL116	61	26	TTL115
TTL114	60	25	TTL113
TTL112	59	24	TTL111
TTL110	58	23	TTL109
TTL108	57	22	TTL107
TTL106	56	21	TTL105
TTL104	55	20	TTL103
TTL102	54	19	TTL101
TTL100	53	18	TTL99
TTL98	52	17	TTL97
TTL96	51	16	TTL95
TTL94	50	15	TTL93
TTL92	49	14	TTL91
TTL90	48	13	TTL89
TTL88	47	12	TTL87
TTL86	46	11	TTL85
TTL84	45	10	TTL83
TTL82	44	9	TTL81
TTL80	43	8	TTL79
TTL78	42	7	TTL77
TTL76	41	6	TTL75
TTL74	40	5	TTL73
TTL72	39	4	TTL71
TTL70	38	3	TTL69
TTL68	37	2	TTL67
TTL66	36	1	TTL65

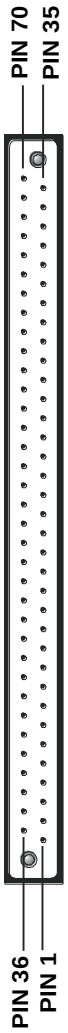
Table 11-2. Front Panel Connector Motherboard J2 Pin Signals



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
TTL_GATE_49_64	69	34	TTL_GATE_33_48
TTL_GATE_17_32	68	33	TTL_GATE_1_16
TTL64	67	32	TTL63
TTL62	66	31	TTL61
TTL60	65	30	TTL59
TTL58	64	29	TTL57
TTL56	63	28	TTL55
TTL54	62	27	TTL53
TTL52	61	26	TTL51
TTL50	60	25	TTL49
TTL48	59	24	TTL47
TTL46	58	23	TTL45
TTL44	57	22	TTL43
TTL42	56	21	TTL41
TTL40	55	20	TTL39
TTL38	54	19	TTL37
TTL36	53	18	TTL35
TTL34	52	17	TTL33
TTL32	51	16	TTL31
TTL30	50	15	TTL29
TTL28	49	14	TTL27
TTL26	48	13	TTL25
TTL24	47	12	TTL23
TTL22	46	11	TTL21
TTL20	45	10	TTL19
TTL18	44	9	TTL17
TTL16	43	8	TTL15
TTL14	42	7	TTL13
TTL12	41	6	TTL11
TTL10	40	5	TTL9
TTL8	39	4	TTL7
TTL6	38	3	TTL5
TTL4	37	2	TTL3
TTL2	36	1	TTL1

Table 11-3. Front Panel Connector Daughterboard PN 85002360 J3 Pin Signals

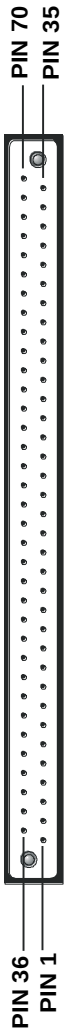
Note: Option 2: 32 Open-Collector and 32 CMOS Channels



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
CMOSGATE_17_32	69	34	CMOSGATE_1_16
OCGATE_17_32	68	33	OCGATE_1_16
CMOS32	67	32	CMOS31
CMOS30	66	31	CMOS29
CMOS28	65	30	CMOS27
CMOS26	64	29	CMOS25
CMOS24	63	28	CMOS23
CMOS22	62	27	CMOS21
CMOS20	61	26	CMOS19
CMOS18	60	25	CMOS17
CMOS16	59	24	CMOS15
CMOS14	58	23	CMOS13
CMOS12	57	22	CMOS11
CMOS10	56	21	CMOS9
CMOS8	55	20	CMOS7
CMOS6	54	19	CMOS5
CMOS4	53	18	CMOS3
CMOS2	52	17	CMOS1
OC32	51	16	OC31
OC30	50	15	OC29
OC28	49	14	OC27
OC26	48	13	OC25
OC24	47	12	OC23
OC22	46	11	OC21
OC20	45	10	OC29
OC18	44	9	OC17
OC16	43	8	OC15
OC14	42	7	OC13
OC12	41	6	OC11
OC10	40	5	OC9
OC8	39	4	OC7
OC6	38	3	OC5
OC4	37	2	OC3
OC2	36	1	OC1

Table 11-4. Front Panel Connector Daughterboard PN 85002360 J4 Pin Signals

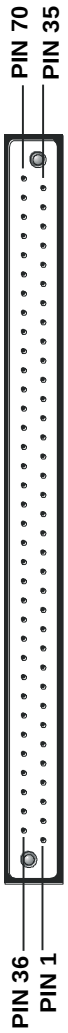
Note: Option 2: 32 Differential Channels



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
(EMPTY)	69	34	(EMPTY)
DIFF_GATE_17_32	68	33	DIFF_GATE_1_16
DIFF32–	67	32	DIFF32+
DIFF31–	66	31	DIFF31+
DIFF30–	65	30	DIFF30+
DIFF29–	64	29	DIFF29+
DIFF28–	63	28	DIFF28+
DIFF27–	62	27	DIFF27+
DIFF26–	61	26	DIFF26+
DIFF25–	60	25	DIFF25+
DIFF24–	59	24	DIFF24+
DIFF23–	58	23	DIFF23+
DIFF22–	57	22	DIFF22+
DIFF21–	56	21	DIFF21+
DIFF20–	55	20	DIFF20+
DIFF19–	54	19	DIFF19+
DIFF18–	53	18	DIFF18+
DIFF17–	52	17	DIFF17+
DIFF16–	51	16	DIFF16+
DIFF15–	50	15	DIFF15+
DIFF14–	49	14	DIFF14+
DIFF13–	48	13	DIFF13+
DIFF12–	47	12	DIFF12+
DIFF11–	46	11	DIFF11+
DIFF10–	45	10	DIFF10+
DIFF9–	44	9	DIFF9+
DIFF8–	43	8	DIFF8+
DIFF7–	42	7	DIFF7+
DIFF6–	41	6	DIFF6+
DIFF5–	40	5	DIFF5+
DIFF4–	39	4	DIFF4+
DIFF3–	38	3	DIFF3+
DIFF2–	37	2	DIFF2+
DIFF1–	36	1	DIFF1+

Table 11-5. Front Panel Connector Daughterboard PN 85002370 J3 Pin Signals

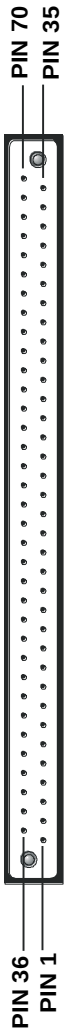
Note: Option 1: TTL Channels 193–256



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
TTL_GATE_241_256	69	34	TTL_GATE_225_240
TTL_GATE_209_224	68	33	TTL_GATE_193_208
TTL256	67	32	TTL255
TTL254	66	31	TTL253
TTL252	65	30	TTL251
TTL250	64	29	TTL249
TTL248	63	28	TTL247
TTL246	62	27	TTL245
TTL244	61	26	TTL243
TTL242	60	25	TTL241
TTL240	59	24	TTL239
TTL238	58	23	TTL237
TTL236	57	22	TTL235
TTL234	56	21	TTL233
TTL232	55	20	TTL231
TTL230	54	19	TTL229
TTL228	53	18	TTL227
TTL226	52	17	TTL225
TTL224	51	16	TTL223
TTL222	50	15	TTL221
TTL220	49	14	TTL219
TTL218	48	13	TTL217
TTL216	47	12	TTL215
TTL214	46	11	TTL213
TTL212	45	10	TTL211
TTL210	44	9	TTL209
TTL208	43	8	TTL207
TTL206	42	7	TTL205
TTL204	41	6	TTL203
TTL202	40	5	TTL201
TTL200	39	4	TTL199
TTL198	38	3	TTL197
TTL196	37	2	TTL195
TTL194	36	1	TTL193

Table 11-6. Front Panel Connector Daughterboard PN 85002370 J4 Pin Signals

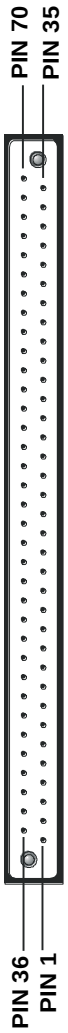
Note: Option 1: TTL Channels 129–192



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
TTL_GATE_177_192	69	34	TTL_GATE_161_176
TTL_GATE_145_160	68	33	TTL_GATE_129_144
TTL192	67	32	TTL191
TTL190	66	31	TTL189
TTL188	65	30	TTL187
TTL186	64	29	TTL185
TTL184	63	28	TTL183
TTL182	62	27	TTL181
TTL180	61	26	TTL179
TTL178	60	25	TTL177
TTL176	59	24	TTL175
TTL174	58	23	TTL173
TTL172	57	22	TTL171
TTL170	56	21	TTL169
TTL168	55	20	TTL167
TTL166	54	19	TTL165
TTL164	53	18	TTL163
TTL162	52	17	TTL161
TTL160	51	16	TTL159
TTL158	50	15	TTL157
TTL156	49	14	TTL155
TTL154	48	13	TTL153
TTL152	47	12	TTL151
TTL150	46	11	TTL149
TTL148	45	10	TTL147
TTL146	44	9	TTL145
TTL144	43	8	TTL143
TTL142	42	7	TTL141
TTL140	41	6	TTL139
TTL138	40	5	TTL137
TTL136	39	4	TTL135
TTL134	38	3	TTL133
TTL132	37	2	TTL131
TTL130	36	1	TTL129

Table 11-7. Front Panel Connector Daughterboard PN 85002630 J4 Pin Signals

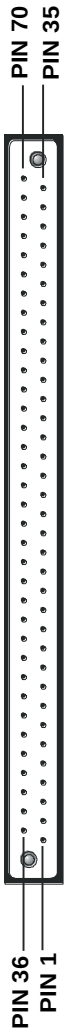
Note: Option 3: 64 Differential Channels (see J3 for channels 33-64)



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
(EMPTY)	69	34	(EMPTY)
DIFF_GATE_17_32	68	33	DIFF_GATE_1_16
DIFF32–	67	32	DIFF32+
DIFF31–	66	31	DIFF31+
DIFF30–	65	30	DIFF30+
DIFF29–	64	29	DIFF29+
DIFF28–	63	28	DIFF28+
DIFF27–	62	27	DIFF27+
DIFF26–	61	26	DIFF26+
DIFF25–	60	25	DIFF25+
DIFF24–	59	24	DIFF24+
DIFF23–	58	23	DIFF23+
DIFF22–	57	22	DIFF22+
DIFF21–	56	21	DIFF21+
DIFF20–	55	20	DIFF20+
DIFF19–	54	19	DIFF19+
DIFF18–	53	18	DIFF18+
DIFF17–	52	17	DIFF17+
DIFF16–	51	16	DIFF16+
DIFF15–	50	15	DIFF15+
DIFF14–	49	14	DIFF14+
DIFF13–	48	13	DIFF13+
DIFF12–	47	12	DIFF12+
DIFF11–	46	11	DIFF11+
DIFF10–	45	10	DIFF10+
DIFF9–	44	9	DIFF9+
DIFF8–	43	8	DIFF8+
DIFF7–	42	7	DIFF7+
DIFF6–	41	6	DIFF6+
DIFF5–	40	5	DIFF5+
DIFF4–	39	4	DIFF4+
DIFF3–	38	3	DIFF3+
DIFF2–	37	2	DIFF2+
DIFF1–	36	1	DIFF1+

Table 11-8 Front Panel Connector Daughterboard PN 85002630 J3 Pin Signals

Note: Option 3: 64 Differential Channels (see J4 for channels 1-32)



Function	Pin	Pin	Function
CHASSIS GROUND	70	35	DIGITAL GROUND
(EMPTY)	69	34	(EMPTY)
DIFF_GATE_33_48	68	33	DIFF_GATE_49_64
DIFF64–	67	32	DIFF64+
DIFF63–	66	31	DIFF63+
DIFF62–	65	30	DIFF62+
DIFF61–	64	29	DIFF61+
DIFF60–	63	28	DIFF60+
DIFF59–	62	27	DIFF59+
DIFF58–	61	26	DIFF58+
DIFF57–	60	25	DIFF57+
DIFF56–	59	24	DIFF56+
DIFF55–	58	23	DIFF55+
DIFF54–	57	22	DIFF54+
DIFF53–	56	21	DIFF53+
DIFF52–	55	20	DIFF52+
DIFF51–	54	19	DIFF51+
DIFF50–	53	18	DIFF50+
DIFF49–	52	17	DIFF49+
DIFF48–	51	16	DIFF48+
DIFF47–	50	15	DIFF47+
DIFF46–	49	14	DIFF46+
DIFF45–	48	13	DIFF45+
DIFF44–	47	12	DIFF44+
DIFF43–	46	11	DIFF43+
DIFF42–	45	10	DIFF42+
DIFF41–	44	9	DIFF41+
DIFF40–	43	8	DIFF40+
DIFF39–	42	7	DIFF39+
DIFF38–	41	6	DIFF38+
DIFF37–	40	5	DIFF37+
DIFF36–	39	4	DIFF36+
DIFF35–	38	3	DIFF35+
DIFF34–	37	2	DIFF34+
DIFF33–	36	1	DIFF33+