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Network Analyzer



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Errata

Title & Document Type: 3570A Network Analyzer Operating and Service Manual

Manual Part Number: 03570-90015

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About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

HP References in this Manual

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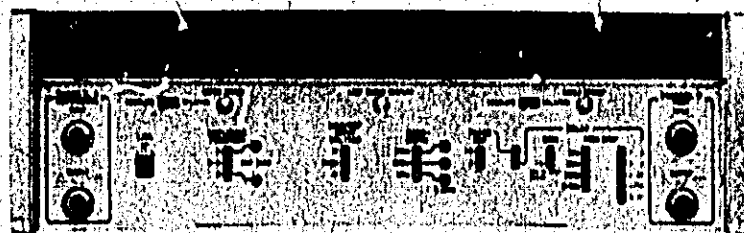


Agilent Technologies

3570A

OPERATING AND SERVICE MANUAL

NETWORK ANALYZER 3570A



HEWLETT  PACKARD



OPERATING AND SERVICE MANUAL

MODEL 3570A NETWORK ANALYZER

Serial Number: 1331A00516 and higher (see note below)

IMPORTANT NOTICE

This loose leaf manual does not normally require a change sheet. All major change information has been integrated into the manual by page revision. In cases where only minor changes are required, a change sheet may be supplied.

If the Serial Number of your instrument is lower than the one on this title page, the manual contains revisions that do not apply to your instrument. Backdating information given in the manual adapts it to earlier instruments.

Where practical, backdating information is integrated into the text, parts list and schematic diagrams. Backdating changes are denoted by a delta sign. An open delta (Δ) or lettered delta (Δ_A) on a given page, refers to the corresponding backdating note on that page. Backdating changes not integrated into the manual are denoted by a numbered delta (Δ_1) which refers to the corresponding change in the Backdating Section (Section VIII).

WARNING

To help minimize the possibility of electrical fire or shock hazards, do not expose this instrument to rain or excessive moisture.

Manual Part No. 03570-90015

Microfiche Part No. 03570-90065

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P.O. Box 301 Loveland, Colorado, U.S.A. 80537

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HEWLETT  PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this instrument met its published specifications at the time of shipment from the factory, Hewlett-Packard Company further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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SECTION I

GENERAL INFORMATION

1-1. DESCRIPTION.

1-2. The Hewlett-Packard Model 3570A Network Analyzer is a narrow-band tracking detector designed to operate in conjunction with an -hp- Model 3320A/B Frequency Synthesizer or an -hp- Model 3330A/B Automatic Synthesizer. The Synthesizer/Analyzer combination forms a versatile measurement system for precision network analysis in the 50 Hz to 13 MHz frequency range. The 3570A Network Analyzer is an integral part of the 3040A, 3041A and 3042A Systems.

1-3. The Model 3570A is designed to measure the amplitude and phase response of two-port linear networks in the frequency domain. It can be used for measuring the absolute transfer functions of networks or for comparing two networks. The major features of the instrument include two identical measurement channels, 100 dB dynamic range (200 Hz to 13 MHz), selectable bandwidths, (10 Hz, 170 Hz and 3 kHz), two digital readouts for simultaneous amplitude and phase presentations, plus complete programmability of all functions, ranges and settings. These standard features, along with optional group delay measurements, offset measurements, limit tests and digital (Isolated General Purpose Interface Bus) outputs, make the 3570A a truly flexible instrument that is well suited for laboratory, maintenance and production-line applications.

1-4. SPECIFICATIONS.

1-5. Table 1-1 is a complete list of the Model 3570A critical specifications that are controlled by tolerances. Table 1-2 contains general information that describes the operating characteristics of the Model 3570A.

1-6. Any changes in specifications due to manufacturing, design, or traceability to the U.S. National Bureau of Standards are included in Table 1-1 in this manual. Specifications listed in this manual supersede all previous specifications for the Model 3570A.

1-7. OPTIONS.

1-8. There are presently four options available for the Model 3570A. These options are listed in Table 1-3. For

further information concerning options, refer to Table 1-2 or Section III in this manual or contact the nearest -hp- Sales and Service Office.

NOTE

The 3570A option numbers used throughout this manual correspond with the 3040A, 3041A and 3042A Systems option numbers listed in Table 1-6.

1-9. ACCESSORIES SUPPLIED.

1-10. Table 1-4 is a list of accessories supplied with the Model 3570A.

NOTE

In addition to the accessories listed in Table 1-4, a spare numeric display module (-hp- Part No. 1990-0329) is included with the instrument. The spare module is plugged into the foam block above the crystal in the A3 card nest and is accessible with the top covers (outer and inner) of the instrument removed.

1-11. ACCESSORIES AVAILABLE.

1-12. Table 1-5 is a list of Hewlett-Packard accessories available for use with the Model 3570A.

1-13. INSTRUMENT AND MANUAL IDENTIFICATION.

1-14. Hewlett-Packard uses a two-section serial number. The first section (prefix) identifies a series of instruments. The last section (suffix) identifies a particular instrument within the series. If a letter is included with the serial number, it identifies the country in which the instrument was manufactured. If the serial number of your instrument is lower than the one on the title page of this manual, refer to Appendix C for backdating information that will adapt this manual to your instrument. All correspondence with Hewlett-Packard should include the complete serial number.

Table 1-1. Specifications.

FREQUENCY RANGE: 50 Hz to 13 MHz

CHANNEL A AND B OUTPUTS:

Output impedance: 50 Ω or 75 Ω $\pm$ 2%.

Maximum output: 1 V rms into 50 Ω or 75 Ω .

Transfer accuracy: $\pm$ 0.4 dB

CHANNEL A AND B INPUTS:

Input impedance: 1 M Ω $\pm$ 2% shunted by < 30 pF.

Input signal range: 1 V rms to 1 μ V rms.

AMPLITUDE ACCURACY (25°C $\pm$ 5°C):

Absolute: No spec. may be calibrated to source using front panel adjustments.

Relative (relative to 0 dB input for 1 V, 0 dBm, and 0.1 V range): A or B "Amplitude Function" (B-A specification determined by sum of Channel A and B accuracies).

10 Hz BW, 100 Hz BW and 3 kHz BW on 1 V range

3 kHz BW, 0.1 V range and 0 dBm range

0 dB	-20 dB	-70 dB	-80 dB	-100 dB
$\pm$ 0.2 dB	$\pm$ 0.5 dB			$\pm$ 1.5 dB
$\pm$ 0.2 dB	$\pm$ 0.5 dB			*Not Specified

*Due to lower noise rejection of 3 kHz BW.

FREQUENCY RESPONSE:

A or B "Amplitude Function": $\leq$ $\pm$ 0.5 dB p-p error.

B - A "Amplitude Function": $\leq$ $\pm$ 0.1 dB p-p error.

DYNAMIC RANGE*

*The following graph is explained in Paragraph 3-59.

FREQUENCY (Hz)

RESIDUAL RESPONSES:

Power line related spurious responses (50 Hz or 60 Hz).

1 V Range, 0 dBm

Fundamental: > 70 dB below 0.1 V

2nd and 4th harmonics: > 85 dB below 0.1 V

3rd harmonic: > 80 dB below 0.1 V

5th harmonic: > 80 dB below 0.1 V

6th and 7th harmonics: > 95 dB below 0.1 V

1 V Range

Fundamental: > 80 dB below 1 V

2nd harmonic: > 95 dB below 1 V

3rd harmonic: > 90 dB below 1 V

RF Feedthru at 100 kHz: < -60 dB

AMPLITUDE STABILITY (8 hr., 25°C $\pm$ 1°C after 3 hr. warmup):

	0 dB	-20 dB	-80 dB	-100 dB
100 Hz and 3 kHz BW	$\pm$ 0.05 dB	$\pm$ 0.05 dB	Not specified	
10 Hz BW	$\pm$ 0.05 dB	$\pm$ 0.15 dB	Not specified	

Temperature coefficient (20°C to 30°C):

100 Hz and 3 kHz BW: $\pm$ 0.02 dB/°C

10 Hz BW: $\pm$ 0.05 dB/°C

PHASE MEASUREMENTS: Phase reference is Channel A.

A/A reference offset: 180° $\pm$ 0.4°

Phase Accuracy (25°C $\pm$ 5°C):

Phase linearity: $\pm$ 0.2° (Channel B within 6 dB of Channel A)

Frequency Response: (Channels at 0 dB)

50 Hz	100 Hz	1 MHz	13 MHz
$\pm$ 0.5°	$\pm$ 0.2°		$\pm$ 1°

Amplitude Response: (Channel B within 6 dB of Channel A)

0 dB	-20 dB	-70 dB	-80 dB	-100 dB
$\pm$ 0.4°	$\pm$ 0.5°	$\pm$ 1°		Not specified

Amplitude Response: (For channels at different levels, specification determined by lowest input)

0 dB	-20 dB	-60 dB	-70 dB	-100 dB
1 Volt Range 50 Hz-60 Hz	$\pm$ 1.3°	$\pm$ 1.5°	$\pm$ 3.5°	NOT SPECIFIED

0 dB	-20 dB	-60 dB	-80 dB	-100 dB
1 Volt Range 60 kHz-13 MHz	$\pm$ 1.3°	$\pm$ 1.5°	$\pm$ 3.5°	NOT SPECIFIED

*See General Information for operating notes.

PEAK-PEAK-NOISE vs. AMPLITUDE: (dependent on bandwidth)

P-P Noise in Degrees (95% confidence level)

DELAY ACCURACY: ($\pm$ % of reading + % of measurement range)

0 dB	-40 dB	-80 dB	-100 dB
$\pm$ (0.2% + 0.2%)	$\pm$ (0.5% + 0.5%)	Not Specified	

MEASUREMENT RANGE:

5 ranges, 19,999 μ s, 199.99 μ s, 1.9999 ms, 19.999 ms and 199.99 ms.

Table 1-2. General Information.

INPUTS*

Front Panel Inputs (A and B):

Connectors: female BNC

Impedance: 1 M Ω , shunted by < 30 pF (28 pF nominal)

Maximum (ac) Input Voltage:

Max/Ref Input Voltage Gating	Maximum Input Voltage
1 V	1 V rms
0 dBm	0.2236 V rms (50 ohms)
	0.2739 V rms (75 ohms)
0.1 V	0.1 V rms

Overload Protection: 15 V rms

Coupling: capacitive

Maximum (dc) Input Voltage: ± 50 Vdc

DC Isolation: none (Inputs referenced to frame ground)

Rear Panel Inputs:

INPUT $\odot$: Triaxial connector mates with -hp- 11172B RF Input Cable connected to ALT OUTPUT $\odot$ of Synthesizer. Receives 50 Hz to 13 MHz signal input from Synthesizer.

Impedance: 50 ohms (std) 75 ohms (Options 001, 003)

20 - 33 MHz INPUT $\square$: Female BNC connector receives 20 MHz to 33 MHz tracking signal from 20 - 33 MHz OUTPUT $\square$ of Synthesizer.

1 MHz INPUT Δ : Female BNC connector receives 1 MHz reference signal from 1 MHz OUTPUT Δ of Synthesizer.

OUTPUTS*

Front Panel Outputs (A and B):

Connectors: female BNC

Impedance: 50 ohms (std) 75 ohms (Options 001, 003)

Coupling: direct

Maximum Applied Voltage: ± 6 Vdc

Output Level: Equal to level set on Synthesizer when driving a 50 - ohm (or 75 - ohm) load.

Maximum (ac) Output Voltage:

2 V rms (open circuit)

1 V rms (50 - ohm or 75 - ohm load)

Maximum (dc) Output Voltage: ± 10 mVdc (nominal)

Transfer Accuracy: ± 0.4 dB (nominal)

DC Isolation: none (output common connects directly to frame ground)

*NOTE: All instrument connections should use double shielded BNC or TRIAX cables. Cables of excessive length may degrade the ability of the Network Analyzer to meet specifications.

Analog Outputs:

Connectors: female BNC

Resistance: 1 k Ω (nominal)

Amplitude Function Output: Supplies dc voltage proportional to amplitude (A, B or B - A)

Output Level: 0.1 V/dB (0 V to ± 10 Vdc for 0 dB to ± 100 dB)

Phase/Delay Output: Supplies dc voltage proportional to phase and dc voltage proportional to group delay (in Sweep Delay Mode only).

Phase Output Level: 0.05 Vdc per degree (0 V to ± 9 Vdc for 0 to ± 180 degrees)

Delay Output Level: 5 mVdc per count (0 V to ± 10 Vdc for 0 to $\pm 1,999$ counts)

Delay (X - Y Recorder) Output: Supplies dc voltage proportional to group delay in Swept Delay Mode. No meaningful output in Phase or CW Delay Mode. Output is controlled by a sample and hold circuit which retains previous reading if present reading exceeds 2,000 counts.

Output Level: 5 mVdc per count (0 V to ± 10 Vdc for 0 to $\pm 1,999$ counts)

Z Axis Output: Provides markers during frequency or amplitude sweeps. Can be set to intensify eleven points, representing 1, 10 or 100 sweep steps or to intensify only center frequency or center amplitude. During limit tests, only the limit transition points are intensified. Marker intensity can be adjusted using the rear panel INTENSITY control.

Connector: female BNC

Blanking Voltage: + 10 Vdc

Unblanking Voltage: 0 V

Marker Amplitude: 0 V to - 7 V (adjustable)

Output Resistance: 1 k Ω

BANDWIDTHS

Selectable Bandwidths: 10 Hz, 100 Hz and 3 kHz

Shape Factor: 20:1 (nominal)

Rejection Characteristics:

Bandwidth	- 3 dB Points	- 60 dB Points
10 Hz	$f_o \pm 5$ Hz	$f_o \pm 100$ Hz
100 Hz	$f_o \pm 50$ Hz	$f_o \pm 1$ kHz
3 kHz	$f_o \pm 1.5$ kHz	$f_o \pm 30$ kHz

RESPONSE TIME

Typical Settling Time (following 40 dB step):

Bandwidth	80 % Settled	100 % Settled
10 Hz	200 ms	800 ms
100 Hz	20 ms	80 ms
3 kHz	1 ms	4 ms

Table 1-2. General Information (Cont'd).

RANGES

Frequency Range:

Bandwidth	Frequency
10 Hz	50 Hz to 13 MHz
100 Hz	500 Hz to 13 MHz
3 kHz	15 kHz to 13 MHz

Dynamic Range: 100 dB (200 Hz to 13 MHz)

Measurement Range: 120 dB (1 μ V rms to 1 V rms in three ranges):

Max/Ref Input Voltage

Setting	Lower Limit	Upper Limit
1 V	10 μ V rms	1 V rms
0 dBm	> 100 dBm	0 dBm (50 or 75 ohms)
0.1 V	1 μ V rms	0.1 V rms

MEASUREMENTS

Amplitude Measurements:

Amplitude Functions: Channel A (dBV, dBm); Channel B (dBV, dBm); B - A (dB)

Display Range (Log A, Log B): 0 dB to - 100 dB

Display Range (B - A): > 100 dB to + 100 dB

Display Resolution: 0.01 dB

Amplitude Reference (Log A, Log B): 0 dB(V) or 0 dB(m), depending on MAX/REF INPUT VOLTAGE setting:

Range	Reference
1 V	1 V rms = 0 dBV
0 dBm	0 dBm (50 or 75 ohms)
0.1 V	0.1 V rms = 0 dBV

Amplitude Reference [B - A (dB)]: Channel A is reference channel. A positive reading means that the signal applied to Channel B is greater in amplitude than the signal applied to Channel A; a negative reading means that the signal applied to Channel B is lower in amplitude than the signal applied to Channel A.

Phase Measurements:

Phase Measurement Range: 359 degrees (- 179.5 degrees to + 179.5 degrees)

Due to amplitude and frequency response of phase accuracy and peak-to-peak noise specifications, the width of the indeterminate phase measurement region discussed in Section III is effectively increased whenever input level is decreased or input frequency is increased.

Display Resolution: 0.01 degree

Phase Reference: A or - A

1) Channel A is the reference channel. A negative phase reading means that B lags A; a positive readings means that B leads A.

2) With the PHASE REFERENCE switch set to the A position, the phase reading is direct. With the switch set to the - A position, Channel A is inverted and the phase reading is offset by 1.0 degrees.

DIGITAL READOUTS

Level: 4 1/2 digits with decimal indicator, polarity sign and annunciators.

Reading Rate (internal sampling): 4 readings per second

Typical A to D Conversion Time (both displays): 400 μ sec

FRONT PANEL ZERO ADJUSTMENTS

The AMP ZERO and θ ZERO adjustments are provided to compensate for slight changes in accuracy that occur due to environmental changes and changes in Bandwidth.

Recommended Input Configuration: Zero adjustments should be performed with the A and B Outputs, terminated in 50-ohm (or 75-ohm) load, connected to the A and B inputs. Synthesizer should be set to 0 dBm (or 0 dBV), 1 MHz.

Frequency of Adjustments: Zero adjustments should be performed on a daily basis and any time BANDWIDTH setting is changed. If 3570A is operated in an uncontrolled environment, more frequent adjustments may be required.

Typical Adjustment Ranges:

Amplitude Zero: $\pm$ 6 dB

Phase (θ) Zero: $\pm$ 10 degrees

REMOTE PROGRAMMING

The 3570A will recognize an internally preset "listen" address and accept 7-bit parallel, word serial ASCII-coded instructions.

Programmability: All functions, ranges and settings (except LINE and LIMIT SWEEP RESTART).

Remote Control Connector: The REMOTE CONTROL connector is a 36-pin*, male PC connector located on the rear panel of the instrument. The connector mates directly with the -hp- 11236B Multi-Unit Cable and the -hp- 11235A Adapter (the -hp- 11235A Adapter mates with the -hp- 10631 HP-IB and the -hp- Model 3260A Marked Card Programmer).

*Remote Control Lines: Fourteen lines are required for a complete remote input/output and control capability (remaining lines on 36-pin connector are used for digital communication between the 3570A and the 3330A/B Automatic Synthesizer when the two instruments are interconnected with the -hp- 11236B Multi-Unit Cable). The fourteen remote control lines include:

- 7 Data lines (LD1 through LD7)
- 1 Remote Enable line (LREN)
- 1 Multiple Response Enable line (LMRE)
- 1 End Output line (LEOP)
- 3 flag lines:
 - Data Valid (LDAV)
 - Ready For Data (HREFD)
 - Data Accepted (HDAC)
- 1 ground line

Isolation: The 3570A remote input/output lines are not isolated. All lines are referenced to frame ground (except in Isolated Hewlett-Packard Interface Bus Option U04).

Remote Logic: The 3570A uses standard TTL logic:

State	Requirements
Low	gnd. or 0 V to + 0.4 V (3.2 mA max.)
High	open or + 2.5 V to + 5 V

Table 1-2. General Information (Cont'd).

When a line functions as an input it is normally held at +3 Vdc by an internal pullup. When a line functions as an output it will supply up to 48 mA in the low state and up to 0.6 mA in the high state. Assertion States: Assertion states are indicated by the prefix "L" (low) or "H" (high). Two flag lines, HRFD and HDAC, have high assertion states; remaining lines have low assertion states. Timing: Timing is controlled by the LDAH flag from the controller to the 3570A and by the HRFD and HDAC flags from the 3570A to the controller. A maximum of 150 μs is required for the 3570A to accept one data word. Addresses: The 3570A is shipped from the factory with a "listen" address of 041 Octal and a "talk" address of 101 Octal ("talk" address applies to Option 004 only). Address code must be accompanied by a Multiple Response Enable (LMRE) instruction. Address codes can be changed by changing the position of jumper plugs on Address Recognition Assembly, A33.	The Frequency Increment, Δf: The 3570A offers twenty choices of Δf, ranging from 5 Hz to 200 kHz in decade multiples of 5 Hz, 10 Hz, 16.6 Hz and 20 Hz. The selection can be made using the front panel FREQ STEP controls or by remote ASCII coded instructions. Delay Measurement Range: Five Ranges: 19.99 μs 199.99 μs 1.9999 ms 19.999 ms 199.99 ms Delay Sensitivity: 1 ns to 10 μs, depending on delay range
GENERAL Operating Temperature: In order for the 3570A to meet the specifications listed in Table 1-1, the operating temperature must be within the range of +20°C to +30°C. The instrument can be operated where the ambient temperature is within the range of 0°C to +20°C or +30°C to +55°C with degraded accuracy. Thermal Cutout: The 3570A is equipped with a thermal switch which automatically removes line voltage when internal temperature exceeds +75°C (operating temperature approximately +60°C). Storage Temperature: -40°C to +75°C Power Requirements: 100 V, 120 V, 220 V or 240 V - 10% + 5%, 48 Hz to 66 Hz, 230 VA max. Dimensions: - Height (including feet): 140.6 mm (5 17/32 in.) - Overall length: 542.9 mm (21 3/8 in.) - Width: 425 mm (16 3/4 in.) - Width (including mounting strips): 483 mm (19 in.)	Offset Feature (Options 002, 003): The 3570A Offset feature permits entry of digital offsets from the front panel or by remote control. Amplitude, phase and delay readings can be offset. Offset Entry: Front Panel: Pressing the respective ENTER OFFSET pushbutton enters the present amplitude, phase or delay reading into memory, providing a zero reference when ABSOLUTE/RELATIVE switch is set to RELATIVE (offset) position. Remote Control: Offsets can be entered remotely by applying an ASCII coded Amplitude or Phase/Delay ENTER OFFSET instruction (same as pressing ENTER OFFSET pushbutton in local) or by a numerical data entry within the range of -199.99 to +199.99. Limit Test Feature (Option 002, 003): The 3570A Limit Test feature permits a pair of digital test limits (upper and lower) to be entered into memory by remote control. The test limits can apply to amplitude or phase/delay but not both simultaneously. If a reading is within the test limits, the "GO" annunciator illuminates; if a reading is above the upper limit or below the lower limit, the "HI" or "LO" annunciator illuminates.
OPTIONS 75-Ohm (Options 001, 003): Channel A and Channel B OUTPUTS have 75-ohm impedances; The 0 dBm MAX/REF INPUT VOLTAGE setting is referenced to 75 ohms and the rear panel INPUT impedance is 75 ohms. Group Delay Measurements (Options 002, 003): For group delay measurements, the 3570A solves the formula: $\tau_g = \frac{\Delta \phi}{360 \Delta f}$ Delay Modes: Swept (SWP): In the SWP mode, the 3570A measures phase and computes group delay at each sweep step, providing a total of 10, 100 or 1,000 delay readings depending on the number of steps selected on the 3330A/B Automatic Synthesizer. Single Frequency (CW): In the CW mode, the 3330A/B Automatic Synthesizer must be programmed to sweep in 10 frequency steps. The 3570A computes group delay based on phase readings taken at F_{min} and F_{max}. The single delay reading represents the mean slope of the phase vs. frequency curve.	Limit Sweep Modes: Limit Sweep Stop Mode: Any transition between "GO", "HI" and "LO" causes the 3330A/B Automatic Synthesizer to stop sweeping. The sweep can be restarted by pressing the LIMIT SWEEP RESTART pushbutton. The Limit Sweep Restart function cannot be programmed remotely. Limit Sweep No Stop Mode: The 3330A/B Automatic Synthesizer continues to sweep regardless of limit test transitions. Markers available at the Z AXIS OUTPUT can be used to intensify limit transition points on scope trace. Isolated Hewlett-Packard Interface Bus (Option 004): Instruments equipped with the Isolated HP-IB Two-Way option will transmit ASCII coded amplitude, phase and delay measurement data in a 7-bit parallel, word serial format. In addition, the remote input/output lines are isolated from signal (frame) ground. DC Isolation: ± 250 Vdc AC Isolation: 30 dB to 1 MHz

Table 1-3. 3570A Options.

3570A Option (Factory Installed)	Description
001	75 - ohm outputs, 0 dBm Max/Ref Input Voltage setting calibrated to 75 ohms
002	Group delay, offset and limit test (50 - ohm outputs)
003	Group delay, offset and limit test (75 - ohm outputs)
004*	Isolated Hewlett-Packard Interface Bus

*Field installation kit -hp- 11176A

Table 1-4. Accessories Supplied.

Item	Qty	-hp- Part No.
RF Input Cable	1 ea.	11172B (50 Ω) 11172C (75 Ω)
Multi-Unit Cable	1 ea.	11236B
Accessory Kit	1 ea.	03570-66501
Includes the following:		
PC Board Extender (25 pin)	1 ea.	03570-66501
PC Board Extender (dual)	1 ea.	03570-66502
PC Board Extender (6 pin)	1 ea.	03570-66503
PC Board Extender (16 pin)	2 ea.	5060-004B
Coax Cable - 50 ohm	2 ea.	8120-1839
Fuse: 1.5A Normal Blow	1 ea.	2110-0043

Table 1-5. Accessories Available.

-hp- Model	Description
11171A*	Front Panel Kit Includes the following: (2) 12" Double Shielded Cables (BNC to BNC) (2) 24" Double Shielded Cables (BNC to BNC) (1) 48" Double Shielded Cable (BNC to BNC) (2) 50 - Ohm Feed-Thru Terminations (1) Screwdriver
5060-8740	Rack Mount Kit
11170A	12" Double Shielded Cable (BNC to BNC)
11170B	24" Double Shielded Cable (BNC to BNC)
11170C	48" Double Shielded Cable (BNC to BNC)
11170D	48" Double Shielded Cable (BNC to BNC) (For 75 Ω System)
11048C	50 - Ohm Feed-Thru Termination
11094B	75 - Ohm Feed-Thru Termination
11095A	600 - Ohm Feed-Thru Termination
1201A/B	Variable Persistence Oscilloscope
3260A	Marked Card Programmer
10004B	Voltage Divider Probe
1120A	Active Probe

* For 75 - ohm systems order -hp- 11171B

Table 1-6. Option Cross Reference.

3570A Option	3040A Option	3041A Option	3042A Option
001	101	DNA	101
002	102	100	102
003	103	101	103
004	104	102	STD

SECTION II

INSTALLATION AND INTERFACE

2-1. INTRODUCTION.

2-2. This section contains information and instructions necessary for installing and shipping and interfacing the Model 3570A Network Analyzer. Included are initial inspection procedures, power and grounding requirements, environmental information, installation instructions, an interconnection procedure and instructions for repackaging for shipment.

2-3. INITIAL INSPECTION.

2-4. This instrument was carefully inspected both mechanically and electrically before shipment. It should be free of marks or scratches and in perfect electrical order upon receipt. To confirm this, the instrument should be inspected for physical damage incurred in transit. If the instrument was damaged in transit, file a claim with the carrier. Check for supplied accessories (Table 1-4) and test the electrical performance of the instrument using the performance check procedures outlined in Section V. If there is damage or deficiency, see the warranty on the inside title page of this manual.

2-5. POWER REQUIREMENTS.

2-6. The Model 3570A can be operated from any power source supplying 100 V, 120 V, 220 V or 240 V (-10% $+5\%$), 48 Hz to 66 Hz. Power dissipation is 230 VA, maximum. Refer to Paragraph 3-155 (Section III) for Instrument Turn-On procedure.

2-7. Power Cords and Plugs.

2-8. Figure 2-1 illustrates the standard power plug configurations that are used throughout the United States and in

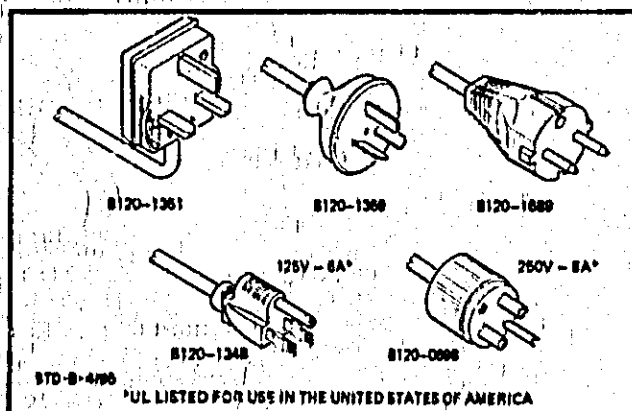


Figure 2-1. Power Cords.

other countries. The -hp- part number shown directly below each plug drawing is the part number for a 3570A power cord equipped with the appropriate plug. If the appropriate power cord is not included with the instrument, notify the nearest -hp- Sales and Service Office and a replacement cord will be provided.

2-9. GROUNDING REQUIREMENTS.

2-10. To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. The Model 3570A is equipped with a three conductor power cable which, when plugged into an appropriate receptacle, grounds the instrument. The offset pin on the power plug is the ground connection.

2-11. ENVIRONMENTAL REQUIREMENTS.

2-12. Cooling Fan.

2-13. The 3570A is equipped with a cooling fan mounted on the rear panel. The instrument should not be mounted in any manner that would obstruct the flow of air through the instrument. The filter for the cooling fan can be removed and cleaned by flushing with soapy water.

2-14. Thermal Cutout.

2-15. The 3570A is equipped with a thermal switch that will automatically remove line voltage when the internal temperature exceeds $+75^{\circ}\text{C}$ (the internal temperature will reach $+75^{\circ}\text{C}$ when the external temperature reaches approximately $+60^{\circ}\text{C}$). The switch will reset automatically when the instrument cools. If a thermal cutout occurs, check for fan stoppage, clogged fan ports or other conditions that could obstruct the flow of air through the instrument.

2-16. Operating and Storage Temperature.

2-17. In order for the 3570A to meet the specifications listed in Table 1-1, the operating temperature must be within the range of $+20^{\circ}\text{C}$ to $+30^{\circ}\text{C}$ ($+68^{\circ}\text{F}$ to $+86^{\circ}\text{F}$). The instrument can be operated where the ambient temperature is within the range of 0°C to $+55^{\circ}\text{C}$ ($+32^{\circ}\text{F}$ to $+131^{\circ}\text{F}$) with degraded accuracy. The storage temperature range is from -40°C to $+70^{\circ}\text{C}$ (-40°F to $+158^{\circ}\text{F}$).

2-18. INSTALLATION.**2-19. Mounting.**

2-20. As part of the 3040A Network Analyzer System, the 3570A is shipped with plastic feet and tilt stand in place, ready for use as a bench instrument. The plastic feet are shaped so that the 3570A can be mounted on top of another Hewlett-Packard instrument. If desired, the 3570A can be rack mounted using the Rack Mounting Kit Option 908 (-hp- 5060-8740). Installation instructions are included with the kit. The rack mount for the Model 3570A is an EIA standard width of 19 inches. As part of the 3041A or 3042A Network Analyzer System, the 3570A is shipped installed in an instrument rack.

2-21. Interconnection Procedure.

2-22. To interconnect the 3570A to the Synthesizer, proceed as follows:

a. Connect the OUTPUT (or ALT OUTPUT $\bigcirc$) of the Synthesizer to the rear panel INPUT $\bigcirc$ of the 3570A. Use the -hp- 11172B RF Input Cable supplied with the instrument.

b. Connect the 20 - 33 MHz OUTPUT $\square$ of the Synthesizer to the 20 - 33 MHz INPUT $\square$ of the 3570A. Use a 24" double-shielded cable equipped with standard BNC connectors (-hp- 11170B Cable Assembly supplied with instrument).

c. Connect the 1 MHz OUTPUT Δ of the Synthesizer to the 1 MHz INPUT Δ of the 3570A. Use a 48" double-shielded cable equipped with standard BNC connectors.

d. For remote control applications and/or swept measurements, connect the -hp- 11236B Multi-Unit Cable between the Synthesizer REMOTE CONTROL connector and the 3570A REMOTE CONTROL connector.

2-23. Interfacing.

2-24. The following paragraphs briefly describe the configurations used to interface the 3570A and the Synthesizer to the -hp- Model 3260A Marked Card Programmer and the -hp- 10631 (A, B or C) HP-IB. Refer to the 3040A, 3041A or 3042A System Interface Manual (or operating note) for further interfacing information. Section III in this manual contains a complete description of the 3570A remote control lines along with basic programming information.

2-25. For remote control applications using the HP-IB structure, the 3570A and the Synthesizer can be interconnected using either the -hp- 11236B Multi-Unit Cable or the -hp- 10631 (A, B or C) HP-IB. Two -hp- 11235A Adapters are required for interconnections using the HP-IB. For

swept measurements (including group delay) using the -hp- Model 3330A or 3330B Automatic Synthesizer, the 3570A and the Synthesizer must be interconnected with the -hp- 11236B Multi-Unit Cable (supplied with system). The 11236B cable contains control lines that are used for exclusive digital communication between the two instruments. These lines are not part of the HP-IB (see Paragraph 3-194).

2-26. To control the 3570A and the Synthesizer using the Model 3260A Marked Card Programmer or the HP-IB, connect the -hp- 11236B Multi-Unit Cable between the Synthesizer REMOTE CONTROL connector and the 3570A REMOTE CONTROL connector. Connect the 3260A Marked Card Programmer or the HP-IB cable to either of the two-way connectors on the 11236B cable using an -hp- 11235A Adapter.

2-27. REPACKAGING FOR SHIPMENT.

2-28. The following paragraphs contain a general guide for repackaging the instrument for shipment. Refer to Paragraph 2-31 if the original container is to be used; 2-32 if it is not. If you have any questions, contact the nearest -hp- Sales and Service Office (See Appendix B for office locations).

NOTE

If the instrument is to be shipped to Hewlett-Packard for service, or repair, attach a tag to the instrument identifying the owner and indicating the service or repair to be accomplished. Include the model number and full serial number of the instrument. In any correspondence, identify the instrument by model number and full serial number.

2-29. Place instrument in original container with appropriate packing material and seal well with strong tape or metal bands.

2-30. If original container is not to be used, proceed as follows:

a. Wrap instrument in heavy paper or plastic before placing in an inner container.

b. Place packing material around all sides of instrument and protect panel face with cardboard strips.

c. Place the instrument and the inner container in a heavy carton or wooden box and seal with strong tape or metal bands.

d. Mark shipping container "DELICATE INSTRUMENT", "FRAGILE", etc.

SECTION III OPERATING INSTRUCTIONS

3-1. INTRODUCTION.

3-2. This section contains complete operating instructions for the Model 3570A Network Analyzer. Included is a brief description of the instrument, a description of controls, general operating information, basic operating procedures and remote programming data.

3-3. ABOUT THE NETWORK ANALYZER.

3-4. The 3570A Network Analyzer is a subsystem component of the -hp- 3040A, 3041A and 3042A Network Analyzer Systems. In this capacity, it operates in conjunction with any of four -hp- Frequency Synthesizers: the 3320A, 3320B, 3330A or 3330B. The 3570A tracks the frequency of the synthesizer and is therefore totally dependent on the synthesizer for its reference, tracking and stimulus signals.

3-5. The 3570A is basically a narrow-band gain/phase meter that is automatically tuned to (tracks) the frequency of a signal source (3320A/B or 3330A/B). The source supplies the stimulus for the network or networks under test and the 3570A measures the response.

3-6. The 3570A is designed to characterize passive and active two-port linear networks that operate in the 50 Hz to 13 MHz frequency range. It has two identical measurement channels and can be used for measuring the absolute transfer functions of networks or for comparing two networks. Specifically, it will measure two basic parameters: Amplitude (gain or loss) and Phase. The 3570A Options 002 and 003, when combined with a 3330A/B Automatic Synthesizer, will also measure group delay.

3-7. Programmability.

3-8. The 3570A is equipped for remote control of all front panel functions, ranges and settings (except LINE and Limit Sweep Restart). It will recognize an internally preset "listen" address and accept 7-bit parallel, word serial ASCII coded instructions. It can be controlled directly from an -hp- 3260A Marked Card Programmer or most TTL tape readers. With proper interfacing, it can also be controlled by a data modem, teletype tape cassette, -hp- calculator or computer.

3-9. Operating Features.

3-10. The major operating features of the 3570A are outlined in Table 3-1.

3-11. How It Works.

3-12. Section IV contains a Simplified Block Diagram Description of the 3570A. A basic understanding of the analog section will be helpful when operating the instrument.

3-13. CONTROLS, CONNECTORS AND INDICATORS.

3-14. Figures 3-1 and 3-2 illustrate and describe the function of all front and rear panel controls, connectors and indicators. The description of each item is keyed to the drawing within the figure.

3-15. GENERAL OPERATING INFORMATION.

3-16. Inputs From the Synthesizer.

3-17. The 3570A is designed to operate in conjunction with an -hp- Model 3320A/B or 3330A/B Frequency Synthesizer. In order for the 3570A to operate properly, it must receive three primary inputs from the Synthesizer:

- a. 50 Hz to 13 MHz Signal Input.
- b. 20 MHz to 33 MHz Tracking Input.
- c. 1 MHz Reference Input.

For remote control applications and/or swept measurements the 3570A and the Synthesizer must also be interconnected with the -hp- 11236B Multi-Unit Cable supplied with the Network Analyzer System. Refer to the -hp- 3040A, 3041A, or 3042A, Systems Interface Manual for details concerning this connection.

3-18. Signal Input (Refer to Figure 3-3). The 50 Hz to 13 MHz signal from the OUTPUT (or ALT OUTPUT $\bigcirc$) of the Synthesizer connects to the rear panel INPUT $\bigcirc$ of the 3570A (Item 27, Figure 3-2). In the 3570A, the signal is divided by an active power splitter and applied to the A and B OUTPUT connectors on the 3570A front panel.

3-19. The INPUT $\bigcirc$ connector on the rear panel of the 3570A is double-shielded (Triaxial) and will not accept a standard BNC connector. The proper mating connector is provided on the -hp- 11172B RF Input Cable supplied with the instrument. This cable is double-shielded to ensure proper grounding between the two instruments.

3-20. Note that the impedance of the 3570A INPUT $\bigcirc$ is either 50 ohms (Standard) or 75 ohms (Options 001/003) and must match the output impedance of your Synthesizer. Do not terminate the output of the Synthesizer when making this connection.

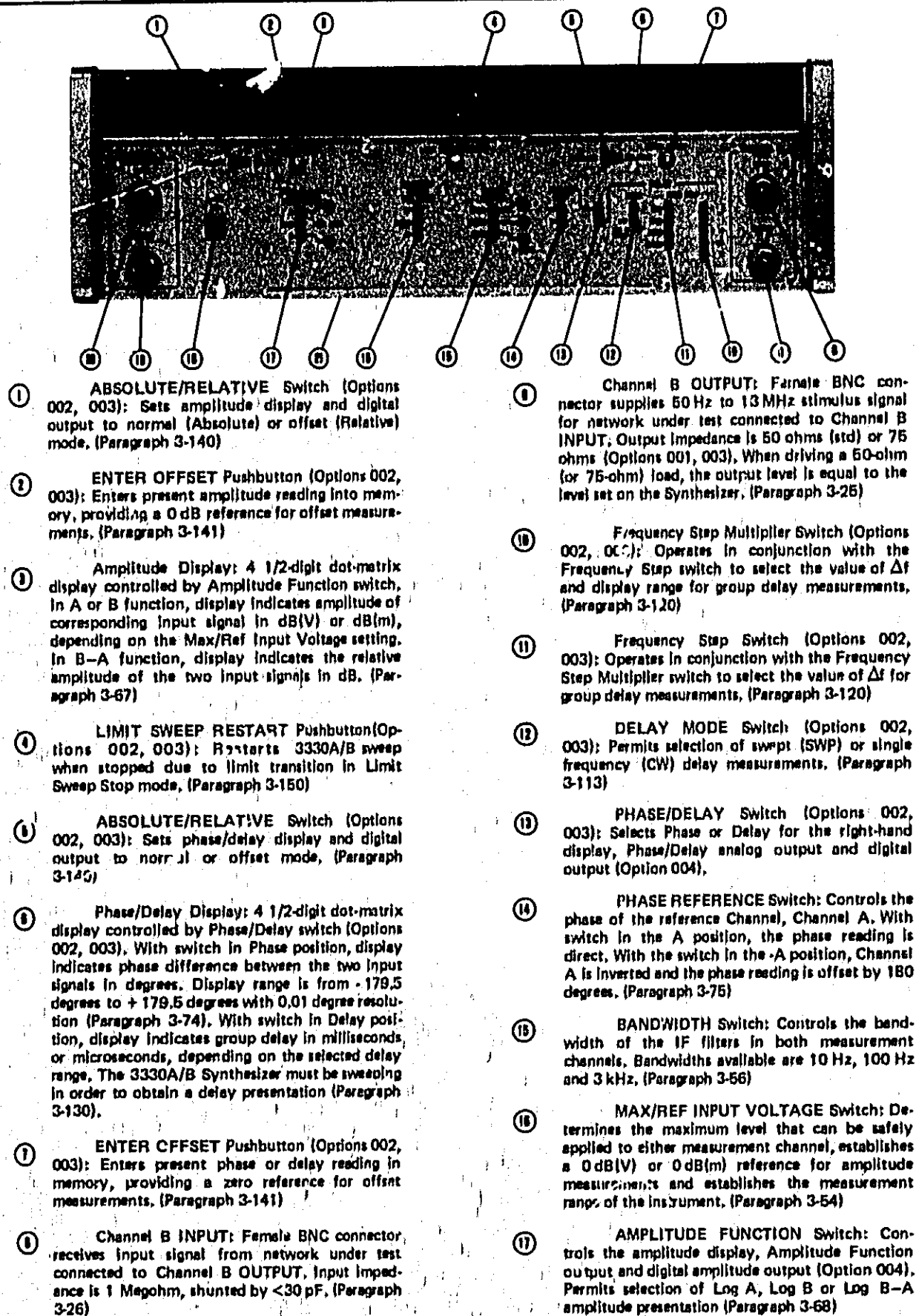


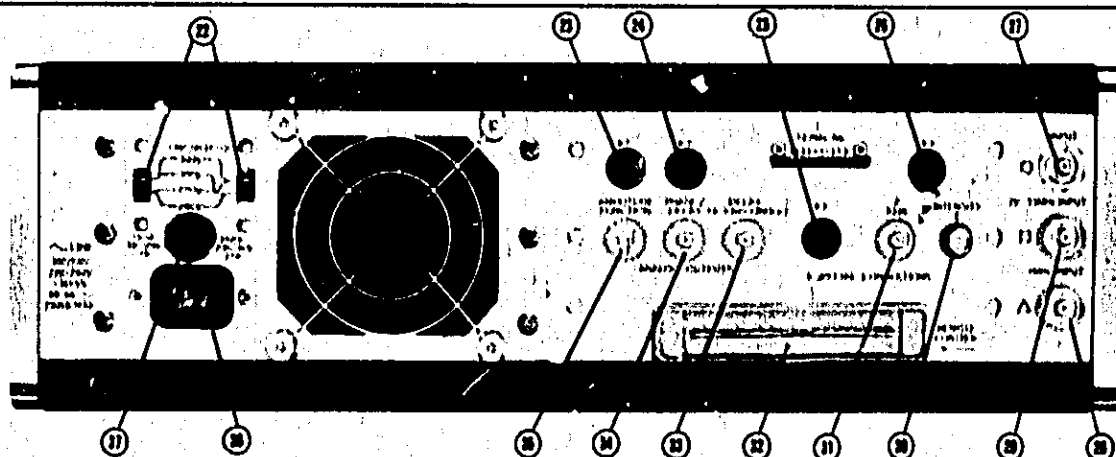
Figure 3-1. Front Panel.

Figure 3-1. Front Panel (Cont'd).

- (16) LINE Switch: Applies line voltage to the instrument when set to the ON position.
- (18) Channel A OUTPUT: Female BNC connector supplies reference signal or stimulus signal for reference network. Output impedance is 50 ohms (std) or 75 ohms (Options 001, 003). When driving a 50-ohm (or 75-ohm) load, the output level is equal to the level set on the Synthesizer. (Paragraph 3-25)

- (20) Channel A INPUT: Female BNC connector receives reference input signal. Can be connected to terminated Channel A OUTPUT or to output of reference network connected to the Channel A OUTPUT. Input impedance is 1 Megohm, shunted by <30 pF. (Paragraph 3-26)

- (21) Pullout Instruction Card: Provides condensed operating information.



- (2) Line Selector Switches: Select one of four line voltage settings: 100 V, 120 V, 220 V or 240 V. Line voltage must be within -10% to +5% of selected line voltage setting (Paragraph 3-153)

- (3) Auxiliary
- (4) Auxiliary
- (5) Auxiliary
- (6) Auxiliary

- (7) INPUT Connector: Triaxial connector mates with hp-11172A RF Input Cable connected to OUTPUT or ALT OUTPUT of Synthesizer. (Paragraph 3-18)

- (8) 1 MHz INPUT Connector: Female BNC connector receives 1 MHz Reference Input from 1 MHz OUTPUT of Synthesizer. (Paragraph 3-22)

- (9) 20-33 MHz INPUT Connector: Female BNC connector receives 20 MHz to 33 MHz Tracking Input from 20-33 MHz OUTPUT of Synthesizer. (Paragraph 3-21)

- (10) INTENSITY control: Sets the intensity of Z Axis markers available at Z AXIS OUTPUT (Paragraph 3-81)

- (11) Z AXIS OUTPUT Connector: Female BNC connector supplies markers which, when applied to the Z Axis Input of an oscilloscope, will intensify the scope trace at eleven equally spaced intervals, representing 1, 10 or 100 sweep steps. By changing the position of a jumper on A33, the markers can be set to intensify only the 5th, 50th or 500th sweep step, representing center amplitude or center frequency. When the optional Limit Test feature is used, markers are generated only at the limit

transition points. (Paragraph 3-87)

- (12) REMOTE CONTROL Connector: 36-pin male PC connector accepts 7-bit parallel, word serial ASCII coded instructions, provides control lines for digital communication between the 3570A and the Synthesizer and in instruments equipped with the Isolated Hewlett-Packard Interface Bus Two-Way Option (Option 004), outputs ASCII coded measurement data. (Paragraph 3-176)

- (13) DELAY (X-Y RECORDER) OUTPUT (Options 002, 003 only): Supplies dc voltage proportional to group delay in Swept Delay mode. Output voltage ranges from 0 V to ± 10 Vdc for 0 to 2,000 counts of delay. This output is controlled by a sample and hold circuit which retains the previous reading if the present reading exceeds 2,000 counts. (Paragraph 3-85)

- (14) PHASE/DELAY OUTPUT: Female BNC connector supplies dc voltage proportional to Phase (in Phase or CW Delay mode) or dc voltage proportional to group delay in Swept Delay mode. Output voltage ranges from 0 V to ± 9 Vdc for 0 to ± 180 degrees of phase or from 0 V to ± 10 Vdc for 0 to 2,000 counts of delay. (Paragraph 3-82)

- (15) AMPLITUDE FUNCTION OUTPUT: Female BNC connector supplies dc voltage proportional to amplitude as controlled by the Amplitude Function switch. Output voltage ranges from 0 V to ± 10 Vdc for 0 dB to ± 100 dB (± 0.1 V/dB). (Paragraph 3-81)

- (16) Power Input Receptacle: Accepts power cord supplied with instrument.

- (17) Fuse Holder: Contains line fuse: 3A, 250 V normal blo for 80 V to 130 V operation, 1.5 A, 259 V normal blo for 198 V to 252 V operation.

Figure 3-2. Rear Panel.

Table 3-1. Operating Features.

Feature	Paragraph
Two Digital Displays 1. Amplitude: 4 1/2 digits with 0.01 dB resolution. 2. Phase: 4 1/2 digits with 0.01 degree resolution.	3-65
Dual Measurement Channels (A and B) 1. Input Impedance: 1 M Ω , < 30 pF.	3-23 3-32
Separate A and B Outputs (supply reference and stimulus signals) 1. Output Impedance 50 ohms (standard), 75 ohms (Options 001, 003).	3-25 3-30
100 dB Dynamic Range (200 Hz to 13 MHz)	3-54
120 dB Measurement Range (1 μ Vrms to 1 Vrms)	3-67
Selectable Bandwidths: 10 Hz, 100 Hz and 3 kHz	3-56
Amplitude Measurements 1. Select one of three Amplitude Functions: A, B or B - A. 2. In A or B function, 3570A measures logarithmic amplitude of A or B input signal in dB(V) or dB(m). Range is from 0 dBV to +100 dBV (1 Vrms or 0.1 Vrms = 0 dBV) or from 0 dBm to +100 dBm 50 ohms (standard) 75 ohms (Options 001, 003).	3-67
Phase Measurements 1. Range: 359 degrees from -179.5 degrees to +179.5 degrees. 2. Phase Reference: A or -A.	3-74
Analog Outputs	3-79
Z Axis (Marker) Output	3-87
Complete Remote Control Capability	3-172
Optional Features: Group Delay Measurements (Options 002, 003)	3-110
Offset Measurements (Options 002, 003)	3-138
Limit Test Capability (Options 002, 003)	3-145
Isolated General Purpose Interface Bus (Option 004)	3-235

3-21. Tracking Input. The 20 MHz to 33 MHz tracking signal from the 20 - 33 MHz OUTPUT $\square$ of the Synthesizer is applied to the 20 - 33 MHz INPUT $\square$ of the 3570A (Item 29, Figure 3-2). In the 3570A, this signal is mixed with a 19.9 MHz reference to produce a 100 kHz to 13.1 MHz local oscillator signal. When making the Tracking Input connection, use one of the -hp- 11170B Cable Assemblies supplied with the instrument.

3-22. Reference Input. The signal from the 1 MHz OUTPUT Δ of the Synthesizer is applied to the 1 MHz INPUT Δ of the 3570A (Item 28, Figure 3-2). This signal is used as a reference to maintain the frequency stability of the Network Analyzer. The Reference Input connection should be made using one of the -hp- 11170B Cable Assemblies supplied with the instrument.

3-23. Input Connections.

3-24. The 3570A has two identical measurement channels: Channel A and Channel B. Channel A is the Reference Channel and Channel B is the Test Channel. Each channel has one output and one input.

3-25. A and B Outputs. The 50 Hz to 13 MHz output from the Synthesizer is applied to the rear panel INPUT $\square$ of the 3570A. From there, the signal is applied to an active power splitter (Figure 3-4) where it is divided and amplified to produce two output signals that are equal in amplitude and in phase. These signals are applied to the Channel A and Channel B OUTPUT connectors on the 3570A front panel. The A Output signal serves as a reference while the B Output signal serves as a stimulus for the network under test.

3-26. Reference and Test Inputs. Most Network Analyzer applications are based on relative measurements where the signals at the input and output (ports) of a network are compared to determine how the network behaves as a signal processor. The two basic parameters measured are gain (or loss) and phase. Both gain and phase measurements require two input signals: a Reference Input and a Test Input.

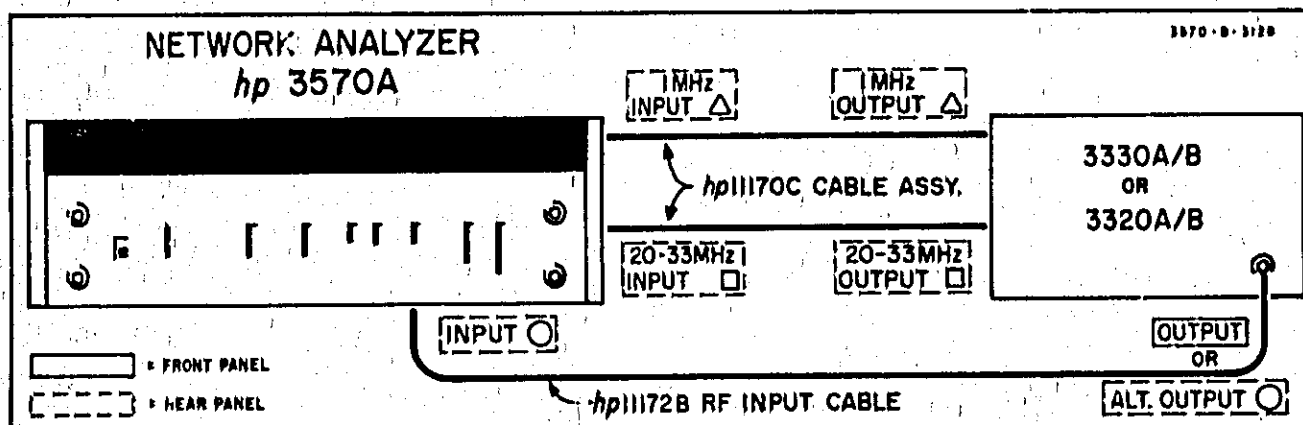


Figure 3-3. Interconnection Diagram.

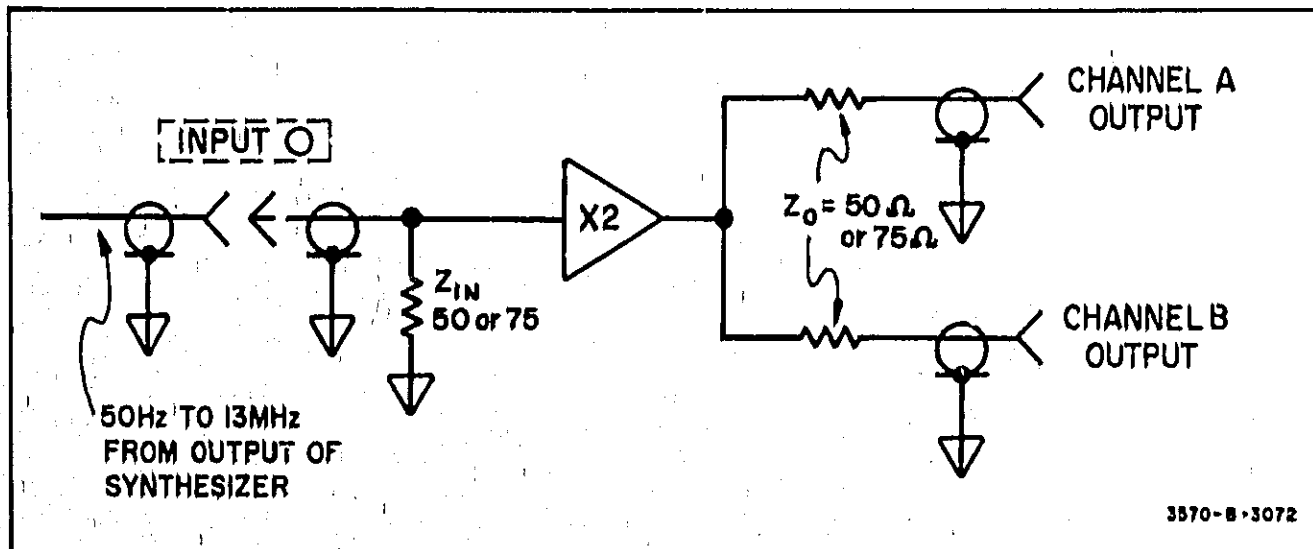


Figure 3-4. Active Power Splitter.

3-27. For basic gain/phase measurements, the Reference Input is obtained by connecting the Channel A Output to the A Input. The Test Input is obtained by inserting the network to be tested between the Channel B Output and the Channel B Input. Since the signals at the A and B outputs are identical, the signal applied to Channel A represents the input to the network while the signal applied to Channel B is the output of the network. By comparing these two signals, the 3570A measures the gain or loss and phase shift introduced by the network. When the frequency is swept over the band of interest with amplitude and phase displayed on a scope, the result is a complete picture or "data model" representing the amplitude and phase response of the transfer function in the frequency domain.

3-28. For production testing, it is often convenient to compare a newly manufactured network to a production standard. The 3570A, being a dual channel instrument lends itself well to this application.

3-29. When comparing two networks, the standard network is connected between the A Output and the A Input to obtain the reference. The network to be tested is then connected between the B Output and the B Input. In this case, the 3570A compares the output signals of the two networks and any differences between the networks are reflected as deviations from 0 dB (B - A amplitude) or 0 degrees (phase). When the frequency is swept over the band of interest with the relative amplitude and phase displayed on a scope, differences between the networks appear as deviations from a straight line on the scope trace. The straight-line reference allows the operator to quickly observe excessive deviations and perform any adjustments required to match the test network to the production standard.

3-30. Output Impedances. Figure 3-5 shows an equivalent circuit for the A and B Outputs. The circuit consists of a "zero impedance" source in series with a 50 or 75 ohm resistor which determines the output impedance. The

standard Model 3570A has 50 - ohm outputs while 3570A Options 001 and 003 have 75 - ohm outputs.

3-31. Output Levels. When the A or B Output is driving a 50 or 75 ohm load, the output level is equal to the level set on the Synthesizer. For example, if the Synthesizer is set for an output of 0 dBm, the level at the A or B Output is also 0 dBm. When an output is driving a load other than 50 or 75 ohms, the output level will differ from that of the Synthesizer. The open-circuit voltage at the A and B Outputs is twice the voltage at the output of the Synthesizer (See Figure 3-4).



THE A AND B OUTPUTS ARE DIRECT (dc) COUPLED AND MUST NOT BE SUBJECTED TO EXTERNAL VOLTAGES GREATER THAN ± 6 Vdc.

3-32. Input Impedances. Both measurement channels have an input impedance of 1 M Ω shunted by < 30 pF (28 pF nominal). This high input impedance has a minimum loading effect on the input signal and allows the 3570A to be used for characterizing networks having output imped-

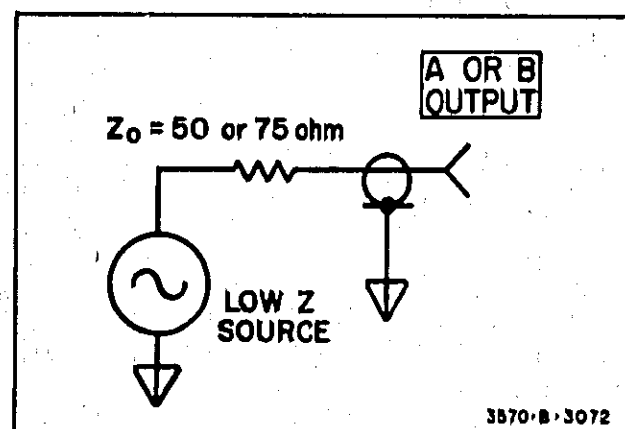


Figure 3-5. Equivalent Output Circuit.

ances other than 50 or 75 ohms. The $1\text{ M}\Omega < 30\text{ pF}$ inputs further permit the use of $10\text{ M}\Omega$, 10 pF Voltage Divider Probes (hp-10004B) which can be used to extend the measurement range or to minimize shunt capacitance.

3-33. Figure 3-6 shows the equivalent circuit for the A and B Inputs. The resistor, R_{in} represents the $1\text{ M}\Omega$ input resistance; the capacitor, C_s represents the 28 pF shunt capacitance. Figure 3-7 shows the input impedance, Z_t as a function of frequency. At low frequencies, the reactance of C_s is very high, making Z_t nearly equal to R_{in} . As frequency increases, the decreasing reactance of C_s becomes more and more significant, causing Z_t to decrease. At high frequencies, R_{in} is no longer significant and Z_t is slightly less than the reactance of C_s (approximately 500 ohms at 13 MHz).

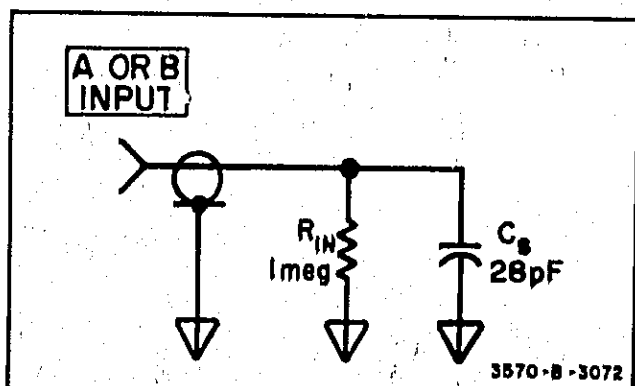


Figure 3-6. Equivalent Input Circuit.

3-34. If a network connected to the A or B Input has a relatively low output impedance such as 50 or 75 ohms and is terminated in a 50-ohm or 75-ohm load, the 3570A input will not load the signal or introduce a significant amount of phase shift. If the network has a high output impedance or is not terminated in its characteristic impedance, the 3570A input can introduce losses and phase shifts that degrade the accuracy of measurements. These losses and phase shifts can be minimized by using high-impedance input probes and by making the impedances in both channels equal so that relative amplitude readings and phase readings will not be affected.

3-35. **Input Configurations.** Figures 3-8A through 3-8F illustrate and describe the basic input configurations for various types of measurements. The illustrations show the 3570A as having 50-ohm outputs, however the same basic configurations apply to instruments having 75-ohm outputs.

3-36. **Input Cable Requirements.** Input connections should be made using shielded cables equipped with standard BNC connectors. Double-shielded cables (available from hp-) are recommended. Table 3-2 is a list of recommended hp- cables. When making input connections, observe the following guidelines:

- a. Keep input cables as short as possible.
- b. Make the total cable length in each channel equal. This is particularly important when measuring phase (or delay) at high frequencies.

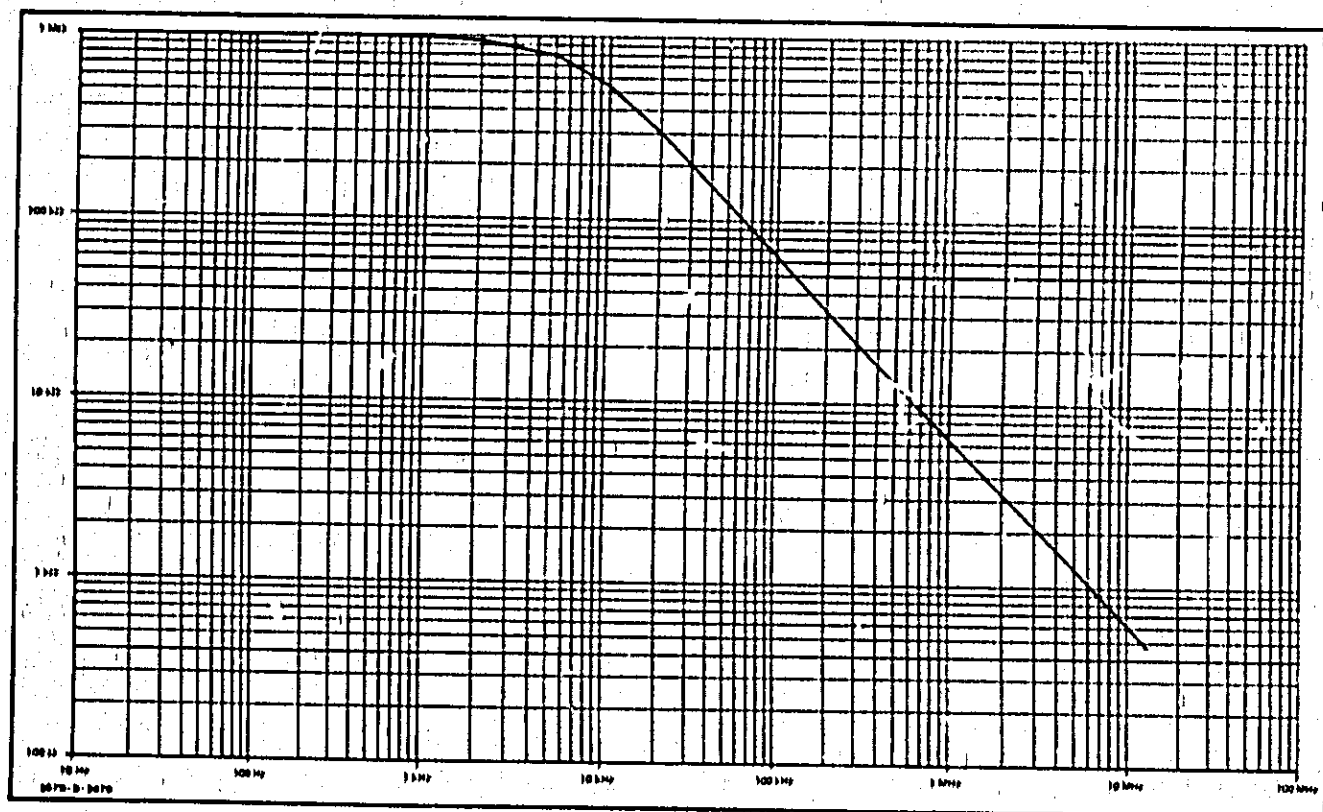


Figure 3-7. Graph: Z_t vs. Frequency.

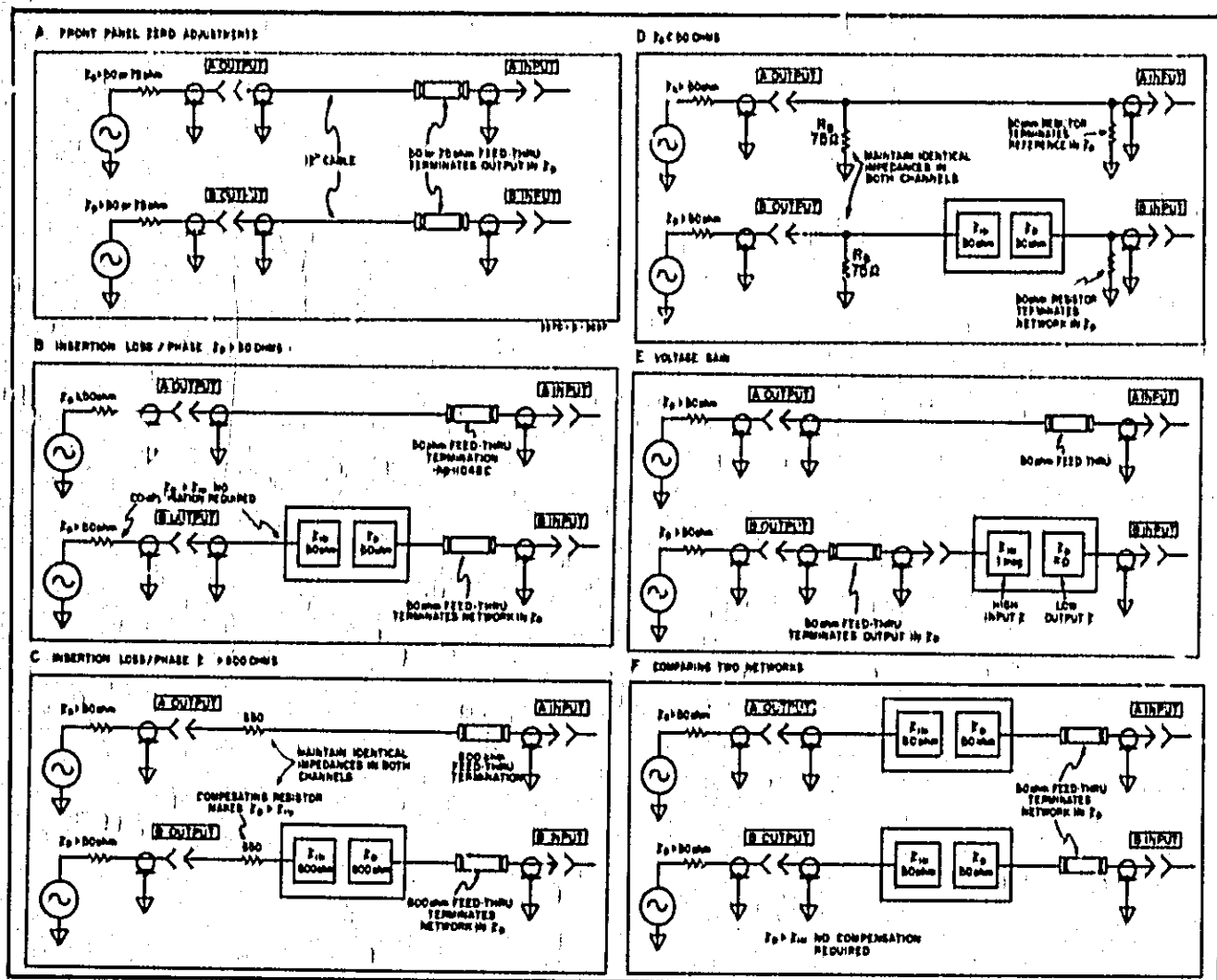


Figure 3-8. (A - F) Input Configurations.

c. When impedance terminations are required, use shielded terminations equipped with suitable RF connectors. Place terminations at the end of the transmission line.

3-37. Impedance Matching. In most measurement applications, the network under test must be driven and terminated in its characteristic impedance. If the characteristic impedance of the network matches the 50 ohm (or 75 ohm) output impedance of the 3570A, the network can be connected directly to the A or B Output as shown in Figure 3-8B.

3-38. If the characteristic impedance of the network is greater than the output impedance of the 3570A, a compensating resistor can be added in series with the A or B Output to obtain the required output impedance. For example, if the input impedance of the network is 600 ohms, a 550 ohm resistor can be added in series with a 50-ohm output to obtain 600 ohms. This is shown in Figure 3-8C. Note that the Reference Input shown in Figure 3-8C also has a compensating resistor and a 600 ohm termination to maintain identical impedances in both channels.

3-39. If the characteristic impedance of the network is lower than the output impedance of the 3570A, connect a shunting resistor across the 3570A Output to obtain the required output impedance. The value of shunt resistance can be calculated using the following formula:

$$R_s = \frac{Z \cdot R_0}{R_0 - Z}$$

Where: R_s = shunt resistance
 R_0 = 50 - ohm or 75 - ohm output impedance
 Z = required output impedance

3-40. When driving an impedance less than 50 ohms (or 75 ohms), a certain amount of insertion loss will be encountered. The amount of loss depends on the type of impedance matching network used and on the various impedance ratios. Whenever a loss is encountered, an equal loss should be introduced in the Reference Channel so that the Reference Input accurately represents the input of the network. This can be accomplished by placing identical

shunt resistances and identical terminations in both channels as shown in Figure 3-8D.

3-41. Accessories. Table 3-3 is a list of impedance terminations available from Hewlett-Packard. A 50 ohm impedance matching network is shown in Figure 3-2 (Section V).

Table 3-2. Recommended Cables.

Length	Type	hp-Part No.
12"	BNC - BNC Double-Shield	11170A
24"	BNC - BNC Double-Shield	11170B
48"	BNC - BNC Double-Shield	11170

Table 3-3. Impedance Terminations.

Termination	hp-Part No.
50 - Ohm Feed-Thru	11048C
75 - Ohm Feed-Thru	11094B
600 - Ohm Feed-Thru	11095A

3-42. High Impedance Probes. The 1 M Ω , < 30 pF inputs of the 3570A are compatible with several hp high impedance scope probes. Two recommended probes are:

- The hp-Model 10004B Voltage Divider Probe.
- The hp-Model 1120A Active Probe.

3-43. The hp-Model 10004B Voltage Divider Probe has a probe-tip impedance of 10 M Ω , shunted by 10 pF and a 10:1 division ratio. The hp-Model 1120A Active Probe has a probe-tip impedance of 100 Ω , shunted by < 3 pF and a 1:1 ratio. The accessory 10:1 divider (hp-10241A) supplied with the 1120A increases the impedance to 1 M Ω , shunted by < 1 pF. The bandwidths of both probes are more than adequate for use with the 3570A. It should be noted that the 1120A Active Probe Power requires an external power source such as the hp-1122A Probe Power Supply. In addition, the 1120A has an output impedance of 50 ohms and must be terminated in a 50 - ohm load. Use a 50 - ohm Feed-Thru Termination such as the hp-Model 11048C.

3-44. When using input probes observe the following guidelines:

- Most scope probes have capacitive compensating adjustments. These adjustments should be performed using the procedure outlined in Paragraph 3-15B.
- Use identical probes in both channels. Avoid using a probe on one channel and a direct input on the other channel.

3-8

3-45. Minimizing Ground Loops. In the design of the 3570A, extra care has been taken to control internal ground currents that could degrade the accuracy of low-level measurements. Due to its wide dynamic range and high sensitivity, however, the 3570A can be affected by external ground currents or "ground loops" which are normally caused by poor grounding. To minimize ground loops, observe the following guidelines:

- Keep output cables as short as possible.
- Use double-shielded cables to ensure good ground connections.
- Connect the 3570A, the synthesizer and any auxiliary equipment to the same power bus.

3-46. Input Constraints.

3-47. The maximum voltage that can be safely applied to the inputs is determined by the MAX/REF INPUT VOLTAGE (Range) setting. Maximum input levels are:

Range	Maximum Voltage
1 V	1 Vrms (0 dBV)
0 dBm	0.2236 Vrms (50 ohms) 0.274 Vrms (75 ohms)
0.1 V	0.1 Vrms (0 dBV)

3-48. Exceeding the maximum input level will cause the overload indicator (Aol/Bol) to illuminate. The input circuitry in the 3570A is protected and can withstand overloads up to 15 Vrms or $\pm$ 50 Vdc. Overloads greater than this can damage the instrument.

3-49. To avoid overloads when operating the 3570A, observe the following guidelines:

- When making input connections, set the Synthesizer to a low level such as -80 dBm.
- When characterizing networks that exhibit gain, set the input level to the network low enough that the maximum level out of the network will not exceed the MAX/REF INPUT setting.
- When using the 3320B or 3330B Synthesizer, ensure that the LEVELING control is set according to the output frequency.
- Exercise caution when using the B-A Amplitude Function or the optional Offset function where amplitude readings do not reveal the actual amplitude of the input signals.

3-50. DC Isolation.

3-51. The A and B Outputs are direct-coupled and must not be subjected to external voltages greater than $\pm$ 6 Vdc. Exceeding this limit can cause damage to the Power Splitter circuitry.

3-52. The A and B Inputs are capacitor coupled to provide dc isolation. The maximum dc voltage that can be safely applied to the inputs is ± 50 Vdc. Exceeding this limit can cause breakdown of the coupling capacitors, resulting in damage to the Input Amplifier circuitry. Note that when using 10:1 Voltage divider probes, the maximum dc voltage that can be safely applied to the probes is still ± 50 Vdc.

3-53. The 3570A cannot be operated in a "floating" condition. All input and output commons are connected directly to outer chassis (frame) ground which connects to earth ground through the offset pin on the power-cord connector.

NOTE

In the 3570A Option 004, the remote inputs and outputs are isolated from frame ground. In these instruments the digital ground can be floated ± 250 Vdc above frame ground.

3-54. MAX/REF INPUT Setting.

3-55. The MAX/REF INPUT VOLTAGE setting establishes three things:

- The maximum level that can be applied to either input channel without overloading the instrument (Paragraph 3-47).
- A 0 dBm (50 or 75 ohms) or 0 dBV reference for amplitude measurements (Paragraph 3-67).
- The highest and lowest input levels the instrument can measure within its 100 dB dynamic range:

Range	Lower Limit	Upper Limit
1 V	10 μ Vrms	1 Vrms (0 dBV)
0 dBm	-100 dBm	0 dBm (50 or 75 ohms)
0.1 V	1 μ Vrms	0.1 Vrms (0 dBV)

3-56. Bandwidth Setting.

3-57. The 3570A uses a heterodyne technique where the 50 Hz to 13 MHz input signal is converted to a 100 kHz intermediate frequency. The 100 kHz IF signal is fed through a series of bandpass filters which reject unwanted frequencies. The BANDWIDTH setting (10 Hz, 100 Hz or 3 kHz) determines the bandwidth of the IF filters and thus, the selectivity of the instrument.

3-58. For operating purposes, each measurement channel can be pictured as having a bandpass filter that is automatically tuned to the frequency of the input signal. The instrument responds only to signals passing through the filters and thereby rejects most of the unwanted signals present at the inputs. The BANDWIDTH setting determines the width of the filter skirts at the -3 dB points above and below the input frequency:

$$\text{Lower 3 dB Point} = f_0 - \frac{BW}{2} \quad \text{Upper 3 dB Point} = f_0 + \frac{BW}{2}$$

Where: f_0 = Input frequency (50 Hz to 13 MHz)

BW = Bandwidth setting (10 Hz, 100 Hz or 3 kHz)

3-59. **Bandwidth Selection.** In order for the 3570A to meet the specifications listed in Table 1-1, the proper Bandwidth must be selected. The frequency and amplitude of the input signal may limit the choice of bandwidths due to local oscillator feedthru. The chart in Table 1-1 labeled "Dynamic Range" gives these bandwidth restrictions as a function of frequency and amplitude. To use the chart, locate the amplitude and frequency of interest and note the acceptable bandwidth(s) for that particular intersection. When in doubt, use the narrower bandwidth. The shaded region labeled "> 600 ohm load only" carries an additional restriction due to source induced ground loops. Large currents present in test leads may produce errors when measuring low level signals. Using system impedances of 600 ohms or greater reduces these currents to an acceptable level.

3-60. Outside of the low frequency and amplitude limit there is no criterion that dictates which bandwidth to use. There are, however, some definite considerations that make one bandwidth a better choice than others for certain measurement applications. These considerations are discussed in the following paragraphs.

3-61. **Rejection.** Due to its wide dynamic range, the 3570A will respond to input levels well below 1 μ Vrms on all three input ranges. This means that in terms of sensitivity, it is capable of responding to noise and other extraneous signals that can create errors, particularly in low-level measurements. Accuracy is, therefore, dependent on the ability of the instrument to reject these undesirables and respond only to the fundamental frequency of the input signal. Rejection depends on the amount of selectivity provided by the Bandwidth setting. The narrower bandwidths provide the greatest selectivity and thus, the greatest rejection of unwanted signals.

3-62. Typically, the rejection characteristics for each Bandwidth setting can be defined by a shape factor of 20:1. This means that the filter skirts are 20 times wider at the -60 dB points than at the -3 dB points. On the 10 Hz Bandwidth, for example, the -3 dB points are 10 Hz apart and the -60 dB points are 20 x 10 or 200 Hz apart. The filter is, in effect, centered on the input frequency f_0 and exhibits 3 dB of rejection to signals that are ± 5 Hz away from f_0 and 60 dB of rejection to signals that are ± 100 Hz away from f_0 . The rejection characteristics for the 100 Hz and 3 kHz Bandwidths are obtained in the same manner and are listed in Table 3-4.

3-63. **Noise Rejection.** Noise is sometimes described as the "universal enemy" in electrical measurements. Nyquist's Noise Equation reveals two important things about noise that apply to the 3570A:

$$E_n = (4 kTB R)^{1/2} \quad \text{Where } E_n = \text{noise level}; k = \text{Boltzmann's constant}; T = \text{temperature (}^\circ\text{K)};$$

$$B = \text{bandwidth (Hz)}; R = \text{input resistance.}$$

Table 3-4. Rejection Characteristics.

Bandwidth	3 dB Rejection	60 dB Rejection
10 Hz	$f_o \pm 5 \text{ Hz}$	$f_o \pm 100 \text{ Hz}$
100 Hz	$f_o \pm 50 \text{ Hz}$	$f_o \pm 1 \text{ kHz}$
3 kHz	$f_o \pm 1.5 \text{ kHz}$	$f_o \pm 30 \text{ kHz}$

a. Noise is proportional to the square root of bandwidth. The 10 Hz and 100 Hz Bandwidth settings will provide the greatest noise rejection.

b. Noise level is proportional to the square root of input resistance. The 3570A has a high (1 M Ω) input resistance which means that noise sensitivity is largely dependent on the output resistance of the network under test. For example, a network that is embedded between a 50-ohm source and a 50-ohm load will exhibit greater noise immunity than a network having a high output resistance. When testing networks having high output resistance, it is advisable to use the 10 Hz or 100 Hz Bandwidth setting to ensure good noise rejection.

3-64. Response Time. Generally, when making swept frequency measurements it is desirable to have good rejection and, at the same time, sweep as rapidly as possible. This involves a definite trade off since the narrower bandwidths provide good rejection but increase the dynamic response time. As the bandwidth is narrowed, the instrument takes longer to respond to electrical changes taking place at the inputs. This means that slower sweep rates are required on the 10 Hz and 100 Hz Bandwidths than on the 3 kHz Bandwidth. Methods for determining the maximum sweep rate are outlined in Paragraph 3-105.

3-65. Display Indications.

3-66. The 3570A is equipped with two digital displays. The left-hand display indicates amplitude and the right-hand display indicates phase or group delay (Options 002, 003). The following paragraphs describe the amplitude and phase presentations and the front panel controls associated with them. Group delay is discussed in Paragraph 3-110.

3-67. Amplitude Display. The amplitude display is controlled by the AMPLITUDE FUNCTION switch which permits selection of A, B or B-A presentation. With the switch in the A or B position, the amplitude display indicates the amplitude of the corresponding input signal in dB(m) or dB(V), depending on the MAX/REF INPUT VOLTAGE setting. With the Reference set to 1 V or 0.1 V the amplitude readings (in dB) represent dB(V) where 0 dBV is equal to 1 Vrms or 0.1 Vrms, respectively. The measurement range is from 0 dBV (1 V or 0.1 V) to -100 dBV (10 μ V or 1 μ V) with 0.01 dB display resolution. With the Reference set to 0 dBm, the A and B amplitude readings (in dB) represent dBm/50 or 75 ohms. The measurement range is from 0 dBm to -100 dBm with 0.01 dB display resolution. Note that "dBm" readings are

3-10

valid only when the input signal is driving a 50 or 75 ohm load. In all other cases, the "dBm" readings only represent input voltage and must be converted to volts or dBV.

3-68. With the AMPLITUDE FUNCTION switch in the B-A position, the amplitude display indicates the relative amplitude (difference between) the two input signals in dB. The range for relative amplitude measurements is from -100 dB to +100 dB with 0.01 dB display resolution. Relative amplitude readings are displayed with respect to Channel A which is the Reference Channel. A negative reading indicates that the signal applied to Channel B is lower in amplitude than the signal applied to Channel A. A positive reading indicates that the signal applied to Channel B is greater in amplitude than the signal applied to Channel A.

3-69. The B-A function is provided for measuring the gain or loss of a network or for comparing two networks. The B-A readings are independent of source variations and are not affected by the "absolute" accuracy of the source. Measurement accuracy depends on having two identical measurement channels with good amplitude linearity.

3-70. Converting Readings. The A and B amplitude readings in dB(V) or dB(m) can be converted to rms volts using the graph shown in Figure 3-9.

3-71. Absolute Amplitude Accuracy. The absolute amplitude accuracy of the 3570A depends on three things:

- The basic calibration of the instrument (Zero Adjustments).
- Amplitude linearity and frequency response as specified in Table 1-1.
- The spectral purity of the input signal.

3-72. Calibration. Amplitude Zero adjustments are provided on the front panel to allow the operator to compensate for amplitude variations that occur due to environmental changes or changes in Bandwidth. These adjustments are normally performed with the A and B Outputs (terminated in 50 or 75 ohms) connected to the A and B Inputs with the synthesizer set for an output of 0 dBm (Paragraph 3-154). The amplitude accuracy depends on the accuracy of the input signals when the adjustments are performed. This relates to the basic accuracy of the synthesizer and the transfer accuracy at the A and B Outputs (see Table 1-2).

3-73. Spectral Purity of Input. The 3570A, being a narrow band instrument, responds only to the fundamental frequency of the input signal. If an applied signal contains harmonics or spurious the 3570A will not accurately reveal the true-rms amplitude of the composite signal. For this reason, measurements should be confined to linear networks or networks that produce insignificant amounts of distortion. This also applies to phase measurements since signals

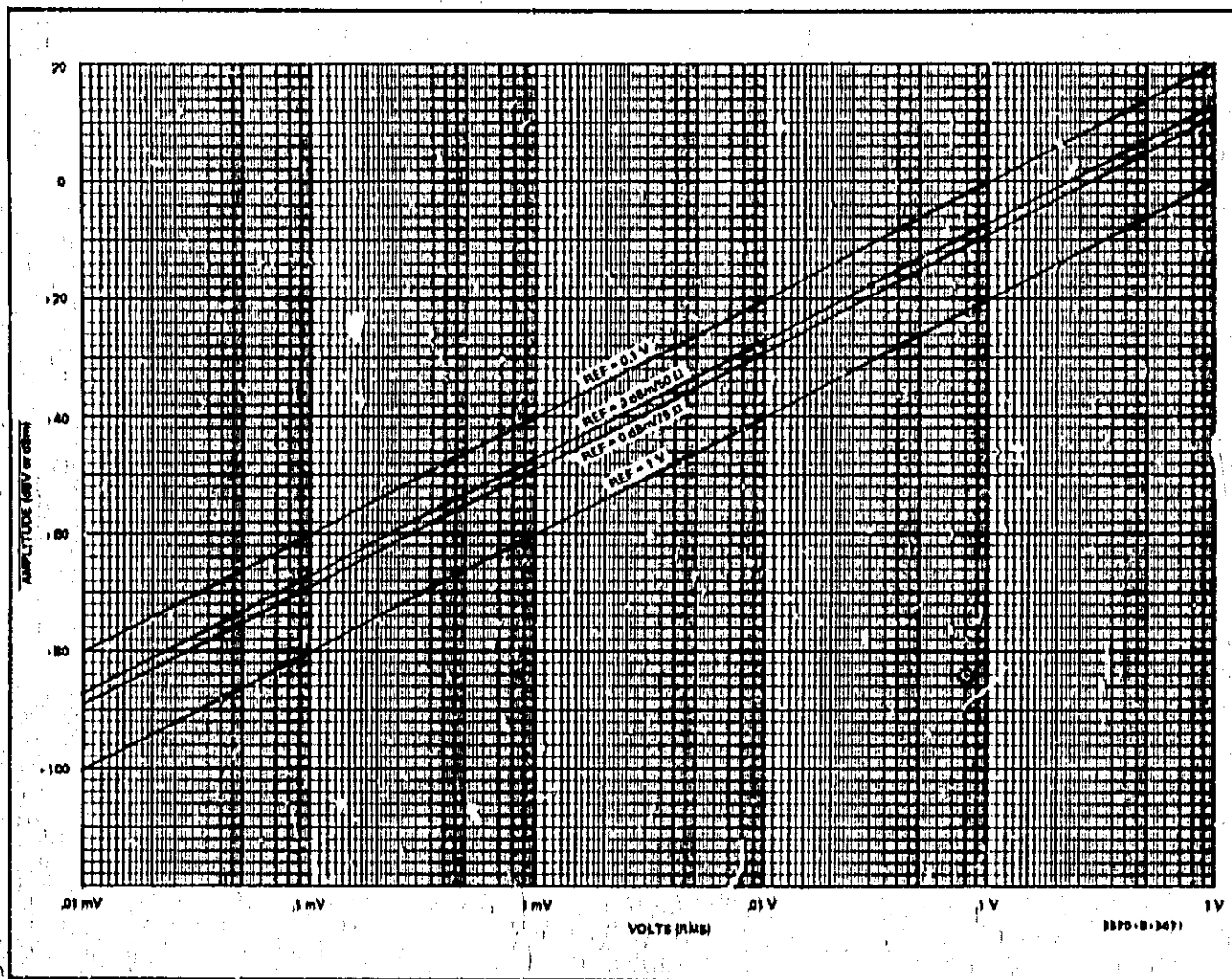


Figure 3-9. Graph: dBV and dBm to Volts Conversion.

containing out-of-phase harmonics will be shifted with respect to the fundamental frequency.

3-74. Phase Display. The phase display indicates the phase difference between the two input signals in degrees. The display range for phase measurements is from -179.5 degrees to +179.5 degrees with 0.01 degree resolution.

3-75. Phase Reference. Phase readings are displayed with respect to Channel A which is the Reference Channel. A negative phase reading means that B lags A; a positive reading means that B leads A.

3-76. With the PHASE REFERENCE set to +A, the phase reading indicates the actual phase difference between the two input signals. With the PHASE REFERENCE set to -A, Channel A is inverted and the phase reading is offset by 180 degrees. There are two practical reasons for changing the PHASE REFERENCE setting:

- To avoid the "Indeterminate region" about 180 degrees.
- To avoid the discontinuity that occurs when the phase detector recycles at 180 degrees.

3-77. Indeterminate Region. The 3570A phase measurement range encompasses 359 degrees, from -179.5 degrees to +179.5 degrees (Figure 3-10). This leaves a ± 0.5 degree gap about 180 degrees where the phase detector cannot respond properly. This gap is called the "indeterminate region". For phase measurements near 180 degrees, the indeterminate region can be avoided by changing the Phase Reference from A to -A. This shifts the phase of the Reference signal (A) by 180 degrees, placing the phase reading in the 0 degree region.

3-78. Discontinuity. When making phase vs. frequency plots using the Phase analog output, a discontinuity will occur in the plot when the phase reading suddenly changes from -180 degrees to +180 degrees or vice-versa. In many cases, however, the discontinuity can be avoided by carefully selecting the Phase Reference setting. For example, consider the case where the two signals are initially at -5 degrees and as frequency is varied the phase difference increases in a negative direction. With the Phase Reference set to +A, the plot begins at -5 degrees and continues in a negative direction until the phase reading reaches approximately -180 degrees. At this time, the phase reading automatically jumps to +180 degrees and

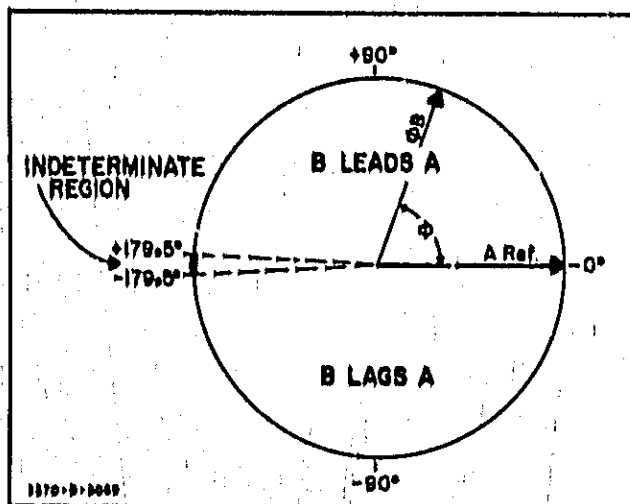


Figure 3-10. Phase Indeterminate Region.

again goes more negative (less positive) with frequency. The result is a discontinuous plot. In this case, a continuous plot could be obtained by initially setting the Phase Reference to -A. The plot would begin at +175 degrees and continue in a negative direction through 0 degrees and down as far as -179.5 degrees. This extends the continuous range by nearly 180 degrees.

3-78. Analog Outputs.

3-80. The Standard Model 3570A and options not equipped for group delay measurements have two analog outputs on the rear panel. These outputs are labeled AMPLITUDE FUNCTION and PHASE/DELAY. The PHASE/DELAY output applies only to phase. On instruments equipped for group delay measurements (Options 002, 003), the PHASE/DELAY analog output is used for both phase and delay. These instruments have one additional analog output labeled DELAY (X-Y RECORDER).

3-81. Amplitude Function Output. The AMPLITUDE FUNCTION output is controlled by the Amplitude Function setting (A, B or B-A). When A or B is selected, the output supplies a dc voltage that is logarithmically proportional to the amplitude of the A or B input signal. When B-A is selected, the output supplies a dc voltage that is logarithmically proportional to the relative amplitude of the two input signals. On all three functions, the output level is 0.1 Vdc per dB. On the A and B functions, the output voltage ranges from 0 Vdc (0 dB) to -10 Vdc (-100 dB). On the B-A function, the output voltage ranges from -10 Vdc (-100 dB) to +10 Vdc (+100 dB).

NOTE

All of the 3570A analog outputs have 1 k Ω output resistances. In order to obtain the output voltages indicated, the load resistance connected to these outputs must be 1 M Ω or greater. Additional loading will not damage the instrument or degrade the linearity but it will reduce the output level by an amount proportional to the load resistance.

3-82. Phase Output. For phase measurements, the PHASE/DELAY analog output supplies a dc voltage proportional to the phase difference between the two input signals. The output level is 0.05 Vdc per degree, ranging from -9 Vdc (-180 degrees) to +9 Vdc (+180 degrees). Like the digital phase display, the phase analog output is controlled by the Phase Reference setting and is affected by the indeterminate region and change in polarity that occurs near ± 180 degrees.

3-83. Delay Output (Options 002, 003 only). In instruments equipped for group delay measurements, the PHASE/DELAY output is controlled by the PHASE/DELAY and SWP/CW switches. In the PHASE or CW Delay Mode, the output supplies a dc voltage proportional to phase as outlined in the preceding paragraph. In the SWP Delay Mode, the output supplies a dc voltage proportional to group delay. The output level ranges from 0 Vdc to ± 10 Vdc for 0 to 1,999 counts of delay (5 mV per count). Note that 1,999 counts (10 Vdc) can represent a delay reading of 19.99 ms, 1.999 ms, 19.99 μ s or 1.999 μ s, depending on the selected delay range.

3-84. When using the PHASE/DELAY output for delay vs. frequency recordings, a discontinuity will be encountered if the two phase readings used to compute group delay fall on opposite sides of the ± 180 degree point. This can be avoided by changing the Phase Reference or by using the DELAY (X-Y RECORDER) output described in the following paragraph.

3-85. Delay (X-Y Recorder) Output. The DELAY (X-Y RECORDER) output is designed specifically for delay vs. frequency measurements using an X-Y recorder or oscilloscope. In the SWP Delay Mode, the output is the same as that from the PHASE/DELAY output except an additional stage of buffering is present. No meaningful output is present in the PHASE or CW Delay Mode.

3-86. The DELAY (X-Y RECORDER) output is controlled by a sample and hold circuit which ensures that the delay reading is 2,000 counts or less before it allows the output level to change. If a delay reading exceeds 2,000 counts, the output level will remain as it was for the previous delay reading. This prevents the output from responding to large, erroneous delay readings that occur when the phase detector recycles at ± 180 degrees.

3-87. Z Axis Output

3-88. The following information applies only when the 3570A is operated with an hp-Model 3330A or 3330B Automatic Synthesizer and the two instruments are interconnected with the hp-11236B Multi-Unit Cable.

3-89. When the 3330A/B is sweeping, the 3570A Z AXIS OUTPUT (Item 31, Figure 3-2) supplies a synchronized pulse train which, when applied to the Z Axis Input of an oscilloscope, will unblank the scope trace at each sweep step and intensify the trace at eleven equally spaced

intervals. During swept frequency or swept amplitude measurements, the intensified points serve as markers, representing 1, 10 or 100 frequency or amplitude steps.

3-90. By changing the position of a jumper plug on the Address Recognition Assembly, A33, the Z Axis Output can be set to intensify only the center point, representing center frequency (F_c) or center amplitude. Instructions for changing the jumper position are outlined in Figure 3-11.

NOTE

When the optional Limit Test feature is used, markers are generated only at the limit transition points.

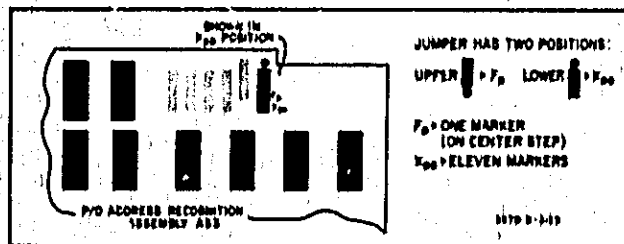


Figure 3-11. Marker Jumper.

3-91. Intensity Control. The INTENSITY control, located near the Z AXIS OUTPUT connector on the 3570A rear panel, sets the amplitude and period of the marker pulses. This control is used in conjunction with the scope intensity control to obtain the desired marker intensity.

CAUTION

EXCESSIVE MARKER INTENSITY WILL BURN THE SCOPE FACE. FOR MINIMUM INTENSITY, SET THE 3570A INTENSITY CONTROL FULLY COUNTERCLOCKWISE (FACING THE REAR PANEL). REFER TO THE INTENSITY ADJUSTMENT PROCEDURE OUTLINED IN PARAGRAPH 3-97.

3-92. Blanking and Unblanking. There are two types of pulses present at the Z Axis Output:

- Unblanking Pulses.
- Marker Pulses.

In the absence of an unblanking pulse or marker pulse, the output voltage is +10 Vdc. This will blank the scope trace.

3-93. Unblanking Pulses. When the 3330A/B is sweeping, unblanking pulses are generated at each sweep step (Figure 3-12). The unblanking pulses are negative going, with a peak amplitude of 0 volts. The pulse width is approximately 64 microseconds. When the 3330A/B is not connected or is not sweeping, an unblanking pulse is generated each time the 3570A samples. The repetition rate is approximately 4 per second when internal sampling is used. When applied to a scope, these pulses may unblank the scope trace causing it to flash at the sample rate.

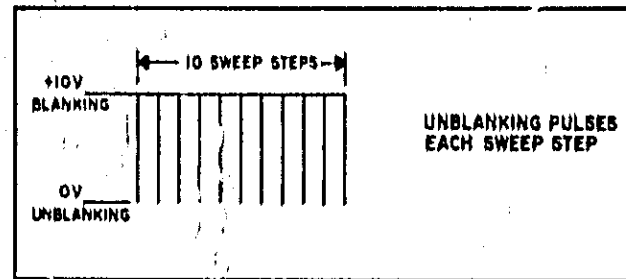


Figure 3-12. Unblanking Pulses.

3-94. Marker Pulses. When the jumper plug on A33 is set to the X00 position, marker pulses are generated every 1, 10 or 100 sweep steps, depending on the number of steps (10, 100 or 1000) selected on the 3330A/B. The peak amplitude of the marker pulses can be varied from 0 V (minimum intensity) to -7 V (maximum intensity) using the INTENSITY control. The INTENSITY control also varies the width of the marker pulses from approximately 100 μ sec at minimum intensity to 400 μ sec at maximum intensity.

3-95. During a 10 step sweep, the unblanking pulses and the marker pulses coincide at each sweep step and the output is as shown in Figure 3-13. Note that the scope trace will be blanked between each sweep step. During a 100 step

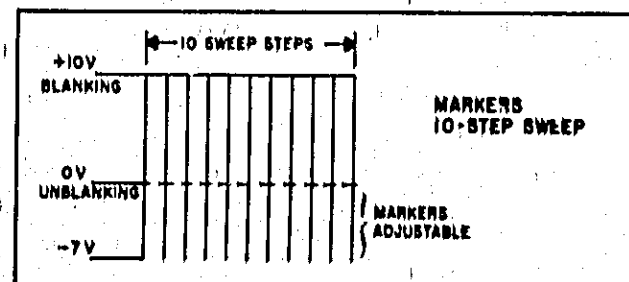


Figure 3-13. Markers (10 Step Sweep).

sweep, marker pulses are generated every ten sweep steps and nine unblanking pulses are generated between each marker pulse (Figure 3-14). On the scope trace, this will produce nine unintensified dots between each marker. During a 1000 step sweep, markers are generated every 100 sweep steps with 99 unblanking pulses in between. As in the 100 step sweep, the unblanking pulses will produce 99 unintensified dots between each marker.

3-96. When the jumper plug on A33 is set to the F_0 position, marker pulses are generated only on the center

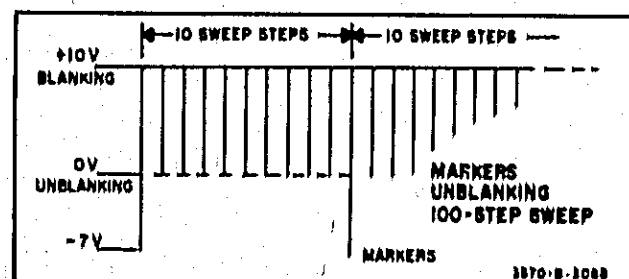


Figure 3-14. Markers (100 Step Sweep).

(5th, 50th or 500th) sweep step. This does not apply during limit tests where markers are generated at the limit transition points. Unblanking pulses are still generated at each sweep step.

3-97. Intensity Adjustment Procedure. To establish the required trace intensity and marker intensity, proceed as follows:

a. Set the scope for minimum intensity. Set the INTENSITY control on the 3570A fully counterclockwise (facing the rear panel).

b. Connect the SWEEP OUTPUT of the 3330A/B to the Horizontal Input of the scope.

c. Set the Horizontal Range (EXT.) on the scope to 1 V/div.

d. Connect the Z AXIS OUTPUT of the 3570A to the Z Axis Input of the scope.

e. Set the 3330A/B for a 100 step UP frequency sweep at 1 msec per step (step size is arbitrary).

f. Start the 3330A/B sweep by entering START CONT.

g. Adjust the scope controls for a 10 division trace of the desired intensity.

h. Adjust the 3570A INTENSITY control for the desired marker intensity.

3-98. Swept Frequency Measurements.

3-99. The primary purpose of network analysis is to fully describe the behavior of networks in the frequency domain. This is accomplished by measuring the amplitude and phase (or delay) response of a network as a function of frequency. One method for doing this is to manually vary the frequency and plot a response curve point-by-point on a graph. This method, however, is tedious, time consuming and often inaccurate since it is easy to skip over points that might reveal important characteristics of the network. A faster, more accurate method is to sweep the frequency over a band of interest and display the response curve on a scope or X-Y recording. Swept measurements provide a continual updating or "refreshing" of information, making it possible to observe any changes in the response characteristics of the network. This is of particular benefit since it allows the network to be adjusted while observing the results of the adjustment.

3-100. The 3570A. As a measuring instrument, the 3570A is fully capable of making swept frequency (or swept amplitude) measurements. The ability to make swept measurements, however, depends on the capabilities of the Frequency Synthesizer being used. The -hp- 3330A and 3330B Automatic Synthesizers have built-in sweep capability. The -hp- 3320A and 3320B Frequency Synthesizers do not have built-in sweep capability but can be swept by

remote control. Refer to the 3320A/B Operating and Service Manual for details.

3-101. The following paragraphs briefly describe swept frequency measurements in terms of the 3570A and the 3330A/B Automatic Synthesizer. The basic concepts, however, apply regardless of the method used to sweep the signal source.

NOTE

For swept measurements, the 3570A and the 3330A/B must be interconnected with the -hp- 11236B Multi-Unit Cable. If they are not interconnected, the 3570A may not sample fast enough to make a measurement at each frequency step. In addition, when the two instruments are interconnected, the 3570A samples at the end of each step period and the 3330A/B sweep is inhibited until the 3570A completes the measurement (Paragraph 3-201). This may, in some cases, cause the sweep rate to be slower than indicated by the 3330A/B TIME/STEP setting.

3-102. The Setup. In a typical swept measurement application, the Sweep Output of the 3330A/B (0 Vdc to +10 Vdc) is connected to the horizontal input of a scope or to the X input of an X-Y recorder. The horizontal range on the scope or X-Y recorder is then set to provide a calibrated X axis representing frequency. With a horizontal setting of 1 V/div, each horizontal division represents 1, 10 or 100 frequency steps, depending on the number of steps (10, 100 or 1000) set on the 3330A/B. If desired, the Z AXIS OUTPUT of the 3570A can be connected to the Z Axis Input of a scope to provide frequency markers (Paragraph 3-87).

NOTE

For a scope presentation, best results will be obtained using a Variable Persistence Scope such as the -hp- Model 1201A/B.

3-103. To complete the setup, the AMPLITUDE FUNCTION, PHASE or DELAY analog output on the 3570A is connected to the vertical input of the scope or the Y input of the X-Y recorder. The scope or X-Y recorder is then adjusted to provide a calibrated Y axis representing amplitude, phase or delay. For amplitude measurements, a vertical setting of 1 V/div will provide a display of 10 dB per division. This allows the entire 100 dB dynamic range to be displayed in 10 vertical divisions on a scope having a 10 x 10 graticule. For phase measurements, a vertical setting of 2 V/div will allow 360 degrees in 9 vertical divisions. For group delay measurements using the DELAY (X-Y RECORDER) output, a vertical setting of 1 V/div will allow 2,000 counts of delay to be displayed in ten vertical divisions.

3-104. The Sweep. A general procedure for starting the 3330A/B sweep is as follows:

a. Set the 3330A/B to the center frequency between F_{min} and F_{max} .

b. Enter the desired Frequency Step and select the number of steps. (A 100 step sweep will provide satisfactory results in most applications.)

c. Select the sweep rate using the TIME/STEP control (Paragraph 3-105).

d. Start the sweep by entering the START CONT or START SINGLE. When using a scope readout, a continuous sweep should be used. A single sweep may be preferable for X-Y recordings.

3-105. Sweep Rate. The maximum sweep rate for a given measurement depends on the bandwidth of the network under test and the BANDWIDTH setting on the 3570A. For narrower bandwidths, more time is required for the network or 3570A to respond to electrical changes taking place at the input. Narrower bandwidths, therefore, require slower sweep rates.

3-106. Disregarding the network or networks under test the approximate maximum sweep rate for each 3570A BANDWIDTH setting is listed in Table 3-5.

Table 3-5. Maximum Sweep Rates.

3570A Bandwidth	Rate (Hz/Sec)
10 Hz	50 Hz
100 Hz	5 kHz
3 kHz	4.5 MHz

3-107. The maximum sweep rate, if not limited by the 3570A Bandwidth, may be limited by the bandwidth of the network under test. For bandpass and low pass filters, a rough approximation of maximum sweep rate can be obtained using the following formula:

$$R_{\max} = \frac{BW^2}{2}$$

Where: $R_{\max}$ = maximum sweep rate in Hz/Sec.
BW = Bandwidth of network

This approximation is based on the characteristics of a Gaussian filter using an error factor of 1 %.

3-108. The following formula can be used to convert from Hz/sec to TIME/STEP:

$$T = \frac{S}{R}$$

Where: T = TIME/STEP in seconds
S = Step size in Hz
R = Sweep rate in Hz/sec

3-109. In practice, it is often difficult, if not impossible, to accurately predict the maximum sweep rate. For this reason, the simplest approach is to start with a slow sweep rate and, while observing the response curve, gradually increase the rate until the curve begins to change. When the curve begins to change, the sweep rate is too fast and should be reduced.

3-110. Group Delay Measurements (Options 002/003 only).

3-111. The 3570A (Option 002 or 003), when combined with an -hp- Model 3330A or 3330B Automatic Synthesizer, will measure group delay on a swept or single-frequency basis. In both cases the 3330A/B must be programmed to sweep and the two instruments must be interconnected with the -hp- 11236B Multi-Unit Cable.

3-112. The 3570A measures group delay by solving the formula:

$$\tau_g = \frac{\Delta\phi}{360\Delta f}$$

It solves the formula by first making phase measurements at two different frequencies, f_1 and f_2 . The digital phase readings (ϕ_1 and ϕ_2) are stored in memory and the difference ($\phi_1 - \phi_2$) is calculated to obtain $\Delta\phi$. The quantity $\Delta\phi$ is then divided by $360\Delta f$, ($\Delta f = f_2 - f_1$) to obtain a delay reading.

3-113. Delay Modes. Group delay measurements can be performed in one of two delay modes: Swept (SWP) or Single Frequency (CW). The desired delay mode can be selected from the front panel (DELAY MODE switch) or by remote control.

3-114. Swept Mode. For group delay measurements using the Swept Mode, the 3330A/B Automatic Synthesizer can be programmed to sweep in 10, 100 or 1000 frequency steps. At each frequency step, the 3570A makes a phase measurement and simultaneously computes group delay. This is illustrated in Figure 3-15.

3-115. In Figure 3-15, the frequency is swept between points F_1 and F_{11} (10 frequency steps). The first delay reading is actually computed at frequency F_2 where the present phase reading (ϕ_2) is subtracted from the previous phase reading (ϕ_1), yielding $\Delta\phi$. The quantity $\Delta\phi$ is then divided by 360 and the frequency step Δf , ($\Delta f = F_1 - F_2$) to obtain a delay reading. This sequence is repeated at each additional frequency through F_{11} , providing a total of ten delay readings.

3-116. The delay reading calculated at a given frequency actually applies to a point half way between that frequency and the preceding frequency. For example, the first delay reading calculated at F_2 actually applies to the center frequency between F_1 and F_2 . This is illustrated in Figure 3-16.

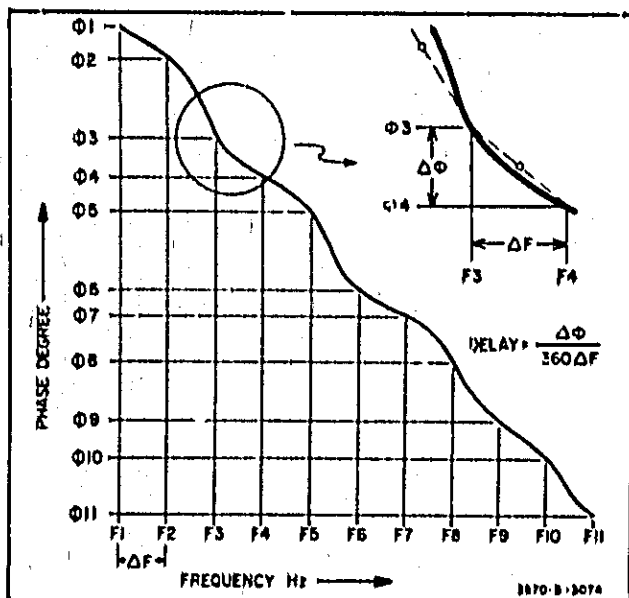


Figure 3-15. Swept Delay.

3-117. CW Mode. In the CW (single-frequency) Mode, the 3330A/B must be programmed to sweep in 10 frequency steps. The 3570A makes a phase measurement at F_{min} and again at F_{max} , 10 steps away (Figure 3-17). The phase difference, $\Delta\phi$, is then divided by Δf (frequency step $\times 10$) to obtain a delay reading. In this case, the single delay reading applies to the center frequency between F_{min} and F_{max} .

3-118. The Frequency Increment, Δf . For group delay measurements, the frequency increment, Δf must be selected by the operator or external controller. The selection can be made using the front panel FREQ STEP controls or by remotely entering an ASCII coded Frequency Step, followed by a Frequency Step Multiplier.

3-119. The 3570A offers twenty choices of Δf , ranging from 5 Hz to 200 kHz. The settings are arranged in decade multiples of 5 Hz, 10 Hz, 16.6 Hz and 20 Hz. Each Δf (FREQ STEP) setting represents a full scale delay range which establishes the sensitivity, resolution and display limits (see Table 3-6).

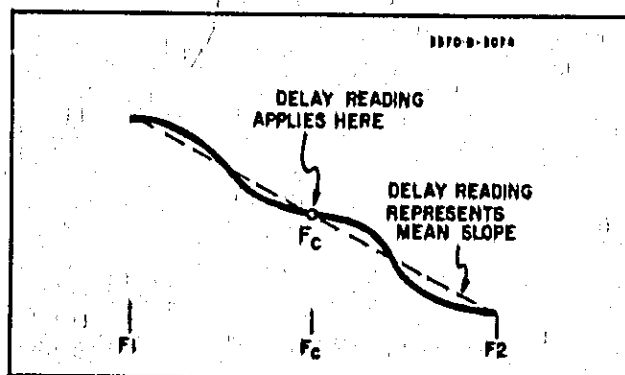


Figure 3-16. Average Delay.

3-120. FREQ STEP Controls. The 3570A is equipped with two FREQ STEP controls: a Frequency Step switch and a Frequency Step Multiplier switch. These switches do not, in any way, control the 3330A/B frequency or frequency step. Their only functions are to select the value of Δf and indicate the correct Frequency Step entry for the 3330A/B.

3-121. By observing the front panel Frequency Step Multiplier control, it can be noted that the multiplier markings are color coded white and blue to correspond with the DELAY MODE switch settings. The color coding is provided as a convenience feature to make the 3570A FREQ STEP setting match that of the 3330A/B in both delay modes. The frequency increment, Δf , is always determined by the white multipliers. The correct 3330A/B Frequency Step entry is indicated by the white multipliers in the SWP mode and by the blue multipliers in the CW mode.

EXAMPLE (SWP Mode): If the Frequency Step switch is set to 5 and the Frequency Step Multiplier switch is set to $X1/X0.1$, the Δf setting and the correct 3330A/B Frequency Step are both: $5 \times 1 = 5$ Hz as indicated by the white multiplier.

EXAMPLE (CW Mode): If the Frequency Step switch is set to 5 and the Frequency Step Multiplier switch is set to $X1/X0.1$, the value of Δf is again 5 Hz as indicated by the white multiplier. The correct 3330A/B Frequency Step, however is $5 \times 0.1 = 0.5$ Hz as indicated by the blue multiplier.

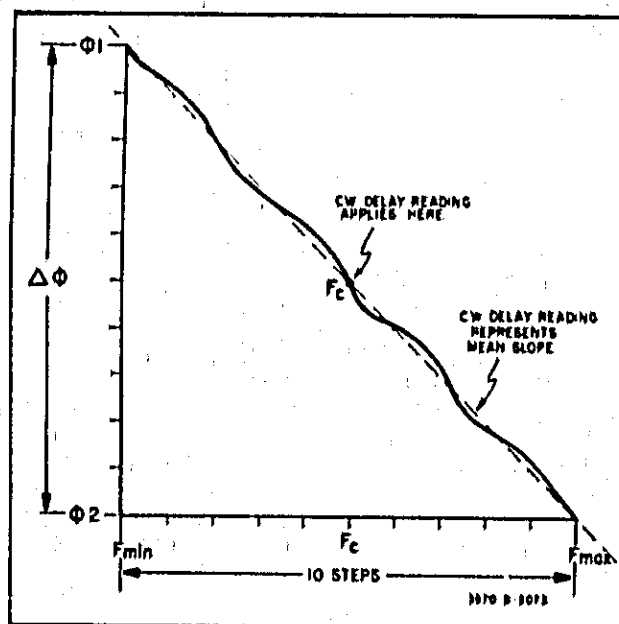


Figure 3-17. CW Delay.

Table 3-6. Delay Ranges.

FREQ. STEP	STEP MULTIPLIER	Δf SETTING	DISPLAY RANGE	MEASUREMENT SENSITIVITY	MEASUREMENT RESOLUTION
5	X1	5 Hz	0.01 msec to 199.99 msec	10 μ sec	200 msec
10	X1	10 Hz	0.01 msec to 199.99 msec	10 μ sec	100 msec
16.6	X1	16.6 Hz	0.01 msec to 199.99 msec	10 μ sec	60 msec
20	X1	20 Hz	0.01 msec to 199.99 msec	10 μ sec	50 msec
5	X10	50 Hz	0.001 msec to 19.999 msec	1 μ sec	20 msec
10	X10	100 Hz	0.001 msec to 19.999 msec	1 μ sec	10 msec
16.6	X10	166 Hz	0.001 msec to 19.999 msec	1 μ sec	6 msec
20	X10	200 Hz	0.001 msec to 19.999 msec	1 μ sec	5 msec
5	X100	500 Hz	0.0001 msec to 1.9999 msec	0.1 μ sec	2 msec
10	X100	1 kHz	0.0001 msec to 1.9999 msec	0.1 μ sec	1 msec
16.6	X100	1.66 kHz	0.0001 msec to 1.9999 msec	0.1 μ sec	0.6 msec
20	X100	2 kHz	0.0001 msec to 1.9999 msec	0.1 μ sec	0.5 msec
5	X1K	5 kHz	0.01 μ sec to 199.99 μ sec	10 nsec	200 μ sec
10	X1K	10 kHz	0.01 μ sec to 199.99 μ sec	10 nsec	100 μ sec
16.6	X1K	16.6 kHz	0.01 μ sec to 199.99 μ sec	10 nsec	60 μ sec
20	X1K	20 kHz	0.01 μ sec to 199.99 μ sec	10 nsec	50 μ sec
5	X10K	50 kHz	0.001 μ sec to 19.999 μ sec	1 nsec	20 μ sec
10	X10K	100 kHz	0.001 μ sec to 19.999 μ sec	1 nsec	10 μ sec
16.6	X10K	166 kHz	0.001 μ sec to 19.999 μ sec	1 nsec	6 μ sec
20	X10K	200 kHz	0.001 μ sec to 19.999 μ sec	1 nsec	5 μ sec

3-122. The Trade Off. The selection of Δf for group delay measurements involves a fundamental trade off between sensitivity and resolution. Sensitivity is the ability to measure gradual changes (small delay readings); resolution is the ability to measure rapid changes (large delay readings). The requirements for having good sensitivity and good resolution are conflicting: If a large value of Δf is used, sensitivity is good but resolution is poor. If a small value of Δf is used, resolution is good but sensitivity is poor. The operator must, therefore, select a value of Δf that will provide the best compromise for a given application.

3-123. Group delay, as defined by the equation

$$\tau_g = \frac{\Delta\phi}{360 \Delta f}$$

represents the slope of the phase curve at a given frequency. The slope, in turn, represents the *rate of change of phase with respect to frequency*. A steep slope indicates a rapid change while a gradual slope indicates a slow change. In a typical phase vs. frequency curve, both rapid and gradual changes will occur (Figure 3-18). In areas where the slope is gradual, a small change in frequency will produce a proportionally small change in phase. In areas where the slope is steep, a small change in frequency will produce a relatively large change in phase. Here is where the trade off occurs: If a small value of Δf is used, the change in phase produced by a gradual slope may be too small to be detected by the measuring instrument. This is *poor*

sensitivity. If, on the other hand, a large value of Δf is used, gradual changes will be detectable (good sensitivity) but rapid changes tend to be averaged out (Figure 3-19). This is *poor resolution*.

3-124. 3570A Delay Sensitivity. For operating purposes, delay sensitivity can be defined as the smallest delay the 3570A can measure for a given value of Δf . Maximum delay sensitivity is determined by two factors:

- The smallest change in phase ($\Delta\phi$) the 3570A can detect.
- The display range.

3-125. In the delay mode the smallest change in phase the 3570A can detect is 0.018 degrees. This differs from the

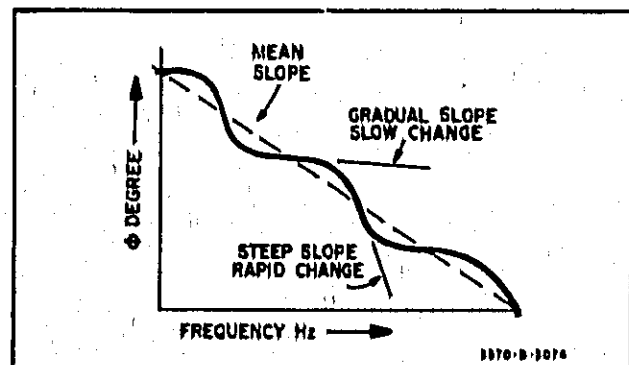
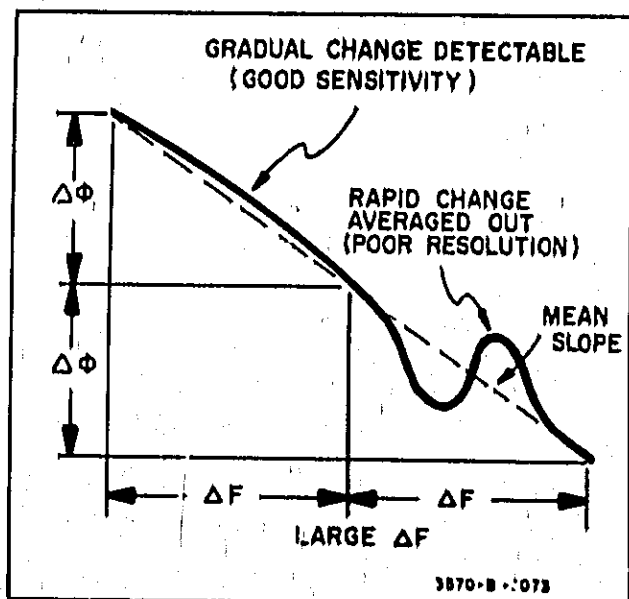


Figure 3-18. Rapid and Gradual Changes.

Figure 3-19. Large Δf .

0.01 degree phase display due to the analog prescaling used for delay measurements. The 0.018 degree phase sensitivity establishes the delay sensitivity when the selected Δf is 5 Hz or a decade multiple thereof; 50 Hz, 500 Hz, 5 kHz or 50 kHz. For all other values of Δf , delay sensitivity is limited by the display range.

3-126. The lower limit of the display range is determined by the Frequency Step Multiplier setting. It is not affected by the Frequency Step setting. The lower limit varies from 1 nanosecond on the X10K range to 10 microseconds on the X1 range (Table 3-6). For any given multiplier setting, the lower limit of the display range corresponds with a delay reading obtained using a Frequency Step of 5 (lowest step setting) and the minimum $\Delta\phi$ of 0.018 degrees. For example, on the X1 (lowest) multiplier setting the limit can be calculated using a Δf of 5 Hz (5 X1) and a $\Delta\phi$ of 0.018 degrees:

$$\frac{0.018}{360 \times 5} = 10 \text{ microseconds}$$

Similarly, on the X10K range the limit is:

$$\frac{0.018}{360 \times 50K} = 1 \text{ nanosecond}$$

3-127. Increasing the Frequency Step from 5 to 20 does not increase sensitivity in terms of the digital display. It does, however, provide greater accuracy when measuring gradual changes. Delay accuracy depends on the ability of the 3570A to accurately measure the change in phase, $\Delta\phi$. A large $\Delta\phi$ will be more accurate than a small $\Delta\phi$. For example, a small $\Delta\phi$ of 0.02 degrees is nearly meaningless due to the noise variations and ambiguity in the last digit of the phase reading. When measuring gradual changes where good sensitivity is required, increasing Δf by increasing the

Frequency Step setting will make $\Delta\phi$ larger, thereby improving the accuracy of the measurement.

3-128. 3570A Delay Resolution. Delay resolution, as opposed to sensitivity, can be defined as the largest delay the 3570A can measure for a given value of Δf . Unlike sensitivity, resolution is never limited by the display range. Resolution is limited only by Δf and the maximum $\Delta\phi$ the 3570A can measure (approximately 360 degrees). For any value of Δf , resolution can be calculated using the maximum $\Delta\phi$ of 360 degrees. For example, if Δf is 5 Hz, resolution is:

$$\frac{360}{360 \times 5} = \frac{1}{5} = 0.2 \text{ sec (199.99 ms)}$$

The resolution for each of the twenty Δf settings is listed in Table 3-6.

3-129. Guidelines for Selecting Δf . Due to the variables encountered in group delay measurements, it is often difficult to predict the optimum value of Δf . The following guidelines, however, will provide satisfactory results in most applications:

a. Using the graph shown in Figure 3-20, select a value of Δf that will produce a $\Delta\phi$ of 1 to 5 degrees for the smallest expected delay reading.

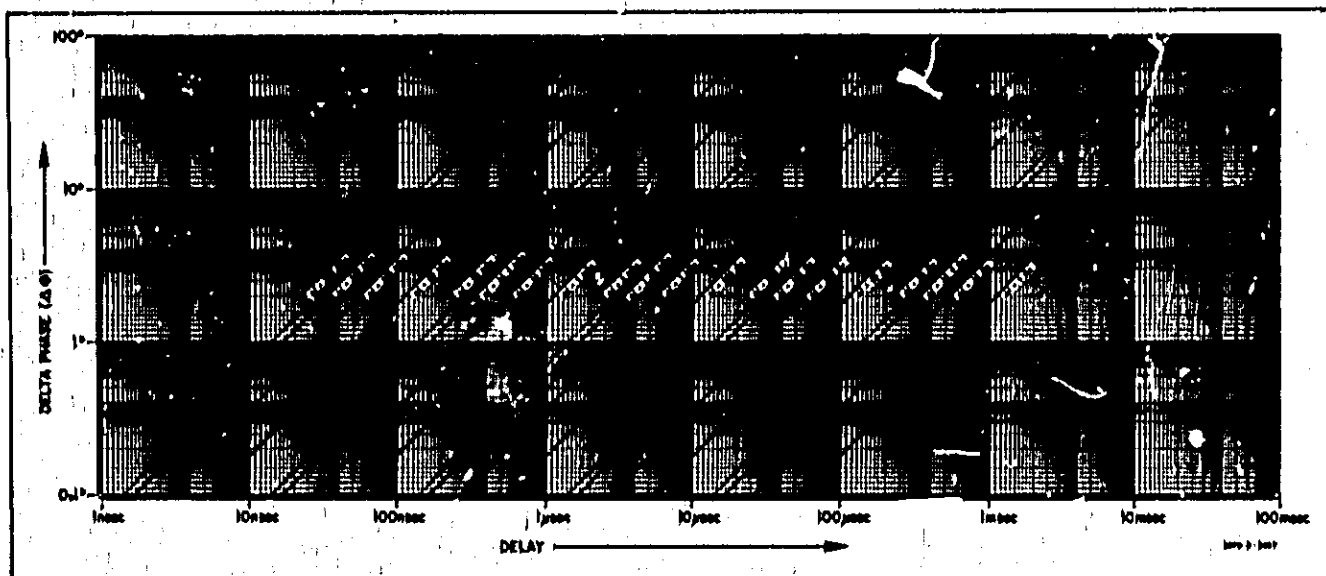
1. If the delay characteristics of the network are totally unknown, a rough approximation can be made using the following formula:

$$T = \frac{N}{8BW} \quad \text{Where: } N = \text{the actual number of poles} \\ BW = \text{bandwidth} \\ T = \text{approximate average delay}$$

b. For swept delay measurements, it is generally desirable to sweep over the entire bandwidth of the network under test. This, in itself, limits Δf to one or two settings since the 3330A/B must be programmed to sweep in 10, 100 or 1000 frequency steps. The approximate Δf setting is equal to the bandwidth divided by the number of steps. For example, if the bandwidth is 48 kHz and the selected number of steps is 100, the approximate Δf setting is 480 Hz. Since 480 Hz is not available, a Δf of 500 Hz could be used. This would extend the swept frequency range to 50 kHz.

c. For swept delay measurements, satisfactory results will generally be obtained using a 100 step sweep.

3-130. Delay Presentation. With the PHASE/DELAY switch in the DELAY position, the right-hand display indicates group delay in milliseconds (mSEC) or microseconds (μ SEC), depending on the Frequency Step Multiplier setting. The display range for each Frequency Step Multiplier setting is listed in Table 3-6.

Figure 3-20. Graph Δf Selection.

3-131. In order to obtain delay readings, the 3330A/B must be sweeping. When the 3330A/B is not sweeping, the presentation will be blanked except for the decimal point, annunciators and polarity sign.

3-132. **Delay Polarity.** When computing $\Delta\phi$ for group delay measurements, the 3570A subtracts the present phase reading (ϕ_2) from the previous phase reading (ϕ_1). If ϕ_2 is more positive than ϕ_1 , $\Delta\phi$ will be negative, yielding a negative delay reading. Conversely, if ϕ_2 is more negative than ϕ_1 , $\Delta\phi$ will be positive, yielding a positive delay reading.

3-133. Typically in group delay measurements, the phase vs. frequency curve of the network under test will have a negative slope in the region of interest. This means that as frequency increases, the phase readings become more and more negative (or less positive), indicating phase lag. A negative slope will produce positive delay readings.

3-134. Negative delay readings are most frequently encountered when the two phase readings, ϕ_1 and ϕ_2 , fall on opposite sides of the ± 180 degree point. For example, if ϕ_1 is -179 degrees and ϕ_2 is -184 degrees, the ϕ_2 reading is actually $+176$ degrees due to the change in polarity at 180 degrees. Since ϕ_2 is more positive than ϕ_1 , the resulting delay reading would be negative and, in this case, totally erroneous since the computed value of $\Delta\phi$ would be -355 degrees (-179) - $(+176)$ rather than $+5$ degrees.

3-135. As indicated in Paragraph 3-77, the ± 180 degree region can be avoided by changing the Phase Reference setting. The only exception to this is where the total phase change between F_{min} and F_{max} is greater than 360 degrees. In this case, the phase curve makes several excursions between -180 degrees and $+180$ degrees and changing the Phase Reference only reverses the transition points. Changing the Phase Reference is, however, a convenient way to test the validity of negative delay

readings. If changing the Phase Reference changes the polarity (and magnitude) of a given delay reading, the negative reading is invalid and the positive reading is correct. If changing the Phase Reference does not change the polarity, the negative reading is valid.

3-136. An interesting sidelight here is that in some of the calculator or computer based systems incorporating the 3570A, the Phase Reference is programmed to change automatically when a negative delay reading is encountered. If the polarity changes, the negative delay reading is rejected and does not appear in the output data.

3-137. Some other causes of negative delay readings are:

- Having the network under test in the Reference Channel (Channel A) rather than the Test Channel.
- Sweeping DOWN instead of UP in the Swept Delay Mode, (Direction of sweep is arbitrary in the CW Mode)
- Having a positive phase vs. frequency slope in the measurement region.

3-138. Offset Measurements (Options 002, 003 only).

3-139. The 3570A optional offset feature allows digital readings to be offset by a value stored in memory. Offsets do not affect the amplitude and phase analog outputs. They do, however, affect both of the delay analog outputs which are derived from the digital delay reading.

3-140. **Functions.** There are two independent offset functions, one for amplitude and one for phase or delay. The respective offset functions are controlled by the two ABSOLUTE/RELATIVE switches on the front panel or by remote ASCII instructions which allow amplitude and/or phase/delay to be programmed to the Absolute (ABS) or Relative (REL) mode. In the Absolute mode, readings are

not offset; in the Relative mode, readings are offset. When the Relative mode is selected, the OFFSET annunciator located above the amplitude or phase/delay display will illuminate.

3-141. Entering Offsets. There are three ways to enter digital offsets into memory:

a. By pressing the ENTER OFFSET pushbutton on the front panel (Local control only). This places the present absolute reading in memory.

b. By applying a remote ASCII instruction: AMPL ENTER OFFSET (Octal code 052) or PHASE/DELAY ENTER OFFSET (Octal code 056). This is the same as pressing the respective Enter Offset pushbutton in Local.

c. By applying a remote ASCII preface (AMPL OFFSET or PHASE/DELAY OFFSET) followed by a numerical data entry. This permits entry of any 5-digit offset within the range of -199.99 to +199.99 (see Paragraph 3-233).

3-142. Offset Readings. In the Relative mode, the digital offset in memory is algebraically subtracted from the present absolute reading. This means that the polarity of the value in memory is changed and the resulting quantity is added (algebraically) to the present absolute reading to obtain the offset reading.

EXAMPLES:

Value In Memory	Absolute Reading	Relative Reading
+180.00	+180.00	00.00
-10.00	+150.00	+160.00
+10.00	+150.00	+140.00
-10.00	-150.00	-140.00

3-143. The display range for relative (offset) readings differs from that of absolute readings. Offset amplitude readings can be within the range of -199.99 dB to +199.99 dB. If a reading exceeds ± 199.99 dB, an overflow will occur causing the reading to be erroneous. *No overflow indication is provided.* Offset phase readings can be within the range of -180.00 degrees to +180.00 degrees. If a reading exceeds ± 180 degrees, the 3570A automatically subtracts 360 degrees from it, yielding a phase reading that is less than 180 degrees and of opposite polarity. The effect is the same as when the phase detector recycles at ± 180 degrees. One exception to this is in the Remote Control mode when Phase (Phase/Delay) and CW Delay (SWP/CW Delay Mode) are selected. In this case, the display range for offset phase readings becomes ± 199.99 degrees. If a reading exceeds ± 199.99 degrees, an overflow will occur causing the reading to be erroneous. Offset delay readings can be within the range of -19,999 counts to +19,999 counts. Readings that exceed $\pm 19,999$ counts will create an overflow.

EXAMPLES:

Value In Memory	Absolute Reading	Relative Reading
-99.99 dB	+100.00 dB	+199.99 dB
-100.00 dB	+100.00 dB	Overflow
-80.00 deg.	+100.00 deg.	+180.00 deg.
-81.00 deg.	+100.00 deg.	-179.00 deg.

3-144. An Offset Application. The 3570A offset capability is a convenience feature which is useful in many measurement applications. One example of this is where it is necessary to quickly measure the gain variations (flatness) of an amplifier as a function of frequency. Consider the case where the gain of an amplifier is specified as 40 dB ± 0.25 dB with frequency response of ± 1.25 dB from 100 Hz to 1 MHz (referred to 1 kHz). The first step in verifying these specifications is to measure the gain at 1 kHz. This can be accomplished using the B-A Amplitude Function with the Absolute/Relative switch set to the ABSOLUTE position. The B-A reading indicates the absolute gain of the amplifier which might be something like +40.13 dB. The next step is to verify the frequency response specification. This could be accomplished in the Absolute mode by adding ± 1.25 dB to +40.13 dB to obtain the test limits. Calculations, however, are time consuming. A faster method would be to simply press the ENTER OFFSET pushbutton and set the Absolute/Relative switch to the RELATIVE position. This would offset the reading by +40.13 dB to provide a 0 dB reference at 1 kHz. The frequency response specification could then be quickly verified by varying the frequency from 100 Hz to 1 MHz while watching for relative readings that exceed the ± 1.25 dB test limits.

3-145. Limit Test Feature (Options 002, 003 only).

3-146. The mention of test limits in the preceding paragraph makes this an appropriate point to discuss the Limit Test feature which is factory installed in 3570A Option 002 and 003. In instruments equipped with the Limit Test feature, a single pair of digital test limits (upper and lower) can be entered into memory by remote control. The test limits can apply to amplitude or phase/delay but not both simultaneously. Depending on the programmed Limit Test mode, the 3570A compares either the amplitude or phase/delay readings to the test limits stored in memory. If a reading is within the test limits, the front panel "GO" annunciator illuminates. If the reading is below the lower limit or above the upper limit, the corresponding "LO" or "HI" annunciator illuminates.

3-147. Limit tests apply to the readings actually displayed on the front panel. Thus, in the Absolute mode the tests apply to the absolute readings. In the Relative mode, the tests apply to the offset readings.

3-148. Limit Test Modes. The three Limit Test modes are:

- a. OFF (Octal code 040)
- b. AMPLITUDE (Octal code 042)
- c. PHASE/DELAY (Octal code 041)

The Limit Test mode is selected by applying the appropriate remote ASCII instruction indicated by the Octal code. When Remote operation is selected, the 3570A remains in the OFF mode until the AMPLITUDE or PHASE/DELAY mode is programmed.

3-149. Limit Sweep Modes. For swept measurements using the hp-3330A or 3330B Automatic Synthesizer, limit tests can be performed in one of two Limit Sweep modes:

- a. Limit Sweep STOP Mode (Octal code 050)
- b. Limit Sweep NO STOP Mode (Octal code 051)

The Limit Sweep mode is selected by applying the appropriate ASCII instruction code. When Remote operation is selected, the 3570A remains in the NO STOP mode until the STOP mode is programmed.

3-150. Stop Mode. When the 3570A is programmed to the Limit Sweep STOP mode, any transition between "GO", "HI" or "LO" causes the 3330A/B to stop sweeping (Figure 3-21). This allows the operator to note the 3570A amplitude and phase readings at the transition point. The test can then be resumed by pressing the LIMIT SWEEP RESTART pushbutton. Note that the Limit Sweep Restart function cannot be programmed remotely.

3-151. No Stop Mode. When the 3570A is programmed to the Limit Sweep NO STOP mode, the 3330A/B continues to sweep regardless of the limit test indications. The 3570A does, however, generate Z Axis markers that will intensify a scope trace at each limit transition point (Figure 3-22).

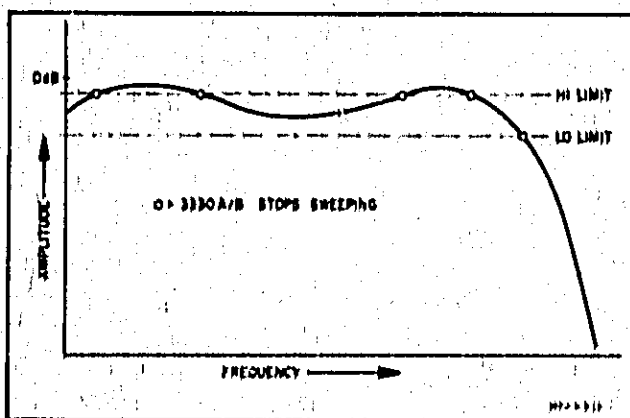


Figure 3-21. Limit Sweep Stop Mode.

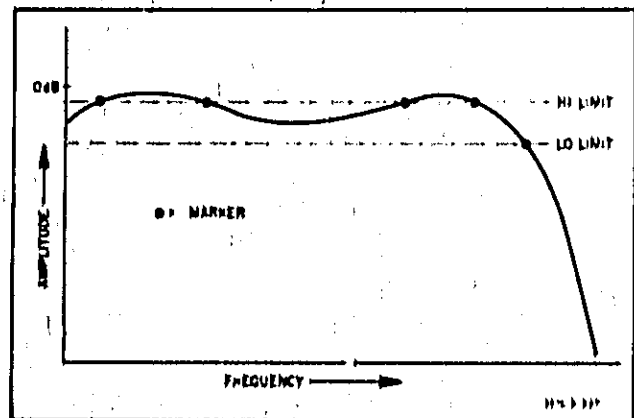


Figure 3-22. Limit Sweep No Stop.

3-152. BASIC OPERATING PROCEDURES.

3-153. Instrument Turn On.

- a. Check the line voltage at the point of installation.
- b. Refer to Figure 3-23. Set the rear panel Line Selector switches to the setting (100, 120, 220 or 240) that corresponds with the line voltage to be used. Line voltage must be within $\pm 10\%$ to $\pm 5\%$ of the selected voltage setting. Line frequency must be within the range of 48 Hz to 66 Hz.
- c. Verify that the proper fuse is installed in the rear panel fuse holder.

Line Setting	Fuse Type	hp Part No.
100 V/120 V	3 A, 250 V Normal Blo	2110-0003
220 V/240 V	1.5 A 250 V Normal Blo	2110-0043

- d. Connect the 3570A to the Frequency Synthesizer (Paragraph 3-16).
- e. Connect the detachable ac power cord to the rear panel power receptacle and to the power source.
- f. Set the LINE switch to the ON position. The front panel displays will illuminate. With no inputs applied to the 3570A, the instrument will respond to extraneous pickup and residual noise. For this reason, the displays may not stabilize until inputs are applied.
- g. Allow a warmup period of at least 1 hour before using the 3570A in a critical measurement application.

3-154. Front Panel Zero Adjustments.

3-155. The front panel Zero adjustments are provided to compensate for slight changes in amplitude and phase accuracy that occur due to environmental changes, source variations and changes in Bandwidth. For optimum accuracy, these adjustments should be performed on a daily basis and any time the Bandwidth setting is changed. If the

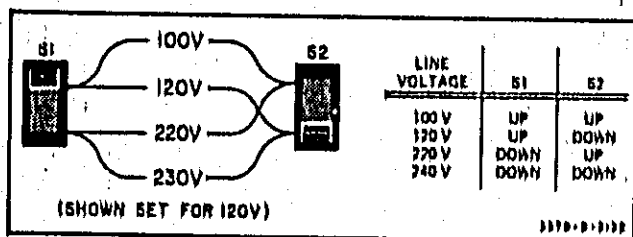


Figure 3-23. Line Selector Switches.

Instrument is operated in an uncontrolled environment, more frequent adjustments may be required.

3-156. Changing the MAX/REF INPUT setting does not normally affect the phase or delay accuracy. It does, however, slightly affect the amplitude accuracy. If, in operation, the setting is to be changed frequently, the Zero adjustments should be performed on the 0 dBm setting to provide the best compromise on all three settings. If one setting is to be used exclusively, optimum accuracy will be obtained by performing the Zero adjustments on that setting. The adjustments should be performed at full level with the Synthesizer set for an output of 0 dBm or 0 dBV (Table 3-7).

3-157. To perform the front panel Zero adjustments, proceed as follows:

a. Using 12" cables (typ. 11170A), connect the A and B Outputs, terminated in 50 or 75 - ohm loads, to the A and B Inputs (Figure 3-8A).

b. Set the MAX/REF INPUT VOLTAGE switch to 0 dBm (or to other range to be used).

c. Set the Synthesizer for an output of 0 dBm (or 0 dBV), 1 MHz.

d. Set the BANDWIDTH switch to the bandwidth that will be used for measurements.

e. Set the AMPLITUDE FUNCTION switch to A.

f. Using a small screwdriver, adjust the A AMP. ZERO control for an amplitude reading of 0 dB $\pm$ 0.05 dB.

g. Set the AMPLITUDE FUNCTION switch to B.

h. Adjust the B AMP. ZERO control for an amplitude reading of 0 dB $\pm$ 0.05 dB.

i. Set the PHASE REFERENCE switch to A.

Table 3-7. Full Level Synthesizer Settings.

Max/Ref Input Setting	Synthesizer Settings	
	50 Ω	75 Ω
1 V	+13.01 dBm	+11.25 dBm
0 dBm	$\pm$ 00.00 dBm	$\pm$ 00.00 dBm
0.1 V	-6.99 dBm	-8.75 dBm

j. Adjust the corresponding (10 Hz, 100 Hz or 3 kHz) ϕ ZERO control for a phase reading of 0 degrees $\pm$ 0.1 degree.

3-158. Input Probe Compensation.

3-159. Before using input probes with capacitive compensating adjustments, it is necessary to adjust the probes for optimum flatness and identical phase characteristics. Once the probes are properly adjusted, they should not require further attention. It is good practice, however, to perform periodic verification checks to ensure that optimum adjustment is maintained.

a. Before connecting the probes, perform the Front Panel Zero Adjustments outlined in Paragraph 3-157.

b. Connect the probes to the A and B Inputs.

c. Connect 50 - ohm (or 75 - ohm) Feed-Thru Terminations directly to the A and B OUTPUT connectors.

d. Connect the A probe to the terminated A Output and the B probe to the terminated B Output.

e. Set the MAX/REF INPUT control and the BANDWIDTH control to the settings used for the Front Panel Zero Adjustments.

f. Set the AMPLITUDE FUNCTION switch to A. Set the PHASE REFERENCE switch to A.

g. Set the Synthesizer amplitude to 0 dBm or 0 dBV (Table 3-7). If 10:1 divider probes are used, the A amplitude reading should now be approximately -20 dB.

h. Set the Synthesizer frequency to 1.5 kHz (10 Hz or 100 Hz Bandwidth) or to 15 kHz (3 kHz Bandwidth).

i. Record the A amplitude reading: ____ dB.

j. Set the Synthesizer frequency to 1 MHz.

k. Adjust the Channel A probe for the same reading recorded in Step i.

l. Repeat Steps h through k until optimum adjustment is obtained.

m. Reset the Synthesizer frequency to 1.5 kHz or 15 kHz (3 kHz BW).

n. Adjust the Channel B probe for a phase reading of 0 degrees $\pm$ 0.1 degree.

o. Set the Synthesizer frequency to 1 MHz.

p. Set the AMPLITUDE FUNCTION switch to B - A.

q. The B - A amplitude reading should be 0 dB $\pm$ 0.2 dB. If it is not, perform the following:

1. Repeat the Front Panel Zero Adjustments.
2. Repeat the probe adjustment procedure.
3. Replace the probes, one at a time, to determine if the problem is caused by faulty probes.

3-160. Amplitude Measurements.

3-161. A and B Function. The A and B Amplitude Functions permit direct measurement of either input level in dB(V) or dB(m) (Paragraph 3-67). To measure the level applied to either input channel, proceed as follows:

- a. Perform the Front Panel Zero Adjustments outlined in Paragraph 3-157.
- b. Connect the network under test to the A or B Output and the A or B Input (Paragraph 3-23).
- c. Set the MAX/REF INPUT VOLTAGE and BANDWIDTH controls to the desired settings (Paragraph 3-54 and 3-56).
- d. Set the Synthesizer amplitude and frequency to obtain the required stimulus.
- e. Set the AMPLITUDE FUNCTION switch to A or B, depending on which input is to be measured.
- f. Observe the amplitude reading in dB(V) or dB(m).
- g. If desired, convert the dB(V) or dB(m) reading to rms volts using the graph shown in Figure 3-9.

3-162. Relative Amplitude Measurements (B - A). In the B - A Amplitude Function, the 3570A measures the relative amplitude of the two input signals in dB. The B - A function can be used for measuring the gain, loss and frequency response of a network or for comparing two networks. For relative measurements using the B - A function, proceed as follows:

- a. Perform the Front Panel Zero Adjustments as outlined in Paragraph 3-157.
- b. To avoid overloads, set the Synthesizer amplitude to 80 dBm.
- c. Make the Reference Input and Test Input connections to the 3570A (Paragraph 3-26).
- d. Set the MAX/REF INPUT VOLTAGE and BANDWIDTH controls to the desired settings (Paragraphs 3-54 and 3-56).
- e. If the network or networks under test exhibit gain:
 1. Set the Synthesizer to a frequency where maximum gain is expected.

2. Set the AMPLITUDE FUNCTION switch to B to monitor the Test Input.

3. Adjust the Synthesizer amplitude setting to obtain a B amplitude reading of 0 dB.

- f. If the network or networks under test exhibit loss:

1. Set the Synthesizer to a frequency where maximum output is expected.

2. Set the AMPLITUDE FUNCTION switch to A to monitor the Reference Input.

3. Adjust the Synthesizer amplitude setting to obtain an A amplitude reading of 0 dB.

- g. Set the Synthesizer to the desired measurement frequency.

- h. Set the AMPLITUDE FUNCTION switch to B - A.

- i. Observe the relative amplitude reading in dB. A negative reading means that B is lower than A (loss); a positive reading means that B is greater than A (gain).

3-163. Phase Measurements.

3-164. The 3570A measures the phase difference between two input signals in degrees. The phase measurement range encompasses 359 degrees, from -179.5 degrees to +179.5 degrees. This leaves a ± 0.5 degree indeterminate region about 180 degrees where the phase detector cannot respond properly. The indeterminate region can be avoided by changing the Phase Reference setting (Paragraph 3-74).

3-165. Phase measurements always require two inputs. When measuring phase, it is important to maintain equal cable lengths in both channels to minimize extraneous phase shifts caused by cable capacitance. In addition, when measuring high impedance circuits use high impedance input probes to minimize the effects of shunt capacitance (Paragraph 3-34).

3-166. To measure phase, proceed as follows:

- a. Perform Steps a through g of the Relative Amplitude Measurement procedure outlined in Paragraph 3-162. The input configurations for relative amplitude measurements and phase (or delay) measurements are identical.

- b. Set the PHASE/DELAY switch (Options 002, 003) to PHASE.

- c. Set the PHASE REFERENCE switch to A.

- d. Observe the phase reading in degrees. A negative reading means that B lags A; a positive reading means that B leads A.

3-167. Group Delay Measurements.

3-168. The 3570A Options 002 and 003, when combined with an -hp- Model 3330A or 3330B Automatic Synthesizer, will measure group delay on a swept or single-frequency basis. In both cases, the 3330A/B must be programmed to sweep and the two instruments must be interconnected with the -hp- 11236B Multi-Unit Cable.

3-169. The following procedures outline the basic steps required to perform CW and swept delay measurements. Refer to Paragraph 3-110 for information concerning the delay measuring process and various control settings.

3-170. CW Delay Measurements.

a. Perform Steps a through f of the Relative Amplitude Measurement procedure outlined in Paragraph 3-162.

b. Set the PHASE/DELAY switch to DELAY. Set the DELAY MODE to CW.

c. Set the PHASE REFERENCE switch to A.

d. Set the 3330A/B to the frequency at which group delay is to be measured. This will be the center frequency between F_{min} and F_{max} .

e. Select the appropriate Δf setting using the 3570A FREQ STEP controls. Note that Δf is always determined by the white multipliers (Paragraph 3-118).

f. Program the 3330A/B Frequency Step to correspond with the 3570A FREQ STEP setting (indicated by blue multipliers).

g. Set the 3330A/B for 10 Frequency Steps. Direction of sweep is arbitrary.

h. Set the 3330A/B TIME/STEP control to obtain the desired sweep rate (Paragraph 3-105).

i. Program the 3330A/B for a continuous sweep (START CONT).

j. Allow time for the delay reading to appear (10 X TIME/STEP).

k. Observe the CW delay reading.

3-171. Swept Delay Measurements.

a. Perform Steps a through f of the Relative Amplitude Measurement procedure outlined in Paragraph 3-162.

b. Set the PHASE/DELAY switch to DELAY. Set the DELAY MODE to SWP.

c. Set the PHASE REFERENCE switch to A.

d. Program the 3330A/B to the center frequency

between F_{min} and F_{max} . When sweeping the entire passband of a network, this will be the center frequency, f_0 .

e. Select the appropriate Δf setting using the 3570A FREQ STEP controls (white multipliers).

f. Program the 3330A/B Frequency Step to correspond with the Δf setting selected on the 3570A (white multipliers).

g. Set the 3330A/B for 10, 100 or 1000 Frequency Steps.

h. Connect and calibrate a scope or X-Y recorder to display the delay vs frequency curve.

i. Set the 3330A/B to sweep UP. A down sweep will produce negative delay readings.

j. Set the 3330A/B TIME/STEP control to obtain the desired sweep rate (Paragraph 3-105).

k. Program the 3330A/B for a continuous sweep (START CONT). (For X-Y recordings a single sweep may be preferable).

l. The delay vs frequency curve of the network will now be presented on the scope or X-Y recording.

3-172. REMOTE PROGRAMMING.

3-173. The 3570A Network Analyzer is equipped for remote control of all front panel functions, ranges and settings (except LINE and Limit Sweep Restart). It will recognize an internally preset "listen" address and accept bit-parallel, word-serial ASCII instructions (see Table 2-1). Instruments equipped with the Isolated HP-IB Two-Way Option (Option 004) will further recognize an internally preset "talk" address and transmit amplitude and phase (or delay) information in a 7-bit ASCII character format.

3-174. The 3570A can be controlled directly from an -hp- 3260A Marked Card Programmer and from most TTL tape readers. With proper interfacing, it can further be controlled by a data modem, tape cassette, teletype, -hp- calculator or computer. The 3570A remote Input/Output structure is directly compatible with the -hp- Model 10631 (A, B or C) isolated HP-IB which allows as many as fifteen com. -hp- instruments to be interconnected and operated on a "party line" basis.

NOTE

This section describes the 3570A Input/Output structure, the basic ASCII format, the remote ASCII instructions and the ASCII output format. All programming information is presented in terms of direct control using an -hp- Model 3260A Marked Card Programmer. For additional information, refer to the -hp- 3040A/3041A/3042A Systems Programming and Interface Manuals.

3-175. Remote Input/Output Structure.

3-176. Remote Connector. The REMOTE CONTROL connector is a 36-pin male printed-circuit connector located on the rear panel of the instrument. It is directly compatible with the mating connectors provided on the -hp- 11236B Multi-Unit Cable. An -hp- Model 11235A Adapter is required for connecting the -hp- Model 3260A Marked Card Programmer. Refer to Section II in this manual and to the 3040A/3041A/3042A Systems Interface Manual for interconnection data and interfacing instructions.

3-177. Remote Pin Connections. Figure 3-24 illustrates the REMOTE CONTROL connector as viewed from the rear of the instrument. The connector drawing and the tables within the figure identify the various control lines.

3-178. A total of fourteen lines are required for a complete remote input/output and control capability. This includes seven Data Lines (LD1 through LD7), six Control Lines (LREN, LMDV, LDAC, HDAC, HRFD and LEOP) and digital circuit ground (Pins 1, A). In the following discussions, these fourteen lines will be referred to as *Remote Control Lines*. The remaining lines on the REMOTE CONTROL connector are used for digital communication between the 3570A and the 3330A or 3330B Automatic Synthesizer. These lines will be referred to as *Synthesizer Control Lines*.

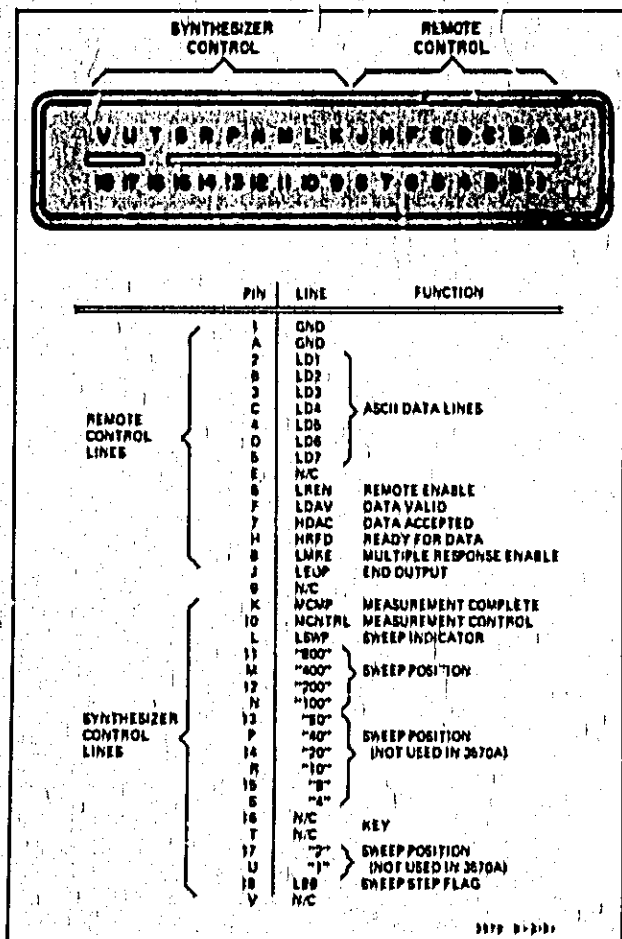


Figure 3-24. Remote Pin Connection.

3-179. Remote Logic. The 3570A uses standard TTL logic for the Remote Control Lines. Logic levels are as follows:

LOW = ground or 0 Vdc to + 0.4 Vdc

HIGH = open or + 2.5 Vdc to + 5 Vdc

With the exception of HDAC and HRFD, all Remote Control Lines have LOW assertion ("1") states as indicated by the prefix "L".

3-180. The Remote Control Lines can serve either as inputs or outputs, depending on the addressed state of the instrument. When a line functions as an input it is normally held at +3 Vdc by a pullup within the instrument. Approximately 3.2 mA of current is required to ensure a logical "1" through a closure to ground. When a line functions as an output, it will supply up to 48 mA in the low state and 0.6 mA in the high state.

3-181. DC Isolation. The *only* instruments with isolated Remote Control Lines are those equipped with the Isolated HP-IB Two-Way option (Option 004). In these instruments, the Remote Control Lines, Synthesizer Control Lines and digital ground can be floated ± 250 Vdc above frame ground if the appropriate options are provided. In all other instruments, digital ground connects directly to frame ground and the remote lines *cannot* be floated.

WARNING

WHEN FLOATING THE 3570A OPTION 004 REMOTE LINES, ENSURE THAT THE FREQUENCY SYNTHESIZER AND ALL OTHER INSTRUMENTS CONNECTED TO DIGITAL GROUND (PINS 1, A) ARE EQUIPPED WITH THE APPROPRIATE OPTIONS AND ARE FLOATING.

3-182. Internal Storage. Internal storage is provided for all remote ASCII instructions applied to the seven Data Lines. Storage is not provided for the single-line instructions such as LREN, LMRE, etc.

3-183. Remote Control Lines.

3-184. The following paragraphs describe the functions of the various Remote Control Lines.

3-185. Data Lines. The seven Data Lines (LD1 through LD7), serve as inputs and outputs for transmitting and receiving 7-bit parallel, word serial ASCII coded data. The Standard Model 3570A and all options are capable of receiving 7-bit ASCII coded instructions applied to these lines. Only instruments equipped with the Isolated HP-IB Two-Way option (Option 004) are capable of transmitting ASCII coded measurement data.

3-186. LREN Line. The LREN (Remote Enable) Line is used to select the Local or Remote control mode. With no input applied to the LREN line, the line is held in the "high" state by an internal pullup, causing the instrument

to remain in Local. When the LREN line is pulled low by an external controller, the instrument switches to Remote. The LREN line does not have internal storage and must, therefore, be held low by the external controller whenever remote operation is required.

NOTE

When using the *hp-3260A Marked Card Programmer*, the LREN line is automatically pulled low when power is applied to the 3260A (LINE ON).

3-187. When Remote operation is selected, the following things take place within the 3570A:

- a. The front panel controls (except LINE and Limit Sweep Restart) are disabled.
- b. The Remote Control Lines are enabled.
- c. The 3570A will retain the settings established by the front panel controls until the settings are changed by remote ASCII instructions.
- d. The 3570A will not accept ASCII instructions or transmit ASCII data until it is properly addressed (Paragraph 3-213).
- e. The 3570A will remain in the AUTO Measurement Control mode (Paragraph 3-231).
- f. The REMOTE annunciator on the 3570A front panel will illuminate.

3-188. When the LREN is released:

- a. The 3570A will remain in remote for a maximum of 2 μ sec before returning to Local.
- b. The Remote Control Lines (except LREN) will be disabled and the front panel controls enabled, causing the 3570A to return to the settings established by the front panel controls.
- c. The 3570A is automatically "unaddressed" (Paragraph 3-224).
- d. Digital offsets and test limits (Options 002, 003) entered in Remote are retained in memory. Note, however, that limit tests can only be performed in Remote (Paragraph 3-145).
- e. The 3570A returns to the AUTO Measurement Control mode (Paragraph 3-231).
- f. The REMOTE annunciator will go out.

3-189. **LMRE Line.** The LMRE line is used by the external controller to obtain the attention of the 3570A and all other instruments connected in parallel on a data bus. The LMRE line must be pulled low by the external controller whenever the 3570A or any other instrument on the bus is

being addressed or unaddressed. Once the instrument has acknowledged receipt of the address or unaddress code, the LMRE line can be released. The LMRE line does not have internal storage. When the 3570A is connected in the *hp-Model 3260A Marked Card Programmer*, the LMRE line is connected to the "200" bit which is otherwise unused (see Paragraph 3-222).

3-190. **LDAV, HDAC and HRFD Lines.** The LDAV (Data Valid) line operated in conjunction with the HDAC (Data Accepted) and HRFD (Ready For Data) lines to synchronize the exchange of ASCII data between external equipment and the 3570A.

3-191. When the 3570A is addressed to "listen" (accept ASCII instructions), the LDAV line is a flag input from the external product ("talker") and the HDAC and HRFD lines are flag outputs to the external product. When the 3570A is addressed to "talk" (transmit ASCII data), the LDAV line is a flag output to the external product and the HDAC and HRFD lines are flag inputs from the external product. In both cases, the operation is the same: When the "talker" outputs data on the seven Data Lines, it pulls the LDAV line low to indicate that valid data is available. If the "listener" is ready to process this data, it sets the HDAC line high and the HRFD line low to indicate that data has been accepted and is being processed. Additional data will not be accepted at this time. When the "listener" has finished processing the data, it sets the HDAC line low and the HRFD line high to indicate that it is ready to accept more data. If more data is available, the sequence is repeated.

3-192. Figure 3-25 shows the timing sequence for the LDAV, HDAC and HRFD lines, along with the LMRE line and the seven Data Lines. Note that the LMRE instruction is given only when the instrument is being addressed and does not accompany the ASCII instructions.

3-193. **LEOP Line.** The LEOP (End Output) line can be used by an external controller to interrupt and unaddress the 3570A and all other instruments on the data bus. The LEOP command is low true.

3-194. Synthesizer Control Lines.

3-195. The following paragraphs describe the functions of the various Synthesizer Control Lines. This information applies only when the 3570A is operated in conjunction with an *hp-3330A* or *3330B Automatic Synthesizer*.

3-196. When the 3570A and the 3330A/B are interconnected with the *hp-11236B Multi-Unit Cable*, there are sixteen data lines that go directly between the two instruments and are not part of the HP-IB. These lines include twelve binary-coded Sweep Lines and four Control Lines: LSWP, LQ, MCNTRL and MCMD.

3-197. **Sweep Lines.** The twelve Sweep Lines are 8-4-2-1 binary-coded outputs from the Synthesizer that are used to indicate the position of the frequency or amplitude sweep.

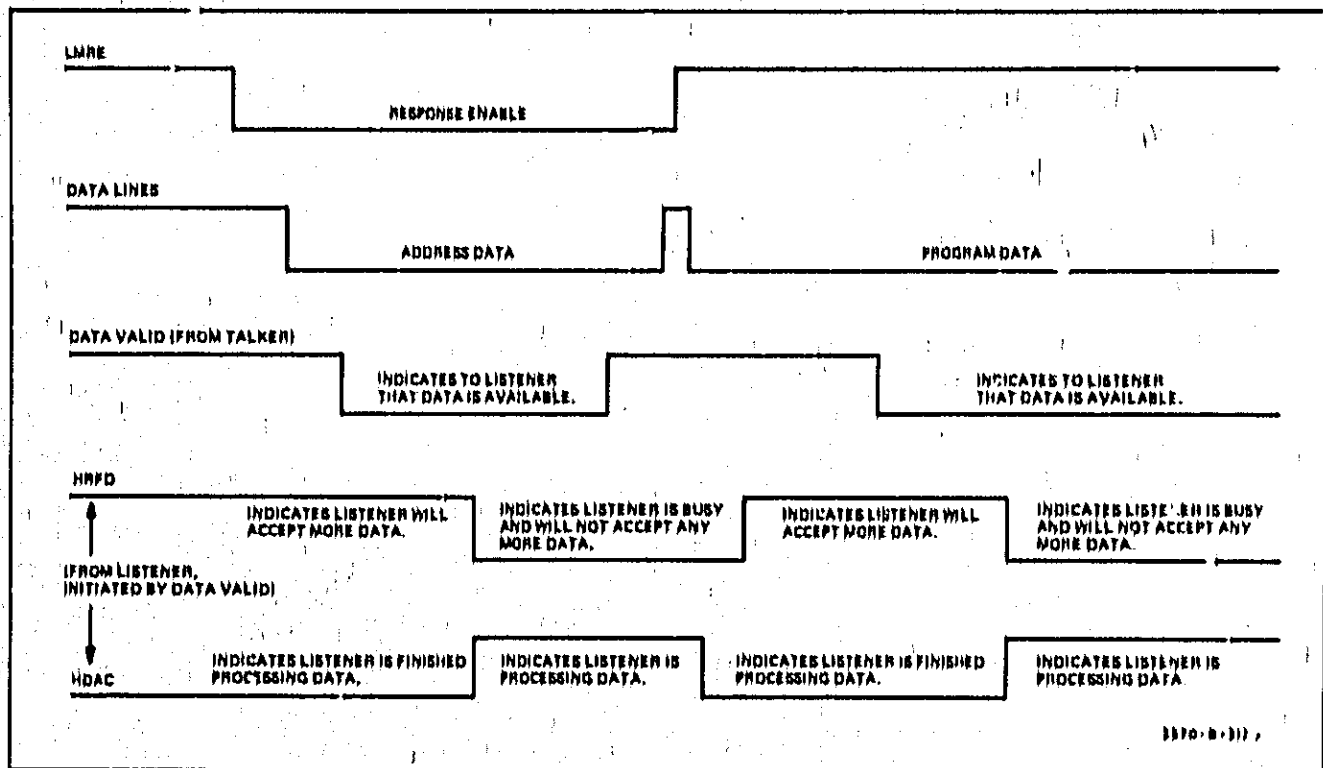


Figure 3-25. Timing Sequence (LDAV, HDAC and HRFD).

Regardless of the number of sweep steps, these lines always count from 000 to 1000 as the frequency or amplitude is incremented from minimum to maximum.

3-198. Although twelve Sweep Lines are available, only four are actually used in the 3570A. These are the "800", "400", "200" and "100" lines which comprise the hundreds and thousands digit in the count from 000 to 1000. In the 3570A, these lines are used to indicate F_{min} , F_c (center) and F_{max} for group delay measurements and marker generation.

3-199. LSWP Line. The LSWP (Sweep) line is an output flag from the 3330A/B which goes low to indicate that it is sweeping. One function of this line is clearly visible when making group delay measurements where the 3330A/B must be sweeping to obtain a delay presentation.

3-200. L00 Line. The L00 line is a flag output from the 3330A/B. This line goes low every 1, 10 or 100 sweep steps, depending on the number of steps selected on the 3330A/B. In the 3570A, the L00 line is used to synchronize the generation of markers available at the Z AXIS OUTPUT.

3-201. MCNTRL and MCMP Lines. The MCNTRL (Measurement Control) and MCMP (Measurement Complete) lines are used to synchronize the 3570A sample rate to the sweep rate of the Synthesizer. Synchronization is required to ensure that the 3570A samples and completes a measurement at each sweep step.

3-202. The Measurement Control line (called Step Ready

in 3330A/B) is an output from the 3330A/B to the 3570A. This line goes low at each sweep step and remains low for the period of the step. (The step period is determined by the TIME/STEP setting on the 3330A/B.) The 3570A does not sample during the step period. At the end of each step period, the Measurement Control line goes high, allowing the 3570A to begin making a measurement. During this time, the 3570A holds the Measurement Complete line (called Sweep Inhibit in 3330A/B) low to prevent the 3330A/B from going to the next sweep step. When the 3570A has completed the measurement, it releases the Measurement Complete line for approximately 40 μ sec, allowing the 3330A/B to proceed to the next sweep step. Figure 3-26 shows the timing sequence for the Measurement Control and Measurement Complete lines.

3-203. The ASCII Format.

3-204. The name ASCII is an abbreviation which stands for the American Standard Code for Information Interchange. The ASCII code is universally recognized and is widely used in the fields of communication and data processing.

3-205. The ASCII code is a human-oriented machine language and as such, takes the form of a 7-bit binary code representing characters such as letters of the alphabet, numbers (0 through 9), punctuation marks and symbols. Many of the symbols are machine instructions found on teletype keyboards.

3-206. Each instruction that the 3570A can recognize (Table 3-8) is represented by an ASCII character. For example, the 3 kHz Bandwidth is represented by the letter

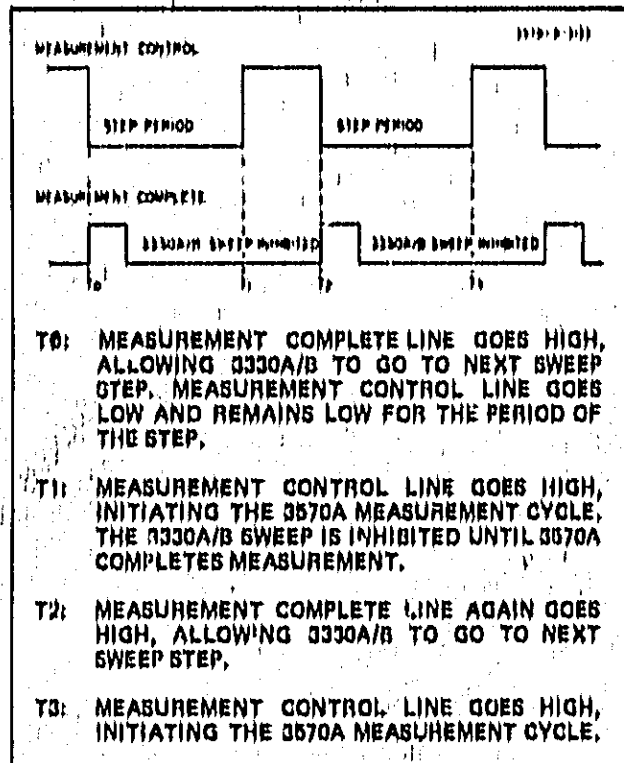


Figure 3-26. Timing Sequence Measurement Control and Measurement Complete.

K; the RELATIVE Amplitude Offset mode is represented by a percent sign (%). Each ASCII character, in turn, represents seven bits of binary information which, when applied to the seven Data Lines (LD1 through LD7) in the 3570A, cause it to execute a given instruction. Continuing with the example, the letter "K" represents a binary code of:

LD7 LD6 LD5 LD4 LD3 LD2 LD1
1 0 0 1 0 1 1

When applied to the seven Data Lines, this code will select the 3 kHz Bandwidth.

3-207. When the 3570A Option 004 transmits amplitude, phase or delay information, the seven Data Lines function as outputs. In this case, a binary code on the data lines represents a numerical digit, polarity sign, comma or teletype instruction (Paragraph 3-235).

3-208. The ASCII instructions and ASCII outputs are in a 7-bit parallel, word serial format. This means that only one 7-bit instruction or one 7-bit character is present on the Data Lines at any given time. Data is transmitted and received in a string of 7-bit ASCII characters.

3-209. Octal Codes. For convenience, the Binary code for each ASCII character is expressed in the form of an Octal code:

3-28

ASCII Char.	Binary	Octal	Instruction
K	1001011	113	3 kHz Bandwidth

3-210. When programming the 3570A using a Marked Card Programmer such as the *hp*-Model 3260A, it is necessary to convert from octal to binary. This is a simple procedure once the relationship between the two is understood. The relationship can best be illustrated by converting from binary to octal:

Binary Code: 1001011 (113 Octal)

The binary code is first divided into three sections:

D7	D6	D5	D4	D3	D2	D1
1	0	0	1	0	1	1

Each section represents a digit of the octal code. Starting from the right, bits D1 - D3 represent the least significant digit (3), bits D4 - D6 represent the second significant digit (1) and D7 is the most significant digit (1).

3-211. Starting with D1, the binary bits are coded in a 1-2-4, 10-20-40, 100 sequence with each Octal digit equaling the sum of the binary-coded bits:

	D7	D6	D5	D4	D3	D2	D1
	"100"	"40"	"20"	"10"	"4"	"2"	"1"
Binary:	1	0	0	1	0	1	1
Octal:	1		1			3	

3-212. Figure 3-27 shows a sample marked card containing several instructions. Any bit that is marked represents a logical "1" while any bit left blank represents a logical "0". Note that the marked card also has a "200" bit. This bit is not used for any of the ASCII codes. It is, however, used to give an LMRE instruction which allows the instrument to be addressed or unaddressed (Paragraph 3-222). The 3570A must always be properly addressed before it will accept ASCII coded instructions or transmit ASCII coded data.

3-213. Addressing.

3-214. The 3570A is designed to operate on a parallel bus structure with other instruments having the same control scheme. For example, when the 3570A and the 3320B (Option 007) or 3330A/B are interconnected with the *hp*-11236B Multi-Unit Cable, the Remote Control lines of the two instruments are connected in parallel, allowing both instruments to be controlled by a single card reader or other controller. If desired, as many as thirteen other instruments could be added using the *hp*-10631 HP-IB and the *hp*-11235A Adapter.

3-215. Since all instruments on a bus share a common set

PROGRAM CARD									
CARD NO. _____ OF _____									
TITLE <u>EXAMPLE INSTRUCTIONS</u>									
NO.	STEP	CODE	200	100	40	20	10	4	2
1	Listen	041							
2	B	102							
3	IV	107							
4	10Hz	112							
5	A	115							
6	100Hz	117							
7									
8									
9									

Figure 3-27. Sample Marked Card - Instructions.

of control lines, the controller must be able to direct the flow of ASCII coded data to and from individual instruments on the bus. This is accomplished by giving each instrument on the bus a different address. The address is a 7-bit ASCII code that a given instrument recognizes and responds to.

3-216. When addressing an instrument, the controller pulls the LMRE line low to obtain the attention of all instruments on the bus. It then gives the ASCII code for the instrument being addressed. When the instrument acknowledges receipt of the address, the controller releases the LMRE line.

3-217. The 3570A Option 004 is a two-way instrument. That is, it receives ASCII instructions and transmits ASCII data on the seven Data Lines. For this reason, it has two addresses: a "listen" address and a "talk" address. When addressed to listen, the 3570A will accept ASCII instructions as outlined in Paragraph 3-226. When addressed to "talk", it will transmit amplitude and phase (or delay) information in the format described in Paragraph 3-241. Instruments not equipped with the Isolated HP-IB Two-Way option (Option 004) cannot transmit ASCII data and, therefore, have only a "listen" address.

3-218. **Changing Addresses.** The 3570A is shipped from the factory with a "listen" address of 041 Octal (ASCII Character I) and a "talk" address of 101 Octal (ASCII Character A). If desired, the address can be changed by changing the position of five jumper plugs on the Address Recognition Assembly, A33.

3-219. Figure 3-28 contains a list of the various address codes available and illustrates the method for changing the address. Note that the "talk" address is always determined by the "listen" address set by the jumper plugs. When the "listen" address is changed, the "talk" address also changes. When changing addresses, be sure that the new address does not conflict with the address or addresses of other instruments on the bus.

JUMPER POSITION		
JUMPER HAVE TWO POSITIONS		
UPPER	+	DOWN
JUMPER ARE NUMBERED LEFT TO RIGHT 5, 4, 3, 2, 1		
SET JUMPER FOR DESIRED ADDRESS CODE LISTED IN TABLE		
OCTAL LISTEN ADDRESS	OCTAL TALK ADDRESS	ADDRESS CODE 5 4 3 2 1
040	100	0 0 0 0 0
041	101	0 0 0 0 1
042	102	0 0 0 1 0
043	103	0 0 0 1 1
044	104	0 0 1 0 0
045	105	0 0 1 0 1
046	106	0 0 1 1 0
047	107	0 0 1 1 1
050	110	0 1 0 0 0
051	111	0 1 0 0 1
052	112	0 1 0 1 0
053	113	0 1 0 1 1
054	114	0 1 1 0 0
055	115	0 1 1 0 1
056	116	0 1 1 1 0
057	117	0 1 1 1 1
060	120	1 0 0 0 0
061	121	1 0 0 0 1
062	122	1 0 0 1 0
063	123	1 0 0 1 1
064	124	1 0 1 0 0
065	125	1 0 1 0 1
066	126	1 0 1 1 0
067	127	1 0 1 1 1
070	130	1 1 0 0 0
071	131	1 1 0 0 1
072	132	1 1 0 1 0
073	133	1 1 0 1 1
074	134	1 1 1 0 0
075	135	1 1 1 0 1
076	136	1 1 1 1 0

Figure 3-28. Address Changing.

3-220. Addressing Format.

3-221. Anytime a "listen" or "talk" address is given, the address code must be accompanied by the LMRE (Multiple Response Enable) instruction. The LMRE instruction is given by pulling the LMRE line low (Paragraph 3-189).

3-222. In the hp-Model 3260A Marked Card Programmer, the "200" bit is wired to the LMRE line. This allows the

programmer to give an LMRE instruction by marking the "200" bit which is otherwise unused. Figure 3-29 shows the proper method for marking a card with a "listen" or "talk" address. Address codes used in Figure 3-29 are 041 and 101, respectively.

PROGRAM CARD		CARD NO. OF											
TITLE LISTEN AND TALK ADDRESS													
NO.	STEP	CODE	200	100	40	20	10	4	2	1			
1	LISTEN	041	☒	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
2	TALK	101	☒	☒	☐	☐	☐	☐	☐	☐	☐	☐	☐
3			☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
4			☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
5			☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

Figure 3-29. Marked Card Talk and Listen Address.

3-223. Clearing the Address. Once the 3570A has been addressed, it will continue to "listen" or "talk" until it is "unaddressed" or cleared by the controller. This means that the 3570A must be cleared before attempting to address another instrument. Conversely, other instruments must be cleared before addressing the 3570A.

3-224. Unaddressing can be accomplished in several ways:

- By applying an "unaddress code" (accompanied by an LMRE instruction).
- By changing from Remote to Local.
- By giving an LEOP (End Output) instruction. (This is a single-line instruction not available when using the Hip-3260A Marked Card Programmer.)
- By addressing another instrument to "talk" when the 3570A is addressed to "talk". (This is the only case where addressing another instrument will clear an address.)

3-225. As in addressing, there are two "unaddress codes": a "listen" unaddress code and a "talk" unaddress code. The "listen" unaddress clears a "listen" address and the "talk" unaddress clears a "talk" address. The "listen" unaddress code is 077 Octal (ASCII Character ?) and the "talk" unaddress code is 137 Octal (ASCII Character _). These are general instruction codes that apply to all instruments on the bus and cannot be changed. The unaddress code must always be accompanied by an LMRE instruction.

3-226. Remote ASCII Instructions.

3-227. Table 3-8 is a complete list of the remote ASCII instructions that apply to the 3570A. These instructions are divided into three categories:

- Front Panel Instructions.

- Special Instructions.

- Numerical Data Entries.

3-228. Front Panel Instructions. The instructions that control front panel functions relate directly to the control settings on the front panel. Refer to Figure 3-1 and the General Operating section for information concerning the various control settings.

3-229. Front panel instructions can be entered in any order desired by the programmer. Note that many of the instructions apply only to instruments equipped with the optional Group Delay, Limit Test and Offset features. These instructions will be ignored by instruments not equipped with the corresponding option.

3-230. Special Instructions. Special instructions do not relate to the front panel and are not available in local. The Special Instructions are:

- Address and unaddress codes (Paragraph 3-220).
- Limit Test Mode: OFF, AMPL, ϕ/D (Paragraph 3-148).
- Limit Sweep Mode: STOP, NOSTOP (Paragraph 3-149).
- Measurement Control: AUTO, CONTR.
- Measure Command.

3-231. Measurement Control and Measure Command. The 3570A uses an internal sample gate to update the amplitude and phase/delay displays at fixed intervals of 250 msec (4 readings/sec). The Measurement Control instructions allow the operator to choose between the internal sample gate (AUTO) and the remote Measure Command (CONTR).

3-232. When Remote operation is selected, the 3570A remains in the AUTO mode and the sample rate is determined by the internal clock. When the CONTR instruction is given, a hold is applied causing both displays to retain the readings present when the instruction was accepted. The readings will not change until the remote Measure Command (054 Octal) is applied. Upon receipt of the Remote Measure Command, the instrument will sample one time and update both displays. The new readings will then be retained until another remote Measure Command is applied.

NOTE

a. During swept measurements, the Measurement Control (MCNTRL) instruction from the 3330A/B overrides the internal sample gate in the AUTO mode.

b. In the CONTR mode, the 3330A/B will continue to control measurements, however the 3570A will also respond to a remote Measure Command unless it is in the process of making a measurement dictated by the 3330A/B.

Table 3-8, ASCII Programming Codes

Function	Detail Code	ASCII Character
FRONT PANEL INSTRUCTIONS:		
Amplitude Function: A	101	A
B + A	103	B
0	102	0
Max/Min Input Voltage: 1 V	107	G
0 dBm	108	E
1 V	106	F
Bandwidth: 3 Hz	113	K
100 Hz	111	I
10 Hz	112	J
Phase Ref: + A	114	L
A	115	M
Phase/Delay: Phase	124	T
Delay	125	U
Frequency Step: 5 Hz	120	P
10 Hz	121	Q
20 Hz	122	R
100 Hz	123	S
Step Multiplier: X1/X.1	136	T
X10/X1	133	I
X100/X10	132	Z
X1k/X100	131	Y
X10k/X1k	130	X
Delay Mode: SWEEP	126	V
CW	127	W
Ampl Offset: REL	045	%
ABS	044	\$
Phase/Delay Offset: REL	047	'
ABS	046	^
Enter Offset (Ampl)	062	'
Enter Offset (B/D)	066	'
SPECIAL INSTRUCTIONS:		
Measurement Control: Auto	116	N
Calc	117	O
Measure Command	054	,
Limit Test Mode: OFF	040	SPACE
AMPL	042	"
B/D	041	
Limit Sweep Mode: STOP	060	{
NOSTOP	061	}
Unaddress Code	077	?
Talk Address	101	A
Listen Address	041	
NUMERICAL DATA ENTRIES:		
AMPL OFFSET	072	:
B/D OFFSET	073	:
UPPER LIMIT	074	<
LOWER LIMIT	075	>
MINUS	065	-
0	060	0
1	061	1
2	062	2
3	063	3
4	064	4
5	065	5
6	066	6
7	067	7
8	070	8
9	071	9

c. In instruments equipped with the Isolated HP-IB Two-Way option, the 3330A/B sweep will be inhibited in the CNTRL mode unless the 3570A is addressed to "talk".

3-233. Numerical Data Entries. Numerical data entries are used in 3570A Options 002 and 003 to store digital offsets and test limits in memory (Paragraph 3-138 and 3-145). Numerical data must always be preceded by one of the following:

AMPL OFFSET (072 Octal)

B/D OFFSET (073 Octal)

UPPER LIMIT (074 Octal)

LOWER LIMIT (075 Octal)

3-234. Numerical data must be entered in order, starting with the Most Significant Digit. Decimal points and leading zeros are assumed; do not enter a decimal point. The polarity sign can be given immediately before, immediately after or during the data string. If a polarity sign is not given, positive polarity is assumed.

EXAMPLES:

Entry: UPPER LIMIT = 159.23 degrees

PROGRAM CARD		CARD NO. _____ OF _____									
TITLE <u>UPPER LIMIT - 159.23 Degrees</u>											
NO.	STEP	CODE	P	70	100	40	20	10	4	2	1
1	Listen	041									
2	B/D	041									
3	UP LIMIT	074									
4	-	055									
5	1	061									
6	5	065									
7	9	071									
8	2	062									
9	3	063									
10											

Entry: AMPLITUDE OFFSET 1.05 dB

PROGRAM CARD		CARD NO. _____ OF _____								
TITLE <u>AMPLITUDE OFFSET 1.05 dB</u>										
NO.	STEP	CODE	200	100	40	20	10	4	2	1
1	Listen	041								
2	AMPL	072								
3	1	061								
4	0	060								
5	5	065								
6										
7										
8										

3-235. ASCII Output (Option 004 only).

3-236. When properly addressed and controlled, the 3570A Option 004 will transmit amplitude and phase/delay information in a 7-bit ASCII character format. Data is transmitted in 7-bit parallel, character serial fashion as controlled by the HDAC and HRFD flags from the "listener" (Paragraph 3-190).

3-237. Initiating the Output Cycle. In order to obtain an ASCII output the following conditions must be met:

a. The Remote Enable line (LREN) must be low (Paragraph 3-189).

b. The 3570A must be in the Controlled (CNTRL) mode (Paragraph 3-232). (When the CNTRL mode is selected the 3330A/B sweep is inhibited until the 3570A is addressed to "talk".)

c. The 3570A must be addressed to "talk" (Paragraph 3-217).

3-238. When the 3570A is interconnected with the hp-3330A/B Automatic Synthesizer and the Synthesizer is sweeping, the output cycle is initiated by the Measure Command from the Synthesizer (Paragraph 3-202). When the 3330A/B is not used or is not sweeping, the output cycle is initiated by the "talk" address which must be preceded by a remote Measure Command (Octal code 054). The following paragraphs outline the instruction sequences required to initiate the output cycle.

NOTE

The 3330A or 3330B Automatic Synthesizer must be used and must be sweeping to obtain an ASCII output using the hp-3260A Marked Card Programmer.

3-239. If the 3330A/B is sweeping:

ENTER: 1) Listen Address
2) CNTRL Mode (Octal code 117)
3) Listen Unaddress
4) Talk Address

Upon receipt of the "talk" address, the 3570A will transmit a complete character string at each sweep step (except in CW Delay Mode)*. The 3330A/B will not go to the next sweep step until all data has been accepted by the "listener". This is determined by the HDAC and HRFD flags from the "listener" which, in turn, control the Measure Complete (sweep inhibit) flag from the 3570A to the 3330A/B.

* In the CW Delay Mode (10 step sweep), the 3570A transmits amplitude on the fifth sweep step (sixth point) and then waits until the tenth sweep step (eleventh point) to transmit the CW delay reading. This does not effect the output format except for the time delay between the amplitude output and the delay output.

3-240. If the 3330A/B is not used or is not sweeping:

ENTER: 1) Listen Address
2) CNTRL Mode (Octal code 117)
3) Measure Command (Octal code 054)
4) Listen Unaddress
5) Talk Address

Upon receipt of the remote Measure Command, the 3570A will sample one time and update the data to be transmitted. It will retain the new data until another remote Measure Command is applied or until the "talk" address is given. Upon receipt of the "talk" address, the 3570A will transmit one complete character string as controlled by the HDAC and HRFD lines from the "listener". Once the complete character string has been accepted by the "listener", the 3570A will stop transmitting and wait for another remote Measure Command. To obtain additional outputs with the 3570A still in the CNTRL mode, the sequence is as follows:

ENTER: 1) Talk Unaddress
2) Listen Address
3) Measure Command (Octal code 054)
4) Listen Unaddress
5) Talk Address

This sequence must be repeated each time an output string is required.

3-241. The Output Format. During each output cycle, the 3570A transmits a series or "string" of 7-bit ASCII characters. Each character string contains two readings: Amplitude and Phase or Amplitude and Delay. In both cases, Amplitude is transmitted first and the two readings are separated by a comma. Each character string is followed by two teletype (TTY) instructions: Carriage Return (CR) and Line Feed (LF).

3-242. The basic formats for Amplitude and Phase and Amplitude and Delay are as follows:

Amplitude and Phase:

Character Order:	Amplitude							Phase							TTY	
	SGN	OR	D4	D3	D2	D1	D0	SGN	OR	D4	D3	D2	D1	D0	CR	LF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Amplitude and Delay:

Character Order:	Amplitude							Delay							TTY	
	SGN	OR	D4	D3	D2	D1	D0	SGN	OR	D4	D3	D2	D1	D0	E EXP	CR LF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Amplitude and Phase readings are transmitted in fixed-point notation, exactly as they appear on the front panel displays. The order is: Polarity Sign (SGN), Overrange "1" (OR), D4, D3, Decimal Point, D2 and D1. Delay readings are transmitted in floating-point notation. The order is: Polarity Sign (SGN), Overrange "1" (OR), D4, Decimal Point, D3, D2 and D1. Immediately after D1, the 3570A transmits the letter "E" followed by a numerical exponent (0 through 4). The exponent indicates the number of places the decimal point must be moved to the right (toward D1) to obtain the correct delay reading in *microseconds*. This differs from the front panel display which is read in

milliseconds or microseconds, depending on the delay range.

3-243. When the optional Limit Test feature is used, a two-digit Limit Code, representing "GO" "HI" or "LO", is transmitted immediately after the Phase or Delay reading. The Limit Code can apply to Amplitude or Phase/Delay depending on the programmed Limit Test mode.

3-244. The Limit Codes are as follows:

COND.	LT1	LT2
"GO"	0	0
"HI"	+	1
"LO"	-	1

3-245. The basic formats for outputs containing Limit Codes are as follows:

Phase and Limit Test
(Preceded by Amplitude Information):

	Phase								Limit Test		TTY.	
Character:	SGN	OR	D4	D3	D2	D1	D0	LT1	LT2	CR	LF	
Order:	9	10	11	12	13	14	15	16	17	18	19	20

Delay and Limit Test
(Preceded by Amplitude Information):

	Delay								Limit Test		TTY.	
Character:	SGN	OR	D4	D3	D2	D1	E	EXP	LT1	LT2	CR	LF
Order:	9	10	11	12	13	14	15	16	17	18	19	22

3-246. Example Printouts. The following are some actual teletype printouts obtained using the 3570A ASCII output. Note that the 3570A output must be converted from bit-parallel to bit-serial to interface with a teletype.

Amplitude and Phase:

-100.01, +163.45

Amplitude and Delay:

+100.01, -00.177E2

Amplitude and Delay and Limit Test:

-112.55, -00.252E1, 00

Delay When 3330A/B is Not Sweeping (display blanked):

-006.44, -07.77E3

3-247. Output codes. Table 3-9 is a list of the various ASCII characters and associated Octal codes used in the 3570A output.

Table 3-9. ASCII Output Codes.

ASCII Character	Octal Code
0	060
1	061
2	062
3	063
4	064
5	065
6	066
7	067
8	070
9	071
.	066
.	064
E	106
+	063
-	065
?	077
CR	015
LF	012

SECTION IV THEORY OF OPERATION

4.1. INTRODUCTION.

4-2. This section contains a Simplified Block Diagram Description and a Functional Description of the 3570A analog section.

4.3. SIMPLIFIED BLOCK DIAGRAM DESCRIPTION (Analog Section).

4-4. Refer to the Simplified Block Diagram, Figure 4-1, for the following discussion.

4-5. The 3570A analog section consists basically of an Active Power Splitter, two identical Measurement Channels, A and B, a Local Oscillator, a Phase Detector and an Output Buffer. The analog (dc) amplitude and phase information from the Output Buffer is applied to the rear panel analog outputs and to an Analog to Digital (A to D) Converter. The A to D converter digitizes the analog amplitude and phase information, providing the binary-coded data for the front panel digital displays.

4-6. The 0 Hz to 13 MHz signal from the output of the Synthesizer is applied to the Active Power Splitter where it is divided and amplified, producing two signals that are equal in amplitude and in phase. These signals are applied to the A and B OUTPUT connectors on the 3570A front panel. The signal at the Channel A OUTPUT is used as a reference while the signal at the Channel B OUTPUT serves as a stimulus for the network under test. The signals from the external reference and test configurations are applied to the Channel A and Channel B INPUT connectors. After passing through a wideband input amplifier, the signals in

each Measurement Channel are mixed with a 0.1 MHz to 13.1 MHz signal from the Local Oscillator, producing a 100 kHz (0.1 MHz) Intermediate frequency (IF). The 100 kHz IF signal in each channel is fed through a series of bandpass filters which provide the three selectable BANDWIDTH settings, 10 Hz, 100 Hz and 3 kHz. The filtered IF signal is then converted to a logarithmic value and applied to an amplitude detector (within Measurement Channel) and to the Phase Detector. In the amplitude detector, the signal is converted to a dc voltage that is logarithmically proportional to the amplitude of the input signal. The logarithmic dc voltages from both Measurement Channels are applied to the Output Buffer. In the Output Buffer, they are filtered, amplified and fed to a function switching circuit where they are individually selected (Log A or Log B) or summed (Log B - Log A) and applied to the A to D Converter and the rear panel AMPLITUDE FUNCTION output. The Phase Detector senses the time difference between the axis crossing points of the two 100 kHz IF signals, producing a dc voltage proportional to phase. This voltage is fed to the Output Buffer where it is filtered, amplified and applied to the A to D Converter and rear panel PHASE/DELAY output.

4.7. FUNCTIONAL DESCRIPTION (Analog Section).

4-8. Refer to the Functional Block Diagram, Figure 7-9. For the following functional description, the analog section of the 3570A is divided into four sections: Measurement Channels (Paragraph 4-9), Phase Limiter and Phase Detector (Paragraph 4-30), Output Buffer (Paragraph 4-35) and Local Oscillator (Paragraph 4-40).

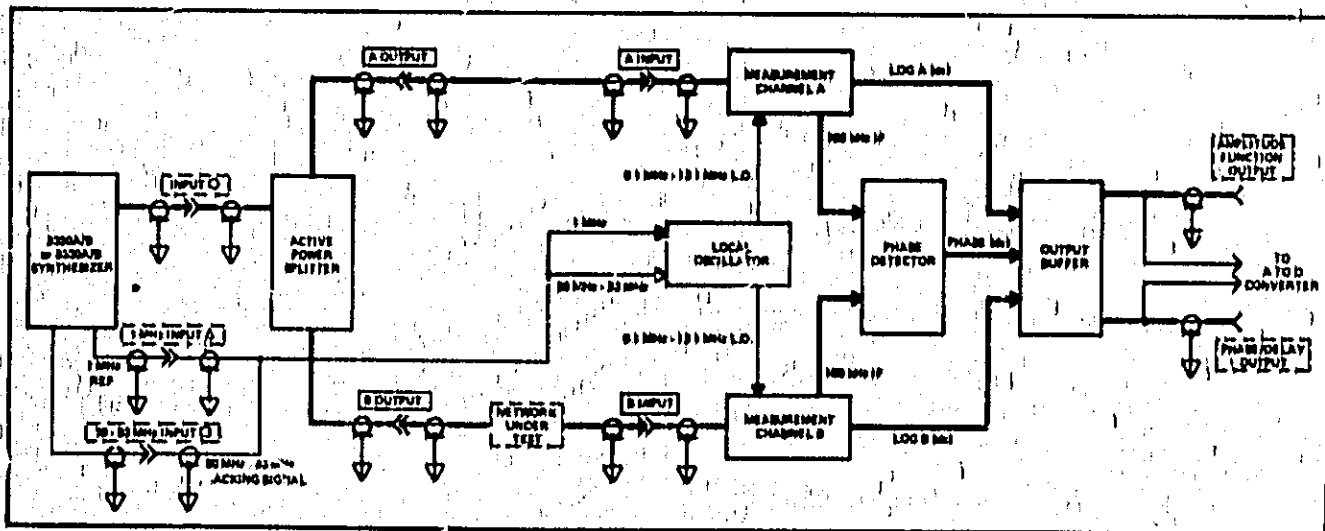


Figure 4-1. 3570A Simplified Block Diagram.

4-9. Measurement Channels.

4-10. Refer to the function Block Diagram, Figure 7-11. Since the two measurement channels are identical, the following description of Channel A applies to both channels.

4-11. Each measurement channel is comprised of an Input Amplifier and Reference Attenuator, an Input Mixer and IF Amplifier, three Crystal Filters, Bandwidth Logic and a Log Amplifier. The Input Amplifier provides impedance conversion between the INPUT connector and the Reference Attenuator. The Reference Attenuator is controlled by the MAX/REF INPUT VOLTAGE setting and is used to attenuate the signal on the 1 V range. The Input Mixer mixes the input frequency with the Local Oscillator frequency producing a 100 kHz IF. The IF Amplifier contains the bandpass filters used for the 3 kHz BANDWIDTH setting. The 10 Hz and 100 Hz Bandwidths are provided by the Crystal Filters. The Bandwidth Logic provides further IF amplification, detects overloads and provides the control signals used for Bandwidth selection. The Log Amplifier converts the IF signal to a logarithmic value, provides a detected log output for amplitude measurements and supplies a filtered 100 kHz output for phase measurements.

4-12. Input Amplifier (A1/A17 Schematic No. 2). Refer to Figure 7-9 and Schematic No. 2 for the following discussion.

4-13. The Input Amplifier is a low noise, broad-band amplifier circuit which provides unity gain and impedance conversion between the input connector and the Reference Attenuator. CR1 through CR4 are overload protection diodes. Q1 is a negative feedback circuit used to minimize the effect of stray capacitance in the diode protection circuit and the input FET (Q2) circuit. Q2 is a low noise high impedance FET that insures a minimum loading effect on the input signal. Q4 is an emitter-follower that looks into a constant load of 1.3 kilohms. The integrator circuit U1, and transistor Q3 provide bias stability for the source of Q2. Q5 is a constant current source for Q4.

4-14. Reference Attenuator. The Reference Attenuator is used to introduce 13 dB of attenuation when the MAX/REF INPUT VOLTAGE is set to 1 V. In this mode K1 is closed and the R13, R14 attenuator resistors are selected to attenuate the signal 13 dB (11.25 dB in 75 ohm option). When K2 is closed, R14 is shunted and R13 acts as a feed through resistor. Q6 is a buffer amplifier and Q7 acts as a constant current source for Q6. The diodes CR5 through CR8 act as transient protection for the Input Mixer.

4-15. Input Mixer (A2/A18 Schematic No. 2). The Input Mixer is comprised of two integrated circuits: a limiter (U1) and an active mixer (U2). The limiter converts the 200 mV rms, 0.1 MHz to 13.1 MHz sine-wave input from the Local Oscillator to two square wave outputs (U1 pins 11 and 12) that are equal in amplitude and 180 degrees out

of phase. These square-wave outputs are used to drive the double-balanced active mixer, U2. When U2 is properly balanced, the output (U2 pin 1) is a composite signal containing only the sum and difference frequencies. The difference frequency is always 100 kHz. There are two adjustments used to balance the Input Mixer: the RF Feedthrough adjustment, R9 and the L.O. Feedthrough adjustment, R26. The RF Feedthrough control is adjusted for minimum feedthrough of a 100 kHz input signal. The L.O. Feedthrough adjustment is performed with the input frequency set to 0 Hz, making the L.O. frequency 100 kHz. Proper adjustment results in minimum feedthrough of the 100 kHz L.O. signal.

4-16. IF Amplifier. The IF Amplifier portion of the Input Mixer board is comprised of a gain control circuit (Q2, Q3), a two stage IF amplifier (Q4, Q5) and an output emitter follower (Q6). The gain control circuit is controlled by bit 3 from the PS Register which, along with PS4, is also used to control the Reference Attenuator of the Input Amplifier board. When PS3 is high (1 V and 0 dBm ranges), the overall gain of the Mixer/IF Amplifier is +13 dB (50-ohm systems) or +11.3 dB (75-ohm systems). When PS3 is low (0.1 V range), the gain is +20 dB. This makes the full-scale output voltage at A2 pin 1 equal to 1 V rms on all three MAX/REF INPUT VOLTAGE settings. The IF amplifier is comprised of two cascaded RLC-tuned amplifier stages. Each stage has a center frequency of 100 kHz and a bandwidth of 5.88 kHz. The IF amplifier filters out the sum frequency from the output of the mixer, making the output frequency 100 kHz. Variable inductors L2 and L3 are adjusted for peak amplitude of the 100 kHz IF signal. The 100 kHz signal from the output of the IF amplifier is applied to the Crystal Filters and to the Bandwidth Logic.

4-17. Crystal Filters (A3, A4, A5/A19, A20, A21 Schematic No. 3). Both measurement Channels contain three cascaded Crystal Filters which are used to establish the 10 Hz and 100 Hz bandwidths. The 3 kHz bandwidth is established by filters on the Input Mixer and Bandwidth Logic boards. Each Crystal Filter can be divided into four basic sections: a crystal (Y1), a compensating network (T1, C1, C2), a variable "Q" switching network (Q1, R3) and an output buffer (Q2, Q3).

4-18. The crystals used in the 3570A are pre-aged at the factory and are selected for a center frequency between 99,997.5 Hz to 99,999.5 Hz. The reason for using crystals with a center frequency slightly lower than the required 100.00 kHz, is to allow the frequency to be adjusted by placing a "pulling" capacitor (C3*, C4* parallel combination) in series with the crystal (see Figure 4-2A).

4-19. The compensating network consisting of T1, C1 and C2, is used to cancel the shunt capacitance (C_s) of the crystal and any additional capacitance introduced by the connectors and circuit boards. Transformer T1 functions as an inverter, producing a voltage that is equal in amplitude and 180 degrees out of phase with the signal applied to the crystal. The combined value of parallel capacitors, C1 and C2, is approximately equal to the shunt capacitance. The

result is that the circulating current flowing through the shunt capacitance is cancelled.

4-20. With the addition of the compensating network, the equivalent circuit appears as shown in Figure 4-2B. The capacitor to ground, C_t , represents the crystal shunt capacitance, C_s , in parallel with the compensating capacitors, C_1 and C_2 . The value of C_t is approximately equal to $2 C_s$ or 40 pF. The 40 pF capacitance to ground has an undesirable effect since it produces high frequency roll off, causing the filter skirts to be unsymmetrical. This is prevented, however, by including C_t in a parallel resonant circuit consisting of C_5 , C_6 and L_1 . The parallel resonant circuit balances out the symmetry of the filter skirts.

4-21. The "Q" of the Crystal Filter can be defined by the equation:

$$Q = \frac{X}{R}$$

Where: Q = figure of merit
X = reactance of crystal at 100 kHz
R = resistance to ground

From this equation, it can be noted that increasing the resistance to ground lowers the Q; decreasing the resistance to ground raises the Q. On the 100 Hz BANDWIDTH setting, transistor Q1 is off and the Q of the filter is determined by resistor R1 and the impedance of the parallel resonant circuit (C_5 , C_6 and L_1). On the 10 Hz

BANDWIDTH setting, transistor Q1 is gated on by a logic signal from the Bandwidth Logic board. This places R3 in the circuit thus lowering the resistance and increasing the Q. On the 100 Hz bandwidth, each Crystal Filter must have a center frequency of 100 kHz, a bandwidth of 196 Hz and a Q of 510.2. On the 10 Hz bandwidth, each filter must have a center frequency of 100 kHz, a bandwidth of 19.6 Hz and a Q of 5102.

4-22. There are two adjustments on A3/A19 and A4/A20: the 10 Hz ADJ. (C_1) and the 100 Hz ADJ. (C_6). The 10 Hz ADJ. capacitor is adjusted for optimum symmetry of the filter skirts. The 100 Hz ADJ. capacitor is adjusted so that the center frequency is exactly 100 kHz. On the A5/A21 boards there is an additional network that is used to insure equal gain when switching the bandwidths.

4-23. The output buffer portion of the Crystal Filter board is a two-stage amplifier circuit consisting of FET Q2 and transistor Q3. This circuit has a high input impedance to prevent the high impedance filter network from being loaded.

4-24. Bandwidth Logic (A6/A22 Schematic No. 3). The Bandwidth Logic board can be divided into three sections: an IF amplifier (Q1 through Q4), an overload detector (Q5 through Q8) and a bandwidth logic circuit (U1, U2). The IF amplifier consists of a low-noise differential amplifier circuit (Q1 through Q3) and an output emitter follower (Q4). The gain of the amplifier is adjustable (R7) from approximately 2.6 to 3.2. The bandwidth is 5.88 kHz as

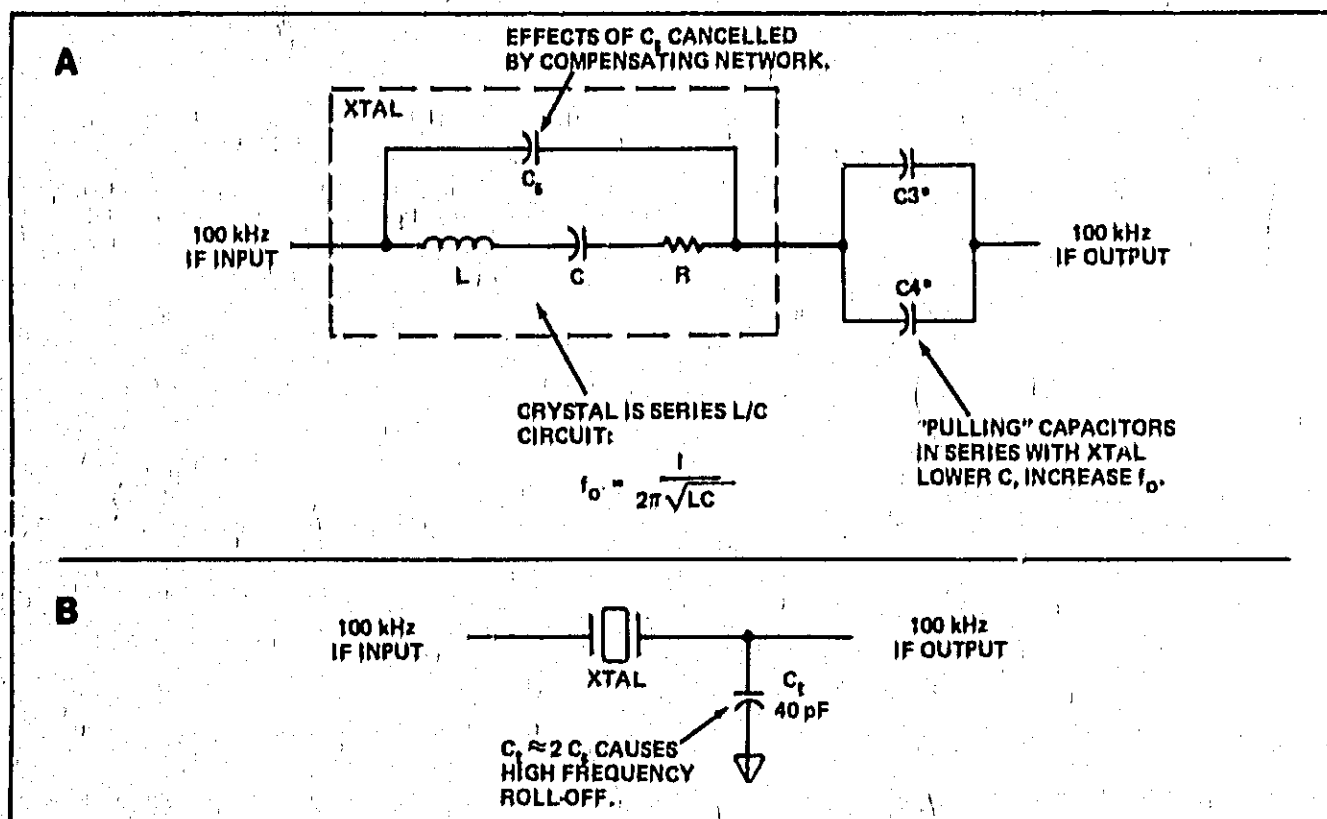


Figure 4-2. Crystal Filters.

amplifiers (Input Mixer board) are also 5.88 kHz. With three cascaded amplifier stages each having a bandwidth of 5.88 kHz, the overall bandwidth is 3 kHz. This provides the required bandpass characteristics for the 3 kHz BANDWIDTH setting. The full scale (0 dB) voltage at the output of the amplifier is 1.7 V rms.

4-25. The overload detector is a high gain, differential amplifier that compares the peak value of the IF signal at the base of Q5 to a +4.6 Vdc reference at the base of Q4. If the peak value of the IF signal exceeds 4.6 V (3.25 V rms), transistors Q5, Q7 and Q8 are biased on, causing the front panel overload indicator (AOL or BOL) to illuminate. The gain of the preceding IF amplifier is adjusted by observing the overload indicator.

4-26. The bandwidth logic circuitry is controlled by bits 1 and 2 of the PS Register which, in turn, are controlled by the BANDWIDTH setting. In response to PS1 and PS2, the bandwidth logic provides bandwidth selection for the Crystal Filters and the decoding and drive signals (L10 Hz, L100 Hz and L3 kHz) that are used to enable the ϕ ZERO controls on the 3570A front panel.

Δ 4-27. Log Amplifier (A7/A23 Schematic No. 4). The Log Amplifier is comprised of three sections: the Log Amplifier (U1 thru U6), an amplitude detector (Q1, Q2, Q3, U7, and Q5, Q6) and an IF amplifier (Q4). The log amplifier is a hybrid circuit designed specifically for use in the 3570A. This circuit converts the amplitude of the incoming IF signal to a logarithmic value, providing the 100 dB dynamic range of the instrument. The control amplifiers are used to gate on succeeding stages within the log amplifier as a function of signal level. The logarithmic signal from pin 11 of the log amplifier package is filtered thru the low pass filter network (C26, C27, C28, and L3) and coupled through C29 to the amplitude detector and the IF amplifier.

Δ 4-28. The amplitude detector is a full wave rectifier circuit which converts the 100 kHz logarithmic signal to a dc voltage. The output of the detector, a dc voltage logarithmically proportional to the amplitude of the input signal, is applied to the Output Buffer (U7). Q5 and Q6 are used to minimize temperature drift.

Δ 4-29. The IF amplifier is a buffer between the log amplifier and the phase limiter.

4-30. Phase Limiter and Phase Detector.

4-31. Phase Limiter (A13 Schematic No. 5). The Phase Limiter is comprised of a phase zero circuit (Q4, C2, R7) and two limiter circuits (U1, U2). The 100 kHz IF signal from the Channel A Log Amplifier is applied to limiter U1 through the phase zero circuit and emitter follower Q5. The IF signal from the Channel B Log Amplifier is applied directly to limiter U2 through emitter follower Q6. The phase zero circuit contains an R/C network (C2, R7) which permits the phase of the Channel A IF signal to be adjusted using the 10 Hz, 100 Hz or 3 kHz ϕ ZERO control on the

3570A front panel. The ϕ ZERO controls are enabled by the respective L10 Hz, L100 Hz and L3 kHz logic signals from the Channel A Bandwidth Logic board (A6). The A and B limiters are dual differential amplifiers which detect the zero crossing points of the applied IF signals and produce symmetrical square-wave outputs that are limited to 1 V p-p. The outputs from the two limiters are A, which is in phase with the signal applied to Channel A, $\bar{A}$ which is 180 degrees out of phase with A, B which is in phase with the signal applied to Channel B and $\bar{B}$ which is 180 degrees out of phase with B. These signals are applied to the Phase Detector.

4-32. Phase Detector (A14 Schematic No. 5). The square-wave outputs from the Phase Limiter, A, $\bar{A}$, B and $\bar{B}$, are applied to the level translator (U1) on the Phase Detector board. The level translator is comprised of two differential amplifiers which convert the levels of the incoming square waves to levels compatible with the ECL logic used in the Phase Detector. The outputs of the level translator are applied to four Exclusive OR gates in U2. The purpose of the Exclusive OR gates is to permit the Channel A signals, A and $\bar{A}$ to be inverted when the ϕ PHASE REFERENCE setting is selected. Note that the Channel A signals are applied to one input of their respective Exclusive OR gates while the other input of each gate is connected to the collector of Q1. Transistor Q1 is controlled by bit 0 of the PS Register which, in turn, is controlled by the PHASE REFERENCE setting. When PS0 is high (A), Q1 is gated on, the logic input to the Exclusive OR gates is low and the Exclusive OR outputs are not inverted. When PS0 is low ($\bar{A}$), the logic input is high causing the Exclusive OR outputs to be inverted. This offsets the phase reading by 180 degrees. The remaining two Exclusive OR gates do not invert the Channel B signals and are included only to make the gate delays of all four signals equal.

4-33. The outputs of the Exclusive OR gates are applied to two high-speed, ac-coupled J-K flip flops (U3). In the upper J-K flip flop, the Q output is set high by a positive transition on A at the J input and is reset low by a positive transition on $\bar{B}$ (same as negative transition on B) at the K input. Similarly, the Q output of the lower J-K flip flop is set high by a positive transition on $\bar{A}$ (same as negative transition on A) at the J input and is reset low by a positive transition on B at the K input. The $\bar{Q}$ outputs of the two flip flops are 180 degrees out of phase with the Q outputs. Figure 4-3 shows the Q outputs of the two flip flops with an applied phase difference of +60 degrees. From Figure 4-3, it can be noted that the 60 degree phase difference is represented by the time between points T0 and T1 where both of the Q outputs are low.

4-34. The Q and $\bar{Q}$ outputs of the two J-K flip flops are applied to switching circuits consisting of transistors Q2 through Q9 and FET switches Q10 through Q13. The Q and $\bar{Q}$ outputs from the upper J-K flip flop control FET switches Q10 and Q11, respectively. The Q and $\bar{Q}$ outputs from the lower J-K flip flop control FET switches Q12 and Q13, respectively. When the Q or $\bar{Q}$ output is high, the associated FET switch is gated on. The function of the FET

switches is to gate current from the two constant current sources (U4, Q14 and U5, Q15). When FET switch Q10 or Q12 (controlled by Q outputs) is gated on, a positive voltage is developed at the junction of C4 and R43, causing the output of summing amplifier/integrator, U6, to go negative. Conversely, if FET switch Q11 or Q13 (controlled by $\bar{Q}$ outputs) is gated on, a positive voltage is developed at the junction of C3 and R44, causing the output of U6 to go positive. Table 4-1 is a truth table which indicates the quiescent voltage at the output of U6 when various combinations of FET switches are gated on. With all four FET switches being gated on and off by the outputs of the J-K flip flops, the summed, integrated voltage at the output of U6 is proportional to the phase difference between the two input signals, A and B. The output level is approximately 20 mVdc per degree, ranging from -3.6 V at -180 degrees to +3.6 V at +180 degrees. This dc output voltage is applied to the Output Buffer, A15.

Table 4-1. Phase Detector Output.

Q10	FET Switches*		Q13	Output Voltage
Q12	Q11			
1	0	0	0	-1.8 V
0	1	0	0	-1.8 V
1	1	0	0	-3.6 V
0	0	1	0	+1.8 V
0	0	0	1	+1.8 V
0	0	1	1	+3.6 V
1	0	0	1	0 V
0	1	1	0	0 V

*"1" = ON; "0" = OFF

4-35. Output Buffer.

4-36. The Output Buffer (A15, Schematic No. 6), provides noise filtering and amplification for the dc amplitude and phase information before it is applied to the rear panel analog outputs and the A to D Converter. In addition, the Output Buffer contains circuitry used for the front panel AMP, ZERO adjustments and provides Amplitude Function and Phase/Delay switching. The Output Buffer can be divided into three sections: noise filters (Q1 through Q10), amplitude section (U1 through U7) and phase/delay section (U8).

4-37. The noise filters consist of a decoder/driver circuit (U1, U2A, Q1 - Q2), FET switches (Q5 through Q10) and filter capacitors (C2 - C4, C6 - C8, C9 - C12). The decoder/driver circuit is controlled by bits PS1 and PS2 which are controlled by the BANDWIDTH setting. The FET switches are used to place filter capacitors in or out of their associated circuits in response to signals from the decoder/driver. Table 4-2 lists the condition of PS1 and PS2 and the resulting states of the various switching transistors for each of the three BANDWIDTH settings.

4-38. The amplitude section is comprised of two dc amplifiers (U4, U6), two level shifters (U3, U5), a summing amplifier (U7) and an amplitude switching circuit (K1 through K3). The dc amplitude outputs from the Channel A and Channel B Log Amplifiers are filtered and applied to the non-inverting inputs of operational amplifiers U4 and U6, respectively. These operational amplifiers provide a gain of 4, making the output level 100 mVdc per dB. The inverting inputs of U4 and U6 are referenced to dc voltages provided by level shifters U3 and U5. Note that the dc voltage from the Log Amplifiers ranges from 2.75 V at 0 dB to 0.25 V at -100 dB. The level shifters introduce the dc offsets required to make the analog outputs from U4 and U6 range from 0 V at 0 dB to -10 V at -100 dB. The amount of offset introduced by the level shifters can be adjusted using the front panel AMP, ZERO controls. The zero controls provide an adjustment range of approximately ± 5 dB. The outputs of U4 and U6 are applied to the Amplitude Function switching circuit and to summing amplifier U7. The output of U7 is equal to the difference between the Log A and Log B inputs, providing the output for the B - A Amplitude Function. The Amplitude Function switching circuit (K1 - K3, U2) is controlled by bits PS6 and PS7 which are controlled by the AMPLITUDE FUNCTION setting. Relays K1 through K3 apply the selected A, B or B - A output to the rear panel AMPLITUDE FUNCTION output and to the A to D Converter.

4-39. The dc phase output from the Phase Detector is filtered and applied to the non-inverting input of operational amplifier U8. Amplifier U8 provides a gain of 2.5, making the phase output 50 mVdc per degree. Relays K4 and K5 are used to apply either the phase or delay (from A24) output to the rear panel PHASE/DELAY analog output. Only the phase output is applied to the A to D Converter.

4-40. Local Oscillator.

4-41. The purpose of the Local Oscillator is to generate a 0.1 MHz to 13.1 MHz tracking signal that is mixed with the 0 Hz to 13 MHz input signal in each measurement channel to produce the 100 kHz IF. For the following discussion, the Local Oscillator is divided into two sections: the Reference Generator section and the L.O. Generator section. The Reference generator consists of the VCXO (A11) and the Sampler (A12). The VCXO and Sampler form a phase-locked loop and generate a 19.9 MHz reference signal that is locked to the 1 MHz reference from the Synthesizer. The L.O. Generator, consisting of the L.O. Generator, A10, and L.O. Amplifier, A9, mixes the 19.9 MHz reference signal with the 20 MHz to 33 MHz tracking signal from the Synthesizer to produce the 0.1 MHz to 13.1 MHz L.O. signal.

4-42. VCXO (A11 Schematic No. 9). The purpose of the VCXO (Voltage-Controlled Crystal Oscillator) is to generate a 19.9 MHz reference signal that is phase locked to the 1 MHz reference from the Synthesizer. The VCXO board is divided into two sections: a voltage-controlled Crystal oscillator (U1, Y1, CR5) and a voltage-sensitive filter (Q1, Q2).

Table 4-2. Noise Filter Switching.

Bandwidth	PS1	PS2	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
10 Hz	0	0	0	0	1	1	1	0	1	0	1	0
100 Hz	1	0	1	1	0	0	0	1	0	1	0	1
3 kHz	1	1	1	1	1	1	0	0	0	0	0	0
"1" = High; "0" = Low			"1" = ON; "0" = OFF									

4-43. The voltage-controlled crystal oscillator is a basic 19.9 MHz crystal oscillator containing a crystal (Y1), a varactor diode (CR5) and an active element (U1). The frequency of the oscillator is controlled by the dc bias applied to the varactor diode in series with the crystal. The amount of bias is determined by the control voltage from the Sampler. There are two outputs from the VCXO: a 19.9 MHz square wave (U1 pin 14) which is applied directly to the Sampler and a 19.9 MHz square wave (U1 pin 1) which is filtered by a two-pole bandpass filter (C11 - C14 and associated circuitry) and applied to the L.O. Generator. The signal applied to the L.O. Generator is a 19.9 MHz sine wave. The output impedance is 50 ohms and the output level is approximately 50 mV rms when the output is terminated in 50 ohms at the input of the L.O. Generator.

4-44. The voltage sensitive filter, consisting of Q1, Q2 and associated circuitry, controls the response of the phase-locked loop as a function of the ripple voltage present on the control signal from the Sampler. When the VCXO frequency is 19.9 MHz and is phase locked to a reference on the Sampler board, the control signal is a dc level with only a slight amount of random noise riding on it. The dc level is typically within the range of -1 V to +1 V but will vary somewhat, depending on the accuracy of the 19.9 MHz VCXO crystal, the 1 MHz reference and on circuit parameters. When the control voltage is a pure dc, transistors Q1 and Q2 are off and the filter response is determined by R1, R6 and C3. The response is approximately 200 Hz in this state. When the VCXO frequency varies causing the loop to unlock, the control voltage becomes an ac signal. The frequency of the signal is equal to the difference between the 19.9 MHz reference and the VCXO frequency. The signal amplitude is approximately 6 V p-p. The ac signal turns on Q1 and Q2, causing Q2 to short across R1. The filter response is then determined only by R6 and C3. This broadens the loop response to approximately 50 kHz, allowing the VCXO to track the control signal until the frequency is again locked on.

4-45. The tracking and output signals from the Synthesizer are locked to a reference within the Synthesizer. The Synthesizer reference is used to generate the 1 MHz reference applied to the 3570A. Any frequency deviations in the Synthesizer are, therefore, reflected by the 1 MHz reference. Since the VCXO frequency is locked to the 1 MHz reference, any frequency deviations in the Synthe-

sizer will produce proportional deviations in the VCXO frequency. Thus, the relationship between the Synthesizer frequency and the VCXO frequency remains constant, maintaining the stability of the Network Analyzer.

4-46. Sampler (A12 Schematic No. 9). The purpose of the Sampler is to compare the VCXO signal to a 19.9 MHz reference and produce the voltage used to control the VCXO frequency. The sampler is comprised of a reference generator circuit (Q1 - Q3, U1) and the sampler circuit (Q4, Q5, U3, U4).

4-47. The highly stable 1 MHz reference signal from the Synthesizer (A12 pin 1) is converted to a 5 V p-p square wave by Q1 and Q2, inverted by U1C and applied to a high speed decade divider, U2. The output of U2 is a 100 kHz square wave which is applied to a shaping network formed by the remaining gates in U1 and transistor Q3. The shaping network converts the 100 kHz square-wave input to a pulse train, containing narrow (8 ns) pulses that are rich in harmonics. These pulses are coupled through T1 to the sampler circuit.

4-48. The sampler circuit is essentially a balanced mixer that is used to detect any difference between the 19.9 MHz VCXO frequency at the collector of Q4 and the 195th harmonic of the reference pulse train coupled by T1. The output of sample gate U3 is filtered by C11, amplified by U4 and applied to the VCXO through the voltage-sensitive filter network.

4-49. L.O. Generator (A10, Schematic No. 8). The L.O. Generator is a double-balanced, active mixer which mixes the 19.9 MHz reference from the VCXO with the 20 MHz to 33 MHz tracking signal from the Synthesizer. The upper sideband is filtered out by a low pass filter (L1, L2 C4 - C8), leaving only the 0.1 MHz to 13 MHz difference frequency. This signal is applied to the L.O. Amplifier.

4-50. L.O. Amplifier (A9 Schematic No. 8). The L.O. Amplifier amplifies, filters and splits the 0.1 MHz to 13.1 MHz L.O. signal before it is applied to the A and B Mixer boards. The added filtering minimizes high frequency components that could produce spurious responses in the IF sections. The L.O. PHASE ADJ., C6, is used to zero the phase difference between the two output signals.

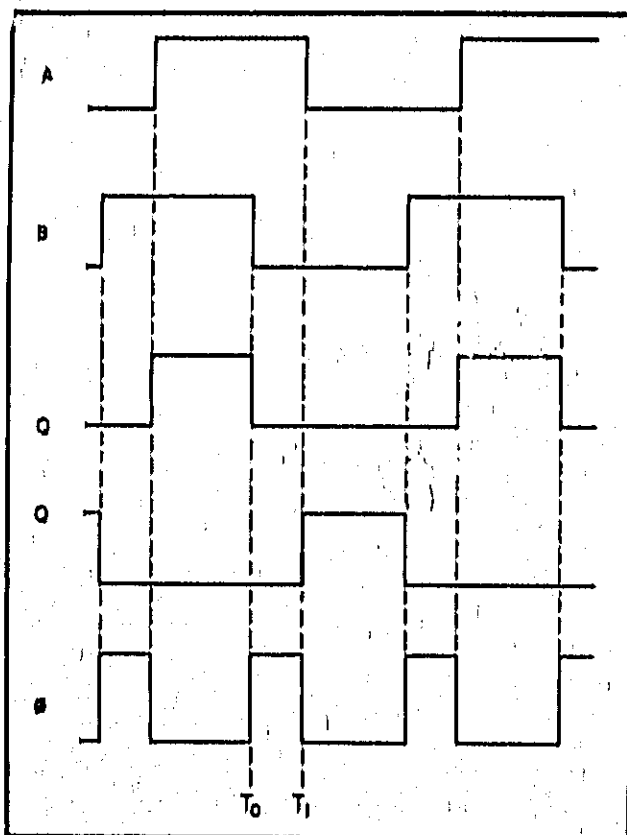


Figure 4-3. Phase Difference + 60 Degrees.

4-51. THE DIGITAL SECTION.**4-52. General Description.**

4-53. The most important function of the Digital Section is providing the internal timing and command signals which operate the instrument. These signals are derived from two types of information inputs. One input is control data and the other input is measurement data. Control data can be

local (Front Panel) or remote (HP-IB). Measurement data is the result of analog-to-digital conversion (see Figure 4-4). The output from the Digital Section is BCD coded information. This information is displayed by the Front Panel and is also accessible to remote devices through the HP-IB. An Algorithmic State Machine, hereafter to be referred to as the ASM, is used to process information within the Digital Section.

4-54. ASM Concepts.

4-55. In order to gain an understanding of the ASM section, we will present some fundamental ASM concepts and relate them to the ASM in the 3570A. We will start with the basic ASM functional devices and add devices to them in a step-by-step fashion until we have a complete Algorithmic State Machine. One device, which has made widespread use of complex ASM machines possible is the ROM.

4-56. The ROM.

4-57. The ROM (Read Only Memory) is the basis for most ASM functions. It is a digital device which is coded by the manufacturer to give a preset output for a specified input (see Figure 4-5). The input to the ROM for ASM applications is called a STATE or ADDRESS. Activating an address input allows a ROM to transfer stored information to the output lines. The address input for ROM's in the 3570A has eight lines. Each line represents one digital bit in the address so there are 2^8 or 256 combinations of input addresses. An address is a location in the ROM, therefore, there are 256 locations which contain data. Each ROM has an enable and an inhibit input which may be used to gate the ROM outputs. The output of the ROM's in the 3570A have four lines. Therefore, each ROM has 256 addresses which contain four bits each. The output from the ROM's are used for two purposes:

- a. To provide a new address for continued ASM operation.

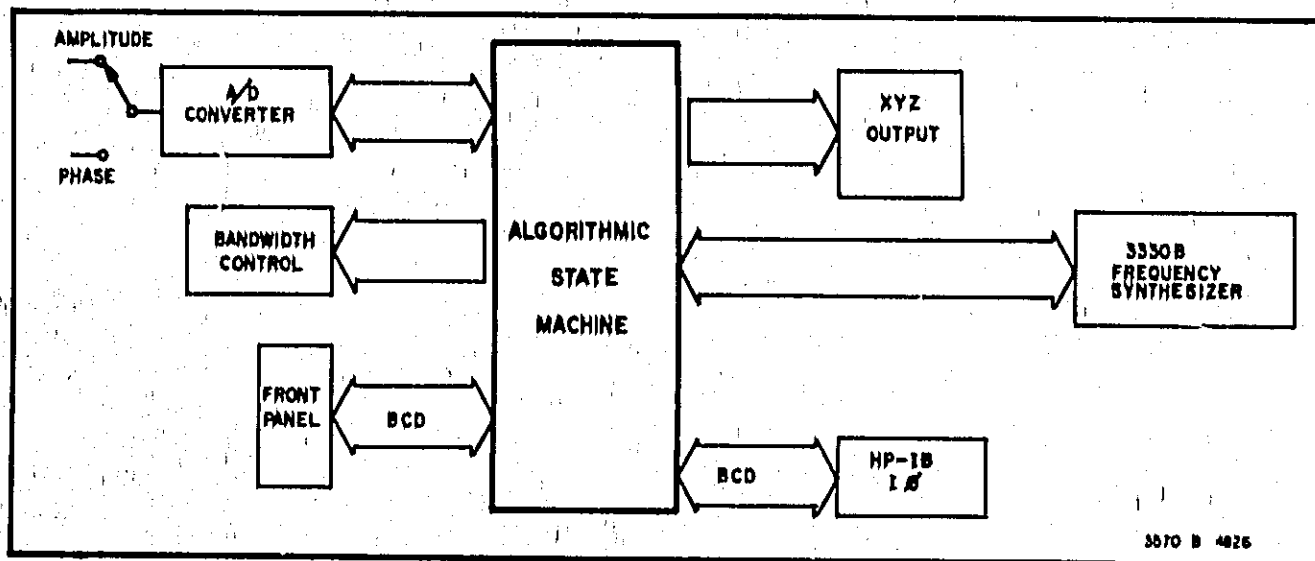


Figure 4-4. The Digital Section.

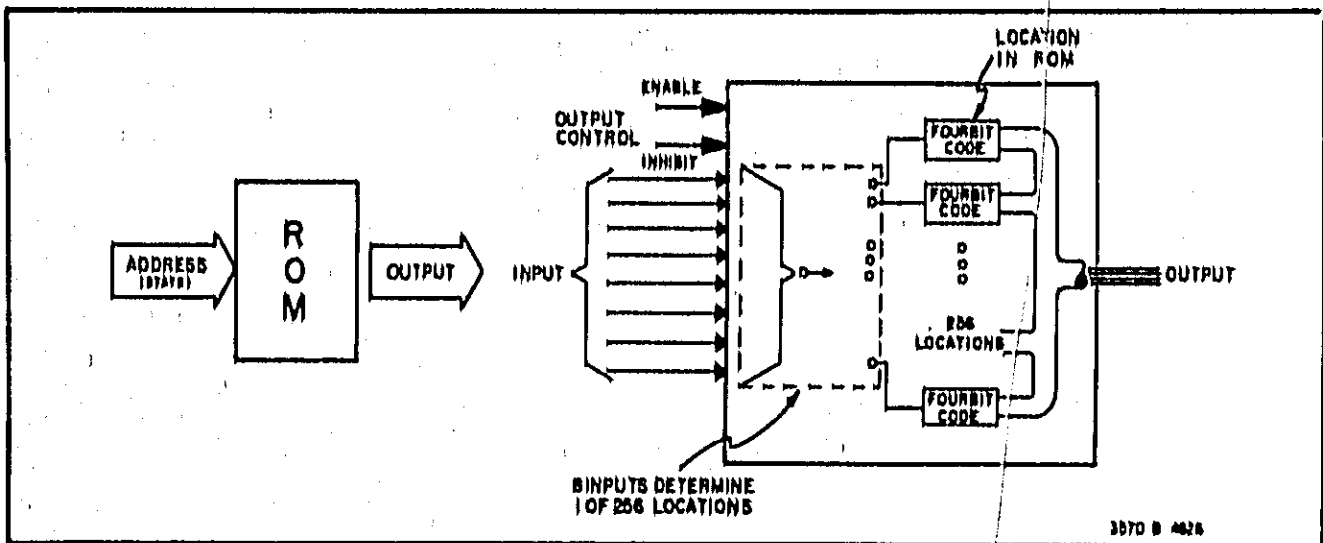


Figure 4-5. The ROM.

b. To provide command signals to operate other devices in the digital section.

To summarize then, each ROM has 256 storage locations. Each storage location contains a four-bit code. For each input (or state), there is a four-bit output and the output is controlled by the enable and inhibit lines. The output may be used for command signals or next state.

4-58. Present State and Next State.

4-59. The Control Section of the ASM is one or more ROM's whose outputs are fed back into their inputs in a controlled sequence (see Figure 4-6). An intermediate device is inserted in the loop to avoid race conditions and provide state control. This device is called the ADDRESS LATCH and is gated by the CONTROL CLOCK. On a signal from the Control Clock, the Latch inputs are transferred to the Latch outputs. Thus, the Latch divides the feedback loop into two sections. The input to the Latch is called the NEXT STATE and the output from the Latch is called the PRESENT STATE. For example, if each location in the ROM contained the address of the next location, the

entire contents of the ROM would pass through the Latch after 256 Control Clock pulses. The PRESENT STATE Bus lines serve two purposes:

a. To provide an address for the Control ROM's.

b. To provide addresses to the Decoding ROM's which produce Instrument Instructions.

The 3570A actually uses three ROM's in the Control Section with their inputs connected in parallel across the Present State Bus. The outputs are used for Next State and Decoding ROM inhibit commands.

4-60. Direct and Alternate Addressing.

4-61. Why do we have direct and alternate addressing and what does it do? Without this modification to the controller, the only type of program we could have would be a fixed sequence loop. (A "program" is an order of events. In ASM, each state constitutes an event.) This loop would only need the clock input to the address latch for it to function. D/A (Direct Alternate addressing) allows us to

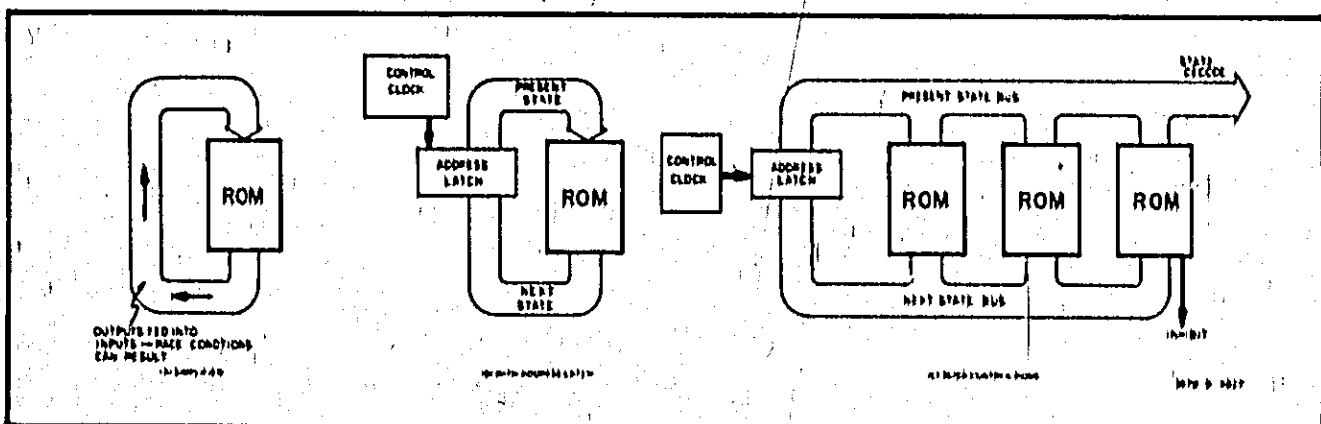


Figure 4-6. Connecting ROM's.

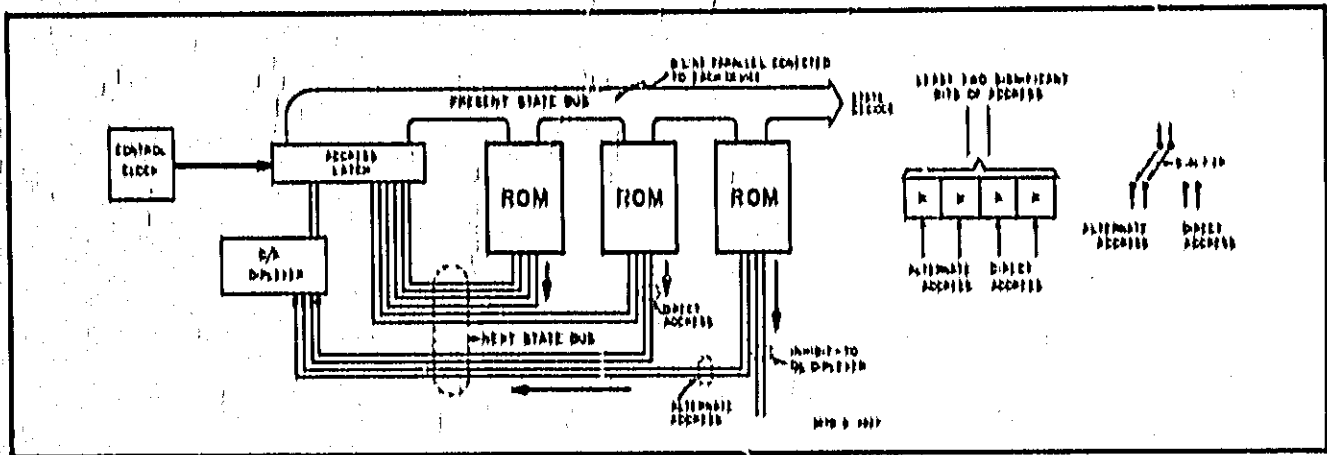


Figure 4-7. D/A Addressing.

change the sequence of the program. For example, suppose we had three operations which we would like our controller to direct. The section of the program which performs an operation is called a subroutine. Without D/A addressing, we would have to execute all three subroutines in some preset order. With D/A addressing, we can perform the subroutines in any order or skip routines. The way this is accomplished is as follows. The six lines that go between the ROM's and the Address Latch form the six most significant bits of the Next State. Four lines from the ROM's go to the D/A DIPLEXER. The D/A Diplexer selects two of

the four lines and outputs these to the Address Latch. These two lines form the least two significant bits of the Next State (see Figure 4-7). Therefore, two of the four inputs to the D/A Diplexer form the Direct Address and the other two inputs form the Alternate Address.

4-62. Qualifier and Data Selector.

4-63. How does the D/A Diplexer select the Direct Address or the Alternate Address? The input which controls the D/A Diplexer is called the QUALIFIER. The Qualifier is

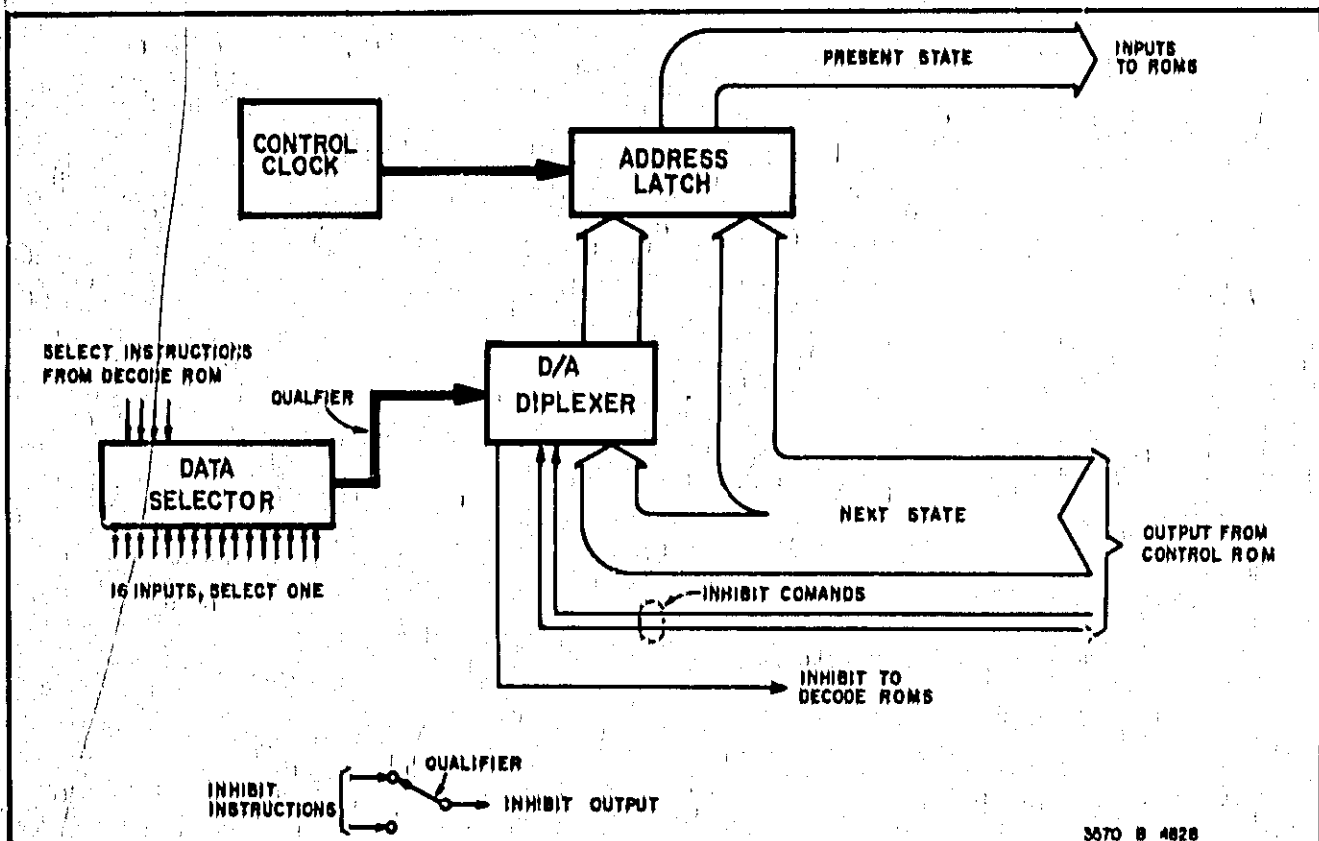


Figure 4-8. Qualifier and Data Selector.

an output from a device called a DATA SELECTOR. The Data Selector is a multi-input IC with one output. One input is selected at a time and lasts for one state period. The Data Selector and its Qualifier output are the means by which the controller checks the status of external functions (see Figure 4-8). The Qualifier has one other function. The D/A Diplexer has an INHIBIT output which goes to the Decoding ROM's. The output is selected from one of two lines which are inhibit commands from the Control ROM's. Therefore, the Qualifier can select a jump to a new subroutine or inhibit an instruction from the Decoding ROM's.

4-64. The Decoding ROM's.

4-65. The Decoding ROM's are the output instruction devices of the ASM (see Figure 4-9). The ROM's are connected in parallel across the Present State Bus. Unlike the control ROM's the Decoding ROM's can be inhibited from outputting instructions. This could take place during a jump to a new subroutine. Since each ROM has four outputs, there can be sixteen different combinations of instructions. For instructions which are used often and in conjunction with other instructions, the output from the ROM may suffice alone. For instructions which are used less frequently, the outputs from the ROM may be connected to a MULTIPLEXER. The Multiplexer will provide sixteen mutually exclusive outputs. It is important to remember that all ROM outputs and each Multiplexer output last for one State Interval (one Control Clock period). One significant function of the outputs from the Decoding ROM's is to control the REGISTERS.

4-66. The Registers.

4-67. The ASM which we have built so far can input information in the form of Qualifiers and it can output informa-

tion through its Decoding ROM's in the form of instructions. Another device which works in conjunction with both the input and output of the ASM is the Register. The Register has many uses. Among these are collecting data at a common point for testing, doing mathematical manipulation of data, and maintaining temporary storage of data. Some registers have parallel input and output capabilities, but all registers have an input and/or output with the Bus System (a line which allows serial transfer of data). The Registers input and output data with the Bus System in a bit serial mode. All register interfacing with the Bus System is accomplished during one Control Clock period (see Figure 4-10). A REGISTER CLOCK is used to provide a common synchronous signal for the registers to shift their data onto the Bus System or accept data from the Bus System.

4-68. The Register Clock and Control Clock.

4-69. We have already established that each state last for one Control Clock period. The length of the Control Clock period depends on the number of Register Clock pulses which occur during that state. Therefore, the Control Clock period can last from one to sixteen Register Clock periods (see Figure 4-11). The number of Register Clock pulses is controlled by a presettable counter in the Register Clock Control Circuit. The presettable counter circuit is fashioned so that it automatically clears itself when sixteen counts have occurred. For example, in order to count one Register Clock pulse, the number fifteen is entered and the counter presets itself to that input. If four Register Clock pulses were needed, the input to the counter would be set to twelve. The number which is used for presetting is an output from a Decoding ROM in the ASM. The Register Clock output is connected to a control circuit for each register.

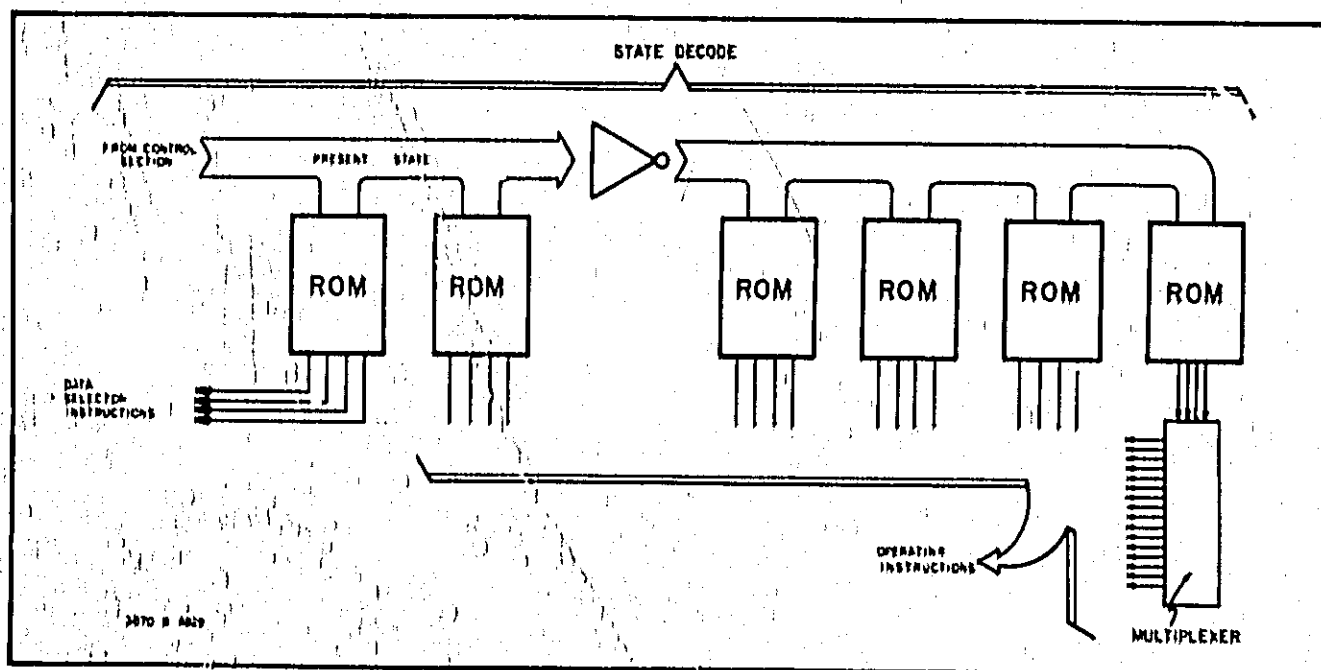


Figure 4-9. The Decode ROM's.

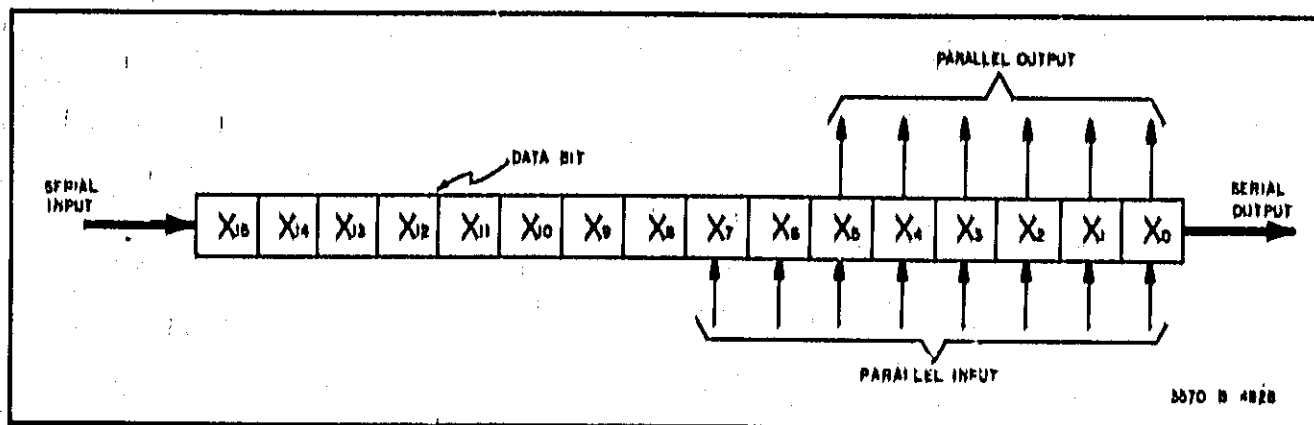


Figure 4-10. Example Register.

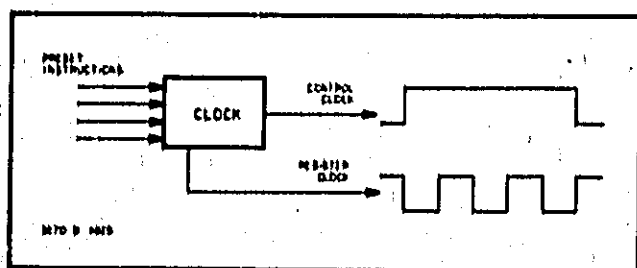


Figure 4-11. Register Clock.

4-70. The Register Control Circuits.

4-71. The Register Control Circuits convert instruction commands into operational signals for register functions. The Control Circuits are easily identified by finding the Bus Inputs and/or outputs. The other inputs to the Control Circuits are the Register Clock and the Register Instruction Commands. During the Control Clock period, the register can transfer data over the Bus System.

4-72. The RST Bus System.

4-73. The Bus System is divided into three sections (see Figure 4-12). The three buses are connected through the ALU (Arithmetic and Logic Unit). The output from the ALU is the T Bus which is the serial input to the registers. The S Bus is the serial output from all registers except the A Register which has a serial output. The R Bus is the serial output for the A Register alone. The R Bus and the S Bus form the inputs to the ALU. If data is to be transferred between two registers via the Bus System, the following events will take place. The serial input and output commands must be issued to the respective Register Control Circuits. The Register Clock is set for the number of register bits to be transferred. If no logic operations are to be performed on the data, a connect S Bus to T Bus command will be issued to the ALU. These events will take place simultaneously for one Control Clock period. Now when the Control Clock is activated, the Register Clock will begin counting. With each Register Clock pulse, a data bit is right shifted from one register through the S Bus, ALU, and T Bus to the input of the receiving register. You might

imagine a train of data bits leaving one register on the right side and entering the receiving register on the left side, the data progressing to the right in both registers. If both registers could hold sixteen bits of data, then the complete information transfer would take place in sixteen Register Clock counts. After the transfer has taken place, the Control Clock will return to its initial point. So that information may be retained for repeated examination, some registers have a Control Circuit which allows bits to be recirculated internally (see Figure 4-12). For this type of register, data bits reenter internally the left side of the register (serial input) as the register is shifted right onto the appropriate bus without accepting information on the normal register input line. The register could be completely rotated with 16 Register Clock pulses.

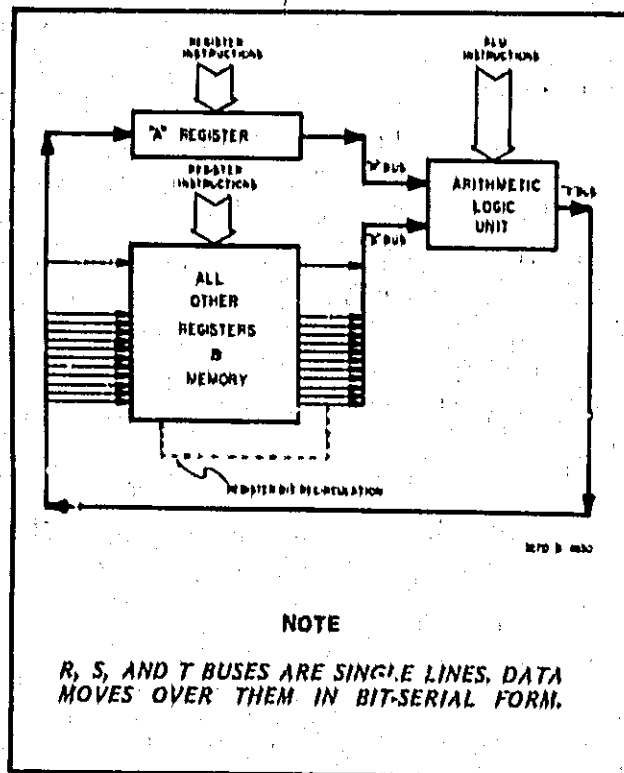


Figure 4-12. RST Bus System.

4-74. The ALU.

4-75. The ALU can perform eight functions. These are: UTS (units to S Bus), IOR (Inclusive OR), R-S (subtract S from R), S-R (subtract R from S), XOR (exclusive OR), ADD (S + R), STT (connect S Bus to T Bus), IOR-CCY (Inclusive OR and clear carry). These mathematical operations are performed on the R and S Bus data bits as they are clocked through the ALU by the Register Clock. The ALU section is composed of a ROM, Diplexer, and a Carry Flip-Flop. The ROM in the ALU is like the other ROM's in the 3570A. It has eight inputs and four outputs. Of the eight inputs, seven are used. Four of the seven are ROM instructions from the decoding section of the ASM. The R Bus, S Bus, and Carry form the remaining inputs. For each Register Clock pulse, a data bit from the R Bus, a data bit from the S Bus, and data bits from the five other inputs form the address for the ROM. As the R and S Buses change their logic states, the address input to the ROM changes accordingly. Thus, for every possible combination of R, S, Carry, and instruction bits, there is a ROM output. Of the four outputs, three are used. One is the ALU output which is the mathematical function of R and S. It is connected to a Diplexer which is controlled by ALU instructions. The Diplexer connects either the ALU output or the S Bus to the T Bus. The other two outputs from the ROM operate the Carry flip-flop (see Figure 4-13).

4-76. Add and subtract operations when executed by the ALU may result in an overflow or underflow. The Carry flip-flop output is also one of the inputs to the Data Selector. The Carry output will indicate when the value of a number, which results from a mathematical operation, is too large or too small for the ASM to use, for example, for the number exceeding sixteen bits in magnitude. A typical mathematical operation would be performed if offset data were entered from the front panel or from the HP-IB. The offset would be added or subtracted from the computed value of Amplitude or Phase. If the number does not produce a Carry output, then the results of the ALU operation may be stored in Memory for future use.

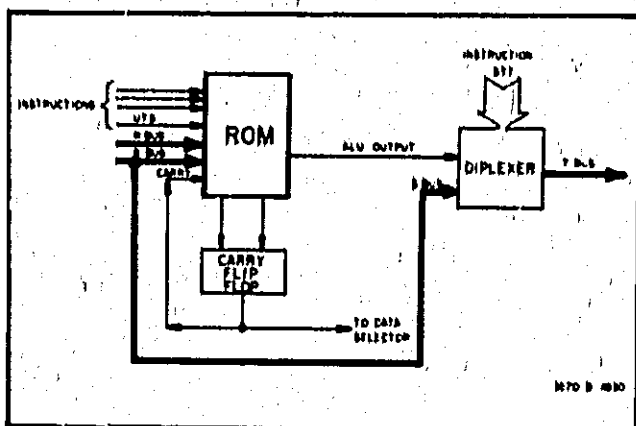


Figure 4-13. The ALU.

4-77. Memory.

4-78. Memory is used when storage of data is needed for an extended period of time. The Memory in the 3570A is a shift register memory which has an input from the T Bus and an output on the S Bus. The Memory is composed of eight registers which are loaded in a manner similar to the other serial registers previously discussed. Since the Memory has only one input and one output, an addressing device is needed to direct the incoming data and outgoing data to and from the correct register. The P Register serves as the memory address storage register and is itself connected to both the T and S Buses. The P Register contents are connected in parallel to the memory address inputs (see Figure 4-14). In order to have the Memory input or output data, we need:

- An input or output instruction.
- A Memory address available in the P Register.
- The correct number of Register Clock pulses to strobe the data onto the S Bus and/or off of the T Bus.

If we wanted to determine how many Register Clock pulses were used or where the information was routed to, we would consult a flowchart.

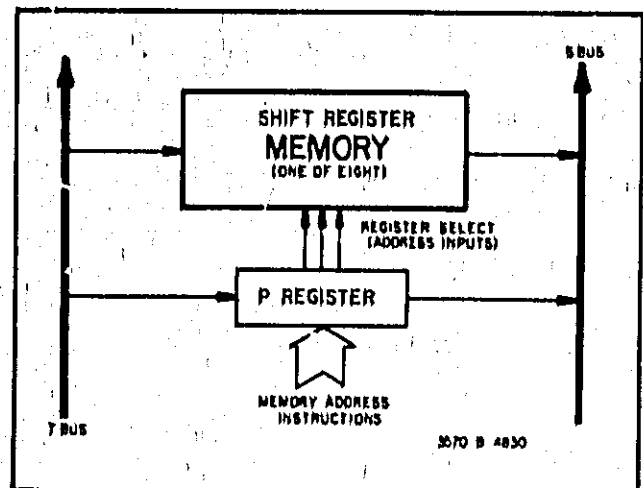


Figure 4-14. The Memory.

4-79. Flowcharting.

4-80. The flowchart is the essence of ASM operation. When used in combination with the electrical schematic, the flowchart can be an important tool for troubleshooting ASM malfunctions. The flowchart indicates the sequence of operations and the relative timing of events in the Digital Section. We will use the explanation of flowcharting as a brief review of the ASM concepts previously discussed. As an aid in visualizing how information flows in the ASM section, refer to the Digital Block Diagram.

4-81. Symbols.

4-82. The two main symbols in flowcharting are the rectangle and the diamond (see Figure 4-15). The rectangle indicates whether the present state is to be executed and also indicates the direct and alternate next states.

4-83. The Rectangular Symbol.

4-84. We now know that a ROM has an input address which we call a state. This state input is called the present state and is indicated on the flowchart above each rectangle on the right as an octal number. This octal number has three digits which correspond to the eight input lines to each ROM in the Control and Decode section of the ASM. The ROM is a memory device which has a four-bit output for each state. The ROM outputs can be instructions or part of the next state addresses. The instructions are indicated inside the rectangle. The next states are the direct state and the alternate state. These are indicated adjacent to the rectangles following the diamond symbol.

4-85. The instructions are two to four letter mnemonics which indicate an operation which is to be performed. See Figure 4-15 example (b). In example (b), the instructions are ITS, STT, and TTQ. They indicate that the I register is to be outputted onto the S Bus (ITS), the ALU will connect the S Bus to the T Bus (STT), and the T Bus will be inputted to the Q register (TTQ). Register Clock pulses are needed to strobe the data from the I register, through the Bus System, to the Q register. The number of Register Clock pulses is indicated in the upper right-hand corner of each rectangle. In the example, the number of clock pulses is six. All operations described in the rectangle occur simultaneously for the indicated state. We know that a state, when executed, lasts from one to sixteen Register Clock pulses. But what if the state is not executed? To determine whether the state will be executed or not is a function of the qualifier.

4-86. The Diamond Symbol.

4-87. The qualifier is the output from the Data Selector. The input to the Data Selector is indicated inside the diamond. In Figure 4-15 example (b), the qualifier is a SWP (sweep) signal from an external instrument. If the qualifier is true, indicated by the (1) on the right side of the diamond, the D/A Diplexer will select the alternate address. If the qualifier is false (0), the D/A Diplexer will select the direct address.

4-88. There is also a shaded area on the right side of the diamond. This is the instruction inhibit indicator. See Figure 4-15 example (a). If the qualifier is true, the instruction in the preceding rectangle will be inhibited from executing. This will make the state last for one Register Clock period. The information transfer in example (b), between the I and Q register would not take place. The inhibit indicator can also be at the bottom of the diamond. This would mean that the instruction in the preceding rectangle would be inhibited if the qualifier were false. If the rectangle or

diamond does not contain information inside, the state or qualifier is non-operational. If the rectangle does not contain information, the state will last for one Register Clock period.

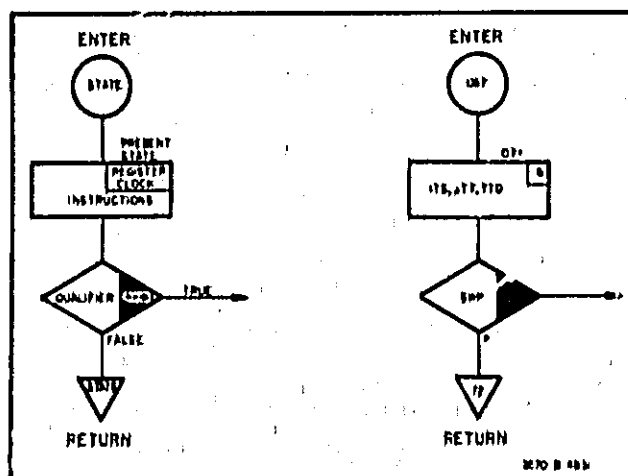


Figure 4-15. Flowchart Symbols.

4-89. We can now define ASM. An algorithm is a step-by-step procedure for solving a problem (the routines of the flowchart). A state is one or more instructions which form a step in the algorithm and last for a defined period of time (the instructions in the rectangles and the Register Clock counts found on the flowchart). A machine is an electronically operated device for performing a task (in this case operating the 3570A).

4-90. Controlling and Processing.

4-91. The ASM in the 3570A controls the instrument functions and processes measurement data. To control the instrument, the ASM generates command instructions which are derived from the Front Panel Switches or from the HP-IB inputs. To process measurement data, the ASM must convert signals from the Output Buffer of the Analog Section into digital data. Depending upon the mode of operation selected, the data may or may not be modified before being converted into Binary Coded Decimal (BCD) for output to the Front Panel Displays. For output to the HP-IB, the BCD data must be converted into ASCII coded data (see Figure 4-16).

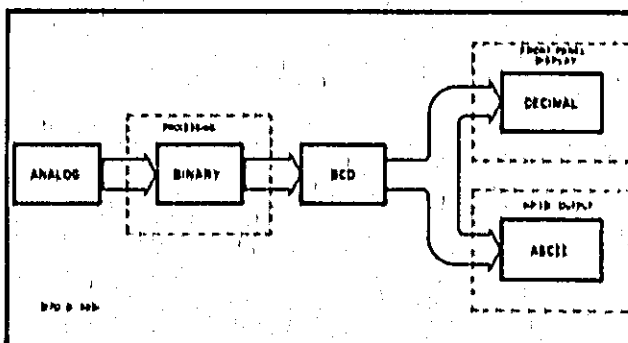


Figure 4-16. Conversion Sequence.

4-92. Front Panel Inputs.

4-93. The Front Panel Switches are enabled when the 3570A is in the Local Mode of operation. The switches are directly connected to the Program Storage (PS) Register. The PS Register is comprised of two four-bit shift registers. The two shift registers have both serial and parallel inputs and outputs. The serial input is the T Bus and the parallel inputs are the Front Panel Switches. The serial output is the S Bus and the parallel outputs are the Control Data Lines (see Figure 4-17). The Offset and Limit Sweep Restart switches are not connected to the PS Register and are used as one of the means to set the Data Flag. Delay Switches (Options 002, 003) are directly connected to the Delay (D) Register which operates in a manner similar to the PS Register.

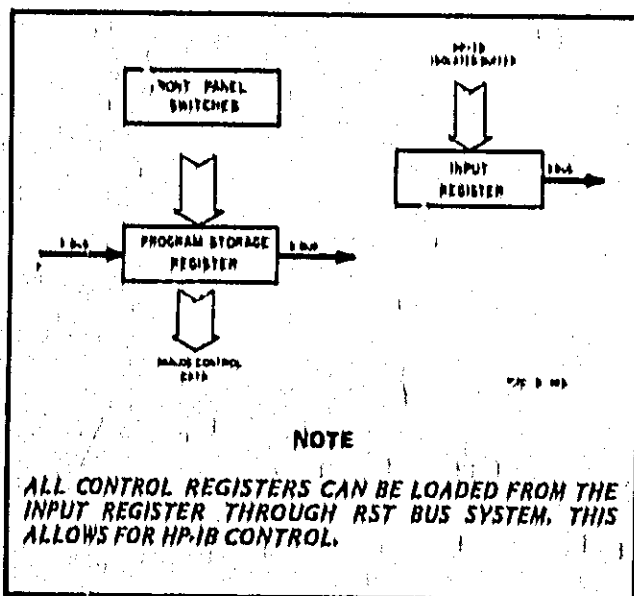


Figure 4-17. Inputs to the ASM.

4-94. HP-IB Data Inputs.

4-95. The 3570A must be in the Remote Mode of operation in order to receive data from the HP-IB (see Section 1.1, Paragraph 3-172, for a description of remote programming). Each time an ASCII coded character is transmitted over the HP-IB, the Data Routine is initiated and the character is loaded into the Input (I) Register. The contents of the I Register are decoded and shifted into the appropriate register depending upon whether the information is control data or numerical data (see flowcharts for a description of the data processing routines).

4-96. Analog-to-Digital Converter.

4-97. The A/D converter in the 3570A must convert an analog signal into its binary equivalent. The technique used is called Successive Approximation.

4-98. Successive Approximation.

4-99. Suppose there is an unknown dc voltage which we

would like to measure. One of the many ways to measure this voltage would be to produce a known voltage and compare it to the unknown voltage by use of a comparator. The comparator is a device which produces an output voltage when the input voltages are not equal (see Figure 4-18).

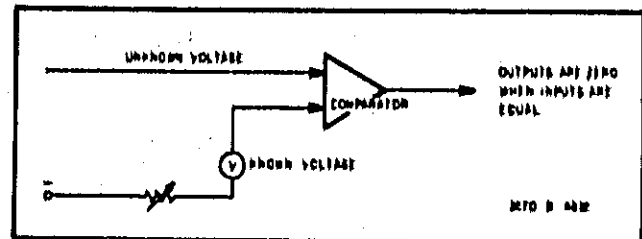


Figure 4-18. The Comparator.

4-100. To determine the magnitude of the unknown voltage, the known voltage is adjusted until the output from the comparator is zero. This type of voltage level measurement lends itself well to digital applications. If we detect the comparator output and produce the known voltage using digital techniques, the unknown voltage can be measured in terms of digital numbers. We can produce the known voltage by summing voltages derived from binary weighted switches used in conjunction with a resistive ladder network.

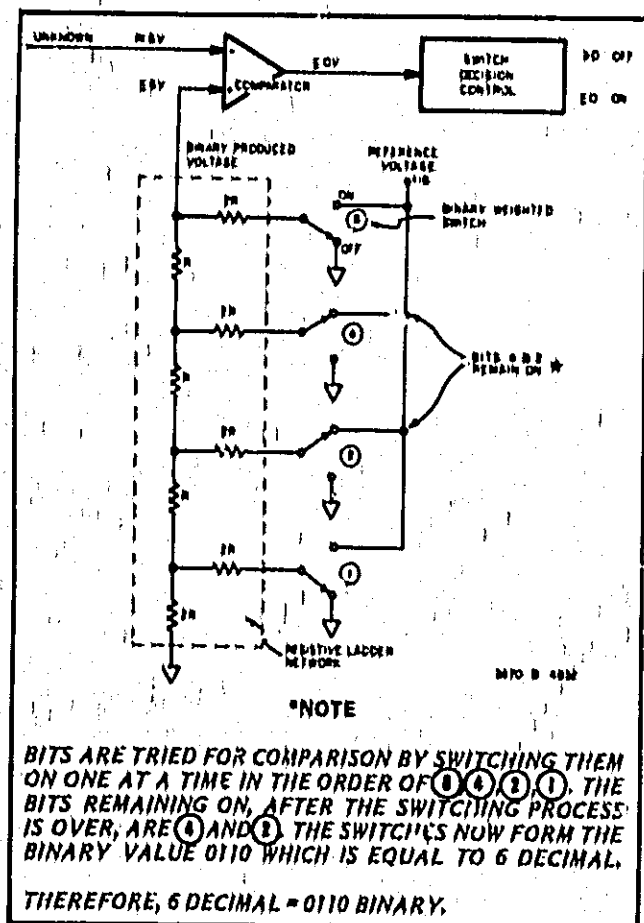


Figure 4-19. An Example of Successive Approximation.

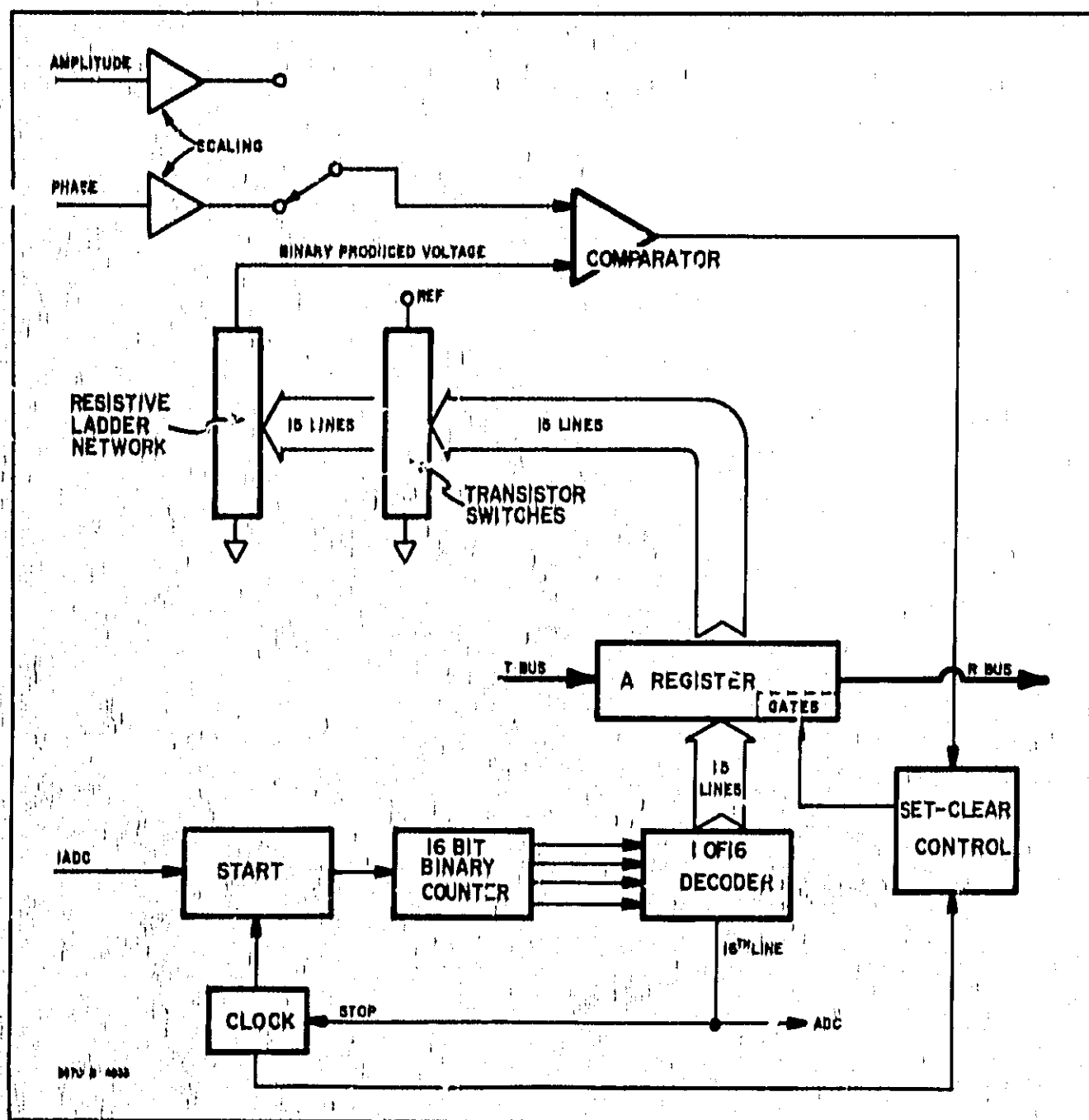


Figure 4-21. 3570A A/D Converter.

4-107. Binary to BCD Conversion.

4-108. The Add 3 Algorithm is the process by which the ASM converts binary to BCD. What is the difference between binary and BCD (Binary Coded Decimal)? Let us take the number 23 decimal for an example. In binary, the number 23 is written 10111. In BCD, the number 23 is written 0010 0011. In BCD we can see that it takes four binary bits to represent one decimal digit. In order to convert from binary to BCD, the Add 3 Algorithm is carried out in a shift register as data is being shifted in.

The shift register is partitioned into sections containing four bits each. Each section represents a BCD numeral.

4-109. We will use Figure 4-22 to explain the Add 3 Algorithm conversion technique. To use the Algorithm, the input binary number is shifted out of an eight bit register and into the B Register which can implement a binary add three. The binary add three is carried out on each of the four-bit BCD sections. The conversion is basically a two-step process which is repeated for as many times as there are bits to be converted. The first step requires that

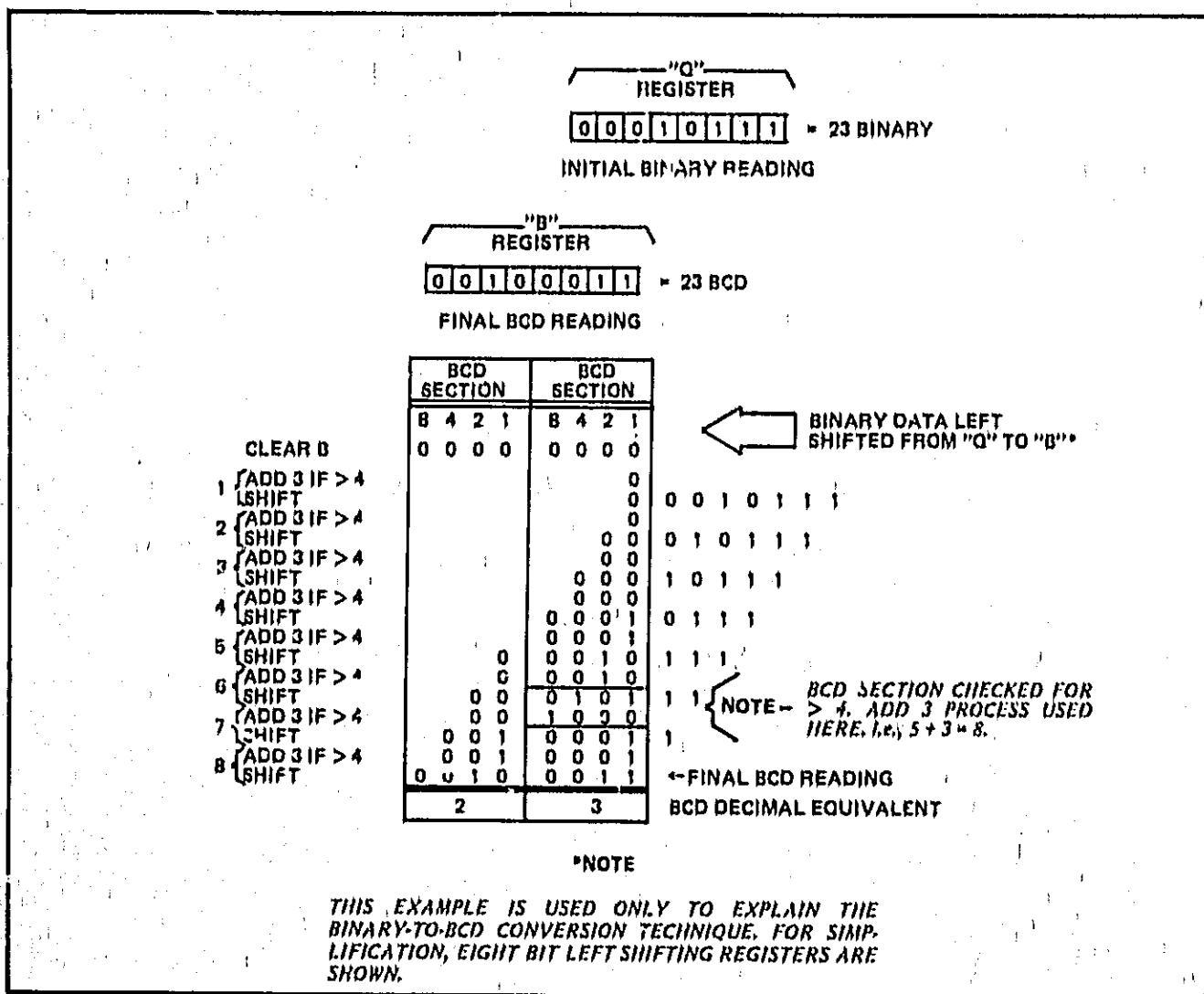


Figure 4-22. An Example of Binary-to-BCD Conversion.

each of the BCD sections be checked to determine if the binary number within that section is greater than four. If the number is greater than four, three is added to it. If the number is less than four, no action is taken and the number remains the same. The second step involves shifting a new binary bit into the register. In Figure 4-22, the add-shift process is carried out eight times. The conversion process will be finished when the binary number is completely shifted into the B Register. The number will now be available for parallel output to other devices as BCD.

4-110. The 3570A uses this same process but with two modifications (see Figure 4-23).

a. The 3570A cannot left shift data between registers. To overcome this problem, the binary data is first shifted into the A Register. Then, the Q Register is parallel loaded with the eight most significant bits from the A Register, but in reverse order. The Q Register is then shifted into the BIDEDEC (Binary-Decimal) Register and the A Register is recirculated for eight bit positions. The Q Register is again parallel loaded from the A Register and shifted into the

BIDEC Register. This process will transfer sixteen bits of data between the A Register and the BIDEC Register with the most significant bit first.

b. The BIDECE Register is constructed so that the add operation can take place as bits are right shifted into the Register. The add three operation in the BIDECE Register is performed by ROM's. The four binary bits in each BCD section are always available as a ROM input address. The ROM has four outputs which are used as parallel inputs to the same BCD section of the BIDECE Register. The ROM outputs will be the same as the ROM inputs if the binary value of the inputs is four or less. If the binary value of the inputs is five or greater, the ROM output will be a binary three greater than the value of the inputs (see Figure 4-24).

4-111. The sequence for binary-to-BCD conversion begins with the BDEC Register set to zero. A load command and a shift command will be given for each bit shifted into the register. The load command parallel loads each BCD section with the ROM outputs. Then the shift command right shifts

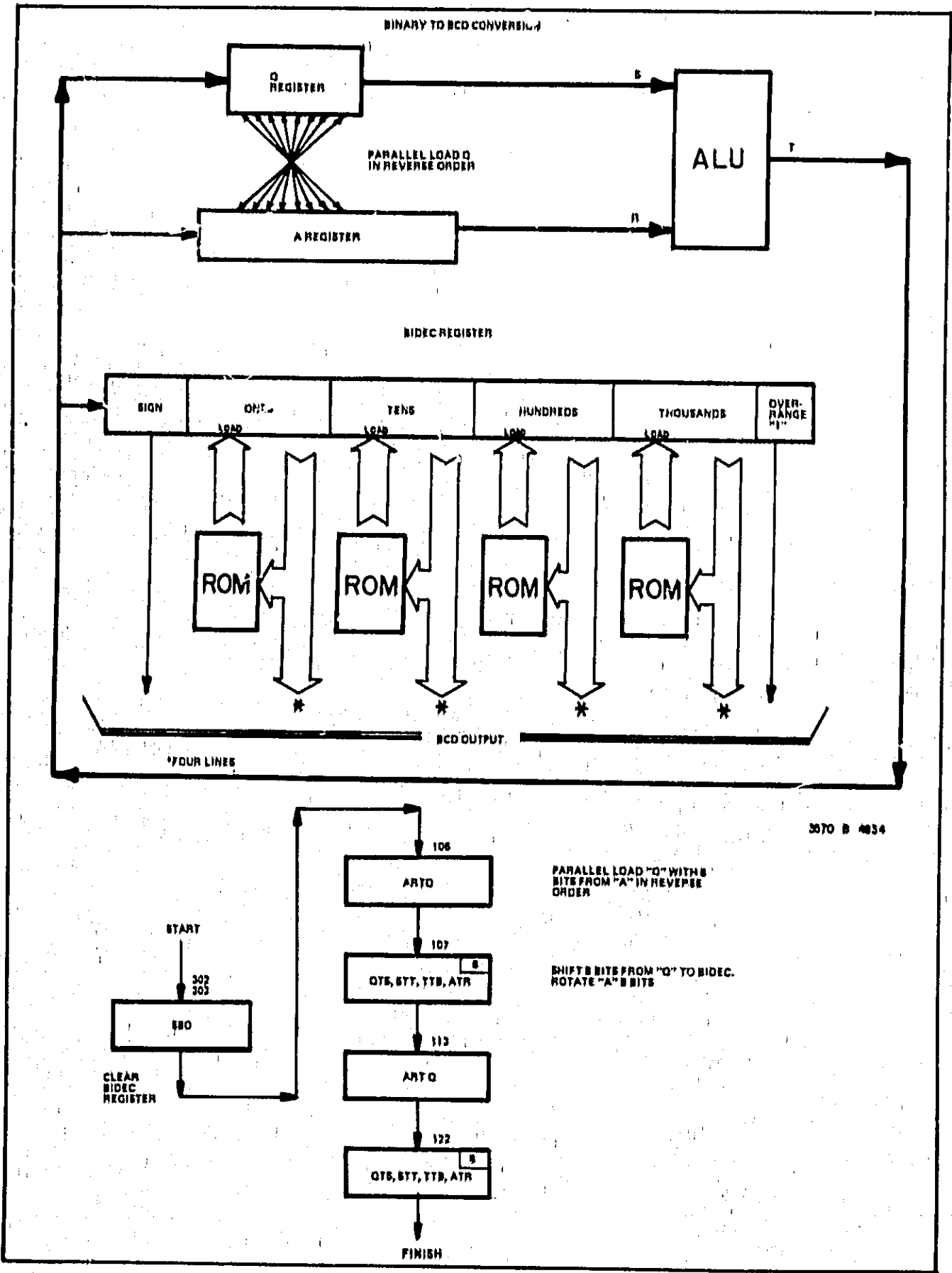


Figure 4-23. Binary-to-BCD Conversion.

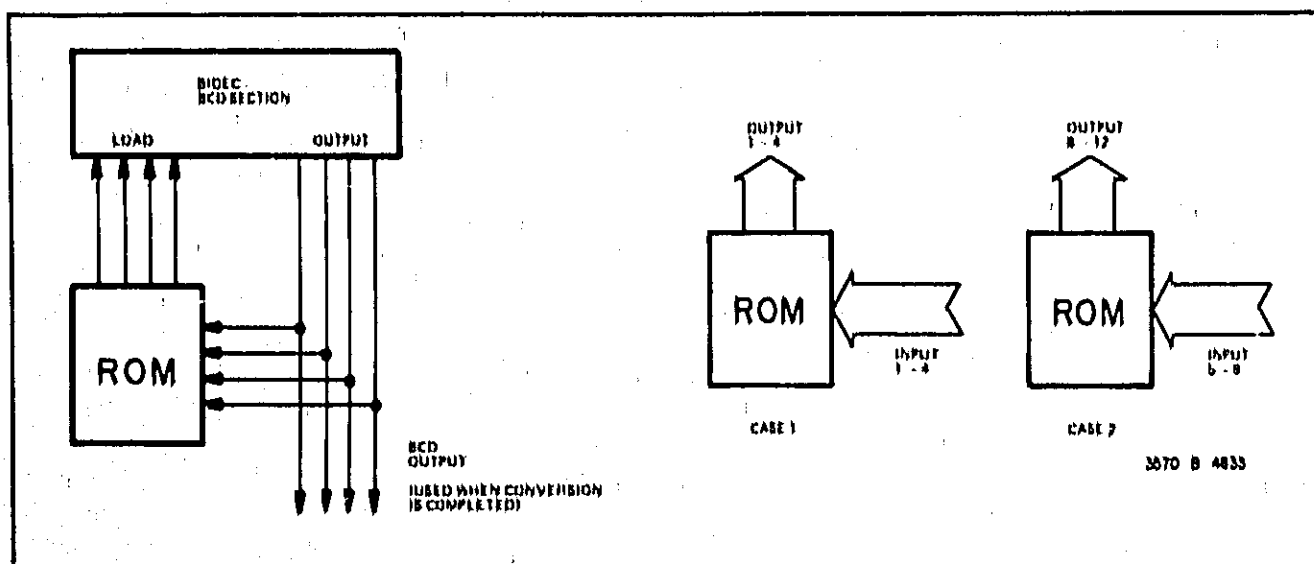


Figure 4-24, BIDEc Conversion ROM's.

the register one bit position (see Figure 4-25 which shows how a binary number is right shifted into the BIDEc Register). The control circuit for the BIDEc Register gives the commands to load and shift for each Register Clock pulse. After the sixteenth clock pulse, the BCD data will be ready for the Front Panel displays and the BCD-to-ASCII converter.

4-112. BCD-to-ASCII Conversion.

4-113. The HP-IB transfers data between devices in the form of ASCII coded characters. In order for the 3570A to communicate on the HP-IB, it must convert the BCD data to ASCII data. What is ASCII code and how can it be generated from BCD? ASCII is an alphanumeric code, which means it is composed of the alphabet, special characters, and numerics. There is also a provision in the code for special instructions such as CR (carriage return) and LF (line feed) which indicate the end of transmission of a string of characters (see Table 4-4 for ASCII output codes which apply to the 3570A).

4-114. ASCII characters are transmitted over the HP-IB as seven bit binary codes. In order to convert BCD numerics to ASCII numerics, two bit positions are added to the four bit positions of BCD (see Table 4-5).

4-115. The 3570A transmits ASCII characters over the HP-IB using fixed formats which correspond to the mode of operation. (The mode of operation is determined by the front panel switch settings.) The sequence of characters, in the format, is determined by a ROM which uses a sixteen bit binary counter for one of the inputs. The binary counter will cause the ROM to address sixteen different locations. Therefore, the counter can supply all the addresses for the characters to compose an output string (see Figure 4-26). The counter is reset after an amplitude reading, phase reading, or delay reading. Four ASM operating instructions are the other inputs to the ROM.

4-116. It is now easy to imagine that the ROM has many strings of characters which are selected by both the mode inputs and the counter inputs. The mode inputs determine the string of characters and the counter inputs determine the character in the string.

4-117. The ROM has eight output lines. Four of the outputs are used for both character generation and multiplexer select lines. The function of the four output lines is determined by the diplexer select line. The multiplexer inputs are arranged so that each of the BCD value bits are grouped together. When a numeric character is needed in the output sequence, the ROM selects the correct combination of multiplexer inputs which are routed through the four bit diplexer. These outputs, from the diplexer, form four of the six bits needed for an ASCII numeric. The other two bits are supplied from the remaining ROM outputs. If a character other than a numeric is needed, the diplexer select line is set so that the four outputs from the ROM are routed directly through the diplexer. These four outputs, together with the remaining ROM outputs, are used for character generation.

4-118. All HP-IB inputs and outputs are light isolated to permit floating measurements by the 3570A.

4-119. Measurement Control and Timing.

4-120. The Measurement Control circuit is comprised of a Measurement Flag flip-flop, an Internal Clock, a clock control circuit, and a Z Axis modulation circuit (see Figure 4-27).

4-121. The Measurement Flag flip-flop is set by a (L)SMF instruction or by the Internal Clock and reset by a (L)RMF instruction. The Internal Clock operates at 4 Hz/sec and is itself controlled by a control circuit which has multiple inputs. The inputs to the control circuits depend on the mode of operation of the 3570A. Thus, the Measurement

Table 4-4. ASCII Output Codes.

ASCII Character	Octal Code
0	060
1	061
2	062
3	063
4	064
5	065
6	066
7	067
8	070
9	071
.	068
E	105 *
+	063
-	065
?	077
CR	015
LF	012

* TO GENERATE NUMBERS ONLY REQUIRES SIX BINARY BITS; OTHER CHARACTERS MAY REQUIRE SEVEN BINARY BITS.

Table 4-5. BCD-to-ASCII Conversion.

NOTE
SEVENTH BIT POSITION NOT SHOWN.

Decimal	ASCII		X	X
	Added Bits	BCD		
0	1 1	0 0 0 0	6	0
1	1 1	0 0 0 1	6	1
2	1 1	0 0 1 0	6	2
3	1 1	0 0 1 1	6	3
4	1 1	0 1 0 0	6	4
5	1 1	0 1 0 1	6	5
6	1 1	0 1 1 0	6	6
7	1 1	0 1 1 1	6	7
8	1 1	1 0 0 0	7	0
9	1 1	1 0 0 1	7	1
	X	X		
	Octal			

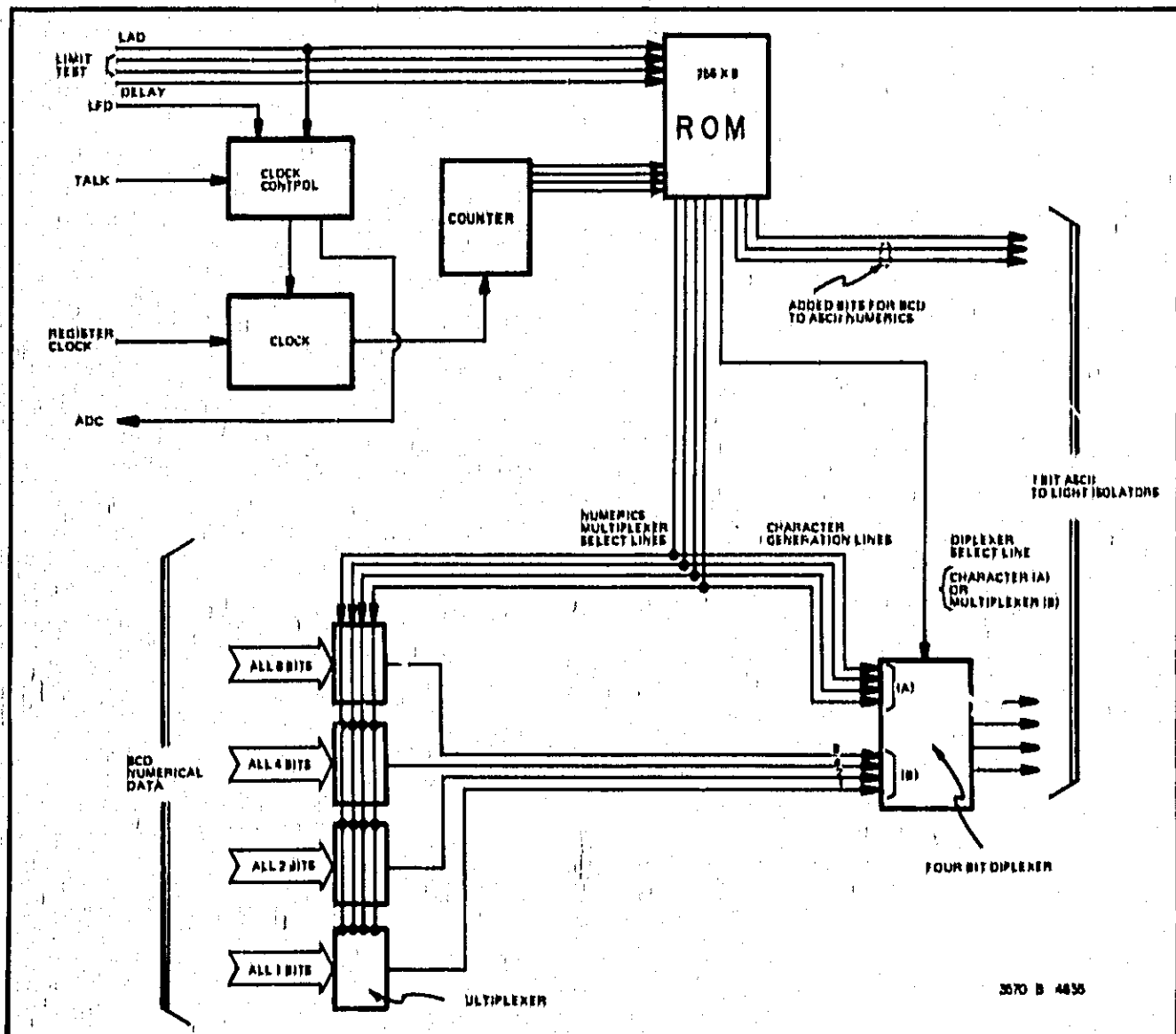


Figure 4-26. BCD-to-ASCII Converter.

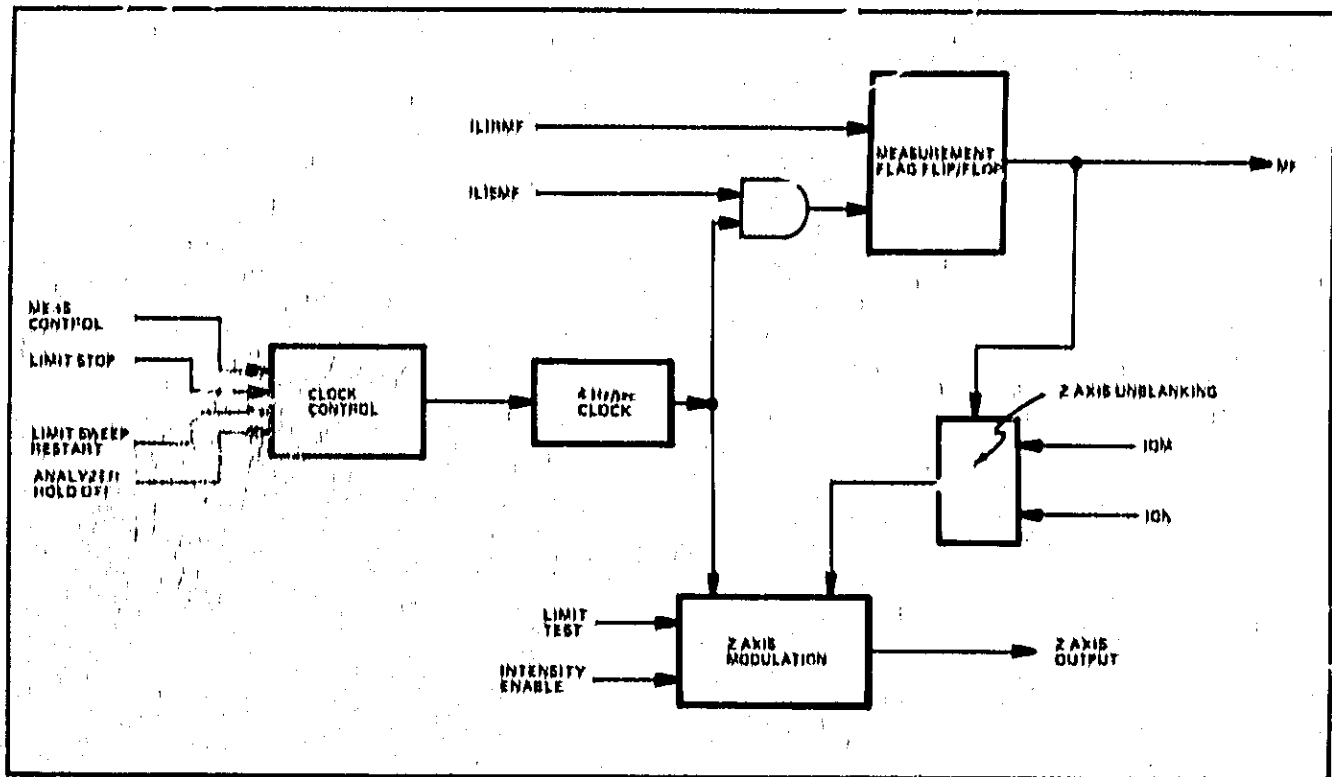


Figure 4-27. Measurement Control and Timing.

WARNING

These servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

Table 5-1. Recommended Test Equipment.

Instrument Type	Required Characteristics	Model
Frequency Synthesizer (See Note 6)	Frequency Range: 50 Hz to 13 MHz Amplitude Range: 0 dB to +100 dB Hewlett-Packard Interface Bus Capabilities	-hp- 0320A/B -hp- 0330A/B
AC/DC Digital Voltmeter	DC Function: Full Scale Ranges: 100 mV through 100 V Resolution: 5-digits Input Resistance: 10 M Ω Accuracy: 0.1 % of reading AC Function: Response: true rms Frequency Range: 50 Hz to 1 MHz Full Scale Ranges: 1 V, 10 V Resolution: 5-digits Input Impedance: 1 M Ω , 100 pF Accuracy: ± 0.16 % to 100 kHz ± 2 % to 1 MHz	(-hp- 3450B) or 3455 or 3465
Variable Attenuator (See Note 1)	Attenuation: 100 dB in 10 dB steps Frequency Range: 50 Hz to 13 MHz Impedance: 50 Ω Accuracy: 0 dB to 20 dB: ± 0.1 dB 20 dB to 80 dB: ± 0.2 dB 80 dB to 100 dB: ± 0.5 dB	(-hp- 355D) 2 required
DC Voltmeter	Range: 1 mV through 100 V Input Resistance: 10 M Ω Accuracy: ± 1 % of range	(-hp- 412A)
Oscilloscope	Sensitivity: 0.005 V/div Sweep: 0.05 μ sec/div to 0.1 sec/div	(-hp- 180A)
Voltage Divider Probe (for oscilloscope)	Division Ratio: 10:1 Impedance: 10 M Ω , 10 pF	(-hp- 10004B)
Oscilloscope (variable persistence)	Vertical Sensitivity: 20 mV/div to 10 V/div Horizontal Sensitivity (EXT): 1 V/div Frequency Range: dc to 100 kHz	(-hp- 1B1A)
Electronic Counter	Frequency Range: 50 Hz to 33 MHz Resolution: 8-digits Sensitivity: 0.1 Vrms	(-hp- 5245L)
DC Power Supply	Range: 0 - 20 V Ripple and Noise (rms/p-p): 40 μ V/100 μ V Resolution: .002% + 100 μ V	-hp- 6101A
Thermal Converter (See Note 2)	Frequency Range: 50 Hz to 13 MHz Frequency Response: ± 0.05 %, 50 Hz to 13 MHz Input Impedance: 50 Ω (or 75 Ω) Maximum Input Voltage: 1 Vrms Maximum Output Voltage: 7.5 mVdc	(-hp- 11050A for 50-ohm systems) (-hp- 11050A/H01 for 75-ohm systems)
Coax Cable (See Note 3)	Impedance: 50 Ω (50-ohm systems) 75 Ω (75-ohm systems) Length: 500 ft. to 1,000 ft. Connectors: BNC	HQ58A/U HQ59A/U
Terminations	(2) 50-ohm Feed-Thru (50-ohm systems) (2) 75-ohm Feed-Thru (75-ohm systems)	-hp- 11048C -hp- 11094A
Impedance Adapter (See Note 4)	50 Ω to 75 Ω	(See Figure 5-2)
Resistor	R1: ad film 453 Ω	-hp- Part No. 0688-2510
Resistor	R2: 1st film 1 M Ω ± 0.1 % 1/4 W	-hp- Part No. 0688-6369
Resistor (See Note 5)	R3: 1st comp 1 M Ω ± 10 % 1/4 W	-hp- Part No. 0684-1051
BNC to C10 Lead Adapter	Straight Through 6" Leads	Pamona 2631

NOTE 1: Variable Attenuator must meet required accuracy specifications or be of known accuracy.

2: Frequency Response Checks for systems using a Model 3320A or 3330A Synthesizer.

3: Optional Phase Linearity Check and/or delay measurement checks.

4: Required for 75-ohm systems only.

5: Required for Delay Measurement Check.

6: 3330B required for delay (Options 002, 003). HP-1B is not available in the 3320A.

SECTION V MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains performance checks (Paragraph 5-5) and adjustment procedures (Paragraph 5-29) for the Model 3570A Network Analyzer. Troubleshooting information is presented in Section VII, along with the Schematic Diagrams.

5-3. RECOMMENDED TEST EQUIPMENT.

5-4. The test equipment that is recommended for maintaining the Model 3570A is listed in Table 5-1. If the recommended model is not available, any instrument that has specifications equal to or better than the required specifications can be used.

5-5. PERFORMANCE CHECKS.

5-6. The following performance checks are in-cabinet procedures that can be used to verify that the 3570A is operating properly and meets the specifications listed in Table 1-1. These procedures can be used for incoming quality control inspection, to check specifications after a repair or for routine maintenance.

5-7. Test Card.

5-8. A Performance Check Test Card is provided at the end of this section for your convenience in recording the performance of the Model 3570A during performance checks. This card can be removed from the manual and used as a permanent record of the incoming inspection or of a routine performance check. The Performance Check Test Card may be reproduced without written permission from Hewlett-Packard.

5-9. Input Impedance Check.

5-10. The purpose of this check is to verify that both channels meet the Input Impedance specification ($1\text{ M}\Omega$, $<30\text{ pF}$) listed in Table 1-1.

RECOMMENDED TEST EQUIPMENT:

3320A/B, 3330A/B Synthesizer

Resistor: R; fixed $1\text{ M}\Omega \pm 0.1\%$ 1/4 W (-hp- Part No. 0698-6369)

NOTE

1. If a $1\text{ M}\Omega \pm 0.1\%$ resistor is not available, a resistor with a higher tolerance can be used, providing it is within the range of $1\text{ M}\Omega \pm 2000\ \Omega$ (0.2%).

2. Synthesizer and 3570A interconnections are given in Paragraph 3-15.

a. Connect the A and B Outputs, terminated in 50-ohm (or 75-ohm) loads, to the A and B Inputs. This is the same input configuration used for the Front Panel Zero Adjustments (see Figure 5-1).

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE ... 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz
PHASE REFERENCE A

Options 002, 003: Set PHASE/DELAY switch to PHASE; ABSOLUTE/RELATIVE switches to ABSOLUTE.

c. Set the Synthesizer to 0 dBm, 50 Hz (3330B Leveling Slow).

d. Adjust the A AMP ZERO control for a 3570A amplitude reading of $0\text{ dB} \pm 0.01\text{ dB}$.

e. Set the AMPLITUDE FUNCTION switch to B.

f. Adjust the B AMP ZERO control for a 3570A amplitude reading of $0\text{ dB} \pm 0.01\text{ dB}$.

g. Adjust the 10 Hz ϕ ZERO control for a phase reading of $0 \pm 0.01\text{ degree}$.

h. Insert the $1\text{ M}\Omega$ resistor between the terminated Channel B OUTPUT and Channel B INPUT as shown in Figure 5-1.

i. The 3570B amplitude reading should be between -5.94 dB and -6.11 dB , verifying the $1\text{ M}\Omega \pm 2\%$ input resistance specification for Channel B.

j. Set the Synthesizer frequency to 10.6 kHz.

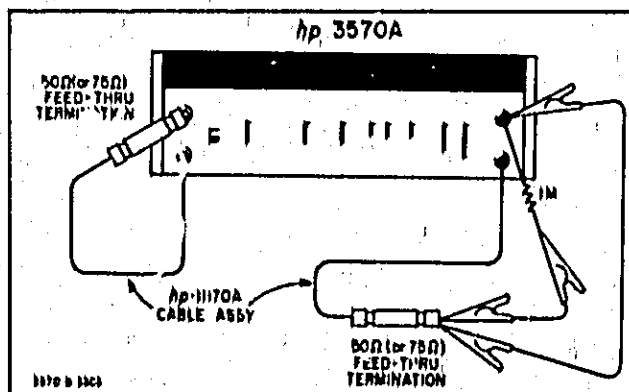


Figure 5-1. Input Impedance Check.

k. The 3570A phase reading should be 45 degrees or less in magnitude, verifying the < 30 pF shunt capacitance specification for Channel B.

l. Set the Synthesizer frequency to 50 Hz.

m. Remove the $1\text{ M}\Omega$ resistor from Channel B. Reconnect the terminated Channel B OUTPUT to the Channel B INPUT.

n. Insert the $1\text{ M}\Omega$ resistor between the terminated Channel A OUTPUT and the Channel A INPUT.

o. Set the 3570A AMPLITUDE FUNCTION switch to A.

p. The 3570A amplitude reading should be between -5.94 dB and -6.11 dB, verifying the $1\text{ M}\Omega \pm 2\%$ input resistance specification for Channel A.

q. Set the Synthesizer frequency to 10.6 kHz.

r. The 3570A phase reading should be 45 degrees or less in magnitude, verifying the < 30 pF shunt capacitance specification for Channel A.

s. This completes the Input Impedance Check. Remove the $1\text{ M}\Omega$ resistor from Channel A and reconnect the terminated Channel A OUTPUT to the Channel A INPUT.

5-11. Check for Power Line Related Spurious Responses.

5-12. This test is made to ensure that the average of the power line related spurious responses are not in the usable measurement range of the 3570A.

a. Set the 3570A front panel controls as follows:

AMPLITUDE FUNCTION A
MAX REF INPUT 1 V
BANDWIDTH 10 Hz

b. Set the 3330B AMPLITUDE to 0.1 volt. (-6.99 dBm, 50 ohm systems; -8.72 dBm, 75 ohm systems). Set the 3330B frequency to 1 MHz.

c. Connect the Channel A OUTPUT to the Channel A input and adjust the front panel zero for an indication of 00.00 dB.

d. Disconnect the input signal to Channel A. Leave the termination connected to the input.

e. Set the 3330B to each frequency listed in the appropriate column of Table 5-2. The average amplitude indication should be equal to or less than the specifications listed in Table 5-2.

f. Set the 3570A MAX/REF INPUT switch to 1 V. Set the synthesizer OUTPUT to 1 volt (+13.01 dBm, 50 ohm systems; +11.68 dBm, 75 ohm systems). Set the 3330B frequency to 1 MHz.

5-2

Table 5-2. Power Line Spurious Test.

Power Line Frequency In Use		Amplitude Limits (Magnitude Only)	
50 Hz Power	60 Hz Power	.1 V Range	1 V Range
50 Hz	60 Hz	> 70 dB	> 80 dB
100 Hz	120 Hz	> 85 dB	> 95 dB
160 Hz	180 Hz	> 80 dB	> 90 dB
200 Hz	240 Hz	> 85 dB	
250 Hz	300 Hz	> 80 dB	
300 Hz	360 Hz	> 95 dB	
350 Hz	420 Hz	> 95 dB	

g. Repeat Steps c through e for input levels given in Step f.

h. Repeat Steps a through g for Channel B.

5-13. Dynamic Range Check.

5-14. The purpose of this check is to verify that the 3570A dynamic range is greater than 100 dB with the frequency tuned to 30 times the selected BANDWIDTH. The 10 Hz bandwidth is checked at 330 Hz to avoid a power line related response at 300 Hz. If, on any Bandwidth setting, the 3570A fails to meet the required specification, perform the LO Feedthrough Adjustments outlined in Paragraph 5-57.

a. Perform the Front Panel Zero Adjustments (amplitude) as outlined in Paragraph 3-157. Use the 0 dBm MAX/REF INPUT VOLTAGE setting and the 10 Hz BANDWIDTH setting with the Synthesizer set to 0 dBm, 1 MHz.

b. Disconnect the A and B Input cables, leaving the A and B INPUTS terminated in 50 or 75 ohms.

c. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0.1 V
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

Options 002, 003: Set ABSOLUTE/RELATIVE switches to ABSOLUTE.

d. Set the Synthesizer frequency to 330 Hz.

e. The 3570A average amplitude reading should be below -100 dB.

f. Set the 3570A BANDWIDTH to 100 Hz.

g. Set the Synthesizer frequency to 3 kHz.

h. The 3570A average amplitude reading should be below -100 dB.

i. Set the 3570A BANDWIDTH to 3 kHz.

j. Set the Synthesizer frequency to 90 kHz.

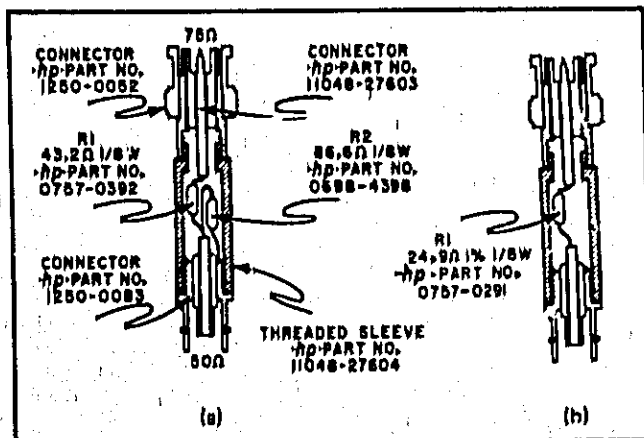


Figure 5-2. (a) 50 - 75 Ohm Adapter (b) 25 Ohm Compensating Resistor.

k. The 3570A average amplitude reading should average -100 dB.

l. Set the 3570A AMPLITUDE FUNCTION switch to B. Set the BANDWIDTH switch to 10 Hz.

m. Repeat Steps d through k.

5-15. Relative Amplitude Checks.

5-16. The purpose of these checks is to verify that the 3570A meets the relative amplitude specifications listed in Table 1-1.

RECOMMENDED TEST EQUIPMENT:

Variable Attenuator (-hp- Model 355D)

For 75 - ohm Outputs:

50 - ohm to 75 - ohm Adapter (see Figure 5-2A).

a. Perform the front panel zero adjustments (amplitude) as outlined in Paragraph 3-157 (Section III). Use the 0 dBm MAX/REF INPUT VOLTAGE setting and the 10 Hz BANDWIDTH setting with the Synthesizer set for an output of 0 dBm, 1 MHz. Leave setup for following steps.

b. Connect the equipment as shown in Figure 5-3(b). Set the Variable Attenuator to 0 dB.

c. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz
ABSOLUTE/RELATIVE ABSOLUTE
(Options 002, 003)

d. Set the Synthesizer frequency to 50 Hz (3330B Leveling Slow).

e. Adjust the Synthesizer amplitude setting for a 3570A amplitude reading of 0 dB $\pm$ 0.01 dB.

f. Set the Synthesizer to -20 dB. Allow time for the 3570A amplitude reading to stabilize.

g. The 3570A amplitude reading should be -20 dB $\pm$ 0.20 dB.

h. Set the Synthesizer to -40 dB.

i. The 3570A amplitude reading should be -40 dB $\pm$ 0.50 dB.

j. Set the Synthesizer to -60 dB.

k. The 3570A amplitude reading should be -60 dB $\pm$ 0.50 dB.

l. The procedure for testing these specifications at 10 kHz, 100 kHz, 1 MHz, 7 MHz and 13 MHz, is as follows:

m. Set the Synthesizer Frequency to the next frequency to be checked.

n. Set the Synthesizer Amplitude for 0 dB and the Variable Attenuator to 0 dB. The 3570A should read 0 dB $\pm$ 0.01 dB. Maintain this tolerance by using the front panel AMP. ZERO adjustments.

o. Leave the Synthesizer at 0 dB and adjust the variable attenuator for -20 dB. The 3570A should read -20 dB $\pm$ 0.2 dB.

p. Adjust the Variable Attenuator for -40 dB. The 3570A should read -40 dB $\pm$.5 dB.

q. Set the Synthesizer Amplitude for -40 dB and the Variable Attenuator for -40 dB. The 3570A should read -80 dB $\pm$ 0.5 dB.

r. Leave the Synthesizer Amplitude at -40 dB and adjust the Variable Attenuator for -60 dB. The 3570A should read -100 dB $\pm$ 1.5 dB.

s. Repeat Steps m through r using the frequency settings discussed in Step l.

t. Move the Input Cable to the Channel E input and repeat Steps e through s.

5-17. Frequency Response Checks (3320A or 3330A Synthesizers).

NOTE

For systems using a Model 3320B or 3330B Synthesizer, refer to Paragraph 5-19.

5-18. The purpose of these checks is to verify that the 3570A meets the Amplitude Frequency Response specifications listed in Table 1-1.

RECOMMENDED TEST EQUIPMENT:

Thermal Converter (-hp- Model 11050A for 50 - ohm systems; -hp- Model 11050A Option H01 for 75 - ohm systems.

DC Digital Voltmeter (-hp- Model 3450B).

a. Connect the A and B Outputs, terminated in 50 - ohm (or 75 - ohm) loads, to the A and B Inputs. This is the same input configuration used for the Front Panel Zero Adjustments.

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 1 V
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

Options 002, 003: Set ABSOLUTE/RELATIVE switches to ABSOLUTE.

c. Set the Synthesizer AMPLITUDE control to 0 dBm.

d. Connect the Thermal Converter AC INPUT to the 3570A CHANNEL A OUTPUT connector. (Remove termination when Thermal Converter is connected.) Connect the DVM to the output of the Thermal Converter.

e. Set the DVM to the 100 mV range (dc function).

f. Set the Synthesizer frequency to 50 Hz.

g. Adjust the Synthesizer AMPLITUDE control for a DVM reading of $7.4 \text{ mV} \pm 0.01 \text{ mV dc}$.

h. Allow approximately two minutes for the Thermal Converter to warm up and stabilize.

i. If necessary, readjust the Synthesizer AMPLITUDE control for a DVM reading of $7.4 \text{ mV} \pm 0.01 \text{ mV dc}$. Record the DVM reading: _____ mV dc.

j. Without disturbing the Synthesizer controls disconnect the Thermal Converter from the Synthesizer. Reconnect the Channel A OUTPUT to the INPUT (using correct termination).

k. Adjust the 3570A AMP, ZERO control for an amplitude reading of 00.00 dB.

l. Set the Synthesizer frequency to 100 Hz.

m. Disconnect the RF Input Cable and reconnect the Thermal Converter as in Step d above.

n. Adjust the Synthesizer AMPLITUDE control for the same DVM reading recorded in Step i.

o. Disconnect the Thermal Converter from the Synthesizer and reconnect the Channel OUTPUTS to the INPUTS (using correct termination).

Table 5-3. Frequency Response Checks.

Synthesizer Frequency	A Amplitude Readings	B Amplitude Readings	B - A Readings
50 Hz	_____ dB	_____ dB	_____ dB
100 Hz	_____ dB	_____ dB	_____ dB
1 kHz	_____ dB	_____ dB	_____ dB
10 kHz	_____ dB	_____ dB	_____ dB
100 kHz*	_____ dB	_____ dB	_____ dB
1 MHz	_____ dB	_____ dB	_____ dB
10 MHz	_____ dB	_____ dB	_____ dB
13 MHz	_____ dB	_____ dB	_____ dB

*If frequency response fails only at 100 kHz, the problem may be rf feedthrough rather than frequency response (Paragraph 5-59).

p. Record the 3570A amplitude readings in the space provided in the Performance Check Test Card.

q. Repeat Steps m through p with the Synthesizer set to each additional frequency listed in Table 5-3.

r. Determine the largest negative reading recorded in Step p. If there are no negative readings, use 0 dB or the smallest positive reading: _____ dB.

s. Determine the largest positive reading recorded in Step p. If there are no positive readings, use 0 dB or the smallest negative reading: _____ dB.

t. Algebraically subtract the largest positive reading from the largest negative reading (or vice-versa) to obtain the peak-to-peak response deviation.

u. The peak-to-peak response deviation should be less than, or equal to $\pm 0.50 \text{ dB}$, verifying the frequency response specification for the A (or B) Amplitude Function.

v. Set the 3570A AMPLITUDE FUNCTION switch to B. Repeat Steps e through u.

w. Connect the CHANNEL OUTPUT to the INPUT (using correct termination). The Thermal Converter is not required for the remaining steps.

x. Set the 3570A AMPLITUDE FUNCTION switch to B - A.

y. Record the B - A amplitude reading with the Synthesizer set to each frequency listed in Table 5-3.

z. Using the readings recorded in Step y, calculate the peak-to-peak response deviation as outlined in Steps r through t.

aa. The peak-to-peak response deviation should be less than, or equal to $\pm 0.10 \text{ dB}$, verifying the frequency response specification for the B - A Amplitude Function.

5-19. Frequency Response Checks (3320B or 3330B Synthesizers).

5-20. The purpose of these checks is to verify that the 3570A meets the Amplitude Frequency Response specifications listed in Table 1-1.

a. Perform the Front Panel Zero Adjustments (amplitude) as outlined in Paragraph 3-157 (Section III). Use the 0 dBm MAX/REF INPUT VOLTAGE setting and the 10 Hz BANDWIDTH setting with the Synthesizer set to 0 dBm, 1 MHz. Leave setup for following steps.

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

Options 002, 003: Set ABSOLUTE/RELATIVE switches to ABSOLUTE.

c. Set the Synthesizer to 0 dBm, 50 Hz (Leveling Slow).

d. With the Synthesizer set to each frequency listed in Table 5-3, record the 3570A amplitude reading in the space provided on the Performance Check Test Card. The following steps determine the peak-to-peak response deviation.

e. Determine the largest negative reading recorded in Step d. If there are no negative readings use 0 dB or the smallest positive reading: _____ dB.

f. Determine the largest positive reading recorded in Step d. If there are no positive readings use 0 dB or the smallest negative reading: _____ dB.

g. Algebraically subtract the largest positive reading from the largest negative reading (or vice-versa) to obtain the peak-to-peak response deviation.

h. The peak-to-peak response deviation should be less than or equal to ± 0.50 dB, verifying the frequency response specification for the A (or B) Amplitude Function.

i. Set the 3570A AMPLITUDE FUNCTION switch to B. Repeat Steps e through h.

j. Set the 3570A AMPLITUDE FUNCTION switch to B-A.

k. On the Performance Check Test Card, record the B-A amplitude reading with the Synthesizer set to each frequency listed in Table 5-3.

l. Using the readings recorded in Step k, calculate the peak-to-peak response deviation as outlined in Steps e through g.

m. The peak-to-peak response deviation should be less than, or equal to ± 0.10 dB, verifying the frequency response specification for the B-A Amplitude Function.

5-21. Phase vs. Frequency and Phase vs. Amplitude Checks. The purpose of these checks is to verify that the 3570A meets the Phase vs. Frequency, Phase vs. Amplitude and Phase Reference specifications listed in Table 1-1. Satisfactory performance during these checks is reasonable verification that the phase detector circuits are operating properly. If further verification of phase accuracy is required, perform the Phase Linearity Check outlined in Paragraph 5-23.

RECOMMENDED TEST EQUIPMENT:

Systems using a Model 3320B or 3330B Synthesizer:
Variable Attenuator (-hp- Model 355D)

Triax to BNC adapter -hp- 1250-0595, 2 each

For 75 - ohm Outputs:

50 - ohm to 75 - ohm Adapter (See Figure 5-2A)

25 - ohm Resistor (See Figure 5-2B).

a. Perform the Front Panel Zero Adjustments (amplitude and phase) as outlined in Paragraph 3-157 (Section III). Use the 0 dBm MAX/REF INPUT VOLTAGE setting and the 10 Hz BANDWIDTH setting with the Synthesizer set for an output of 0 dBm, 1 MHz. Leave setup for following steps.

b. Insert the Variable Attenuator between the OUTPUT (or ALT OUTPUT O) of the Synthesizer and the rear panel INPUT of the 3570A as shown in Figure 5-3C. Set the Variable Attenuator to 0 dB.

c. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz
PHASE REFERENCE A

Options 002, 003: Set PHASE/DELAY switch to PHASE; ABSOLUTE/RELATIVE switches to ABSOLUTE.

d. Set the Synthesizer for an output of 0 dBm, 50 Hz.

NOTE

1. The following checks require that the amplitude be varied from 0 dBm to -80 dBm in steps of 10 dB.

2. If using a Model 3320B or 3330B Synthesizer be sure the LEVELING control is set in accordance with the output frequency.

e. Allow time for the 3570A phase reading to stabilize.

f. The 3570A phase reading should be within the tolerances listed in Table 5-4A for the corresponding frequency and amplitude setting.

Table 5-4. Phase Checks.

a) Phase vs. Frequency Phase vs. Amplitude		Channel A within 6 dB of Channel B
Synth. Frequency	Amplitude Setting	Phase (0 Degrees)
50 Hz	0 dB	± 1.2
50 Hz	-20 dB	± 1.2
50 Hz	-70 dB	± 1.4
50 Hz	-80 dB	± 1.8
100 Hz	0 dB	± 0.6
100 Hz	-20 dB	± 0.6
100 Hz	-70 dB	± 0.8
100 Hz	-80 dB	± 1.2
500 Hz	0 dB	± 0.6
500 Hz	-20 dB	± 0.6
500 Hz	-70 dB	± 0.8
500 Hz	-80 dB	± 1.2
1 kHz	0 dB	± 0.6
1 kHz	-20 dB	± 0.6
1 kHz	-70 dB	± 0.8
1 kHz	-80 dB	± 1.2
15 kHz	0 dB	± 0.6
15 kHz	-20 dB	± 0.6
15 kHz	-70 dB	± 0.8
15 kHz	-80 dB	± 1.2
30 kHz	0 dB	± 0.6
30 kHz	-20 dB	± 0.6
30 kHz	-70 dB	± 0.8
30 kHz	-80 dB	± 1.2
100 kHz	0 dB	± 0.6
100 kHz	-20 dB	± 0.6
100 kHz	-70 dB	± 0.8
100 kHz	-80 dB	± 1.2
500 kHz	0 dB	± 0.6
500 kHz	-20 dB	± 0.6
500 kHz	-70 dB	± 0.8
500 kHz	-80 dB	± 1.2
1 MHz	0 dB	± 0.6
1 MHz	-20 dB	± 0.6
1 MHz	-70 dB	± 0.8
1 MHz	-80 dB	± 1.2
7 MHz	0 dB	± 1.4
7 MHz	-20 dB	± 1.4
7 MHz	-70 dB	± 1.6
7 MHz	-80 dB	± 2.0
13 MHz	0 dB	± 1.4
13 MHz	-20 dB	± 1.4
13 MHz	-70 dB	± 1.6
13 MHz	-80 dB	± 2.0

b) Phase vs. Amplitude with Channels at Different Levels			
Frequency 1 MHz			
Channel A	Channel B	Range	
		1 V	.1 V
0 dB	-20 dB	$\pm 1.3^\circ$	$\pm 1.3^\circ$
0 dB	-40 dB	$\pm 1.5^\circ$	$\pm 1.5^\circ$
0 dB	-60 dB	$\pm 1.5^\circ$	$\pm 1.5^\circ$
0 dB	-80 dB	$\pm 3.0^\circ$	$\pm 4.5^\circ$
-20 dB	0 dB	$\pm 1.3^\circ$	$\pm 1.3^\circ$
-40 dB	0 dB	$\pm 1.5^\circ$	$\pm 1.5^\circ$
-60 dB	0 dB	$\pm 1.5^\circ$	$\pm 1.5^\circ$
-80 dB	0 dB	$\pm 3.5^\circ$	$\pm 4.5^\circ$

g. Repeat Steps e and f for each frequency and amplitude setting listed in Table 5-4A.

h. Set the synthesizer amplitude to 0 dB and frequency to 1 MHz.

i. Adjust the 3570A 10 Hz ϕ ZERO control for a phase reading of +2.00 degrees.

j. Set the 3570A 10 Hz ϕ PHASE REFERENCE to -A.

k. The 3570A phase reading should be -178 degrees ± 0.4 degree, verifying the Phase Reference specification listed in Table 1-1.

5-22. Phase vs. Amplitude (Channels at Different Levels).

RECOMMENDED TEST EQUIPMENT:

Systems using a Model 3320A/B or 3330A/B: 1 Variable Attenuator (355D).

For 75 - ohm Outputs:

50 - ohm to 75 - ohm Adapter (see Figure 5-2)

a. Perform the front panel Zero Adjustments (amplitude and phase) as outlined in Paragraph 3-157 (Section III).

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE..... 1 V
AMPLITUDE FUNCTION..... A
BANDWIDTH..... 10 Hz
PHASE REFERENCE..... A

Options 002, 003: Set PHASE/DELAY switch to PHASE; ABSOLUTE/RELATIVE switch to ABSOLUTE.

c. Insert the Variable Attenuator between the Input and Output of Channels A as shown in Figure 5-3D.

NOTE

Be sure the synthesizer LEVELING control is set in accordance with the output frequency.

d. Perform the front panel Zero adjustments as outlined in Paragraph 3-157.

e. To check Phase vs. Amplitude (Channels at different levels), set the Synthesizer to +13.01 dBm when the 3570A is on the 1 V range and to -6.99 dBm when the 3570A is on the .1 V range. Set Bandwidth to 10 Hz.

f. Set the Synthesizer frequency to 1 MHz and vary the amplitude with the Attenuator in 10 dB steps. The 3570A Phase reading should be within the tolerances listed in Table 5-4B.

g. Remove input attenuator from Channel A and connect it between the INPUT and OUTPUT of Channel B. Repeat Steps d through f to check Channel B.

5-23. Phase Linearity Check.

5-24. The purpose of this check is to verify that the 3570A meets the ± 0.2 degree Phase Linearity specification listed in Table 1-1. This check is performed by inserting a 1,000 ft. length of coax cable in Channel B to produce a linear phase vs. frequency response at the 3570A inputs.

RECOMMENDED TEST EQUIPMENT:

1,000 ft. coax cable equipped with BNC connectors (RG58A/U for 50 - ohm systems) (RG59A/U for 75 - ohm systems)

NOTE

If a 1,000 ft. length of coax cable is not available, this check can be performed using a cable length as short as 500 ft. A longer cable will provide greater resolution, thus improving the validity of the check.

a. Using a 12" cable, connect the Channel A OUTPUT, terminated in 50 - ohm (or 75 - ohm) load, to the Channel A INPUT. Using a 1,000 ft. cable, connect the Channel B OUTPUT, terminated in 50 - ohm (or 75 - ohm) load, to the Channel B INPUT.

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 1 V
AMPLITUDE FUNCTION B
BANDWIDTH 100 Hz
PHASE REFERENCE A

c. Set the Synthesizer frequency to 500 kHz. Adjust the Synthesizer amplitude for a 3570A amplitude reading of - 20 dB (3320B/3330B Synthesizers) or - 10 dB (3320A or 3330A Synthesizers).

d. Increase the Synthesizer frequency to obtain a 3570A phase reading of 0 degrees ± 2 degrees (approximately 600 kHz for 1,000 ft. cable; approximately 1.2 MHz for 500 ft. cable).

e. Adjust the 3570A 100 Hz ϕ ZERO control for a phase reading of 00.00 degrees.

f. Increment the Synthesizer frequency in steps of 10 kHz until the 3570A phase reading is approximately - 175 degrees. The change in phase that occurs from step to step should be constant, within ± 0.2 degrees. Options 002, 003; set ABSOLUTE/RELATIVE switch to RELATIVE and press ENTER OFFSET at 0 degrees. Each time the frequency is incremented, observe the change in phase and again press ENTER OFFSET.

5-25. Bandwidth Checks.

5-26. Optional. The purpose of the following steps is to check the bandwidth settings. The bandwidth checks are strictly optional and are included only to verify that the

crystal filters are aligned to provide the recommended performance characteristics. Since bandwidths are not specified in Table 1-1, readings outside of the test limits given in the bandwidth checks only indicate that crystal filter alignment is recommended and do not, in themselves, constitute a performance failure. If you desire to check the bandwidth settings perform Steps a through l; if not proceed to Paragraph 5-27.

RECOMMENDED TEST EQUIPMENT:

Systems using a Model 3330B Automatic Synthesizer: none required.

Systems using a Model 3320B Frequency Synthesizer: Electronic Counter (hp- Model 5245L or equivalent).

a. Connect the 3570A to the Synthesizer as shown in Figure 5-3A. Connect the fixed 1 MHz (Δ) to the Channel A input.

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 1V
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

Options: 002, 003: Set ABSOLUTE/RELATIVE switches to RELATIVE.

c. Set the Synthesizer to 1 MHz and +13.01 dBm.

d. Vary the frequency slightly to achieve a peak amplitude reading on the 3570A.

e. Record the frequency (F1) and amplitude (A1) measured in Step d on the Performance Test Card.

f. Increase the frequency of the synthesizer until the amplitude decreases to (A1 - 3 dB) $\pm .01$ dB.

g. Record the frequency (F2) and the amplitude (A2) measured in Step f on the Performance Test Card.

h. Decrease the frequency of the Synthesizer until the amplitude reading is again equal to A2 $\pm .01$ dB.

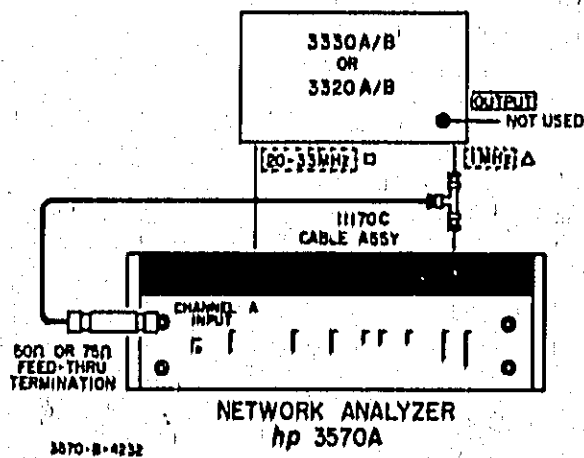
i. Record the frequency reading (F3) on the Performance Test Card.

j. Subtract F1 from F2 and subtract F3 from F1. The results should be within $\pm 15\%$ of the selected bandwidth divided by two.

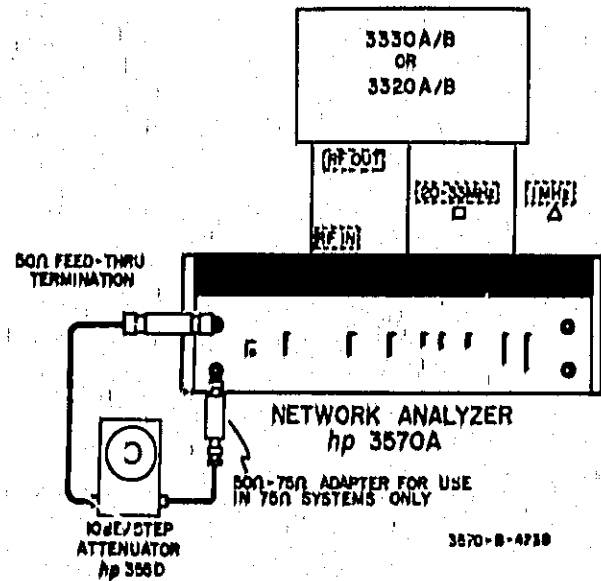
k. Record the result on the Performance Test Card.

l. Repeat Steps c through k for the 100 Hz and 3 kHz bandwidth.

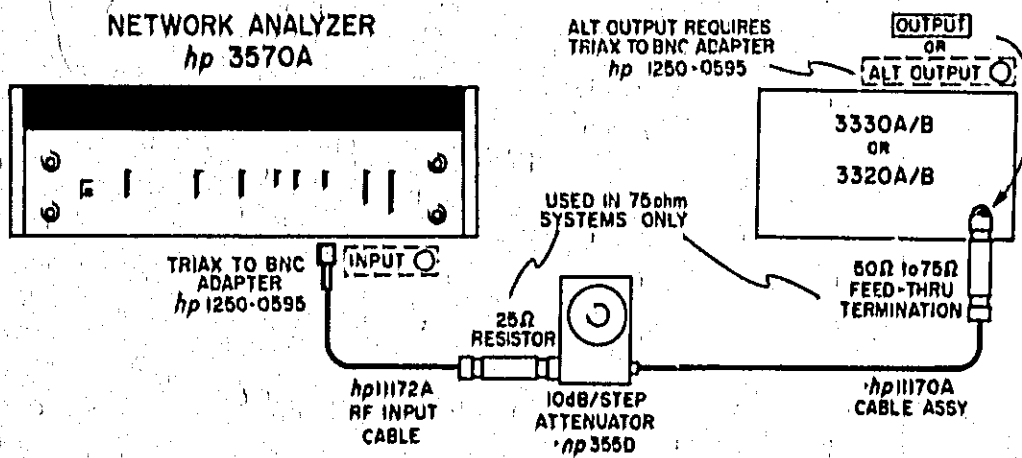
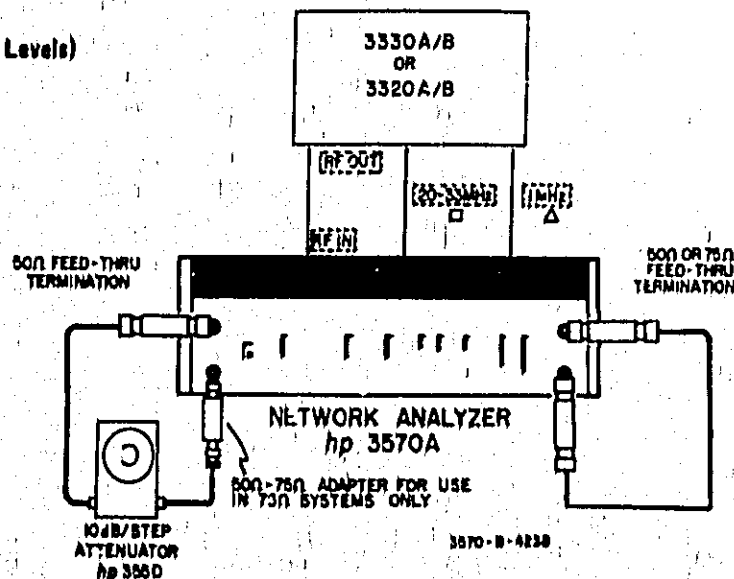
(a). Bandwidth Setup for Testing Channel A.



(b). Amplitude Linearity.



(c). Phase vs. Frequency.

(d). Phase vs. Amplitude.
(Channels at Different Levels)

5-17. Delay Measurement Check (Options 002, 003 only).**NOTE**

Requires use of 3330B Synthesizer.

5-28. The purpose of this check is to verify the ability of the 3570A to accurately compute group delay. This check is performed by applying a constant $\Delta \phi$ of 36 degrees and changing the 3570A Δf (FREQ STEP) setting from 5 Hz to 200 kHz while observing the computed delay readings. Satisfactory performance during this check and the phase accuracy checks (Paragraph 5-21 and 5-23) is reasonable verification of delay accuracy. If further verification is required, check delay accuracy using a network with known delay characteristics or using the 1,000 ft. length of coax cable recommended in the Phase Linearity Checks (Paragraph 5-23). Delay accuracy specifications are listed in Table 1-1.

RECOMMENDED TEST EQUIPMENT:

Resistor: $1\text{ M}\Omega \pm 10\%$ 1/4 W (hp- Part No. 0684-1051)

NOTE

hp- 11236B Multi-Unit Cable must be connected between the 3570A and 3330B Remote Control connectors.

a. Perform the Front Panel Zero Adjustments (phase) as outlined in Paragraph 3-157. Use the 0 dBm MAX/REF INPUT VOLTAGE setting and the 100 Hz BANDWIDTH setting with the Synthesizer set to 0 dBm, 1 MHz.

b. Insert the $1\text{ M}\Omega$ resistor between the terminated Channel B OUTPUT and the Channel B INPUT as shown in Figure 5-1.

c. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A

BANDWIDTH.....100 Hz
 PHASE/DELAY.....PHASE
 PHASE REFERENCE.....A
 ABSOLUTE/RELATIVE
 (Phase/Delay).....ABSOLUTE

d. Set the 3330A/B Automatic Synthesizer as follows:

AMPLITUDE.....0 dBm
 FREQUENCY.....1 kHz
 FREQ STEP.....20 Hz
 TIME/STEP.....30 msec
 SWEEP.....UP/FREQUENCY
 STEPS.....10

e. Adjust 100 Hz BANDWIDTH for Zero.

f. Using the FREQ ↑ key, increment the Synthesizer frequency to obtain a phase reading of approximately -36 degrees.

g. Press the Synthesizer FREQ STEP + 10 key twice. Using the FREQ ↑ and FREQ ↓ keys, adjust the Synthesizer frequency for a phase reading of -36.00 degrees (± 0.01 degree).

h. Record the Synthesizer frequency: _____ Hz.

i. Subtract 1,000 Hz from the Synthesizer frequency recorded in Step h: _____ Hz. Enter the resulting frequency as the FREQ STEP on the Synthesizer.

EXAMPLE:

If the Synthesizer frequency (Step h) is 10,351.0 Hz, the resulting frequency (Step i) is 10,351.0 - 1,000 = 9,351.0 Hz. The Synthesizer entry is then: FREQ STEP 9,351.0 Hz.

j. Press the FREQ STEP + 10 key.

k. Set the Synthesizer frequency to 1 kHz. Set the TIME/STEP control to 1000 msec.

l. Increment to center frequency by pressing the FREQ ↑ key five times.

m. Press the Synthesizer FIRST POINT key. The 3570A phase reading should be 00.00 degrees, ± 0.01 degree.

n. Set the Synthesizer SWEEP control to DOWN. Again press the FIRST POINT key. The 3570A phase reading should be -36.00 degrees, ± 0.01 degree.

o. Set the Synthesizer SWEEP control to UP. Set the TIME/STEP control to 300 msec.

p. Set the 3570A controls as follows:

DELAY MODE.....CW
 ABSOLUTE/RELATIVE.....ABSOLUTE
 PHASE/DELAY.....DELAY
 FREQ STEP:
 Frequency Step Switch.....5 Hz
 Frequency Step Multiplier.....X1
 (use WHITE multipliers)

q. Start the sweep by pressing the Synthesizer START CONT key.

r. Allow 10 seconds for the delay reading to stabilize.

s. The delay reading should be 20.00 msec ± 0.04 msec.

t. Set the 3570A Frequency Step and Frequency Step Multiplier controls to each setting listed in Table 5-5. At each setting the delay reading should be within the tolerances listed in the table. Allow 10 seconds for the delay reading to stabilize at each step setting.

Table 5-5. Delay Measurement Check.

Freq Step	Step Multiplier	Δf Setting	Absolute Delay	Lower Limit	Upper Limit
5	X1	5 Hz	20.00 msec	19.96 msec	20.04 msec
10	X1	10 Hz	10.00 msec	9.98 msec	10.02 msec
16.6	X1	16.6 Hz	6.00 msec	5.99 msec	6.01 msec
20	X1	20 Hz	5.00 msec	4.99 msec	5.01 msec
5	X10	50 Hz	2.000 msec	1.996 msec	2.004 msec
10	X10	100 Hz	1.000 msec	0.998 msec	1.002 msec
16.6	X10	166 Hz	0.600 msec	0.599 msec	0.601 msec
20	X10	200 Hz	0.500 msec	0.499 msec	0.501 msec
5	X100	500 Hz	0.2000 msec	0.1996 msec	0.2004 msec
10	X100	1 kHz	0.1000 msec	0.0998 msec	0.1002 msec
16.6	X100	1.66 kHz	0.0600 msec	0.0599 msec	0.0601 msec
20	X100	1 kHz	0.0500 msec	0.0499 msec	0.0501 msec
5	X1 K	5 kHz	20.00 μ sec	19.96 μ sec	20.04 μ sec
10	X1 K	10 kHz	10.00 μ sec	9.98 μ sec	10.02 μ sec
16.6	X1 K	16.6 kHz	6.00 μ sec	5.99 μ sec	6.01 μ sec
20	X1 K	20 kHz	5.00 μ sec	4.99 μ sec	5.01 μ sec
5	X10 K	50 kHz	2.000 μ sec	1.996 μ sec	2.004 μ sec
10	X10 K	100 kHz	1.000 μ sec	0.998 μ sec	1.002 μ sec
16.6	X10 K	166 kHz	0.600 μ sec	0.599 μ sec	0.601 μ sec
20	X10 K	200 kHz	0.500 μ sec	0.499 μ sec	0.501 μ sec

5-29. ADJUSTMENT PROCEDURES.

5-30. This portion of Section V contains complete adjustment procedures for the Model 3570A Network Analyzer:

Power Supply Adjustments (Paragraph 5-35)
 Power Splitter Zero Adjustment (Paragraph 5-37)
 Analog A to D Zero Adjustment (Paragraph 5-39)
 B - A Zero Adjustment (Paragraph 5-41)
 Phase Detector Symmetry Adjustments (Paragraph 5-43)
 Phase Detector Adjustments (Paragraph 5-45)
 Log Amplifier Phase Adjustments (Paragraph 5-47)
 Bandwidth Logic Phase Adjustments (Paragraph 5-49)
 Input Mixer Phase Adjustments (Paragraph 5-51)
 Crystal Filter Adjustments (Paragraph 5-53 and 5-55)
 LO Feedthrough Adjustments (Paragraph 5-57)
 RF Feedthrough Adjustments (Paragraph 5-59)
 Log Amplifier Adjustments (Paragraph 5-61)
 High Frequency Phase Adjustments (Paragraph 5-63)
 Bandwidth Gain Switching Adjustments (Paragraph 5-65)
 Overload Indicator Adjustments (Paragraph 5-67)
 Delay Crossover Adjustment (Paragraph 5-69)
 Phase vs. Amplitude Adjustment (Paragraph 5-71)

5-31. Test Equipment.

5-32. The test equipment required for the adjustments is listed in Table 5-1 and at the beginning of each adjustment procedure. If the recommended model is not available, any instrument that has specifications equal to or better than the required specifications can be used.

5-33. Test Point and Adjustment Locations.

5-34. Test point and adjustment locations are shown in Figure 5-9. Most of the test points and adjustments are easily accessible with the top outer cover of the instrument removed. In some cases, however, it will be necessary to remove the inner covers and place PC assemblies on extenders. *Set the 3570A LINE switch to OFF when removing or replacing a PC assembly.*

NOTE

1. Unless otherwise specified, all adjustments should be performed with the A and B OUTPUTS, terminated in 50-ohm (or 75-ohm) loads, connected to the A and B INPUTS. This is the same input configuration that is used for the Front Panel Zero Adjustments (Paragraph 3-157).
2. All test measurements should be made with respect to circuit ground which is available at any point on the instrument chassis.

5-35. Power Supply Adjustments.

5-36. These adjustments set the levels of the + 15 V dc and - 15 V dc regulated power supplies.

RECOMMENDED TEST EQUIPMENT:

DC Digital Voltmeter (-hp- Model 3450B)

- a. Connect DVM to A37TP1 (+ 15 V TP).
- b. Adjust A37R6 (+ 15 V ADJ) for a DVM reading of + 15 V $\pm$ 0.02 V dc.
- c. Connect DVM to A17TP2 (- 15 V TP).
- d. Adjust A37R14 (- 15 V ADJ) for a DVM reading of - 15 V $\pm$ 0.02 V dc.

5-37. Power Splitter Zero Adjustment.

5-38. This adjustment nulls out any dc offset present at the A and B OUTPUT connectors.

RECOMMENDED TEST EQUIPMENT:

DC Voltmeter (-hp- 3450B)

- a. Connect DC Voltmeter to the Channel A OUTPUT.
- b. Set the Synthesizer LINE switch to STANDBY or OFF.
- c. Adjust A8R6 (DC OFFSET ADJ) for 0 V $\pm$ 10 mV dc.
- d. Set the Synthesizer LINE switch to ON.

5-39. Analog A to D Zero Adjustment.

5-40. These adjustments null out offsets introduced by the operational amplifiers on the Analog A to D Assembly, A16. This is accomplished by applying a dc voltage to A16TP1 and A16TP4 which simulates an input to the A to D converter.

RECOMMENDED TEST EQUIPMENT:

DC Digital Voltmeter (-hp- Model 3450B),
 DC Power Supply (-hp- Model 6101A).

a. Set the 3570A LINE switch to OFF. Remove the Output Buffer Assembly, A15. Set the 3570A LINE switch to ON.

b. Options 002, 003: Set PHASE/DELAY switch to PHASE.

c. Apply + 10 mV to A16TP4 and adjust A16R14 so the display reads + 0.10 dB.

d. Apply - 10 mV to A16TP4 and adjust A16R9 so the display reads - 0.10 dB.

e. Apply ± 10.0 V to A16TP4. The amplitude display should read $\pm (98.00$ dB to 102.00 dB). The sign depends on the polarity of the applied signal at the R16TP4. The absolute values of the readings should be within ± 0.04 dB.

f. Apply + 10 mV dc to A16TP1 and adjust R39 so the display reads 0.20° .

g. Apply - 10 mV dc to A16TP1 and adjust R47 so the display reads - 0.20.

h. Apply ± 10.0 Vdc to A16TP1. The phase display should read $\pm (196.00^\circ$ to $204.00^\circ)$. The sign depends on the polarity of the applied signal at A16TP1. The absolute values of the readings should be within $\pm 0.05^\circ$.

5-41. B - A Zero Adjustment.

5-42. This adjustment nulls out any dc offset introduced by the summing amplifier (U7) on the Output Buffer Assembly, A15.

RECOMMENDED TEST EQUIPMENT:

DC Digital Voltmeter (-hp- Model 3450B)

a. Connect the DVM to the rear panel AMPLITUDE FUNCTION output.

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

c. Set the Synthesizer for an output of 0 dBm, 1 MHz.

d. Adjust the Channel A front panel AMP ZERO control for a DVM reading of $0\text{ V} \pm 0.001\text{ V dc}$.

e. Set the AMPLITUDE FUNCTION switch to B.

f. Adjust the Channel B front panel AMP ZERO control for a DVM reading of $0\text{ V} \pm 0.001\text{ V dc}$.

g. Set the AMPLITUDE FUNCTION switch to B - A.

h. Adjust A15R29 (B - A ZERO ADJ) for a DVM reading of $0\text{ V} \pm 0.001\text{ V dc}$.

5-43. Phase Detector Symmetry Adjustments.

5-44. These adjustments optimize the symmetry of the two limited signals applied to the Phase Detector.

RECOMMENDED TEST EQUIPMENT:

Oscilloscope (-hp- Model 180A with 10:1 Divider Probe)

a. Set the 3570A LINE switch to OFF.

b. Remove the Channel B Log Amplifier Assembly, A23.

c. Place the Phase Limiter Assembly, A13, on an extender.

d. Connect a short clip lead between A13TP1 and A13TP2 (labeled TPA and TPB).

e. Set the 3570A controls as follows:

LINE ON
MAX/REF INPUT VOLTAGE 0 dBm
BANDWIDTH 3 kHz
PHASE REFERENCE A

f. Set the Synthesizer for an output of 0 dBm, 1 MHz.

g. Connect the oscilloscope to A14TPA.

h. Set the Oscilloscope controls as follows:

Vertical Sensitivity 0.1 V/div
(ac coupled)
Sweep Time 0.5 $\mu\text{sec/div}$

i. Alternately observe the positive and negative halves of the square wave by switching from + Slope (trigger) to - Slope on the oscilloscope.

j. Adjust A13R16 (A SYMMETRY ADJUST) until the positive and negative halves of the square wave are exactly equal in duration (see Figure 5-4).

k. Connect the oscilloscope to A14TPB.

l. Adjust A13R36 (B SYMMETRY ADJUST) until the positive and negative halves of the square wave are exactly equal in duration.

m. Remove the oscilloscope.

5-45. Phase Detector Adjustments.

5-46. These adjustments set the current sources and cur-

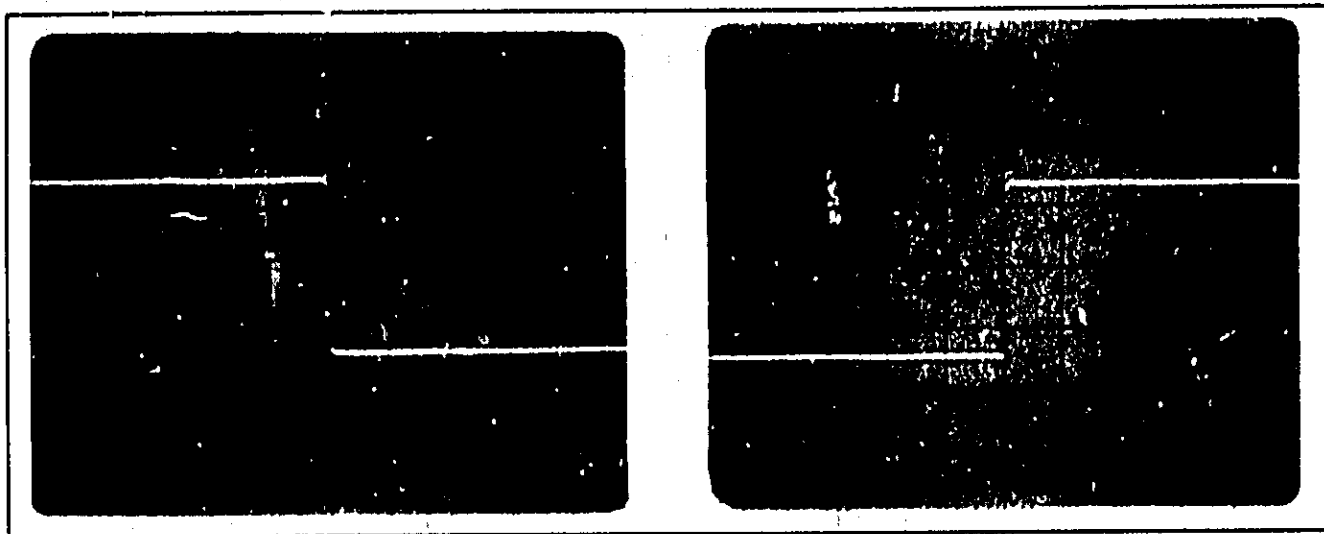


Figure 5-4. Phase Detector Symmetry Adjustment: Positive and Negative Half-Cycles.

rent sinks to produce the proper dc levels at the output of the Phase Detector.

a. Perform Steps a through f of the Phase Detector Symmetry Adjustment procedure outlined in Paragraph 5-43.

b. Set the test switch (S1) on the Phase Detector, A14, to position 1.

c. Adjust A14R52 (ADJ 1) for a phase reading of 00.00 degrees.

d. Set the test switch to the operate (OP) position.

e. Adjust the front panel 3 kHz ϕ ZERO control for a phase reading of 00.00 degrees.

f. Set the test switch to position 2.

g. Adjust A14R37 (ADJ 2) for a phase reading of +90.00 degrees.

h. Set the test switch to position 3.

i. Adjust A14R36 (ADJ 3) for a phase reading of +90.00 degrees.

j. Repeat Steps b through i.

k. Set the test switch to the operate (OP) position.

l. Adjust the front panel 3 kHz ϕ ZERO control for a phase reading of 00.00 degrees.

m. Set the 3570A BANDWIDTH switch to 100 Hz.

n. Adjust the front panel 100 Hz ϕ ZERO control for a phase reading of 00.00 degrees.

o. Set the 3570A BANDWIDTH switch to 10 Hz.

p. Adjust the front panel 10 Hz ϕ ZERO control for a phase reading of 00.00 degrees.

q. This completes the Phase Detector Adjustments. Remove the short from A13 and Replace A13 and A23.

r. If the Phase Zero readings cannot be obtained, the range of the Phase Zero adjustments may be altered by substituting another resistor for A13R7 from the Padding List given below.

Padding List For A13R7*

Value	Imp. Part No.
909 OHM .01	0757-0442
931 OHM .01	0698-4465
953 OHM .01	0698-4125
1050 OHM .01	0698-4157
1100 OHM .01	0757-0424

Δ 5-47. Log Amplifier Phase Adjustments.

Δ 5-48. These adjustments are not necessary for 3570A's equipped with A7/A23 Log Amplifier Boards numbered 03570-66555 or 03570-69555. These new type boards will introduce approximately 2° of phase error which can be compensated for in the Bandwidth Logic Phase Adjustments (Paragraph 5-45). See the 3570A manual backdating for the Log Amplifier Phase Adjustments necessary for 3570A's equipped with A7/A23 Log Amplifier Boards numbered 03570-66535 or 03570-69535.

5-49. Bandwidth Logic Phase Adjustments.

(For instruments equipped with 03570-66555 or 03570-69555 Log Amplifier Boards only. See the 3570A

manual backdating for instruments equipped with 03570-66535 or 03570-69535 Log Amplifiers.)

- Δ 5-50. These adjustments peak the 100 kHz response of the IF amplifiers on the Bandwidth Logic Assemblies and equalize the phase shift introduced by the A and B Bandwidth Logic circuits.

RECOMMENDED TEST EQUIPMENT:

AC Digital Voltmeter (-hp- Model 3450B)

a. Set the 3570A LINE switch to OFF. Remove the Channel B IF Mixer Assembly, A18.

b. Place both Bandwidth Logic Assemblies, A6 and A22, on extenders.

c. Connect a e"p lead between A6 pin 1 and A22 pin 1.

d. Set the 3570A controls as follows:

LINEON
MAX/REF INPUT VOLTAGE 0 dBm
BANDWIDTH 3 kHz
PHASE REFERENCE A

e. Set the Synthesizer for an output of 0 dBm, 1 MHz.

f. Connect the DVM (ac function) to A6TP1.

g. Adjust A6L1 (IF OUTPUT ADJ) for a maximum reading on the DVM. Be sure the *absolute peak* is found (intermediate peaks may occur).

h. Connect the DVM to A22TP1.

i. Adjust A22L1 (IF OUTPUT ADJ) for a maximum reading on the DVM. Be sure the *absolute peak* is found.

j. Disconnect the DVM.

k. Observe the front panel phase reading. If the phase reading is greater than ± 2.00 degrees, repeat Steps f through k. If the phase reading is less than ± 2.00 degrees, alternately adjust A6L1 and A22L1 for a phase reading of 00.00 ± 0.05 degrees.

l. This completes the Bandwidth Logic Phase Adjustments. Proceed to the Input Mixer Phase Adjustments (Paragraph 5-51).

5-51. Input Mixer Phase Adjustments.

5-52. These adjustments peak the 100 kHz response of the IF amplifiers on the Input Mixer Assemblies and equalize the phase shift introduced by the Input Mixers.

RECOMMENDED TEST EQUIPMENT:

AC Digital Voltmeter (-hp- Model 3450B)

a. Perform the Log Amplifier Phase Adjustments (for 03570-66535 or 03570-69535 Log Amplifier Boards only) and the Bandwidth Logic Phase Adjustments (Paragraph 5-49).

b. Set the 3570A LINE switch to OFF.

c. Place both Input Mixer Assemblies, A2 and A18, on extenders.

d. Set the 3570A controls as follows:

LINEON
MAX/REF INPUT VOLTAGE 0 dBm
BANDWIDTH 3 kHz
PHASE REFERENCE A

e. Set the Synthesizer for an output of 0 dBm, 1 MHz.

f. Connect the DVM (ac function) to A2 pin 1.

g. Adjust A2L2 and A2L3 for a maximum reading on the DVM. Be sure the *absolute peak* is found (intermediate peaks may occur).

h. Connect the DVM to A18 pin 1.

i. Adjust A18L2 and A18L3 for a maximum reading on the DVM. Be sure the *absolute peak* is found.

j. Disconnect the DVM.

k. Observe the front panel phase reading. If the phase reading is greater than ± 2.00 degrees, repeat Steps f through k. If the phase reading is less than ± 2.00 degrees, alternately adjust A2L2/L3 and A18L2/L3 for a phase reading of 00.00 ± 0.05 degrees.

l. Replace A2 and A18.

m. Observe the front panel phase reading. The phase reading should be 00.00 ± 0.30 degrees. If it is not, repeat the Log Amplifier Phase Adjustments (for 03570-66535 or 03570-69535 Log Amplifier boards only), the Bandwidth Logic Phase Adjustments (Paragraph 5-49), and the Input Mixer Phase Adjustments.

5-53. Crystal Filter Adjustments (3320A and 3320B Frequency Synthesizers).

NOTE

For systems using the Model 3330A or 3330B Automatic Synthesizer, refer to Paragraph 5-55.

5-54. The purpose of these adjustments is to align the three Crystal Filters in each measurement channel. The Crystal Filter adjustments are tedious and time consuming and, for this reason, should be performed only if one of the following conditions exists:

1. If a crystal has been replaced.
2. If a Crystal Filter Assembly has been repaired or replaced.
3. If the 3570A fails to meet the test specifications given in the Bandwidth Checks (Paragraph 5-25).

RECOMMENDED TEST EQUIPMENT:

Electronic Counter (-hp- Model 5245L)
 (2) 6-pin PC Extenders (-hp- Part No. 03570-66503)

NOTE

For the following steps, the front panel ϕ ZERO controls should not have been disturbed since performing the Phase Detector Adjustments (Paragraph 5-15). If the controls have been disturbed, perform the Phase Detector Adjustments before proceeding.

a. Connect the 3570A to the Synthesizer as shown in Figure 5-3(a). Connect the fixed 1 MHz (Δ) to Channel A INPUT.

b. Using short pieces of insulated wire, short between pins 1 and C on each of the two 6-pin PC Extenders supplied with the instrument.

c. Set the 3570A LINE switch to OFF. Remove the second and third Crystal Filter Assemblies, A4 and A5 (or A20, A21). Leave the first Crystal Filter Assembly, A3, (A19) in place.

NOTE

The Crystal Filter boards are matched in their associated crystals and should not be interchanged. Each crystal has a serial number printed on the mica visible from the topside. For identification purposes, the last three digits of the crystal serial numbers are marked in the responding Crystal Filter boards. All crystals can be left in the instrument during the adjustments. Crystals or crystal filter boards may be changed separately if defective. This procedure matches a crystal filter board to its crystal.

d. Place the two 6-pin extenders in the vacant board slots (be sure pin 1 of the extenders is facing the front panel). Leave the two Crystal Filter boards out of the instrument.

e. Using short pieces of solid wire (resistor lead, alligator clip, etc.), short between TP1 and TP2 (Fc CHECK) and between TP3 and TP4 (RI_L) of the Crystal Filter board under test.

f. Set the 3570A controls as follows:

AMPL FUNCTION A or B
 INPUT VOLTAGE 1 V
 BANDWIDTH 100 Hz

g. Set the Synthesizer amplitude to 0 dBm and frequency to 1,000,000.0 Hz (as indicated on the Electronic Counter). Note the 3570A amplitude reading.

NOTE

In the following steps where the Synthesizer frequency adjusted for a peak amplitude reading, be sure the absolute peak is obtained (intermediate peaks will occur).

h. Adjust the Synthesizer frequency for a peak amplitude reading (minimum -dB). The peak will be as much as 10 dB above the 1 MHz reading and must occur between 999,997.5 Hz and 999,999.5 Hz. If the peak reading is not between 999,997.5 Hz and 999,999.5 Hz the corresponding crystal should be replaced. This is because the compensating capacitor (C3* and C4*) on the Crystal Filter board may not be able to "pull" the crystal frequency far enough to meet the frequency specification in Step k.

i. Remove the short from between TP1 and TP2 (Fc CHECK) of the Crystal Filter board under test.

j. Adjust the Synthesizer frequency for a peak amplitude reading (minimum -dB). The absolute peak should occur at 1,000,000 Hz $\pm$ 0.2 Hz. If it does not, change the value of C3* and C4* on the Crystal Filter board under test. Increasing C3* and C4* lowers the peak frequency; decreasing C3* and C4* raises the peak frequency. A change of 100 pF will change the peak frequency by approximately 0.1 Hz. Refer to the Padding List in Table 5-6.

Table 5-6. Padding List.

Description	-hp- Part No.
C - F 22 pF 300 V	0140-0145
C - F 51 pF 300 V	0160-2201
C - F 75 pF 300 V	0160-2202
C - F 100 pF 300 V	0140-0176
C - F 130 pF 300 V	0140-0195
C - F 150 pF 300 V	0140-0196
C - F 180 pF 300 V	0140-0197
C - F 200 pF 300 V	0140-0198
C - F 240 pF 300 V	0140-0199
C - F 300 pF 300 V	0140-0225
C - F 360 pF 300 V	0160-2209
C - F 400 pF 300 V	0140-0177
C - F 460 pF 300 V	0140-0232
C - F 500 pF 300 V	0160-0991
C - F 1000 pF 300 V	0140-0179
C - F 1100 pF 300 V	0160-2219
C - F 1200 pF 300 V	0160-2220
C - F 1300 pF 500 V	0140-0164
C - F 1500 pF 300 V	0160-2222
C - F 1800 pF 300 V	0160-2224
C - F 2000 pF 300 V	0140-0180
C - F 2200 pF 300 V	0160-2226
C - F 2400 pF 500 V	0160-0940
C - F 2500 pF 300 V	0160-0147
C - F 2700 pF 300 V	0160-2228
C - F 3000 pF 100 V	0140-0172
C - F 3300 pF 300 V	0160-2230
C - F 4700 pF 300 V	0140-0162
C - F 5600 pF 300 V	0140-0170

k. Remove the short from between TP3 and TP4 of the Crystal Filter board under test.

l. Set the 3570A BANDWIDTH to 100 Hz.

m. Set the Synthesizer frequency to 995,000.0 Hz and note the 3570A amplitude reading.

n. Set the Synthesizer frequency to 1,005,000.0 Hz and note the 3570A amplitude reading.

o. Adjust the 10 Hz ADJ on the Crystal Filter board under test so that the readings in Steps m and n are identical (within ± 0.25 dB). When optimum adjustment is obtained, the two readings will be approximately -62 dB.

p. Set the Synthesizer frequency to 999,980.0 Hz and note the 3570A amplitude reading.

q. Set the Synthesizer frequency to 1,000,020.0 Hz and note the 3570A amplitude reading.

r. Adjust the 100 Hz ADJ on the Crystal Filter board under test so that the readings in Steps p and q are identical (within ± 0.05 dB).

s. Repeat Steps m through r until optimum adjustment is obtained.

t. Remove A3 (A19) and replace it with the 6-pin PC Extender from the A4 (A20) slot.

u. Repeat Steps e through s for Crystal Filter Assembly, A4 (A20).

v. Remove A4 (A20) and replace it with the 6-pin PC Extender from the A5 (A21) slot.

w. Repeat Steps e through s for Crystal Filter Assembly, A5 (A21).

x. Replace A3 (A19) and A4 (A20), leaving A5 (A21) in place.

y. Repeat Steps p through r. In Step r, adjust the 100 Hz ADJ on the center Crystal Filter board, A4 (A20).

z. Set the 3570A AMPLITUDE FUNCTION switch to B. Move the 1 MHz input from Channel A INPUT to Channel B INPUT.

NOTE

For the following steps, the front panel ϕ ZERO controls should not have been disturbed since performing the Phase Detector Adjustments (Paragraph 5-45). If the controls have been disturbed, perform the Phase Detector Adjustments before proceeding.

aa. Repeat Steps e through y for the A19, A20 and A21 Crystal Filter boards in Channel B.

bb. Set the Synthesizer frequency to 1 MHz. Connect the 3570A in the configuration used to perform the front panel Zero adjustments (see Paragraph 3-157).

cc. Set the 3570A BANDWIDTH to 3 kHz. Note the phase reading.

dd. Set the 3570A BANDWIDTH to 100 Hz. The phase reading should be within ± 2 degrees of the reading noted in Step cc.

ee. Set the 3570A BANDWIDTH to 10 Hz. The phase reading should be within ± 2 degrees of the reading noted in Step cc.

ff. If the phase readings in Steps dd and ee are not within ± 2 degrees of the reading noted in Step cc, repeat the Crystal Filter adjustments.

NOTE

If the error cannot be reduced to within ± 2 degrees by adjustment, one or more of the crystals may be defective.

5-55. Crystal Filter Adjustments (3330A and 3330B Automatic Synthesizers).

NOTE

For systems using the Model 3320A or 3320B Frequency Synthesizer, refer to Paragraph 5-53).

NOTE

This adjustment can be made easier by using the Z-AXIS modulation from the 3570A to mark the center frequency of the crystals. Check the plug-in programming pins on the A33 Address Recognition Board (03570-66567) of the 3570A. Connect the pins in the following position as indicated in Figure 5-5.

5-56. The purpose of these adjustments is to align the Crystal Filters in Channel A and Channel B. The Crystal Filter adjustments are time consuming and, for this reason, should be performed only if one of the following conditions exists:

1. If a crystal has been replaced.
2. If a Crystal Filter Assembly has been repaired or replaced.
3. If the 3570A fails to meet the test specifications given in the Bandwidth Checks (Paragraph 5-25).

RECOMMENDED TEST EQUIPMENT:

- Variable Persistence Oscilloscope (-hp- Model 1201 A)
- (2) 6-pin PC Extenders (-hp- Part No. 03570-66503)

NOTE

The following procedure is performed first for Channel A and then again for Channel B. The Channel A Crystal Filter boards are A3, A4 and A5; the Channel B Crystal Filter boards are A19, A20 and A21.

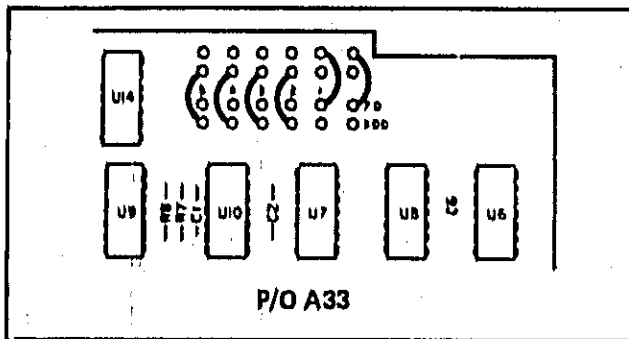


Figure 5-5. Part of Address Recognition Board Showing Current Position of Jumpers.

- a. Connect the 3570A to the Synthesizer as shown in Figure 5-3(a). Connect the fixed 1 MHz (Δ) to Channel A INPUT.

- b. Using short pieces of insulated wire, short between pins 1 and C on each of the two 6-pin PC Extenders supplied with the instrument.

- c. Set the 3570A LINE switch to OFF. Remove the second and third Crystal Filter Assemblies, A4 and A5 (or A20, A21). Leave the first Crystal Filter Assembly, A3 (A19), in place.

NOTE

The Crystal Filter boards are matched to their associated crystals and should not be interchanged. Each crystal has a serial number printed on the mica which is visible from the top side. For identification purposes, the last three digits of the crystal serial numbers are marked on the corresponding Crystal Filter boards. All crystals can be left in the instrument while the adjustments are being performed. Crystals or crystal filter boards may be changed separately if defective. This procedure matches a crystal filter board to its crystal.

- d. Place the two 6-pin extenders in the vacant board slots (be sure pin 1 of the extenders is facing the front panel). Leave the two Crystal Filter boards out of the instrument.

- e. Using short pieces of solid wire (resistor lead, alligator clip, etc.) short between TP1 and TP2 (Fc CHECK) and between TP3 and TP4 (FL) of the Crystal Filter board under test.

- f. Set the 3570A controls as follows:

```

LINE ..... ON
MAX/REF INPUT VOLTAGE ..... 1 V
AMPLITUDE FUNCTION ..... A
                        (Channel A adjustments)
BANDWIDTH ..... 10 Hz
PHASE REFERENCE ..... A

```

- g. Set the Synthesizer as follows:

FREQUENCY 1 MHz
FREQUENCY STEP 0.1 Hz

TIME/STEP 300 msec
AMPLITUDE (No Effect)

- h. Connect the Synthesizer SWEEP OUTPUT to the Horizontal Input of the scope. Connect the 3570A rear panel AMPLITUDE FUNCTION output to the Vertical Input of the scope.

1. Set the scope controls as followst

Horizontal (Ext.) 1 V/div
Vertical Sensitivity 1 V/div (dc coupled)

NOTE:

In the following steps where the Synthesizer frequency is adjusted for a peak amplitude reading, be sure the absolute peak is obtained (intermediate peaks will occur).

- j. Note the 3570A amplitude reading.

- k. Using the FREQ ↑ and FREQ ↓ keys, adjust the Synthesizer frequency for a peak amplitude reading (minimum - dB). The absolute peak will be as much as 10 dB above the 1 MHz reading (Step j) and must occur at 1,000,000.0 Hz ± 0.2 Hz. If the peak reading does not occur at this frequency, the corresponding crystal should be replaced.

1. Remove the short from between TP1 and TP2 (Fe CHECK) of the Crystal Filter board under test.

- m. Adjust the Synthesizer frequency for a peak amplitude reading (minimum - dB). The absolute peak should occur at 1,000,000.0 Hz $\pm$ 0.2 Hz. If it does not, change the value of C3* and C4* on the Crystal Filter board under test. Increasing C3* and C4* lowers the peak frequency; decreasing C3* and C4* raises the peak frequency. A change on 100 pF will change the peak frequency by approximately 0.1 Hz. Refer to the Padding List in Table 5-6.

- n. Remove the short from between TP3 and TP4 of the Crystal Filter board under test.

- c. Set the 3570A BANDWIDTH to 100 Hz.**

- p. Set the Synthesizer as follows:

```

FREQUENCY ..... 1 MHz
FREQUENCY STEP ..... 20 Hz
TIME/STEP ..... 3 msec
STEPS ..... 1000
SWEEP ..... UP

```

Connect the Z-AXIS output on the 3570A to the Z-AXIS Input on the Oscilloscope.

- q. Start the sweep by pressing **START CONT.**

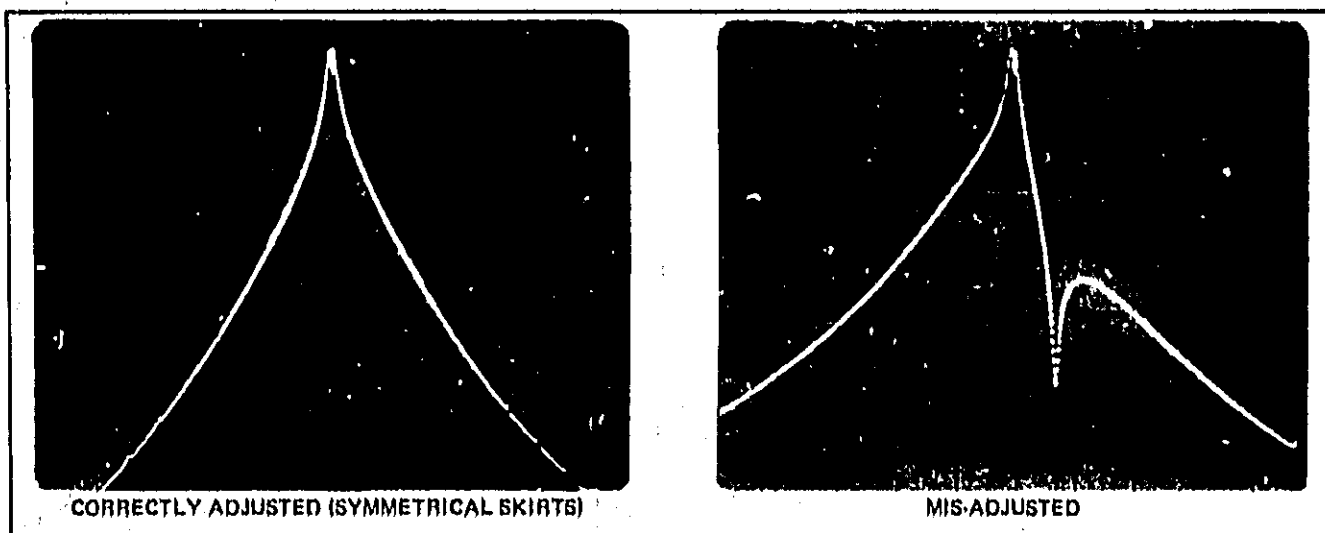


Figure 5-6. Crystal Filter Response: 10 Hz Adjustment.

r. Adjust the 3570A Z-AXIS intensity control for a bright dot on the trace being displayed by the scope. This is the 100 kHz center frequency of the crystal. Adjust the oscilloscope control so this marker is in the center of the display. This marker can then be used in all future steps as a center reference point.

s. Adjust the 10 Hz ADJ on the Crystal Filter board under test for symmetrical skirts (see Figure 5-6).

t. Set the Synthesizer as follows:

FREQUENCY 1 MHz
 FREQUENCY STEP 1 Hz
 TIME/STEP 30 msec
 STEPS 100
 SWEEP UP

u. Set the oscilloscope Vertical Sensitivity to 0.1 V/div.

v. Start the sweep by pressing START CONT.

w. Adjust the 100 Hz ADJ on the Crystal Filter board under test so that the filter response peaks at exactly 100 kHz (center of display). The skirts should be symmetrical about the center frequency (see Figure 5-7).

x. Remove A3 (A19) and replace it with the 6-pin extender from the A4 (A20) slot. Repeat Steps e through w for Crystal Filter Assembly, A4 (A20).

y. Remove A4 (A20) and replace it with the 6-pin extender from the A5 (A21) slot. Repeat Steps e through w for Crystal Filter Assembly, A5 (A21).

z. Remove the extenders. Replace A3 (A19) and A4 (A20), leaving A5 (A21) in place.

aa. Set the oscilloscope vertical sensitivity to 1 V/div. Repeat Steps p through 4 (In Step p, set the Synthesizer FREQUENCY STEP to 2 Hz).

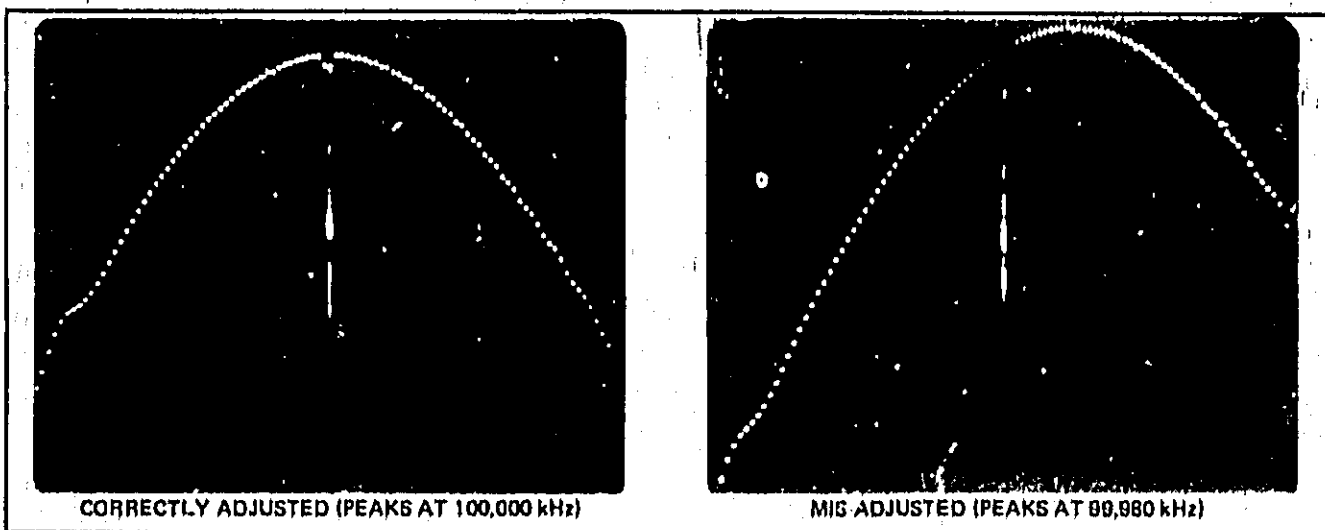


Figure 5-7. Crystal Filter Response: 100 Hz Adjustment.

bb. Check the symmetry of the filter skirts. If the skirts are not symmetrical, alternately adjust the three 10 Hz ADJ capacitors for optimum symmetry.

cc. Repeat Steps t through v.

dd. The filter response should peak at exactly 100 kHz (center of display) and the filter skirts should be symmetrical about the peak frequency. If necessary, adjust the three 100 Hz ADJ capacitors to obtain the proper peak response.

ee. Repeat Steps c through dd for the A19, A20 and A21 Crystal Filter boards in Channel B. (Set the AMPLITUDE FUNCTION switch to B.)

NOTE

For the following steps, the front panel ϕ ZERO controls should not have been disturbed since performing the Phase Detector Adjustments (Paragraph 5-45). If the controls have been disturbed, perform the Phase Detector Adjustments before proceeding.

ff. Set the Synthesizer frequency to 1 MHz. Connect the 3570A in the configuration required to perform the front panel Zero Adjustments (Paragraph 3-157).

gg. Set the 3570A BANDWIDTH to 3 kHz. Note the phase reading: _____ degrees.

hh. Set the 3570A BANDWIDTH to 100 Hz. The phase reading should be within ± 2 degrees of the reading noted in Step gg. If it is not, repeat the Crystal Filter adjustments.

ii. Set the 3570A BANDWIDTH to 10 Hz. The phase reading should be within ± 2 degrees of the reading noted in Step gg. If it is not, repeat the Crystal Filter adjustments.

NOTE

If the error cannot be reduced to within ± 2 degrees by adjustment, one or more crystals may be defective.

jj. This completes the Crystal Filter Adjustment procedure. Reconnect the RF Input Cable to the OUTPUT or ALT OUTPUT $\bigcirc$ of the Synthesizer.

5-57. LO Feedthrough Adjustments.

5-58. These adjustments balance the active mixers on the Input Mixer Assemblies, A2 and A18. In the following procedure, the Synthesizer frequency is set to 0 Hz, making the Local Oscillator frequency equal to the 100 kHz IF frequency. When the mixer is balanced, the 100 kHz LO signal is cancelled and is not fed into the IF section. This results in a minimum reading on the front panel Amplitude display.

a. Disconnect the input cables from the A and B INPUT terminals. Leave the terminations connected.

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

c. Set the Synthesizer frequency to 0 Hz (LEVELING OFF).

d. Adjust A2R26 (LO FEEDTHROUGH ADJ) for a minimum reading (maximum -dB) on the front panel Amplitude display. The reading should be -60.00 dB or below.

e. Set the 3570A AMPLITUDE FUNCTION switch to B.

f. Adjust A18R26 (LO FEEDTHROUGH ADJ) for a minimum reading (maximum -dB) on the front panel Amplitude display. The reading should be -60.00 dB or below.

g. Reconnect the A and B OUTPUTS, terminated in 50 - ohm (or 75 - ohm) loads, to the A and B INPUTS.

5-59. RF Feedthrough Adjustments.

5-60. These adjustments balance the LO limiter stages on the Input Mixer Assemblies, A2 and A18, resulting in minimum feedthrough of the 100,001 Hz input signal.

a. Set the Synthesizer as follows:

FREQUENCY 100,001
AMPLITUDE 0 dB

b. Set the 3570A as follows:

AMPLITUDE FUNCTION A
MAX/REF INPUT VOLTAGE 0 dBm
BANDWIDTH 10 Hz

c. Connect a jumper from A37TP5V to A11 VCXO Control Test Point.

d. Adjust A2R9 for -60 dB or lower (3570A front panel reading).

e. Repeat the above steps for Channel B.

A7 5-61. Log Amplifier Adjustments.

(For instruments equipped with 03570-66555 or 03570-69555 Rev. C Log Amplifier Boards only. See the 3570A Manual Section VIII for instruments equipped with 03570-66535, 03570-69535 or Revision B of the above Log Amplifier Boards.)

A7 5-62. The following adjustments establish the amplitude linearity of the A and B Log Amplifiers, A7 or A23.

RECOMMENDED TEST EQUIPMENT:

AC/DC Digital Voltmeter (-hp- Model 3450B)
Variable Attenuator (-hp- Model 35511)

For 75 - ohm systems:

50 - ohm to 75 - ohm Adapter (see Figure 5-2 for 75 - ohm systems)

453 - ohm resistor

BNC to Clip Lead Adapter

NOTES

1. The following procedure is performed first for Channel A and then again for Channel B. The Channel A adjustments are located on Channel A Log Amplifier Assembly, A7; the Channel B adjustments are located on the Channel B Log Amplifier Assembly, A23.

2. Steps a to d of the following procedure need to be performed *ONLY* in cases where L3 or C27 of the log Amplifier have been replaced.

a. Read Note 2 before proceeding. Place the A7/23 assembly on an extender board and set the Synthesizer to 300 kHz and +13 dBm. Connect the Synthesizer as shown in Figure 5-8.

b. Remove the log amp (U5) and, using a 453 ohm (hp-0698-3510) series resistor, connect the signal from the Synthesizer to pin 11 of the U5 socket.

c. Connect the Oscilloscope to TP2 and adjust L3 for a voltage null at TP2.

d. Remove the signal and the resistor from pin 11 and replace U5.

e. Connect the 355D variable attenuator in the channel under test as shown in Figure 5-3(b).

f. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION CHANNEL
UNDER TEST
BANDWIDTH 10 Hz

g. Set the Variable Attenuator to 0 dB and the Synthesizer to 0 dBm, 1 MHz. (Place the Log Amplifier to be adjusted on an extender board.)

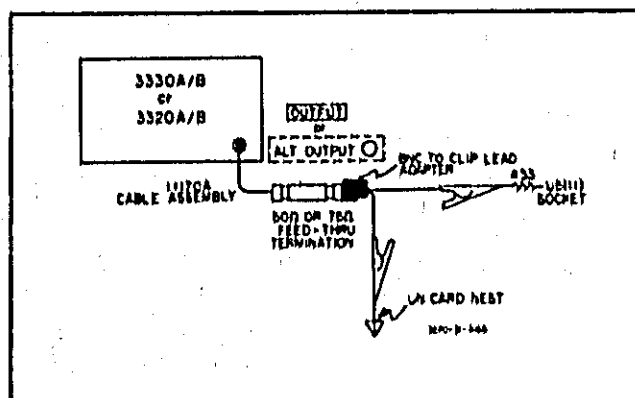


Figure 5-8. L3 Adjustments.

h. Adjust R13 (0 dB ADJ) clockwise until the pot starts clicking. Then turn R13 counterclockwise 4 turns.

i. For 50 ohm systems, proceed to Step j. For 75 ohm systems, perform the following:

1. Install the 75-to 50-ohm adapter between the front panel output of the 3570A and the attenuator as shown in Figure 5-3(b). The output of the attenuator should be terminated in 50 ohms.

2. Connect the 3450B DVM to the attenuator output.

3. Adjust the Synthesizer Amplitude for a DVM reading of 0.2739 V rms.

4. Disconnect the DVM and connect the attenuator output to Channel A input.

j. Connect the DVM (dc function) to TP1 of the Log Amplifier.

k. Adjust R23 (SLOPE ADJ) for a DVM reading of +5.00 V dc.

l. Adjust the front panel AMP ZERO control for a reading of 00.00 dB on the front panel Amplitude display.

m. Set the Variable Attenuator to 30 dB.

n. The front panel amplitude display should read -30.00 ± .02 dB. If not, compute the error and triple it. Record your results.

Example: Amplitude display of -29.50 dB
Error = -29.50 - (-30.00 dB) = +0.50 dB
0.50 dB x 3 = +1.50 dB

o. Set the Variable Attenuator to 0 dB.

p. Adjust R23 (SLOPE ADJ.) for a front panel Amplitude display equal to the value recorded in Step n (± .01 dB).

q. Adjust the front panel AMP ZERO control for a reading of 00.00 dB ± .01 dB.

r. Repeat Steps m through q until readings of -30.00 dB and 00.00 dB are obtained. Return to 00.00 dB.

s. Set variable attenuator to 10 dB.

t. The front panel should read -10.00 dB ± .12 dB. If not, compute the error, triple it, and change its sign. Record your results.

Example: Amplitude display of -9.95 dB
Error = -9.95 - (-10.00) = +.05
3 x .05 = +.15
Result = -.15

u. Adjust R13 (0 dB ADJ) for a front panel amplitude display equal to the result of Step t. Set variable attenuator to 0 dB.

v. Adjust the front panel AMP ZERO control for a reading of 0.00 dB $\pm$.01 dB.

w. Repeat Steps s through v.

x. The slope and 0 dB adjustments interact. Repeat Steps m through w until both -10 and -30 dB read within $\pm$.05 dB of the correct value.

y. Set the variable attenuator to 50 dB and adjust R36 for a display of -50.00 dB $\pm$.30 dB.

z. Set the Synthesizer to -50 dB and the variable attenuator to -20 dB. Adjust R37 for a display of -70.00 $\pm$.3 dB.

aa. Set the synthesizer to -50 dB and the variable attenuator to 40 dB. Adjust R38 for a display of -90.00 $\pm$.8 dB.

bb. Set the variable attenuator to 50 dB. Adjust R39 for a display of -100.00 $\pm$.8 dB. The reading will vary and it will be necessary to try to set -100.00 at the center of the variations.

cc. Use Table 5-7 to verify proper Log Amplifier performance.

5-63. High Frequency Phase Adjustments.

(For instruments equipped with 03570-66551, 03570-69551, 03570-66558, or 03570-69558 Input Amplifier Boards. For instruments equipped with 03570-66531, 03570-69531, 03570-66528, or 03570-69528 Input Amplifier Boards, see Manual Backdating.)

5-64. These adjustments set the Input Amplifiers (A1 and A17) and the LO Buffer, A9, for optimum (flat) phase vs. frequency response.

a. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
BANDWIDTH 10 Hz
PHASE REFERENCE A

Table 5-7. Amplifier Adjustments.

3570A Input	Attenuator Setting	Synthesizer* Setting	Test Tolerance
0 dBm	0 dB	0 dB	0 dB $\pm$ 0.05 dB
-10 dBm	10 dB	0 dB	-10 dB $\pm$ 0.15 dB
-20 dBm	20 dB	0 dB	-20 dB $\pm$ 0.15 dB
-30 dBm	30 dB	0 dB	-30 dB $\pm$ 0.3 dB
-40 dBm	40 dB	0 dB	-40 dB $\pm$ 0.3 dB
-50 dBm	50 dB	0 dB	-50 dB $\pm$ 0.3 dB
-60 dBm	10 dB	-50 dB	-60 dB $\pm$ 0.3 dB
-70 dBm	20 dB	-50 dB	-70 dB $\pm$ 0.3 dB
-80 dBm	30 dB	-50 dB	-80 dB $\pm$ 0.3 dB
-90 dBm	40 dB	-50 dB	-90 dB $\pm$ 0.3 dB
-100 dBm	50 dB	-50 dB	-100 dB $\pm$ 0.3 dB

*For 75-ohm systems, 0 dB corresponds to the level set up in Step e; -50 dB corresponds to a synthesizer setting 50 dB lower than that in Step e.

b. Set the Synthesizer for an output of 0 dBm, 10 kHz.

c. Adjust the front panel 10 Hz ϕ ZERO control for a phase reading of 00.00 degrees.

d. Set the Synthesizer frequency to 13 MHz.

e. Adjust A9C6 (LO PHASE ADJ) for a phase reading as close to 00.00 degrees as possible. ($\pm 1^\circ$ is the specification, although $\pm .5^\circ$ or better should be realizable.)

f. Set the Synthesizer frequency to 1 MHz.

g. If necessary, adjust A9C6 (LO PHASE ADJ) for a phase reading of 0 $\pm$ 0.2 degrees. If this cannot be done or if the 13 MHz reading is no longer well within the $\pm 1^\circ$ phase error specification, perform Steps i through l. Otherwise, perform Step h.

h. Note the phase readings with the Synthesizer frequency set to 500 kHz, 1 MHz, 5 MHz, and 13 MHz. At each frequency the phase error from 00.00 $^\circ$ should be well within the Phase Accuracy Frequency Response Specifications listed in Table 1-1. If any of the readings are out of tolerance, repeat Steps b through h. Otherwise, the High Frequency Phase Adjustments are completed.

i. Adjust A9C6 (LO PHASE ADJ) such that the two sets of blades of the capacitor are "half-way" engaged.

j. Set the Synthesizer to a frequency of 1 MHz and 13 MHz. Note the polarity and magnitude of the phase error at each frequency.

1 MHz _____ 13 MHz _____

k. Select either A2C8* or A18C8* to bring both of these frequency points well within tolerance ($\pm .2^\circ$ for 1 MHz and $\pm 1^\circ$ for 13 MHz). If the phase error is positive, select A18C8*. If the phase error is negative, select A2C8*. Use the following information in the selection:

1. The typical value of each capacitor is 2 pF (hip Part No. 0150-0031).
2. Increasing the value of A2C8* will increase the phase reading.
Decreasing the value of A2C8* will decrease the phase reading.
3. A18C8* has the opposite effect as A2C8*. Increasing the value of A18C8* will decrease the phase reading while decreasing it will increase the phase reading.

4. Use the following value of capacitors:

.68 pF	0150-0046
1.0 pF	0150-0029
1.5 pF	0150-0011
2.0 pF	0150-0031
2.2 pF	0150-0015
3.3 pF	0150-0022

1. Do Step h.

5-65. Bandwidth Gain Switching Adjustment.

(For instruments equipped with 03570-66553, A5A21 Crystal Filter Boards only. This adjustment is not necessary for instruments equipped with 03570-66535, A5/A21 Crystal Filter Boards.)

5-66. This adjustment sets the three bandwidth filter gains equally so that little or no front panel adjustment is necessary when switching between bandwidths.

a. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 3 kHz

b. Set the synthesizer to:

AMPLITUDE 0 dBm
FREQUENCY 1 MHz

c. Adjust the front panel A AMP ZERO control for a reading of 00.00 dB on the front panel Amplitude display.

d. Set the 3570A controls to:

BANDWIDTH 100 Hz

e. Adjust A4(or A21)R14 for a front panel indication of 00.00 dB.

f. Set the 3570A controls to:

BANDWIDTH 10 Hz

g. Adjust A4(or A21)R15 for a front panel indication of 00.00 dB.

h. Repeat Steps a through g for Channel B.

5-67. Overload Indicator Adjustments.

5-68. These adjustments set the thresholds for the A and B Overload (OL) indicators.

a. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 100 Hz

b. Set the Synthesizer for an output of 0 dBm, 1 MHz.

c. Adjust the front panel A AMP ZERO control for a reading of 00.00 dB on the front panel Amplitude display.

d. Adjust the Synthesizer amplitude for a 3570A amplitude reading of + 0.80 dB.

e. Set A6R7 (A OL ADJ) and A22R7 (B OL ADJ) fully counterclockwise.

f. Adjust A6R7 (A OL ADJ) until the front panel A_{OL} annunciator illuminates. Do not adjust R7 any further than necessary to obtain the overload indication.

g. Adjust A22R7 (B OL ADJ) until the front panel B_{OL} annunciator illuminates. Do not adjust R7 any further than necessary to obtain the overload indication.

h. Repeat Steps b and c.

i. Adjust the Synthesizer amplitude for a reading of + 0.7 dB on the front panel Amplitude display. Both A_{OL} and B_{OL} should be out.

5-69. Delay Crossover Adjustment (Options 002, 003 Only).

5-70. This adjustment sets the polarity convergence of the delay analog output amplifier.

RECOMMENDED TEST EQUIPMENT:

Oscilloscope (hp- Model 180A)

DC Digital Voltmeter (hp- Model 3450B)

a. Connect the Horizontal Input of the Oscilloscope to the SWEET OUTPUT of the 3330A/B. Connect the Vertical Input of the Oscilloscope to the rear panel PHASE/DELAY output of the 3570A. Connect the Z AXIS from the 3570A to the Oscilloscope.

b. Set the Oscilloscope controls as follows:

Horizontal Sensitivity 1 V/div
Vertical Sensitivity 0.2 V/div
(de coupled)

c. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
BANDWIDTH 3 kHz
PHASE REFERENCE A
PHASE/DELAY DELAY
DELAY MODE SWP
Frequency Step 20 Hz
Frequency Step Multiplier X100
(white)

d. Set the 3330A/B as follows:

AMPLITUDE 0 dBm
FREQUENCY 1 MHz
FREQUENCY STEP 1 kHz
STEPS 10
TIME/STEP 1 msec
SWEEP FREQ./UP

e. Adjust the 3 kHz Bandwidth (3570A) zero adjust for 00.00° phase on the front panel. Start the 3330A/B sweep by pressing START CONT.

f. The front panel Delay display should rapidly alternate between +00.00 and -00.00. One row of dots should appear across the oscilloscope screen. If two rows appear, adjust A24R16 (DELAY ANALOG ADJ) until the two rows merge together.

g. Put A.16 on an extender.

h. Ground pin "0" of R50.

i. Put a dc voltmeter on pin #1 of A24.

j. Adjust R51 of A17 until the voltmeter reads 0.000 V dc at pin #1 of A24.

5-71. PHASE vs. AMPLITUDE ADJUSTMENT.

5-72. This adjustment corrects for a Phase reading which is not within the tolerances set in Table 5-4 for Phase vs. Amplitude (Channel A within -6 dB of Channel B).

RECOMMENDED TEST EQUIPMENT

2 Variable Attenuators (355D)

a. Connect the Attenuators as shown in Figure 5-3(b).

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 1 V
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz
PHASE REFERENCE A

Options 002, 003: Set PHASE/DELAY switch to PHASE; ABSOLUTE/RELATIVE switches to ABSOLUTE.

c. Set the Synthesizer controls as follows:

FREQUENCY 1 MHz
AMPLITUDE 13 dBm
TIME/STEP 300

d. Adjust the front panel 10 Hz Bandwidth Zero until the Phase display reads zero.

e. Step the Channel A Attenuator in 10 dB steps to -80 dB and record each Phase reading with its sign. Return the Channel A Attenuator to 0 dB.

f. Step the Channel B Attenuator in 10 dB steps to -80 dB and record each Phase reading with its sign. Return the Channel B Attenuator to 0 dB.

g. Compare the results of Channel A to Channel B at each 10 dB step. (The ideal condition is for Channel A to be just as positive as Channel B is negative.)

h. Selection of A7/A23 C1, C5, C8 or C12 will bring the Phase reading into tolerances specified in Table 5-4. Use the following information in the selection.

1. Increasing the capacitance makes the phase reading more negative and decreasing the capacitance makes the phase reading more positive.

2. Make the necessary corrections to A7 for Channel A and to A23 for Channel B.

3. The capacitors exert their influence as follows:

Capacitor	Range
C1	0 - 20 dB
C5	20 - 50 dB
C8	50 - 80 dB
C12	80 - 100 dB

4. Use the following values of capacitors:

.0012 μ F	0160-0297
.0015 μ F	0160-0298
.0022 μ F	0160-0154
.0027 μ F	0160-0300
.0033 μ F	0160-0155
.0047 μ F	0160-0157
.0068 μ F	0160-0159
.01 μ F	0160-0161
.015 μ F	0160-0194
.018 μ F	0160-0302
.022 μ F	0160-2230

5. Allow at least 10 minutes after changing the cap so it can cool (soldering heat will affect the readings).

i. Having made the necessary corrections repeat Paragraph 5-21 (Amplitude vs. Phase) Steps e and f.

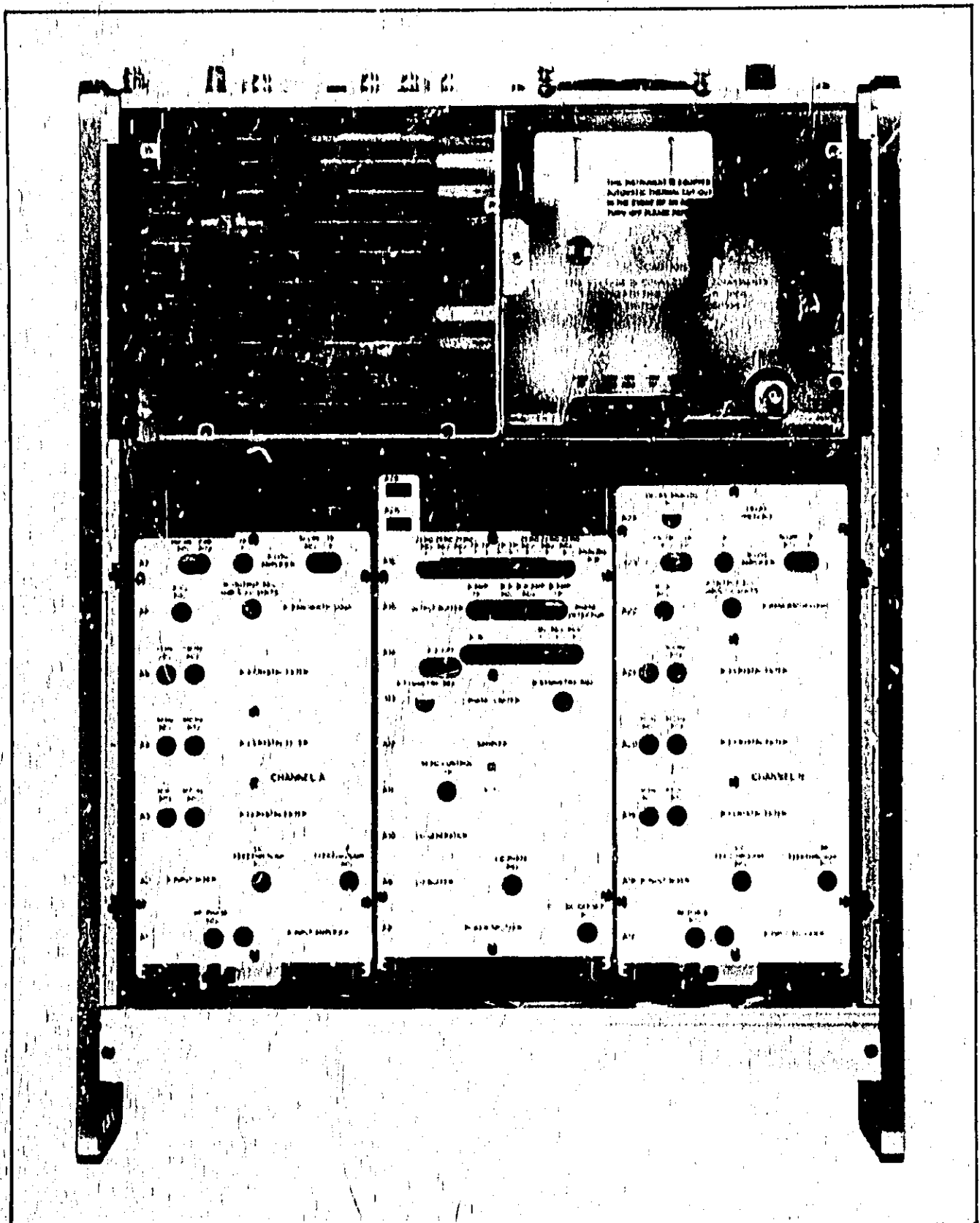


Figure 5-9. Adjustment Locations (Top View).

PERFORMANCE CHECK TEST CARD

Hewlett-Packard Model 3570A

Network Analyzer

Serial No. _____

Tests Performed By _____

Date _____

INPUT IMPEDANCE CHECK

Test Channel	Ampl. Reading	Ampl. Tolerance	Phase Reading	Phase Tolerance
B	_____ dB	> 5.94 dB to < 6.11 dB	_____ deg.	< 45 deg.
A	_____ dB	> 5.94 dB to < 6.11 dB	_____ deg.	< 45 deg.

DYNAMIC RANGE CHECK

Bandwidth Setting	A Ampl. Reading	B Ampl. Reading	Test Tolerance
10 Hz	_____ dB	_____ dB	> > 100 dB
100 Hz	_____ dB	_____ dB	> > 100 dB
3 kHz	_____ dB	_____ dB	> > 100 dB

PERFORMANCE CHECK TEST CARD (Cont'd)

RELATIVE AMPLITUDE CHECKS

Synth. Amplitude Paragraph 6-14 Step 3	Synth. Frequency	Variable Attenuator	A Amplitude Reading	B Amplitude Reading	Test Tolerance
0 dB	50 Hz	0 dB	_____ dB	_____ dB	± 0.01 dB*
-20 dB	50 Hz	0 dB	_____ dB	_____ dB	± 0.2 dB
-40 dB	50 Hz	0 dB	_____ dB	_____ dB	± 0.5 dB
-60 dB	50 Hz	0 dB	_____ dB	_____ dB	± 0.5 dB
0 dB	10 kHz	0 dB	_____ dB	_____ dB	± 0.01 dB*
0 dB	10 kHz	-20 dB	_____ dB	_____ dB	± 0.2 dB
0 dB	10 kHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	10 kHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	10 kHz	-60 dB	_____ dB	_____ dB	± 1.5 dB
0 dB	100 kHz	0 dB	_____ dB	_____ dB	± 0.01 dB*
0 dB	100 kHz	-20 dB	_____ dB	_____ dB	± 0.2 dB
0 dB	100 kHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	100 kHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	100 kHz	-60 dB	_____ dB	_____ dB	± 1.5 dB
0 dB	1 MHz	0 dB	_____ dB	_____ dB	± 0.01 dB*
0 dB	1 MHz	-20 dB	_____ dB	_____ dB	± 0.2 dB
0 dB	1 MHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	1 MHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	1 MHz	-60 dB	_____ dB	_____ dB	± 1.5 dB
0 dB	7 MHz	0 dB	_____ dB	_____ dB	± 0.01 dB*
0 dB	7 MHz	-20 dB	_____ dB	_____ dB	± 0.2 dB
0 dB	7 MHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	7 MHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	7 MHz	-60 dB	_____ dB	_____ dB	± 1.5 dB
0 dB	13 MHz	0 dB	_____ dB	_____ dB	± 0.01 dB*
0 dB	13 MHz	-20 dB	_____ dB	_____ dB	± 0.2 dB
0 dB	13 MHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	13 MHz	-40 dB	_____ dB	_____ dB	± 0.5 dB
-40 dB	13 MHz	-60 dB	_____ dB	_____ dB	± 1.5 dB

* Maintain this tolerance using front panel AMP, ZERO adjustments.

PERFORMANCE CHECK TEST CARD (Cont'd)

FREQUENCY RESPONSE CHECKS

Synthesizer Frequency	A Amplitude Readings	B Amplitude Readings	B - A Readings
50 Hz	_____ dB	_____ dB	_____ dB
100 Hz	_____ dB	_____ dB	_____ dB
1 kHz	_____ dB	_____ dB	_____ dB
10 kHz	_____ dB	_____ dB	_____ dB
100 kHz	_____ dB	_____ dB	_____ dB
1 MHz	_____ dB	_____ dB	_____ dB
10 MHz	_____ dB	_____ dB	_____ dB
13 MHz	_____ dB	_____ dB	_____ dB

PHASE VS. FREQUENCY
PHASE VS. AMPLITUDE CHECK

Channels at Different Levels

Frequency 1 MHz				Readings	
Channel A	Channel B	Range*			
		1 V Phase	.1 V Phase	1 V Range	.1 V Range
0 dB	-20 dB	± 1.3°	± 1.3°	_____	_____
0 dB	-40 dB	± 1.5°	± 1.5°	_____	_____
0 dB	-60 dB	± 1.5°	± 1.5°	_____	_____
0 dB	-80 dB	± 3.0°	± 4.5°	_____	_____
-20 dB	0 dB	± 1.3°	± 1.3°	_____	_____
-40 dB	0 dB	± 1.5°	± 1.5°	_____	_____
-60 dB	0 dB	± 1.5°	± 1.5°	_____	_____
-80 dB	0 dB	± 3.5°	± 4.5°	_____	_____

PERFORMANCE CHECK TEST CARD (Cont'd)

PHASE VS. FREQUENCY,
PHASE VS. AMPLITUDE CHECKS
(CONTINUED)

Synth. Frequency	Amplitude Setting	Phase Reading	Tolerance (0 Degrees)
50 Hz	0 dB	_____	± 1.2
50 Hz	-20 dB	_____	± 1.2
50 Hz	-70 dB	_____	± 1.4
50 Hz	-80 dB	_____	± 1.8
100 Hz	0 dB	_____	± 0.6
100 Hz	-20 dB	_____	± 0.6
100 Hz	-70 dB	_____	± 0.8
100 Hz	-80 dB	_____	± 1.2
500 Hz	0 dB	_____	± 0.6
500 Hz	-20 dB	_____	± 0.6
500 Hz	-70 dB	_____	± 0.8
500 Hz	-80 dB	_____	± 1.2
1 kHz	0 dB	_____	± 0.6
1 kHz	-20 dB	_____	± 0.6
1 kHz	-70 dB	_____	± 0.8
1 kHz	-80 dB	_____	± 1.2
15 kHz	0 dB	_____	± 0.6
15 kHz	-20 dB	_____	± 0.6
15 kHz	-70 dB	_____	± 0.8
15 kHz	-80 dB	_____	± 1.2
30 kHz	0 dB	_____	± 0.6
30 kHz	-20 dB	_____	± 0.6
30 kHz	-70 dB	_____	± 0.8
30 kHz	-80 dB	_____	± 1.2
100 kHz	0 dB	_____	± 0.6
100 kHz	-20 dB	_____	± 0.6
100 kHz	-70 dB	_____	± 0.8
100 kHz	-80 dB	_____	± 1.2
500 kHz	0 dB	_____	± 0.6
500 kHz	-20 dB	_____	± 0.6
500 kHz	-70 dB	_____	± 0.8
500 kHz	-80 dB	_____	± 1.2
1 MHz	0 dB	_____	± 0.6
1 MHz	-20 dB	_____	± 0.6
1 MHz	-70 dB	_____	± 0.8
1 MHz	-80 dB	_____	± 1.2
7 MHz	0 dB	_____	± 1.4
7 MHz	-20 dB	_____	± 1.4
7 MHz	-70 dB	_____	± 1.6
7 MHz	-80 dB	_____	± 2.0
13 MHz	0 dB	_____	± 1.4
13 MHz	-20 dB	_____	± 1.4
13 MHz	-70 dB	_____	± 1.6
13 MHz	-80 dB	_____	± 2.0

PERFORMANCE CHECK TEST CARD (Cont'd)

PHASE LINEARITY CHECK

Synthesizer Frequency	Phase Reading	Phase Change
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____

BANDWIDTH CHECKS

Bandwidth	A1	A2	F1	F2	F3	Results ± 15% BW/2
10 Hz	_____	_____	_____	_____	_____	_____
100 Hz	_____	_____	_____	_____	_____	_____
3 kHz	_____	_____	_____	_____	_____	_____

DELAY MEASUREMENT CHECK

Freq Step	Step Multiplier	Δf Setting	Delay Reading	Lower Limit	Upper Limit
5	X1	5 Hz	_____	19.96 msec	20.04 msec
10	X1	10 Hz	_____	9.98 msec	10.02 msec
16.6	X1	16.6 Hz	_____	5.99 msec	6.01 msec
20	X1	20 Hz	_____	4.99 msec	5.01 msec
5	X10	50 Hz	_____	1.996 msec	2.004 msec
10	X10	100 Hz	_____	0.998 msec	1.002 msec
16.6	X10	166 Hz	_____	0.599 msec	0.601 msec
20	X10	200 Hz	_____	0.499 msec	0.501 msec
5	X100	500 Hz	_____	0.1996 msec	0.2004 msec
10	X100	1 kHz	_____	0.0998 msec	0.1002 msec
16.6	X100	1.66 kHz	_____	0.0599 msec	0.0601 msec
20	X100	1 kHz	_____	0.0499 msec	0.0501 msec
5	X1 K	5 kHz	_____	19.96 μsec	20.04 μsec
10	X1 K	10 kHz	_____	9.98 μsec	10.02 μsec
16.6	X1 K	16.6 kHz	_____	5.99 μsec	6.01 μsec
20	X1 K	20 kHz	_____	4.99 μsec	5.01 μsec
5	X10 K	50 kHz	_____	1.996 μsec	2.004 μsec
10	X10 K	100 kHz	_____	0.998 μsec	1.002 μsec
16.6	X10 K	166 kHz	_____	0.599 μsec	0.601 μsec
20	X10 K	200 kHz	_____	0.499 μsec	0.501 μsec

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts. Table 6-1 is a standard table of abbreviations, Table 6-2 is a code list of manufacturers and Table 6-3 lists parts in alphanumeric order of their reference designators and indicates the description, ship part number of each part, together with any applicable notes, and provides the following:

- a. Total quantity used in the instrument (Qty column). The total quantity of a part is given the first time the part number appears.
- b. Description of the part. (See Table 6-1 below.)
- c. Typical manufacturer of the part in a five-digit code. (See Table 6-2.)
- d. Manufacturers part number.

6-3. Miscellaneous parts are listed at the end of Table 6-3.

6-4. ORDERING INFORMATION.

6-5. To obtain replacement parts, address order or inquiry to your local Hewlett-Packard Field Office. (See Appendix A for list of office locations.) Identify parts by their Hewlett-Packard part numbers. Include instrument model and serial numbers.

6-6. NON-LISTED PARTS.

6-7. To obtain a part that is not listed, include:

- a. Instrument model number.
- b. Instrument serial number.
- c. Description of the part.
- d. Function and location of the part.

6-8. PROPRIETARY PARTS.

6-9. Items marked by a dagger (†) in the reference designator column are available only for repair and service of Hewlett-Packard instruments.

Table 6-1. Standard Abbreviations.

ABBREVIATIONS					
Ag	silver	Hz	hertz (cycle/s) per second	NP	negative positive n.p.
Al	aluminum	ID	inside diameter	ns	(zero temperature coefficient) nanosecond(s) = 10 ⁻⁹ seconds
A	ampere(s)	imp	impregnated	nr	not separately replaceable
Au	gold	incd	incandescent		
C	capacitor	ins	insulation(s)		
cer	ceramic	kΩ	kiloohm(s) = 10 ³ ohms		
coef	coefficient	kHz	kiloherz = 10 ³ hertz	Ω	ohm(s)
com	common			abd	order by description
comp	composition			OD	outside diameter
conn	connection				
dep	deposited	L	inductor	P	peak
DPDT	double pole double throw	lin	linear taper	pA	picoampere(s)
DPST	double pole single throw	log	logarithmic taper	pc	printed circuit
elect	electrolytic	mA	milliampere(s) = 10 ⁻³ amperes	pF	picofarad(s) 10 ⁻¹² farad
encap	encapsulated	MHz	megahertz = 10 ⁶ hertz	piv	peak inverse voltage
F	farad(s)	MΩ	megohm(s) = 10 ⁶ ohms	p/o	part of
FET	field effect transistor	met film	metal film	pos	position(s)
fix	fixed	mfr	manufacturer	poly	polystyrene
GaAs	gallium arsenide	ms	millisecond	pot	potentiometer
GHz	gigahertz = 10 ⁹ hertz	mg	milligram	pp	peak to peak
gd	guarded	mV	millivolt(s) = 10 ⁻³ volts	ppm	parts per million
Ge	germanium	μF	microfarad(s)	prec	precision (temperature coefficient, long term stability and/or tolerance)
gnd	grounded	μs	microsecond(s)	R	resistor
H	henry(ies)	μV	microvolt(s) = 10 ⁻⁶ volts	Rh	rhodium
Hg	mercury	my	mylar	rms	root mean square
		nA	nanampere(s) = 10 ⁻⁹ amperes	rot	rotary
		NC	normally closed		
		Ne	neon	Se	selenium
		NO	normally open	sect	section(s)
				Si	silicon
DECIMAL MULTIPLIERS					
Prefix	Symbol	Multiplier	Prefix	Symbol	Multiplier
tera	T	10 ¹²	centi	c	10 ⁻²
giga	G	10 ⁹	milli	m	10 ⁻³
mega	M or Meg	10 ⁶	micro	μ	10 ⁻⁶
kilo	K or k	10 ³	nano	n	10 ⁻⁹
hecto	h	10 ²	pico	p	10 ⁻¹²
deka	da	10	deci	d	10 ⁻¹
deci	d	10 ⁻¹	atto	a	10 ⁻¹⁸
DESIGNATORS					
A	assembly	FL	filter	Q	transistor
B	motor	HR	heater	QCR	transistor diode
BT	battery	IC	integrated circuit	R	resistor
C	capacitor	J	jack	RT	thermistor
CR	diode	K	key	S	switch
OL	delay line	L	inductor	T	transformer
DS	lamp	M	meter	TB	terminal board
E	misc electronic part	MP	mechanical part	TC	thermocouple
F	fuse	P	plug	TP	test point
				TS	terminal strip
				U	microcircuit
				V	vacuum tube, neon bulb, photocell, etc.
				W	wire
				X	box(es)
				XDS	lampholder
				XF	lampholder
				Y	crystal
				Z	network

STD 8 3734

Table 6-2. Code List of Manufacturers.

Code No.	Manufacturer	Address
0004A	Arizona Coll Inc.	Nogales, AZ 85621
00213	Sage Electronics Corp.	Rochester, NY 14010
01121	Allen Bradley Co.	Milwaukee, WI 53212
01285	Texas Instruments Inc. Semiconductor Component Division	Dallas, TX 75231
02114	Ferrotech Corp.	Saugerties, NY 12477
02735	RCA Corp. Solid State Division	Sommerville, NJ 08876
03888	Pyrofilm Corp.	Whippany, NJ 07981
04713	Motorola Semiconductor Products	Phoenix, AZ 85008
07263	Fairchild Semiconductor Division	Mountain View, CA 94040
07716	TRW Inc. Burlington Division	Burlington, IA 52601
11502	TRW Inc. Boone Division	Boone, NC 28607
16289	Corning Glass Work Elec. Component Division	Raleigh, NC 27604
18324	Signetics Corp.	Sunnyvale, CA 94086
19701	Mepco/Electra Corp.	Mineral Wells, TX 76067
2K497	Cablewave Systems Inc.	North Haven, CT 06473
24226	Gowanda Electronics Corp.	Gowanda, NY 14070
24546	Corning Glass Works	Bradford, PA 16701
27014	National Semiconductor	San Jose, CA 95051
28480	Hewlett-Packard Co. Corporate HQ	Palo Alto, CA 94304
30983	Mepco/Electra Corp.	San Diego, CA 92121
32997	Bourns Inc. Trimpot Prod. Division	Riverside, CA 92507
34371	Harris Semiconductor Division Harris-Intertype	Melbourne, FL 32901
34649	Intel Corp.	Mountain View, CA 94040
50522	Monsanto Co. Elek. Special Prod.	Cupertino, CA 95014
53021	Sangamo Electric Co.	Springfield, IL 62705
56289	Sprague Electric Co.	North Adams, MA 01247
71400	Bussman Mfg. Division of McGraw-Edison Co.	St. Louis, MO 63017
71785	TRW Elek. Components Cinch Division	Elk Grove Village, IL 60007
72136	Electro Motive Mfg. Co. Inc.	Willimantic, CT 06226
72982	Erle Technological Products Inc.	Erie, PA 16512
73138	Beckman Instruments Inc. Helipot Division	Fullerton, CA 92634
73168	Fenwal Inc.	Ashland, MA 01721
74970	Johnson E. F. Co.	Waseca, MN 56093
75042	TRW Inc. Philadelphia Division	Philadelphia, PA 19108
79727	C-W Industries	Warminster, PA 18974
84411	TRW Capacitor Division	Ogallala, NE 68153
86684	RCA Corp. Electronic Components	Harrison, NJ 07029
91506	Augat Inc.	Attleboro, MA 02703
91637	Dale Electronics Inc.	Columbus, NE 68601
95121	Quality Components Inc.	St. Marys, PA 15857
98291	Seelectro Corp.	Mamaroneck, NY 10544

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2K18	0157-C280	24	RESISTOR 1K 1% .125W F TUBULAR	24546	C4-1/B-YO-1001-F
A2K19	0157-C457		RESISTOR 1K 1% .125W F TUBULAR	24546	C4-1/B-YO-1102-F
A2K21	0157-C431		RESISTOR 3.3K 1% .125W F TUBULAR	24546	C4-1/B-YO-2321-F
A2K22	0157-C431		RESISTOR 2.43K 1% .125W F TUBULAR	24546	C4-1/B-YO-2431-F
A2K23	0157-C280		RESISTOR 1K 1% .125W F TUBULAR	24546	C4-1/B-YO-1001-F
A2K24	0658-3280	1	RESISTOR 11.5K 1% .125W F TUBULAR	16299	C4-1/B-YO-1152-F
A2K25	0157-C430	10	RESISTOR 2.21K 1% .125W F TUBULAR	24546	C4-1/B-YO-2211-F
A2K26	0157-C428	4	RESISTOR 1.62K 1% .125W F TUBULAR	24546	C4-1/B-YO-1621-F
A2K27	0157-C458	6	RESISTOR 75 OHM 1% .125W F TUBULAR	24546	C4-1/B-YO-75R0-F
A2K28	0658-3458	1	RESISTOR 8.66K 1% .125W F TUBULAR	16299	C4-1/B-YO-866R-F
A2K29	0658-3516	2	RESISTOR 6.34K 1% .125W F TUBULAR	16299	C4-1/B-YO-6341-F
A2K31	0658-4434	4	RESISTOR 2.32K 1% .125W F TUBULAR	16299	C4-1/B-YO-2321-F
A2K32	0658-4431		RESISTOR 2.87K 1% .125W F TUBULAR	16299	C4-1/B-YO-2871-F
A2K33	0157-C430		RESISTOR 75 OHM 1% .125W F TUBULAR	24546	C4-1/B-YO-75R0-F
A2K34	0658-4434		RESISTOR 2.32K 1% .125W F TUBULAR	16299	C4-1/B-YO-2321-F
A2K35	0658-4434		RESISTOR 2.87K 1% .125W F TUBULAR	16299	C4-1/B-YO-2871-F
A2K36	0157-C430	2	RESISTOR 75 OHM 1% .125W F TUBULAR	24546	C4-1/B-YO-75R0-F
A2K37	0658-4434		RESISTOR 2.32K 1% .125W F TUBULAR	16299	C4-1/B-YO-2321-F
A2K38	0658-4434		RESISTOR 2.87K 1% .125W F TUBULAR	16299	C4-1/B-YO-2871-F
A2K39	0157-C430		RESISTOR 75 OHM 1% .125W F TUBULAR	24546	C4-1/B-YO-75R0-F
A2K40	0157-C430		RESISTOR 75 OHM 1% .125W F TUBULAR	24546	C4-1/B-YO-75R0-F
A2L1	1158-CC64	1	1% LIN CA3049 AMPLIFIER	86684	CA3049
A2L2	1126-CC62	1	IC MIXER CIRCUIT	28480	1126-0762
A2	03570-66533	4	BOARD ASSY, CRYSTAL FILTER	28480	03570-66533
A3C1	0121-0432	6	CAPACITOR; VAR; TYPN; AIR: 1.7/14.1PF	74970	189-505-105
A3C2	0160-2222	6	CAPACITOR-FRD 12PF 5-5% 300WVDC MICA 0+	28480	0160-9987
A3C3	0160-2222	6	CAPACITOR-FRC 1500PF 5-5% 300WVDC MICA	28480	0160-2222
A3C4	0160-9987	6	FACTORY SELECTED PART	28480	0160-9987
A3C5	0160-9987	6	FACTORY SELECTED PART	28480	0160-9987
A3C6	0140-0184	6	CAPACITOR-FRC 110PF 5-5% 300WVDC MICA	04622	UM15F1110300WVDC
A3C7	0121-0036	7	CAPACITOR; VAR; TYPN; AIR: 5.5-16PF 350V	04615	DV11P1818A
A3C8	0150-0056	8	CAPACITOR-F 0.05UF 5-5% 200VDC CER	28480	0150-0056
A3C9	0150-0042	6	CAPACITOR-F 4.7PF 5-5% 300WVDC T1 D10X	95121	TYPE DC
A3C10	0160-0127	15	CAPACITOR-F 1UF 5-5% 200VDC CER	28480	0160-0127
A3C11	0180-0157	6	CAPACITOR-FRC 2.2UF 5-5% 20VDC TA	56289	1800225X9020A2
A3C12	0180-0157	6	CAPACITOR-FRD 2.2UF 5-5% 20VDC TA	56289	1800225X9020A2
A3CP1	1901-0040	1	DIODE-SWITCHING 2A5 30V 50MA	28480	1901-0040
A3L1	9140-3286	6	INDUCTOR	28480	9107-3286
A3L2	9140-3286	24	COIL; FRI; MOLDED PF CHOKE; 1MH 5% 24226	24226	17/104
A3L3	9140-3286		COIL; FRI; MOLDED PF CHOKE; 1MH 5% 24226	24226	17/104
A3Q1	1854-0371	6	TRANSISTOR NPN 51 PD=300MW PF=200MHZ	28480	1854-0371
A3Q2	1853-0086		TRANSISTOR J-FET N-CHAN, D-MODE 51	01295	2N5245
A3Q3	1853-0086		TRANSISTOR PNP 51 CHIP PG-31JH	28480	1853-0086
A2K1	0157-C463	6	RESISTOR 82.5K 1% .125W F TUBULAR	24546	C4-1/B-YO-8252-F
A2K2	0157-C407	12	RESISTOR 200 OHM 1% .125W F TUBULAR	24546	C4-1/B-YO-201-F
A2K3	0658-4472		RESISTOR 7.68K 1% .125W F TUBULAR	24546	C4-1/B-YO-7681-F
A2K4	0157-C407		RESISTOR 2K 1% .125W F TUBULAR	24546	C4-1/B-YO-2001-F
A2K5	0658-4472	23	RESISTOR 7.68K 1% .125W F TUBULAR	24546	C4-1/B-YO-7681-F
A2K6	0157-C427	8	RESISTOR 1.5K 1% .125W F TUBULAR	24546	C4-1/B-YO-1501-F
A2K7	0658-4123	16	RESISTOR 495 OHM 1% .125W F TUBULAR	16299	C4-1/B-YO-495R-F
A2K8	0658-4640	7	RESISTOR 3.4K 1% .125W F TUBULAR	16299	C4-1/B-YO-3401-F
A2K9	0658-3486	8	RESISTOR 232 OHM 1% .125W F TUBULAR	16299	C4-1/B-YO-232R-F
A2K11	0157-C430	6	RESISTOR 22.1K 1% .125W F TUBULAR	24546	C4-1/B-YO-2212-F
A2K12	0658-4123	1	RESISTOR 495 OHM 1% .125W F TUBULAR	16299	C4-1/B-YO-495R-F
A2K13	0658-4060	6	TRANSISTOR, NEG TC, 500 OHM DISC	73168	8825J1
A2T1	9100-3262	10	TRANSFORMER	28480	9100-3262
A4	03570-66533	1	BOARD ASSY, CRYSTAL FILTER	28480	03570-66533
A5	03570-66533	2	BOARD ASSY, ACJ FILTER	28480	03570-66533
A5C1	0121-0432	6	CAPACITOR; VAR; TYPN; AIR: 1.7/14.1PF	74970	189-505-105
A5C2	0160-2222		CAPACITOR-FRD 12PF 5-5% 300WVDC MICA 0+	28480	0160-9987
A5C3	0160-2222		CAPACITOR-FRC 1500PF 5-5% 300WVDC MICA	28480	0160-2222
A5C4	0160-9987		FACTORY SELECTED PART	28480	0160-9987

See Introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
ABC5	0140-0104		CAPACITOR-FXC 110PF +-5% 100VDC MICA	04522	DM15F1110300WVICH
ABC6	0121-0030		CAPACITOR VARI TAPR1 A1M1 65-18PF 350V	04616	DV11P1R1E1A
ABC7	0150-CC46		CAPACITOR-FXD .05UF +-20% 250VDC CER	24480	0150-CC46
ABC8	0150-CC42		CAPACITOR-FXC 4.7PF +-5% 500VDC T1 D10X	95121	TYPE OC
ABC9	0140-0127		CAPACITOR-FXD 1UF +-20% 250VDC CER	24480	0140-0127
ABC10	0140-0127		CAPACITOR-FXC 1UF +-20% 250VDC CER	24480	0140-0127
ABC11	0180-0157		CAPACITOR-FXD: 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
ABC12	0180-0157		CAPACITOR-FXC: 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
ABC13	0150-CC46		CAPACITOR-FXD .05UF +-20% 250VDC CER	24480	0150-CC46
ABC14	0140-0174	10	CAPACITOR-FXD .47UF +-20% 250VDC CER	24480	0140-0174
ACF1	1501-CC4C		DIODE-SWITCHING 2A5 30V 50MA	24480	1501-CC4C
ASL1	9140-3246		INDUCTOR	24480	9140-3246
ASL2	9140-0137		COIL: FWD: POLDED PF CHOKER 1MH 5R	24226	15/104
ASL3	9140-0137		COIL: FWD: POLDED PF CHOKER 1MH 5R	24226	15/104
ASG1	1854-0071		TRANSISTOR NPN 51 PD=300MW FT=200MHZ	24480	1854-0071
ASG2	1851-0021		TRANSISTOR: J-FET N-CHAN, D-MOSFET 51	01295	2N5245
ASG3	1851-0021		TRANSISTOR PNP 51 CHIP PD=310MW	24480	1851-0021
ASG4	1854-0071		TRANSISTOR NPN 51 PD=300MW FT=200MHZ	24480	1854-0071
ASR1	0757-C243		RESISTOR 22.5K 1% .125W F TUBULAR	24546	C4-1/B-T0-B.152-F
ASR2	0757-C247		RESISTOR 200 OHM 1% .125W F TUBULAR	24546	C4-1/B-T0-2U1-F
ASR3	0658-4472		RESISTOR 7.68K 1% .125W F TUBULAR	24546	C4-1/B-T0-T481-F
ASR4	0757-C243		RESISTOR 2K 1% .125W F TUBULAR	24546	C4-1/B-T0-2001-F
ASR5	0658-4472		RESISTOR 7.68K 1% .125W F TUBULAR	24546	C4-1/B-T0-T481-F
ASR6	0757-1.27		RESISTOR 1.5K 1% .125W F TUBULAR	24546	C4-1/B-T0-1501-F
ASR7	0658-4123		RESISTOR 495 OHM 1% .125W F TUBULAR	16299	C4-1/B-T0-495R-F
ASR8	2458-4440		RESISTOR 3.4K 1% .125W F TUBULAR	16299	C4-1/B-T0-T481-F
ASR9	0658-3486		RESISTOR 232 OHM 1% .125W F TUBULAR	16299	C4-1/B-T0-232R-F
ASR10	0837-CC40		THERMISTOR, NEG TC, 500 OHM DISC	73108	RN25J1
ASR11	0757-C450		RESISTOR 22.1K 1% .125W F TUBULAR	24546	C4-1/B-T0-2212-F
ASR12	0658-4123		RESISTOR 495 OHM 1% .125W F TUBULAR	16299	C4-1/B-T0-495R-F
ASR13	0757-C422		RESISTOR 909 OHM 1% .125W F TUBULAR	24546	C4-1/B-T0-T09R-F
ASR14	2100-3C54	2	RESISTOR-VAR TRIM 500OHM 10% C SIDE ADJ	37997	300AP-1-503
ASR15	2100-3103	2	RESISTOR-VAR TRIM 10KOHM 10% C SIDE ADJ	32497	300AP-1-103
ASR16	0757-C243		RESISTOR 2K 1% .125W F TUBULAR	24546	C4-1/B-T0-2001-F
ATF1	9100-3242		TRANSFORMER	24480	9100-3242
AB	03570-64534	2	BOARD ASSY, B4 LCGIC	24480	03570-64534
ACC1	0150-CC46	48	CAPACITOR-FXC .1UF +-20% 250VDC CER	24480	0150-CC46
ACC2	0180-3548		CAPACITOR-FXC .01UF +-1% 100VDC MICA	24480	0180-3548
ACC3	0140-0127		CAPACITOR-FXD 1UF +-20% 250VDC CER	24480	0140-0127
ACC4	0150-CC46		CAPACITOR-FXC .1UF +-20% 250VDC CER	24480	0150-CC46
ACC5	0180-0157		CAPACITOR-FXC: 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
ACC6	0180-0157		CAPACITOR-FXC: 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
ACC7	0150-CC46		CAPACITOR-FXD .05UF +-20% 250VDC CER	24480	0150-CC46
ACC8	0180-0157		CAPACITOR-FXD: 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
ACC9	0150-CC46		CAPACITOR-FXD .05UF +-20% 250VDC CER	24480	0150-CC46
ACC10	0150-CC46		CAPACITOR-FXD .05UF +-20% 250VDC CER	24480	0150-CC46
ACC11	0180-0157		CAPACITOR-FXD: 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
ACC12	0150-CC46		CAPACITOR-FXC .05UF +-20% 250VDC CER	24480	0150-CC46
ACF1	1501-CC4C		DIODE-SWITCHING 2A5 30V 50MA	24480	1501-CC4C
ACF2	1501-CC4C		DIODE-SWITCHING 2A5 30V 50MA	24480	1501-CC4C

See Introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7C16	15C1-314V	2	DIODE-1N4 9.05V 5% 00-7 PD=4M	04713	52 10939-170
A7C17	15C1-051B	4	DIODE-SCHOTTKY	28480	1901-051B
A7C18	15C1-051B		DIODE-SCHOTTKY	28480	1901-051B
A7L1	9140-C210	8	COIL FRC POLDED RF CHOKE 100UH 5% 24226	15/103	
A7L2	9140-C210		COIL FRC POLDED RF CHOKE 100UH 5% 24226	15/103	
A7L3 A7	9100-0665	2	COIL FRC POLDED RF CHOKE 500UH 10% 28480	0100-0665	
A7Q1	1854-CC31		TRANSISTOR APH 51 PD=300MH FT=200MHZ 28480	1854-0071	
A7Q2	1854-CC31		TRANSISTOR APH 51 PD=300MH FT=200MHZ 28480	1854-0071	
A7Q3	1853-C086		TRANSISTOR APH 51 CMIP PD=310MH 28480	1853-0086	
A7Q4	1854-0071		TRANSISTOR APH 51 PD=300MH FT=200MHZ 28480	1854-0071	
A7Q5	1854-CC31		TRANSISTOR APH 51 PD=300MH FT=200MHZ 28480	1854-0071	
A7Q6	1854-CC31		TRANSISTOR APH 51 PD=300MH FT=200MHZ 28480	1854-0071	
A7R1	049E-4435	10	RESISTOR 2.49K 1% .125W F TUBULAR 16299	CA-1/R-TO-2491-F	
A7R2 A7	0608-4485	3	RESISTOR 23.7K 1% .125W F TUBULAR 16299	CA-1/R-TO-2372-F	
A7R3 A7	049E-4435		RESISTOR 2.49K 1% .125W F TUBULAR 16299	CA-1/R-TO-2491-F	
A7R4 A7	0608-4485	4	RESISTOR 23.7K 1% .125W F TUBULAR 16299	CA-1/R-TO-2372-F	
A7R5	049E-4435		RESISTOR 2.49K 1% .125W F TUBULAR 16299	CA-1/R-TO-2491-F	
A7R6 A7	0608-4485		RESISTOR 23.7K 1% .125W F TUBULAR 16299	CA-1/R-TO-2372-F	
A7R7	049E-4435		RESISTOR 2.49K 1% .125W F TUBULAR 16299	CA-1/R-TO-2491-F	
A7R8 A7	0608-2769	5	RESISTOR 7.87K 1% .125W F TUBULAR 16299	CA-1/R-TO-7871-F	
A7R9	049E-4435	3	RESISTOR 1.10K 1% .125W F TUBULAR 24546	CA-1/R-TO-1101-F	
A7R10	049E-4435	19	RESISTOR 1.10K 1% .125W F TUBULAR 24546	CA-1/R-TO-1101-F	
A7R11	049E-4435		RESISTOR 1.10K 1% .125W F TUBULAR 24546	CA-1/R-TO-1101-F	
A7R12	049E-4435		RESISTOR 1.10K 1% .125W F TUBULAR 24546	CA-1/R-TO-1101-F	
A7R13	210C-3141	2	RESISTOR-VAR 100K 200MH 10% C SIDE ADJ 32997	3008P-1-20	
A7R14	0757-C354	11	RESISTOR 51.1 OHM 1% .125W F TUBULAR 24546	CA-1/R-TO-51R1-F	
A7R15	049E-4435	4	RESISTOR 17.0K 1% .125W F TUBULAR 16299	CA-1/R-TO-1702-F	
A7R16 A7	0757-0427	2	RESISTOR 150K 1% .125W F TUBULAR 24546	CA-1/R-TO-1501-F	
A7R17 A7	0757-0427	2	RESISTOR 200K .25W CC TUBULAR 24546	CA-1/R-TO-2003-F	
A7R18	0757-C354		RESISTOR 51.1 OHM 1% .125W F TUBULAR 24546	CA-1/R-TO-51R1-F	
A7R19	049E-4435	2	RESISTOR 23.7K 1% .125W F TUBULAR 24546	CA-1/R-TO-2372-F	
A7R20 A7	0608-3279		RESISTOR 400K 1% .125W F TUBULAR 16299	CA-1/R-TO-4001-F	
A7R21	049E-4435	2	RESISTOR 2K 1% .125W F TUBULAR 19701	MFAC1/R-T9-2001-F	
A7R22	049E-4435	2	RESISTOR 20K 1% .125W F TUBULAR 19701	MFAC1/R-T9-2002-F	
A7R23	210C-3141	2	RESISTOR-VAR 100K 200MH 10% C SIDE ADJ 73138	89PKK	
A7R24	049E-4435	8	RESISTOR 100K 1% .125W F TUBULAR 19701	MFAC1/R-T9-1003-F	
A7R25	049E-4435		RESISTOR 100K 1% .125W F TUBULAR 19701	MFAC1/R-T9-1003-F	
A7R26	049E-4435		RESISTOR 100K 1% .125W F TUBULAR 19701	MFAC1/R-T9-1003-F	
A7R27	049E-4435		RESISTOR 100K 1% .125W F TUBULAR 19701	MFAC1/R-T9-1003-F	
A7R28	049E-4435		RESISTOR 2.49K 1% .125W F TUBULAR 16299	CA-1/R-TO-2491-F	
A7R29	0757-0281	2	RESISTOR 2.74K 1% .125W F TUBULAR 24546	CA-1/R-TO-2741-F	
A7R30	0757-0465	5	RESISTOR 100K 1% .125W F TUBULAR 24546	CA-1/R-TO-1003-F	
A7R31	0757-0465		RESISTOR 100K 1% .125W F TUBULAR 24546	CA-1/R-TO-1003-F	
A7R32	0757-0354		RESISTOR 51.1 OHM 1% .125W F TUBULAR 24546	CA-1/R-TO-51R1-F	
A7R33	049E-4435		RESISTOR 17.0K 1% .125W F TUBULAR 16299	CA-1/R-TO-1702-F	
A7R34 A7	0757-0427		RESISTOR 150K 1% .125W F TUBULAR 24546	CA-1/R-TO-1501-F	
A7R35 A7	0608-4485		RESISTOR 150K 1% .125W F TUBULAR 24546	CA-1/R-TO-1501-F	
A7R36-R50 A7	210C-2216		RESISTOR-VAR 5K 1% 81048	170-502	
A7T1, T2	9100-3782		TRANSFORMER 28480	0100-3782	
A7U1	1826-0043	8	IC LIM AMPLIFIER 34371	HA2-2425-80593	
A7U2	1826-0043		IC LIM AMPLIFIER 34371	HA2-2425-80593	
A7U3	1826-0043		IC LIM AMPLIFIER 34371	HA2-2425-80593	
A7U4	1826-0043		IC LIM AMPLIFIER 34371	HA2-2425-80593	
A7U5	1813-0017	2	IC LIM AMPLIFIER 28480	1813-0017	
A7U6	1826-0043	14	IC LIM LP307M AMPLIFIER 27014	LM307M	
A7U7	1826-0043		IC LIM LP307M AMPLIFIER 27014	LM307M	
AE	03570-24536	1	NCARC ASSY, POWER SPLITTER 28480	03570-24536	
AEC1	0150-0127		CAPACITOR-FXD .01UF +20% 250VDC CER 28480	0150-0127	
AEC2	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEC3	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEC4	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEC5	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEC6	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEC7	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEC8	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEC9, C11	0150-0084	4	CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0084	
AEL12	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEL13	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEL14	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEL15	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	
AEL16	0150-0093		CAPACITOR-FXD .01UF +20% 100VDC CER 28480	0150-0093	

See Introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A10C11	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
A10C12	0180-0084		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
A10C13	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
A10L1	9140-CC54	4	COIL FND POLCED RF CHOKER 100H 10R	24226	15/101
A10L2	9100-1214	4	CCIL FND POLCED RF CHOKER 100H 10R	24226	15/820
A10L3	9140-0114	6	COIL FND POLCED RF CHOKER 100H 10R	24226	15/102
A10L4	9170-CC54		CCREI PAG SHIELDING BEACI .125 OD .047	02114	86-590-85/444
A10Q1	1254-C345		TRANSISTOR NPN 2N5179 SI PD=200MH	04713	2N5179
A10Q2	1254-0345		TRANSISTOR NPN 2N5179 SI PD=200MH	04713	2N5179
A10Q3	1254-C345		TRANSISTOR NPN 2N5179 SI PD=200MH	04713	2N5179
A10R1	0757-C41J	7	RESISTOR 301 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-301R-F
A10R2	0757-C244	1	RESISTOR 17.8 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-178R-F
A10R3	0458-4387	4	RESISTOR 40.4 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-404R-F
A10R4	0458-4625	3	RESISTOR 1.43K 1% .125W F TUBULAR	24546	CA-1/4-TO-1431-F
A10R5	0757-C344	4	RESISTOR 10 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-10R-F
A10R6	0757-C401		RESISTOR 100 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-101-F
A10R7	0458-4387		RESISTOR 40.4 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-404R-F
A10R8	0458-4625		RESISTOR 1.43K 1% .125W F TUBULAR	24546	CA-1/4-TO-1431-F
A10R9	0458-4625		RESISTOR 1.43K 1% .125W F TUBULAR	24546	CA-1/4-TO-1431-F
A10R10	0458-4387		RESISTOR 40.4 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-404R-F
A10R11	0757-C401		RESISTOR 100 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-101-F
A10R12	0458-4387	1	RESISTOR 1.43K 1% .125W F TUBULAR	16299	CA-1/8-TO-1431-F
A10R13	0458-4387	2	RESISTOR 40.4 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-404R-F
A10R14	0458-4387	1	RESISTOR 26.7 OHM 1% .125W F TUBULAR	03808	MF55-1/8-TO-267-F
A10R15	0458-4387		RESISTOR 442 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-442R-F
A10R16	0458-4387		RESISTOR 442 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-442R-F
A10R18	0458-4387	1	RESISTOR 442 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-442R-F
A10R17	0458-4387	1	RESISTOR 1K 1% .125W F TUBULAR	24546	CA-1/8-TO-1001-F
A10T1	9100-1361	5	TRANSFORMER-TOROID	28480	9100-1361
A10T2	9100-1361		TRANSFORMER-TOROID	28480	9100-1361
A10T3	9100-1361		TRANSFORMER-TOROID	28480	9100-1361
A10T4	9100-1361		TRANSFORMER-TOROID	28480	9100-1361
A10U1	1501-1011	2	CIRCUIT MULTI-DIODE ARRAY	28480	1501-1011
A	03570-44537	1	PC ASSY, INPUT BUFFER	28480	03570-44537
A C1	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
A C2	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
A C3	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
A L1	9170-CC54		COIL FND POLCED RF CHOKER 100H 10R	02114	86-590-85/444
A L2	9170-CC54		COIL FND POLCED RF CHOKER 100H 10R	02114	86-590-85/444
A R1	1254-C345	4	RESISTIVE NETWORK	28480	1254-C345
A R2	1254-C345		RESISTIVE NETWORK	28480	1254-C345
A L1	1820-C174	16	IC DCTL 5474 04 N INVERTER	01295	547404N
A L2	1820-C174		IC DCTL 5474 04 N INVERTER	01295	547404N
A L3	1820-C174		IC DCTL 5474 13 N SCHMITT TRIGGER	01295	547413N
A L4	1820-C174		IC DCTL 5474 13 N SCHMITT TRIGGER	01295	547413N
A L5	1820-C174		IC DCTL 5474 13 N SCHMITT TRIGGER	01295	547413N
A0	03570-44537	1	PC ASSY, APPLICATOR	28480	03570-44537
ABC1	0180-CC64	1	CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC2	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC3	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC4	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC5	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC6	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC7	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC8	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC9	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC10	0180-CC64	2	CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC11	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABC12	0180-CC64		CAPACITOR-FXC .1UF +80-20V 100VDC CER	28480	0180-0084
ABL1	9140-CC54		COIL FND POLCED RF CHOKER 100H 10R	24226	15/101
ABL2	9100-1214		CCIL FND POLCED RF CHOKER 100H 10R	24226	15/820
ABL3	9140-0114		COIL FND POLCED RF CHOKER 100H 10R	24226	15/102
ABQ1	1254-C345		TRANSISTOR NPN 2N5179 SI PD=200MH	04713	2N5179
ABQ2	1254-C345		TRANSISTOR NPN 2N5179 SI PD=200MH	04713	2N5179
ABR1	0757-C41J		RESISTOR 301 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-301R-F
ABR2	0757-C244		RESISTOR 17.8 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-178R-F
ABR3	0458-4387		RESISTOR 40.4 OHM 1% .125W F TUBULAR	16299	CA-1/8-TO-404R-F
ABR4	0458-4625		RESISTOR 1.43K 1% .125W F TUBULAR	24546	CA-1/4-TO-1431-F
ABR5	0757-C344	2	RESISTOR 10 OHM 1% .125W F TUBULAR	24546	CA-1/8-TO-10R-F

See Introduction to this section for ordering information

Table 6-3, Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
ADR6 ADR7 ADR8 ADR9 ADR10	0757-C385 0451-4434 0658-4387 0658-7810 0757-C251	1 2	RESISTOR 33.2 OHM 1% .125W F TUBULAR RESISTOR 2.2K 1% .125W F TUBULAR RESISTOR 60.4 KHM 1% .125W F TUBULAR RESISTOR 2.03K 1% .25W F TUBULAR RESISTOR 24.9 OHM 1% .125W F TUBULAR	24544 16299 16299 30943 30943	CA-1/B-TO-53R2-F CA-1/B-TO-2321-F CA-1/B-TO-60KA-F MF52C1/4-TO-2051-F MF4C1/B-TO-2492-F
ADR11 ADR12	0757-C291 0757-C454		RESISTOR 24.9 OHM 1% .125W F TUBULAR RESISTOR 130 OHM 1% .125W F TUBULAR	30943 24544	MF4C1/B-TO-2492-F CA-1/B-TO-131-F
ALL	03570-44519	1	BOARD ASSY, YCAG	28480	03570-44519
ALLC1 ALLC2 ALLC3 ALLC4 ALLC5	0140-C170 0140-C174 0140-C183 0140-C157 0140-C053	4 1	CAPACITOR-PXC .22UF +80-20V 250VDC CER CAPACITOR-PXC .47UF +80-20V 250VDC CER CAPACITOR-PXC .47UF +80-20V 500VDC MET CAPACITOR-PXC .22UF +80-20V 20VDC TA CAPACITOR-PXD .01UF +80-20V 100VDC CER	28480 28480 28480 28480 28480	0140-C170 0140-C174 HEW-101 150D25K9020A2 0150-0093
ALLC6 ALLC7 ALLC8 ALLC9 ALLC10	0150-C053 0150-C053 0150-C053 0150-C053 0150-C053		CAPACITOR-PXC .01UF +80-20V 100VDC CER CAPACITOR-PXD .01UF +80-20V 100VDC CER CAPACITOR-PXC .01UF +80-20V 100VDC CER CAPACITOR-PXD .01UF +80-20V 100VDC CER CAPACITOR-PXD .01UF +80-20V 100VDC CER	28480 28480 28480 28480 28480	0150-0093 0150-0093 0150-0093 0150-0093 0150-0093
ALLC11 ALLC12 ALLC13 ALLC14 ALLC15	0140-C144 0140-C159 1140-0378 0140-2206 0140-0378	1 1	CAPACITOR-PXC .22UF +80-20V 100VDC MICA CAPACITOR-PXC .22UF +80-20V 100VDC MICA CAPACITOR-PXC .22UF +80-20V 100VDC MICA CAPACITOR-PXC .22UF +80-20V 100VDC MICA CAPACITOR-PXC .22UF +80-20V 100VDC MICA	24226 24226 24226 24226 24226	DM15E20J0300HV1CR DM15E24J0300HV1CR 0140-0378 0140-2206 0140-0378
ALLC16	0150-C053		CAPACITOR-PXD .01UF +80-20V 100VDC CER	28480	0150-0093
ALLCP1 ALLCP2 ALLCP3 ALLCP4 ALLCP5	1501-0025 1501-0025 1501-0025 1501-0025 0122-0059	4 1	LIODE-GEN PNP 100V 200MA LIODE-GEN PNP 100V 200MA LIODE-GEN PNP 100V 200MA LIODE-GEN PNP 100V 200MA LIODE-VOLTAGE VARIABLE CAPACITANCE	28480 28480 28480 28480 28480	1501-0025 1501-0025 1501-0025 1501-0025 0122-0059
ALLL1 ALLL2 ALLL3 ALLL4 ALLL5	9140-0179 9140-0179 9100-1614 9140-0056 9140-0160	2	COILS PND POLCED PF CHOKES 22UH 10% COILS PND POLCED PF CHOKES 22UH 10% COILS PND POLCED PF CHOKES 22UH 10% COILS PND POLCED PF CHOKES 22UH 10% COILS PND POLCED PF CHOKES 22UH 10%	24226 24226 24226 24226 24226	15/222 15/222 15/222 15/222 15/222
ALLL6 ALLL7	9140-0160 9140-0160		COILS PND POLCED PF CHOKES 22UH 10% COILS PND POLCED PF CHOKES 22UH 10%	24226 24226	15/222 15/222
ALLC1 ALLC2	1453-0086 1453-0086		TRANSISTOR PNP 51 CHIP PD-310MB TRANSISTOR J-FET N-CHAN, D-MODE 51	28480 01245	1453-0086 24226
ALLP1 ALLP2 ALLP3 ALLP4 ALLP5	0658-4419 0757-C442 0757-C447 0658-1081 0658-1081	1 25 2	RESISTOR 100K 1% .125W F TUBULAR RESISTOR 10K 1% .125W F TUBULAR RESISTOR 10K 1% .125W F TUBULAR RESISTOR 1M 1% .25W CC TUBULAR RESISTOR 1M 1% .25W CC TUBULAR	24544 24544 24544 01121 01121	CA-1/B-TU-1403-F CA-1/B-TU-1002-F CA-1/B-TU-1002-F CR1051 CR1051
ALLP6 ALLP7 ALLP8 ALLP9 ALLP10	0757-C437 0658-2275 0658-4445 0757-C457 0757-C354	1 1	RESISTOR 4.75K 1% .125W F TUBULAR RESISTOR 4.75K 1% .125W F TUBULAR RESISTOR 5.74K 1% .125W F TUBULAR RESISTOR 200 OHM 1% .125W F TUBULAR RESISTOR 51.1 OHM 1% .125W F TUBULAR	24544 16299 16299 24544 24544	CA-1/B-TU-4751-F CA-1/B-TU-4751-F CA-1/B-TU-5741-F CA-1/B-TU-201-F CA-1/B-TU-5111-F
ALLP11 ALLP12 ALLP13 ALLP14 ALLP15	0658-2279 0757-C442 0757-C419 0757-C410 0757-C394	1 2	RESISTOR 4.75K 1% .125W F TUBULAR RESISTOR 10K 1% .125W F TUBULAR RESISTOR 681 OHM 1% .125W F TUBULAR RESISTOR 301 OHM 1% .125W F TUBULAR RESISTOR 51.1 OHM 1% .125W F TUBULAR	16299 24544 24544 24544 24544	CA-1/B-TU-4751-F CA-1/B-TU-1002-F CA-1/B-TU-681R-F CA-1/B-TU-301R-F CA-1/B-TU-5111-F
ALLP16 ALLP17 ALLP18 ALLP19 ALLP20	0757-C410 0658-2279 0658-2275 0757-C415 0757-C410		RESISTOR 301 OHM 1% .125W F TUBULAR RESISTOR 4.75K 1% .125W F TUBULAR RESISTOR 4.75K 1% .125W F TUBULAR RESISTOR 681 OHM 1% .125W F TUBULAR RESISTOR 301 OHM 1% .125W F TUBULAR	24544 16299 16299 24544 24544	CA-1/B-TU-301R-F CA-1/B-TU-4751-F CA-1/B-TU-4751-F CA-1/B-TU-681R-F CA-1/B-TU-301R-F
ALLP21 ALLP22 ALLP23 ALLP24 ALLP25	0757-0154 0757-C276 0658-4377 0757-C264 0658-4379	1 3 1 1	RESISTOR 51.1 OHM 1% .125W F TUBULAR RESISTOR 61.9 OHM 1% .125W F TUBULAR RESISTOR 37.4 OHM 1% .125W F TUBULAR RESISTOR 150 OHM 1% .125W F TUBULAR RESISTOR 44.2 OHM 1% .125W F TUBULAR	24544 24544 16299 24544 16299	CA-1/B-TU-5111-F CA-1/B-TU-6192-F CA-1/B-TU-374-F CA-1/B-TU-151-F CA-1/B-TU-442-F
ALLP26 ALLP27	0757-C464 0757-C464		RESISTOR 130 OHM 1% .125W F TUBULAR RESISTOR 130 OHM 1% .125W F TUBULAR	24544 24544	CA-1/B-TU-131-F CA-1/B-TU-131-F
ALLL1	1458-C019	3	IC OGTL AMPLIFIER	02735	
ALLP1	0410-C471	1	CRYSTAL/QUARTZ	28480	0410-C471
ALL	03570-44540	1	BOARD ASSY, SAMPLE	28480	03570-44540

See Introduction to this section for ordering information

Table 6-3, Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A12C1	0150-C099	1	CAPACITOR-FXD .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C2	0140-C205		CAPACITOR-FXC 10PF +-5% 300WVDC MICA O+	28480	0140-C205
A12C3	0150-C099		CAPACITOR-FXD .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C4	0150-C099		CAPACITOR-FXC .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C5	0150-C099		CAPACITOR-FXC .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C6	0150-C099	1	CAPACITOR-FXD .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C7	0150-C099		CAPACITOR-FXD .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C8	0140-C205		CAPACITOR-FXD 10PF +-5% 300WVDC MICA	72134	0M15F20F0300WV1CR
A12C9	0150-C099		CAPACITOR-FXD .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C10	0150-C099		CAPACITOR-FXD .01UF +80-20V 100WVDC CER	28480	0150-C099
A12C11	0140-C174	1	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	72134	0M15F101G0300WV1CR
A12C12	0150-C197		CAPACITOR-FXC 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
A12C13	0150-C197		CAPACITOR-FXC 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
A12C14	0150-C197		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
A12CR1	1901-0040	1	DIODE-SWITCHING 2HS 30V 50MA	28480	1901-0040
A12CR2	1901-0040		DIODE-SWITCHING 2HS 30V 50MA	28480	1901-0040
A12CR3	1901-0040		DIODE-SWITCHING 2HS 30V 50MA	28480	1901-0040
A12CR4	1901-0040		DIODE-SWITCHING 2HS 30V 50MA	28480	1901-0040
A12L1	9140-0114	1	COIL; FWD; MCLDED PF CHOKER; 82UH 10V	24224	15/820
A12L2	9140-0114		COIL; FWD; MCLDED PF CHOKER; 10UH 10V	24224	15/102
A12L3	9140-0114		COIL; FWD; MCLDED PF CHOKER; 1UH 10V	24224	15/101
A12L4	9140-0114		COIL; FWD; MCLDED PF CHOKER; 400UH 10V	0004A	5-400J-1
A12L5	9140-0114		COIL; FWD; MCLDED PF CHOKER; 400UH 10V	0004A	5-400J-1
A12L6	9100-1447	1	COIL; FWD; MCLDED PF CHOKER; 470UH 5V	24224	14/473
A12C1	1854-CC71		TRANSISTOR NPN 51 PD=300MW FT=200MHZ	28480	1854-0071
A12C2	1854-CC71		TRANSISTOR NPN 51 PD=300MW FT=200MHZ	28480	1854-0071
A12C3	1853-0203		TRANSISTOR PNP 51 CH/P TO-18 D=36CMW	28480	1853-0203
A12C4	1854-CC71		TRANSISTOR NPN 51 TO-18 PD=300MW	28480	1854-0071
A12C5	1854-CC71		TRANSISTOR NPN 51 PD=300MW FT=200MHZ	28480	1854-0071
A12R1	0757-C294	11	RESISTOR 51.1 OHM 1% .125W F TUBULAR	24546	C4-1/B-TO-3181-F
A12R2	0498-4440		RESISTOR 3.4K 1% .125W F TUBULAR	16299	C4-1/B-TO-3401-F
A12R3	0757-C280		RESISTOR 2K 1% .125W F TUBULAR	24546	C4-1/B-TO-2001-F
A12R4	0757-C410		RESISTOR 201 OHM 1% .125W F TUBULAR	24546	C4-1/B-TO-3018-F
A12R5	0757-C283		RESISTOR 2K 1% .125W F TUBULAR	24546	C4-1/B-TO-2001-F
A12R6	0757-C442	11	RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12R7	0757-C346		RESISTOR 10 OHM 1% .125W F TUBULAR	24546	C4-1/B-TO-1000-F
A12R8	0757-C446		RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12R9	0757-C446		RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12R10	0757-C442		RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12R11	0757-C442	2	RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12R12	0757-C280		RESISTOR 1K 1% .125W F TUBULAR	24546	C4-1/B-TO-1001-F
A12R13	0757-C280		RESISTOR 1K 1% .125W F TUBULAR	24546	C4-1/B-TO-1001-F
A12R14	0498-4377		RESISTOR 37.4 OHM 1% .125W F TUBULAR	16299	C4-1/B-TO-374-F
A12R15	0498-4377		RESISTOR 37.4 OHM 1% .125W F TUBULAR	16299	C4-1/B-TO-374-F
A12R16	0757-C442	2	RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12R17	0757-C418		RESISTOR 5.11K 1% .125W F TUBULAR	24546	C4-1/B-TO-5111-F
A12R18	0757-C442		RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12R19	0757-C426		RESISTOR 5.11K 1% .125W F TUBULAR	24546	C4-1/B-TO-5111-F
A12R20	0757-C442		RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/B-TO-1002-F
A12T1	9100-1321	1	TRANSFORMER-TOROID	28480	9100-1321
A12U1	1820-0370		IC DCTL 5N74N 00 N GATE	01295	5N74N00N
A12U2	1820-0095		IC DCTL 5N74N 90 N COUNTER	01295	5N74N0N
A12U3	1901-1011		DIODE; MULTI; DIODE ARRAY	28480	1901-1011
A12U4	1824-CC43	1	IC LIN LP307M AMPLIFIER	28480	LP307M
A13	03570-66541	1	BOARD ASSY, PHASE LIMITER	28480	03570-66541
A13C1	0140-0220	1	CAPACITOR-FXC 200PF +-5% 300WVDC MICA	72134	0M15F20F0300WV1CR
A13C2	0140-C174		CAPACITOR-FXC 1000PF +-5% 300WVDC MICA	72134	0M15F10F0300WV1CR
A13C3	0140-C174		CAPACITOR-FXD .47UF +80-20V 25WVDC CER	28480	0140-C174
A13C4	0140-C174		CAPACITOR-FXD .47UF +80-20V 25WVDC CER	28480	0140-C174
A13C5	0140-C174		CAPACITOR-FXD .47UF +80-20V 25WVDC CER	28480	0140-C174
A13C6	0140-C164	4	CAPACITOR-FXD .033UF +-10% 200WVDC POLYE	56289	292P33932
A13C7	0150-0084		CAPACITOR-FXC .1UF +80-20V 100WVDC CER	28480	0150-0084
A13C8	0150-C197		CAPACITOR-FXC 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
A13C9	0150-0164		CAPACITOR-FXC .033UF +-10% 200WVDC POLYE	56289	292P33932
A13C11	0140-C174		CAPACITOR-FXD .47UF +80-20V 25WVDC CER	28480	0140-C174
A13C12	0140-C174	1	CAPACITOR-FXD .47UF +80-20V 25WVDC CER	28480	0140-C174
A13C13	0140-0164		CAPACITOR-FXC .033UF +-10% 200WVDC POLYE	56289	292P33932
A13C14	0150-0084		CAPACITOR-FXC .1UF +80-20V 100WVDC CER	28480	0150-0084
A13C15	0150-C197		CAPACITOR-FXC 2.2UF+-10% 20VDC TA	56289	1500225X9020A2
A13C16	0140-0164		CAPACITOR-FXD .033UF +-10% 200WVDC POLYE	56289	292P33932
A13C17	0150-C160	6	CAPACITOR-FXD .47UF+-10% 35VDC TA	56289	1500475X9035B2
A13C18	0150-0160		CAPACITOR-FXC .47UF+-10% 35VDC TA	56289	1500475X9035B2
A13C19	0150-0160		CAPACITOR-FXC .47UF+-10% 35VDC TA	56289	1500475X9035B2
A13C20	0150-0160		CAPACITOR-FXD .47UF+-10% 35VDC TA	56289	1500475X9035B2

See Introduction to this section for ordering information

Table 6-3, Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A14C1	1854-CC71	4	TRANSISTOR NPN 51 PD=100MW FT=20CMHZ	28480	1854-0071
A14C2	1853-0203		TRANSISTOR PNP 51 CHIP TC-18 PD=100MW	28480	1853-0203
A14C3	1853-0018		TRANSISTOR PNP 51 FIP TC-72 PD=200MW	28480	1853-0018
A14C4	1853-C1C3		TRANSISTOR PNP 51 CHIP TC-18 PD=100MW	28480	1853-0203
A14C5	1853-0018		TRANSISTOR PNP 51 CHIP TC-72 PD=200MW	28480	1853-0018
A14Q7	1853-C203	4	TRANSISTOR PNP 51 CHIP TC-18 PD=100MW	28480	1853-0203
A14Q8	1853-CQ18		TRANSISTOR PNP 51 CHIP TC-72 PD=200MW	28480	1853-0018
A14Q9	1853-0203		TRANSISTOR PNP 51 CHIP TC-18 PD=100MW	28480	1853-0203
A14Q10	1853-0018		TRANSISTOR PNP 51 CHIP TC-72 PD=200MW	28480	1853-0018
A14Q11	1853-CC81		TRANSISTOR J-FET N-CHAN, D-MODE 51	01295	2N5245
A14C11	1853-CC81	4	TRANSISTOR J-FET N-CHAN, D-MODE 51	01295	2N5245
A14C12	1853-CC81		TRANSISTOR J-FET N-CHAN, D-MODE 51	01295	2N5245
A14C13	1853-CC81		TRANSISTOR J-FET N-CHAN, D-MODE 51	01295	2N5245
A14C14	1853-CC81		TRANSISTOR J-FET N-CHAN, D-MODE 51	01295	2N5245
A14C15	1853-CC81		TRANSISTOR J-FET N-CHAN, D-MODE 51	01295	2N5245
A14P1	0884-1C31	1	RESISTOR 10K 10% .25W CC TUBULAR	01121	C81031
A14P2	0757-0401		RESISTOR 100 OHM 1% .125W F TUBULAR	24546	CA-1/B-TO-101-F
A14P3	0757-0401		RESISTOR 100 OHM 1% .125W F TUBULAR	24546	CA-1/B-TO-101-F
A14P4	0884-4721		RESISTOR 4.7K 10% .25W CC TUBULAR	01121	C84721
A14P5	0814-1711		RESISTOR 270 OHM 1% .25W CC TUBULAR	01121	C82711
A14P6	0884-2221	4	RESISTOR 2.2K 10% .25W CC TUBULAR	01121	C82221
A14P7	0884-2221		RESISTOR 2.2K 10% .25W CC TUBULAR	01121	C82221
A14P8	0498-4126		RESISTOR 35.7 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-187-F
A14P9	0498-4415		RESISTOR 165 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-165R-F
A14P11	0498-4421		RESISTOR 249 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-249R-F
A14P12	0498-4437	4	RESISTOR 133 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-133R-F
A14P13	0757-0417		RESISTOR 562 OHM 1% .125W F TUBULAR	24546	CA-1/B-TO-562R-F
A14P14	0757-0433		RESISTOR 3.32K 1% .125W F TUBULAR	24546	CA-1/B-TO-3321-F
A14P15	0498-4416		RESISTOR 35.7 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-187-F
A14P16	0498-4426		RESISTOR 165 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-165R-F
A14P17	0498-4421	4	RESISTOR 249 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-249R-F
A14P18	0498-4417		RESISTOR 133 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-133R-F
A14P19	0757-0413		RESISTOR 3.32K 1% .125W F TUBULAR	24546	CA-1/B-TO-3321-F
A14P21	0757-0417		RESISTOR 562 OHM 1% .125W F TUBULAR	24546	CA-1/B-TO-562R-F
A14P22	0498-4126		RESISTOR 35.7 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-187-F
A14P23	0498-4415	4	RESISTOR 165 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-165R-F
A14P24	0498-4421		RESISTOR 249 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-249R-F
A14P25	0498-4437		RESISTOR 133 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-133R-F
A14P26	0757-0433		RESISTOR 3.32K 1% .125W F TUBULAR	24546	CA-1/B-TO-3321-F
A14P27	0757-0417		RESISTOR 562 OHM 1% .125W F TUBULAR	24546	CA-1/B-TO-562R-F
A14P28	0498-4126	4	RESISTOR 35.7 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-187-F
A14P29	0498-4415		RESISTOR 165 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-165R-F
A14P31	0498-4421		RESISTOR 249 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-249R-F
A14P32	0498-4437		RESISTOR 133 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-133R-F
A14P33	0757-0417		RESISTOR 562 OHM 1% .125W F TUBULAR	24546	CA-1/B-TO-562R-F
A14P34	0757-0413	1	RESISTOR 3.32K 1% .125W F TUBULAR	24546	CA-1/B-TO-3321-F
A14P35	0498-4126		RESISTOR 35.7 OHM 1% .125W F TUBULAR	16299	CA-1/B-TO-187-F
A14P36	2100-3112		RESISTOR-VAR 10K 200 OHM 10% C SIDE / AJ	73138	899A200
A14P37	2100-3112		RESISTOR-VAR 10K 200 OHM 10% C SIDE ADJ	73138	899A200
A14P38	0757-0200		RESISTOR 1K 1% .125W F TUBULAR	24546	CA-1/B-TO-1001-F
A14P39	0498-0196	2	RIFRD FLN 3053 OHM	28480	0498-0196
A14P41	0757-0200		RESISTOR 1K 1% .125W F TUBULAR	24546	CA-1/B-TO-1001-F
A14P42	0498-0196		RIFRD FLN 3053 OHM	28480	0498-0196
A14P43	0498-7952		RIFRD FLN 1804 OHM	28480	0498-7952
A14P44	0498-7952		RIFRD FLN 1804 OHM	28480	0498-7952
A14P45	0498-7952	1	RIFRD FLN 1804 OHM	28480	0498-7952
A14P46	0498-7952		RIFRD FLN 1804 OHM	28480	0498-7952
A14P47	0498-7952		RIFRD FLN 1804 OHM	28480	0498-7952
A14P48	0498-7952		RIFRD FLN 1804 OHM	28480	0498-7952
A14P49	0884-1C31		RESISTOR 10K 10% .25W CC TUBULAR	01121	C81031
A14P51	0884-4721	1	RESISTOR 4.7K 10% .25W CC TUBULAR	01121	C84721
A14P52	2100-3107		RESISTOR-VAR 10K 200 OHM 10% C SIDE ADJ	73138	899A200
A1451	3101-1637	1	SWITCHSLIDE EP4T	28480	3101-1637
A14U1	1820-C203	1	IC DTL MC 1035P SCHMITT TRIGGER	04713	MC1035P
A14U2	1820-C200	1	IC DTL MC 1035P SCHMITT TRIGGER	04713	MC1035P
A14U3	1820-C301	1	IC DTL MC 1032P FLIP-FLOP	04713	MC1032P
A14U4	1820-C359	3	IC LIN LM201AM AMPLIFIER	27014	LM201AM
A14U5	1820-C359	3	IC LIN LM201AM AMPLIFIER	27014	LM201AM
A14U6	1820-C359	3	IC LIN LM201AM AMPLIFIER	27014	LM201AM
A15	03570-46556	1	BOARD ASSY, OUTPUT BUFFER	28480	03570-46556
A15C1	0160-0128	4	CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-0128
A15C2	0160-0128		CAPACITOR-FXD 2.2UF +-20% 25VDC CER	28480	0160-0128
A15C3	0160-0170		CAPACITOR-FXD 2.2UF +-20% 25VDC CER	28480	0160-0170
A15C4	0160-0159		CAPACITOR-FXD 8800PF +-10% 200VDC POLYE	28480	292P88292
A15C5	0150-0016		CAPACITOR-FXD .1UF +-20% 200VDC CER	28480	0150-0016

See Introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A28C1	0180-03C9		CAPACITOR-FPD 4.7UF+-20% 10VDC TA	28289	1500479X0010A2
A28C2	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A28C3	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A28C4	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A28C5	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A28C6	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A28C7	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A28C8	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A28J1	1200-0473	2A	SOCKET: ELEC IC 14-CONT DIP 8LDR TERM	28480	1200-0473
A28J2	1200-0474	2	SOCKET: ELEC IC 14-CONT DIP 8LDR TERM	28480	1200-0474
A28L1	9170-0854		COIL: FPD SHIELDING HEAD: .138 OD .047	02114	94-990-89/4A6
A28L2	9140-0054	4	COIL: FPD POLDED PP CHOKER: .000M 100	24226	19/880
A28L3	9170-0854		COIL: FPD SHIELDING HEAD: .138 OD .047	02114	94-990-89/4A6
A28R1	0683-1039	11	RESISTOR 10K 5% .25W CC TUBULAR	01121	C81039
A28R2	0683-2725		RESISTOR 2.7K 5% .25W CC TUBULAR	01121	C82725
A28R3	0683-2725		RESISTOR 2.7K 5% .25W CC TUBULAR	01121	C82725
A28R4	0683-2725		RESISTOR 2.7K 5% .25W CC TUBULAR	01121	C82725
A28R5	0683-2725		RESISTOR 2.7K 5% .25W CC TUBULAR	01121	C82725
A28R6	1810-0041	8	CIRCUIT: PRV: NON-REPAIRABLE IN	28480	1810-0041
A28R7	1810-0041		CIRCUIT: PRV: NON-REPAIRABLE IN	28480	1810-0041
A28R8	0683-2725		RESISTOR 2.7K 5% .25W CC TUBULAR	01121	C82725
A28R9	0683-2725		RESISTOR 2.7K 5% .25W CC TUBULAR	01121	C82725
A28R10	0683-2725		RESISTOR 2.7K 5% .25W CC TUBULAR	01121	C82725
A28U1	1820-0584	12	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28U2	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A28U3	1820-0584	2	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28U4	1814-0017	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28U5	1814-0018	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28L6	1814-0019	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28L7	1814-0020	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28L8	1814-0021	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28L9	1820-0584	4	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28U10	1820-0584	4	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28L11	1820-0584	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28U12	1820-0584	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A28U13	1820-0584	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A29	03570-88583	1	BOARD ASSY, CONTROL #2	28480	03570-88583
A29C1	0180-03C9		CAPACITOR-FPD 4.7UF+-20% 10VDC TA	28289	1500479X0010A2
A29C2	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A29C3	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A29C4	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A29C5	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A29J1	1200-0473		SOCKET: ELEC IC 14-CONT DIP 8LDR TERM	28480	1200-0473
A29L1	9170-0854		COIL: FPD SHIELDING HEAD: .138 OD .047	02114	94-990-89/4A6
A29L2	9140-0054		COIL: FPD POLDED PP CHOKER: .000M 100	24226	19/880
A29L3	9170-0854		COIL: FPD SHIELDING HEAD: .138 OD .047	02114	94-990-89/4A6
A29R1	1810-0041		CIRCUIT: PRV: NON-REPAIRABLE IN	28480	1810-0041
A29R2	1810-0041		CIRCUIT: PRV: NON-REPAIRABLE IN	28480	1810-0041
A29R3	0683-4721		RESISTOR 4.7K 10% .25W CC TUBULAR	01121	C84721
A29U1	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U2	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U3	1814-0021	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U4	1814-0021	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U5	1814-0021	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A29L6	1814-0021	1	IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U7	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U8	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A29L9	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U10	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U11	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A29U12	1820-0584		IC DTL M72 TOP REGISTER	04713	MC72TOP
A30	03570-88584	1	BOARD ASSY, DELAY/LOW OSC.	28480	03570-88584
A30C1	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C2	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C3	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C4	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C5	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C6	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C7	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C8	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C9	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093
A30C10	0180-0C93		CAPACITOR-FPD .01UF +80-20% 100MVDC CER	28480	0180-0093

See Introduction to this section for ordering information.

Table 6-3. Replaceable Parts(Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A32C6	0180-0053		CAPACITOR-FIXED, .01UF +80-20% 100VDC CER	28480	0180-0053
A32C7	0180-0053		CAPACITOR-FIXED, .01UF +80-20% 100VDC CER	28480	0180-0053
A32C8	0180-0053		CAPACITOR-FIXED, .01UF +80-20% 100VDC CER	28480	0180-0053
A32C9	0180-0053		CAPACITOR-FIXED, .01UF +80-20% 100VDC CER	28480	0180-0053
A33J1	1300-0473		SOCKET; ELEC; IC 14-CHNT DIP SMD TERM	28480	1300-0473
A33L1	9170-C054		CORE; MAG; SHIELDING HEAD; .138 OD .047	02114	96-390-45/4A6
A33L2	9170-C054		CORE; MAG; SHIELDING HEAD; .138 OD .047	02114	96-390-45/4A6
A33L3	9170-C054		CORE; MAG; SHIELDING HEAD; .138 OD .047	02114	96-390-45/4A6
A33M1	0284-1031		RESISTOR 10K 10W .25W CC TUBULAR	01121	CR1031
A33M2	0284-1721		RESISTOR 2.7K 10W .25W CC TUBULAR	01121	CR1721
A33M3	0284-1031		RESISTOR 10K 10W .25W CC TUBULAR	01121	CR1031
A33M4	0284-1031		RESISTOR 10K 10W .25W CC TUBULAR	01121	CR1031
A33M5	0284-1721		RESISTOR 2.7K 10W .25W CC TUBULAR	01121	CR1721
A33M6	0284-1031		RESISTOR 10K 10W .25W CC TUBULAR	01121	CR1031
A33M7	0284-1721		RESISTOR 2.7K 10W .25W CC TUBULAR	01121	CR1721
A33M8	0284-1031		RESISTOR 10K 10W .25W CC TUBULAR	01121	CR1031
A33M9	0284-1721		RESISTOR 2.7K 10W .25W CC TUBULAR	01121	CR1721
A33M10	0284-1721		RESISTOR 2.7K 10W .25W CC TUBULAR	01121	CR1721
A33M11	0284-1031		RESISTOR 10K 10W .25W CC TUBULAR	01121	CR1031
A33U1	1820-0544		IC DCTL MC72 70P REGISTER	04713	MC7270P
A33U2	1820-0544		IC DCTL MC72 70P REGISTER	04713	MC7270P
A33U3	1820-0544		IC DCTL MC74 00A GATE	27014	DM7400M
A33U4	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U5	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U6	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U7	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U8	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U9	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U10	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U11	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U12	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U13	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U14	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U15	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U16	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U17	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U18	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A33U19	1820-0544		IC DCTL MC74 00A GATE	01295	SN7400M
A34A	03670-06668		PC ASSY, INPUT BUFFER	28480	03670-06668
A34AC1	0180-0309		CAPACITOR-FIXED, .47UF +20% 10VDC TA	66269	180022A9015B2
A34AC2, C3	0180-0093		CAPACITOR-FIXED, .01UF +80-20% 100VDC CER	28480	0180-0093
A34AL1, L2	0170-0064		CORE; MAG; SHIELDING HEAD; .138 OD .047	02114	96-390-45/4A6
A34AR1, R2	1810-0136		RESISTIVE NETWORK	28480	1810-0136
A34AU1, U2	1820-0174		IC DCTL MC7400M INVERTER	01295	SN7400M
A34AU3, U4	1820-0637		IC DCTL MC7413N SCHMITT TRIGGER	01295	SN7413M
A34AU5	1820-0766		IC DCTL MC7413N SCHMITT TRIGGER	04713	MC7413P
A34B	03670-06668		PC ASSY, ISOLATOR	28480	03670-06668
A34BC1	0180-0140		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	282P22242
A34BC2	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC3	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	282P22242
A34BC4	0180-0140		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	282P22242
A34BC5	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC6	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	282P22242
A34BC7	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC8	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC9	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC10	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC11	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC12	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC13	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34BC14	0180-0228		CAPACITOR-FIXED, .22UF +20% 10VDC TA-SOLID	66269	180022A9015B2
A34B1	1300-0473		SOCKET; ELEC; IC 14-CHNT DIP SMD TERM	28480	1300-0473
A34B11	9170-C054		CORE; MAG; SHIELDING HEAD; .138 OD .047	02114	96-390-45/4A6
A34B12	9170-C054		CORE; MAG; SHIELDING HEAD; .138 OD .047	02114	96-390-45/4A6
A34B13	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B14	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B15	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B16	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B17	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B18	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B19	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B20	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B21	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B22	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B23	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B24	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B25	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B26	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B27	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B28	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B29	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F
A34B30	0498-4455		RESISTOR 50K 10W .25W F TUBULAR	24346	C4-1/8-YO-338K-F

Table 6-3, Replaceable Parts(Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number	
					NIW	EXCIANON
A1	03570-66558	2	PC Assy: Input Ampl (75 ohm) Opt 001, 003	28480	03570-66558	03570-87902
A1	03570-66558	2	PC Assy: Input Ampl (50 ohm) Std, Opt 002	28480	03570-66558	03570-87901
A2	03570-66559	2	PC Assy: Mixer, IF Ampl (75 ohm) Opt 001, 003	28480	03570-66559	03570-87903
A2	03570-66559	2	PC Assy: Mixer, IF Ampl (50 ohm) Std, Opt 002	28480	03570-66559	03570-87902
A3 thru A4	03570-66533	5	PC Assy: Crystal filter	28480	03570-66533	
A5	03570-66534	1	PC Assy: Bandwidth logic	28480	03570-66534	
A7	03570-66535	1	PC Assy: Log amplifier	28480	03570-66535	03570-87900
A8	03570-66536	1	PC Assy: Power splitter (50 ohm) Std, Opt 002	28480	03570-66536	
A8	03570-66536	1	PC Assy: Power splitter (75 ohm) Opt 001, 003	28480	03570-66536	
A9	03570-66537	1	PC Assy: LO driver	28480	03570-66537	
A10	03570-66538	1	PC Assy: LO generator	28480	03570-66538	
A11	03570-66539	1	PC Assy: VCO	28480	03570-66539	
A13	03570-66540	1	PC Assy: Sampler	28480	03570-66540	
A13	03570-66541	1	PC Assy: Phase limiter	28480	03570-66541	
A14	03570-66542	1	PC Assy: Phase detector	28480	03570-66542	03570-87904
A15	03570-66543	1	PC Assy: Output buffer	28480	03570-66543	03570-87905
A16	03570-66544	1	PC Assy: Analog A-D	28480	03570-66544	03570-87906
A17	03570-66555	1	PC Assy: Input Ampl (75 ohm) Opt 001, 003	28480	03570-66555	03570-87902
A17	03570-66555	1	PC Assy: Input Ampl (50 ohm) Std, Opt 002	28480	03570-66555	03570-87901
A18	03570-66539	1	PC Assy: Mixer, IF Ampl (75 ohm) Opt 001, 003	28480	03570-66539	03570-87903
A18	03570-66539	1	PC Assy: Mixer, IF Ampl (50 ohm) Std, Opt 002	28480	03570-66539	03570-87902
A19 thru A20	03570-66533	1	PC Assy: Crystal filter	28480	03570-66533	
A22	03570-66534	1	PC Assy: Bandwidth logic	28480	03570-66534	
A23	03570-66535	1	PC Assy: Log amplifier	28480	03570-66535	03570-87900
A24	03570-66545	1	PC Assy: Delay generate Opt 002, 003	28480	03570-66545	
A25	03570-66546	1	PC Assy: A-D control	28480	03570-66546	03570-87904
A26	03570-66547	1	PC Assy: A register	28480	03570-66547	03570-87905
A27	03570-66548	1	PC Assy: Timing	28480	03570-66548	
A28	03570-66549	1	PC Assy: ROM control #1	28480	03570-66549	03570-87906
A29	03570-66550	1	PC Assy: ROM control #2	28480	03570-66550	03570-87907
A30	03570-66551	1	PC Assy: Delay and Limit offset Opt 002, 003	28480	03570-66551	
A31	03570-66552	1	PC Assy: ALU and Memory Opt 002, 003	28480	03570-66552	03570-87908
A32	03570-66553	1	PC Assy: Clock	28480	03570-66553	
A33	03570-66554	1	PC Assy: Address recognition	28480	03570-66554	
A34A	03570-66555	1	PC Assy: Input buffer Std, Opt 003	28480	03570-66555	
A34B	03570-66556	1	PC Assy: Isolated input buffer Opt 004	28480	03570-66556	03570-87909
A35	03570-66571	1	PC Assy: IN DEC Register	28480	03570-66571	03570-87910
A36	03570-66572	1	PC Assy: ASCII Output Opt 004	28480	03570-66572	03570-87911
A37	03570-66590	1	PC Assy: Power Supply	28480	03570-66590	
A38	03570-66590	1	PC Assy: Display	28480	03570-66590	
A39	03570-66595	1	PC Assy: Switch board, Front panel	28480	03570-66595	
A50	03570-66598	1	PC Assy: Mother board, digital	28480	03570-66598	
A51	03570-66599	1	PC Assy: Mother board, analog	28480	03570-66599	
			MISCELLANEOUS PARTS			
U1	3160-0286	1	F80	28480	3160-0286	
C1, C2	0180-2489	2	C: Fwd 5000 uF 35V	28480	0180-2489	
C3, C4	0180-2488	2	C: Fwd 15,000 uF 15V	28480	0180-2488	
C5, C6	0160-3333	2	C: Fwd 5000 pF 1.4KV	28480	0160-3333	
C7	0160-3025	1	C: Fwd 4uF	28480	0160-3025	
F1	2110-0003	1	Fuse: 3 Amp NII	75015	2110-0003	
J1	1250-2367	1	Connector: Power Input	28480	1250-2367	
J2 thru J5	1250-0102	5	Connector: IINC	28480	1250-0102	
J6	1250-1414	1	Connector: T/Taxial	03316	1250-1414	
J7, J8	1250-0102	2	Connector: IINC	28480	1250-0102	
J9 thru J12	1250-0116	4	Connector: IINC	24931	1250-0116	
L1, L2	0140-0136	2	Inductor: Fwd RF 22uH	28480	0140-0136	
Q1, Q2	1854-0063	2	TRFR: NPN 2N3055	80131	1854-0063	
Q3	1854-0245	1	TRFR: NPN	28480	1854-0245	
A5	03570-66553	1	PC Assy: Crystal filter	28480	03570-66553	
A21	03570-66553	1	PC Assy: Crystal filter	28480	03570-66553	

Table 6.3. Replaceable Parts(Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
H1, H2	0887-1031	2	H1 Fan 1000 ohm 0.1%	01121	K11 1031
H3	0887-3311	1	H3 Fan 330 ohm 0.1%	01121	K31 3311
S1	3101-1888	1	Switch: Power	28480	3101-1888
S2 thru S4	3101-1881	3	Switch: Pushbutton	00383	3101-1881
S5, S6	3101-0883	2	Switch: Slide	28480	3101-0883
S7	3103-0020	1	Switch: Thermal reset	28480	3103-0020
T1	0100-3278	1	Transformer: Power	28480	0100-3278
U1	1820-0430	1	IC: Linear (Power supply)	28480	1820-0430
W1	03570-81810	1	Cable Assy: Line switch	28480	03570-81810
W2	03570-81803	1	Cable Assy: Front panel HF Input	28480	03570-81803
W3	03570-81888	1	Cable Assy: Power Splitter Output	28480	03570-81888
W4	03570-81808	1	Cable Assy: 20-MHz HF Input	28480	03570-81808
W5	03570-81806	1	Cable Assy: 1 MHz HF Input	28480	03570-81806
W6	03570-81880	1	Cable Assy: Rear Panel HF Input	28480	03570-81880
W7	03570-81830	1	Cable Assy: Analog Output	28480	03570-81830
W8	03570-81831	1	Cable Assy: Digital A50 to A51	28480	03570-81831
W9	03570-81832	1	Cable Assy: Front Panel A55 to A56	28480	03570-81832
W10	03570-81831	1	Cable Assy: Digital, A55 to A56	28480	03570-81831
W11	03570-81822	1	Cable Assy: Digital, A55 to A56	28480	03570-81822
W12	03570-81823	1	Cable Assy: Digital, A55 to A56	28480	03570-81823
W13	03570-81824	1	Cable Assy: Digital, A55 to A56	28480	03570-81824
W14	03570-81825	1	Cable Assy: Digital, A55 to A56	28480	03570-81825
W15	03570-81826	1	Cable Assy: Digital, A55 to A56	28480	03570-81826
W16	03570-81828	1	Cable Assy: Mother Board A51 to A57	28480	03570-81828
XA1, XA2	1251-1888	12	Connector: 15 contact (1x15)	71785	252-15-30-350
XA3 thru XA5	1251-0478	6	Connector: 12 contact (2x6)	71785	252-06-30-340
XA6	1251-1888	6	Connector: 30 contact (2x15)	71785	252-15-30-320
XA7 thru XA12	1251-1888	10	Connector: 15 contact (1x15)	71785	252-15-30-350
XA13	1251-1888	1	Connector: 30 contact (2x15)	71785	252-15-30-340
XA14	1251-1888	1	Connector: 15 contact (1x15)	71785	252-15-30-350
XA15, XA16	1251-1888	2	Connector: 30 contact (2x15)	71785	252-15-30-340
XA17, XA18	1251-1888	2	Connector: 15 contact (1x15)	71785	252-15-30-350
XA19 thru XA21	1251-0478	3	Connector: 12 contact (2x6)	71785	252-06-30-340
XA22	1251-1888	1	Connector: 30 contact (2x15)	71785	252-15-30-340
XA23	1251-1888	1	Connector: 15 contact (1x15)	71785	252-15-30-350
XA24 thru XA26	1251-1888	3	Connector: 30 contact (2x15)	71785	252-15-30-340
XA27 thru XA29	1251-2414	3	Connector: 60 contact (2x30)	71785	252-25-30-340
XA30A/B	1251-1888	1	Connector: 30 contact (2x15)	71785	252-15-30-340
XA31 thru XA36	1251-2414	6	Connector: 60 contact (2x30)	71785	252-25-30-340
XA37	1251-2573	1	Connector: 18 contact (1x18)	28480	1251-2573
XF1	3110-0470	1	FUSEHOLDER-EXTR POST POA 300V	04703	3110-0470
	3110-0465	1	FUSEHOLDER-EXTR POST UL10C	28480	3110-0465
	0360-1612	1	TERMINAL-GOLDER STUD	08701	6T-1000SL-1L
	3180-0240	1	Filter: Fan (Fan)	28480	3180-0240
	3180-0260	1	Guard: Fan blade	28480	3180-0260
	03570-02345	1	Cover: Power Switch	28480	03570-02345
	03570-06860	1	Bracket: Transformer	28480	03570-06860
	03570-22002	1	Trim: Top	28480	03570-22002
	03570-22003	1	Trim: Bottom	28480	03570-22003
	03570-22004	1	Trim: Center	28480	03570-22004
	03570-22501	1	Cover: Power Supply Top	28480	03570-22501
	03570-22502	1	Cover: Power Supply Bottom	28480	03570-22502
	03570-22503	1	Cover: Top Rear Left	28480	03570-22503
	03570-22504	1	Hard: Extender	28480	03570-22504
	03570-66501	1	Board: Extender 20 contact (2x10)	28480	03570-66501
	03570-66502	1	Board: Extender 12 contact (2x6)	28480	03570-66502
	03570-66503	1	Manual: Operating and Service	28480	03570-66503
	03570-00000	1	Window: Display	28480	4114-0721
	4114-0721	1	Cover: Front Side	28480	5000-8520
	5000-8520	1	Cover: Rear Side	28480	5000-8531
	5000-8531	1	Frame: Side	28480	03570-22001
	03570-22001	1	Handle Assy	28480	5000-0222
	5000-0222	1	Foot Assy	28480	5000-0167
	5000-0167	1	Retainer: Handle B1	28480	5000-8737
	5000-8737	1	Cord: Power (U.C. Only)	70903	K118-7041
	70903	1	Card: Instruction	28480	0230-0055
	0230-0055	1	Cover: Top Left	28480	03570-05503
	03570-05503	1	Cover: Top Center	28480	03570-05505
	03570-05504	1	Cover: Top Right	28480	03570-05504
	03570-05505	1	Cover: Outside Top	28480	03330-04117
	03330-04117	1	Cover: Outside Bottom	28480	03330-04118

SECTION VII

TROUBLESHOOTING AND CIRCUIT DIAGRAM

7-1. INTRODUCTION.

7-2. This section of the manual contains troubleshooting information and circuit diagrams for the Model 3570A Network Analyzer. Included are troubleshooting trees, a functional block diagram, schematic diagrams and component location diagrams.

7-3. TROUBLESHOOTING.

7-4. Troubleshooting Trees.

7-5. Figure 7-3 through 7-10 are troubleshooting trees designed to assist in the isolation of malfunctions. Table 7-1 is a list of the troubleshooting trees and their respective figure numbers.

Table 7-1. Troubleshooting Trees.

Figure	Troubleshooting Tree
7-3	Preliminary Troubleshooting Tree
7-4	Single Channel Amplitude Troubleshooting Tree
7-5	Dual Channel Amplitude Troubleshooting Tree
7-6	Phase Troubleshooting Tree
7-7	A/D Display Troubleshooting Tree
7-8	Timing, Control, and PS Register Troubleshooting Tree
7-9	Remote Troubleshooting Tree
7-10	Option Troubleshooting Tree

7-6. Troubleshooting Procedure.

NOTE

Digital Block Diagrams, Flowcharts, and Instructions for using the 1601A are located beginning with Part, graph 7-14.

7-7. The following procedure is recommended to efficiently determine the source of trouble in the 3570A:

a. Determine the exact symptoms of the problem. If necessary, attempt the Performance Checks outlined in Section V to verify that a problem exists.

b. Once the nature of the problem is defined, attempt the Adjustment Procedures outlined in Section V. Some apparent malfunctions can be corrected by these adjustments or the inability to obtain correct adjustment will often reveal the source of trouble.

c. Check for burned or loose components, loose connections or any other obvious condition that might be the source of trouble.

d. Go first to the Preliminary Troubleshooting Tree (Figure 7-1). The preliminary tree will lead to one of several other trees which should lead to the cause of the problem.

e. If the end of a tree is reached without finding the trouble, carefully recheck the symptoms and again go through the appropriate trees. Watch for marginal or erratic voltages at measurement points. If the trouble still cannot be localized, use the schematics for further troubleshooting. The troubleshooting trees may be helpful in indicating which boards could cause the problem even though they do not lead directly to the problem.

7-8. Instructions for Using the 1601A Logic State Analyzer.

7-9. The 1601A, when used in conjunction with the flowcharts, can be a valuable aid in troubleshooting. The basic procedure involves connecting the 1601A to the Present State Bus and then monitoring the state changes and the functions associated with each state.

7-10. Access to the Present State Bus is provided by a test jack located on PC card A28 (ROM Control No. 1). The test jack contains all of the bus data plus the Control Clock and a system ground. Connection to the test jack can best be accomplished by the use of a sixteen pin adapter (see Figure 7-1). Once the adapter is inserted into the socket, the 1601A can be connected to the adapter via an IC test clip.

7-11. Connect the leads from the 1601A Data Probes as follows:

a. Connect bits 0 to 5 to IC clip pins 1 to 6.

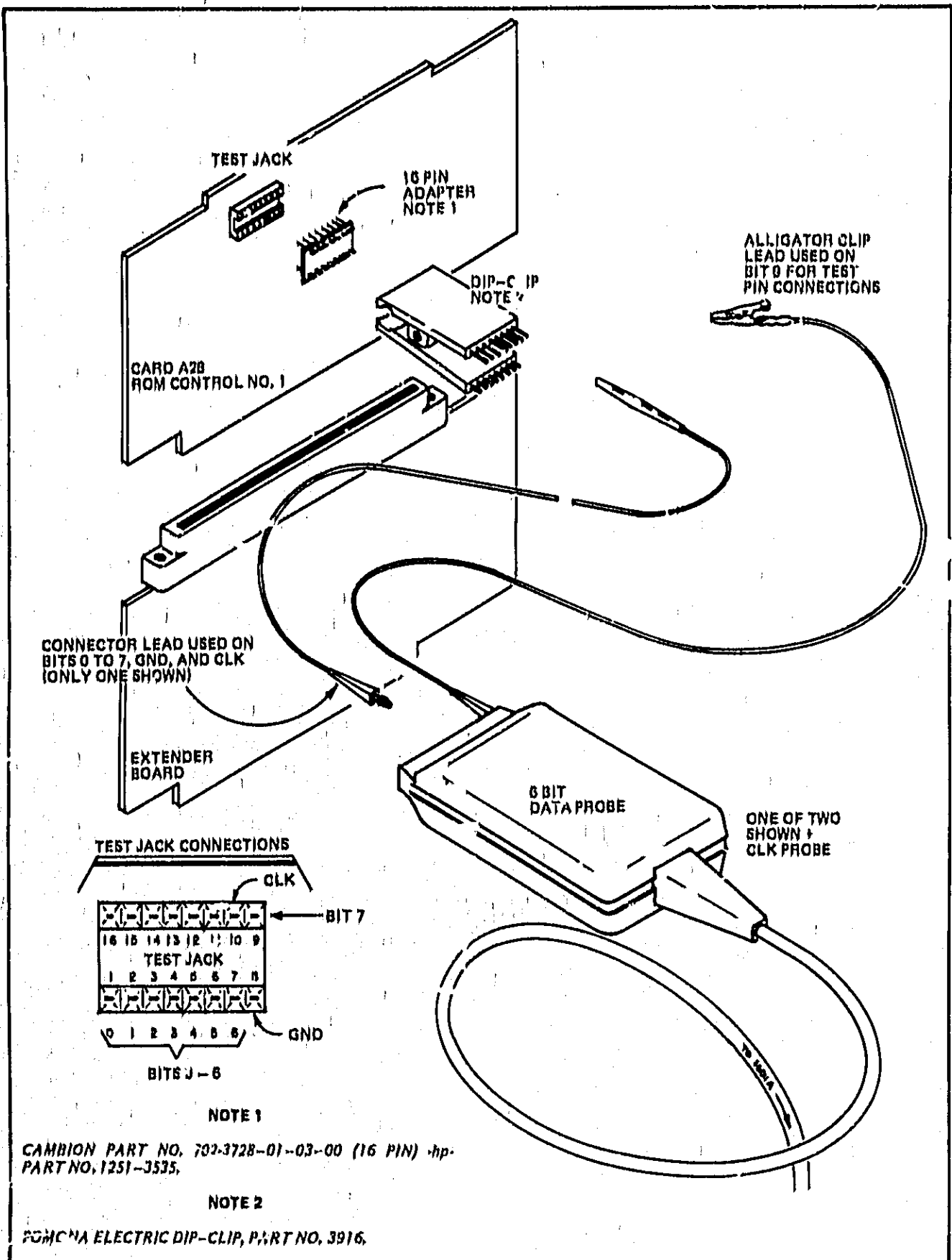


Figure 7-1. Connecting the I601A Logic State Analyzer.

b. From the second Data Probe, connect bits 6 and 7 to IC clip pins 7 and 9 respectively. Then place an alligator clip lead in bit position 9 on the Data Probe. Other leads may remain unconnected.

c. From the Clock Probe, connect the CLK lead to IC clip pin 10 and the GND lead to pin 8.

7-12. Set the switches of the 1601A as follows:

LOGIC	POS
CLOCK	POS
THRESHOLD	TTL
SAMPLE MODE	SINGLE
TRIGGER MODE	START DISPLAY
DELAY SET	ZERO
BYTE	OCT

When the 1601A is turned on, set COLUMN BLANKING for a ten column display.

7-13. Set the Analyzer TRIGGER WORD switches as follows:

- Set bit positions 8 through 11 to the OFF position.
- Bits 0 through 7 are used to set the state number.

7-14. Use the 1601A for troubleshooting as follows:

- Turn on the 1601A, 3570A, and 33302.
- Use the flowcharts to determine the area of possible program execution error. As an example, if the 3570A does not process numerical entries from the HP-IB but otherwise operates correctly, a good place to investigate first would be the Data Entry Routine.

c. Set the TRIGGER WORD switches (bits 0 - 7) to the state (or the state which begins a routine) of interest.

d. Connect the alligator clip (bit 9) to the TTL test point in question. For example, the alligator clip could be connected to the Qualifier Output (TP Q).

e. Press the SAMPLE MODE RESET BUTTON and observe the display on the 1601A.

7-15. The display on the 1601A will indicate in 1's and 0's the digital values for sixteen successive states (see Figure 7-2). The order of the states displayed should correspond to the order of the states in the flowchart. Note, however, that a state which loops back upon itself (state 114) will indicate the same state numbers until the looping operation is terminated by a qualifier. In this case, set the TRIGGER WORD switches to the next state and press the Sample Mode RESET button.

7-16. Since the 1601A displays only sixteen lines of binary code, it will be necessary to reset the TRIGGER WORD switches for each group of sixteen successive states.

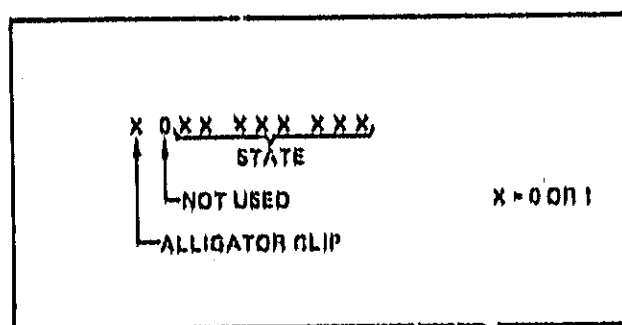


Figure 7-2. 1601A Display.

7-17. To verify that an instruction is being executed during a state, connect the alligator clip to the instruction test point and press the Sample Mode RESET button (see Digital Block Diagram for instruction sources and test points). The 1601A will now display the logic level of that instruction and the associated state. This procedure can be used to display the logic level of any Decode ROM output.

7-18. The 1601A may also be used to aid in determining if data resulting from a register transfer operation is present on a bus. This troubleshooting technique requires the use of another oscilloscope. Connect the Trigger Output from the 1601A to the Trigger Input of the oscilloscope. Set the TRIGGER WORD switches to the state previous to the state under examination. With a scope probe connected to a bus, adjust the oscilloscope for the best display (approximately 2 microsecond/cm sweep rate). If the instruction is operating and the data is available, the oscilloscope will show strings of pulses.

7-19. The troubleshooting techniques given will aid in isolating the problem to a component or group of components. Further troubleshooting can be implemented with an oscilloscope or logic probe and the schematics in Section VII.

7-20. FUNCTIONAL BLOCK DIAGRAM.

7-21. The Functional Block Diagram, Figure 7-9, is a detailed block diagram showing the overall relationship between the major circuit elements in the analog section of the 3570A. The diagram shows the main signal paths and provides information that should be helpful when troubleshooting the instrument.

7-22. SCHEMATIC DIAGRAMS.

7-23. The schematic diagrams, Figure 7-10 through 7-32, show the detailed circuits of the standard Model 3570A and Options 001 through 004. Each schematic is assigned a numerical callout (1 through 23) which is used for referencing. The schematics are arranged to provide as much signal continuity as possible and assemblies do not necessarily appear in the order of their reference designations. Refer to Table 7-2 for a complete cross reference listing.

Table 7-2. Assembly Cross Reference.

Assembly Number	Ship Part No.	Assembly Title	Schematic Number	Assembly Number	Ship Part No.	Assembly Title	Schematic Number
A1	03570-66551	Input Amplifier (A)	2	A21	03570-66553	Crystal Filter (B)	3
A2	03570-66532	Input Mixer (A)	2	A22	03570-66534	Bandwidth Logic (B)	3
A3	03570-66533	Crystal Filter (A)	3	A23	03570-66555	Log Amplifier (B)	4
A4	03570-66533	Crystal Filter (A)	3	A24	03570-66545	Delay Prescaler*	10
A5	03570-66533	Crystal Filter (A)	3	A25	03570-66546	A - D Control	7, 11
A6	03570-66534	Bandwidth Logic (A)	3	A26	03570-66547	A Register	11
A7	03570-66555	Log Amplifier (A)	4	A27	03570-66551	Timing Assembly	18
A8	03570-66536	Power Splitter	1	A28	03570-66552	ROM Control No. 1	10
A9	03570-66538	L.O. Buffer	5	A29	03570-66553	ROM Control No. 2	10
A10	03570-66537	L.O. Generator	8	A30	03570-66554	Delay and Limit Offset Option*	20
A11	03570-66539	VCO	9	A31	03570-66555	ALU and Memory*	21
A12	03570-66540	Sampler	9	A32	03570-66556	Clock and Basic Annunciator	14
A13	03570-66541	Phase Limiter	5	A33	03570-66557	Address Recognition	15
A14	03570-66542	Phase Detector	5	A34A	03570-66558	Input Buffer	16
A15	03570-66556	Output Buffer	5	A34B	03570-66559	Isolated Input Buffer**	17
A16	03570-66544	Analog A - D	7	A35	03570-66571	B1 DEC Register	12
A17	03570-66551	Input Amplifier (B)	2	A36	03570-66572	ASCII Output**	22
A18	03570-66532	Input Mixer (B)	2	A37	03570-66590	Power Supply	23
A19	03570-66533	Crystal Filter (B)	3	A38	03570-66580	Display	13
A20	03570-66533	Crystal Filter (B)	3	A39	03570-66585	Front Panel Switch	5, 6, 15, 20

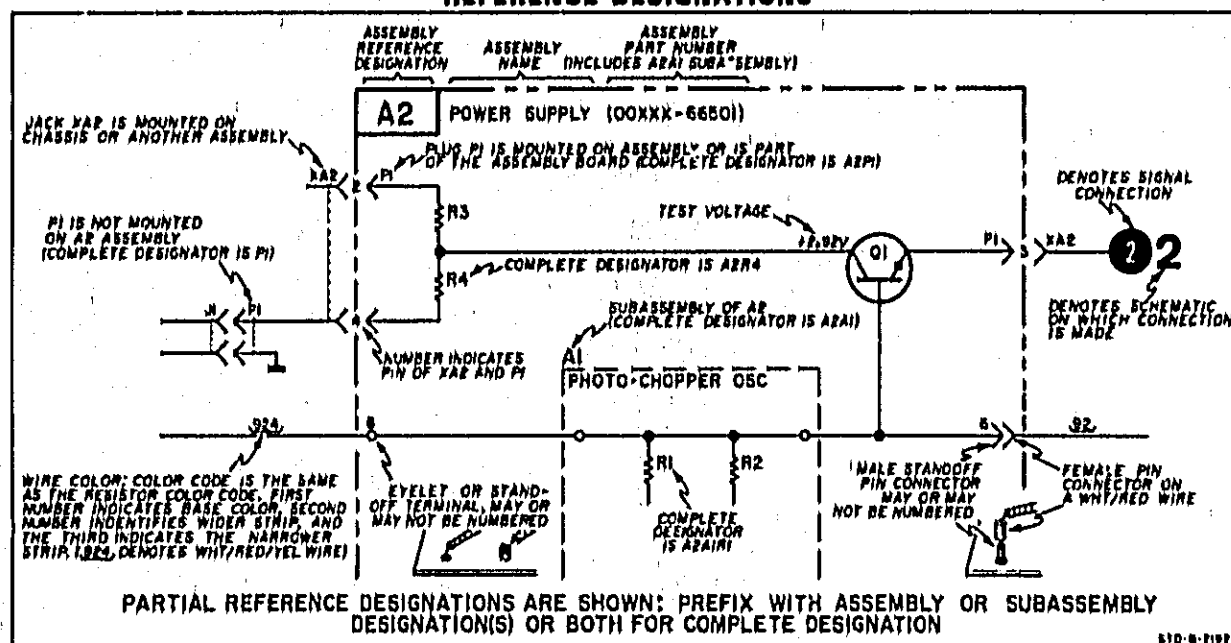
*Options 002, 003 only

**Option 004 only

7-24. Notes.

7-25. Refer to the General Schematic Notes for further information concerning the schematic diagrams.

REFERENCE DESIGNATIONS



GENERAL SCHEMATIC NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH ASSEMBLY OR SUBASSEMBLY DESIGNATION(S) OR BOTH FOR COMPLETE DESIGNATION.

2. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED,
RESISTANCE IN OHMS
CAPACITANCE IN MICROFARADS
INDUCTANCE IN MILLIHENRYS

3.  DENOTES EARTH GROUND, USED FOR TERMINALS WITH NO LESS THAN A NO. 18 GAUGE WIRE CONNECTED BETWEEN TERMINAL AND EARTH GROUND TERMINAL OR AC POWER RECEPTACLE.

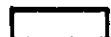
4.  DENOTES FRAME GROUND, USED FOR TERMINALS WHICH ARE PERMANENTLY CONNECTED WITHIN APPROXIMATELY 0.1 OHM OF EARTH GROUND.

5.  DENOTES GROUND ON PRINTED CIRCUIT ASSEMBLY, (PERMANENTLY CONNECTED TO FRAME GROUND).

6.  DENOTES ASSEMBLY.

7.  DENOTES MAIN SIGNAL PATH.

8.  DENOTES FEEDBACK PATH.

10.  DENOTES FRONT PANEL MARKING.

11.  DENOTES REAR PANEL MARKING.

12.  DENOTES SCREWDRIVER ADJUST.

13. AVERAGE VALUE SHOWN, OPTIMUM VALUE SELECTED AT FACTORY. THE VALUE OF THESE COMPONENTS MAY VARY FROM ONE INSTRUMENT TO ANOTHER. THE METHOD OF SELECTING THESE COMPONENTS IS DESCRIBED IN SECTION V OF THIS MANUAL.

14.  DENOTES SECOND APPEARANCE OF A CONNECTOR PIN.

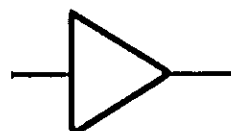
15. 924 DENOTES WIRE COLOR; COLOR CODE SAME AS RESISTOR COLOR CODE. FIRST NUMBER IDENTIFIES BASE COLOR, SECOND NUMBER IDENTIFIES WIDER STRIP, THIRD NUMBER IDENTIFIES NARROWER STRIP, (e.g. - WHITE, RED, YELLOW.)

17. ALL RELAYS ARE SHOWN DEENERGIZED.

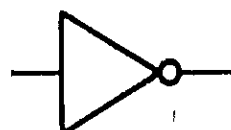
18. WAVEFORMS AND AC VOLTAGE MEASUREMENTS WERE MADE WITH RESPECT TO CHASSIS GROUND USING AN OSCILLOSCOPE WITH A 10:1 DIVIDER PROBE (10 MEGOHM, 10 pF). THE VOLTAGE LEVELS SHOWN ON THE WAVEFORMS ARE ACTUAL VOLTAGE LEVELS AND ARE NOT TO BE CONFUSED WITH OSCILLOSCOPE SETTING. THE VOLTAGE LEVELS SHOWN ARE NOMINAL AND MAY VARY FROM ONE INSTRUMENT TO ANOTHER. A VARIATION OF $\pm 10\%$ IN MEASUREMENTS SHOULD BE ALLOWED.

19. DC VOLTAGE LEVELS WERE MEASURED WITH RESPECT TO CIRCUIT GROUND USING A VTVM WITH 10 MEGOHM

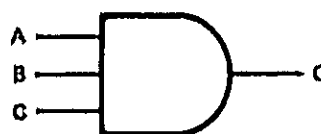
INPUT IMPEDANCE. THE VOLTAGE LEVELS SHOWN ARE NOMINAL AND MAY VARY FROM ONE INSTRUMENT TO ANOTHER DUE TO CHANGE IN TRANSISTOR CHARACTERISTICS. A VARIATION OF $\pm 10\%$ SHOULD BE ALLOWED.



DENOTES BUFFER



DENOTES INVERTER



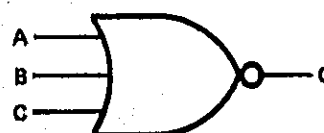
DENOTES AND GATE

A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



DENOTES NAND GATE

A	B	C	Q
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



DENOTES NOR GATE

A	B	C	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



DENOTES EXCLUSIVE OR GATE

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

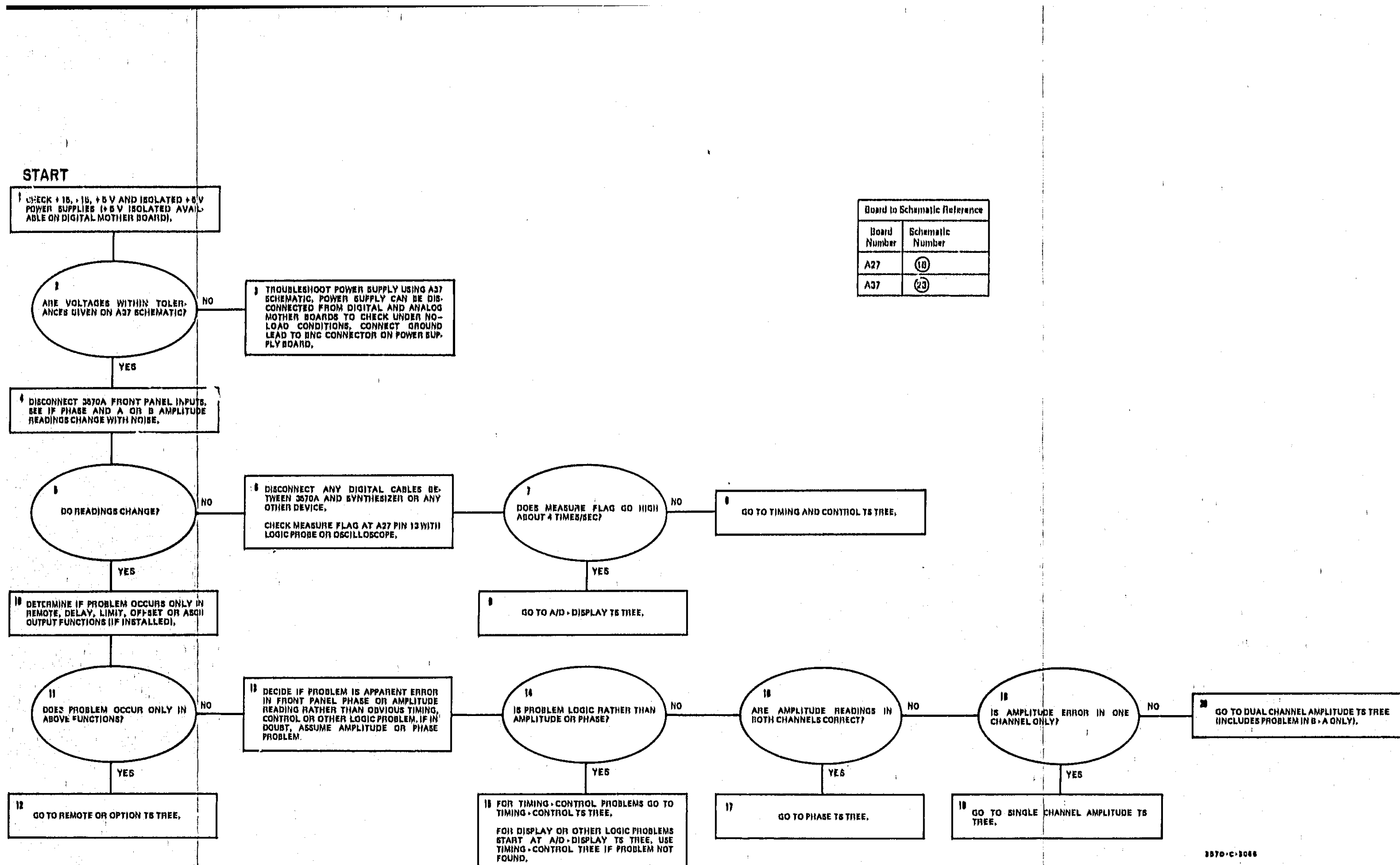


Figure 7-3. Preliminary Troubleshooting Tree.
7-7/7-8

START

1 SET SYNTHESIZER OUTPUT TO 1 VOLT (1.001 GHz/50 MHz, 1.1 GHz/50 MHz), 50 MHz. SET 3670A REF V TO 1 VOLT.

MEASURE FRONT PANEL OUTPUTS FOR BOTH CHANNELS WITH DVM/DCI TERMINATED IN 50 OHMS.

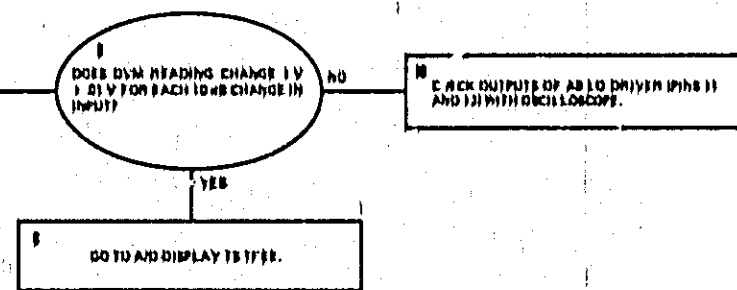
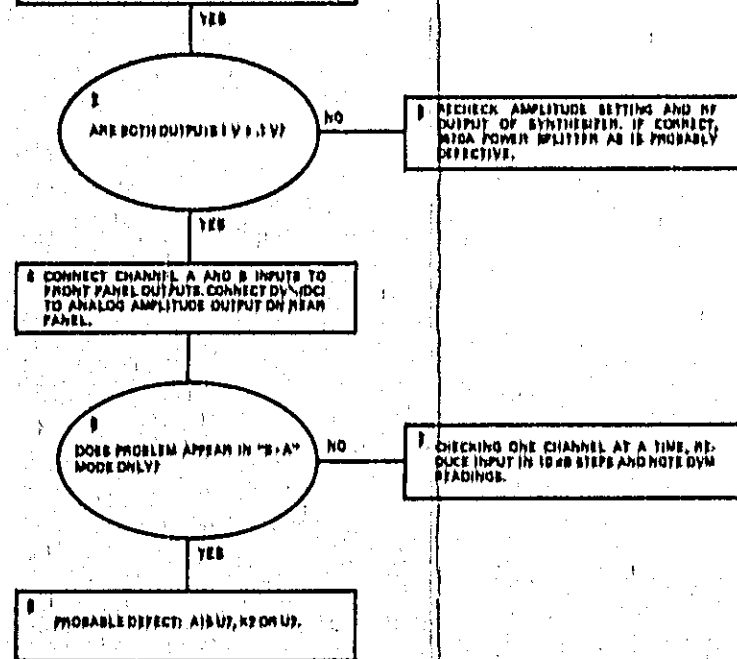
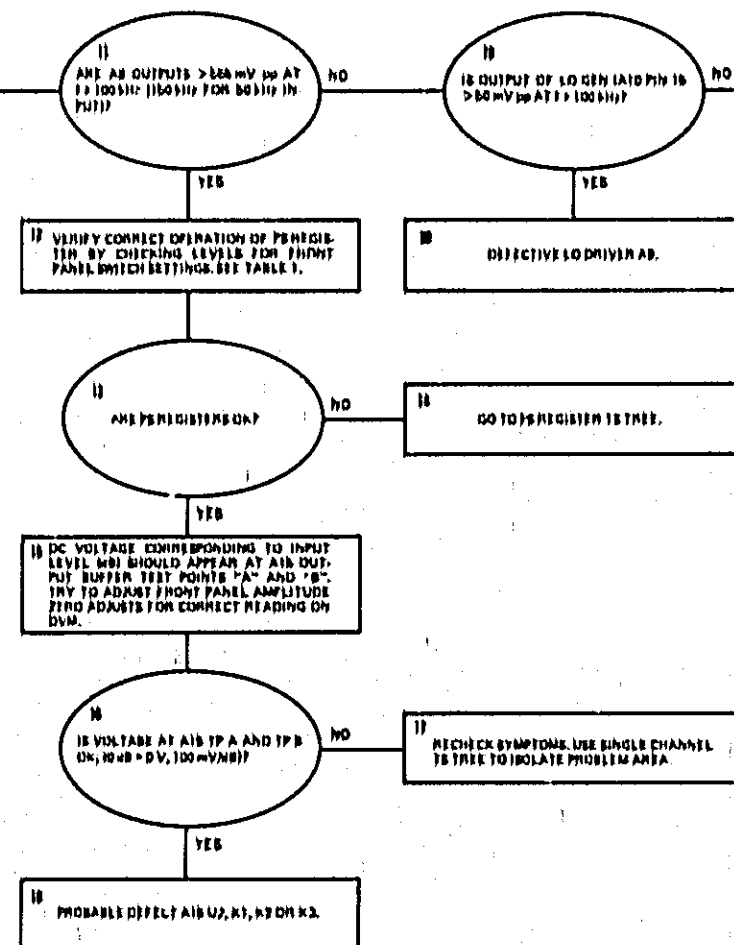


TABLE 1
PSEUDO-LOGIC LEVELS

> 1.8 V = "1"
< .8 V = "0"

AMPLITUDE FUNCTION		SAMPLER MODE		MARKER INPUT VOLTAGE			BANDWIDTH			PHASE REF	
PS1	PS2	PS3	PS4	PS5	PS6	PS7	PS8	PS9	PS10	PS11	PS12
A	B	A	B	A	B	A	B	A	B	A	B
1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0

PS1 CAN ONLY BE CHANGED WHILE IN REMOTE. IT IS NOT USED IN THE ANALOG SECTION OF THE 3670A.



Board to Schematic Reference

Board Number	Schematic Number
A8	①
A9, A10	②
A11, A12	③
A15	④

NOTE 1

100 MHz PHASE-LOCKED LOOP CHECKS

1. Disconnect 1 MHz cable between synthesizer and 3670A. Leave 20 ± 22 MHz cable connected.
2. Connect synthesizer RF Output to 3670A 1 MHz input.
3. Set synthesizer to 1 MHz, 1 V output.
4. Connect counter to 100 MHz Test Point on VCKO board (A11). (Counter settings: 1 V range, 1 second time base)
5. Counter should read 1000000 MHz ± .000010 MHz (approximately 125 mV p-p square wave).
6. Connect DVM (DC) to VCKO Control TP on A11. Voltage should be less than ± 1 V.
7. Change 1 MHz from synthesizer to 100 Hz.
8. 100 MHz should change ± 2 kHz, and DC control voltage should change ± 1.5 V.
9. If this happens, the VCKO is probably working correctly.

NOTE 2

A11 VCKO CHECKS

1. Remove A12 Sampler board.
2. Ground A11 pin 1 and measure frequency at pin 11.
3. Frequency should read 10000 MHz ± 2 kHz. This is basic frequency of VCKO. Replace VCKO if not in specifications.
4. Apply DC voltage (not to exceed ± 3 V) to A11 pin 1 and measure frequency at pin 11. Each 1.5 volt change should produce approximately a 2 kHz frequency change. If not, replace A11.
5. These tests verify VCKO is good. Defective A12 Sampler board is probable cause of 100 MHz loop malfunction. Bad A12 can be confirmed in the following test:

A12 SAMPLER CHECKS

1. Place A12 on extender board. Remove A11.
2. Disconnect all signals to 3670A from synthesizer.
3. Use synthesizer to apply 1 MHz (35 V rms) (1 V p-p) signal directly to A12 pin 1.
4. Use external source, such as hp 8600A synthesizer to apply 100 MHz signal directly to A12 pin 11.
5. The control voltage at A12 pin 1 should be a slowly varying signal. The frequency of this signal should increase from less than 1 Hz as either input frequency is varied in 1 Hz steps. If frequency cannot be reduced to less than 1 Hz, or will not change, A12 is bad.

Figure 7-5, Dual Channel Amplitude Troubleshooting Tree.
7-11/7-12

START

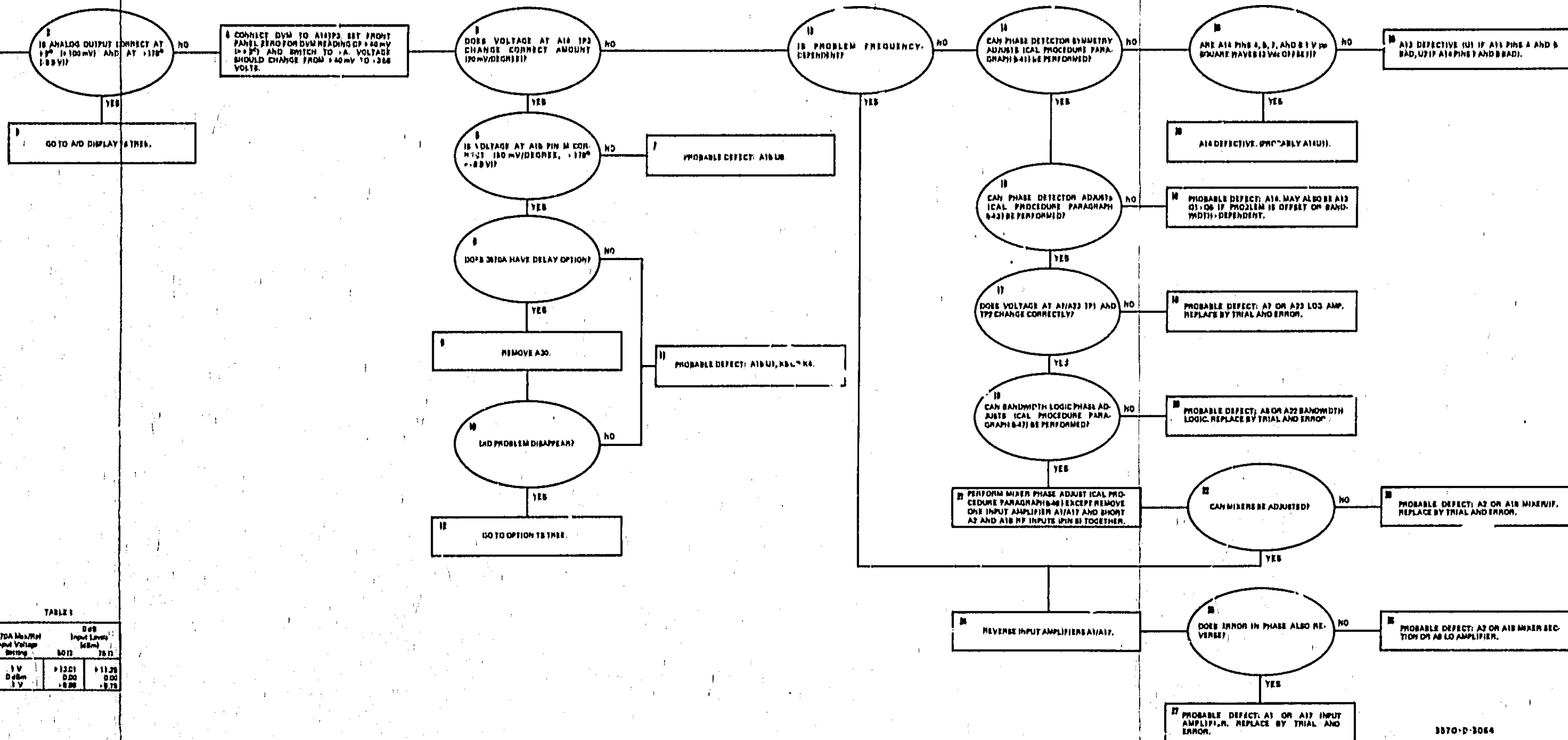
NOTE: CHANNEL A AND B AMPLITUDES SHOULD BE WORKING BEFORE TROUBLESHOOTING PHASE PROBLEMS.
CONNECT FRONT PANEL OUTPUTS TO CHANNEL A AND B INPUTS THROUGH 50Ω CHIA TERMINATIONS USING SHORT CABLES OF IDENTICAL LENGTH. APPLY 0dB INPUT (SEE TABLE 1, 3070A BANDWIDTH) TO 3MHz, PHASE REF TO "A".

CONNECT DVM TO ANALOG PHASE OUTPUT ON REAR PANEL. ATTEMPT TO ZERO OUTPUT ON EACH BANDWIDTH USING FRONT PANEL PHASE ZERO ADJUSTS (10mV).

SET ANALOG PHASE TO 100mV (1-2°) IF POSSIBLE AND SWITCH PHASE REF TO "A".

Board Number	Schematic Number
A1, A17	①
A2, A11	②
A7, A23	③
A13, A14	④
A15	⑤
A22	⑥
A30	⑦

TABLE 1		0dB Input Levels (dBm)	
3070A Max/Mn Input Voltage Setting	50Ω	75Ω	
1V	+13.01	+11.75	
0.1V	0.00	0.00	
0.01V	-8.00	-9.75	



3070-D-3064

Figure 7-6. Phase Troubleshooting Tree.
7-13/7-14

START

NOTE
ANALOG AMPLITUDE AND PHASE OUTPUTS SHOULD BE OPERATING CORRECTLY BEFORE TROUBLESHOOTING A/D DISPLAY PROBLEMS.

1. IF ANNUNCIATOR IS NOT WORKING PROPERLY, SEE NOTE 1.
2. TURN POWER OFF.
3. REMOVE A30, A31 AND A36 IF OPTIONS 002, 003 OR 004 ARE INSTALLED.
4. REMOVE A26 A REGISTER FROM 3670A, DISCONNECT CABLE FROM A26 TO A25.
5. TURN POWER ON.
6. SET PHASE/DELAY SWITCH TO PHASE.

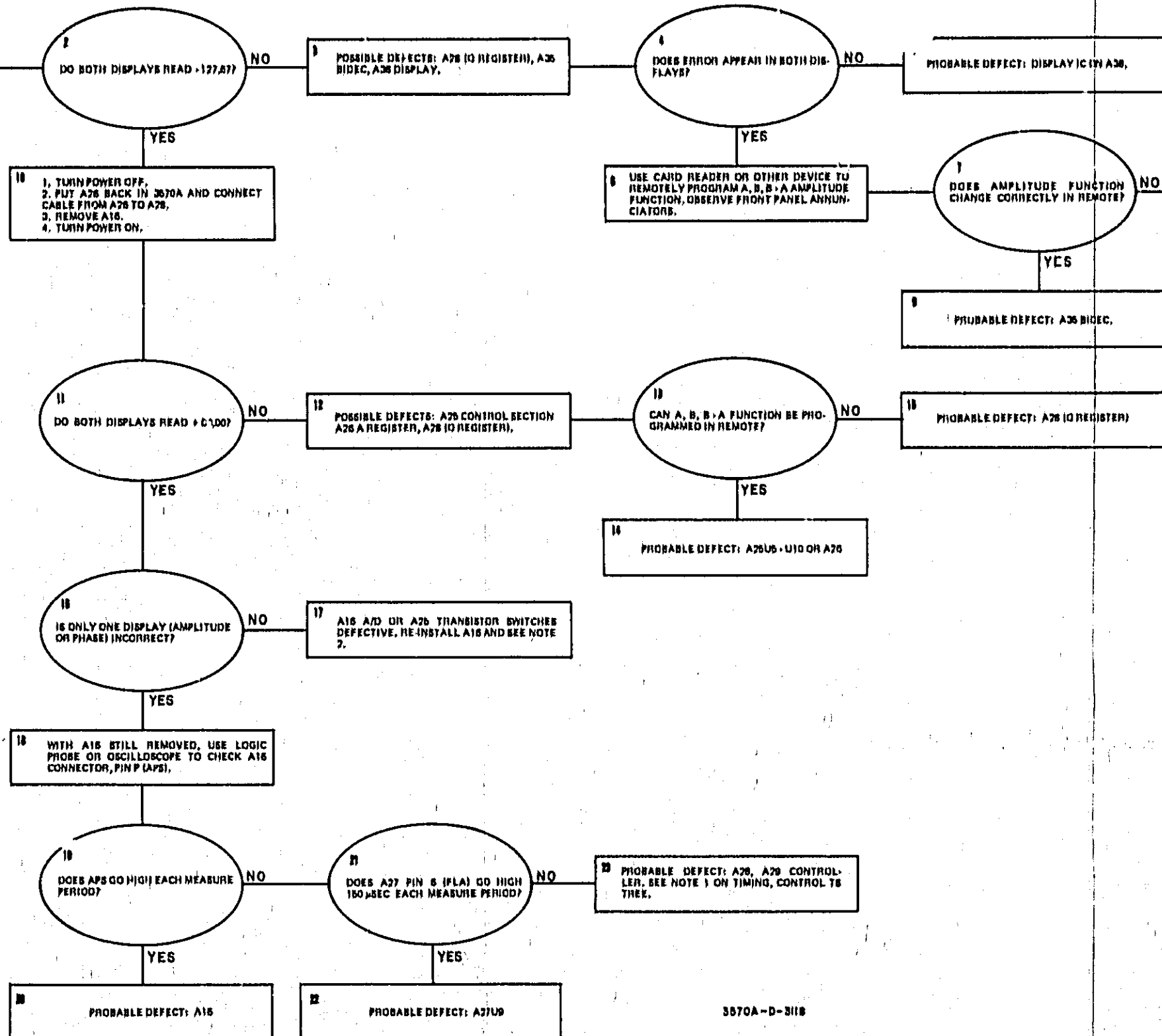
NOTE 1
ANNUNCIATORS
CONTROL SIGNALS FOR THE FOLLOWING ANNUNCIATORS COME TO THE FRONT PANEL BY MEANS OF A CABLE FROM A32. THE BOARDS ON WHICH THE SIGNALS ACTUALLY ORIGINATE ARE LISTED FOR CONVENIENCE.

ANNUNCIATOR	ORIGINATING BOARD
AMPLITUDE/PH	A32
A	A33 (P84)
B	A33 (P86, P87)
PHASE/D	A33 (P87)
A.O.L.	A32 (A30 FOR OPTION 002 AND 003)
B.O.L.	A8
REMOTE	A22
	A34

OPTIONS 002 AND 003. CONTROL SIGNALS FOR THE FOLLOWING ANNUNCIATORS COME TO THE FRONT PANEL BY MEANS OF A CABLE FROM A30. ALL SIGNALS ORIGINATE ON A30.

OFFSET (AMPLITUDE)
OFFSET (PHASE/DELAY)
DELAY
MSEC
USEC
DELAY DECIMAL POINTS
AMPLITUDE LIMIT TEST ARROW
PHASE/DELAY LIMIT TEST ARROW
HI
GO
LO

Board to Schematic Reference	
Board Number	Schematic Number
A16	(7)
A26	(7) (11)
A28	(11)
A27	(10)
A28	(12) (18)
A29	(18)
A33	(18)
A36	(12)
A38	(13)



NOTE 2
PROCEDURE TO CHECK A26 A/D CONTROL SWITCHES AND A16 RESISTIVE LADDER NETWORK

1. REMOVE A26 A REGISTER.
2. USE A26 SCHEMATIC TO DETERMINE PIN NUMBERS AND SHORT EACH INPUT LINE WHILE MEASURING THE CORRESPONDING OUTPUT VOLTAGE. LEFT-MOST CONNECTOR IS KA26A (INPUTS), RIGHT-MOST CONNECTOR IS KA26B (OUTPUTS).
3. VOLTAGE ON OUTPUT LINES SHOULD BE $10V \pm 1\%$. WHEN THE INPUT IS OPEN, AND 0 VOLTS WHEN THE INPUT IS SHORTED. ALL LINES SHOULD HAVE THE SAME HIGH AND LOW LEVELS.
4. IF ANY VOLTAGES ARE INCORRECT, CHECK THE CORRESPONDING TRANSISTOR SWITCHES ON A26.
5. IF TRANSISTOR SWITCHES ARE GOOD, CHECK THE A16 RESISTIVE LADDER NETWORK USING THE PROCEDURE LISTED BELOW.
6. CONNECT DVM TO A16U8 PIN 2.
7. EACH INPUT TO THE LADDER NETWORK CAUSES THE OUTPUT VOLTAGE TO CHANGE ACCORDING TO THE BINARY WEIGHTINGS OF THE INPUTS.
8. WITH A26 REMOVED, DVM SHOULD READ $10V \pm 1\%$. SHORTING EACH A26 INPUT SHOULD REDUCE THE DVM READING TO:

$V_{oc} (1 - 2^{-N})$,
WHERE N IS KA26A PIN NO., AND V_{oc} IS VOLTAGE WITH ALL PINS OPEN.

THE FOLLOWING TABLE GIVES REDUCTION FACTOR:

SHORT A26 INPUT PIN NO. (N)	$1 - 2^{-N}$
1	.50000
2	.75000
3	.87500
4	.93750
5	.96875
6	.98438
7	.99219
8	.99610
9	.99805
10	.99902
11	.99951
12	.99976
13	.99988
14	.99994
15	.99997

EXAMPLE:
 $V_{oc} = 10.0000$ (ON DVM)
SHORT A26 INPUT PIN 4
DVM SHOULD READ:
 $10.0000 \times .93750 = 9.3750V$

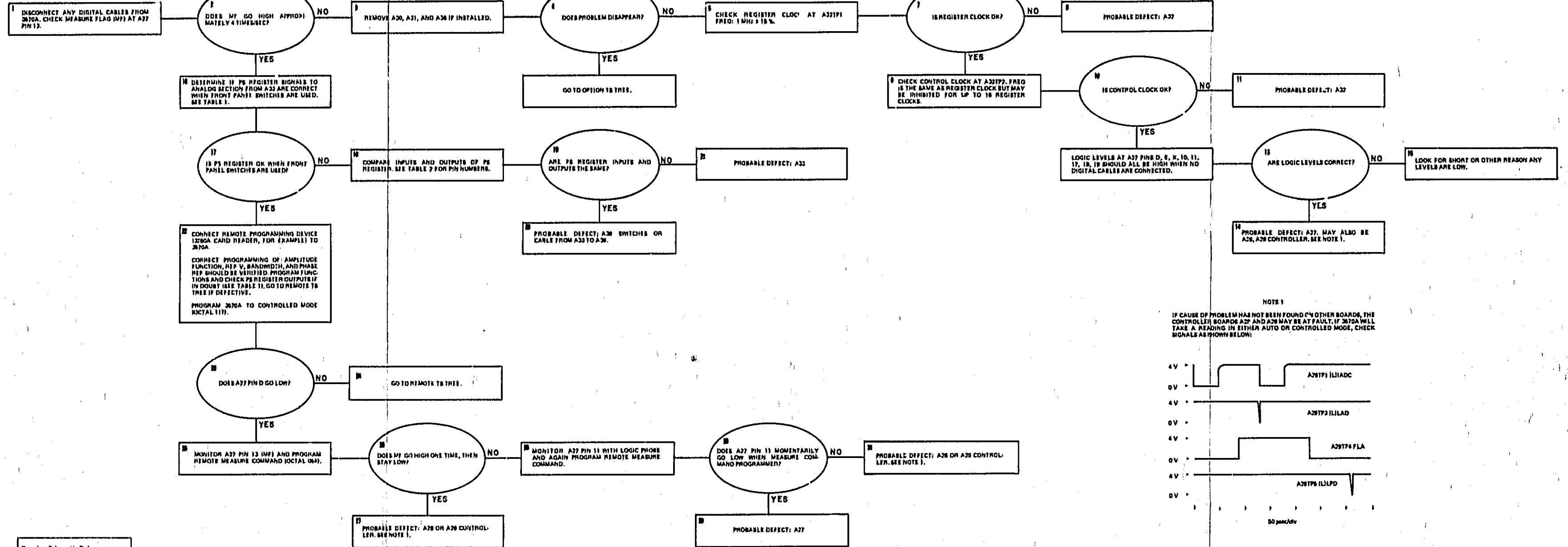
9. IF DVM READINGS ARE CORRECT A26 SWITCHES AND A16 RESISTIVE LADDER NETWORK ARE WORKING CORRECTLY.

10. ERRORS IN LADDER NETWORK OUTPUT WILL CAUSE ERROR IN 3670A DISPLAYS.

3670A-D-3118

Figure 7-7. A/D - Display Troubleshooting Tree.
7-15/7-16

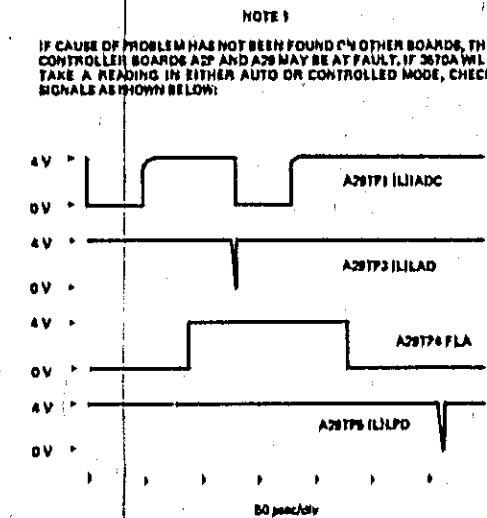
START



Board to Schematic Reference	
Board Number	Schematic Number
A27	18
A28	19
A30	20
A31	21
A32	14
A33	15
A36	22
A39	5 6 15 20

TABLE 1 PS REGISTER LOGIC LEVELS V<2.5V="1" V>2.5V="0"											
AMPLITUDE FUNCTION		SAMPLE MODE*		MAXIMUM INPUT VOLTAGE		BANDWIDTH		PHASE REF			
PS1	PS6	PS1	PS6	PS1	PS6	PS1	PS6	PS1	PS6	PS1	PS6
A	B	1	1	1V	1	33Hz	1	A	1		
B	A	1	1	1V	1	100 Hz	1	A	1		
A33	C	D		1V	1	10 Hz	1	A	1		
*PS6 CAN ONLY BE CHANGED WHILE IN REMOTE. IF NOT USED IN THE ANALOG SECTION OF THE 3570A.											

TABLE 2 PS REGISTER A32/P1 AND U2		
PS1	PARALLEL INPUTS (FRONT PANEL OPERATION)	OUTPUTS
PS1	U2 PIN 2	U2 PIN 4
PS6	U2 PIN 1	U2 PIN 8
PS4	U2 PIN 12	U2 PIN 10
PS2	U1 PIN 2	U1 PIN 4
PS3	U1 PIN 1	U1 PIN 8
PS5	U1 PIN 12	U1 PIN 10
PS7	U1 PIN 1	U1 PIN 1



NOTE 1
IF CAUSE OF PROBLEM HAS NOT BEEN FOUND ON OTHER BOARDS, THE CONTROLLER BOARDS A27 AND A28 MAY BE AT FAULT. IF 3570A WILL TAKE A READING IN EITHER AUTO OR CONTROLLED MODE, CHECK SIGNALS AS SHOWN BELOW:

3570A SHOULD BE SET FOR AMPLITUDE AND PHASE MEASUREMENTS WITH NO LIMIT TEST OR OFFSET FUNCTIONS IN USE. USE A28/P1 AS REFERENCE SIGNAL AND TRIGGER, AND MONITOR OTHER TEST POINTS WITH OTHER CHANNEL OF DUAL TRACT OSCILLOSCOPE. TEST POINTS ARE ON RIGHT SIDE OF A28. A28/P2 (LDI) IS USED ONLY IN DELAY MEASUREMENTS, AND WILL CHANGE FROM ONE STATE TO ANOTHER FOR EACH SUCCESSIVE READING IN THE DWP DELAY MODE.

IF SIGNALS ARE CORRECT, CONTROLLER IS PROBABLY WORKING CORRECTLY.

IF SIGNALS ARE NOT CORRECT, CONTROLLER IN BOARD A28 OR A29 MAY BE DEFECTIVE. MISSING QUALIFIERS TO A28 COULD ALSO CAUSE A PROBLEM. QUALIFIERS USED IN THE BASIC MEASUREMENT ROUTINE (AMPLITUDE AND PHASE) ARE MF, DF, FLA AND ADC.

ANOTHER SOURCE OF CONTROLLER ERRORS COULD BE DEFECTIVE CONTROL CLOCK AND DECODE INHIBIT CIRCUITRY ON A37.

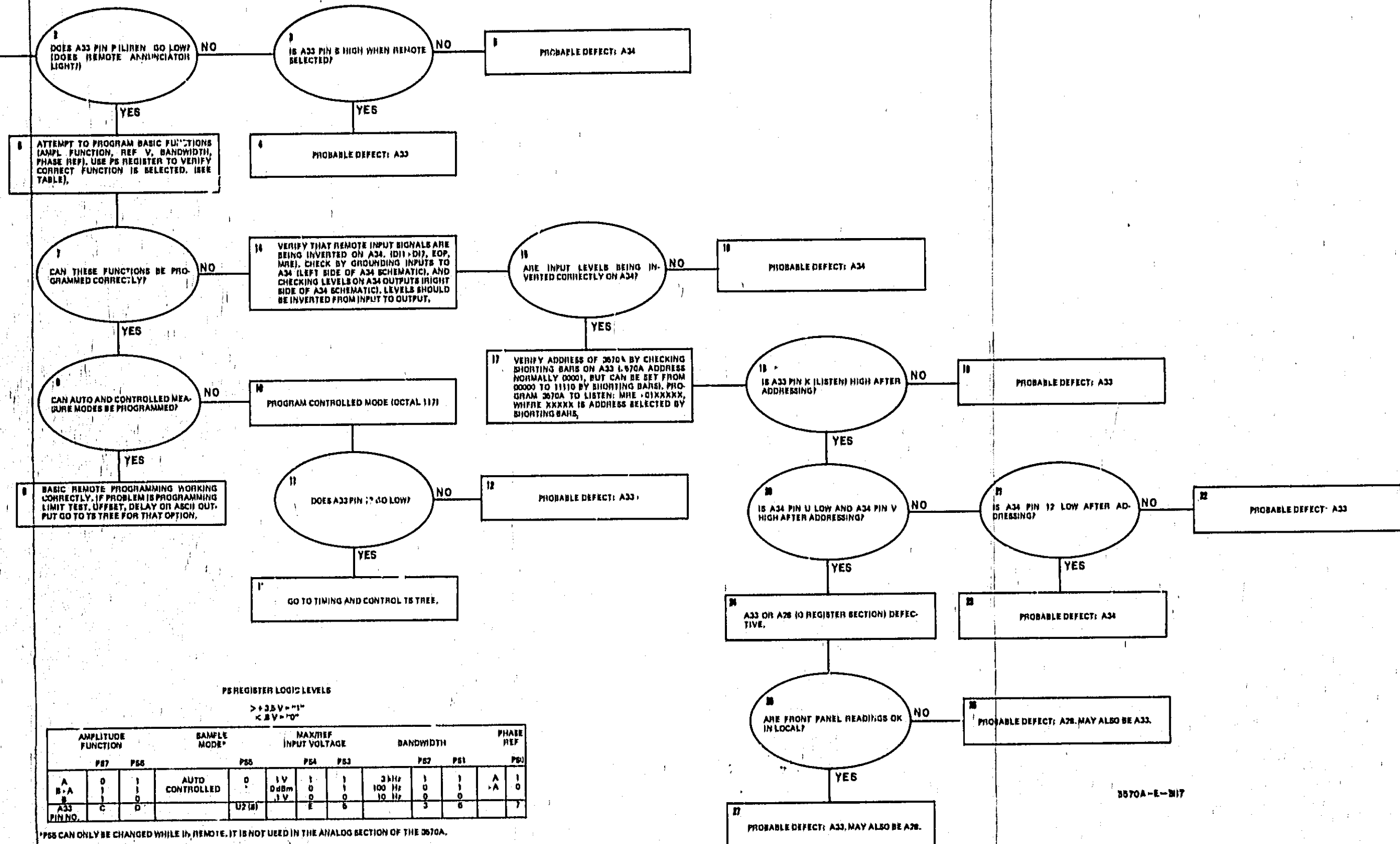
IF 3570A WILL NOT TAKE A MEASUREMENT, A28 AND A29 SHOULD BE REPLACED BY TRIAL AND ERROR.

3570A-D-51/6

Figure 7-8. Timing, Control and PS Register Troubleshooting Tree.

START

GROUND REMOTE LINE INEAR CONNECTION PIN 6). THIS IS DONE AUTOMATICALLY WHEN 3570A CARD READER IS TURNED ON.



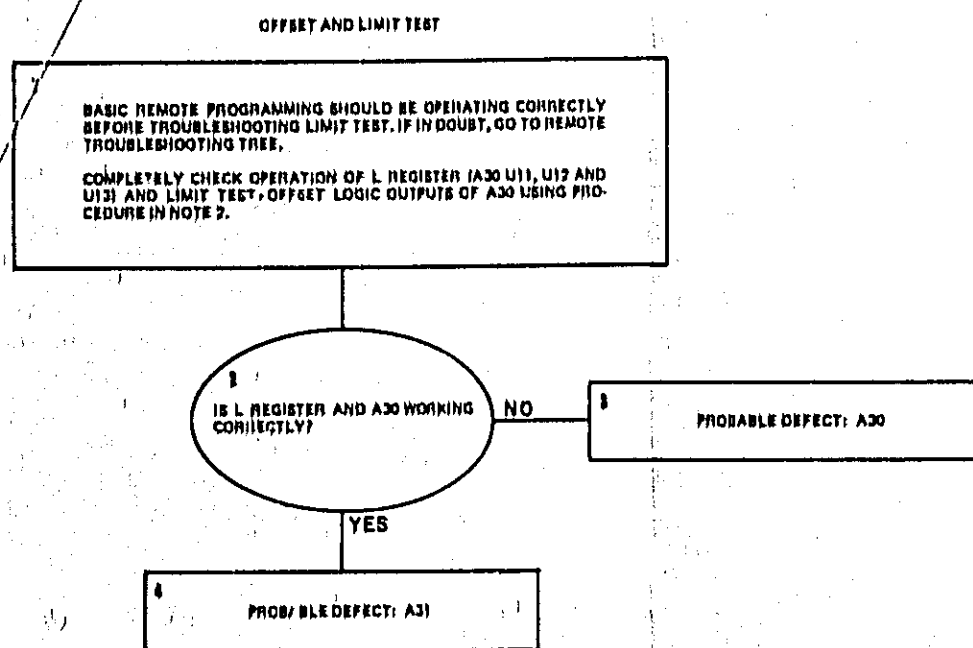
Board to Schematic Reference	
Board Number	Schematic Number
A28	18
A33	15
A34A & B	16 17

PS REGISTER LOGIC LEVELS										
> +3.5V = "1"										
< 2.5V = "0"										
AMPLITUDE FUNCTION	SAMPLE MODE*		MAX/REF INPUT VOLTAGE			BANDWIDTH			PHASE REF	
	PS7	PS8	PS5	PS4	PS3	PS2	PS1	PS0		
A-B-A	0	1	0	1	1	1	1	1	A	1
B-A	1	1	0	0	1	0	1	1	A	0
B	1	0		0	0	0	0			
A33	C	D	U2 (A)	E	B	3	6			7
PIN NO.										

*PS5 CAN ONLY BE CHANGED WHILE IN REMOTE. IT IS NOT USED IN THE ANALOG SECTION OF THE 3570A.

3570A-E-217

Figure 7-9. Remote Troubleshooting Tree. 7-19/7-20



NOTE 2

LIMIT TEST AND OFFSET LOGIC TROUBLESHOOTING

LIMIT TEST AND OFFSET FUNCTIONS ARE CONTROLLED BY L REGISTER (U1), U12 AND U13) ON A30. COMPLETELY CHECK L REGISTER BY ENTERING OFFSETS IN LOCAL AND REMOTE, AND BY PROGRAMMING LIMIT TEST FUNCTIONS REMOTELY. CHECK LOGIC LEVELS AT L REGISTER TEST POINTS ON A30, AND COMPARE WITH TABLE. LEVELS MAY BRIEFLY CHANGE STATE ONCE EACH MEASURE PERIOD, BUT "STEADY STATE" LEVELS ARE LEVELS OF INTEREST.

L REGISTER

ENTRY SEQUENCE	LIMIT SWEEP		AMPL OFFSET		PHASE/DELAY OFFSET		LIMIT TEST MODE		L REGISTER CONDITION	
	L0	L1	L2	L3	L4	L5	L6	L7	L8	L9
NO ENTRY	0	X	X	STOP	0	ABSOLUTE	0	ABSOLUTE	0	NONE
AMPL OFFSET	1	0	0	NO STOP	1	RELATIVE	1	RELATIVE	1	LO
PHASE/DELAY OFFSET	1	0	1							HI
UPPER LIMIT	1	1	0							GO
LOWER LIMIT	1	1	1							

X = DON'T CARE

"0" <+ 8V
"1" >+ 35V

L0 WILL GO HIGH WHENEVER FOLLOWING COMMANDS ARE GIVEN:

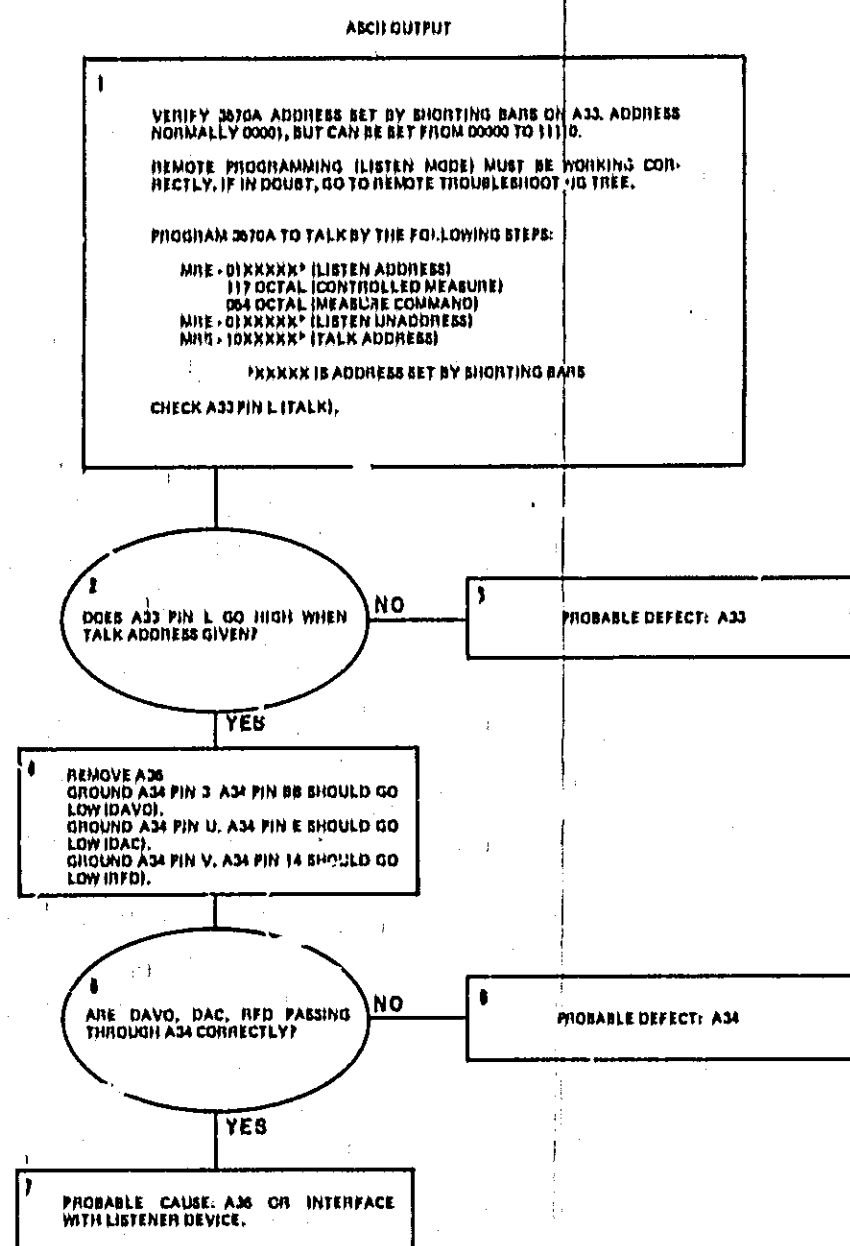
AMPL OFFSET
PHASE/DELAY OFFSET
UPPER LIMIT
LOWER LIMIT

L0 WILL REMAIN HIGH AS DIGITS ARE ENTERED AFTER ANY OF THESE COMMANDS. L0 WILL GO LOW WHEN A COMMAND OTHER THAN ONE OF THE FOUR LISTED ABOVE IS RECEIVED, THIS WILL TERMINATE THE DIGIT ENTRY SEQUENCE.

L1 AND L8 ARE DETERMINED BY THE 3670A AND SHOULD CORRESPOND TO THE FRONT PANEL LIMIT TEST ANNUNCIATORS.

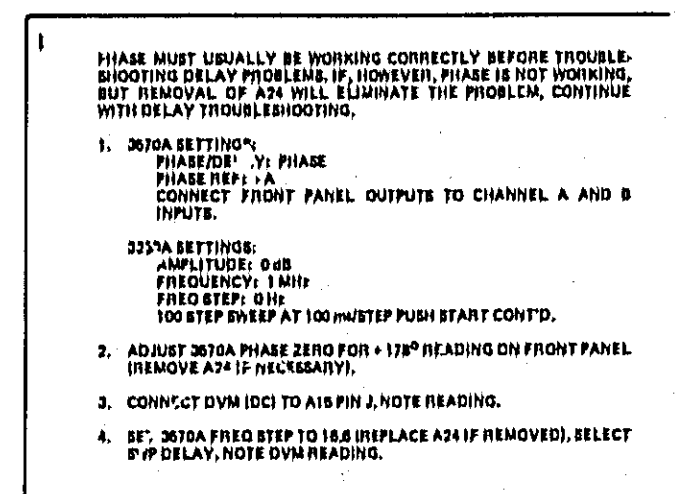
A30 LOGIC LEVELS (PINS ON RIGHT CONNECTOR):

PIN L1: 0 = LIMIT TEST MODE
PIN L2: 0 = LIMIT TEST STOP MODE
PIN L3: NORMALLY HIGH, LOW PULSES GENERATED WHEN EITHER "ENTER OFFSET" BUTTON PUSHED IN LOCAL OR "ENTER OFFSET" BUTTON PUSHED IN REMOTE



Board to Schematic Reference

Board Number	Schematic Number
A30	(20)
A31	(21)
A33	(16)
A34	(17)
A36	(22)



NOTE 1

DELAY LOGIC TROUBLESHOOTING D REGISTER AND A30

USE FRONT PANEL SWITCHES TO CHANGE DELAY SETTING AND OBSERVE LOGIC LEVELS ON TEST POINTS FOR D REGISTER ON LEFT SIDE OF A30. LEVELS MAY MOMENTARILY CHANGE STATE ONCE EACH MEASURE PERIOD, BUT THE "STEADY STATE" LEVEL IS THE ONE OF INTEREST.

D REGISTER (A30 U1, U2)

FREQ STEP	FREQ MULTIPLIER		SWP/CW	
	D7 D6	D5 D4 D3	D2	D1 D0
5 Hz	0 0	1 0 0 0	PHASE	0
10 Hz	0 1	1 0 0 1	SWP	0
20 Hz	1 0	0 1 0 0	DELAY	1
166 Hz	1 1	1 0 1 1	CW	1

X = DON'T CARE

IF LEVELS ARE NOT CORRECT, VERIFY THAT LEVELS AT INPUT TO U1 AND U2 FROM FRONT PANEL SWITCHES ARE CORRECT (SEE A30 SCHEMATIC).

REPEAT THE ABOVE CHECK OF OUTPUTS, THIS TIME REMOTELY PROGRAMMING THE DELAY MODES. (BASIC REMOTE SHOULD BE WORKING, SEE REMOTE TROUBLESHOOTING TREE IF IN DOUBT.) IF LEVELS ARE NOT CORRECT A30 IS PROBABLY DEFECTIVE.

IF D REGISTER OUTPUTS ARE CORRECT, CHECK THE FOLLOWING A30 OUTPUTS WHILE IN DELAY MODE (PINS ON LEFT CONNECTOR OF A30):

PIN 6 (L) CW DELAY: 1 = SWP DELAY OR PHASE
0 = CW DELAY
PIN 9 (L) SWP DELAY: 1 = CW DELAY OR PHASE
0 = SWP DELAY
PIN 8 (L) DELAY: 1 = PHASE
2 = DELAY
PIN 3 (L) 16.8 Hz: 1 = 5, 10, 20 Hz
0 = 16.8 Hz

OUTPUTS IN DELAY MODE

SIGNAL	A30 PIN	FREQ MULTIPLIER					
		X1	X10	X100	X1K	X10K	
(L) 1 SEC	P	0	0	0	1	1	
(L) 10 SEC	N	1	1	1	0	1	
(L) 100 SEC	M	1	1	0	1	1	
(L) 1000 SEC	L	1	0	1	1	0	
(L) 10000 SEC	K	0	1	1	0	1	
CXP	H	0	0	0	1	1	
BEXP	7	0	1	1	0	0	
AEXP	6	1	0	0	0	0	

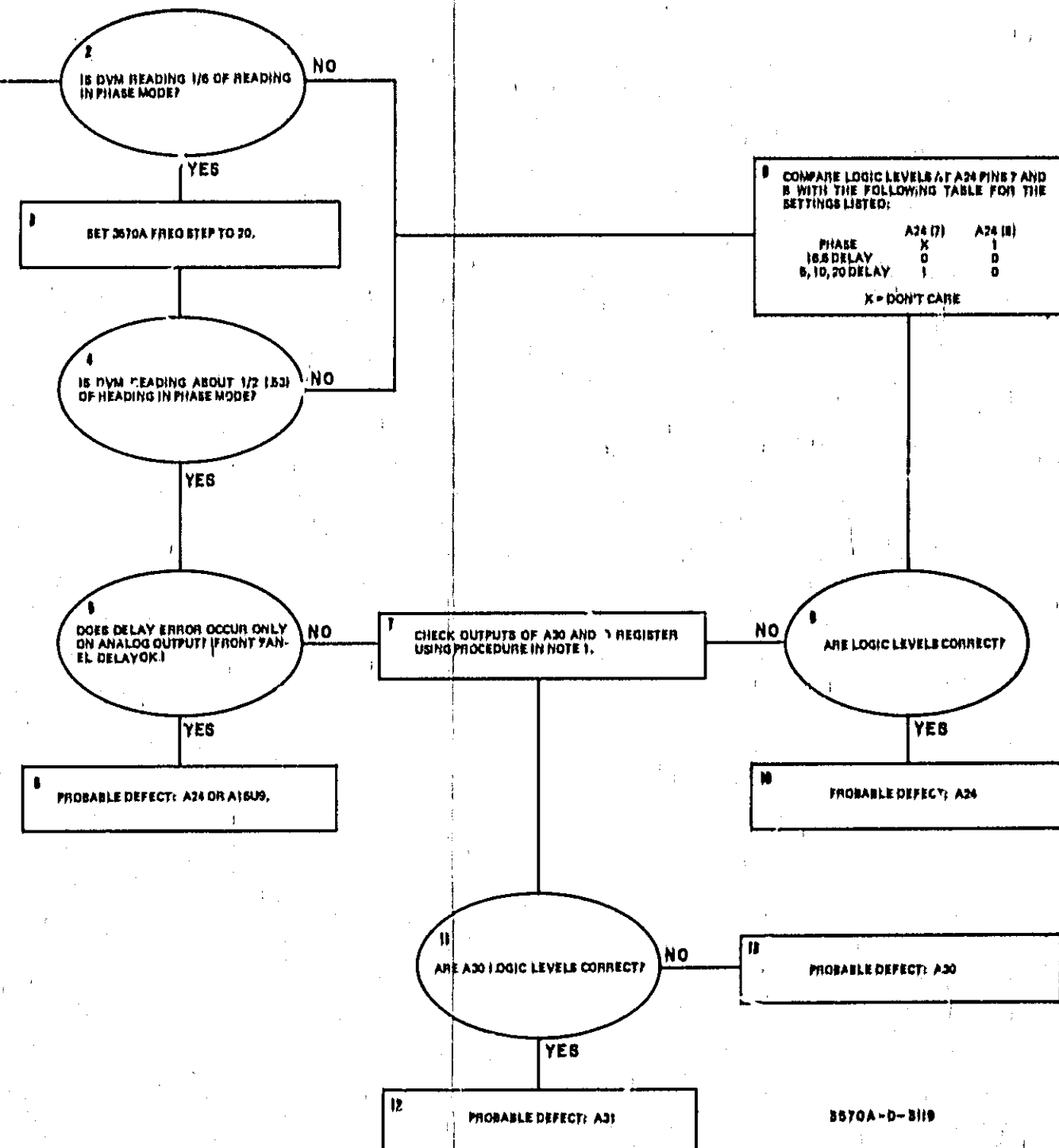


Figure 7-10. Option Troubleshooting Tree.
7-21/7-22

3570A Max/Ref Input Voltage Setting	0 dB Input Levels (dBm)		Voltage at A1/A17 Pin 5 with 0 dB Input Applied (V rms)		Voltage at A2/A18 Pin 1 with 0 dB Input (V rms)	A1/A17 Input Attenuation (dB)		A2/A18 I.F. Gain (dB)	
	50 Ω	75 Ω	50 Ω	75 Ω	50/75 Ω	50 Ω	75 Ω	50 Ω	75 Ω
1 V	+13.01	+11.25	.224 $\pm$.025	.274 $\pm$.025	1 $\pm$.1	13	+1.25	13	+11.25
0 dBm	0.00	0.00	.224 $\pm$.025	.274 $\pm$.025	1 $\pm$.1	0	0	13	+11.25
.1 V	-6.90	-8.75	.100 $\pm$.01	.100 $\pm$.01	1 $\pm$.1	0	0	20	20

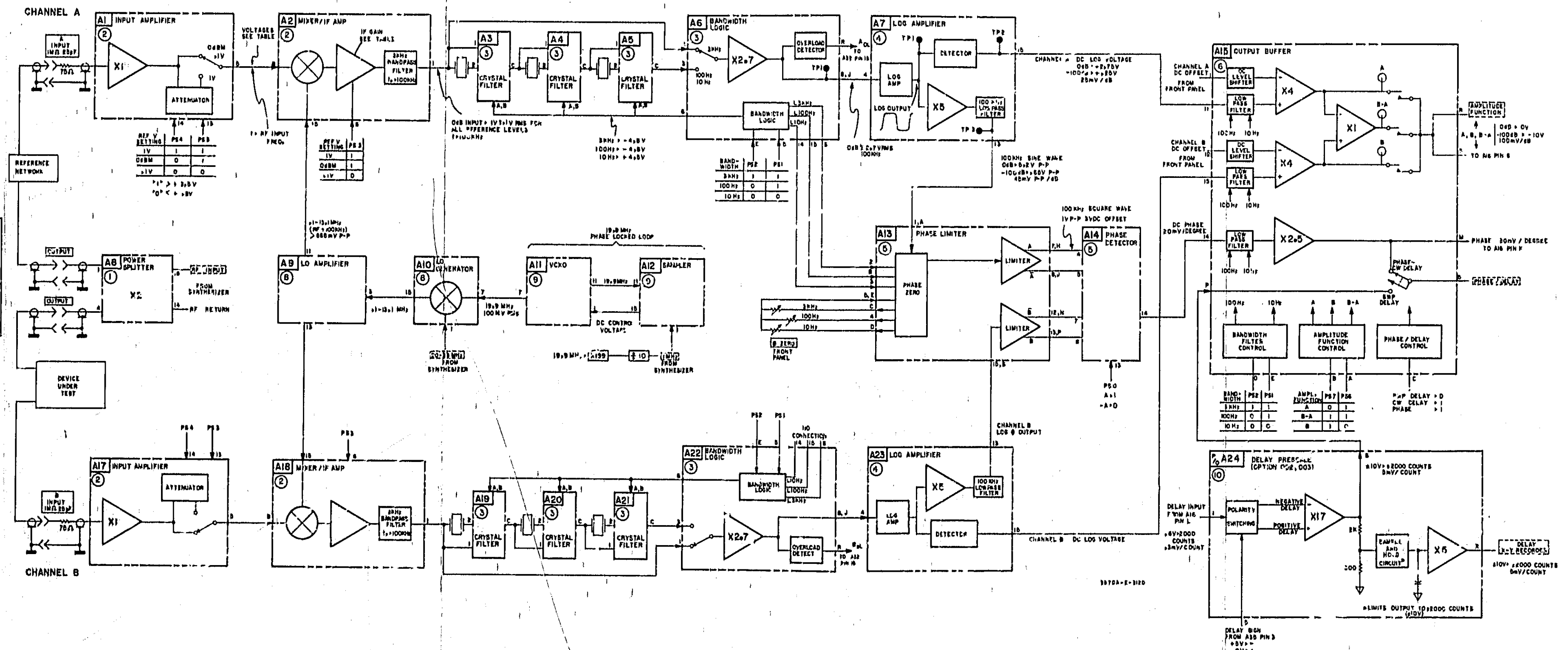
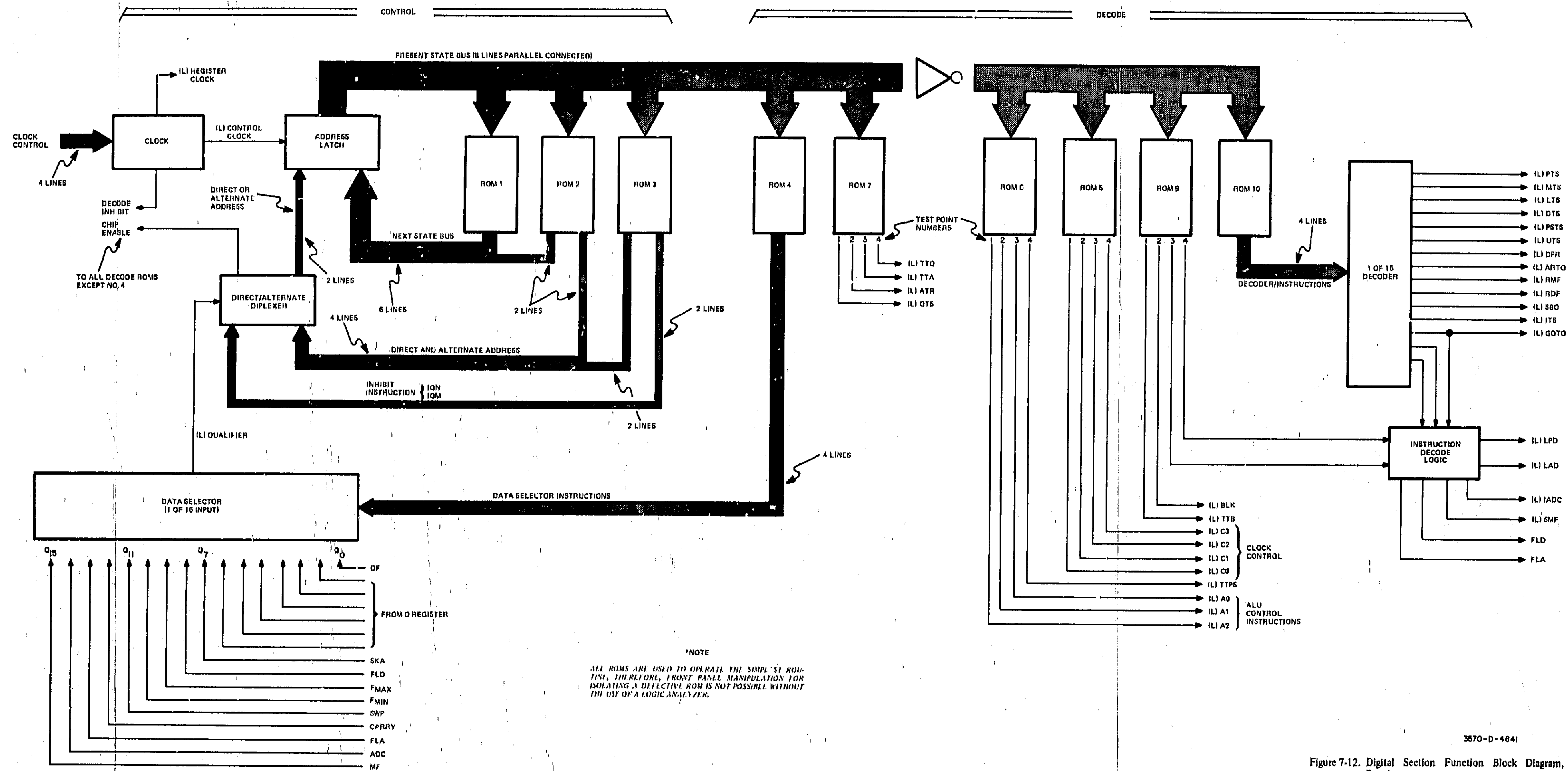


Figure 7-11. Functional Block Diagram (Analog).
7-23/7-24

Table 7-3, Mnemonic Definitions.

I. Register Instructions A. Registers to X Bus 1. DTS Delay (Delay to S Bus) 2. ITS Input 3. ITS Limit 4. MTS Memory 5. PTS Program 6. PSTS Program Storage 7. QTS Qualifier B. Register to R Bus 1. ATR Analog/Digital (Analog/Digital to R Bus) C. T Bus to Registers 1. TTA Analog/Digital (TBus to Analog/Digital) 2. TTB Bidec 3. TTD Delay 4. TTL Limit 5. TTM Memory 6. TTP Program 7. TTPS Program Storage 8. TTQ Qualifier D. Parallel Load Qualifier Register 1. ARTQ (A Register to Q Register) Loads Q register with the eight most significant bits of A register. II. Internal Device Operating Instructions DPR Disable Print. Inhibits markers from being generated at X axis output. BLK Blank Display. Used with phase/delay display in delay mode to indicate that sweeping of the synthesizer has not occurred. GOTO The GOTO instruction when combined with a number (XX) (GOTO XX) parallel loads the P register with the binary equivalent of that number. The number is present on the Register Clock preset lines, but the Register Clock will count only one pulse. IADC Initiate Analog to Digital Conversion. LAD *Latch Amplitude Display LPD *Latch Phase Display *These two commands latch information available in the BIDEc register into the amplitude or phase read-outs. RDF Reset Data Flag. Resets Data Flag after the data input routine is completed.	RMF Reset Measure Flag. Resets Measure Flag after a measurement routine is completed. MF Set Measure Flag. Initiates measurement cycle. TFLA Set Flag Amplitude. Sets flag for an amplitude measurement. TFLD Set Flag Delay. Sets flag for a delay measurement. III. Qualifiers The Qualifiers are numbered according to their input designation on the Data Selector. 0. SKA Skip Amplitude. Causes controller to skip amplitude measurement routine—is used for CW delay measurements. 1. Q1 2. Q2 Qualifiers from the Q register. These qualifiers depend on data which has been shifted into the Q register. 3. Q3 4. Q4 5. Q5 6. Q6 7. DF Data Flag. Signal that data is ready to be processed by the data subroutine. 8. MF Measure Flag. Signals that a measurement request is being made. This can be Auto-Internal or HP-IB Control. 9. ADC Analog Digital Conversion Complete. Signals end of conversion sequence, also used to signal end of data output sequence on HP-IB. 10. FLA Amplitude/Phase Flag. Indicates phase measurement when set, amplitude measurement when cleared. 11. CARRY Indicates overflow or underflow from an ALU operation. 12. SWP Sweep. Indicates 3330B is sweeping, is used in delay measurement routine. 13. FMIN Frequency Minimum. Indicates 3330B minimum sweep position. 14. FMAX Frequency Maximum. Indicates 3330B maximum sweep position. 15. FLD Flag Delay. Indicates delay mode of operation has been selected.
---	--



3570-D-4841

Figure 7-12. Digital Section Function Block Diagram, Part 1.

7-25/7-26

Table 7-4. The Registers.

Registers	
1. I Register (located on A33). The I Register accepts parallel inputs of remote ASCII data when the 3570A is addressed to listen.	5. BIDEDEC (Binary-Decimal) Register (A35). The BIDEDEC Register converts binary to BCD. The BCD reading is available to the Front Panel displays and the ASCII converter.
2. Q Register (located on A28). The Q Register acts as a data handling register since six bits serve as qualifier inputs to the Data Selector. The eight most significant bits of the A Register are parallel loaded into the Q Register in reverse order for output to the BIDEDEC Register.	6. D Register (located on A30, Option 002 or 003). The D Register controls the Delay functions of the instrument.
3. A Register (located on A26). The A Register is used to store the binary result of an A/D conversion and/or the calculated result in the Relative or Delay mode.	7. L Register (located on A30, Option 002 or 003). The L Register controls limit testing and offset functions and also stores the Limit Test decision.
4. Program Storage (PS) Register (located on A33). The PS Register controls the basic instrument functions in the analog function.	8. Memory (located on A31). The Memory contains eight sixteen bit words for storing limits, offsets, or previous phase or delay computations.
	9. P Register (located on A31). The P Register selects the specific memory location (0-7) to be connected to the S Bus and/or the T Bus. The P Register can also be used to generate an arbitrary constant (0-15) for use in computations by the ALU.

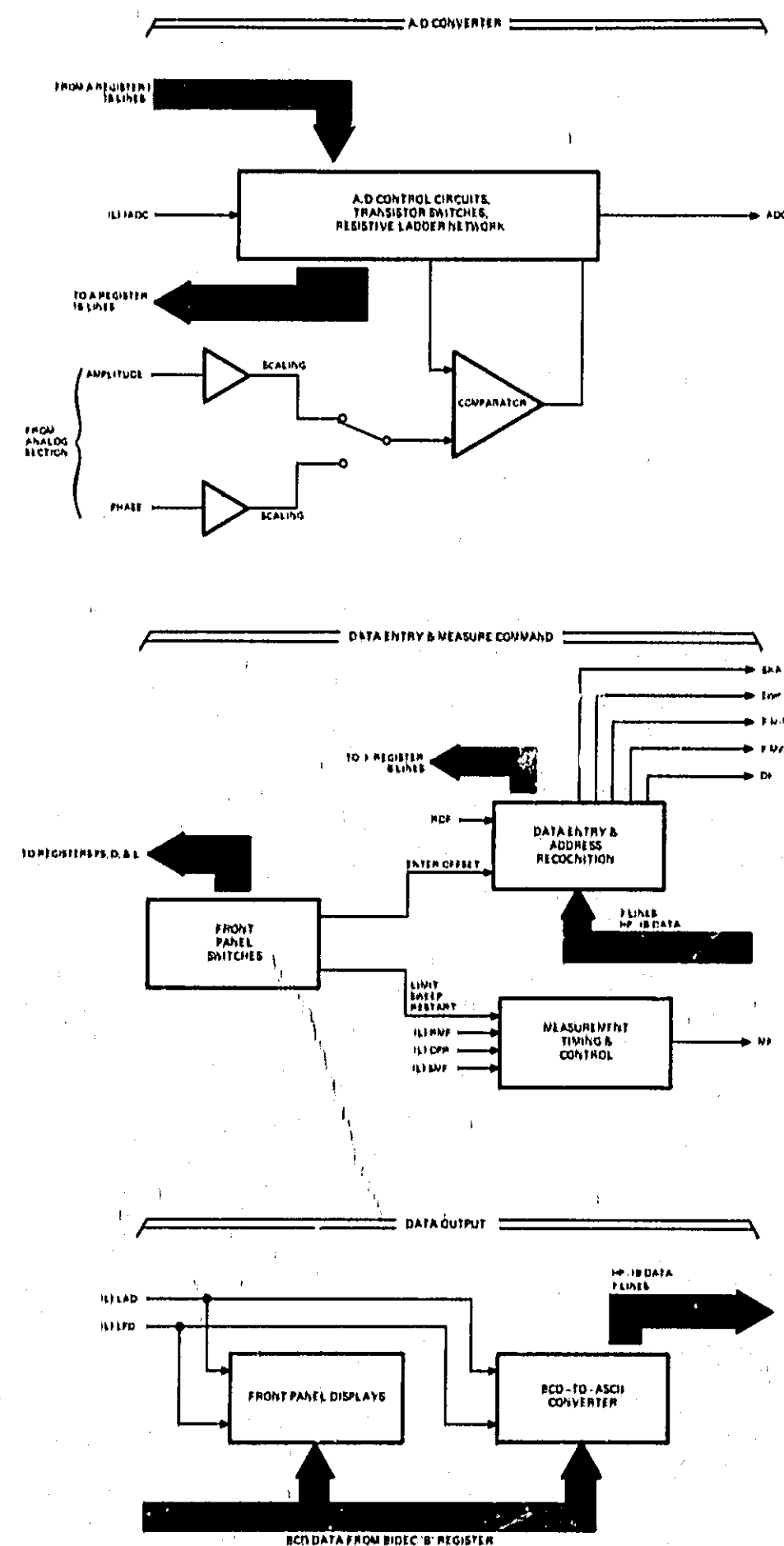
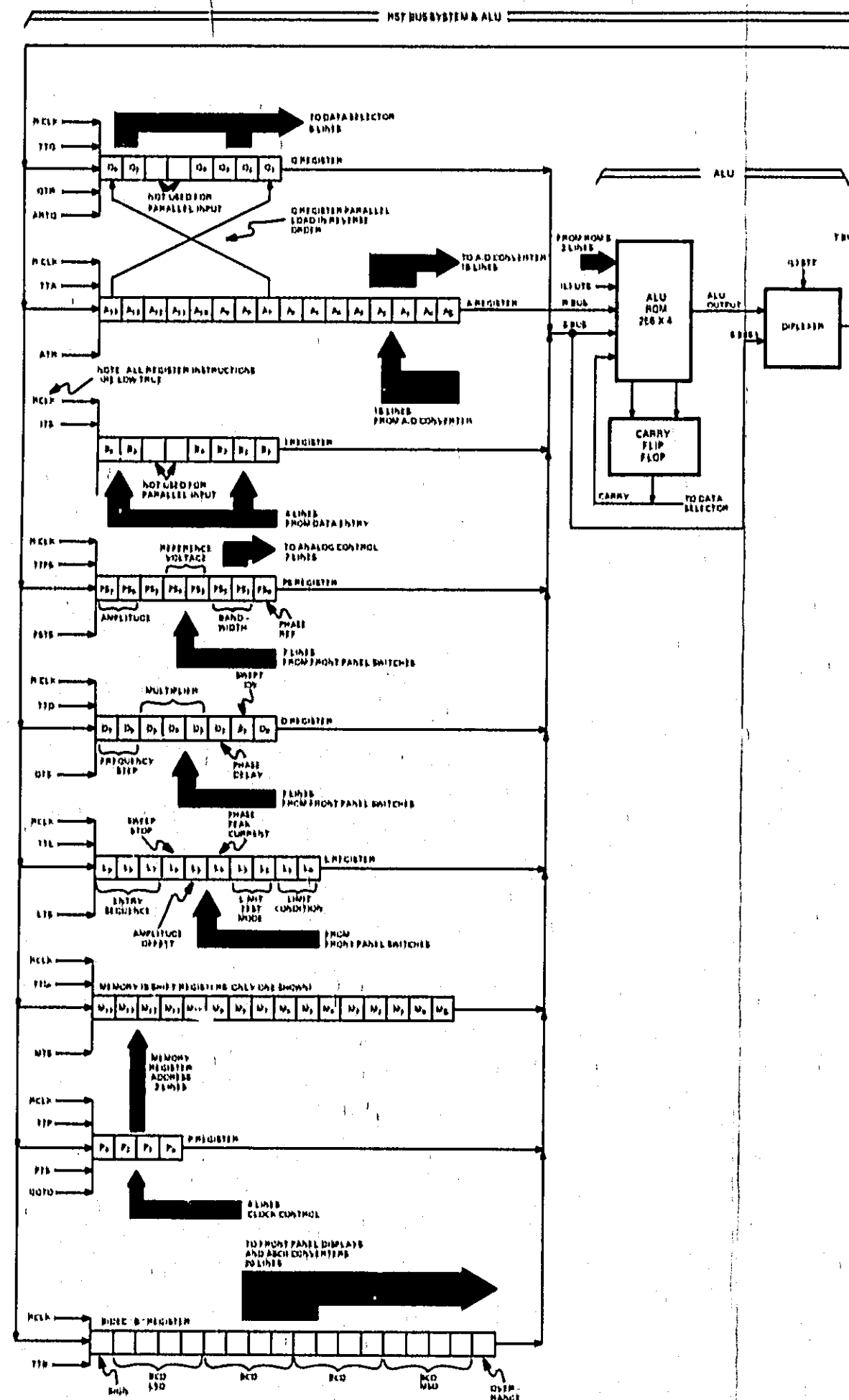


Figure 7-13. Digital Section Functional Block Diagram, Part II.

7-27/7-28

NOTE
To troubleshoot basic measurement routine verify the following instrument conditions:
a. Instrument in local mode of operation.
b. No offsets entered.
c. Phase/delay mode switch to phase.

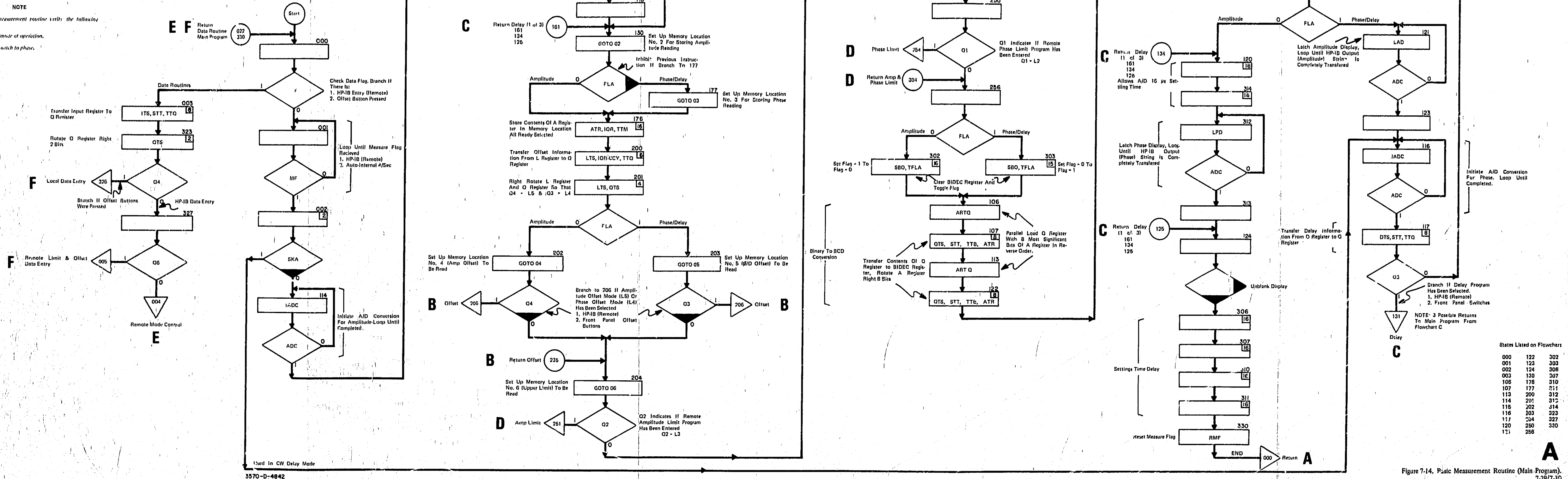


Figure 7-14. Basic Measurement Routine (Main Program).
7-29/7-30

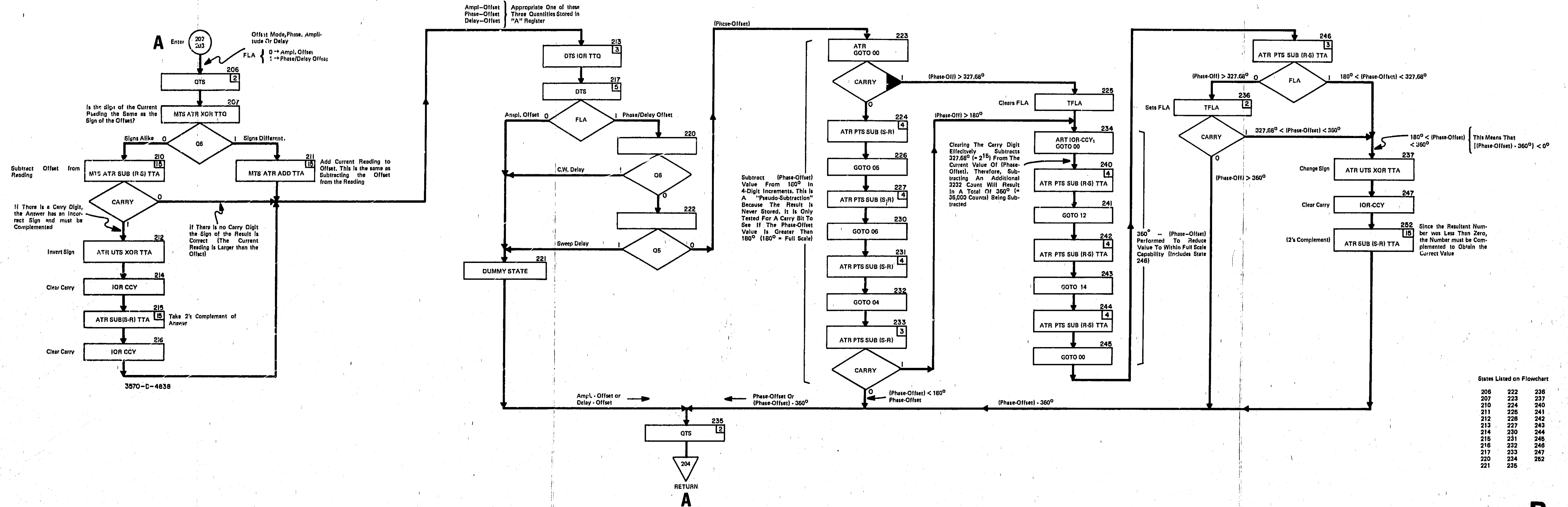
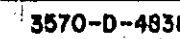


Figure 7-15. Offset Subroutine.
7-31/7-32

2. To Solve The Delay Equation For 10 Hz And 20 Hz, The 5 Hz Prescale (K) Is Used. The Dependent Variable (T) Is Divided By 2 For 10 Hz And Divided By 2 Again For 20 Hz.

C

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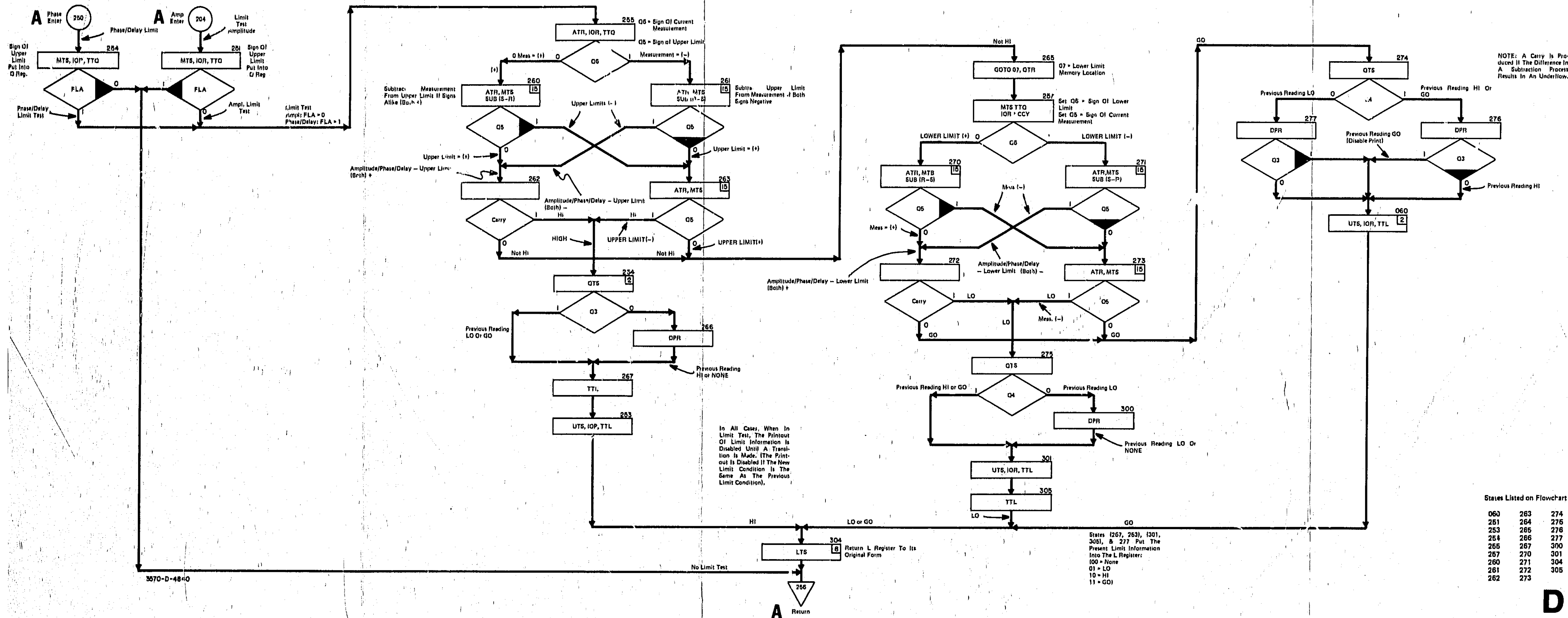
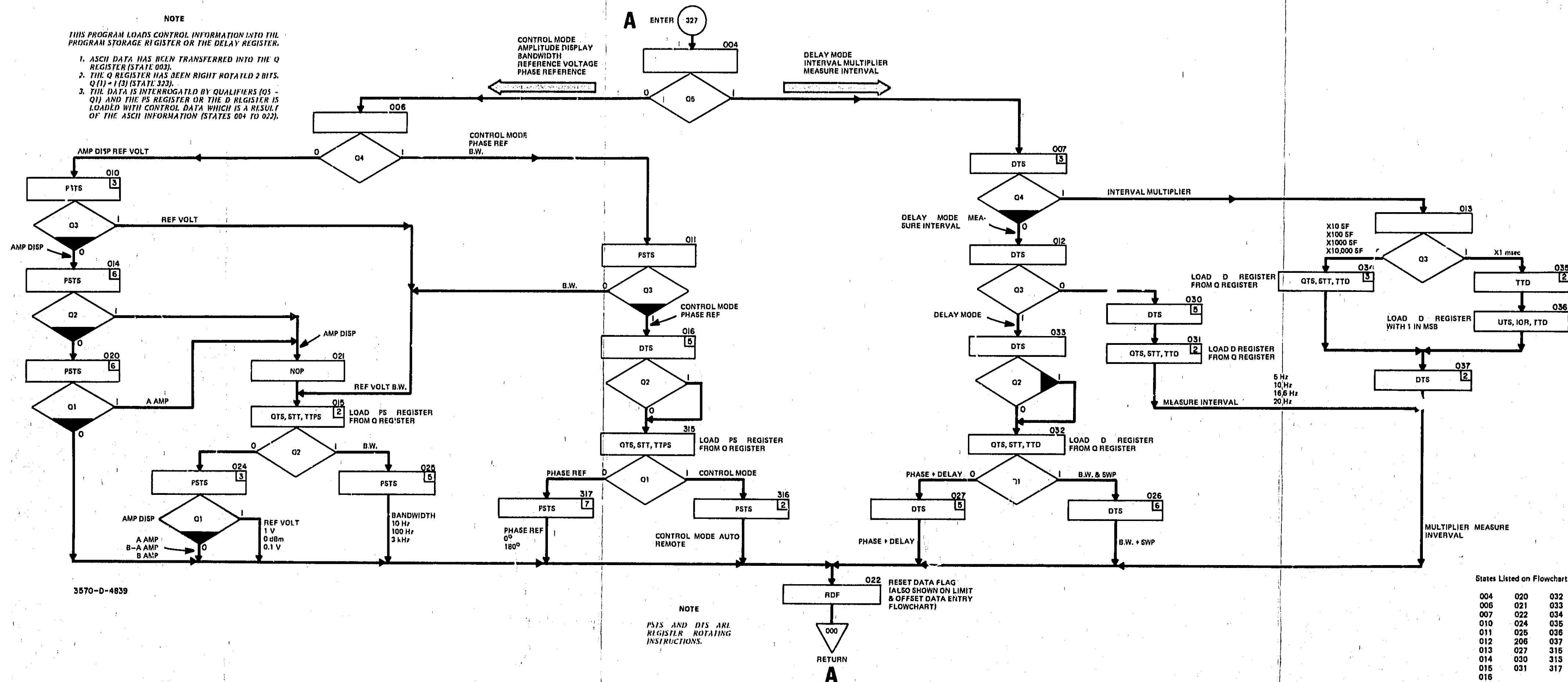


Figure 7-17, Limit Test Subroutine, 7-35/7-36

NOTE
THIS PROGRAM LOADS CONTROL INFORMATION INTO THE PROGRAM STORAGE REGISTER OR THE DELAY REGISTER.

1. ASCII DATA HAS BEEN TRANSFERRED INTO THE Q REGISTER (STATE 003).
2. THE Q REGISTER HAS BEEN RIGHT ROTATED 2 BITS. Q(1) = 1(3) (STATE 323).
3. THE DATA IS INTERROGATED BY QUALIFIERS (Q5 - Q1) AND THE PS REGISTER OR THE D REGISTER IS LOADED WITH CONTROL DATA WHICH IS A RESULT OF THE ASCII INFORMATION (STATES 004 TO 022).



States Listed on Flowchart

004	020	032
006	021	033
007	022	034
010	024	035
011	025	036
012	026	037
013	027	315
014	030	313
015	031	317
016		

Figure 7-18. Basic and Delay Data Entry Subroutine.
7-37/7-38

NOTE 1
THE OVERALL PROCEDURE INVOLVING THIS BRANCH OF THE SUBROUTINE IS AS FOLLOWS:

1. ASCII BUS DATA WAS PARALLEL LOADED INTO THE INPUT REGISTER.
2. THE INPUT REGISTER WAS SHIFTED INTO THE Q REGISTER, STATE 003.
3. THE Q REGISTER WAS RIGHT ROTATED 2 BITS, STATE 323 (Q(1) = 1(3)).
4. THE ASCII DATA IS INTERROGATED IN THE Q REGISTER BY USE OF QUALIFIERS (Q4 TO Q1) AND THE L REGISTER IS SET UP SO THAT IT WILL CONTAIN THE CORRECT MODE OPERATING INFORMATION, STATES 040 TO 054.

- NOTE 2
1. ASCII DATA IS IN Q REGISTER.
 2. QUALIFIERS Q4 TO Q1 USED TO INTERROGATE ASCII DATA.
 3. ASCII DATA IS CONVERTED INTO BINARY AND USED TO SET UP MEMORY (FIRST TIME THROUGH). IT THEN STORES NUMERICS IN THE MEMORY LOCATION AS THEY ARE ENTERED BY THE HP1B.

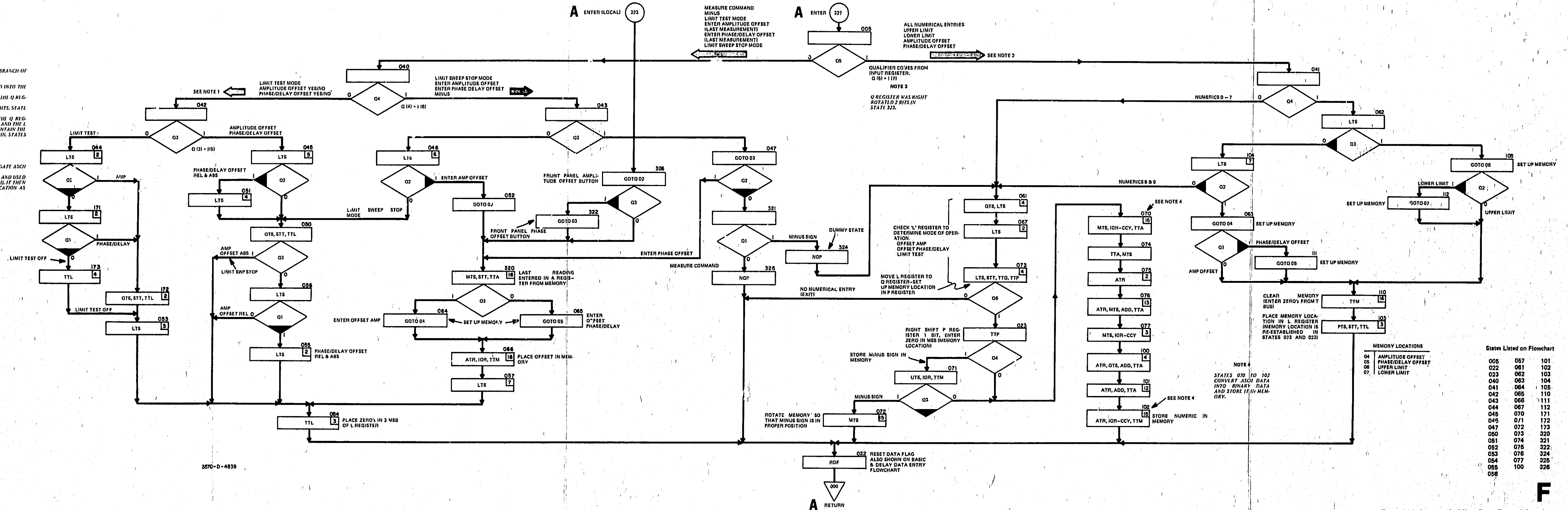


Figure 7-19. Limit and Offset Data Entry Subroutine.
7-39/7-40

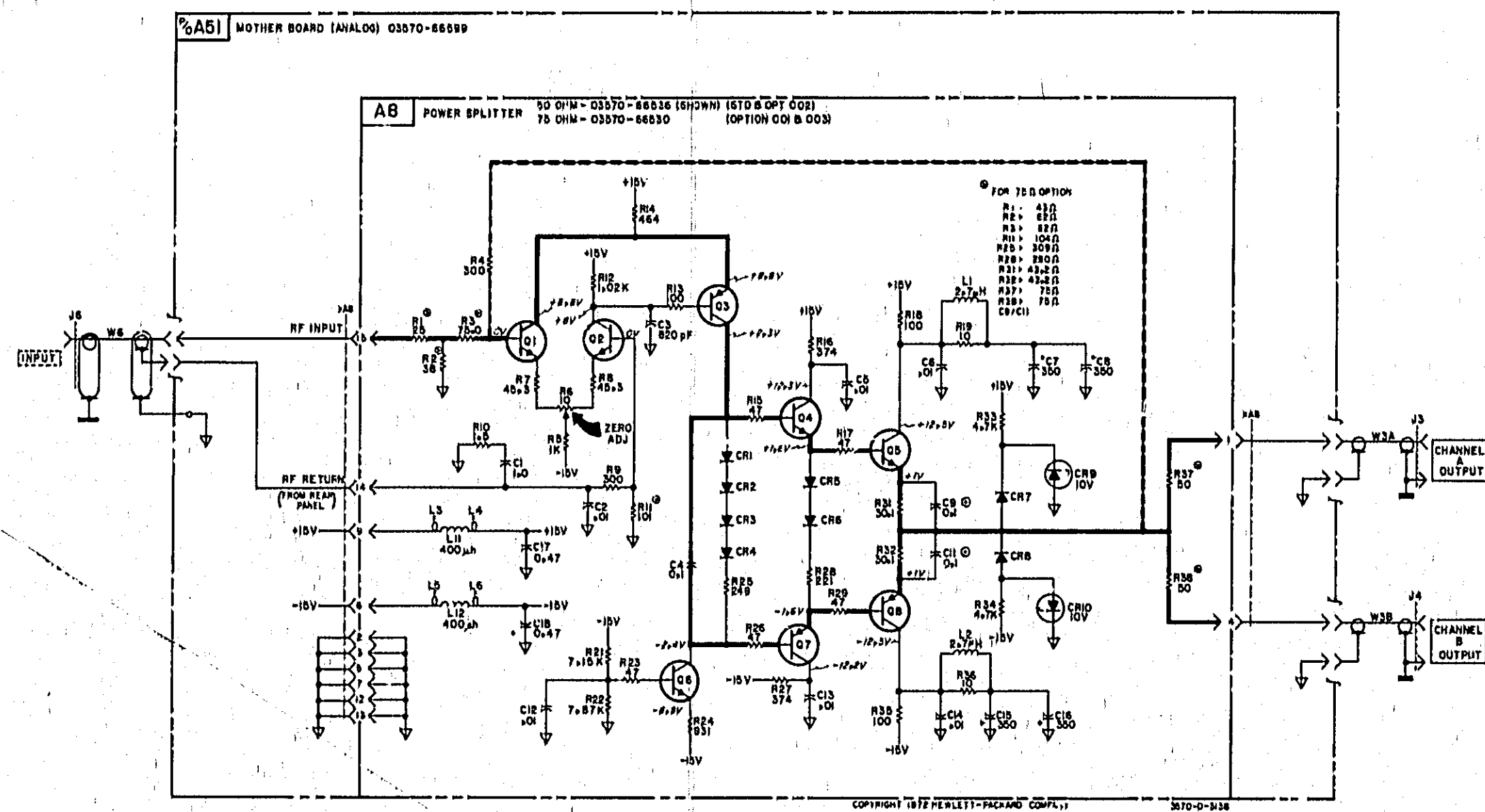
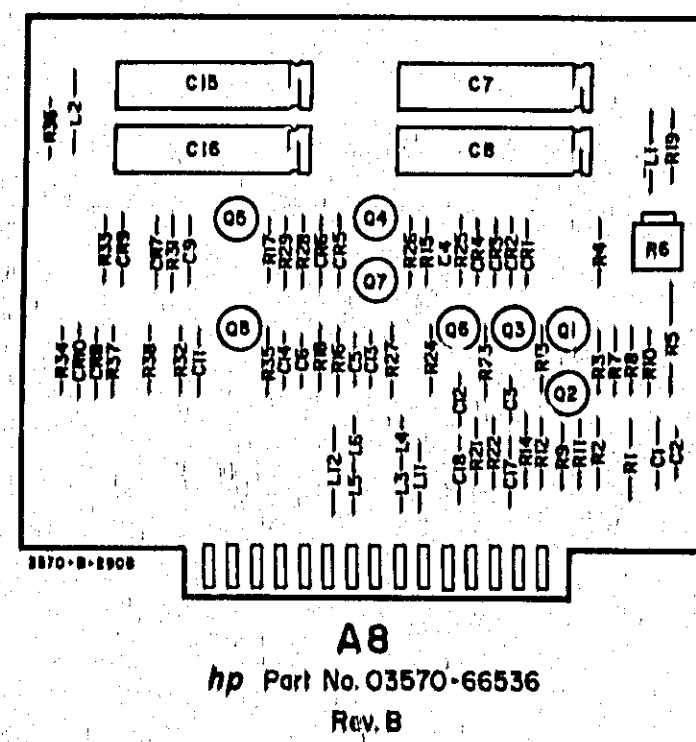


Figure 7-20. Power Splitter (A8) Schematic and Component Location Diagram.

7-41/7-42

NOTE 1

C4 IS USED FOR AMPLITUDE AND PHASE FLATNESS,

NOTE 2

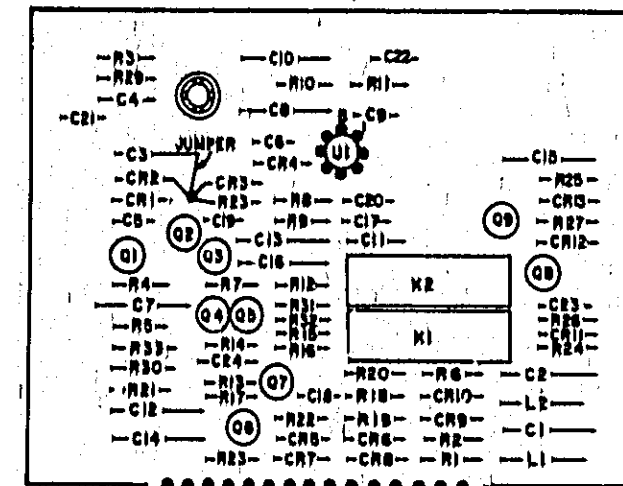
WHEN USING AN INTERNALLY COMPENSATED OP AMP FOR U1 SUCH AS 741 OR LM307, C9 IS NOT NEEDED. WHEN USING AN OP AMP THAT IS NOT INTERNALLY COMPENSATED SUCH AS LM301, C9 (100pF) MUST BE INSTALLED.

NOTE 3

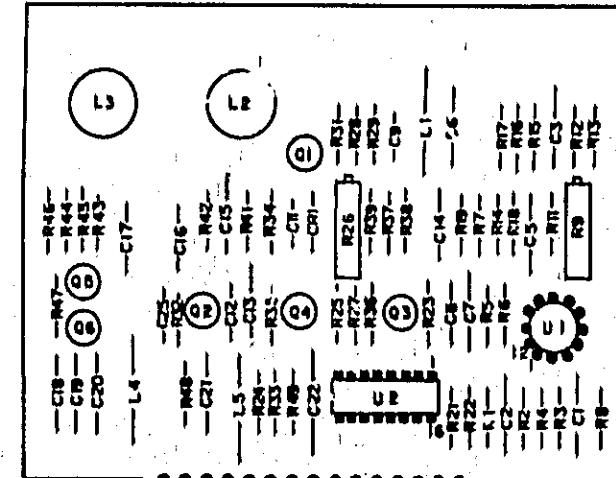
FOR 75 Ω OPTION, R13 = 383 Ω

NOTE 4

FOR 75 Ω OPTION, R35 = 2.74 K,
R36 = 1.33 K.



hp Part No. 03570-66551 (50 ohms) Rev. A
03570-66556 (75 ohms) Rev. A



hp Part No. 03570-66532 (50 ohms) Rev. B
03570-66529 (75 ohms) Rev. A

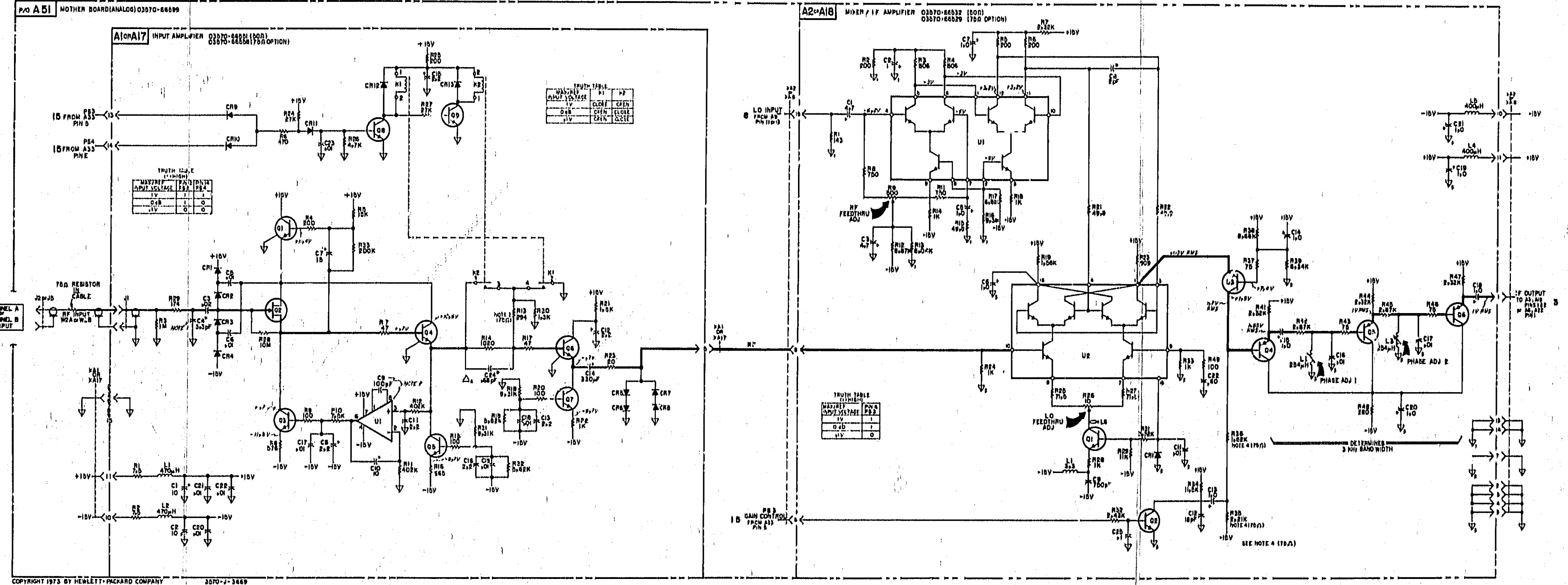
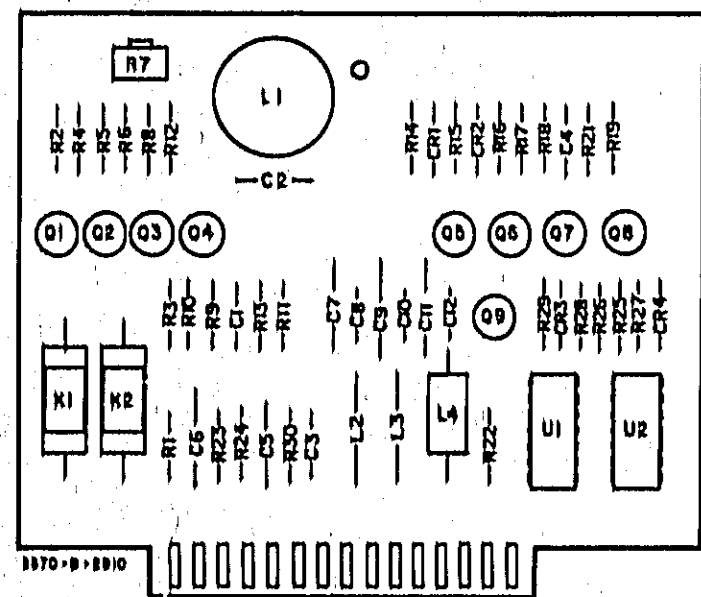
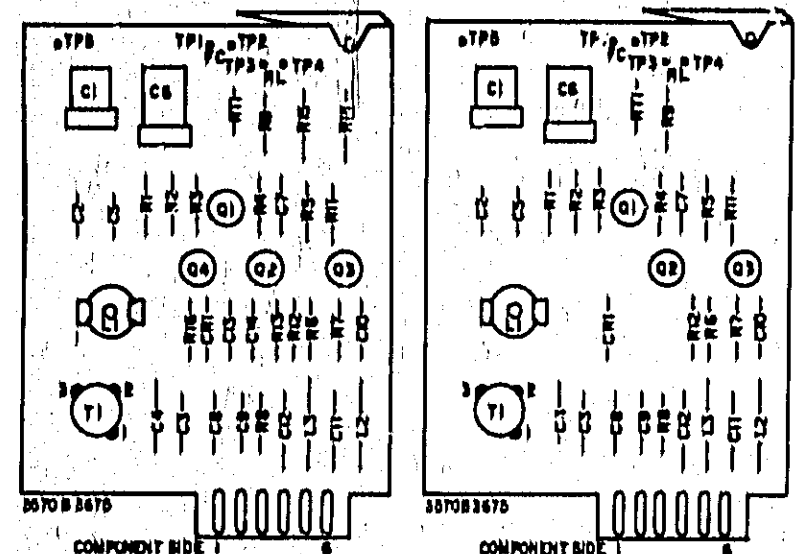


Figure 7-21. Input Amplifier (A1/A17) and Input Mixer (A2/A18) Schematics and Component Location Diagrams.



A6 and A22
hp Part No. 03570-66534
Rev. B



A5 and A21
hp Part No. 03570-66553
REV B

A3, A4, A19, A20
hp Part No. 03570-66553
REV B

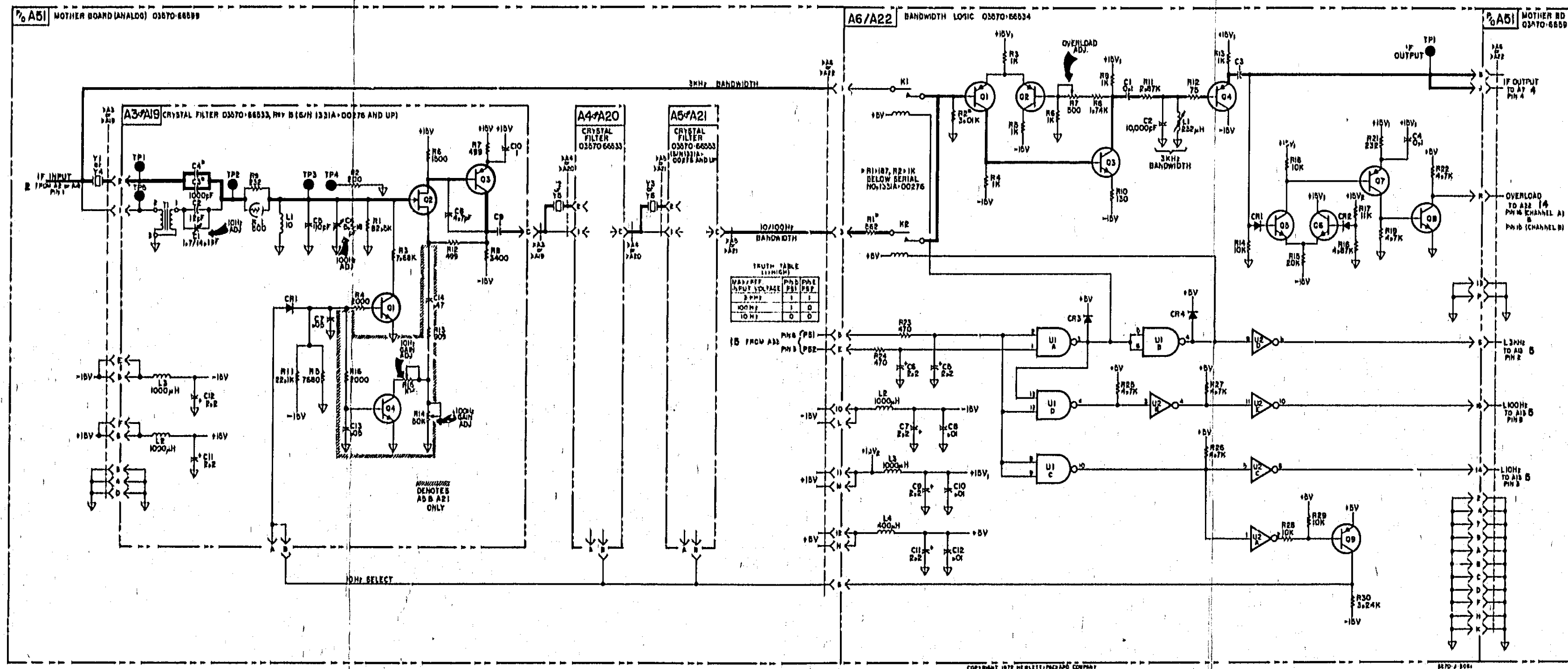


Figure 7-22, Crystal Filter (A3, A4, A5/A19, A20, A21) and Bandwidth Logic (A6/A22) Schematics and Component Location Diagrams.

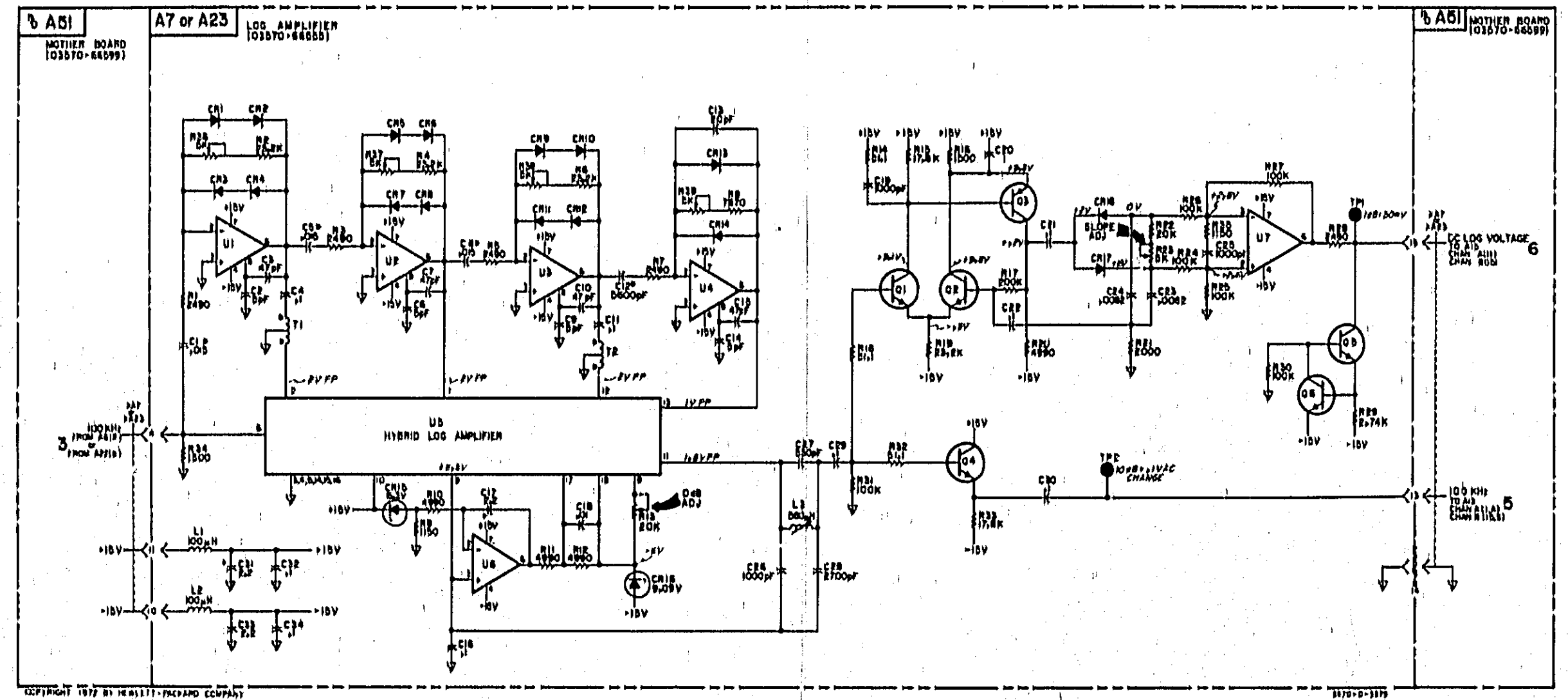
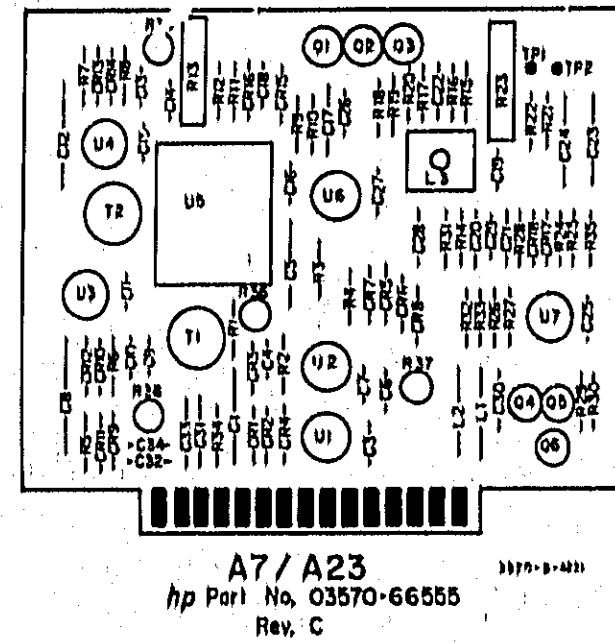
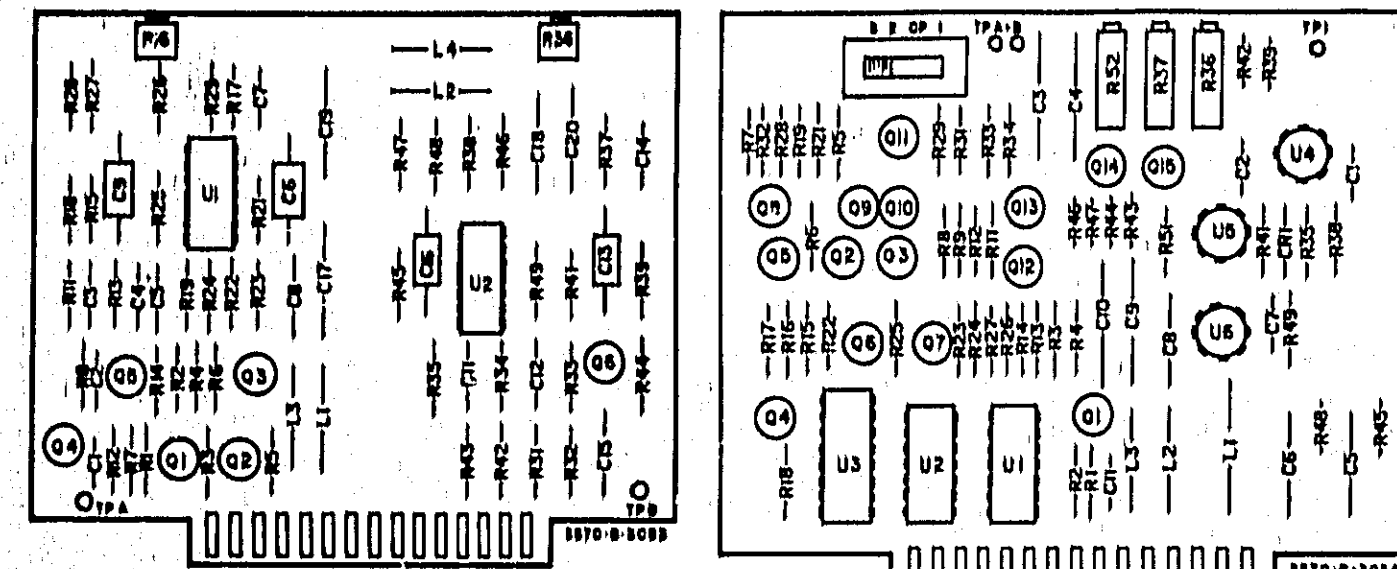
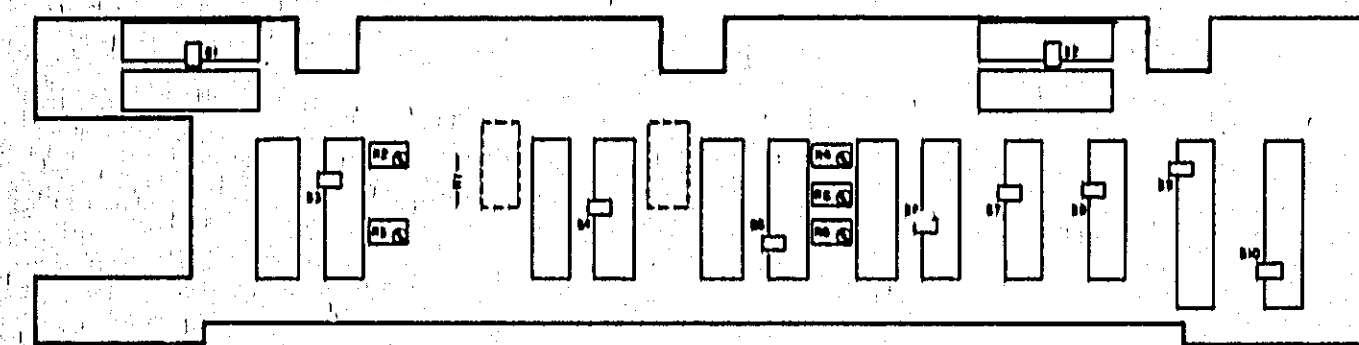


Figure 7-23. Log Amplifier (A7/A23) Schematic and Component Location Diagram.

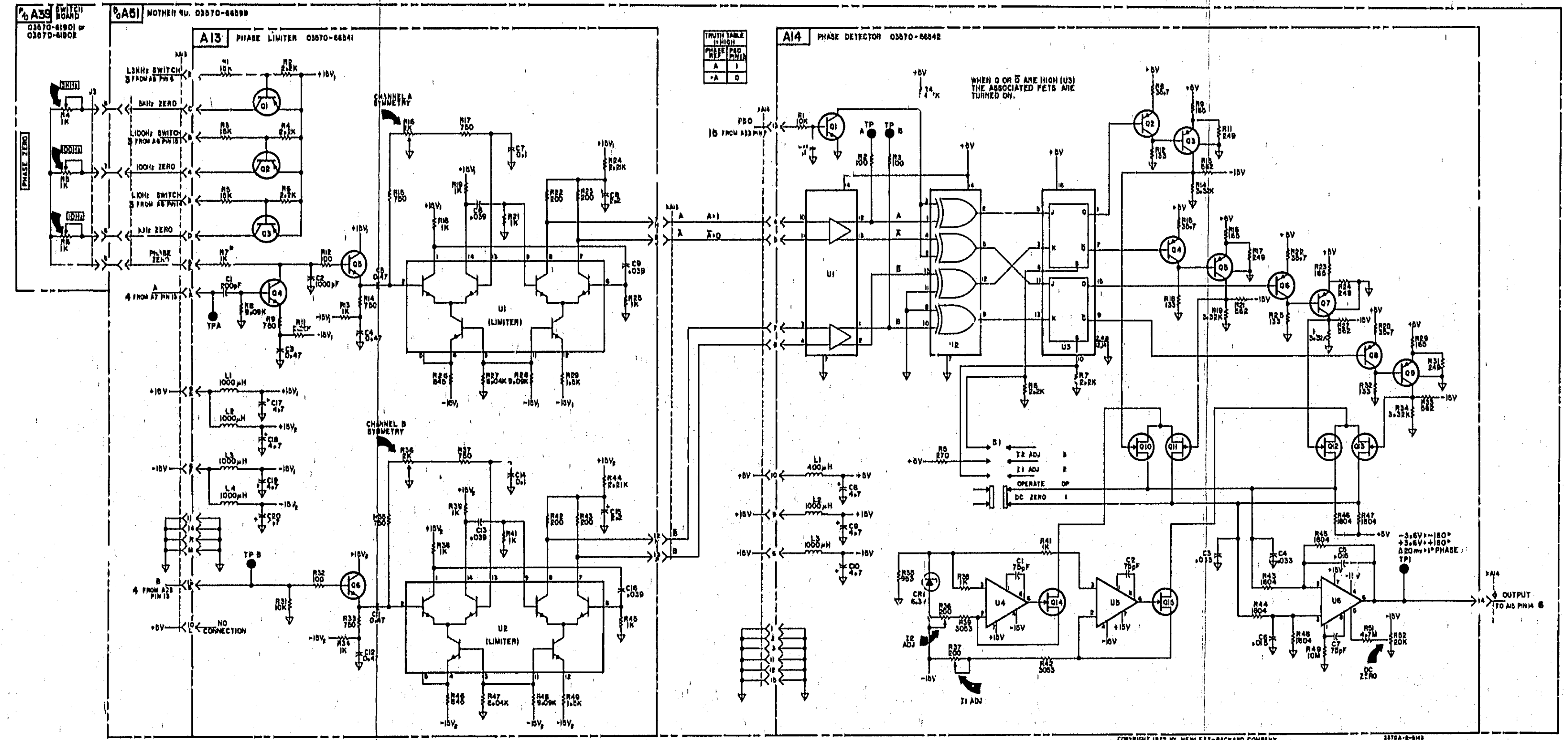


A13
hp Part No. 03570-66541
Rev. A

A14
hp Part No. 03570-66542
Rev. A



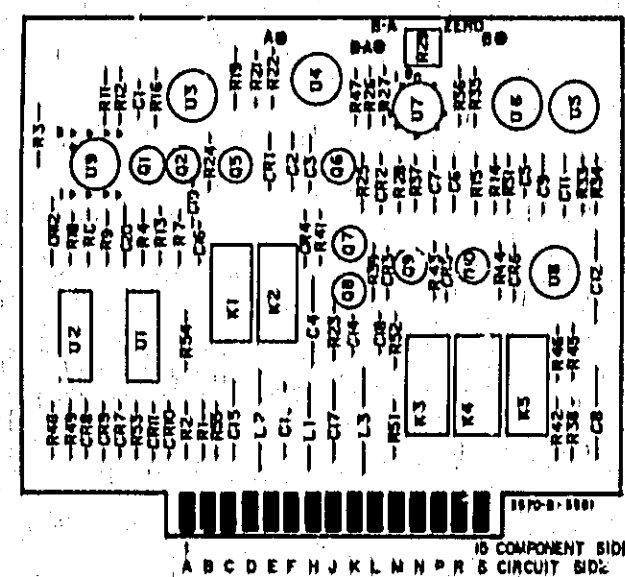
A39
hp Part No. 03570-61901
or 03570-61902 (SHOWN)
Rev. A



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3570A-B-5H43

5
Figure 7-24. Phase Limiter (A13), Phase Detector (A14) and P/O Front Panel Switch (A39) Schematics and Component Location Diagrams.
7-49/7-50

Bandwidth	PS1	PS2	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
10 Hz	0	0	0	0	1	1	1	0	1	0	1	0
100 Hz	1	0	1	1	0	0	0	1	0	1	0	1
3 kHz	1	1	1	1	1	0	0	0	0	0	0	1
"1" = High; "0" = Low			"1" = ON; "0" = OFF									



A15
hp Part No. 03570-66556
Rev A

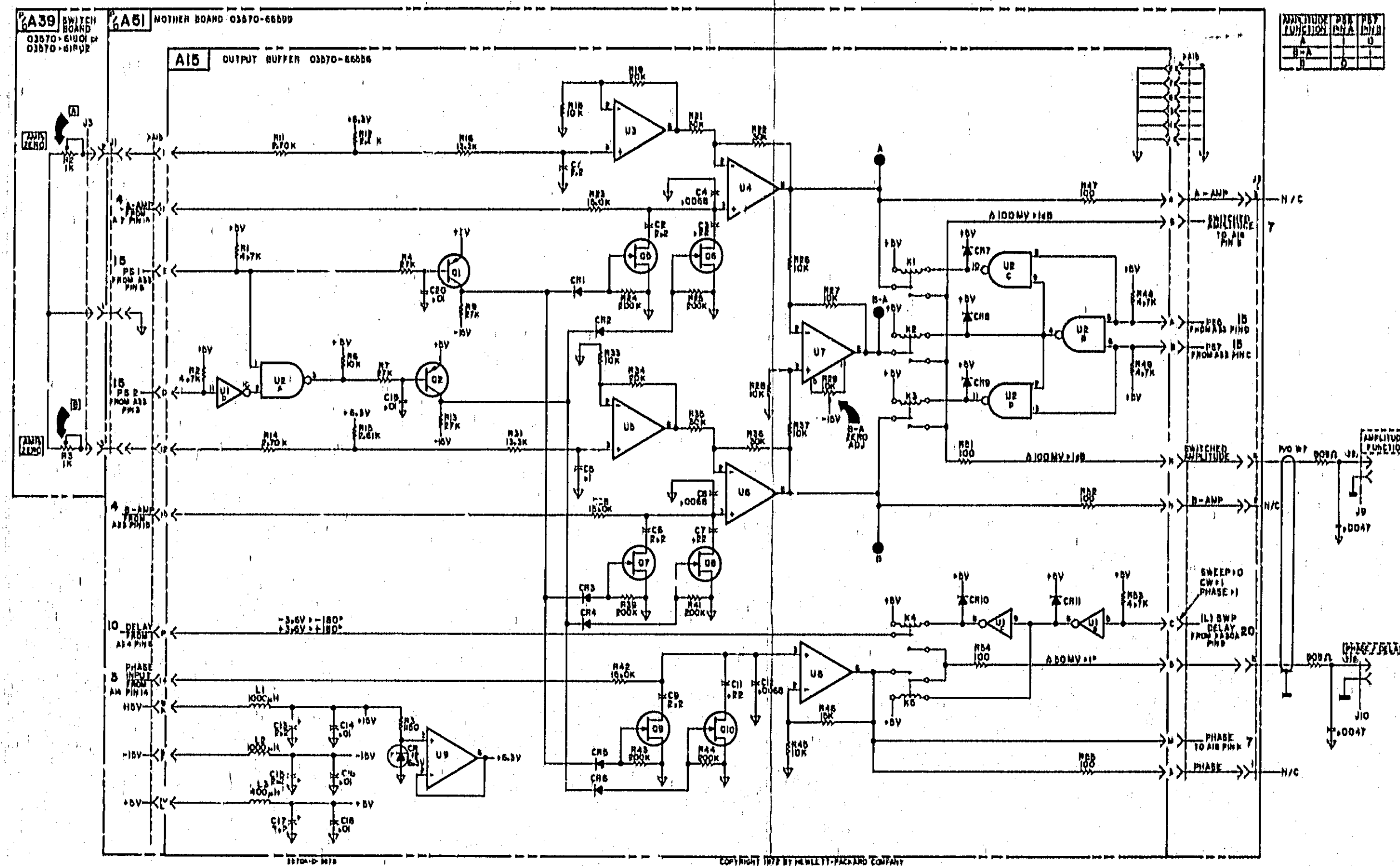


Figure 7-25. Output Buffer (A15) and P/O Front Panel Switch (A39) Schematics and Component Location Diagrams.

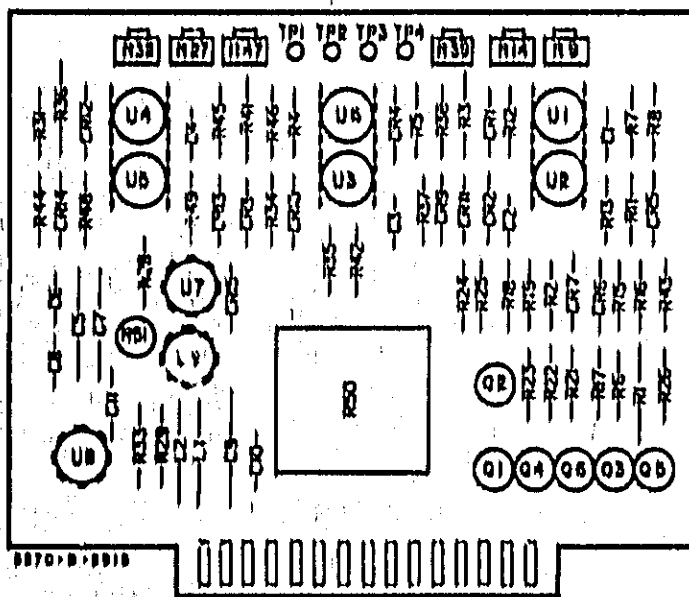
7-51/7-52

NOTE 1

MATCHED PAIR (MUST BE WITHIN 1 %),

NOTE 2

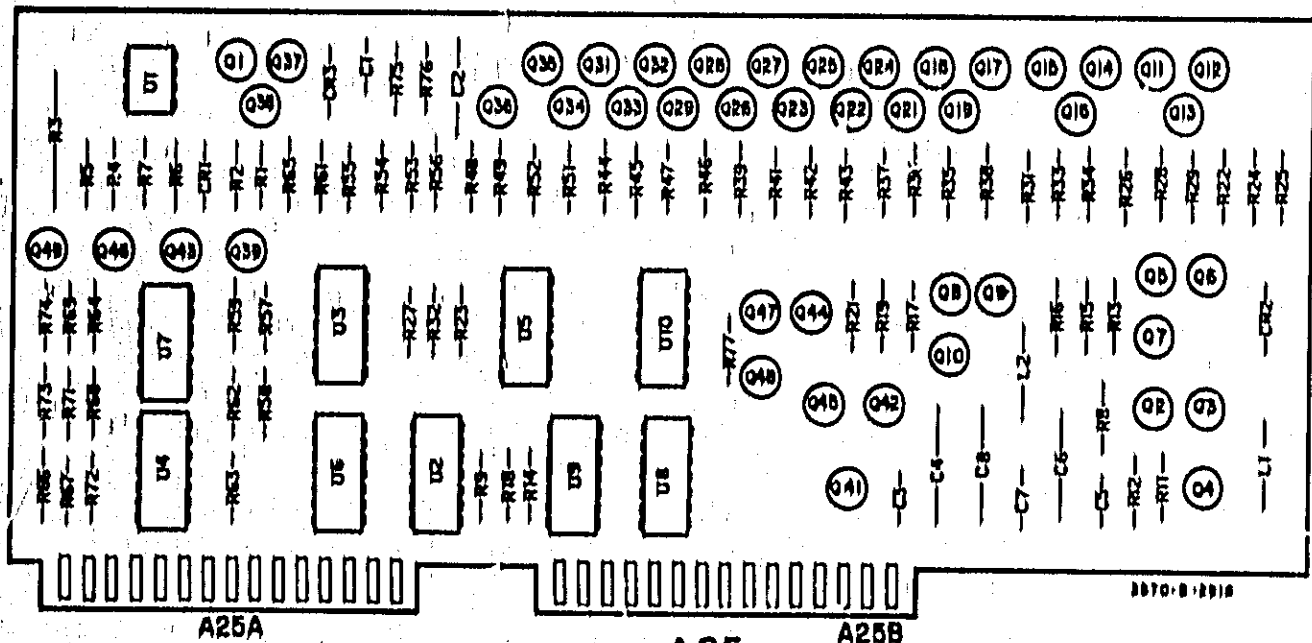
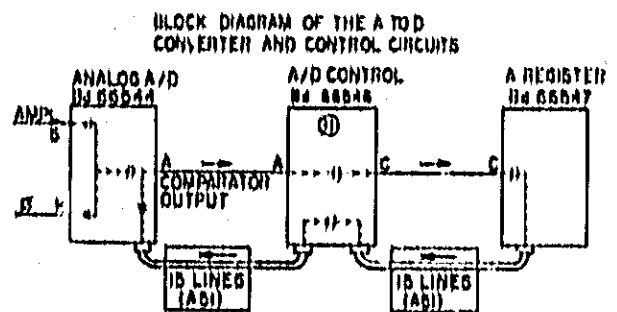
IF THE PHASE LINEARITY IS BAD OR THE FRONT PANEL AMPLITUDE ZERO ADJUST IS WIDE, CHANGE R60 WHEN THE TROUBLE HAS BEEN ISOLATED TO A16,



A16

hp Part No. 03570-66544

Rev. 0



A25

hp Part No. 03570-66546

Rev. B

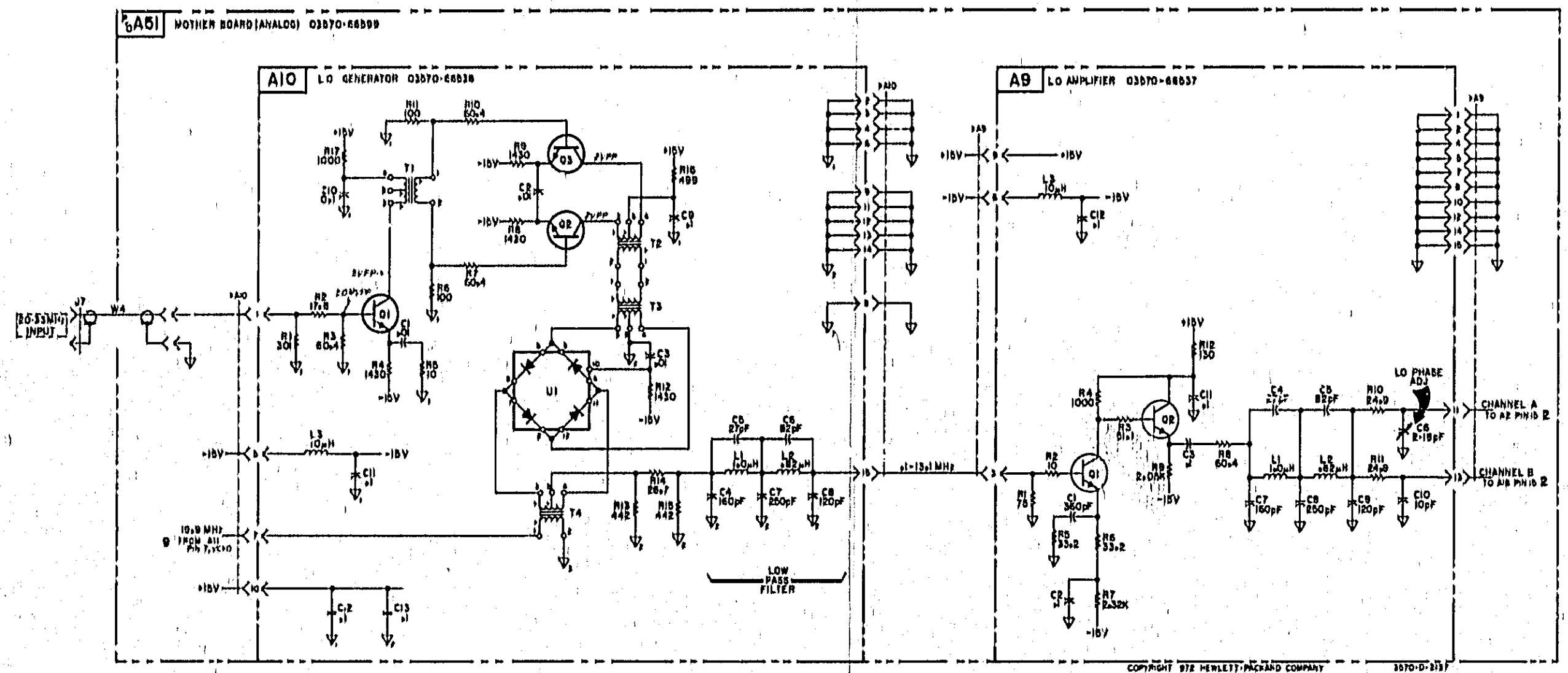
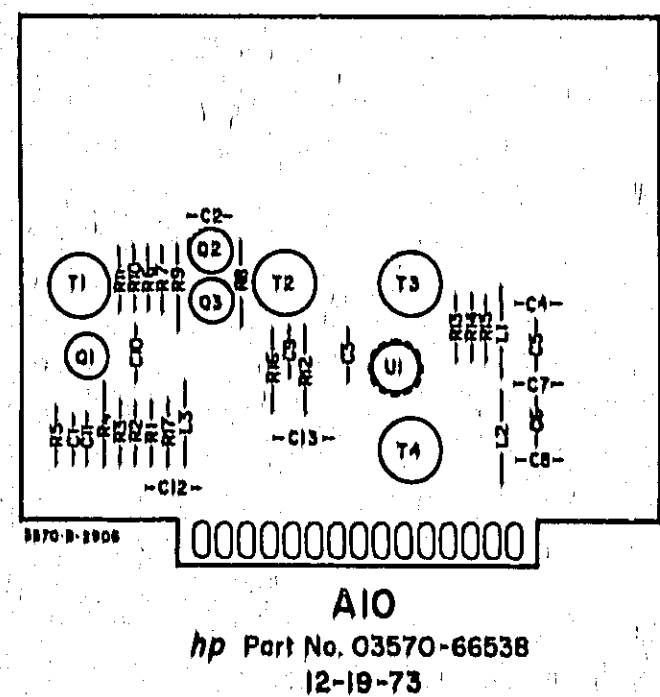
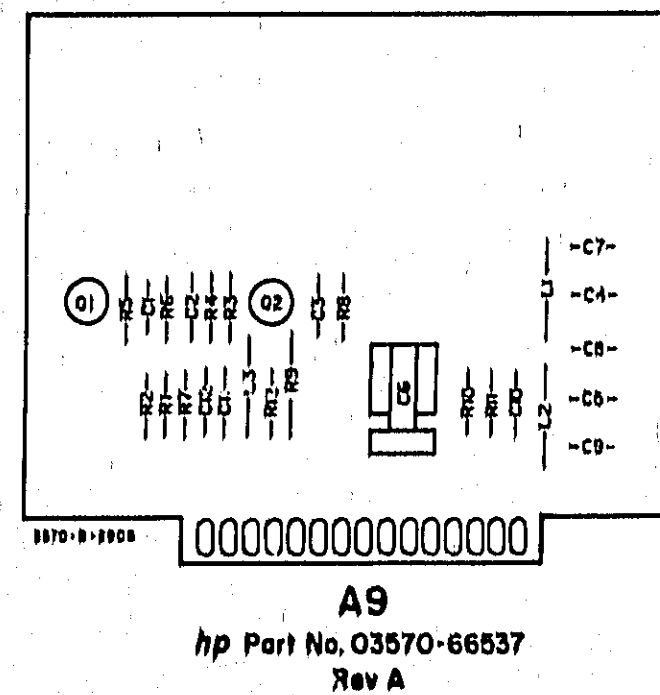
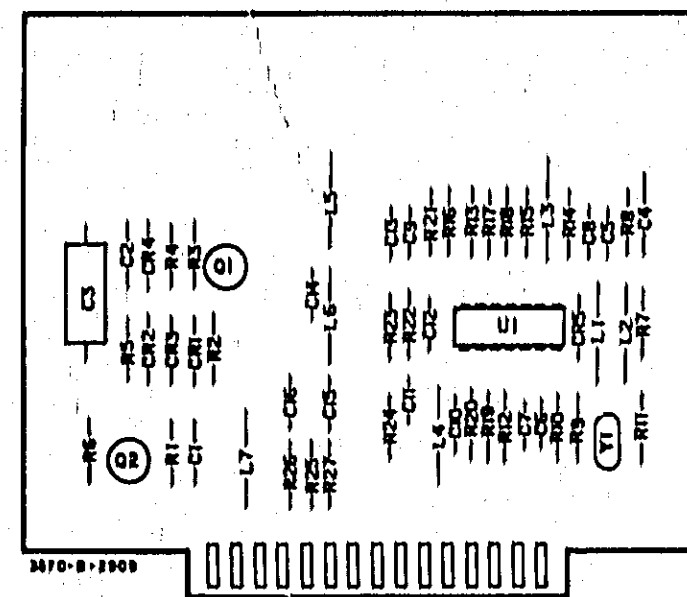
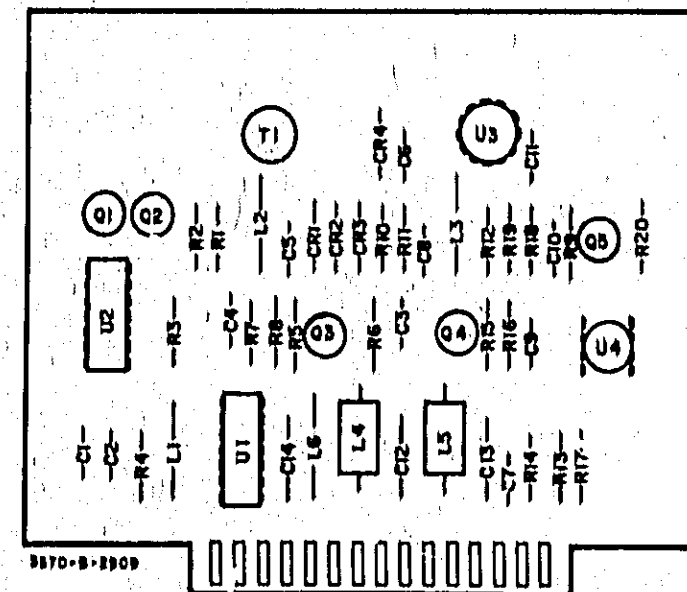


Figure 7-27. L.O. Buffer (A9) and L.O. Generator (A10) Schematics and Component Location Diagrams.



A11
hp Part No. 03570-66539
Rev. A



A12
hp Part No. 03570-66540
Rev. A

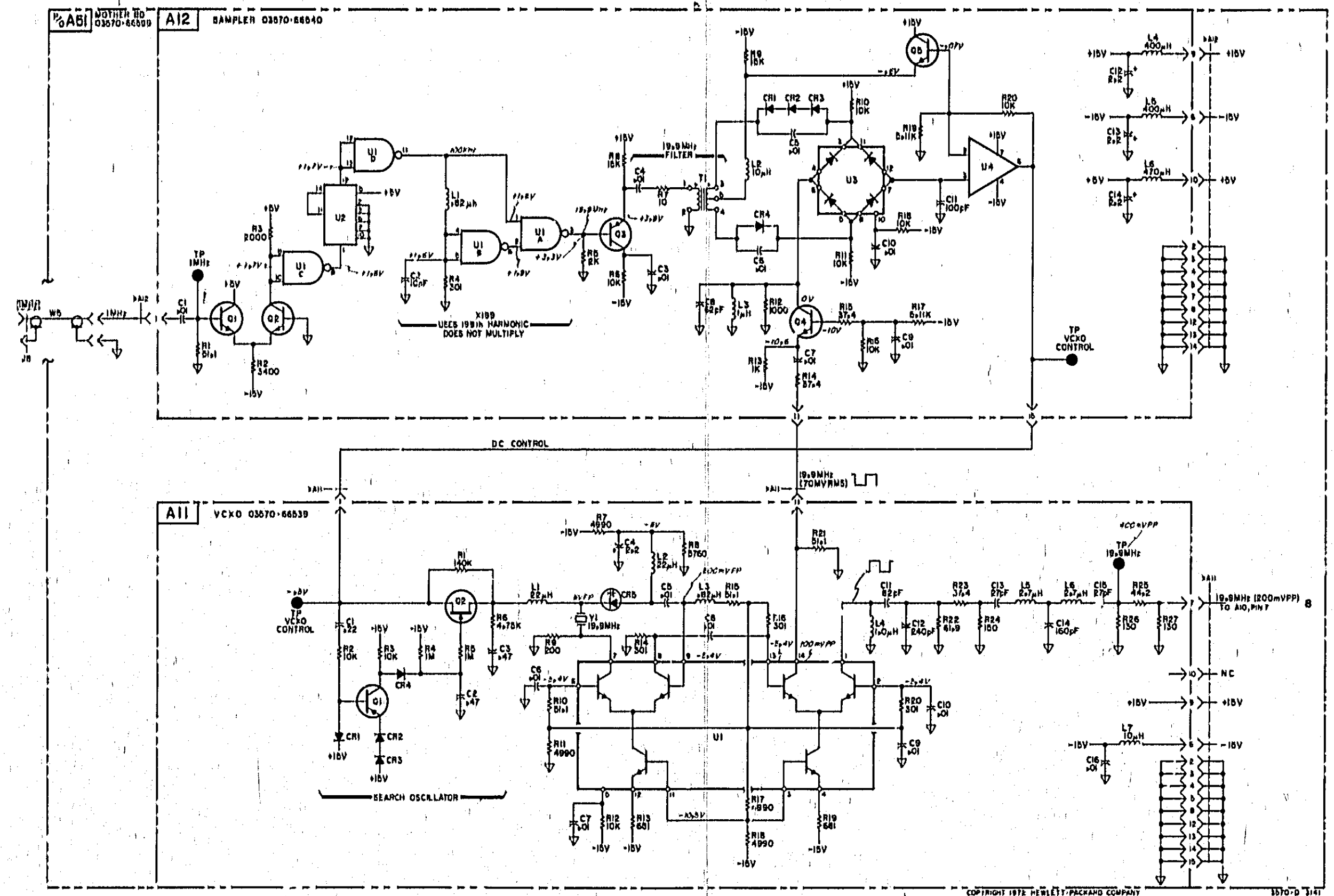


Figure 7-28. VCXO (A11) and Sampler (A12) Schematics and Component Location Diagrams.

7-57/7-58

NOTE 1
PULSES MUST EQUAL 5 V P-P, IF NOT, REPLACE U5.

NOTE 2
SHORTING U5 PIN 4 TO GROUND CAUSES THE FRONT PANEL READINGS (AMPLITUDE AND PHASE) TO GO TO 127.57. SHORTING U5 PIN 1 TO GROUND CAUSES THE FRONT PANEL READINGS (AMPLITUDE AND PHASE) TO GO TO ALL ZEROS.

NOTE 3
TO CHECK U22, SYNC THE SCOPE TO CHANNEL B, CONNECT CHANNEL B TO U22 PIN 4, CONNECT CHANNEL A TO PINS 1 THROUGH 16 IN SUCCESSION. THE SCOPE PICTURE WILL BE AS FOLLOWS:

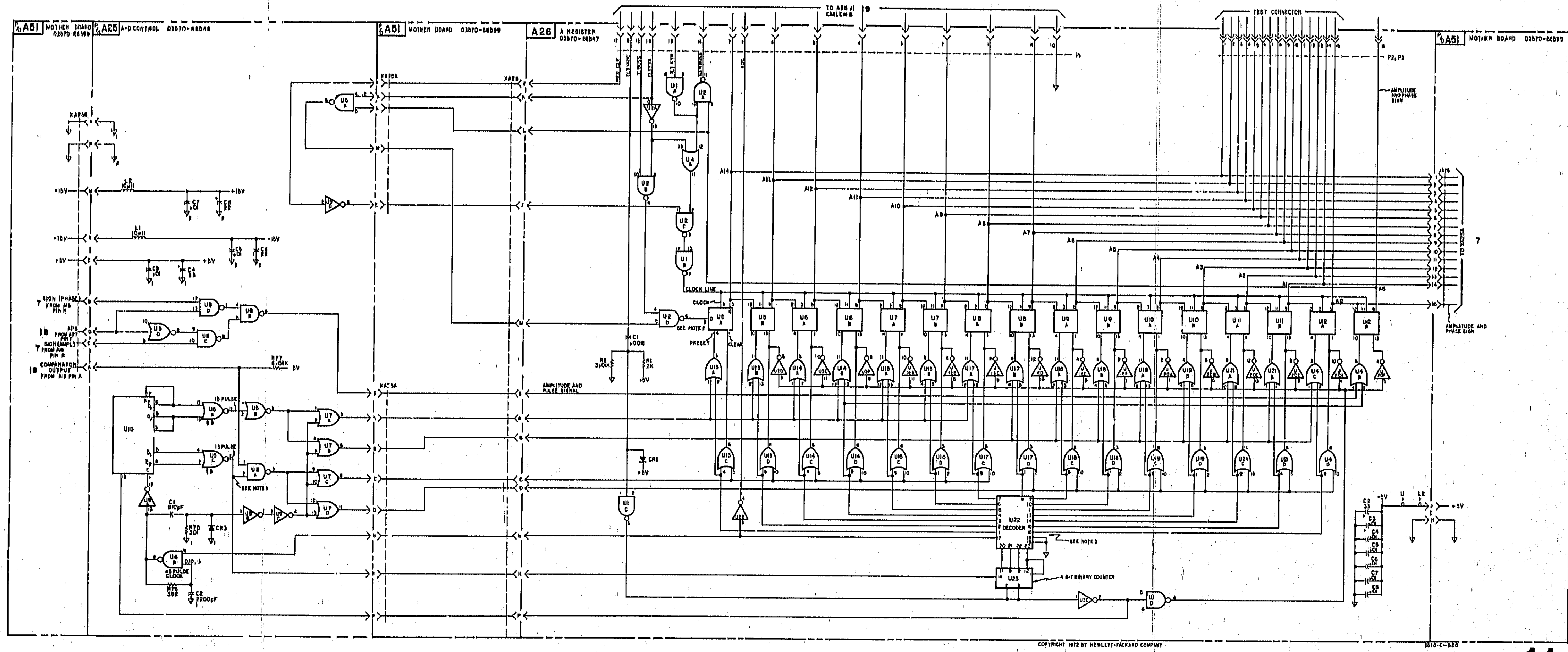
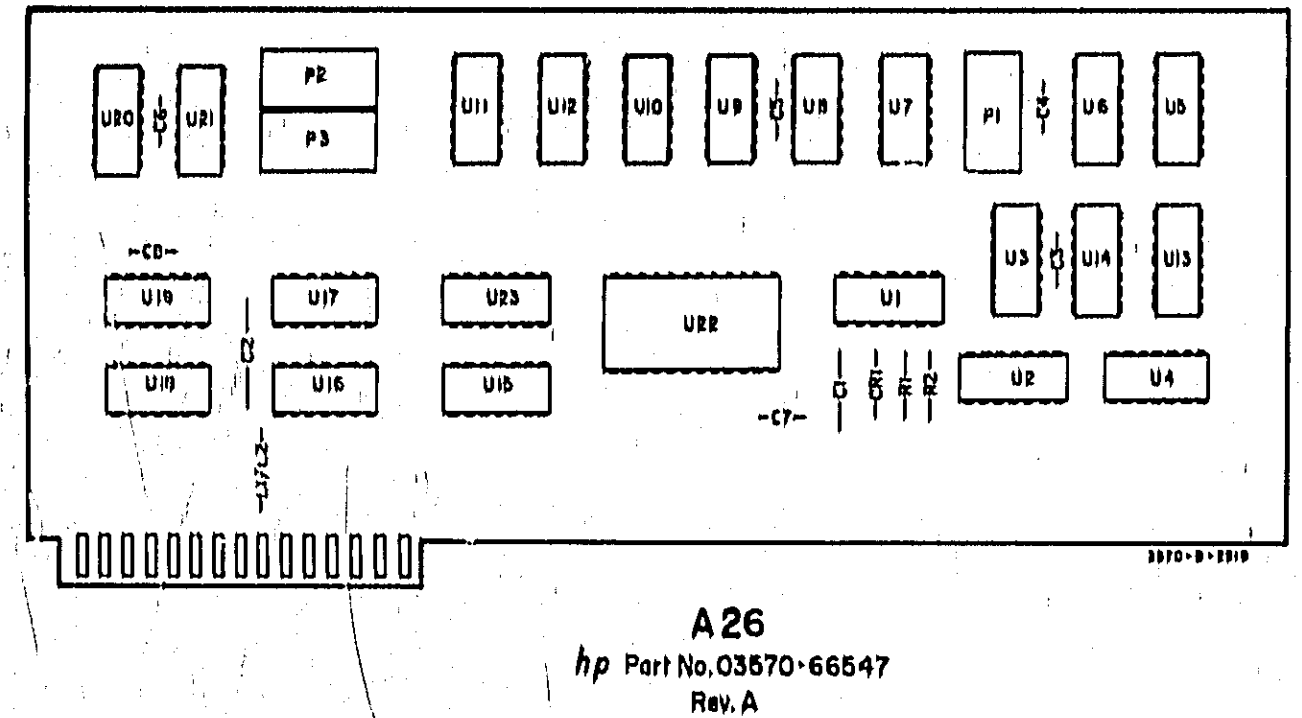
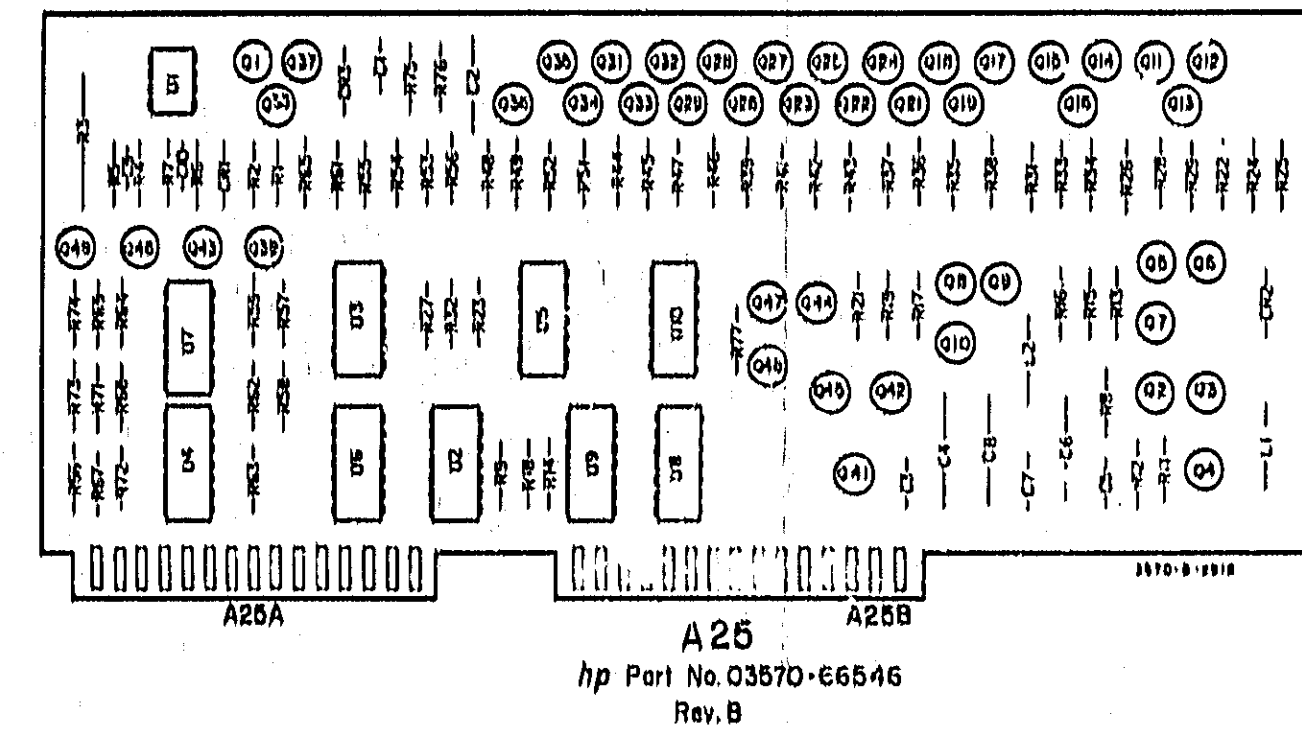
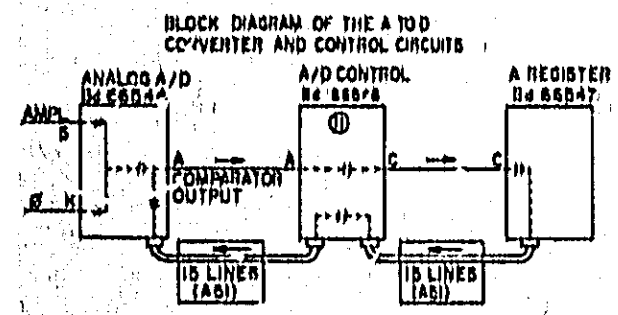
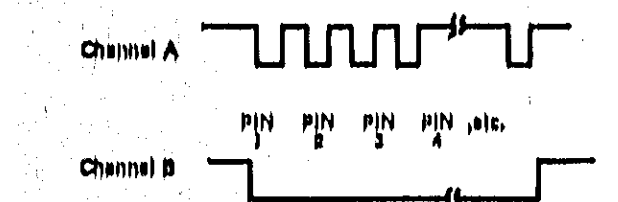
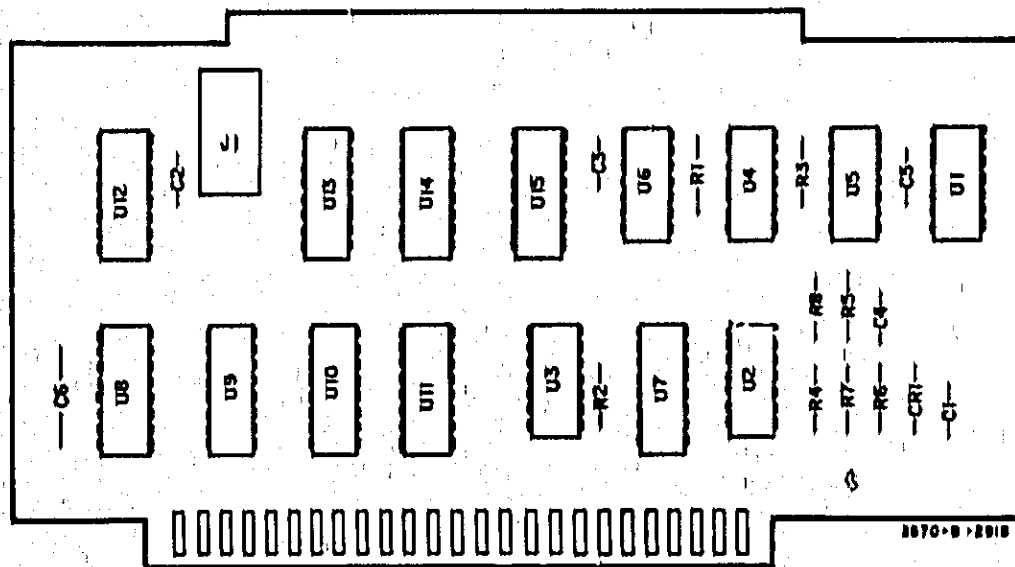
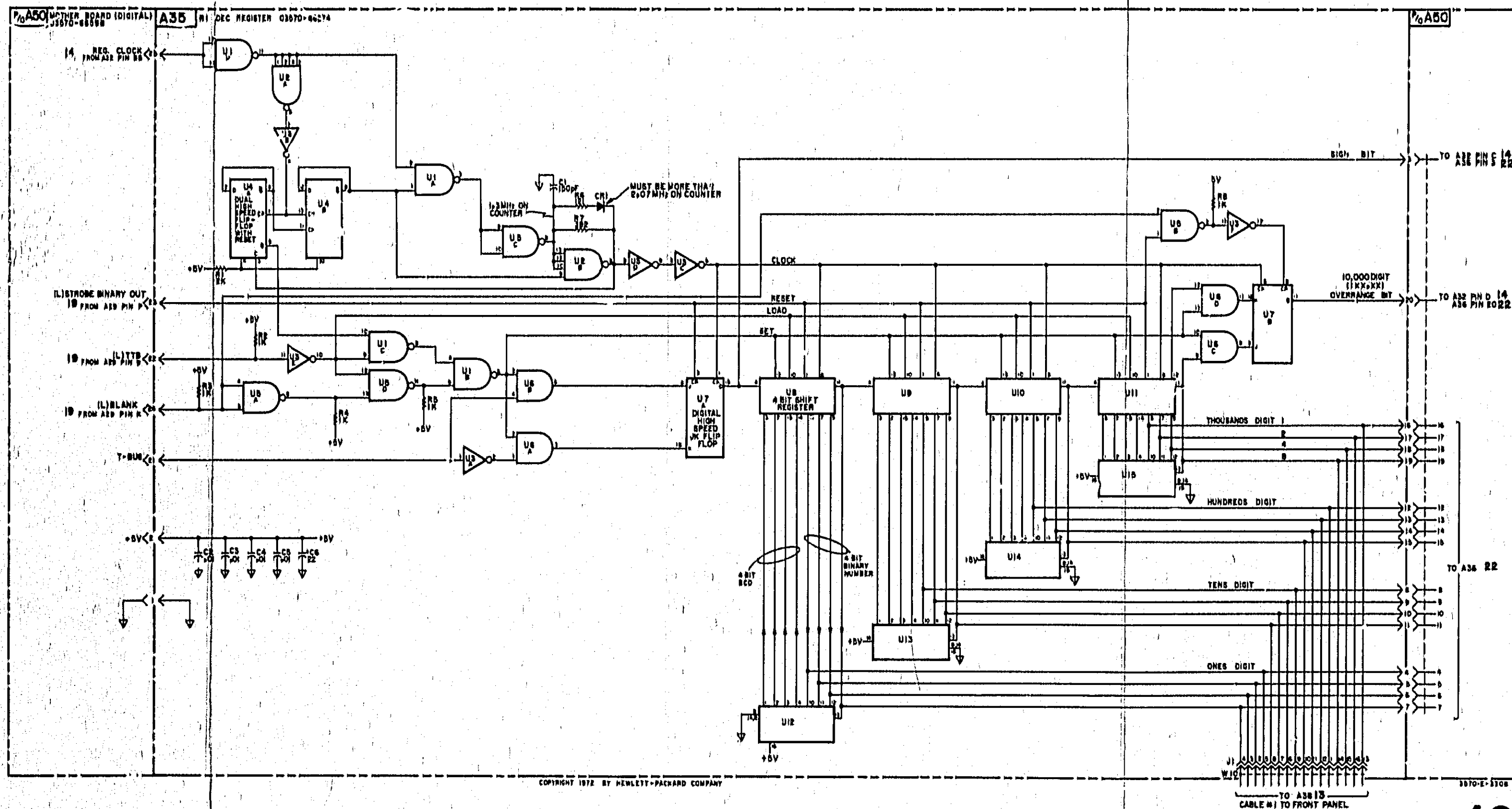


Figure 7-30. A Register (A26) and P/O A - D Control (A25) Schematics and Component Location Diagrams.



1070-B-2010

A35
hp Part No. 03570-66572
 Rev. A



NOTE 1

FOR TEST CONDITION ON DISPLAYS (127.07 BOTH AMPLITUDE AND PHASE), REMOVE CABLE NUMBER 6 (BLUE) FROM A38 (03070-66580),

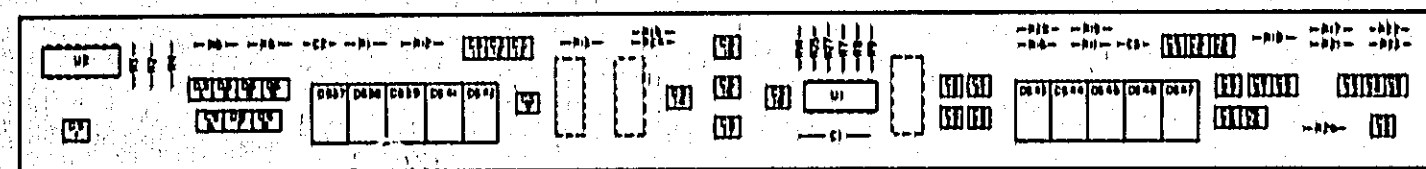
Truth Table for: DS37, 43.
1 = High

CHARACTER	PIN NO.	PIN NO.	PIN NO.	PIN NO.
+	1	2,3	4	8
-	1	X	X	1
Decimal point	X	1	X	X
Blank	0	0	0	0

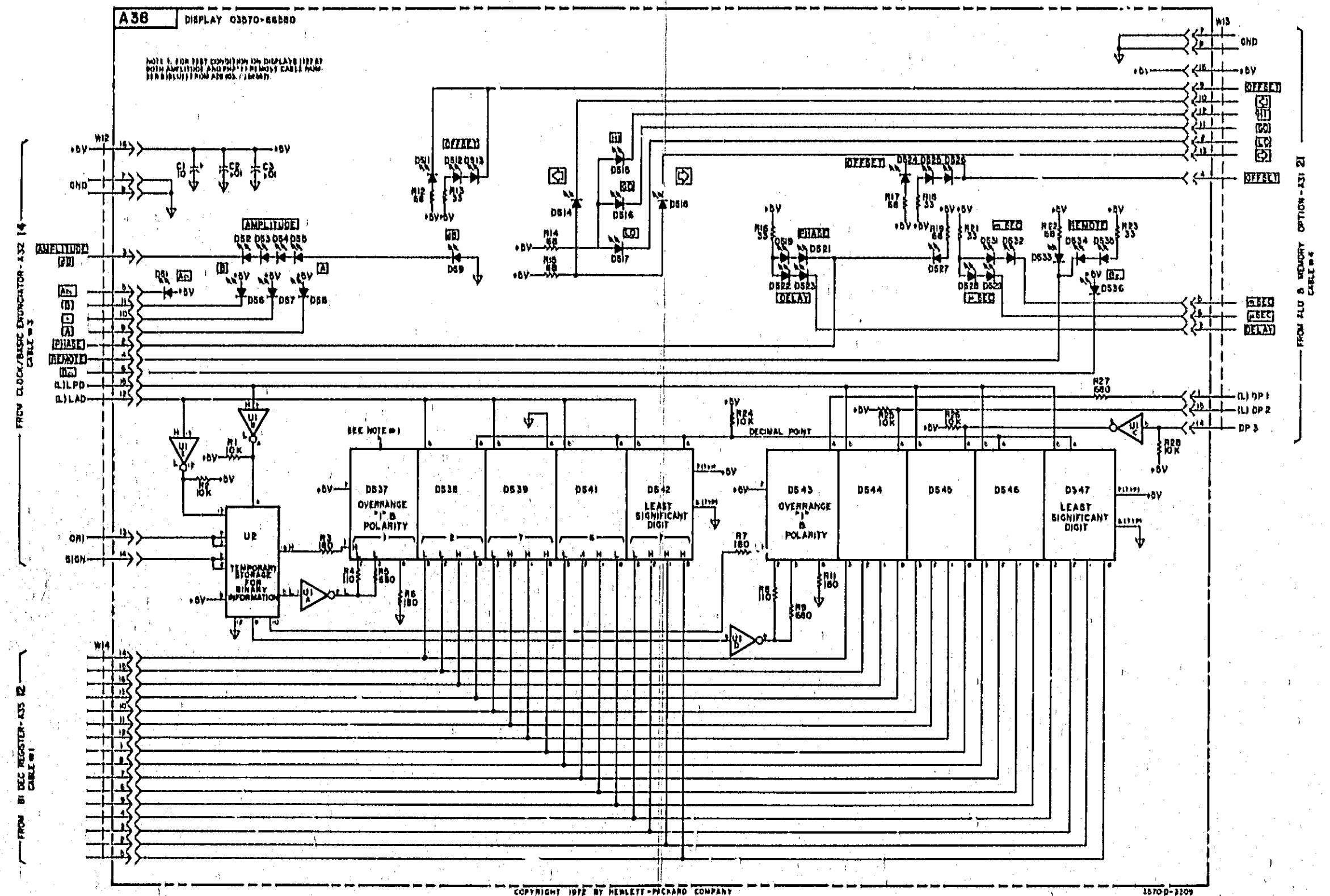
X = Don't Care

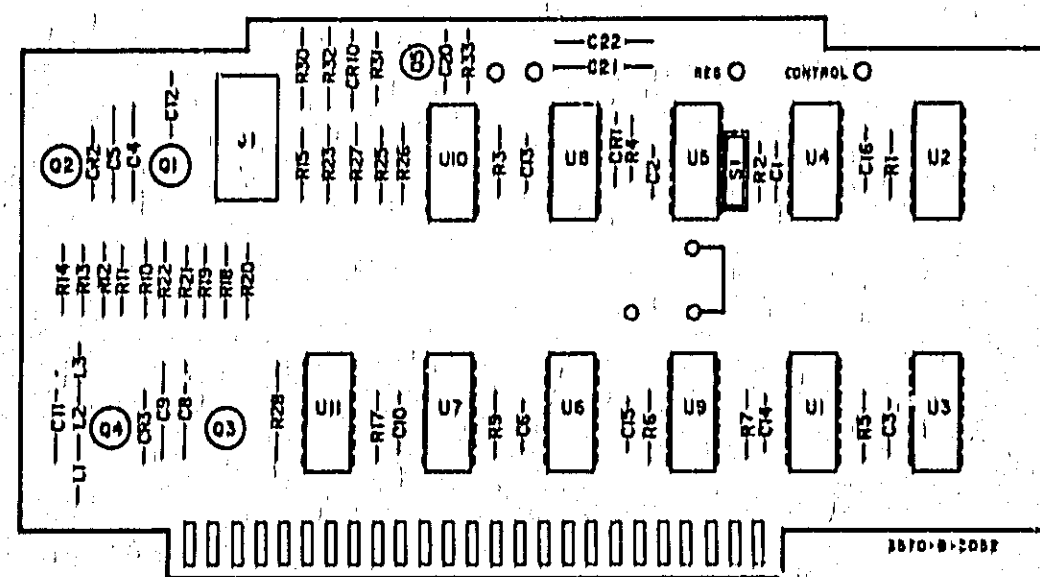
CHARACTER	INPUTS			
	PIN 5	PIN 2	PIN 1	PIN 8
0	X8	X4	X2	X1
1	L	L	L	L
2	L	L	L	L
3	L	L	L	L
4	L	L	L	L
5	L	L	L	L
6	L	L	L	L
7	L	L	L	L
8	L	L	L	L
9	L	L	L	L
Test	H	H	H	H
Blank	H	H	H	H
Blank	H	H	H	H
Blank	H	H	H	H
Blank	H	H	H	H
Blank	H	H	H	H

Decimal Point On DP_{IN} = L
Decimal Point Off DP_{IN} = H



A38
App Part No. 03070-66580
Rev A

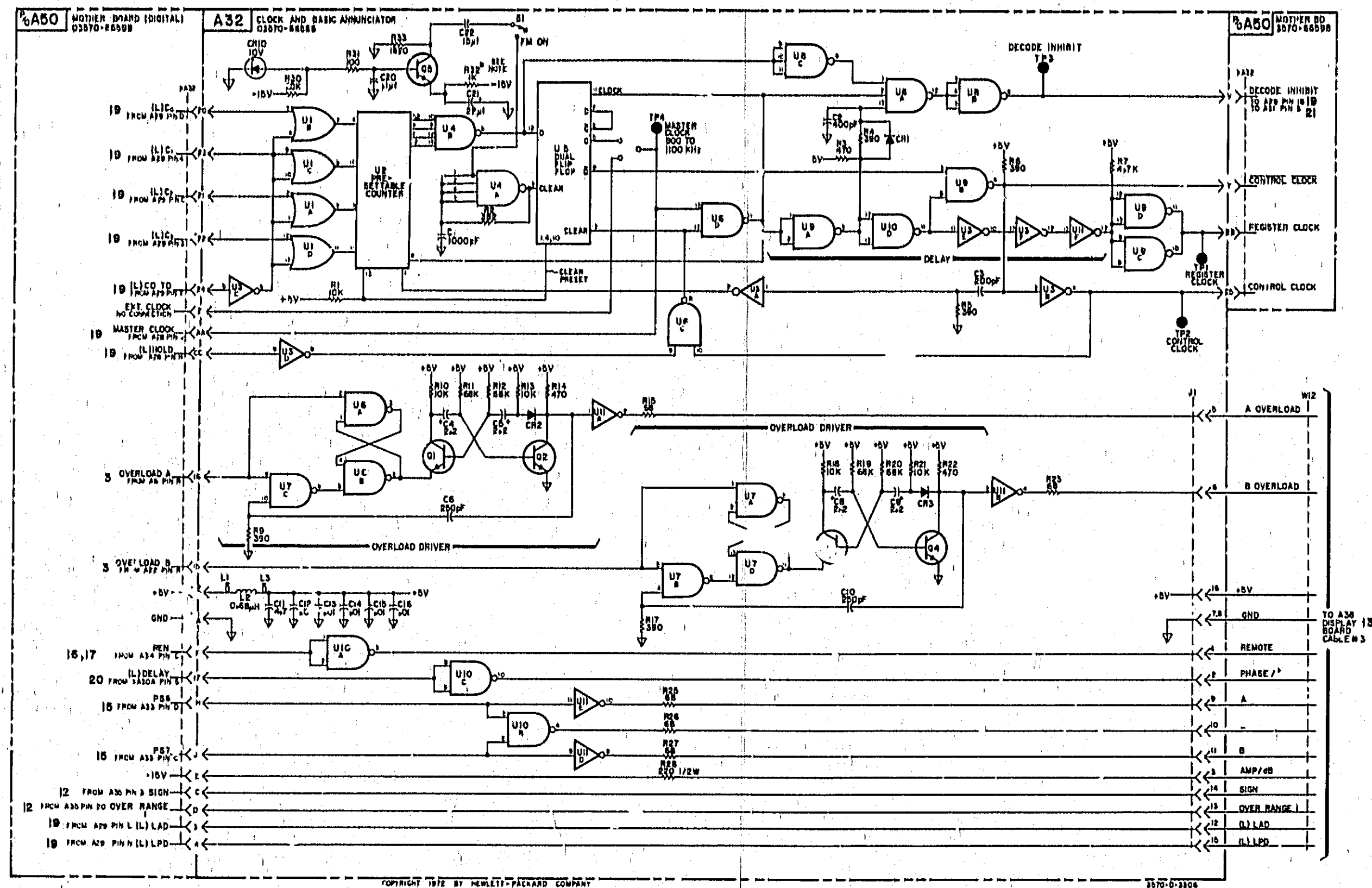




A32
hp Part No. 03570-66566
Rev. B

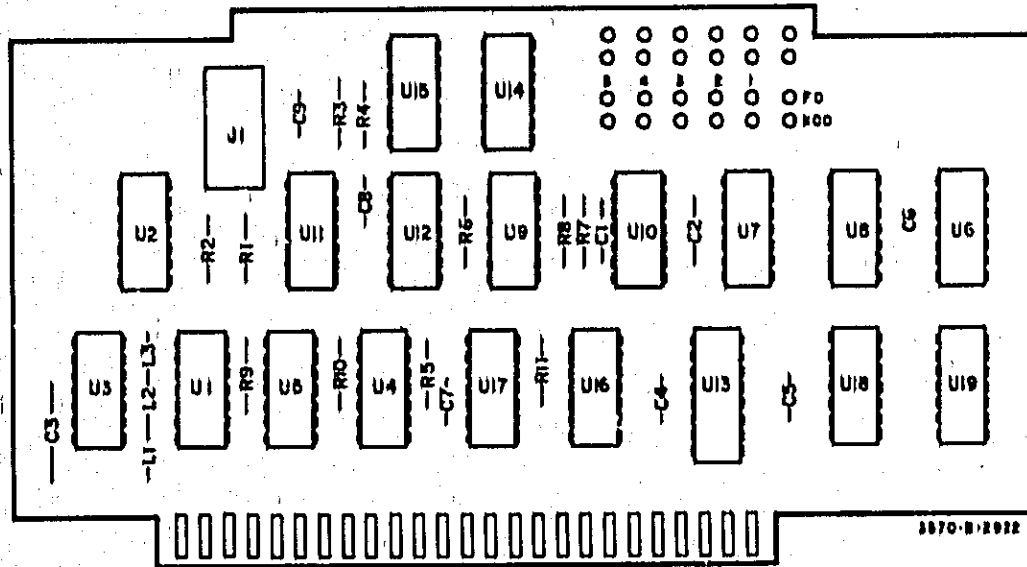
NOTE If A32U4 is changed or fails to function properly in the circuit, substitute one of the following resistors for A32R2 to reestablish operation.

348 OHM .01	0698-3455
274 OHM .01	0698-4452
392 OHM .01	0757-0413

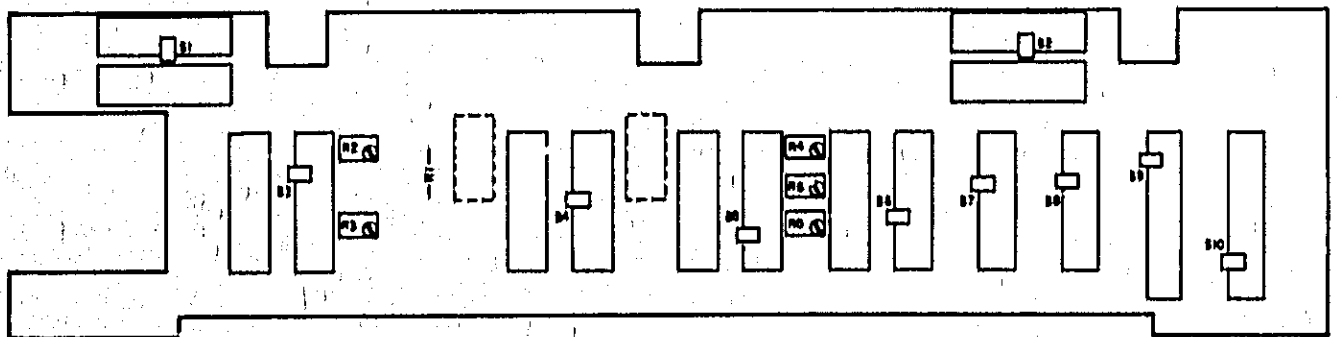


NOTE 1

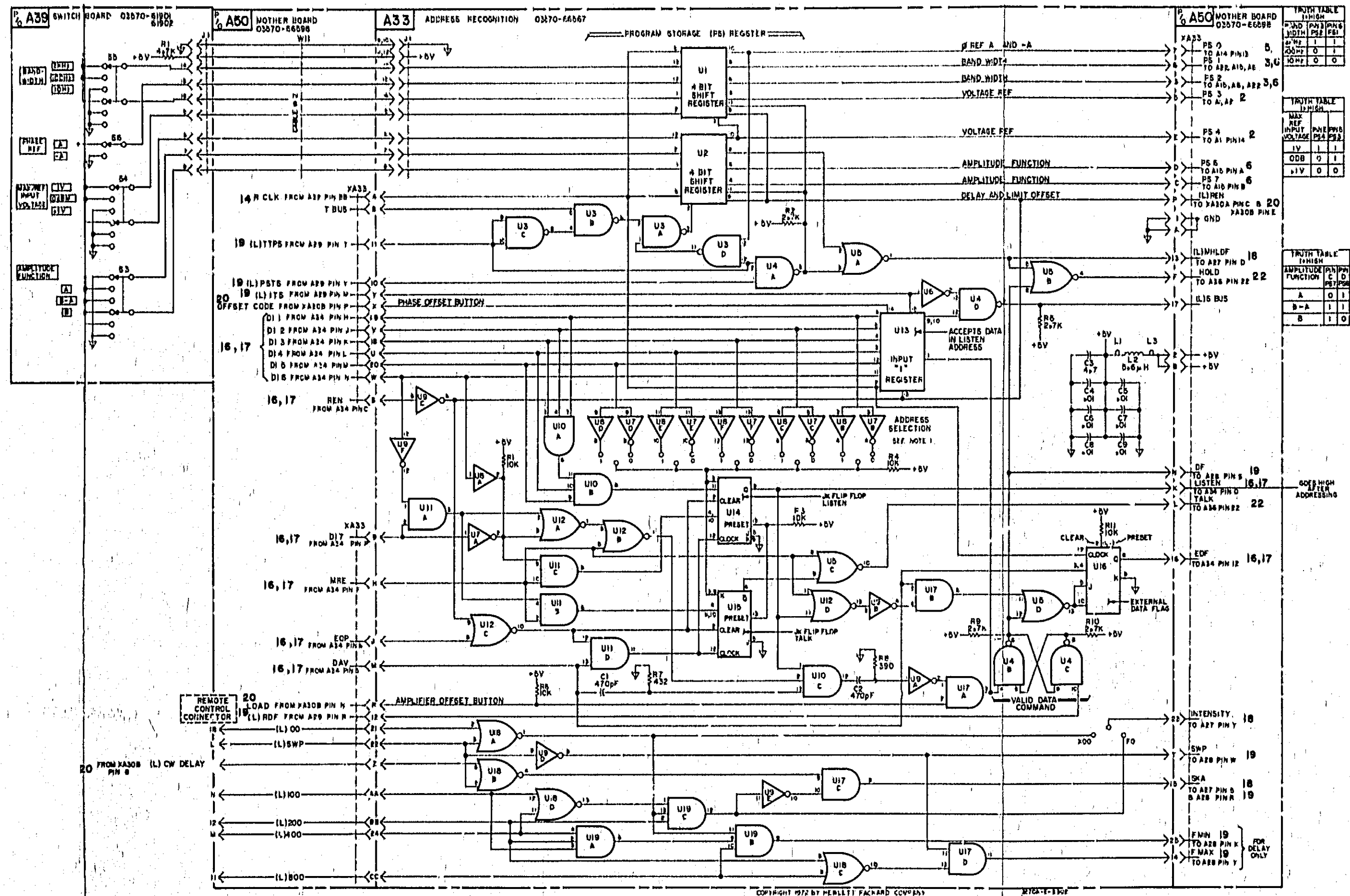
1 ohm resistors (Part No. 8150-3375) may have been installed as jumpers at the factory. These parts can be replaced using insulated jumper wires.



A33
hp Part No. 03570-66567
Rev. A



A39
hp Part No. 03570-61901
or 03570-61902 (SHOWN)
Rev. A



15

Figure 7-34. Address Recognition (A33) and P/O Front Panel Switch (A39) Schematics and Component Location Diagrams.

7-69/7-70

NOTE 1

WHEN THE INPUTS ARE GROUNDED, THESE LINES WILL GO HIGH.

NOTE 2

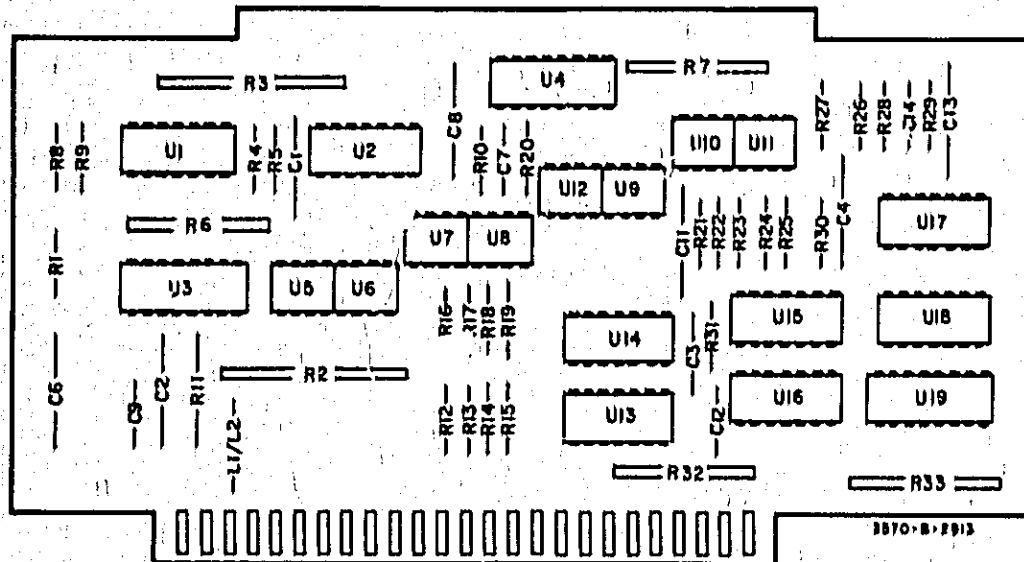
GROUND PIN "U", PIN "E" SHOULD GO LOW.

NOTE 3

GROUND PIN "V", PIN 14 SHOULD GO LOW.

NOTE 4

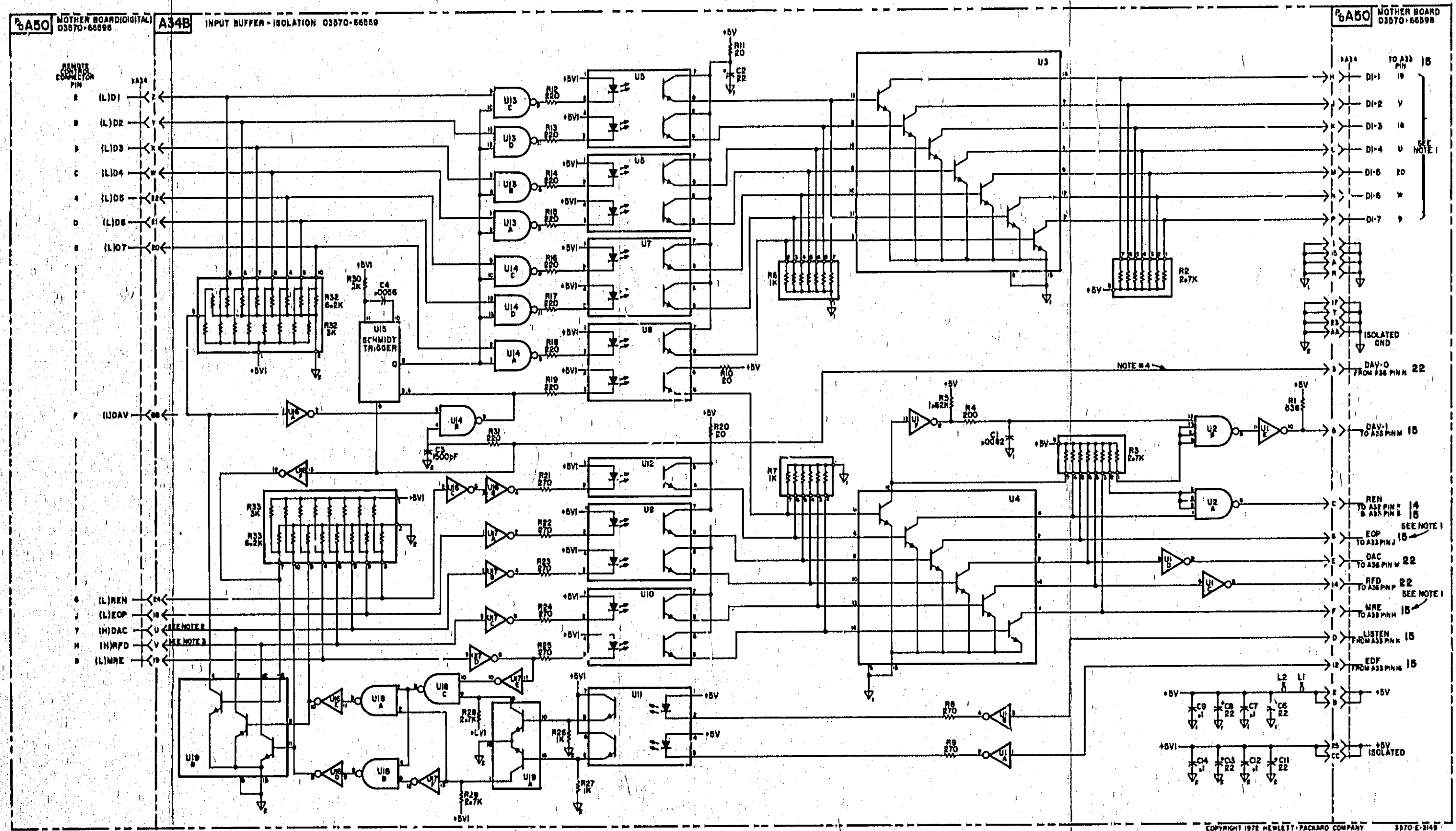
GROUND PIN "3", PIN "BB" SHOULD GO LOW.



A348

Part No. 03570-66569

Rev. A



NOTE 1

TO TROUBLESHOOT THIS BOARD USE THE 10525T LOGIC PROBE,

NOTE 2

IF THE FRONT PANEL DISPLAYS RACK AROUND AT HIGH SPEED, CHECK THE CLOCK CIRCUIT.

NOTE 3

THIS CIRCUIT PUTS MARKER DOTS ON THE WAVEFORM WHEN USING A SCOPE.

NOTE 4

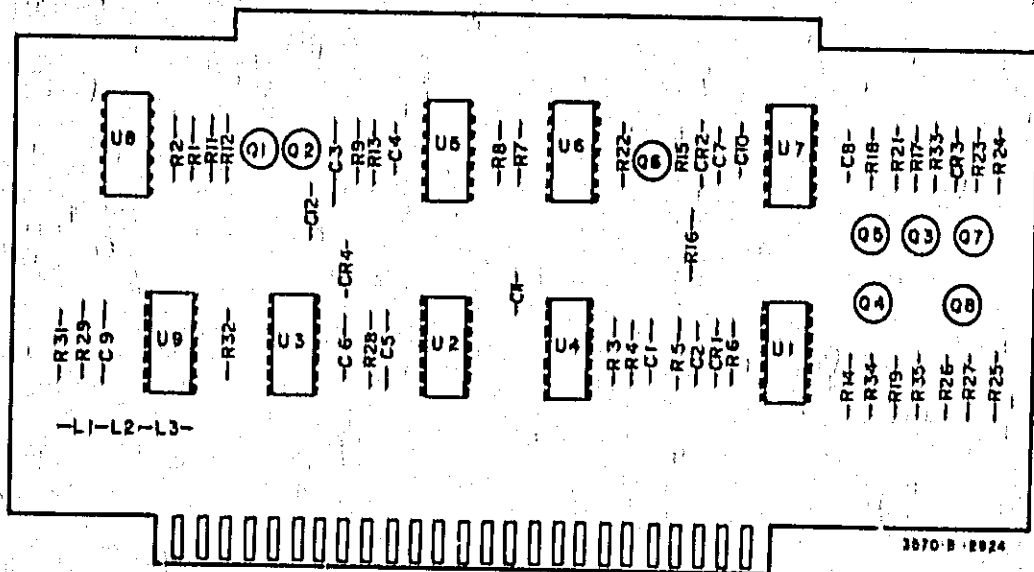
USED ONLY DURING LIMIT TESTING AT LIMIT TRANSITIONS.

NOTE 5

UID STOPS THE CLOCK WHEN A LIMIT IS REACHED.

NOTE 6

WHEN THE GPIB CABLE IS DISCONNECTED PINS D, E, X, 10, 11, 17, 18, AND 19 WILL BE HIGH.



A27

hp Part No. 0357-66561

Rev. A

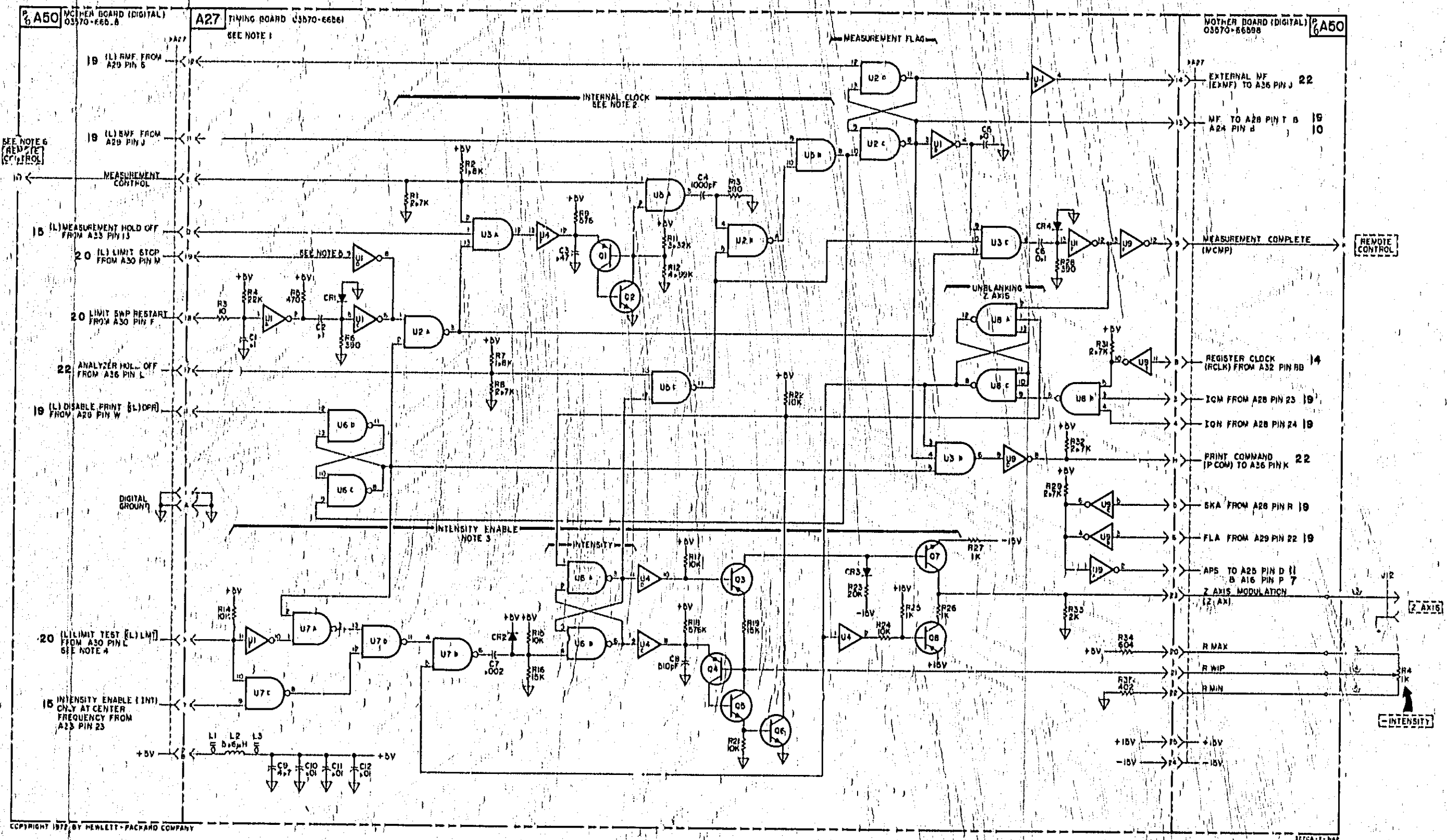
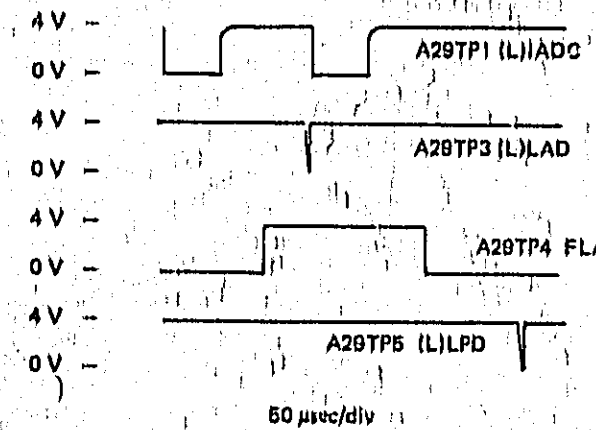


Figure 7-37. Timing Assembly (A27) Schematic and Component Location Diagram.

NOTE 1
IF CAUSE OF PROBLEM HAS NOT BEEN FOUND ON OTHER BOARDS, THE CONTROLLER BOARDS A28 AND A29 MAY BE AT FAULT. IF 3570A WILL TAKE A READING IN EITHER AUTO OR CONTROLLED MODE, CHECK SIGNALS AS SHOWN BELOW:



3570A SHOULD BE SET FOR AMPLITUDE AND PHASE MEASUREMENTS WITH NO LIMIT TEST OR OFFSET FUNCTIONS IN USE. USE A28TP1 AS REFERENCE SIGNAL AND TRIGGER, AND MONITOR OTHER TEST POINTS WITH OTHER CHANNEL OF DUAL TRACE OSCILLOSCOPE. TEST POINTS ARE ON RIGHT SIDE OF A28. A28TP2 (FLO) IS USED ONLY IN DELAY MEASUREMENTS, AND WILL CHANGE FROM ONE STATE TO ANOTHER FOR EACH SUCCESSIVE READING IN THE SWP DELAY MODE.

IF SIGNALS ARE CORRECT, CONTROLLER IS PROBABLY WORKING CORRECTLY.

IF SIGNALS ARE NOT CORRECT, CONTROLLER BOARD A28 OR A29 MAY BE DEFECTIVE. MISSING QUALIFIERS TO A28 COULD ALSO CAUSE A PROBLEM. QUALIFIERS USED IN THE BASIC MEASUREMENT ROUTINE (AMPLITUDE AND PHASE) ARE MF, DF, FLA AND ADC.

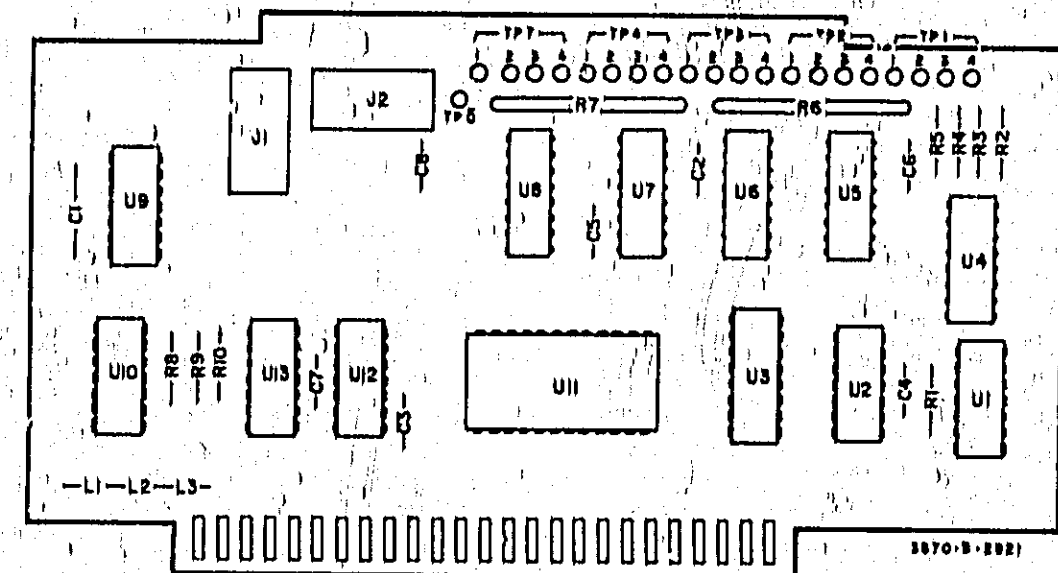
ANOTHER SOURCE OF CONTROLLER ERRORS COULD BE DEFECTIVE CONTROL CLOCK AND DECODE INHIBIT CIRCUITRY ON A32.

IF 3570A WILL NOT TAKE A MEASUREMENT, A28 AND A29 SHOULD BE REPLACED BY TRIAL AND ERROR.

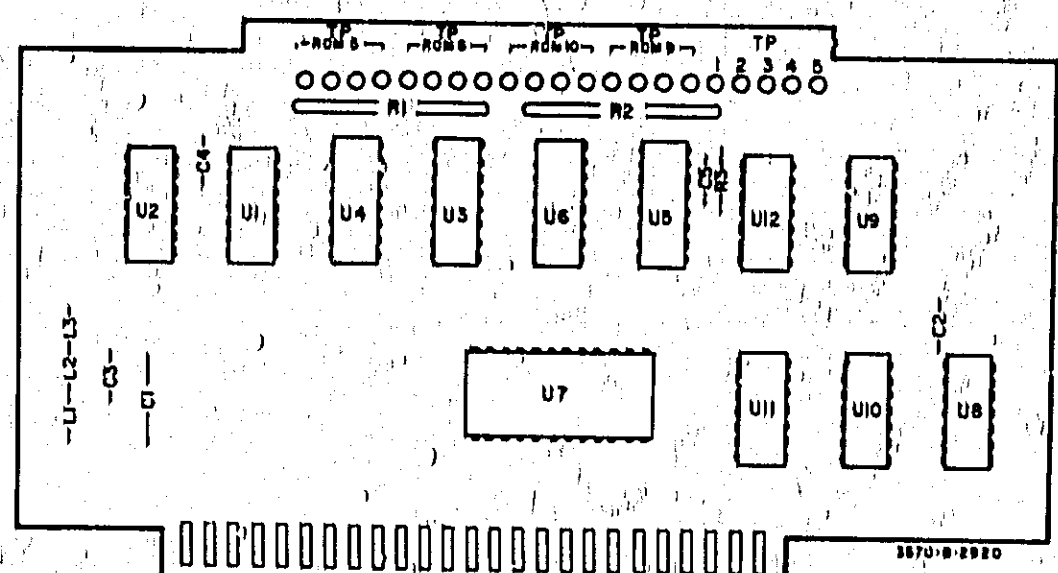
NOTE 2
WHEN ROMs 1, 2, 3, 4, AND 7 ARE REMOVED, U1 AND U2 SHIFT REGISTER OUTPUTS GO HIGH.

NOTE 3
"Q" REGISTER IS DATA HANDLING. THE 6 BITS THAT SERVE AS THE QUALIFIERS FOR THE CONTROLLER ARE AS FOLLOWS:

Qualifier	Pin	U
1	10	12
2	8	12
3	6	12
4	4	12
5	4	13
6	6	13



A28
hp Part No. 03570-66562
Rev. A



A29
hp Part No. 03570-66563

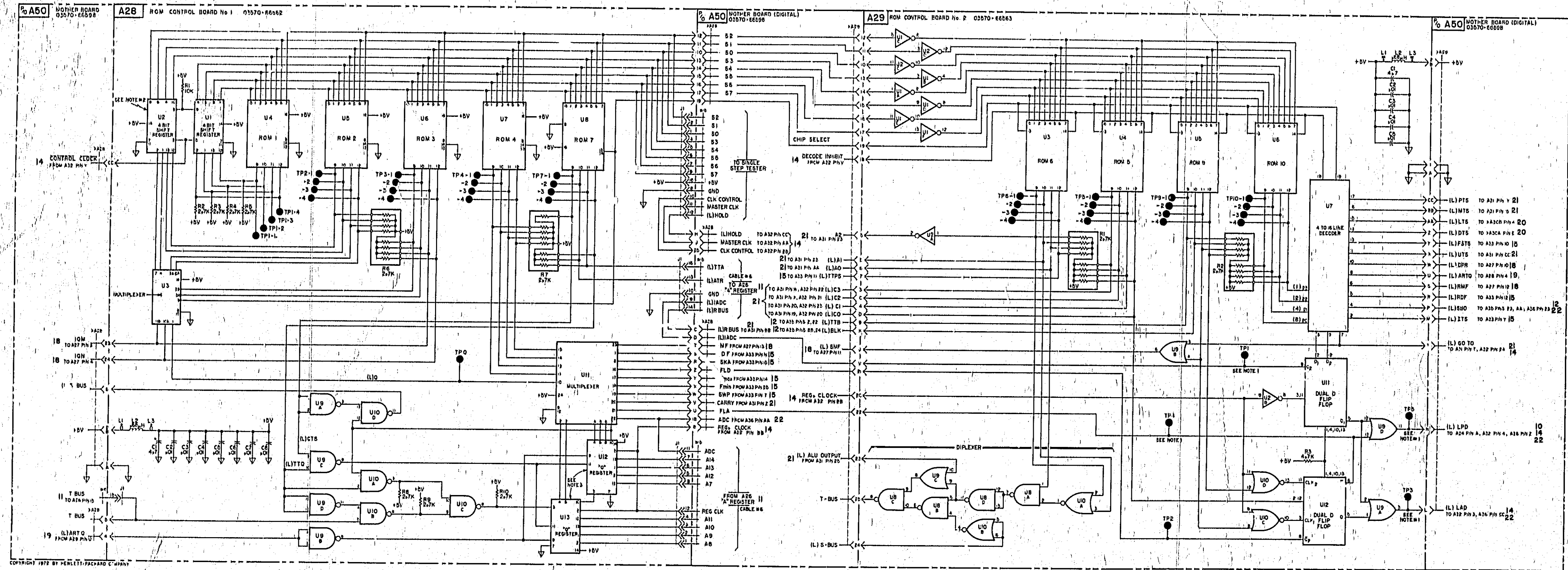


Figure 7-38. ROM Control No. 1 (A28) and ROM Control No. 2 (A29) Schematics and Component Location Diagrams.

NOTE 1
PIN N GOES LOW WHEN THE AMPLITUDE OFFSET BUTTON IS DEPRESSED IN LOCAL.

NOTE 2
PIN "P" GOES HIGH WHEN THE PHASE OFFSET BUTTON IS DEPRESSED IN LOCAL.

NOTE 3
LIMIT TEST AND OFFSET FUNCTIONS ARE CONTROLLED BY L REGISTER (U1), U2 AND U3 ON A30. COMPLETELY CHECK L REGISTER BY ENTERING OFFSETS IN LOCAL AND REMOTE, AND BY PROGRAMMING LIMIT TEST FUNCTIONS REMOTELY. CHECK LOGIC LEVELS AT L REGISTER TEST POINTS ON A30, AND COMPARE WITH TABLE. LEVELS MAY BRIEFLY CHANGE STATE ONCE EACH MEASURE PERIOD, BUT "STEADY STATE" LEVELS ARE LEVELS OF INTEREST.

NOTE 4
TPL9 WILL GO HIGH WHENEVER FOLLOWING COMMANDS ARE GIVEN:

AMPL OFFSET
PHASE/DELAY OFFSET
UPPER LIMIT
LOWER LIMIT

TPL9 WILL REMAIN HIGH AS DIGITS ARE ENTERED AFTER ANY OF THESE COMMANDS. TPL9 WILL GO LOW WHEN A COMMAND OTHER THAN ONE OF THE FOUR LISTED ABOVE IS RECEIVED. THIS WILL TERMINATE THE DIGIT ENTRY SEQUENCE.

TPL1 AND TPL8 ARE DETERMINED BY THE 3570A AND SHOULD CORRESPOND TO THE FRONT PANEL LIMIT TEST ANNUNCIATORS.

A30 LOGIC LEVELS (PINS ON RIGHT CONNECTOR):

PIN L: 0 = LIMIT TEST MODE
PIN M: 0 = LIMIT TEST STOP MODE
PIN N: NORMALLY HIGH, LOW PULSES GENERATED WHEN EITHER "ENTER OFFSET" BUTTON PUSHED IN LOCAL.
PIN P: GOES HIGH WHEN PHASE "ENTER OFFSET" BUTTON PUSHED.

THE FOLLOWING TABLE GIVES A COMPLETE BREAKDOWN OF THE TEST POINTS L0 THROUGH L9.

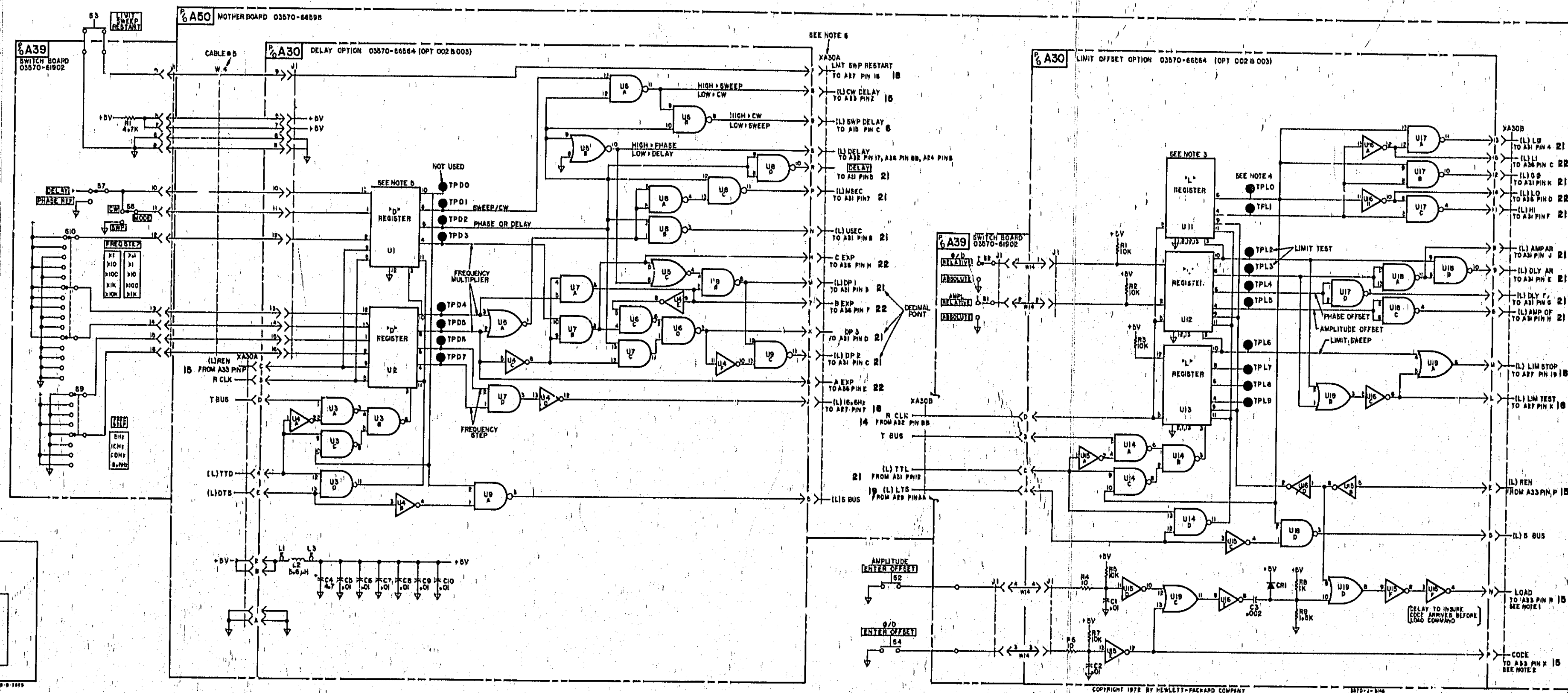
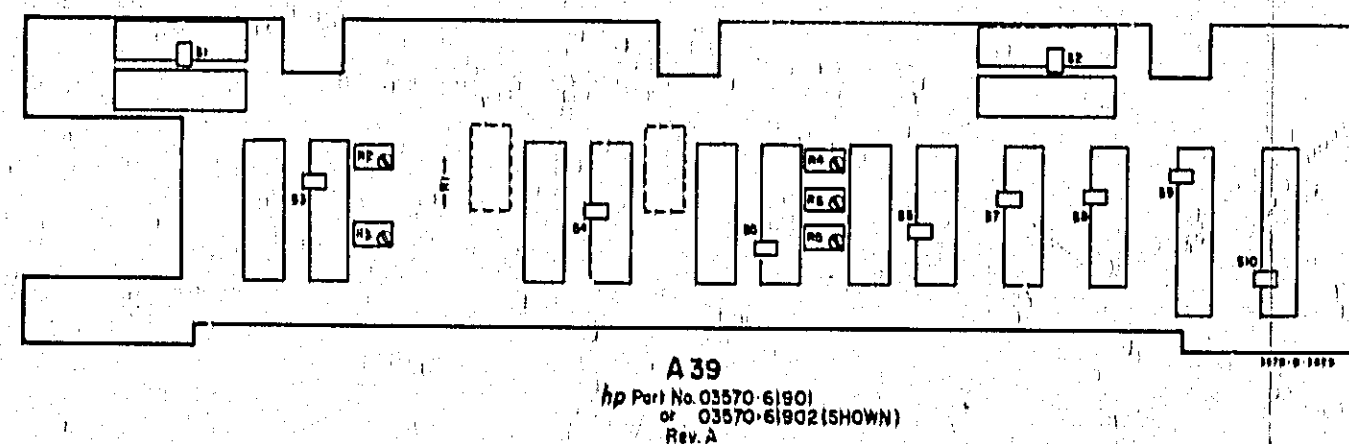
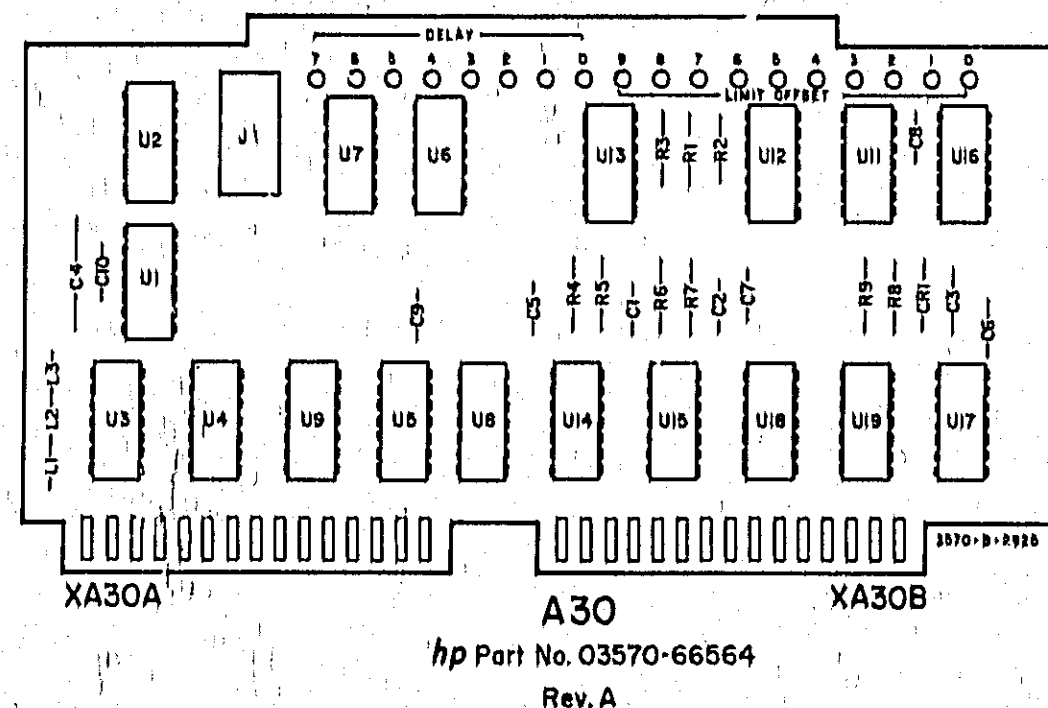
ENTRY SEQUENCE				LIMIT SWEEP		AMPL OFFSET		PHASE/DELAY OFFSET		LIMIT TEST MODE			LIMIT CONDITION	
TP	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0				
NO ENTRY	0	X	X	STOP	0	ABSOLUTE	0	ABSOLUTE	0	AMPL	1	X	NONE	0
AMPL OFFSET	1	0	0	NO STOP	1	RELATIVE	1	RELATIVE	1	PHASE/ DELAY	0	1	LO	0
PHASE/DELAY OFFSET	1	0	1							NO LIMIT TEST	0	0	HI	1
UPPER LIMIT	1	1	0										GO	1
LOWER LIMIT	1	1	1											

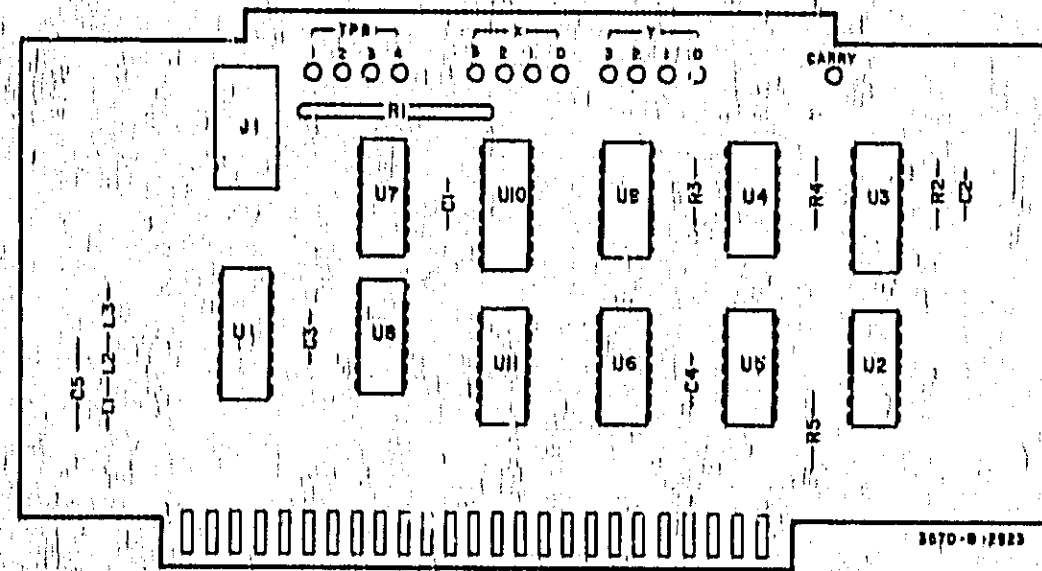
D Register (A30U1 and U2)										
TP	D7	D6	D5	D4	D3	D2	D1	D0		
5 Hz	0	0	10 K	0	0	0	Phase Delay	0	1	SWP
10 Hz	0	1	1 K	0	0	1	Delay	0	1	CW
20 Hz	1	0	100	0	1	1		0	1	
100 Hz	1	1	10	1	1	1		0	1	Not Used

X = DON'T CARE

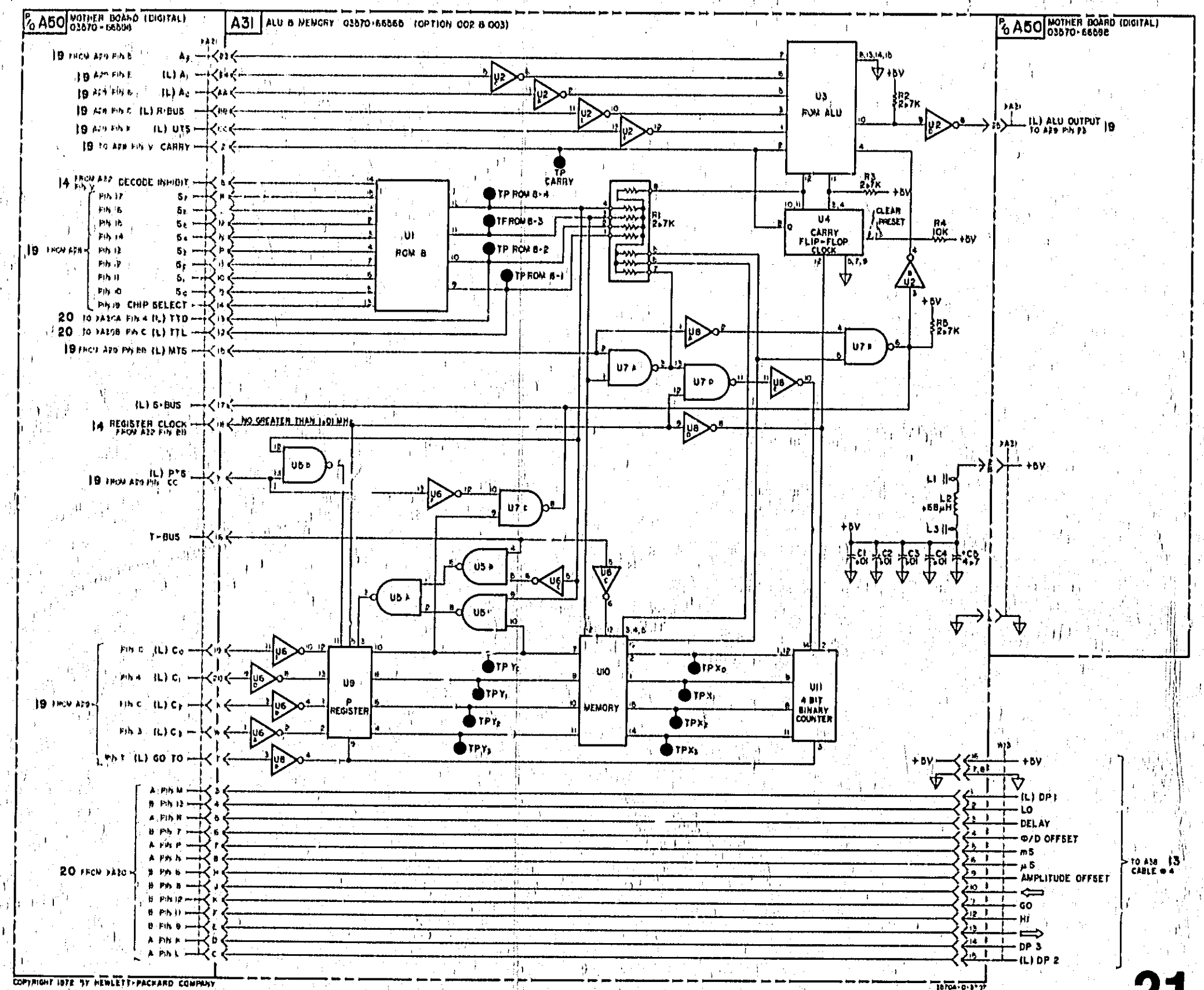
IF D REGISTER OUTPUTS ARE CORRECT, CHECK THE FOLLOWING A30 OUTPUTS IN DELAY MODE (PINS ON LEFT CONNECTOR OF A30XA30A):						
PIN B (L)CW DELAY	1 = SWP DELAY OR PHASE					
PIN G (L)SWP DELAY	0 = CW DELAY					
PIN S (L)DELAY	1 = PHASE					
PIN J (L)16.6 Hz	0 = DELAY					
	1 = 5, 10, 20 Hz					
	0 = 16.6 Hz					

(OUTPUTS IN DELAY MODE)						
FREQ MULTIPLIER						
SIGNAL	A30 PIN	X1	X10	X100	X1K	X10K
(L)MSEC	P	0	0	0	1	0
(L)USEC	N	1	1	1	0	1
(L)D1	M	1	1	0	1	1
(L)D2	L	1	0	1	1	0
(L)D3	K	0	1	1	0	1
C EXP	H	0	0	0	1	1
B EXP	7	0	1	1	0	0
A EXP	6	1	0	0	0	0





A31
hp Part No. 03570-66565
Rev. A

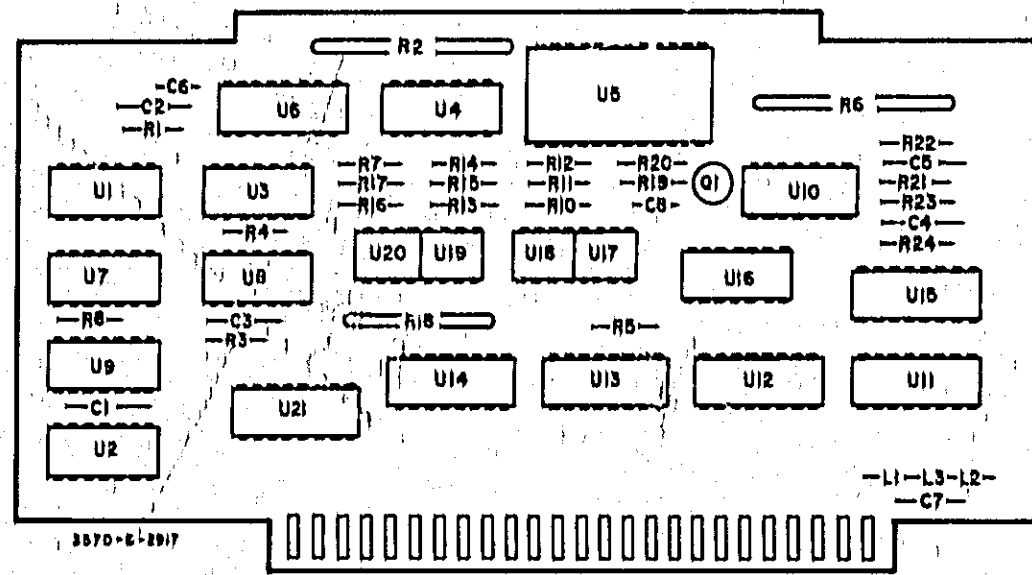


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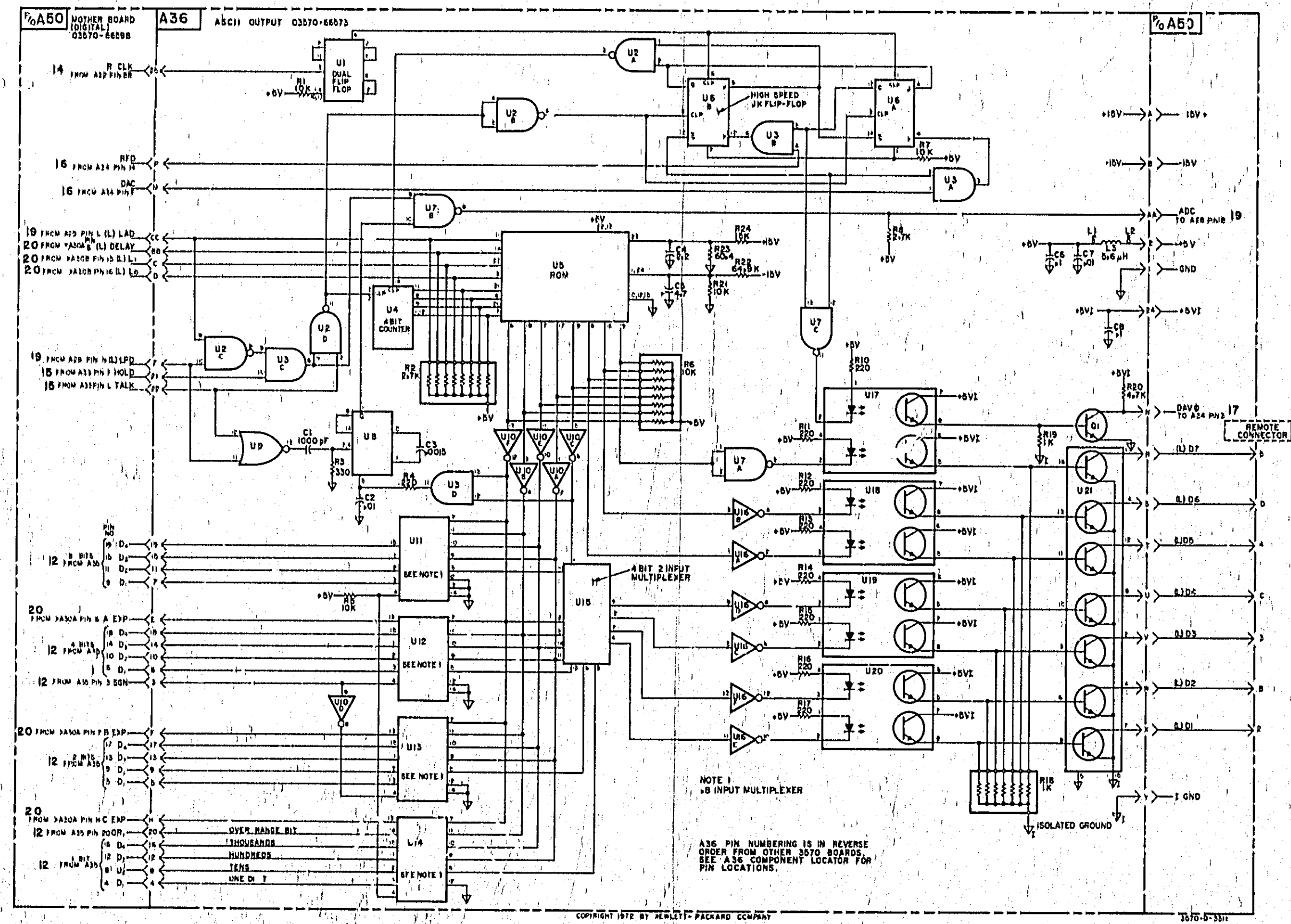
1070A-0-17-27

Figure 7-40. ALU and Memory (A31) Schematic and Component Location Diagram.

7-81/7-82



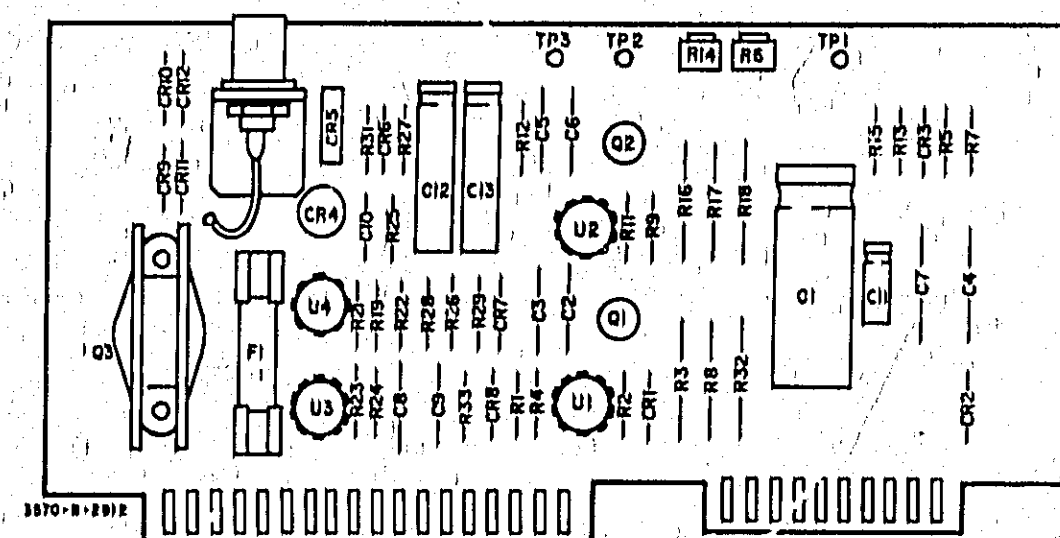
A36
hp Part No. 03570-66573
 Rev. A



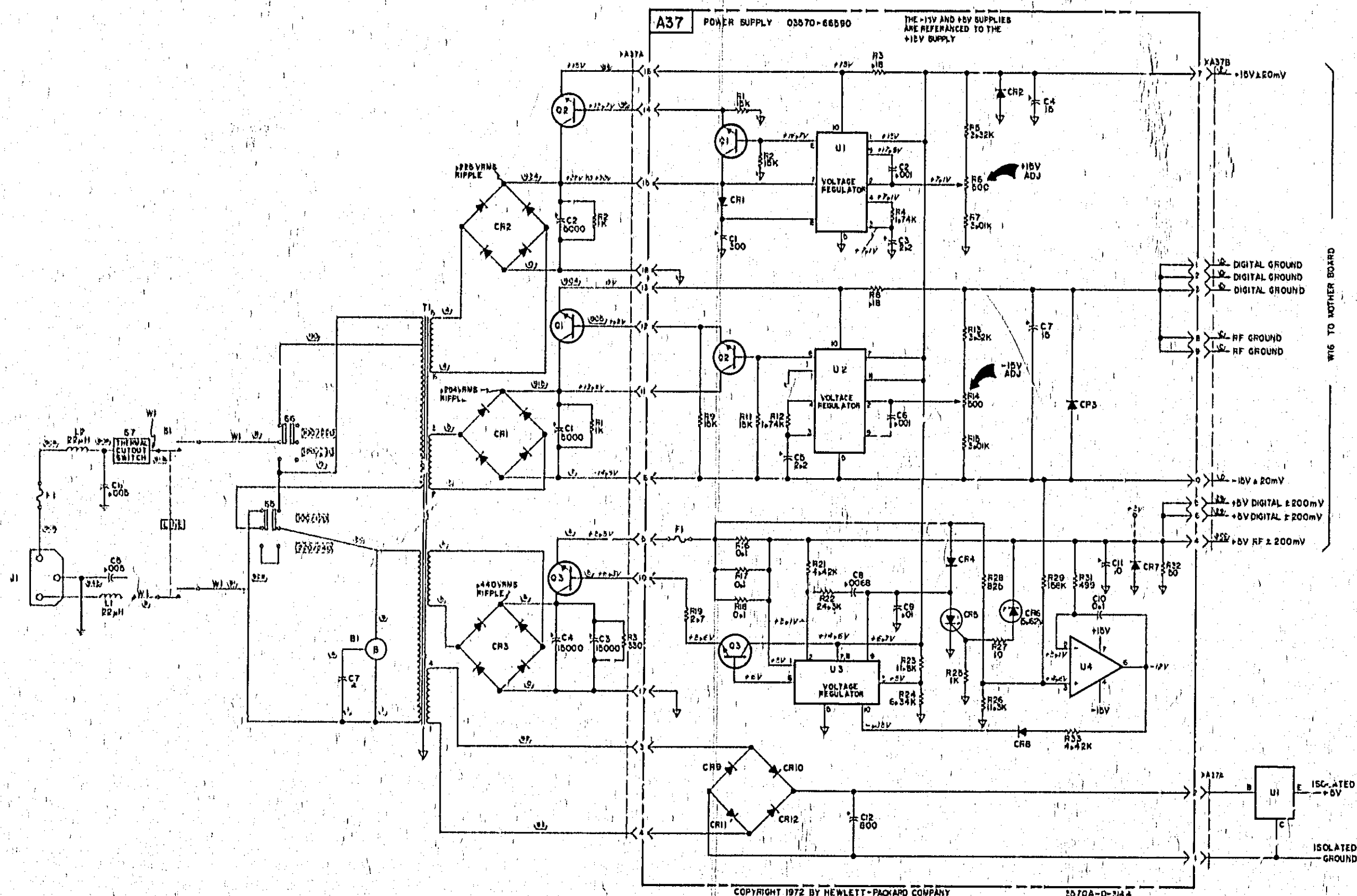
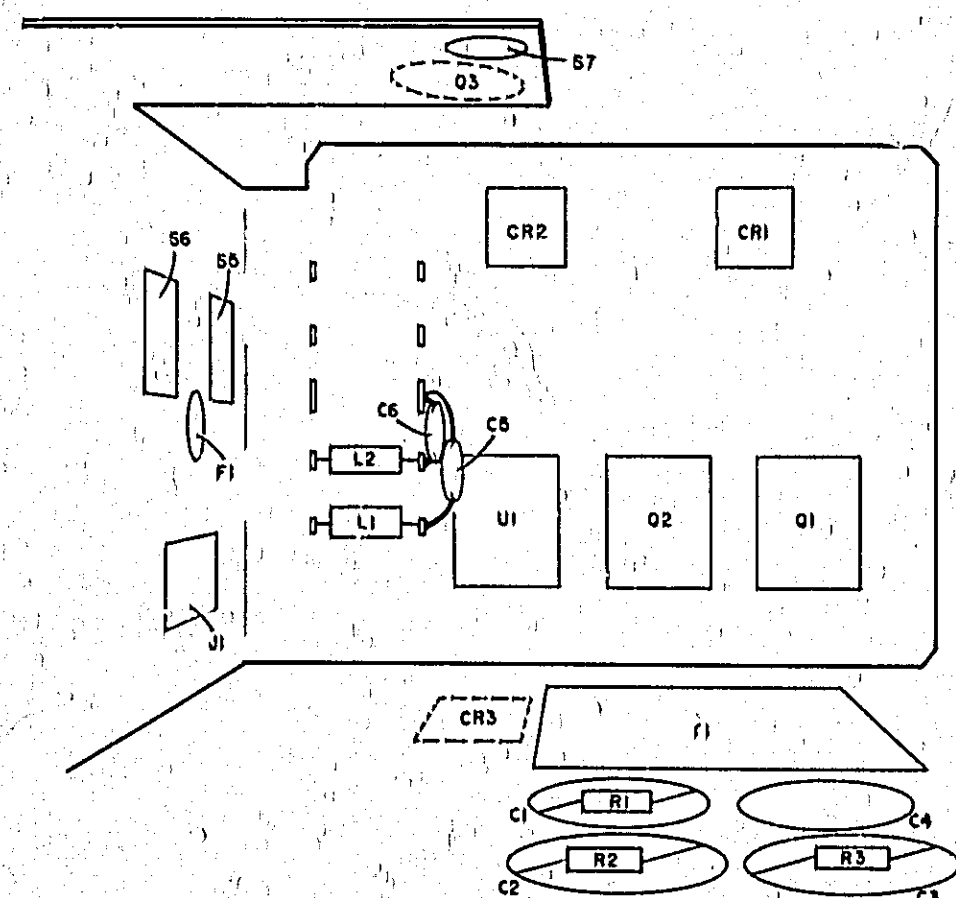
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Figure 7-41. ASCII Output Assembly (A36) Schematic and Component Location Diagram.

7-83/7-84



A37
Part No. 03570-66590
Rev. A



SECTION VIII BACKDATING

8-1. INTRODUCTION.

8-2. This section contains backdating changes which make this manual applicable to earlier instruments. Where possible, backdating changes have been integrated into the manual text, parts list and schematic diagrams. Changes that are too long or otherwise impractical to integrate into the manual are covered in this section. Backdating changes included in this section are referenced by a numbered delta (Δ) which appears in the text, parts list and schematic diagrams. The number indicates the number of the corresponding backdating change. Make all backdating changes that apply to your instrument.

- Δ 8-3. Change number 1 for serial numbers 11251A00245 and below. Paragraphs affected by this change will be 4-27, 4-28, 4-29, 5-47, 5-48, 5-49, 5-50, 5-61, 5-62 and Figures 7-13 and 7-15. (Backdated schematics for this change are Figures 8-3 and 8-4.) The paragraphs affected are as follows:

4-27. Log Amplifier (A7/A23 Schematic No. 4). The Log Amplifier is comprised of three sections: the log amplifier (U1 through U6), an amplitude detector (Q1, Q2, U7) and an IF amplifier (Q3, Q4). The log amplifier section consists of a log amplifier (U5) and five control amplifiers (U1 through U4, U6). The log amplifier is a hybrid circuit designed specifically for use in the 3570A. This circuit converts the amplitude of the incoming IF signal to a logarithmic value, providing the 100 dB dynamic range of the instrument. The control amplifiers are used to gate on succeeding stages within the log amplifier as a function of signal level. The logarithmic signal from pin 11 of the log amplifier package is coupled through C17 to the amplitude detector and the IF amplifier.

4-28. The amplitude detector is a full wave rectifier circuit which converts the 100 kHz logarithmic signal to a dc voltage. The output of the detector, a dc voltage logarithmically proportional to the amplitude of the input signal, is applied to the Output Buffer.

4-29. The IF amplifier is a two-stage, narrow-band amplifier circuit which provides a gain of five and filters the logarithmic signal, making it a pure 100 kHz sine wave. The 100 kHz sine-wave output is applied to the Phase Limiter.

5-47. Log Amplifier Phase Adjustments. (For instruments equipped with 03570-66535 or 03570-69535 Log Amplifier Boards only. Not necessary for instruments equipped with 03570-66555 or 03570-69555 Log Amplifier Boards.)

5-48. These adjustments peak the amplitude of the signals applied to the Phase Limiter and equalize the phase shift introduced by the A and B Log Amplifiers, A7 and A23.

RECOMMENDED TEST EQUIPMENT:

AC Digital Voltmeter (hp-Model 3450A)

a. Perform the Front Panel Zero Adjustments (phase) as outlined in Paragraph 3-157 (Section III). Use the 0 dBm Max/Ref Input Voltage setting and the 3 kHz Bandwidth setting with the Synthesizer set to 0 dBm, 1 MHz.

b. Set the 3570A LINE switch to OFF. Remove the Channel B Bandwidth Logic Assembly, A22.

c. Place both Log Amplifier Assemblies, A7 and A23, on extenders.

d. Connect a clip lead between A7 pin 4 and A23 pin 4.

e. Set the 3570A controls as follows:

LINE ON
MAX/REF INPUT VOLTAGE ... 0 dBm
BANDWIDTH 3 kHz
PHASE REFERENCE A

f. Set the Synthesizer for an output of 0 dBm, 1 MHz.

g. Connect the DVM (ac function) to A7TP3.

h. Adjust A7L1 for a maximum reading on the DVM. Be sure the *absolute peak* is found (intermediate peaks will occur).

i. Connect DVM to A23TP3.

j. Adjust A23L1 for a maximum reading on the DVM. Be sure the *absolute peak* is found.

k. Disconnect the DVM.

l. Observe the front panel phase reading. If the phase reading is greater than ± 2.00 degrees, repeat Steps g through i. If the phase reading is less than ± 2.00 degrees, alternately adjust A7L1 and A23L1 for a phase reading of 00.00 degrees, ± 0.05 degrees.

m. This completes the Log Amplifier Phase Adjustments. Proceed to the Bandwidth Logic Phase Adjustments (Paragraph 5-47).

5-49. Bandwidth Logic Phase Adjustments. (For instruments equipped with 03570-66535 or 03570-69535 Log Amplifier Boards only. See Section V, Paragraph 5-47 for instruments equipped with 03570-66555 or 03570-69555 Log Amplifier Boards.)

5-50. These adjustments peak the 100 kHz response of the IF amplifiers on the Bandwidth Logic Assemblies and equalize the phase shift introduced by the A and B Bandwidth Logic circuits.

RECOMMENDED TEST EQUIPMENT:

AC Digital Voltmeter (hp-Model 3450A)

a. Perform the Log Amplifier Phase Adjustments (Paragraph 5-45).

b. Set the 3570A LINE switch to OFF. Remove the Channel B IF Mixer Assembly, A18.

c. Place both Bandwidth Logic Assemblies, A6 and A22, on extenders.

d. Connect a clip lead between A6 pin 1 and A22 pin 1.

e. Set the 3570A controls as follows:

LINE ON
MAX/REF INPUT VOLTAGE .. 0 dBm
BANDWIDTH 3 kHz
PHASE REFERENCE A

f. Set the Synthesizer for an output of 0 dBm, 1 MHz.

g. Connect the DVM (ac function) to A6TP1.

h. Adjust A6L1 (IF OUTPUT ADJ) for a maximum reading on the DVM. Be sure the *absolute peak* is found (intermediate peaks may occur).

i. Connect the DVM to A22TP1.

j. Adjust A22L1 (IF OUTPUT ADJ) for a maximum reading on the DVM. Be sure the *absolute peak* is found.

k. Disconnect the DVM.

l. Observe the front panel phase reading. If the phase reading is greater than ± 2.00 degrees, repeat Steps g through i. If the phase reading is less than ± 2.00 degrees, alternately adjust A6L1 and A22L1 for a phase reading of 00.00 ± 0.05 degrees.

m. This completes the Bandwidth Logic Phase Adjustments. Proceed to the Input Mixer Phase Adjustments (Paragraph 5-49).

5-61. Log Amplifier Adjustments. (For instruments equipped with 03570-66535 or 03570-69535 Log Amplifier Boards only. See Section V, Paragraph 5-59 for instruments equipped with 03570-66555 or 03570-69555 Log Amplifier Boards.)

5-62. The following adjustments establish the amplitude linearity of the A and B Log Amplifiers, A7 and A23.

RECOMMENDED TEST EQUIPMENT:

AC/DC Digital Voltmeter (hip- Model 3450A)

Variable Attenuator (hip- Model 3551D)

For 75-ohm systems:

50-ohm to 75-ohm Adapter (see Figure 5-2)

25 ohm Compensating Resistor (see Figure 5-3)

NOTE

The following procedure is performed first for Channel A and then again for Channel B. The Channel A adjustments are located on the Channel A Log Amplifier Assembly, A7; the Channel B adjustments are located on the Channel B Log Amplifier Assembly, A23.

a. Connect the Variable Attenuator between the OUTPUT (or ALT OUTPUT $\odot$) of the Synthesizer and the rear panel INPUT of the 3570A as shown in Figure 5-4.

b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE .. 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

c. Set the Variable Attenuator to 0 dB.

d. Set the Synthesizer to 0 dBm, 1 MHz.

e. For 50-ohm systems, proceed to Step f. For 75-ohm systems, perform the following:

1. Connect the 3570A Channel A OUTPUT, terminated in 75-ohm load, to the DVM. Set the DVM to measure ac volts.

2. Adjust the Synthesizer amplitude for a DVM reading of 0.2739 Vrms. Do not disturb the Synthesizer amplitude setting in the following steps.

3. Disconnect the DVM and reconnect the terminated Channel A OUTPUT to the Channel A INPUT.

f. Connect the DVM (ac function) to TP1 of the Log Amplifier.

g. Adjust R19 (0 dB ADJ) for a DVM reading of 1.2 Vrms.

h. Connect the DVM (dc function) to TP2 of the Log Amplifier.

i. Adjust R28 (SLOPE ADJ) for a DVM reading of $+ 2.75$ Vdc.

j. Adjust the front panel / MP ZERO control (A or B) for a reading of 00.00 dB on the front panel Amplitude display.

k. Set the Variable Attenuator to 80 dB.

l. Adjust R18 (100 dB ADJ) for a reading of $- 80.00$ dB on the front panel Amplitude display.

m. Set the Variable Attenuator to 50 dB.

n. Adjust R19 (0 dB ADJ) for a reading of $- 50.00$ dB on the front panel Amplitude display.

o. Set the Variable Attenuator to 0 dB.

p. Adjust R28 (SLOPE ADJ) for a reading of 00.00 dB on the front panel Amplitude display.

q. Repeat Steps m through p until readings of 50.00 dB and 00.00 dB (respectively) are obtained.

r. Set the Variable Attenuator to each setting listed in Table 5-6. At each attenuator setting, the 3570A amplitude reading should be within the tolerances listed in the table. If all readings are in tolerance, set the 3570A AMPLITUDE FUNCTION switch to B and repeat Steps f through r for Channel B. If any readings are marginal or out of tolerance, proceed to Step s.

s. Set the Variable Attenuator to the highest setting (minimum attenuation) that produces a marginal or out-of-tolerance reading. If the attenuator setting is between 0 dB and 50 dB, perform Steps t through x; if not, proceed to Step y.

t. Adjust R19 (0 dB ADJ) for an in-tolerance reading.

u. Set the Variable Attenuator to 0 dB. Adjust R28 (SLOPE ADJ) for a reading of 00.00 dB.

- v. Set the Variable Attenuator as in Step s.
- w. Repeat Steps t through v until the reading that was marginal or out of tolerance is well within tolerance.
- x. Repeat Step r.
- y. Adjust R1R (100 dB ADJ) for an in-tolerance reading.
- z. Set the Variable Attenuator to 0 dB. Adjust R2R (SLOPE ADJ) for a reading of 00.00 dB.
- aa. Set the Variable Attenuator as in Step s.
- bb. Repeat Steps y through aa until the reading that was marginal or out of tolerance is well within tolerance.
- cc. Repeat Step r.

Table 5-6. Amplifier Adjustments.

Attenuator Setting	Test Tolerance
0 dB	0 dB $\pm$ 0.05 dB
10 dB	10 dB $\pm$ 0.15 dB
20 dB	20 dB $\pm$ 0.15 dB
30 dB	30 dB $\pm$ 0.3 dB
40 dB	40 dB $\pm$ 0.3 dB
50 dB	50 dB $\pm$ 0.3 dB
60 dB	60 dB $\pm$ 0.3 dB
70 dB	70 dB $\pm$ 0.4 dB
80 dB	80 dB $\pm$ 0.4 dB
90 dB	90 dB $\pm$ 0.8 dB
100 dB	100 dB $\pm$ 0.8 dB

Δ2 8-4. Change number 2 for serial numbers 11251A00245 and below. Paragraphs affected by this change are 4-13, 4-14, 5-63, 5-64 and Figure 7-11. (Backdated schematic for this change is Figure 8-1.) The paragraphs affected are as follows:

4-13. The Input Amplifier is a low noise, broadband amplifier circuit which provides gain (X2) and impedance conversion between the input connector and the Reference Attenuator. The Input Amplifier is comprised of an input amplifier stage (Q1), a differential driver stage (Q2 through Q4), a complementary-symmetry output stage (Q5, Q6) and an integrator (U2). The input amplifier (Q1) is a low noise field-effect transistor which, having a high input impedance, insures a minimum loading effect on the input signal. The input circuit is protected against overloads exceeding 2.4 V p-p by the limiter circuit consisting of CR1, CR2 and associated circuitry. The complementary-symmetry output stage provides a low output impedance and supplies the power required to drive the following low impedance stages. Overall gain, stability, and linearity is maintained by negative feedback from the junction of R27 and R28 through R31 to the source of FET Q1. Added stability is provided by dc feedback from the output of the Reference Attenuator through integrator U2 to the gate of Q1. The purpose of this feedback is to maintain 0 Vdc at the input of the following mixer stage.

4-14. Reference Attenuator. The Reference Attenuator is a pi attenuator pad consisting of resistors A1R32 through A1R35 and relay A1K1. Relay A1K1 is controlled by the

logic circuit formed by U1 which, in turn, is controlled by bits 3 and 4 of the PS Register in the digital section (PS3, PS4). The condition of bits PS3 and PS4 is determined by the MAX/REF INPUT VOLTAGE (Range) setting. With Range switch set to the 1 V position, relay K1 is energized and the Reference Attenuator introduces 13.01 dB of attenuation (50-ohm systems) or 11.25 dB of attenuation (75-ohm systems). The impedance of the attenuator network in 75-ohms, making the full scale output voltage represent 0 dBm (0.2236 V rms 50-ohm systems or 0.2739 V rms 75-ohm systems) when the network is terminated in 75 ohms by the following Input Mixer stage. With the Range switch set to the 0 dBm or 0.1 V rms position, relay K1 is de-energized, removing the attenuator network from the circuit. This leaves only the 75 ohm output resistor, R32 and the terminated output voltage is equal to the voltage at the INPUT connector. The diode limiter circuit consisting of CR13 through CR16 protects the following Input Mixer stage from overloads greater than 2.4 V p-p.

5-63. High Frequency Phase Adjustments. (For instruments equipped with 03570-66531, 03570-69531, 03570-66528, or 03570-69528 Input Amplifier Boards only. See Section V, Paragraph 5-61 for instruments equipped with 03570-66551, 03570-69551, 03570-66558, or 03570-69558 Input Amplifier Boards.)

5-64. These adjustments set the Input Amplifiers (A1 and A17) and the I.O. Buffer, A9, for optimum (flat) phase vs. frequency response.

- a. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
BANDWIDTH 10 Hz
PHASE REFERENCE A

- b. Set the Synthesizer for an output of 0 dBm, 10 kHz.

- c. Adjust the front panel 10 Hz ϕ ZERO control for a phase reading of 00.00 degrees.

- d. Center A1R8 and A17R8 (RF PHASE ADJ).

- e. Set the Synthesizer frequency to 13 MHz.

- f. Adjust A9C6 (L.O. PHASE ADJ) for a phase reading as near 00.00 degrees as possible.

- g. If necessary, adjust the front panel 10 Hz ϕ ZERO control for a phase reading of 00.00 degrees.

- h. Set the 3570A LINE switch to OFF. Exchange the A and B Input Amplifiers, A1 and A17.

- i. Set the 3570A LINE switch to ON. Allow 30 seconds for the phase reading to stabilize.

- j. Record the phase reading: _____ degrees.

- k. Adjust A1R8 (RF PHASE ADJ) for a phase reading that is 3/4 of the reading recorded in Step j.

- l. Adjust A17R8 (RF PHASE ADJ) for a phase reading that is 1/2 of the reading recorded in Step j.

- m. Repeat Steps h and i.

- n. Set the Synthesizer frequency to 10 kHz.

o. Adjust the front panel 10 Hz ϕ ZERO control for a phase reading of 00.00 degrees.

p. Set the Synthesizer frequency to 13 MHz.

q. Adjust A9C6 (L.O. PHASE ADJ) for a phase reading as close to 00.00 degrees as possible. ($\pm 1^\circ$ is the specification, although $\pm .5^\circ$ or better should be realizable.)

r. Set the Synthesizer frequency to 1 MHz.

s. If necessary, adjust A9C6 (L.O. PHASE ADJ) for a phase reading of 0 ± 0.1 degrees. If this cannot be done or if the 13 MHz phase reading is no longer well within the $\pm 1^\circ$ phase error specification, perform Steps u through x. Otherwise, perform Step t.

t. Note the phase readings with the Synthesizer frequency set to 500 kHz, 1 MHz, 5 MHz, and 13 MHz. At each frequency the phase reading error from 00.00° should be well within the phase accuracy frequency response specifications listed in Table 1-1. If any of the readings are out of tolerance, repeat Steps b through i. Otherwise, the High Frequency Phase Adjustments are completed.

u. Adjust A9C6 (L.O. PHASE ADJ) such that the two sets of blades of the capacitor are "half-way" engaged.

v. Set the Synthesizer to a frequency of 1 MHz and 13 MHz. Note the polarity and magnitude of the phase error at each frequency.

1 MHz _____ 13 MHz _____

w. Select either A2C8* or A18C8* to bring both of these frequency points well within tolerance ($\pm .2^\circ$ for 1 MHz and $\pm 1^\circ$ for 13 MHz). Use the following information for the selection:

1. The typical value of each capacitor is 2 pF (chip Part No. 0150-0031).
2. Increasing the value of A2C8* will increase the phase reading. Decreasing the value of A2C8* will decrease the phase reading.
3. A18C8* has the opposite effect as A2C8*. Increasing the value of A18C8* will decrease the phase reading while decreasing it will increase the phase reading.

4. Use the following value of capacitors:

.68 pF	0150-0046
1.0 pF	0150-0029
1.5 pF	0150-0011
2.0 pF	0150-0031
2.2 pF	0150-0015
3.3 pF	0150-0022

x. Do Step i.

$\Delta 3$ 8-5. Change number 3 for serial numbers 1331 A00275 and below. Paragraph affected by this change will be 4-22 and Figure 7-12. (Backdated schematic for this change is Figure 8-2).

4-22. There are two adjustments on each Crystal Filter board: the 10 Hz ADJ. (C1) and the 100 Hz ADJ. (C6).

The 10 Hz ADJ. capacitor is adjusted for optimum symmetry of the filter skirts at the ± 3 dB points. The 100 Hz ADJ. capacitor is adjusted so that the center frequency is exactly 100 kHz.

$\Delta 4$ 8-6. Change number 4 for serial numbers 1331 A00575 and below.

Page 6-3. Delete A1C24*, 0150-0046, .68 pF 500 wvdc. Add A1C24, 0150-0011, 1.5 pF 500 wvdc.

Page 7-25/7-26. Change A1C24*, .68 pF to A1C24, 1.5 pF.

$\Delta 5$ 8-7. Change number 5 for serial numbers 1331 A00620 and below.

Page 6-29. Under A51 miscellaneous parts, change Part No. 1251-3751 to 1251-3300.

$\Delta 6$ 8-8. Change number 6 for serial numbers 1331 A00635 and below.

Page 6-29 Under A39 miscellaneous parts, change Part No. 1251-3751 to 1251-3300.

$\Delta 7$ 8-9. Change number 7 for serial numbers 1331 A00615 and below. Paragraphs affected by this change will be 5-61, 5-62, Table 6-1, and Figure 7-13. The backdated schematic for this change is Figure 8-5. The Paragraphs and Tables affected are as follows:

$\Delta 1$ 5-61. Log Amplifier Adjustments.

(For Instruments equipped with 03570-66555 or 03570-69555 Log Amplifier Boards only. See the 3570A manual backdating for instruments equipped with 03570-66535 or 03570-69535 Log Amplifier Boards).

$\Delta 1$ 5-62. The following adjustments establish the amplitude linearity of the A and B Log Amplifiers, A7 and A23.

RECOMMENDED TEST EQUIPMENT:

AC/DC Digital Voltmeter (chip Model 3450A)

Variable Attenuator (chip Model 355D)

For 75 - ohm systems:

50 - ohm to 75 - ohm Adapter (see Figure 5-3)

25 - ohm Compensating Resistor (see Figure 5-4)

NOTES

1. The following procedure is performed first for Channel A and then again for Channel B. The Channel A adjustments are located on Channel A Log Amplifier Assembly, A7; the Channel B adjustments are located on the Channel B Log Amplifier Assembly, A23.

2. This procedure is intended for use with Log Amplifiers that are known to be grossly out of adjustment. If the Log Amplifier is reasonably close to meeting specifications, perform only Steps 1 through 2 of this procedure.

3. The Log Amplifier Adjustment can be difficult unless a "physical feeling" for the adjustments is known. Figure 5-9(a) gives an approximate description of the effect each adjustment will have over the 100 dB range of the Log Amplifiers.

4. Log Amplifiers differ slightly among themselves in their characteristics over the 100 dB amplitude range. However, there are certain trends which are worth noting. Figure 5-9(a) shows a typical error plot of a Log Amplifier. A positive error means the amplifier is reading higher (-89 dB instead of -90 dB) than it should. Also included in Figure 5-9(b) are the instrument specifications over the same amplitude range and the adjustment specifications.

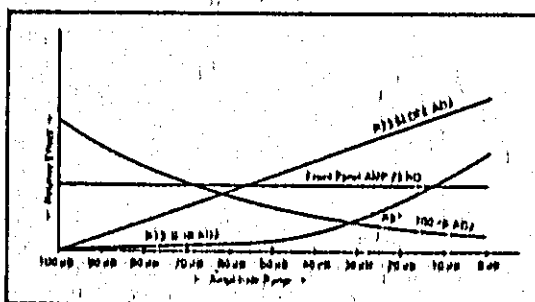


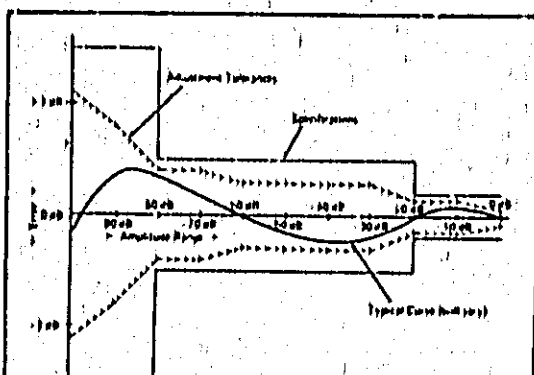
Figure 5-9(a). Relative Effect of Log Adjustments.

- a. Connect the Variable Attenuator between the OUTPUT (or ALT OUTPUT O) of the Synthesizer and the rear panel INPUT of the 3570A as shown in Figure 5-5.

- b. Set the 3570A controls as follows:

MAX/REF INPUT VOLTAGE 0 dBm
AMPLITUDE FUNCTION A
BANDWIDTH 10 Hz

- c. Set the Variable Attenuator to 0 dB and the Synthesizer to 0 dBm, 1 MHz.



Notice the peak error around -80 or -90 dB and the sharp drop off at 100 dB. Notice the less prominent trends at lower levels. By becoming aware of the trends of the particular log amplifier being adjusted and using the adjustments properly, the peak error points can be positioned on either side of the zero error line such that all points fall within specification, even though some may read high and others read low.

Figure 5-9(b). Typical Log Amplifier Curve.

- d. Adjust R13 (0 dB ADJ) clockwise until the pot starts clicking. Then turn R13 counterclockwise 4 turns.

- e. For 50-ohm systems, proceed to Step f. For 75-ohm systems, perform the following:

1. Connect the 3570A Channel A OUTPUT, terminated in 75-ohm load, to the DVM. Set the DVM to measure ac volts.

2. Adjust the Synthesizer amplitude for a DVM reading of 0.2739 V rms.

3. Disconnect the DVM and reconnect the terminated Channel A OUTPUT to the Channel A INPUT.

- f. Connect the DVM (dc function) to TP1 of the Log Amplifier.

- g. Adjust R23 (SLOPE ADJ) for a DVM reading of +5.00 Vdc.

- h. Adjust the front panel AMP ZERO control (A or B) for a reading of 00.00 dB on the front panel Amplitude display.

- i. Set the Variable Attenuator to 50 dB.

- j. The front panel amplitude display should read -55.00 ± .01 dB. If not, compute the error and double it. Record your results.

Example: Amplitude display of -49.50 dB
Error = -49.50 - (-55.00 dB) = +0.50 dB
0.50 dB x 2 = +1.00 dB

- k. Set the Variable Attenuator to 0 dB.

- l. Adjust R23 (SLOPE ADJ) for a front panel Amplitude display equal to the value recorded in Step j (± .01 dB).

- m. Adjust the appropriate front panel AMP ZERO control for a reading of 00.00 dB ± .01 dB.

- n. Repeat Steps i through m until readings of -50.00 dB and 00.00 dB (respectively) are obtained.

- o. Set the Variable Attenuator and Synthesizer to each setting listed in Table 5-6. At each setting, the 3570A amplitude reading should be within the tolerances listed in the table. If all readings are in tolerance, set the 3570A AMPLITUDE FUNCTION switch to B and repeat Steps f through o for Channel B. If any readings are marginal or out of tolerance, proceed to Step p.

Table 5-6. Amplifier Adjustments.

3570A Input	Attenuator Setting	Synthesizer [†] Setting	Tolerance
0 dBm	0 dB	0 dB	0 dB ± 0.05 dB
10 dBm	10 dB	0 dB	-10 dB ± 0.15 dB
20 dBm	20 dB	0 dB	-20 dB ± 0.15 dB
30 dBm	30 dB	0 dB	-30 dB ± 0.3 dB
40 dBm	40 dB	0 dB	-40 dB ± 0.3 dB
50 dBm	50 dB	0 dB	-50 dB ± 0.3 dB
60 dBm	10 dB	-60 dB	-60 dB ± 0.3 dB
70 dBm	20 dB	-60 dB	-70 dB ± 0.4 dB
80 dBm	30 dB	-60 dB	-80 dB ± 0.4 dB
90 dBm	40 dB	-60 dB	-90 dB ± 0.8 dB
100 dBm	50 dB	-60 dB	-100 dB ± 1.1 dB

[†]For 75-ohm systems, 0 dB corresponds to the level set up in Step e; -60 dB corresponds to a synthesizer setting 50 dB lower than that in Step e.

- p. Set the variable attenuator for -20 dB.

- q. Calculate the error in the reading and then multiply it by 3. Record your results.

Example: Attenuator set to +20 dB and a1 Amplitude display of +19.50 dB.
 Error = +19.50 dB - (+20.00 dB) = +00.50 dB
 $00.50 \text{ dB} \times 3 = +01.50 \text{ dB}$

r. Subtract the value calculated in q from what should be the correct reading. Record your result.

Example: +20.00 dB - (+01.50 dB) = +21.50 dB.

s. Adjust R13 (0 dB ADJ) for a front panel Amplitude display equal to that recorded in Step r (+21.50 dB).

t. Set the Variable Attenuator to 0 dB. Adjust R23 (SLOPE ADJ.) for a reading of 00.00 dB.

u. Repeat Step o.

v. Set the 3570A input to the lowest setting (most attenuation) that produces a marginal or out-of-tolerance reading.

w. Select R4*, R6*, and R8* for an in-tolerance reading. R4* will effect the +55 dB to +100 dB, R6* will effect the +60 dB to +100 dB, and R8* will effect the +80 dB to +100 dB ranges. Use the values given in Table 5-7. A lower value of resistance will increase the magnitude of the reading approximately .1 dB/1 k Ω . (An increase in magnitude means a decrease in the absolute value of the reading; +85 dB > +90 dB.) See Note 4.

x. Set the input to 0 dB. Adjust R23 (SLOPE ADJ) for a reading of 00.00 dB.

y. Repeat Step v through x until the reading that was marginal or out of tolerance is within tolerance (according to Table 5-6).

z. Repeat Step u.

Pages 6-7/6-8, Table 6-1.

Change:

A7C4, C11, C16, C20, C29, C32, and C34 to 0150-0084, Cap: Fxd .1 μ F 100 wyde.

A7L3 to 9100-1648, Coll: fxd 560 μ H 5%.

A7R2 to 0698-4486, Resistor 24.2 K 1% 1/8 W.

A7R4*, A7R6* to 0698-3158, Resistor 23.7 K 1% 1/8 W.

A7R8* to 0698-3484, Resistor 6.65 K 1% 1/8 W.

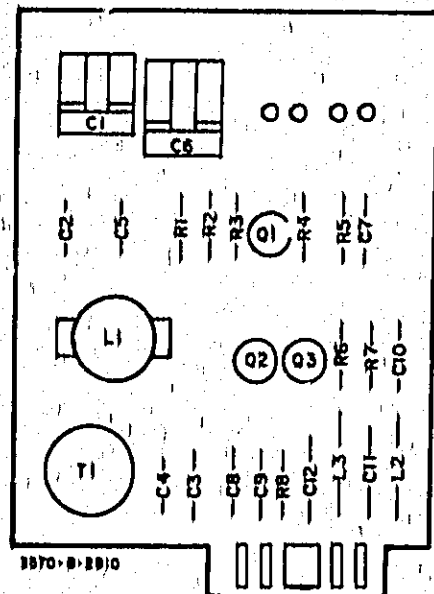
A7R16 to 0698-0084, Resistor 2150 1% 1/8 W.

A7R17 to 0698-1035, Resistor 1 M 5% 1/4 W.

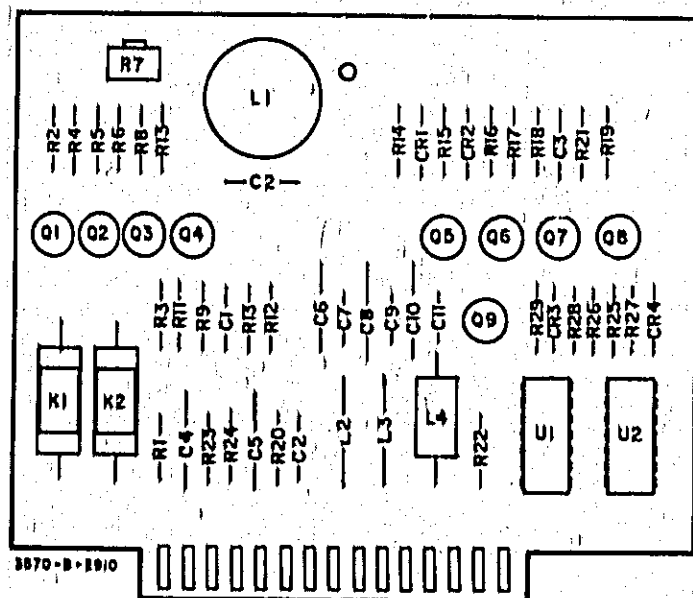
A7R20 to 0757-0440, Resistor 7.5 K 1% 1/8 W.

Delete:

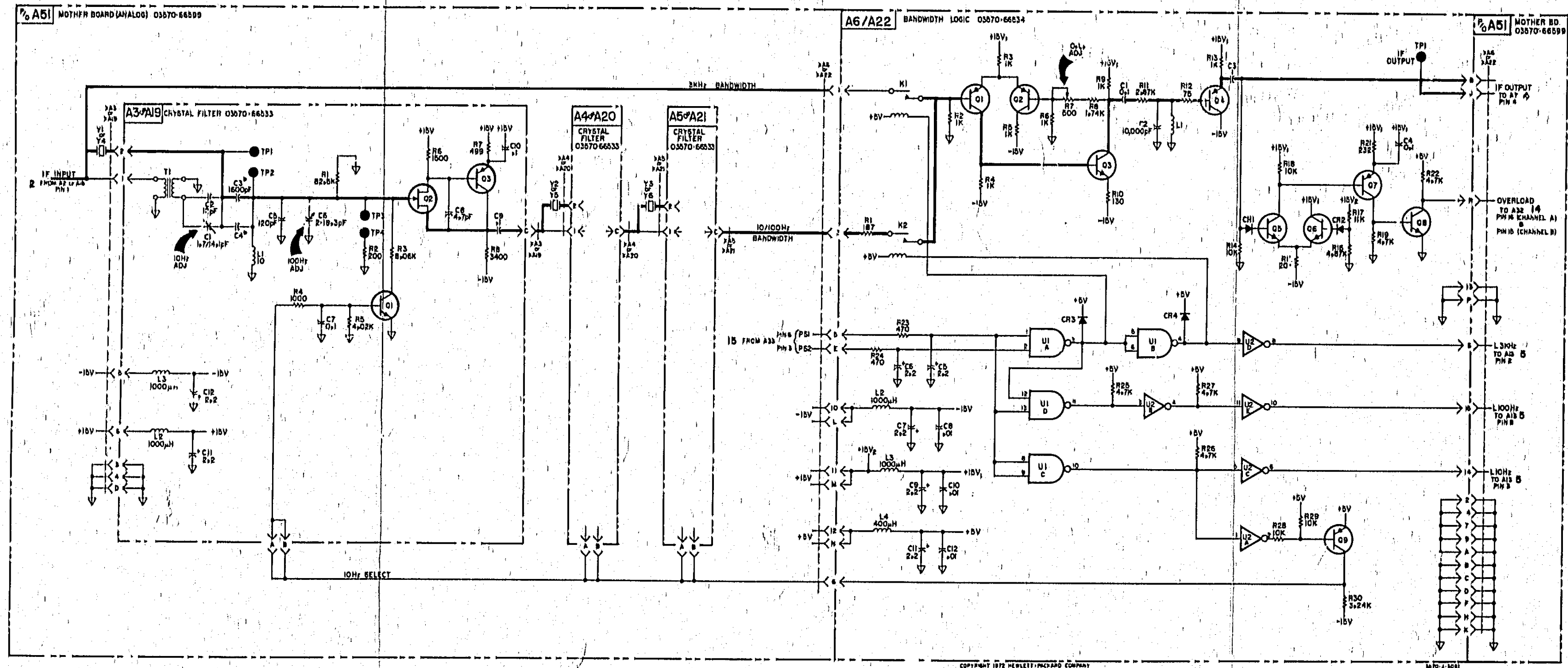
A7R34, R35, R36, R37, R38, and R39.



A3, A4, A5, A19, A20, A21
hp Part No. 03570-66533
Rev. A

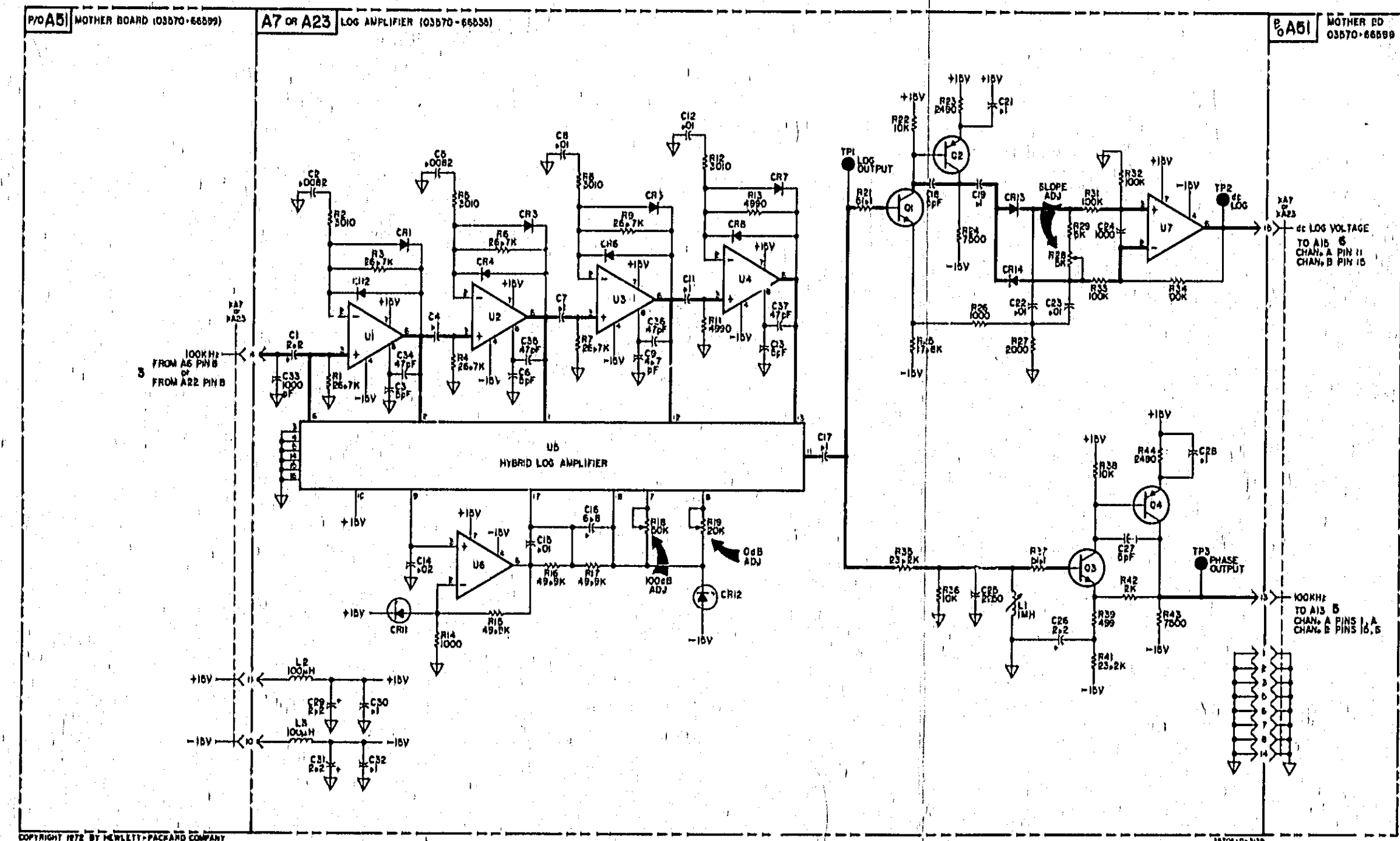
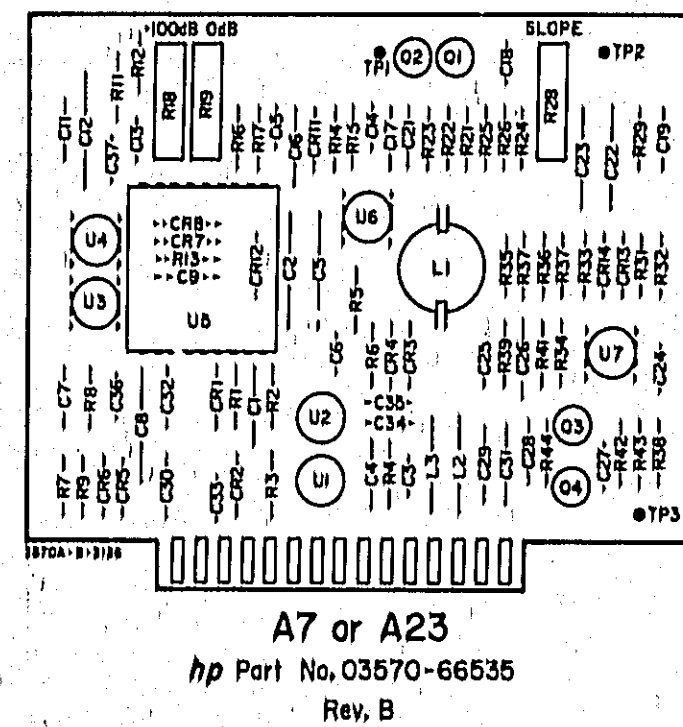


A6 and A22
hp Part No. 03570-66534
Rev. A



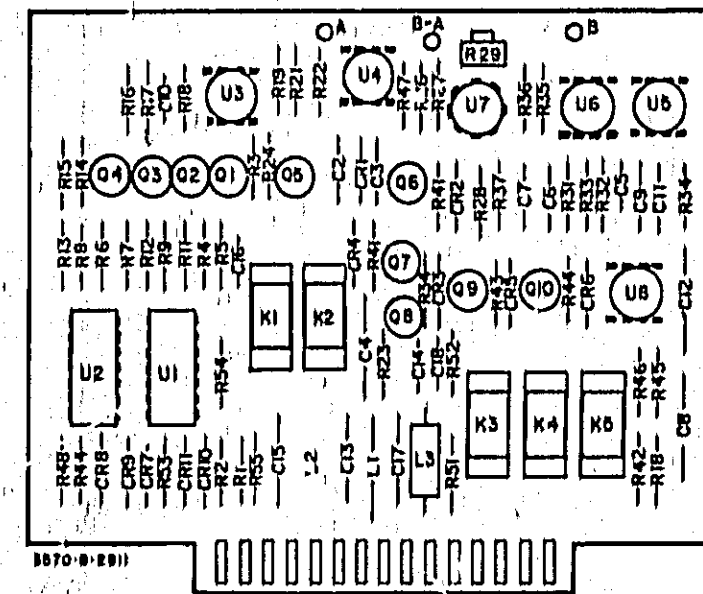
Backdating for instruments with serial numbers 1251A00275 and lower.

Figure 8-2. Crystal Filter (A3, A4, A5/A19, A20, A21) and Bandwidth Logic (A6/A22) Schematic and Component Location Diagrams.

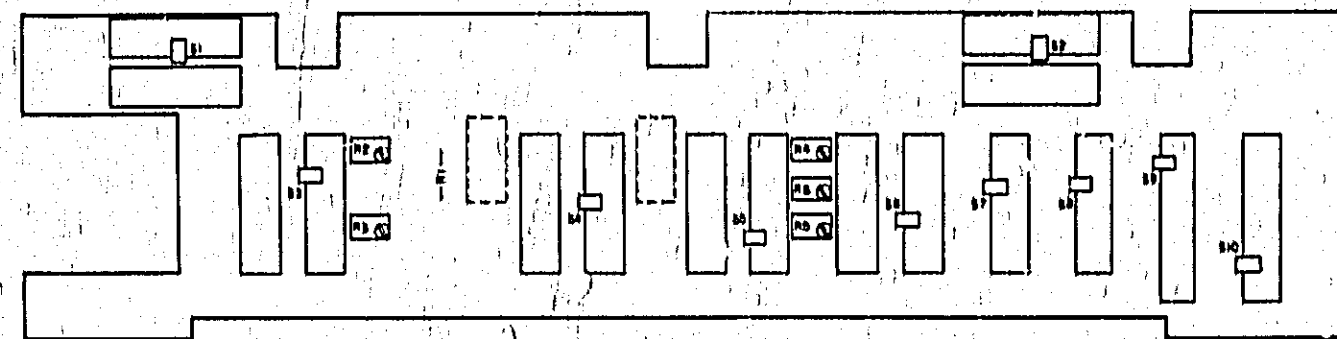


Backdating for instruments with serial numbers 1251AC0245 and lower.

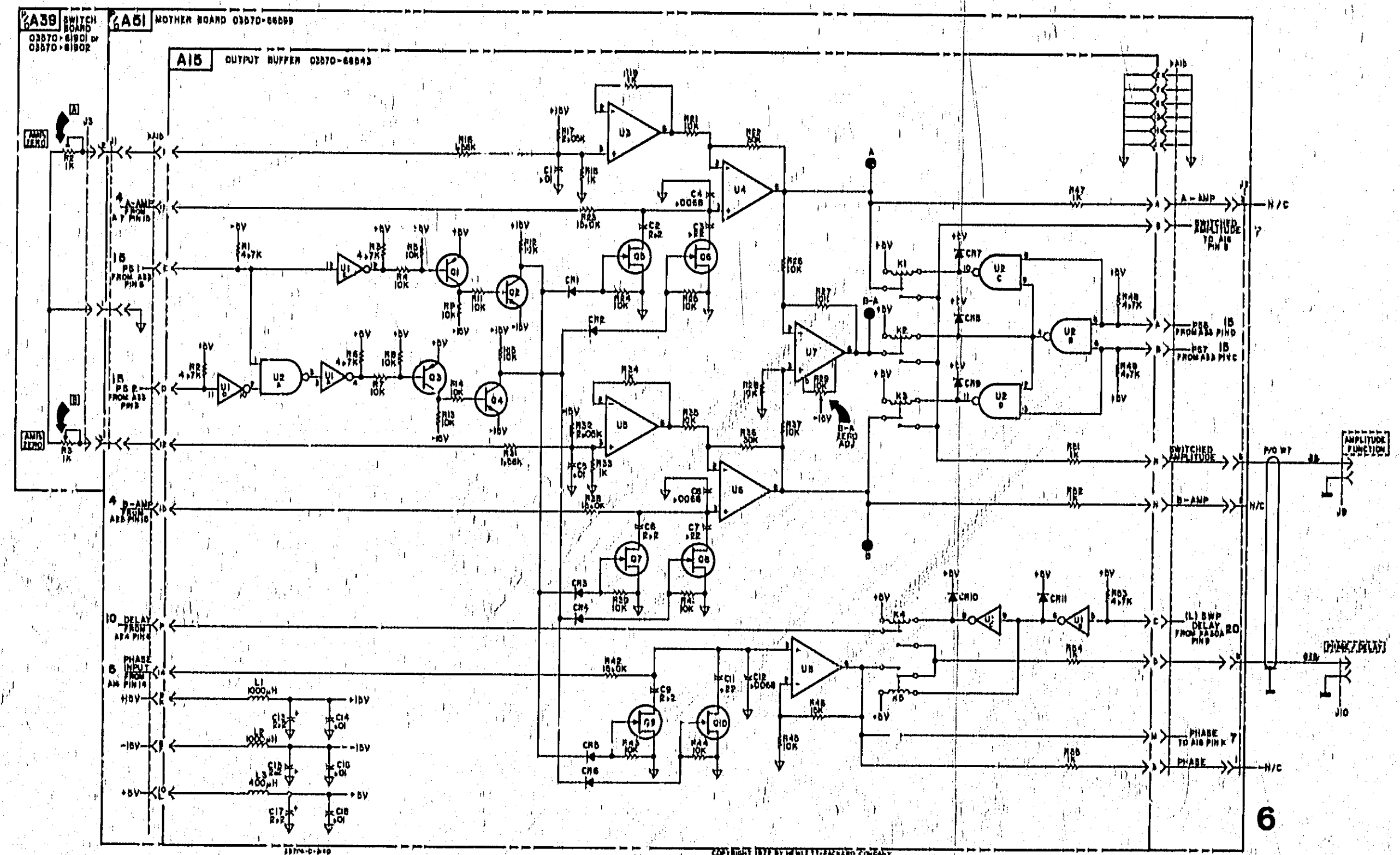
Figure 8-3. Log Amplifier (A7/A23) Schematic and Component Location Diagram.
8-9/8-10



A15
Part No. 03570-66543
Rev. A

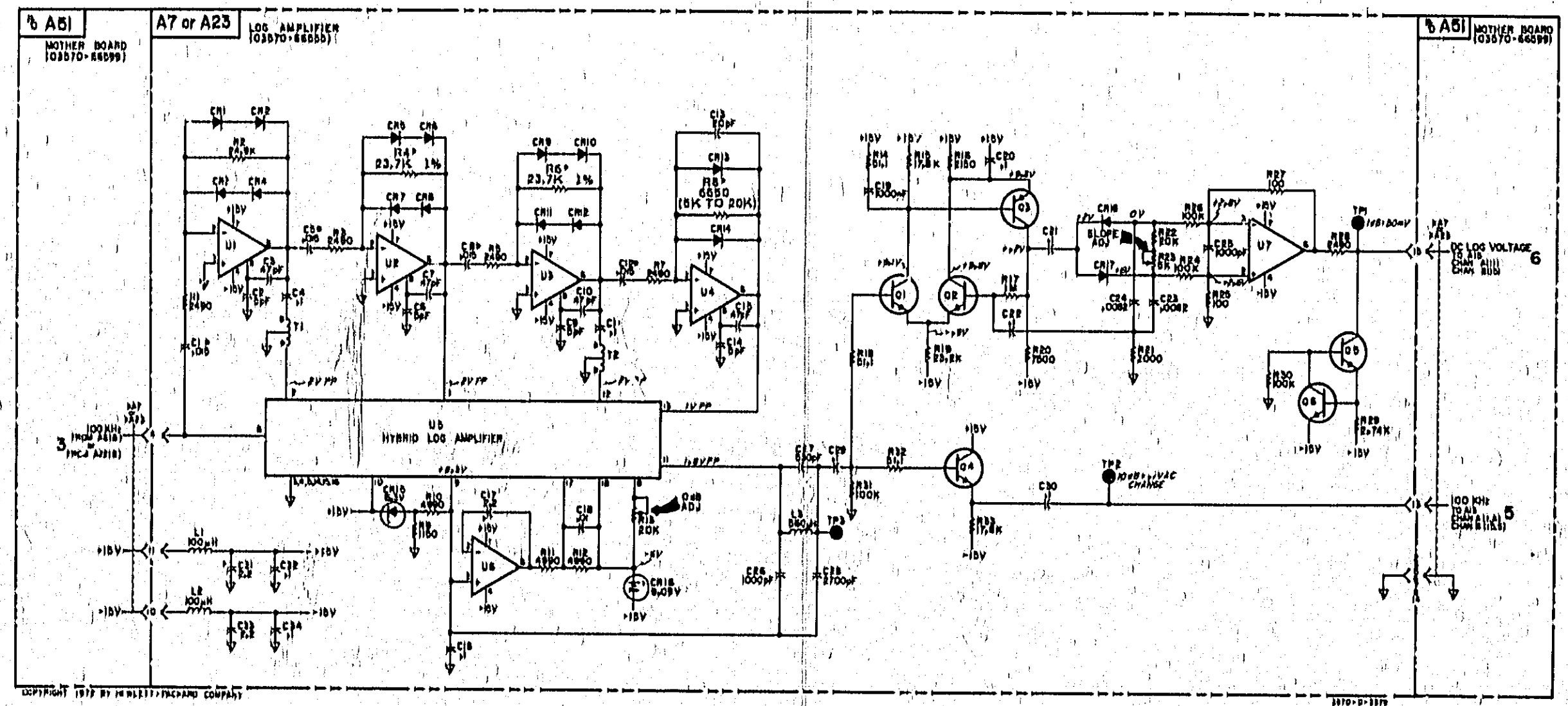
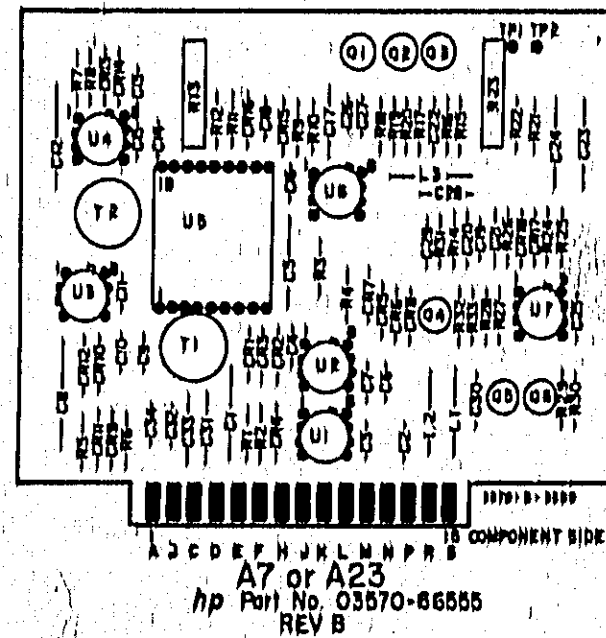


A39
hp Part No. 03570-61901
or 03570-61902 (SHOWN)
Rev. A



Backdating for instruments with serial numbers 1251A00245 and lower.

Figure 8-4. Output Buffer (A15) and P/O Front Panel Switch (A39)
Schematics and Component Location Diagrams.
8-11/8-12



Backdating for Instruments with Serial Numbers 1331 A00515 and lower.

Figure 8-5, Log Amplifier (A7/A23) Schematic and Component Location Diagram.

HP MANUAL CHANGES

hp- MODEL 3570A

NETWORK ANALYZER

Manual Part Number 03570-90015

► New or Revised Item

CHANGE NO. 1: affected serial numbers: 1331A01391 and greater - applicable to all model serial numbers.

Purpose: Allows substitution of available parts when standard value is unavailable.

Pages 6-22, 6-23, and 6-24; Table 6-3.

- a. CHANGE: A28L2 TO A29L2*
- b. CHANGE: A28L2 TO A29L2*
- c. CHANGE: A31L2 TO A31L2*
- d. CHANGE: A32L2 TO A32L2*
- e. ADD: Padding List

9100-3550 Coll-Fxd .62 μ H .05
9140-0394 Coll-Fxd .68 μ H
9100-3811 Coll-Fxd .78 μ H .5

CHANGE NO. 2: applicable to all model serial numbers

Page 1-8; Table 1-4.

- a. CHANGE: 11172B (50 Ω) TO 03570-61651 (50 Ω)
- b. CHANGE: 11172C (75 Ω) TO 03570-61662 (75 Ω)

Page 1-8; Table 1-3.

CHANGE:

"*Field Installation Kit -hp- 11176A"

TO:

"*Field Installation Kit -hp- Part Number 03570-80006"

CHANGE NO. 3: affected serial numbers: 1331A01311 and greater - applicable to all model serial numbers.

NOTE

This change should be made on any instrument that appears to have phase measurement problems when measuring under HP-IB control.

Page 6-15; Table 6-3.

CHANGE:

A16R1 0664-4721 Resistor 4.7 K 10% .25W CC
Tubular 01121 CB 4721

FROM:

A16R1 0757-0280 Resistor 1 K Ohm .01 .125 W F
Tubular 24546 C4-1/8-TO-1001-F

Page 7-51/7-52; Figure 7-26, Schematic (A16) 8. Change value of R1 from 4.7 K to 1.0 K.

CHANGE NO. 4: affected serial numbers: all

Page 6-31; Table 6-3.

- a. ADD: 3050-0604 2 ea. Stainless Steel Washer
- b. ADD: 5001-1952 1 ea. Insulator

CHANGE NO. 5: affected serial numbers: 1331A01881 and greater - applicable to all model serial numbers.

Page 6-30; Table 6-3.

CHANGE:

B1 3160-0256 1 Fan 28480 3160-0256

TO:

B1 03571-27401 1 Blower-Mach 28480 03570-27401

ADD:

03571-06871 1 Bracket 28480 03570-06871

NOTE

The fans are completely interchangeable; however the new fan (03571-27401) must be used when a new bracket (03571-06871) is used.

CHANGE NO. 6: affected serial numbers: 1331A01976 and greater - applicable to all model serial numbers.

Purpose: Increases the range of the offset adjustment circuit.

Page 6-18; Table 6-3.

CHANGE:

A24R15 0698-8175 Resistor 5M 2% .125 W F
Tubular 30883 GE10-1/8-TO5004-G

TO:

A24R15 0699-0024 Resistor 2.61M

Page 7-55/7-56; Schematic (A24) 18. Change value of R15 from 5M to 2.61 M.

CHANGE NO. 7: affected serial numbers: 1331A01243 and greater - applicable to all model serial numbers.

Purpose: Increase range of the offset adjustment circuit.

Page 6-16 and 6-17; Table 6-3.

CHANGE:

A16R8, A16R13, A16R38, A16R46

FROM: 0698-8175 Resistor 5M 2% .125 W

TO: 0699-0085 Resistor 2.61M Ohm

Page 7-53/7-54; Schematic (A16) 7. Change value of R8, R13, R38, and R56 from 5M to 2.61M.

CHANGE NO. 8: affected serial numbers: 1331A01281 and greater applicable to all model serial numbers.

Page 6-8; Table 6-3.

CHANGE:

A7R4* Δ 7 TO A7R4 Δ 7
A7R6* Δ 7 TO A7R6 Δ 7

31 October 1980

Supplement B for 03570-90015

CHANGE:

A7R22 0698-6690 Resistor 20 K, 1%, 125 W P
Tubular 19701 MFAC1/8-T9-2002.0

TO:

A7R22 0698-7979 Resistor 22.1 K 1%

Page 6-18; Table 6-3,

CHANGE:

A16R12, A16R15 TO A16R12*, A16R15*

ADD:

Padding List (R12* and R15*)

0698-6631 2.6 K

0698-6672 2.7 K

0698-7631 2.87 K

CHANGE NO. 8; affected serial numbers: 1331A01330 and smaller,

Page 6-28; Table 6-3,

CHANGE:

A04BU5-11 1990-0400 Photo Isolator

TO:

A04BU5-11 1990-0636 Isolator

CHANGE NO. 19; affected serial numbers: 1331A01331 and greater - applicable to all model serial numbers.

NOTE

Two circuit boards have been obsoleted and replaced by two boards which will ensure accurate data transmissions on the HP-IB bus.

03570-66579 (A34B) Replaces 03570-66569 (A34B)

03570-66583 (A36) Replaces 03570-66573 (A36)

The new boards are direct replacements for the old.

Page 7-4; Table 7-2.

CHANGE:

A04R 03570-66569 Isolated Input Buffer** 17

TO:

A04B 03570-66579 Isolator PC Assembly 17a

CHANGE:

A36 03570-66579 ASCII Output** 22

TO:

A36 03570-66583 ASCII PC Assembly 22a

NOTE

Make references, as you deem necessary, throughout your manual concerning Replaceable Parts, Component Locators, and Schematics for the new boards (66579, 66583).

DELETE

All references to the Isolated Hewlett-Packard Interface Bus being option 004; it is now standard.

Page 6-28; Table 6-3.

DELETE

A04A 03570-66568 and all its components.

Page 6-18; Table 6-3,

DELETE

A04A 03570-66568 and all its components.

Page 7-4; Table 7-2.

DELETE

A04A 0357-66568 Input Buffer.

Page 7-71/7-72.

DELETE

Figure 7-36, Input Buffer (A04A) Schematic and Component Location Diagram.

Page 7-69/7-70.

DELETE

All references made to schematic 16.

CHANGE NO. 1; applies to serial numbers 1331A-0103 and above.

DELETE

All reference to the offset and Limit Test Feature being option 002 or 003; this feature is now standard.

Page 7-4; Table 7-2

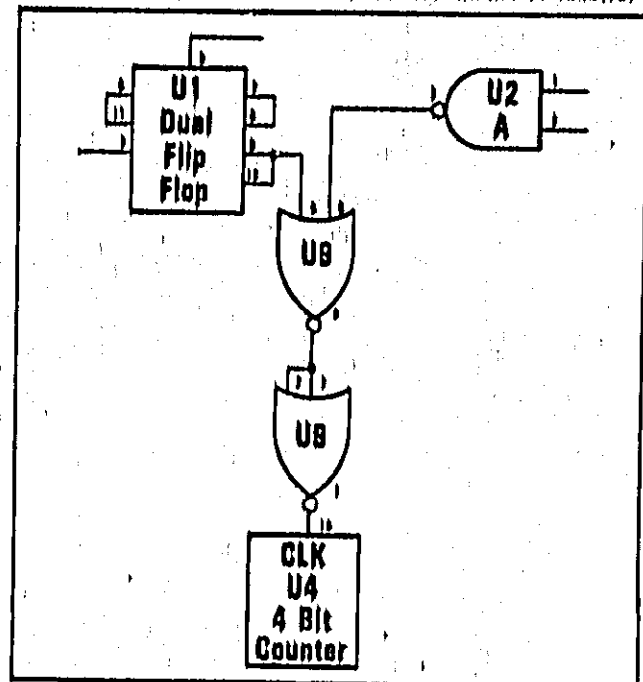
DELETE

The asterisk next to the A24, A30, and A31 boards. These boards are now standard—not option 002 or 003.

CHANGE NO. 12; applies to serial numbers 1331A-0103 and above.

PAGE 6/8 of Supplement B (yellow sheets).

Two NOR gates should be added to the schematics as follows:



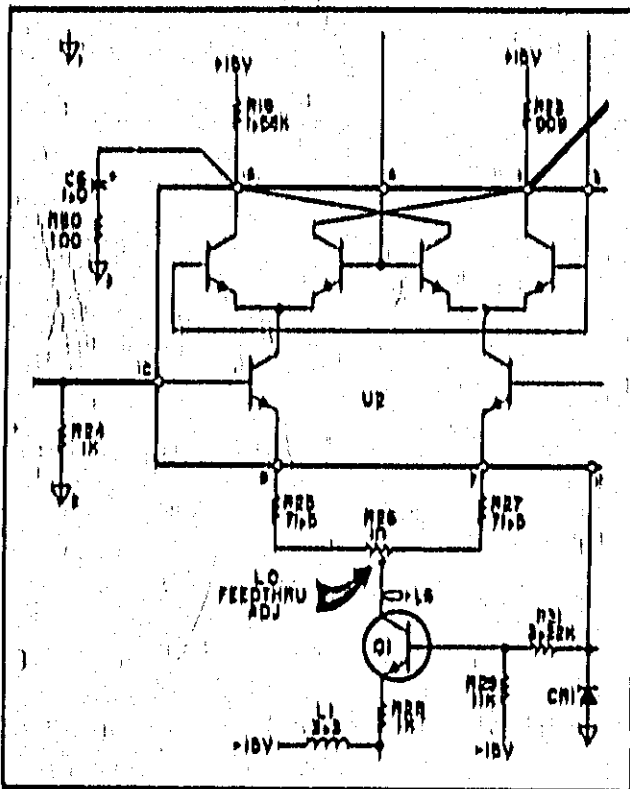
NOTE

This change is made to modify the clocking technique used to increment the counter. Previously, the counter would occasionally count 0, 2, 3, instead of 0, 1, 2, 3,.... This modification eliminates this problem.

CHANGE NO. 13, applies to serial numbers 1331A-01000 and above.

Page 7-43/7-44, Figure 7-21.

Add A2 (A1B for opt. 001) RFO as follows:



Page 8-5, Table 8-3

Add A2R50 0757-0401 Resistor 1000 1%.

NOTE

R50 has been added in series to stabilize ground currents on the board. Previously, this instability caused erratic phase measurements at amplitudes less than 70 dBm.

ERRATA

Page 7-43/7-44, Figure 7-22.

On the component locations for the A5 and A21 board as well as for the A3, A4, A19, and A20 board, reverse the locations for C3 and C4.

Page 8-5, Table 8-5.

Change the upper and lower limits for the Delay Measurement check to the following:

Lower Limits	Upper Limits
19.56 msec	20.44 msec
9.56 msec	10.42 msec
5.56 msec	6.41 msec
4.56 msec	5.41 msec
1.956 msec	2.044 msec
.956 msec	1.042 msec
.556 msec	0.6412 msec
.456 msec	0.541 msec
.1956 msec	.2044 msec
.0956 msec	.1042 msec
.0556 msec	.0641 msec
.0456 msec	.0541 msec
19.56 μsec	20.44 μsec
9.56 μsec	10.42 μsec
5.56 μsec	6.41 μsec
4.56 μsec	5.41 μsec
1.956 μsec	2.044 μsec
.956 μsec	1.042 μsec
.556 μsec	0.641 μsec
.456 μsec	0.541 μsec

A17a

Figure 7-36a, Isolated Input Buffer (A34B) Schematic.

Page 5/6

22a

Figure 7-41a, ASCII Output Assembly (A36) Schematic.

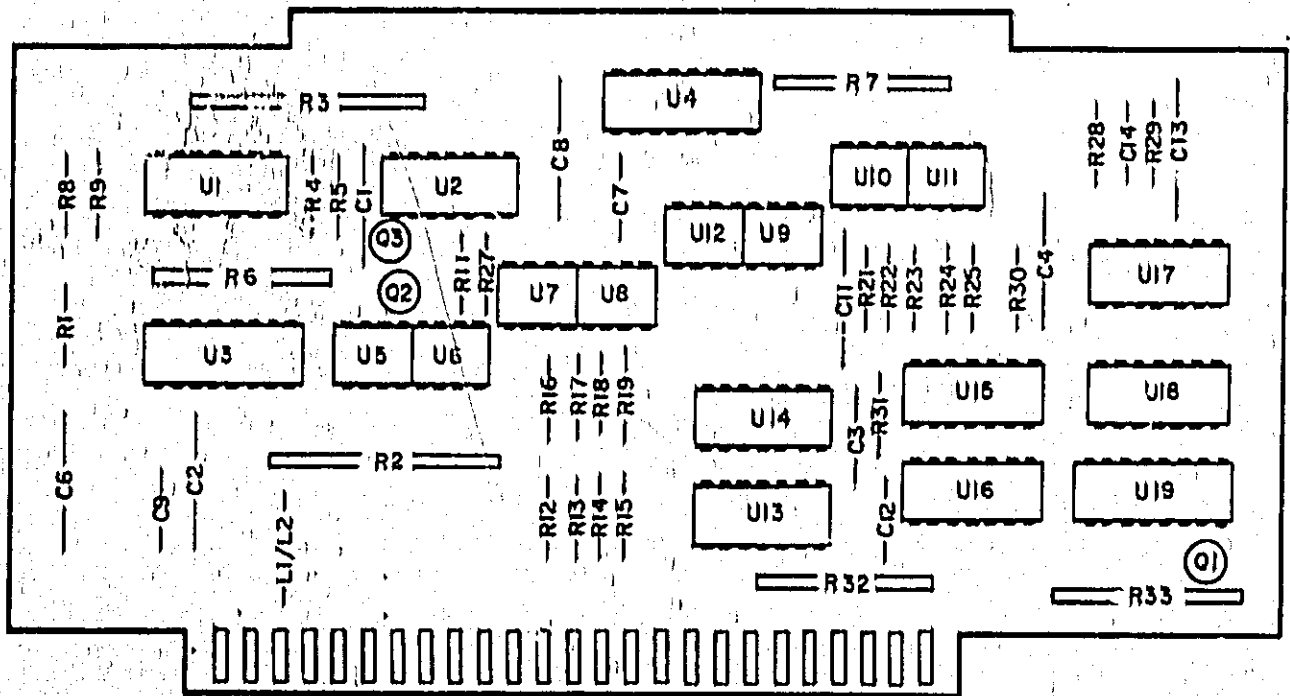
Page 7/8

Table 6-1, Replaceable Parts

REFERENCE DESIGNATOR	Part NO.	TQ	DESCRIPTION	MFR.	MFR. PART NO.
A34B	03570-88579		PC ASSY, ISOLATOR	28480	03570-88579
	0403-0221	1	EXTR. PC BD BLK POLYC. 07 BD THKN5	28480	0403-0221
	1200-0473	4	SOCKET, IC 16-CONT DBL STPP DIP, SLD	28480	1200-0473
	4040-0747	1	EXTR. PC BD GRA POLYC .082 BD THKN5	28480	4040-0747
C1	0160-0160	1	CAPACITOR, FXD 8200PF $\pm 10\%$ 200WVDC	56289	282P82282
C2	0160-0228	1	CAPACITOR, FXD 1500PF $\pm 10\%$ 15VDC	56289	150D226X901502
C3	0160-0298	1	CAPACITOR, FXD 1500PF $\pm 10\%$ 200WVDC	56289	282P15292
C4	0160-0168	1	CAPACITOR, FXD 5500PF $\pm 10\%$ 200WVDC	56289	282P55282
C5	0160-0228	1	CAPACITOR, FXD 22UF $\pm 10\%$ 15VDC	56289	150D226X901502
C7	0160-0084	1	CAPACITOR, FXD .1UF $\pm 80\%$ -20% 100WVDC	28480	0150-0084
C8	0160-0228	1	CAPACITOR, FXD 22UF $\pm 10\%$ 15VDC	56289	150D226X901502
C9	0160-0084	1	CAPACITOR, FXD $\pm 80\%$ -20% 100WVDC CER	28480	0150-0084
C11	0160-0228	1	CAPACITOR, FXD 22UF $\pm 10\%$ 15VDC	56289	150D226X901502
C12	0160-0084	1	CAPACITOR, FXD .1UF $\pm 80\%$ -20% 100WVDC	28480	0150-0084
C13	0160-0228	1	CAPACITOR, FXD 22UF $\pm 10\%$ 15VDC	56289	150D226X901502
C14	0160-0084	1	CAPACITOR, FXD .1UF $\pm 80\%$ -20% 100WVDC	28480	0150-0084
L1	9170-0884	1	CORE, MAG; SHIELDING BEAD, .138 OD .047	02114	56-580-85/4A6
L2	9170-0884	1	CORE, MAG; SHIELDING BEAD, .138 OD .047	02114	56-580-85/4A6
Q1	1854-0215	1	TRANSISTOR NPN 51 PD-350 MW FT = 300MHZ	02037	2N3904
Q2	1853-0020	1	TRANSISTOR PNP 51 PD-300MW FT = 150MHZ	28480	1853-0020
Q3	1854-0215	1	TRANSISTOR NPN 51 PD-350MW FT = 300MHZ	02037	2N3904
R1	0688-4455	1	RESISTOR 536 OHM 1% .125W F TUBULAR	24546	C4-1/4-TO-536R-F
R2	1810-0041	1	CIRCUIT; P.I.V.; NON-REPLACABLE IN	28480	1810-0041
R3	1810-0041	1	CIRCUIT; P.I.V.; NON-REPLACABLE IN	28480	1810-0041
R4	0757-0407	1	RESISTOR 200 OHM 1% .125W F TUBULAR	24546	C4-1/8-TO-201-F
R5	0757-0428	1	RESISTOR 1.62K 1% .125W F TUBULAR	24546	C4-1/8-TO-1621-F
R6	1810-0184	1	NETWORK, RES 9-SID 4.7K OHM X8	05524	C5P08C07-472J
R7	1810-0184	1	NETWORK, RES 9-SID 4.7K OHM X8	05524	C5P08C07-472J
R8	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R9	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R11	0683-3325	1	RESISTOR 3.3 K 5% .25W TC = $-400/+700$	01607	CB3325
R12	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R13	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R14	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R15	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R16	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R17	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R18	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R19	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R21	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R22	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R23	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R24	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R25	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R26	0683-2715	1	RESISTOR 270 OHM 5% .25W CC TUBULAR	01121	CB2715
R27	0683-5625	1	RESISTOR 5.6K 5% .25W FC TC = $-400/+700$	01607	CB5625
R28	0683-4725	1	RESISTOR 4.7K 5% .25W FC TC = $-400/+700$	01607	CB4725
R29	0683-5625	1	RESISTOR 5.6K 5% .25W FC TC = $-400/+700$	01607	CB5625
R30	0683-5625	1	RESISTOR 5.6K 5% .25W FC TC = $-400/+700$	01607	CB5625
R31	0757-0283	1	RESISTOR 2K 1% .125W F TC = 0 ± 100	03292	C4-1/8-TO-2001-F
R32	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R33	1810-0136	1	NETWORK, RES 10-SIP MULTI-VALUE	28480	1810-0136
	1810-0136	1	NETWORK, RES 10-SIP MULTI-VALUE	28480	1810-0136
U1	1820-0307	1	IC DCTL HEX	01688	SN15836N
U2	1820-0637	1	IC DCTL SN74 13 N SCHMITT TRIGGER	01295	SN7413N
U3	1820-0668	1	IC BFR TTL NON-INV HEX 1-INP	01688	SN7407N
U4	1820-0668	1	IC BFR TTL NON-INV HEX 1-INP	01688	SN7407N
U5	1890-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U6	1890-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U7	1890-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U8	1890-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U9	1890-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U10	1890-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U11	1890-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355

Table 6-1. Replaceable Parts (Cont'd)

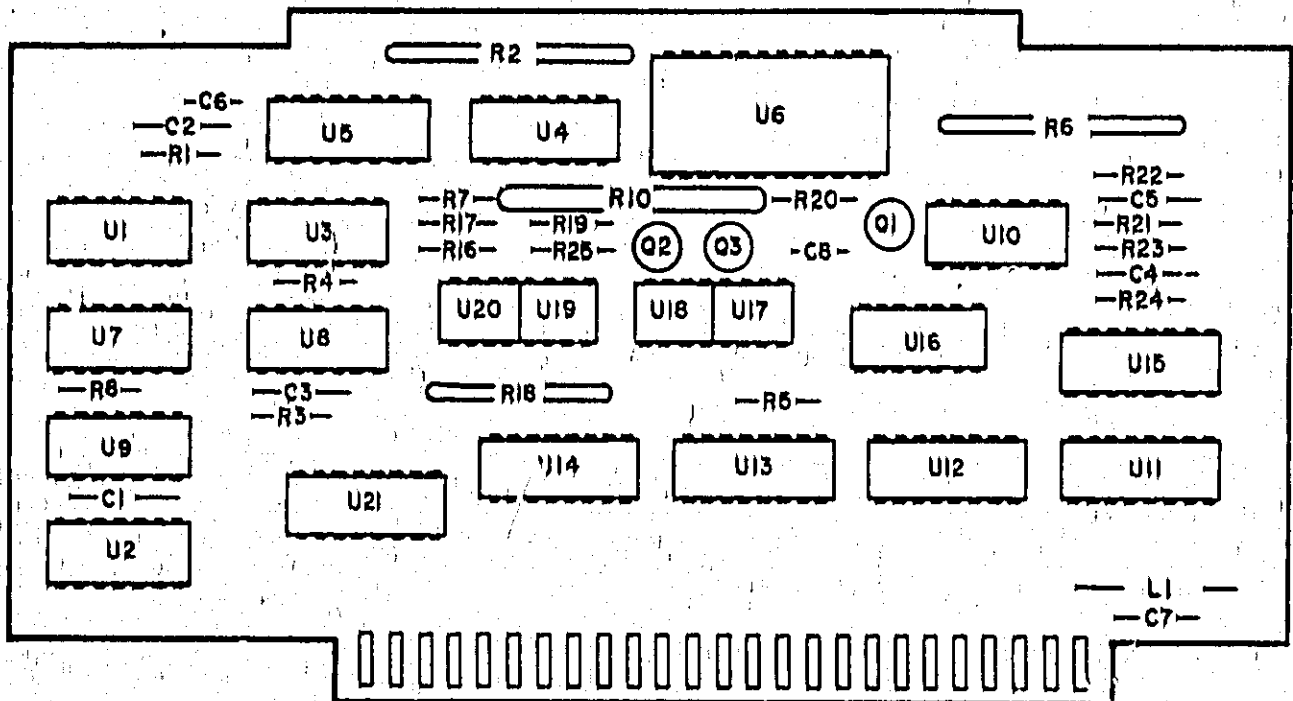
REFERENCE DESIGNATOR	hip- PART NO.	TQ	DESCRIPTION	MFR.	MFR. PART NO.
U12	1820-0444	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=25MA	01542	6N136
U13	1820-0054	1	IC; DGTL; GATE	01295	5N7400N
U14	1820-0054	1	IC; DGTL; GATE	01295	5N7400N
U15	1820-0261	1	IC DGTL 5N74 121 N MULTIVIBRATOR	01295	5N74121N
U16	1820-0307	1	IC DTL HEX	01698	5N15835N
U17	1820-0174	1	IC DGTL 5N74 04 N INVERTER	01295	5N7404N
U18	1820-1188	1	IC GATE TTL LS NAND QUAD 2-INP	01698	5N74LS03N
A36	03570-66583	1	PC ASSY-ASCU	28480	03570-66583
	1200-0473	2	SOCKET-IC 16-CONT DBL STRP DIP-SLDR	28480	1200-0473
	1200-0474	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
	1250-0658	1	SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0658
	4040-0748	1	EXTR PC BD BLK POLYC .062-BD-THKNS	28480	4040-0748
	4040-0749	1	EXTR PC BD BRN POLYC .062-BD-THKNS	28480	4040-0749
C1	0160-0153	1	CAPACITOR-FXD 1000PF +-10% 200WVDC	56289	292P10292
C2	0160-3847	1	CAPACITOR-FXD .01UF +100 -0% 25WVDC	28480	0160-3847
C3	0160-0258	1	CAPACITOR-FXD 1500PF +-10% 200WVDC	56289	292P15292
C4	0180-0197	1	CAPACITOR-FXD 2.2UF +-10% 20VDC TA	56289	150D225X8020A2
C5	0180-0309	1	CAPACITOR-FXD 4.7UF +-20% 10VDC TA	56289	150D475X0010A2
C6	0160-3622	1	CAPACITOR-FXD .1UF +80 -20% 100WVDC	28480	0160-3622
C7	0160-3847	1	CAPACITOR-FXD .01UF +100 -0% 25WVDC	28480	0160-3847
C8	0160-3622	1	CAPACITOR-FXD .1UF +80 -20% 100WVDC	28480	0160-3622
L1	9170-0894	1	CORE; MAG; SHIELDING BEAD; .138 OD .047	02114	56-590-65/4A6
L2	9170-0894	1	CORE; MAG; SHIELDING BEAD; .138 OD .047	02114	56-590-65/4A6
L3	9100-1618	1	COIL; FXD; MOLDED RF CHOKE; 5.6UH 10%	24226	15/561
C1	1854-0354	1	TRANSISTOR NPN SI TO-62 PD=360MW	28480	1854-0354
Q2	1854-0215	1	TRANSISTOR NPN SI PD=360MW FT=300MHZ	02037	2N3904
Q3	1854-0215	1	TRANSISTOR NPN SI PD=360MW FT=300MHZ	02037	2N3904
R1	0684-1031	1	RESISTOR 10K 10% .25W CC TUBULAR	01121	CB1031
R2	1810-0041	1	CIRCUIT; PSIV; NON-RPRABLE IN	28480	1810-0041
R3	0683-3315	1	RESISTOR 330 OHM 5% .25W CC TUBULAR	01121	CB3315
R4	0683-2215	1	RESISTOR 220 OHM 5% .25W CC TUBULAR	01121	CB2215
R5	0684-1031	1	RESISTOR 10K 10% .25W CC TUBULAR	01121	CB1031
R6	1810-0055	1	CIRCUIT; PSIV; NON-RPRABLE IN	28480	1810-0055
R7	0684-1031	1	RESISTOR 10K 10% .25W CC TUBULAR	01121	CB1031
R8	0683-2725	1	RESISTOR 2.7K 5% .25W FC TC=-400/+700	01607	CB2725
R10	1810-0259	1	NETWORK-RES 9-SIP 300.0 OHM X8	05524	CSP09C07-301J
R18	1810-0164	1	NETWORK-RES 9-SIP 4.7K OHM X8	05524	CSP09C06-472J
R19	0683-4725	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01607	CB4725
R20	0684-4721	1	RESISTOR 4.7K 10% .25W FC TC=-400/+700	01607	CB4721
R21	0757-0442	1	RESISTOR 10K 1% .125W F TUBULAR	24546	C4-1/8-TO-1002-F
R22	0696-4502	1	RESISTOR 64.9K 1% .125W F TUBULAR	24546	C4-1/8-TO-6482-F
R23	0699-3572	1	RESISTOR 60.4K 1% .125W F TUBULAR	5299	C4-1/8-TO-6042-F
R24	0757-0446	1	RESISTOR 15K 1% .125W F TUBULAR	24546	C4-1/8-TO-1502-F
R25	0683-4725	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01607	CB4725
U1	1820-0077	1	IC DGTL 5N74 74 N FLIP-FLOP	01295	5N7474N
U2	1820-0054	1	IC; DGTL; GATE	01295	5N7400N
U3	1820-0141	1	IC; DGTL; GATE	04713	MC3001P
U4	1820-0099	1	IC DGTL 5N74 93 N COUNTER	01295	5N7493N
U5	1818-2101	1	ROM	28480	1818-2101
U6	1820-0715	1	IC DGTL 5N74H 106 N FLIP-FLOP	01295	5N74H106N
U7	1820-0269	1	IC DGTL 5N74 03 NGATE	01295	5N7403N
U8	1820-0261	1	IC DGTL 5N74 121 N MULTIVIBRATOR	01295	5N74121N
U9	1820-0328	1	IC; DGTL; GATE	01295	5N7402N
U10	1820-0174	1	IC DGTL 5N74 04 N INVERTER	01295	5N7404N
U11	1820-0622	1	IC DGTL 5N74 151 N MULTIPLEXER	01295	5N74151N
U12	1820-0622	1	IC DGTL 5N74 151 N MULTIPLEXER	01295	5N74151N
U13	1820-0622	1	IC DGTL 5N74 151 N MULTIPLEXER	01295	5N74151N
U14	1820-0622	1	IC DGTL 5N74 151 N MULTIPLEXER	01295	5N74151N
U15	1820-0616	1	IC; DGTL; MULTIPLEXER	07263	9322DC
U16	1820-0668	1	IC BFR TTL NON-INV HEX 1-INP	01698	5N7407N
U17	1990-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U18	1990-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U19	1990-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U20	1990-0577	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA	01542	5082-4355
U21	1858-0023	1	IC LIN CA3081 TRANSISTOR ARRAY	02735	CA3081



A34B

Part No. 03570-66579

Rev. A



A36

hp Part No. 03570-66583

Rev. A

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