

HP 44711A / 44712A / 44713A

24 / 48-Channel Single Ended High Speed FET Multiplexer Component Module



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Table 10-8 HP 44711A/44712A/44713A Specifications

HP 44711A 24 Channel High Speed FET Multiplexer

Maximum Switch Rates: 5500 channels/second (from back-plane)*
100000 channels/second (from ribbon cable)

Maximum Input Voltage: Rear and back-plane inputs protected to 16 V peak (input impedance decreases above 12 V due to internal protection circuitry). With analog back-plane disconnected from multiplexer, the back-plane voltage can go up to 42 V peak.

Maximum Input Current: 1 mA non-inductive per channel

Input Impedance:

Impedance	Terminals	
	High to Low	High or Low to Chassis
Power On Resistance (Ω)	$>10^8$	$>10^8$
Power Off Resistance (Ω) V_{in} 10 V	>1000	>1000
Power Off Resistance (Ω) V_{in} >10 V	>200	>200
Max. Capacitance (pf) at 1MHz	200	200

Closed Channel Path Resistance: 3.1 k Ω for either High or Low Inputs considered separately

Bandwidth: 1.0% flatness at 20 kHz, -3 dB Bandwidth at 200 kHz (50 Ω source, 1 M Ω termination)

Crosstalk: -50 dB at 10 kHz, -35 dB at 100 kHz (channel-to-channel, 50 Ω source, 1 M Ω termination)

Maximum Offset Voltage: 15 μ V at 0 to 28 $^{\circ}$ C
185 μ V at 28 to 55 $^{\circ}$ C
(offset voltage between High and Low)

Maximum Bias Current: ± 5 nA DC at 0 to 28 $^{\circ}$ C
 ± 15 nA DC at 28 to 55 $^{\circ}$ C
(Current sourced by High or Low to Chassis into Input Terminals or back-plane, with isolation relays closed)

± 1 nA DC at 0 to 55 $^{\circ}$ C
(Current sourced by High or Low to Chassis into back-plane, with isolation relays open)

Maximum Wire Size: 16 AWG

Table 10-8 HP 44711A/44712A/44713A Specifications (Cont.)

HP 44712A 48 Channel Single Ended High Speed FET Multiplexer

Maximum Switch Rates: 5500 channels/second (from back-plane)*
100000 channels/second (from ribbon cable)

Maximum Input Voltage: Rear and back-plane inputs protected to 16 V peak (input impedance decreases above 12 V due to internal protection circuitry). With analog back-plane disconnected from multiplexer, the back-plane voltage can go up to 42 V peak.

Maximum Input Current: 1 mA non-inductive per channel

Input Impedance: High to Low, $>10^8 \Omega$, $\leq 200 \text{ pF}$ (at 1 MHz)
Power Off Resistance, $>1000 \Omega$ ($V_{in} \leq 10 \text{ V}$)
Power Off Resistance, $>200 \Omega$ ($V_{in} > 10 \text{ V}$)

Closed Channel Path Resistance: 3.1 k Ω for either High or Low
Inputs considered separately

Bandwidth: 1.0% flatness at 20 kHz, -3 dB Bandwidth at 200 kHz
(50 Ω source, 1 M Ω termination)

Crosstalk: -50 dB at 10 kHz, -35 dB at 100 kHz
(channel-to-channel, 50 Ω source, 1 M Ω termination)

Maximum Offset Voltage: 15 μV at 0 to 28 $^{\circ}\text{C}$
185 μV at 28 to 55 $^{\circ}\text{C}$
(offset voltage between High and Low)

Maximum Bias Current: $\pm 5 \text{ nA DC}$ at 0 to 28 $^{\circ}\text{C}$
 $\pm 15 \text{ nA DC}$ at 28 to 55 $^{\circ}\text{C}$
(Current sourced by High or Low to Chassis into Input Terminals or back-plane, with isolation relays closed)

 $\pm 1 \text{ nA DC}$ at 0 to 55 $^{\circ}\text{C}$
(Current sourced by High or Low to Chassis into back-plane, with isolation relays open)

Maximum Wire Size: 16 AWG

HP 44713A 24 Channel High Speed FET Mux with Thermocouple Compensation

Maximum Switch Rates: 5500 channels/second (from back-plane)*
100000 channels/second (from ribbon cable)

Table 10-8 HP 44711A/44712A/44713A Specifications (Cont.)

Maximum Input Voltage: Rear and back-plane inputs protected to 16 V peak (input impedance decreases above 12 V due to internal protection circuitry). With analog back-plane disconnected from multiplexer, the back-plane voltage can go up to 42 V peak.

Maximum Input Current: 1 mA non-inductive per channel

Input Impedance:

Impedance	Terminals	
	High to Low	High or Low to Chassis
Power On Resistance (Ω)	$>10^8$	$>10^8$
Power Off Resistance (Ω) $V_{in} 10\text{ V}$	>1000	>1000
Power Off Resistance (Ω) $V_{in} >10\text{ V}$	>200	>200
Max. Capacitance (pf) at 1MHz	200	200

Closed Channel Path Resistance: 3.1 k Ω for either High or Low Inputs considered separately

Bandwidth: 1.0% flatness at 20 kHz, -3 dB Bandwidth at 200 kHz (50 Ω source, 1 M Ω termination)

Crosstalk: -50 dB at 10 kHz, -35 dB at 100 kHz (channel-to-channel, 50 Ω source, 1 M Ω termination)

Maximum Offset Voltage: 15 μV at 0 to 28 $^{\circ}\text{C}$
185 μV at 28 to 55 $^{\circ}\text{C}$
(offset voltage between High and Low)

Maximum Bias Current: $\pm 5\text{ nA}$ DC at 0 to 28 $^{\circ}\text{C}$
 $\pm 45\text{ nA}$ DC at 28 to 55 $^{\circ}\text{C}$
(Current sourced by High or Low to Chassis into Input Terminals or back-plane, with isolation relays closed)

$\pm 1\text{ nA}$ DC at 0 to 55 $^{\circ}\text{C}$
(Current sourced by High or Low to Chassis into back-plane, with isolation relays open)

Maximum Wire Size: 16 AWG

Ref. Junction Compensation Accuracy: 0.1 $^{\circ}\text{C}$ (over 18 to 28 $^{\circ}\text{C}$ operating temperature)

Max Temperature Difference Across Isothermal Module: 0.2 $^{\circ}\text{C}$

*Applies to HP 3852As with firmware revision 2.0 or above.

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