Avtec Systems PCI-6200

Monarch PCI Frame Synchronizer / Telemetry Simulator

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MONARCH-E

PCI Frame Synchronizer/Telemetry Simulator with Reed-Solomon Encoder/Decoder

Features

- Supports both CCSDS and IRIG formats
- Bidirectional synchronous serial I/O at up to 25 Mbps
- 32-bit PCI interface provides 133 MBps burst transfer rates
- Serial input performs frame synchronization, derandomization, deinterleaving, Reed-Solomon (RS) decoding and outputs data to PCI bus
- Serial output reads data from PCI bus and performs CRC encoding, RS encoding, interleaving, sync marker insertion, pseudo-randomization, and convolutional encoding
- Onboard frequency synthesizer with output frequency from 100 Hz to 25 MHz

Applications

- CCSDS/TDM Front-end Processor
- High Speed PCM Frame Synchronization
- CCSDS/TDM Simulator
- Command Uplink

Avtec's MONARCH-E provides 25 Mbps bi-directional performance on a PCI card

Overview

The MONARCH Frame Synchronizer/PCM Simulator is a PCI-based serial I/O card that supports both CCSDS (Conventional and Advanced Orbiting Systems) and time division multiplexed (TDM) telemetry and command formats.

The MONARCH-E Reed-Solomon (RS) encoder/decoder provides complete error detection and correction for each of the CCSDS-recommended grades of service for Advanced Orbiting Systems.

The MONARCH/MONARCH-E input channel accepts serial data and clock and outputs frame data to the PCI bus. The input channel performs frame synchronization, derandomization, CRC error detection, deinterleaving, RS error detection and correction, time-tagging, and quality annotation. The input channel transfers annotated frame data to PC memory for further processing.

The MONARCH/MONARCH-E output channel reads frame data from PC memory via the PCI bus and outputs serial data and clock at up to 25 Mbps. The output channel performs RS encoding, interleaving, CRC encoding, sync marker insertion, pseudo-randomization, and convolutional encoding.

Hardware

Serial Input Logic

For CCSDS telemetry, the serial input logic synchronizes to channel access data units and formats them for input to the Reed-Solomon (RS) Decoder. For TDM telemetry, the serial input logic bypasses the RS Decoder and outputs frame data directly to the PCI interface.

Reed Solomon Error Correction (RSEC)

The RSEC chip is an LSI Logic ASIC that was designed by engineers at NASA's Goddard Space Flight Center. The RSEC chip accepts parallel data from the Serial Input Logic. It performs RS (255,223) VCDU error correction with interleaving depth from 1 to 8, RS (10,6) VCDU header error correction, and real-time quality generation and annotation. Shortened code blocks are also supported. The RSEC chip outputs corrected VCDUs with quality annotation to the PCI interface.

Reed-Solomon Encoder

The Reed-Solomon encoder is implemented in a Field Programmable Gate Array. The encoder accepts parallel data from the PCI interface and performs RS (255,223) VCDU encoding with an interleave depth from 1 to 8. Shortened code blocks are also supported. The RS encoder outputs interleaved code words to the Serial Output Logic.

Serial Output Logic

The serial output logic performs parallel to serial conversion, CRC encoding, pseudo-randomization, and convolutional encoding at up to 25 Mbps. It contains a programmable frequency synthesizer with an output range from 100 Hz to 25 MHz with 0.1 Hz resolution.

Specifications

Serial Input/Output Options

- Data rates to 25 Mbps
- TTL signals
  - 50 Ohm termination
  - BNC connectors
- RS-422 signals
  - 124 Ohm termination
    (62 Ohm to ground on each signal)
  - TRIAX connectors

Frame Synchronizer

- Programmable frame sync pattern up to 32 bits
- Programmable frame sync mask up to 32 bits
- Programmable sync pattern error threshold up to 15 bit errors
- Adaptive sync strategy with 0 to 7 check frames and 0 to 7 flywheel frames
- Programmable bit slip window from 0 to ± 3
- Auto-polarity detection and correction
- Frame length up to 8192 words/frame
- Programmable word size from 4 to 16 bits

De-Randomizer

- Exclusive OR received frame data following sync pattern with pseudo-random pattern given by $h(x) = x^8 + x^7 + x^5 + x^3 + 1$
- Shift register is initialized to all "ones" at the start of each frame

Reed-Solomon Error Correction

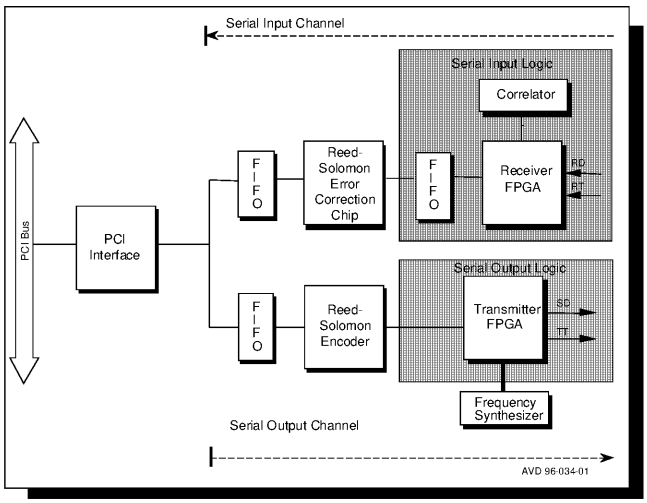
- CCSDS Reed-Solomon (255,223) error correction
- Support for shortened code blocks using "virtual" fill
- Interleave depth from 1 to 8
- CCSDS Reed-Solomon (10,6) header error correction
- Real-time quality generation and annotation for each VCDU

CRC Frame Error Control

- Computes frame error control field from received data using the polynomial $g(x) = x^{16} + x^{12} + x^5 + 1$
- Feed-back shift register is initialized to all "ones" at the start of each frame
- Programmable inclusion/exclusion of Attached Sync Marker

PCI Interface

- Based on PLX 9080
- 133 MBps data transfer rate
- Support for Plug and Play auto configuration



MONARCH-E Block Diagram

Telemetry Simulator

- Programmable clock and data polarity
- Frame length up to 8192 words/ frame
- Programmable word size from 4 to 16 bits
- Programmable output frequency from 100 Hz to 25 MHz with 0.1 Hz resolution

CRC Frame Error Control

- Computes frame error control field using the polynomial $g(x) = X^{16} + x^{12} + X^5 + 1$
- Feed-back shift register is initialized to all "ones" at the start of each frame
- Overlay computed CRC remainder into output frame
- Programmable inclusion/exclusion of Attached Sync Marker

Reed-Solomon Encoding

- CCSDS Reed-Solomon (255,223) encoding
- Support for shortened code blocks using "virtual" fill
- Interleave depth from 1 to 8

Pseudo-Randomizer

- Exclusive OR frame data following sync pattern with pseudorandom pattern given by $h(x) = x^8 + x^7 + x^5 + x^3 + 1$
- Shift register is initialized to all "ones" at the start of each frame

Convolutional Encoder

- Rate 1/2, constraint-length 7, convolutional code
- Connection vectors G1 =1111001 and G2 = 1011011
- Programmable parity order and parity inversion

These specifications are subject to change without notice.

AVTEC SYSTEMS

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