HP 18184A

V.35 Interface

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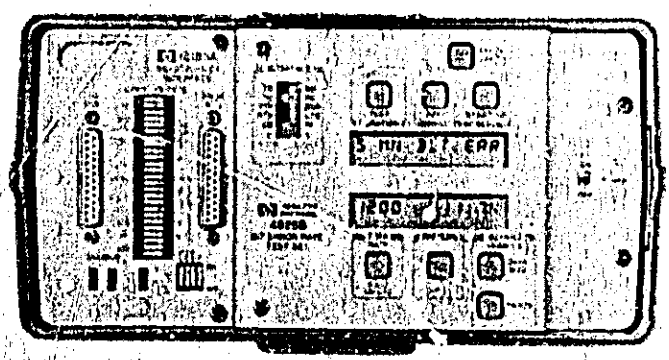
OPERATING AND SERVICE MANUAL

HP 4925B

Bit Error Rate Test Set and Accessories



HEWLETT PACKARD

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section I for general safety considerations applicable to this product.

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

For Warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designed by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance. No other warranty is expressed or implied. HP specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

EXCLUSIVE REMEDIES

The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products. For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

CW&A 4/84

Operating and Service Manual

HP 4925B
BIT ERROR RATE TEST SET

SERIAL NUMBERS

This manual applies to instruments with serial numbers prefixed 2501A and 2537A.

The HP 18185A and the HP 18194A are intended to be used ONLY with the HP 4925B. Plugging anything else into the HP 4925B, the HP 18185A, or the HP 18194A may cause equipment damage.

Manual Part No: 04925-90033
Microfiche Part No: 04925-90034

Printed: April 1986

WARNING

SAFETY

If this instrument is to be energized via an autotransformer for voltage reduction, make sure the common terminal is connected to the earthed pole of the power source.

BEFORE SWITCHING ON THIS INSTRUMENT, the protective earth terminals of this instrument must be connected to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by use of an extension cord (power cable) without a protective conductor (grounding).

Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuse holders must be avoided.

Whenever it is likely that the protection offered by fuses has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

GROUNDING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal can make this instrument dangerous. Intentional interruption is prohibited.

HIGH VOLTAGE

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Adjustments and service described herein are performed with power supplied to the instrument while protective covers are removed. Energy available at many points, if contacted, result in personal injury.

CAUTION

LINE VOLTAGE

BEFORE SWITCHING ON THIS INSTRUMENT, make sure instrument requirements match the voltage of the power source.

GROUNDING

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that all devices connected to this instrument are connected to the protective (earth) ground.

BEFOPE SWITCHING ON THIS INSTRUMENT, ensure that the line power (mains) plug is connected to a three-conductor line power outlet that has a protective (earth) ground. (Grounding one conductor of a two-conductor outlet is not sufficient.)

IEC SYMBOLS

The following is a list of key IEC symbols used by Hewlett Packard. All symbols are normally applied adjacent to the device requiring the symbol. They shall not be placed on removable parts likely to be detached or lost.

Instruction Manual symbol: If necessary, to preserve the apparatus from damage it is necessary for the user to refer to the instruction manual, then shall the apparatus be marked with this symbol (IEC 348,16a).

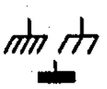
Terminal devices fed from the interior by live voltages that may be dangerous when connecting to or disconnecting from those devices shall be marked with the flash shown when the voltage exceeds 1 KV: The flash shall be red (IEC 348,16c).

Earth Terminals: If the use of this symbol for the protective earth terminal is not permitted by National Standards, it may be modified, for example, by being placed inside a circle (IEC 348;18a).

AC current (IEC 117-1, symbol No. 3).

DC current (IEC 117-1, symbol No. 2).

AC or DC current (IEC 117-1, symbol No. 8).



Frame or chassis connection. The hatching may be completely or partly omitted if there is no ambiguity. If the hatching is omitted, the line representing the frame or chassis shall be thicker (IEC 117-1, symbol No. 87).

A — Ampere (IEC 117-4, symbol No. 356).

V — Volt (IEC 117-4, symbol No. 357).

VA — Voltampere (IEC 117-4, symbol No. 358).

W — Watt (IEC 117-4, symbol No. 360).

Wh — Watthour (IEC 117-4, symbol No. 361).

VAh — Voltamperehour (IEC 117-4, symbol No. 362).

Hz — Hertz (IEC 117-4, symbol No. 365).

Contactor, normally closed. In order to avoid confusion with the symbol for a capacitor, the distance between the horizontal (as drawn here) lines should be at least equal to the length of those lines (IEC 117-3, symbol No. 215-2).

In addition the following describes the use of Warnings, Cautions and Notes used in HP Automatic Test System Manuals.

Warnings, cautions and notes. (All) Warnings and cautions shall precede the text to which each applies but notes may precede or follow applicable text depending on the material to be highlighted. Warnings, cautions, and notes shall not contain procedural steps nor shall they be numbered. When a warning, caution, or note consists of two or more paragraphs, the heading WARNING, CAUTION, NOTE, shall not be repeated above each paragraph. If it is ever necessary to precede a paragraph by both a warning and a note, or a caution and a note, etc, they shall appear in the sequence as noted, namely, warnings, cautions, notes. Such inserts in the text shall be short and concise and be used to emphasize important and critical instructions.

WARNING

An operating procedure, practice, etc, which, if not correctly followed, could result in personal injury or loss of life.

CAUTION

An operating procedure, practice, etc. which, if not strictly observed, could result in damage to, or destruction of, equipment.

NOTE: An operating procedure, condition, etc. which it is essential to highlight.

Health hazards precaution data. (All) When hazardous chemicals or adverse health factors, in the environment or use of the equipment cannot be eliminated, appropriate precautionary requirements shall be included.

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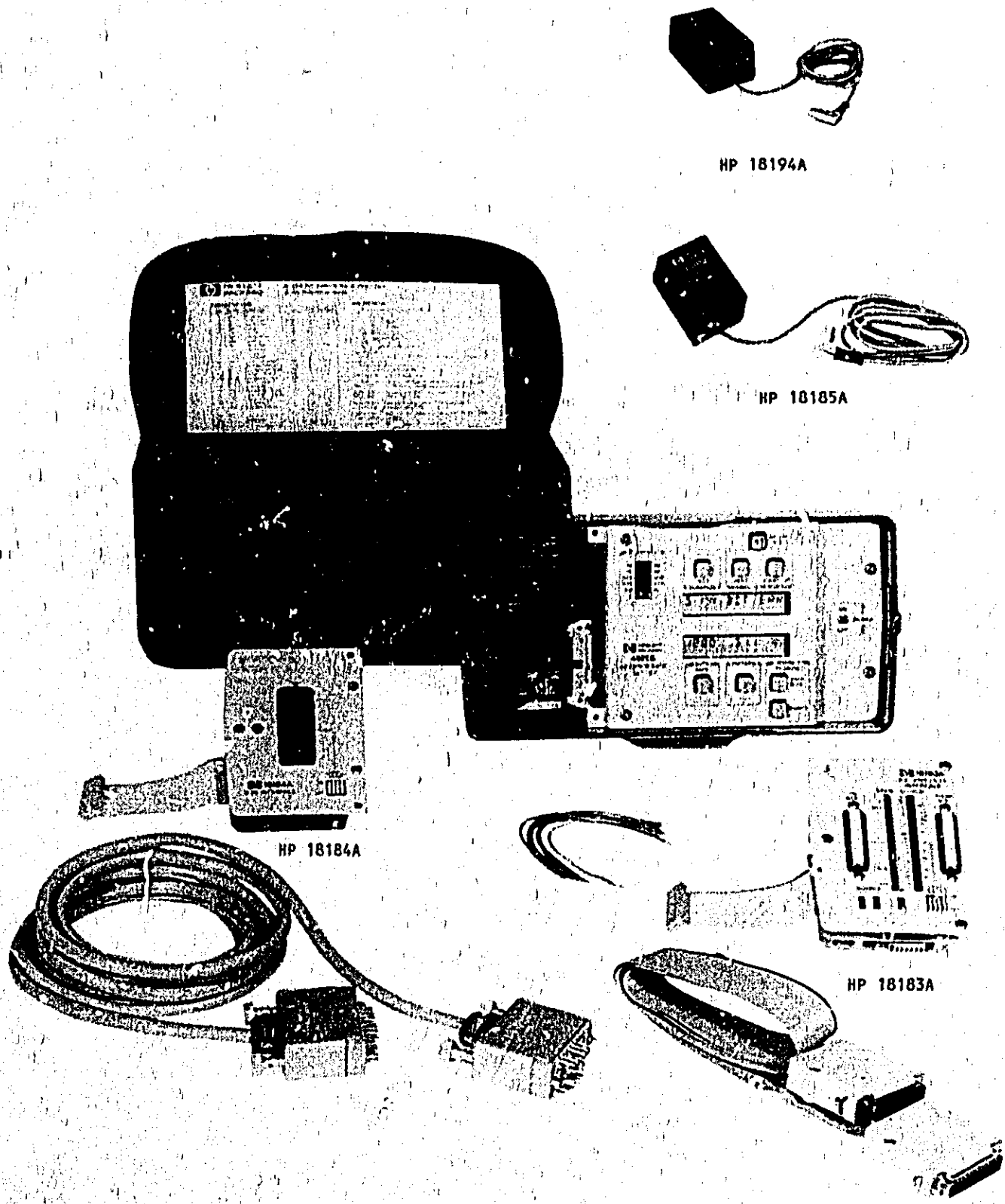


Figure 1-1. HP 4925B Bit Error Rate Test Set

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

This Operating and Service Manual provides information to install, operate, test, adjust, and service the Hewlett-Packard 4925B Bit Error Rate Test Set and accessories. This information is described in the following sections:

SECTION I, GENERAL INFORMATION, contains specifications, safety considerations, instrument identification, options, accessories, description of the instrument and recommended test equipment list.

SECTION II, INSTALLATION, gives instructions for initial inspection, preparation for use, and storage and shipment.

SECTION III, OPERATION, describes controls, indicators, and cables, gives detailed operating instructions, and describes software menus.

SECTION IV, PERFORMANCE TESTS, details procedures to verify instrument performance.

SECTION V, ADJUSTMENTS, the HP 4925B requires no adjustments.

SECTION VI, REPLACEABLE PARTS, provides information required to order all parts and assemblies.

SECTION VII, MANUAL CHANGES, contains information to backdate the manual for instruments with serial numbers earlier than listed on the Title Page.

SECTION VIII, SERVICE, provides service and troubleshooting information. This includes a Theory of Operation, Block Diagrams, Troubleshooting Procedures, Component Locators, and Schematics.

APPENDIX A, HP 4925B IN CCITT MODE, instructions to configure the HP 4925B for CCITT mode operation at turn on.

APPENDIX B, GUIDE TO INTERPRETING ANSI SYMBOLS, brief description of ANSI symbology with examples and a quick reference table.

APPENDIX C, HP 18183A RS-232C/V.24 INTERFACE, contains a description of the Instrument, Replaceable Parts, Theory of Operation, Troubleshooting, Component Locator, and Schematic

APPENDIX D, HP 18184A V.35 INTERFACE, contains a description of the Instrument, Replaceable Parts, Theory of Operation, Troubleshooting, Component Locator, and Schematic.

Appendix E, HP 18185 AC Power Supply, contains a description of the power supply, Replaceable Parts, Theory of Operation, Troubleshooting, Component Locator, and Schematic.

Appendix F, HP 18191A Rack Mount Kit, contains a description of the Rack Mount, Replaceable Parts, and Installation procedures.

Appendix G, HP 18194A AC Power Supply, contains a description of the power supply, Replaceable Parts, Theory of Operation, Troubleshooting, Component Locator, and Schematic.

1-2. SPECIFICATIONS

Instrument specifications are listed in Table 1-1. These are the performance standards or limits for this instrument.

Table 1-1. Bit Error Rate Test Set Specifications

DATA MODES:	Synchronous to 72 Kbps Asynchronous (unframed and unframed to 19.2 Kbps)	
DATA RATES:	75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 14.4K, 19.2K bps for asynchronous systems or synchronous systems where the HP 4925B provides the clock.	
BLOCK SIZES:	1000 bits or per CCITT recommendation V.53: select 511 bits when using a 511 PRBS pattern or select 2047 bits when using a 2047 PRBS pattern	
PATTERNS:	63, 511, or 2047 bit pseudo random binary sequence, FOX message	
DURATION OF TEST:	Number of bits - 10^3 through 10^9 bits Time - 5 min, 10 min, 15 min, continuous	
BIT ERROR TESTING:	simultaneous detection of bit errors, block errors, and error seconds (asynchronous error seconds, real time)	
PERCENT ERROR FREE SECONDS:	For acceptance testing in Dataphone Digital Service (DDS) or general verification of throughput Resolution - 0.1%	
ASYNCHRONOUS TERMINAL AND PRINTER TESTING:	Parity error analysis - received characters are analyzed for parity errors using odd or even parity	
	FOX message transmission	
	5 bit BAUDOT code	with odd, even, mark, space, or no parity
	6 bit EBCD code	with odd, even, mark, space, or no parity
	7 bit ASCII code	with odd, even, mark, space, or no parity. ASCII message is 80 characters long and includes character patterns for testing Dataspeed 40 printers
	8 bit EBCDIC code	with odd, even, or no parity

Table 1-1. Bit Error Rate Test Set Specifications (cont)

BIT ERROR TESTING IN CHARACTER ORIENTED NETWORKS:	Data levels - 5, 6, 7, or 8 bits per character Parity - odd, even, or no parity Stop Bits - 2 (5 bit code has 1.5 stop bits)		
REQUEST TO SEND - CLEAR TO SEND DELAY TIME MEASUREMENT	Auto repeating RTS-CTS Delay Time measurement operates in both active (asserts RTS) or passive (bridge monitor) modes		
	Delay Time:	Resolution:	1 msec
		Accuracy:	+-4% of reading
		Maximum Reading:	999 msec
START UP TESTING:	Three distinct start up tests verify the capability of half-duplex modems with auto-equalization circuits to compensate for analog line impairments		
POWER:	6 nine volt alkaline transistor batteries HP 18183A Interface, battery life exceeds 50 hours of non-continuous operation HP 18184A Interface, battery life is nominally 15 minutes. HP 18185A AC Power Module supplies continuous power for both interfaces HP 18194A AC Power Module supplies continuous power for 220 volts.		
TEMPERATURE RANGE:	Operating:	0° C to 50° C (32° F to 122° F)	
	Storage:	-40° C to 65° C (-40° F to 149° F)	
PHYSICAL SIZE:	Weight:	(with batteries) 1.5 kg (3lbs)	
	Height:	9.1 cm (3.6 in)	
	Length:	26.1 cm (10.3 in)	
	Depth:	12.6 cm (4.9 in)	

GENERAL INFORMATION

* Inject error function
* Detection and annunciation of clock slips and dropouts

1-3. SAFETY CONSIDERATIONS

When internal circuits are exposed, caution must be used. Observe all warnings and cautions marked on the instrument or listed in the procedures.

CAUTION

The internal circuits of this instrument are static sensitive. Refer to paragraph 8-7 for handling instructions.

1-4. SAFETY SYMBOLS

A complete list of safety symbols used in this manual is given on the page preceding the Table of Contents. Included are symbols and descriptions.

1-5. INSTRUMENT IDENTIFICATION

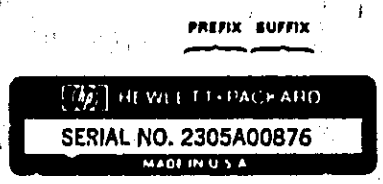


Figure 1-2. Typical Serial Number Plate

This instrument has a two part serial number stamped on a plate, located on the inside of the case cover. The first four digits and the letter are the serial number prefix. The last five digits form a sequential suffix, unique to each instrument. The manual applies directly to instruments with the same or lower serial number prefix as listed under SERIAL PREFIXES on the Title Page.

An instrument manufactured after the printing of this manual may have a serial prefix higher than listed on the Title Page. This indicates that the Bit Error Rate Test Set has been modified and a yellow Manual Change Sheet will accompany the manual to provide information to adapt the manual to the newer instrument.

In addition to change information, the Manual Change Sheet contains error corrections. To keep this manual as up to date as possible, Hewlett-Packard recommends that you periodically request the latest Manual Change Sheet. It is keyed to the manual's print date and part number, both appear on the Title Page.

1-6. DESCRIPTION

The HP 4925B Bit Error Rate Test Set is a portable digital test instrument. It fulfills test requirements for modem installation and maintenance as well as communications equipment installation in character and bit oriented networks. It also verifies customer premise installation of Digital Data System (DDS). Quick, proper identification of faulty network components is accomplished by data error analysis, start up tests, and complete interface testing.

The Bit Error Rate Test Set performs tests in seven catagories of digital network testing.

- Bit Error including block error and asynchronous error seconds
- Bit Error Tests in Character Oriented Networks
- Asynchronous Terminal and Printer Testing
- Request-To-Send - Clear-To-Send (RTS-CTS) Delay Time Test
- Start Up Testing
- Interface Tests
- Bit Error testing in the CCITT Environment

The RS-232C/V.24 and V.35 interfaces are located in Appendixes C and D respectively.

1-7. BIT ERROR TESTING

Bit error tests indicate the probability of bit errors in a stable, established communications channel and is an indication of the data link quality. Generally, a bit error occurs when a one is changed to a zero or vice versa. Bit error rate is calculated by the number of errors divided by the number of received bits in a given test. The HP 4925B performs six bit error tests and identifies when clock slips and dropouts occur.

Bit Error Rate — The number of bit errors during a test for a given number of received bits.

$$BER = \frac{\text{number of errors}}{\text{number of received bits in given test}}$$

Bit Error Count — The number of bit errors during a test for a given amount of time.

Block Error Rate — The number of blocks containing one or more bit errors during testing for a given number of received blocks A block is a subdivision of the serial bit stream with a fixed number of bits (1 block = 1000 bits, except for CCITT).

$$BLER = \frac{\text{number of blocks containing errors}}{\text{number of blocks received in given test}}$$

Block Error Count — The number of blocks that contain one or more bit errors during a test for a given amount of time.

Error Seconds — The number of one second time intervals that contain one or more bit errors.

Percent Error Free Seconds — Represents the percentage of the total number of 1 second time intervals that were error free. It is calculated after a test is completed.

Clock Slip — A synchronization error in which the input data has moved backwards or forwards in relation to the data stream clock.

Dropout — Dropout occurs when there are at least 16 consecutive clock cycles without a data transition.

1-10. BIT ERROR TESTING IN CHARACTER ORIENTED NETWORKS

In addition to performing the six Bit Error Tests described above, with this feature the HP 4925B can frame the output bit patterns as asynchronous data. It has true framed PRBS, odd, even, or no parity, and 5, 6, 7, or 8 bits per character. Some character oriented networks appear asynchronous to the user, but operate synchronous internally.

1-11. ASYNCHRONOUS TERMINAL AND PRINTER TESTING

The FOX message,

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.

checks the operation of terminals and printers. Each line of the FOX message is terminated with a carriage return and a line feed. The FOX message is transmitted using one of four data codes. The selected parity is appended to each character.

Table 1-2. Asynchronous Test Codes

LEVEL	CODE	PARITY	STOP BITS
5 Bit	BAUDOT	odd, even, mark, space, none	1.5
6 Bit	EBCD	odd, even, mark, space, none	2
7 Bit	ASCII	odd, even, mark, space, none	2
8 Bit	EBCDIC	odd, even, none	2

The 7 bit ASCII message is 80 characters long. It begins with the FOX message; however, the remaining characters are filled with the pattern below which fully exercises the printing mechanism in Dataspeed 40 printers.

AMZZMAAMZZMAAMZZMA...

1-12. PARITY ERROR ANALYSIS

Checking received asynchronous data for parity errors while transmitting the FOX message is the function of parity error analysis. Odd or even parity is calculated in received characters and compared with the expected parity.

1-13. REQUEST-TO-SEND - CLEAR-TO-SEND DELAY TIME

Request-To-Send - Clear-To-Send delay time measures the time delay between a Request-To-Send initiated by the Bit Error Rate Test Set and the Clear-To-Send response by a modem. Modems not meeting their specified speed capabilities decrease the network efficiency.

1-14. START UP TESTING

Start up testing checks the capability of modems with auto-equalization circuits to compensate for analog line impairments. The probability of error is greatest immediately after a modem takes control of a line. Each of the following tests sends a known, fixed length message which is transmitted immediately after the Bit Error Rate Test Set receives the Clear-To-Send signal from the modem.

End-to-End (ping pong)

End-to-End testing is used in half duplex, switched carrier networks. Testing is done on 100 exchanges of a 32 bit long random pattern message. Each HP 4925B test set displays the number or messages received with at least one error as well as the total number of messages received.

Loopback

Loopback checks configurations in which the modem is configured for switched carrier in one direction and constant carrier in the other, for example, multidrop networks. Testing is done on 100 transmissions of a 32 bit long random pattern message. The test set displays the number of messages received with at least one error as well as the total number of messages received.

208B Remote

208B Remote performs start up tests utilizing the remote test capability of the Bell 208B modem. Testing is done on 100 exchanges of either a steady MARK or a steady SPACE message. The Bit Error Rate Test Set displays the ratio of remote messages received with errors to total remote messages received and the ratio of local messages received with errors to the total number of local messaged received. Table 1-3 describes how the received message is interpreted.

Table 1-3. 208B Remote Test Results

Message Received by HP 4925B	208B Performance	
	Receiver	Transmitter
Mark	good	good
Mark with errors	good	error
Space	error	good
Space with errors	error	error

1-16. TESTING IN THE CCITT ENVIRONMENT

CCITT recommendations state that the block size for Bit Error testing should be 511 bits when sending 511 bit PRBS and 2047 bits when sending 2047 bit PRBS. This feature may be accessed in the HP 4925B by performing a shift operation before testing or by removing a jumper on one of the PC boards.

NOTE

Instructions for CCITT operation are located in Appendix A.

1-17. RELATED MANUALS

A quick reference guide describing the basic operating information for the HP 4925B is located in the carrying case.

1-18. OPTIONS

Options for the HP 4925B are listed below. All options should be requested at the time of the initial order.

OPTION	DESCRIPTION
001	Adds the carrying case
101	Adds the RS-232C/V.24 interface and cable
102	Adds the CCITT V.35 interface and cable and the AC Power Module (North America Only)
104	Adds the CCITT V.35 interface and cable and the AC Power Module (220 volts)
910	Adds the Operating/Service Manual

1-19. ACCESSORIES

The HP 4925B has several accessories. Accessories may be ordered anytime during the life of the product. For your convience, all accessory installation, operation, and service information is located in the appropriate Appendix.

ACCESSORY	DESCRIPTION
HP 18183A	RS-232C/V.24 interface and cable
HP 18184A	CCITT V.35 interface and cable
HP 18185A	AC Power Module (North America only)
HP 18191A	Rack Mount Kit
HP 18192A	Carrying Case
HP 18194A	AC Power Module (220V)

1-20. WARRANTY

The HP 4925B has a one year bench warranty as described on the inside of the front cover of the manual. Option 101, the HP 18183A and option 102, the HP 18184A also have one year bench warranties as described on the inside of the front cover of the manual, with the exception of the batteries. There are six 9 volt alkaline transistor type batteries, they are not covered by warranty. The AC Power Modules carry one year warranties.

NOTE

Due to the high power consumption of the V.35 interface, it will nominally run for only 15 minutes; therefore, we recommend that you use the AC Power Module.

1-21. RECOMMENDED TEST EQUIPMENT

Table 1-4 lists recommended test equipment. Equipment with equivalent characteristics may be used.

Table 1-4. Recommended Test Equipment

Instrument	Recommended Model	Use
Test Connectors	ET11293 ET25113	P,T P,T
Function Generator	HP 3325A	P
Signature Multimeter	HP 5005B	T
Oscilloscope	HP 1740B	T
Multimeter	HP 3466A	T

P=Performance Tests T=Troubleshooting

The following cables are necessary to operate and perform tests on the HP 4925B.

04925-61607	RS-232C/V.24 Cable
04925-61608	Patch Jumpers
10368-61601	V.35 Cable

NOTE

Figure 6-1 is the drawing for ET 11293.
Figure 6-2 is the drawing for ET 25113.

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section contains information on initial inspection, preparation for use, power requirements, and storage and shipment instructions for the HP 4926B Bit Error Rate Test Set.

2-2. INITIAL INSPECTION

Inspect the shipping container for damage. If the container or cushioning material is damaged, keep it. Check the contents of the shipment for completeness, then check the unit mechanically and electrically. Refer to Section IV for Performance Verification tests.

If the unit is incomplete, mechanically damaged or fails the tests in Section IV, notify the carrier and the nearest Hewlett-Packard office (listed in the rear of this manual). Keep the shipping materials for the carriers inspection. Hewlett-Packard will arrange for repair or replacement of the instrument without waiting for claim settlement.

2-3. PREPARATION FOR USE

2-4. POWER REQUIREMENTS

When the Bit Error Rate Test Set has option 101 installed, it is generally powered by six 9 volt alkaline transistor batteries. If the batteries have insufficient charge to reliably power the instrument, the BAT indicator will light. The BAT indicator is in the lower left corner of the bottom display.

If option 102 is running on the 9 volt batteries, the same indicator will light when the batteries have insufficient charge. However, we recommend using the HP 4925B with the AC Power Module when using the V.35 interface.

NOTE

Due to the high power consumption of the V.35 interface, it will nominally run for only 15 minutes; therefore we recommend that you use the AC Power Module.

2-5. CABLES

The HP 4925B has no cables. The HP 18183A, RS-232C/V.24 interface is supplied with an interface cable and six patch wires. The HP 18184A, V.35 interface is supplied with an interface cable.

2-6. OPERATING ENVIRONMENT

The instrument may be stored or operated in environments with the following limits.

OPERATING	
Temperature	+0°C to +50°C (+32°F to +122°F)
Altitude	up to 4600 metres (15,000 ft)
STORAGE	
Temperature	-40°C to +65°C (-40°F to +149°F)
Altitude	up to 15,300 metres (50,000 ft)

The HP 4925B should be protected from temperature extremes which can cause condensation within the instrument.

2-7. STORAGE AND SHIPMENT

2-8. Tagging for Service

If the HP 4925B or any accessory is returned to Hewlett-Packard for service, complete one of the blue repair tags located at the end of this manual and attach it to the instrument.

2-9. Original Packaging

Containers and materials similar to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is returned to Hewlett-Packard for service, complete and attach the blue repair tag. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model and serial number.

2-10. Other Packaging

Use these general instructions for packaging with commercially available materials:

a. Wrap the instrument in aluminum foil or an antistatic bag. If shipping to a Hewlett-Packard Sales or Service Office, include a completed blue repair tag.

CAUTION

The internal components of this instrument are static sensitive.
Refer to paragraph 8-7 for handling procedures.

b. Use a strong shipping container such as a double-wall carton with 275 lbs burst test.

c. Use a layer of shock absorbing material, 70-100 mm (3-4 in.) thick. This provides a firm cushion and prevents movement inside the container.

d. Seal the carton securely and mark it FRAGILE to ensure careful handling.

SECTION III
OPERATION

3-1. INTRODUCTION

This section describes the front panel controls, indicators, and connectors, as well as operation of the HP 4925B Bit Error Rate Test Set. Read this description before operating the instrument to understand the full capabilities and functions of each button. Second, basic operating procedures are described. The format is as follows: the instruction, set up choices for the test selected, and an example of a typical test set up. The blue characters represent the section of the display that changes when a button is pressed. Throughout the Operating Section the RS-232C/V.24 (HP 18183A) is the interface used in the test descriptions. When using the V.35 interface (HP 18184A) no changes other than those specifically described are necessary. Refer to Appendix C for information on the RS-232C/V.24 interface and Appendix D for the V.35 interface.

3-2. SELF CHECK

The HP 4925B automatically performs a basic self check procedure at power up. Error indications are shown on the display annunciators.

Table 3-1. Power Up Error Indications

ERROR MESSAGE	DESCRIPTION
CHECK POWER	Check the batteries or check the AC Power Module and connections
SELF TEST FAILED	Call Service Center for repairs

3-3. ERROR MESSAGES

During the initiation of a test, an error message may appear. Error messages are given with each appropriate test procedure.

3-4. CONTROLS, CONNECTORS, AND INDICATORS

Figure 3-1 shows the front panel controls, connectors, and indicators of the Bit Error Rate Test Set. The controls, connectors, and indicators for each interface are described in the appropriate appendix.

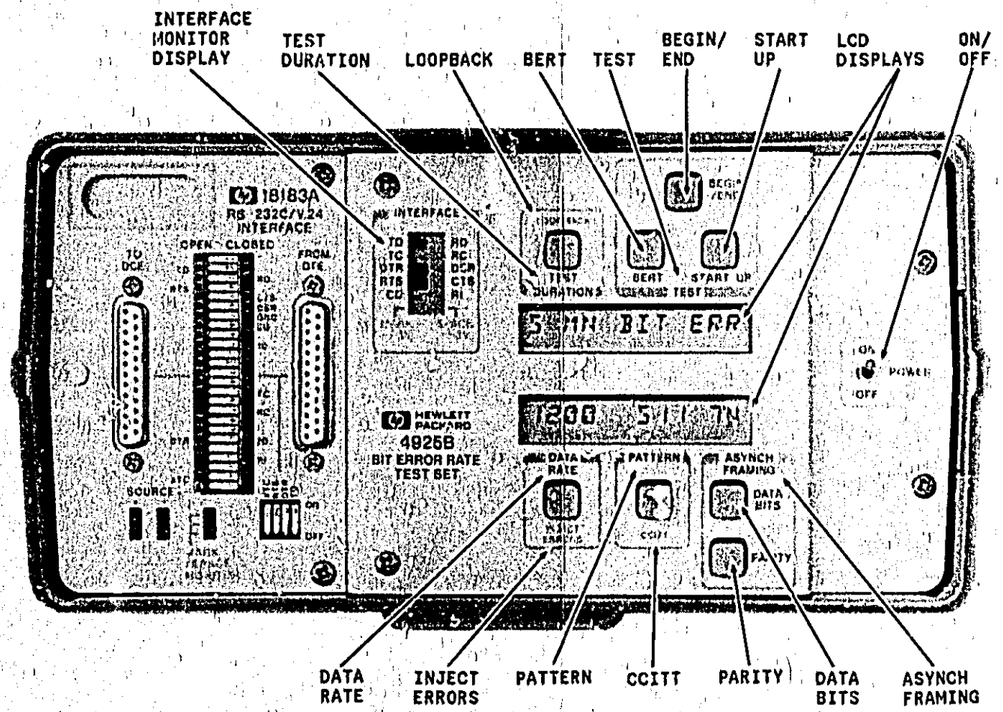


Figure 3-1. HP 4925B Front Panel, Error Analyzer Section

ON/ OFF Switches power to Bit Error Rate Test Set on or off.

TEST DURATION Determines duration of the test in number of bits or amount of time as shown below. When number of bits is selected, an error rate will be displayed. When an amount of time is selected, an error count will be displayed. The CONT set up allows the test to run indefinately or until the BEGIN/END button is pressed.

Number of bits	10/3, 10/4, 10/5, 10/6, 10/7, 10/8, 10/9
Time	5 MN, 10MN, or 15MN, CONT

NOTE

10/5, for example, should be read as the exponent of 10 is 5, or 100,000 bits.

5 MN, for example, should be read as 5 minutes.

TEST There are three buttons in this section: BERT, START UP, AND BEGIN/END.

BERT Selects the Bit Error test, the test choices are listed in Table 3-2. All Bit Error tests are performed simultaneously. Cumulative test results are displayed while the test is running. To view the other test results, press the BERT button until all results have been displayed.

Table 3-2. BERT Test Selections and Results

TEST SELECT MNEMONIC	TEST RESULT MNEMONIC	DESCRIPTION	TEST DURATION ENTRY
BIT ERR	BE	Bit Error Count	time
BLK ERR	BLE	Block Error Count	time
ERR SEC	ERS	Error Seconds	time
not selected	%EFS	Percent Error Free Sec	time
BER	BE	Bit Error Rate	number of bits
BLER	BLE	Block Error Rate	number of bits

START UP

Selects RTS-CTS delay time measurement or Start Up tests. The Start UP tests transmit and receive a fixed length message which checks the auto-equalization capability of the modem. For Start Up, tests ASYNCHRONOUS FRAMING and TEST DURATION cannot be operator selected and are therefore blanked out. The DATA RATE must be selected before pressing the START UP button with the exception of the RTS-CTS DELAY TIME test.

Table 3-3. Start Up Test Selections

MNEMONICS	MNEMONIC DESCRIPTION
RTS-CTS TIME	Request-To-Send - Clear-to-Send Delay Time
RANDOM MSG XMIT FIRST	End-to-end Start Up test, Transmit First
RANDOM MSG RECV FIRST	End-to-end Start Up test, Receive First
RANDOM MSG LOOPBACK	Loopback Start Up test
MARK MSG 208B REMOTE	Remote start up test for Bell 208B modem

BEGIN/ END

Initiates a selected test or aborts a test in progress. It also shifts to expand the capabilities of the Bit Error Rate Test Set, see the shift heading for descriptions.

DATA RATE

Controls system clocking. The display is shown in bits per second. For asynchronous modems, data is clocked out on the TD line and clocked in on the RD line at any one of the set rates given in Table 3-4.

For externally timed synchronous modems, the selected rate is available on the External Transmit Clock line (XTC, pin 24). Selection of rates is the same for asynchronous modems.

Table 3-4. Data Rates

75	110	134.5	150	200	300
600	1200	1800	2400	3600	4800
7200	9600	14.4K	19.2K		

For internally timed synchronous modems, select EXT. The HP 4925B will accept transmitter and receiver timing on TC (pin 15) and RC (pin 17) respectively.

PATTERN Selects the desired data sequence. Each sequence, with the exception of FOX is a pseudo random binary sequence. There are four patterns: 63, 511, 2047, and FOX.

The FOX message: THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789. (carriage return, line feed)

The 7 bit ASCII message: THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.AMZZMAAMZZMAAMZZMA... (carriage return, line feed)

Note that the 7 bit ASCII FOX message repeats the AMZZMAA... sequence until 80 characters are transmitted. After each line of the FOX pattern, there is a carriage return and a line feed.

ASYNCH FRAMING There are two buttons, one selects DATA Bits and the other PARITY. When the ASYNCH FRAMING display is blank, framing is disabled.

DATA BITS Selects the number of pseudo random data bits to be framed with start and stop bits and the character code when transmitting the FOX message.

Table 3-5. DATA BIT and PARITY Selections

Pattern	Data Bits	Parity	Output Data
63, 511, 2047	5	odd, even, none	Framed PRBS
63, 511, 2047	6	odd, even, none	Framed PRBS
63, 511, 2047	7	odd, even, none	Framed PRBS
63, 511, 2047	8	odd, even, none	Framed PRBS
FOX	5	odd, even, none, space, mark	BAUDOT CODE, FOX
FOX	6	odd, even, none, space, mark	EBCD CODE, FOX
FOX	7	odd, even, none, space, mark	ASCII CODE, FOX
FOX	8	odd, even, none	EBCDIC CODE, FOX

PARITY Selects the parity bit to be appended to the transmitted characters. Parity selections are shown in Table 3-5. Parity analysis is performed on received characters only when transmitting the FOX message. When odd parity is selected, the appended parity bit is set (1) or reset (0), to make an odd number of 1's in the character, including the parity bit.

Shift BEGIN /END

Pressing the shift button plus BEGIN/END expands the capabilities of the Bit Error Rate Test Set. When BEGIN/END is pressed, the word SHIFT is displayed and there is a 1/2 second delay. If LOOPBACK, INJECT ERRORS, or CCITT are pressed during the 1/2 second delay, then the function will be active.

NOTE

If an expanded function is not pressed within 1/2 second, then the set up test sequence begins.

shift LOOPBACK

This is the expanded function of the TEST DURATION button. The test set is put into internal digital loopback mode before the interface and internally connects TD to RD. It is primarily used for demonstrations and Self Test. To enable the internal loopback, press BEGIN/END, then TEST DURATION, the lower display will read LOOPBACK. Press BEGIN/END then TEST DURATION to cancel the loopback function, the lower display will read NORMAL.

shift INJECT ERRORS

This is the expanded function of the DATA RATE button. It is used before or after a test sequence is initiated. Before a test, press BEGIN/END, then DATA RATE to transmit a burst of errors.

During a test, press only the DATA RATE button and a burst of errors is injected for a fixed length of time with a 1 in 16 error rate except when transmitting errors with framing. This verifies the mechanical connection during end-to-end or loop-around testing. Holding down the INJECT ERRORS button causes a continuous injection of errors. INJECT ERRS is displayed while the button is held down. If the display overflows (OVF), the tests continue and valid data will be obtained.

shift CCITT

This is the expanded function of the PATTERN button for 511 and 2047 PRBS. When pressed, CCITT will appear in the lower display. The block or sequence length is then equal to the PRBS length selected. If the pattern selected is 511, then the block length is 511 bits. If the pattern selected is 2047, then the block length is 2047 bits. Testing in the CCITT mode is otherwise identical to testing in the standard 1000 bit block mode. Press BEGIN/END, then PATTERN to revert to the 1000 bit block configuration or cycle the power switch. If BEGIN/END then PATTERN is pressed, the lower display will read 1000 BIT/BLK. Press BERT button to return to the menus.

If operation in CCITT mode is permanently desired, refer to Appendix A.

LCD Display

There are two alphanumeric Liquid Crystal Displays (LCD). The top display shows set up and test results for TEST DURATION and TEST sections. The bottom display shows set up for DATA RATE, PATTERN, and ASYNCH FRAMING selections. Error messages also appear on these displays. After displaying test results for 5-7 minutes, the displays will turn off. To turn them back on, press any set up button.

INTERFACE Monitor Display

An LCD bargraph display which monitors the status of selected lines. Table 3-6 lists the lines monitored. A flashing bar indicates that the line is active either the data or clock. When the bar is ON, a space condition is indicated; when it is OFF, a mark condition or an invalid EIA stateline. The MARK and SPACE monitor is a tristate monitor showing the status of the MARK/SPACE MONITOR on the interface.

Table 3-6. Interface Monitor Displays

TD	Transmit Data	RD	Receive Data
TC	Transmit Clock	RC	Receive Clock
DTR	Data Terminal Ready	DSR	Data Set Ready
RTS	Request To Send	CTS	Clear To Send
CD	Carrier Detect	RI	Ring Indicator

MARK/SPACE MONITOR

MARK	SPACE
negative voltage, binary one, signal mark, function OFF	positive voltage, binary zero, signal space, function ON

3-5. OPERATING PROCEDURES

A variety of set up selections for each test allows operator flexibility. Capabilities of each feature are detailed in paragraph 3-4. Instrument operation is described by a series of typical test applications. Paragraph 3-7 describes the initial instrument power up sequence. From the top level menu any of the test sequences may be initiated. Each typical test application is described and illustrated with a sample set up procedure. In the sample set up procedure there are three columns. The first, Set Up Instructions gives the steps that the test operator must perform. Choices, the second column lists menu selections appropriate for that test. Finally in the Sample Display column, a possible test set up is illustrated by showing how the HP 4925B displays will appear as each button is pressed. The blue characters show what part of the display changes as each set up is selected. Press BEGIN/END once to begin testing, press it again to halt testing. STOPPED is displayed to indicate the end of testing.

3-6. BIT ERROR TEST ERROR MESSAGES

Table 3-7 lists error messages which may appear while initiating a Bit Error test.

Table 3-7. Bit Error Test Error Messages

ERROR DISPLAY	PROBLEM	CORRECTION
OUT OF LOCK DATA FAULT	wrong data or data with large number of errors received after BEGIN/END button pressed	need to receive relatively error free data
OUT OF LOCK SYNCH LOSS	during a test, a clock slip or dropout on TD or RD occurred	test suspended while HP 4925B resynchronizes with receive data

The tests may be run without operator attendance. If a dropout or clock slip occurred during the test, it will be displayed on the annunciators until the test results are viewed and the test menus are accessed. Annunciator error codes are given in Table 3-8.

Table 3-8. Annunciator Error Codes

CODE	DESCRIPTION
0	Dropout
1	Clock Slip

3-7. INITIAL HP 4925B BIT ERROR RATE TEST SET SET UP

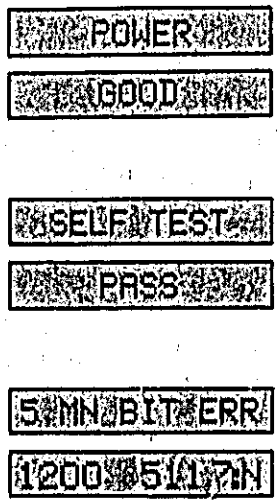
When using the V.35 interface, connect the cable and proceed with the desired test sequence. The tests are described using the RS-232C/V.24 interface for illustration; however, unless specifically described there are no differences when using the V.35 interface.

When using the RS-232C/V.24 interface, you must configure the Breakout Box before testing. For most test procedures, the Breakout Box Switches are CLOSED and the XTC, RTS, DTR, TD, ON/OFF switches are ON. This set up changes for testing in bridge mode configurations. If a different switch set up is required for a test procedure, the recommended configuration is described.

The following sequence occurs each time the instrument is turned on.

INITIAL INSTRUMENT POWER ON SEQUENCE

Turn on the POWER switch. The following sequence of displays should appear.



The last display is the top level menu, you are now ready to begin testing. Read the display as follows:

A bit error rate count with a data rate of 1200 bps and 511 PRBS with 7 data bits and no parity will be performed for 5 minutes.

3-8. BIT ERROR TESTS

Several variations of Bit Error Tests are described in the following paragraphs. Described are Bit Error Tests and Bit Error Tests in Character Oriented Networks. All Bit Error tests are performed simultaneously. Paragraph 3-11 describes the results of the Bit Error Rate tests.

3-9. BIT ERROR TESTING IN ASYNCHRONOUS NETWORKS

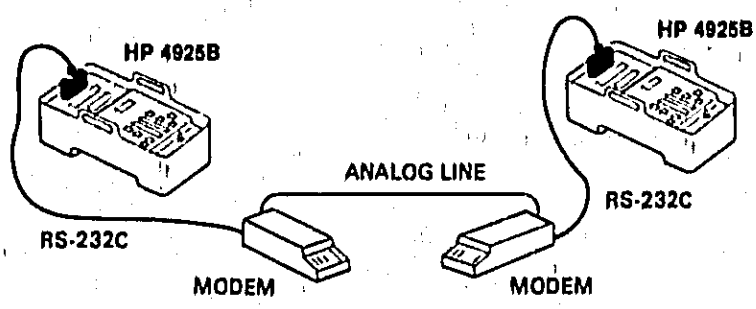


Figure 3-2. Typical Bit Error Test with Asynchronous Modems

Description

This test checks the ability of asynchronous modems to maintain the integrity of transmitted and/or received data bits. In addition to the test shown in Figure 3-3 (end-to-end test), testing may be done in loopback mode.

BIT ERROR TESTS

Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		5'MN BIT ERR 1200 511 7:N
Press  to select the modem data rate.	75, 110, 135.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 14.4 k, 19.2 k	5'MN BIT ERR 2400 511 7:N
Press  to select the Pseudo Random Bit Sequence (PRBS).	63 511 2047	5'MN BIT ERR 2400 2047 7:N
Press  to select number of data bits in each character compatible with equipment under test.	5 6 7 8	5'MN BIT ERR 2400 2047 7:N
Press  to select parity of equipment being tested.	O (odd) E (even) N (none)	5'MN BIT ERR 2400 2047 7:E
Press  to select length of test.	10^3 - 10^9 5 MN 10 MN 15 MN CONT	10MN BIT ERR 2400 2047 7:E
Press  to see the test menu.	BIT ERR BLK ERR ERR SEC BER BLER	10MN BIT ERR 2400 2047 7:E

BIT ERROR TESTS

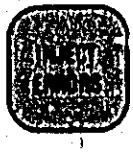
Running the Test

During the test, the TEST DURATION display field flashes, this indicates that the test is in progress. Elapsed time is displayed as seconds until one minute, after which minutes are displayed. When Number of Bits is chosen, the number of received bits is displayed, starting with 10^3 (1003). The display shows the HP 4925B counting to the selected number.

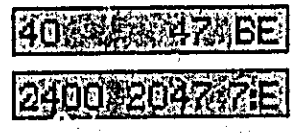
Asynchronous framing may be disabled by pressing the DATA BITS button until the display field goes blank.

NOTE, testing Asynchronous Networks this way is not representative of actual data format and is not recommended.

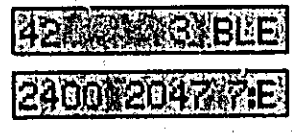
Press  to start the tost.

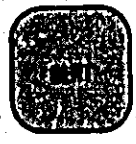
Press  to inject errors any time. (Error count appears on receiving test set)

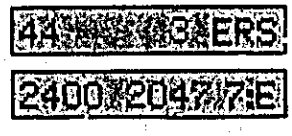
Accumulated error count is continuously displayed.



Press  to see accumulated error count at any time.



Press  to see accumulated error count at any time.



Press  to stop the test at any time. Testing automatically stops when the selected duration ends.

3-10. Bit Error Testing in Synchronous Networks

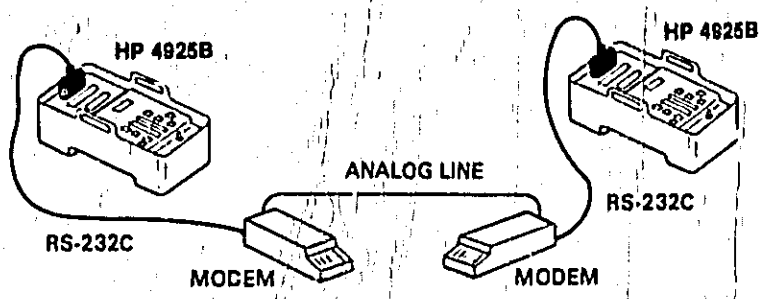


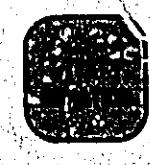
Figure 3-3. Typical Bit Error Test with Synchronous Modems

Description

This test checks the ability of externally timed synchronous modems to maintain the integrity of transmitted and/or received data bits. In addition to the test shown in Figure 3-3 (end-to-end test), testing may be done in loopback mode.

Test Procedure

Verify that the modem provides clock on the interface. The TC and RC Interface Monitor Displays should be active.

Set Up Instructions			Choices	Sample Display
Turn on the HP 4925B				5MN BIT ERR 1200 511 2MN
Press		to select EXT since the modem provides timing.	EXT	5MN BIT ERR EXT 511 2MN
Press		to select the Pseudo Random Bit Sequence (PRBS).	63 511 2047	5MN BIT ERR EXT 2047 2MN
Press		to select length of test	10^3 - 10^9 5 MN 10 MN 15 MN CONT	10MN BIT ERR EXT 2047 2MN

BIT ERROR TESTS

Set Up Instructions	Choices	Sample Display
Press  to see the test menu	BIT ERR BLK ERR ERR SEC BER BLER	10MN BIT ERR EXT 2047

NOTE

Externally timed synchronous modems may use the HP 4925B internal clock, see paragraph 3-9 for set up.

Running the Test

During the test, the TEST DURATION display field flashes, indicating that the test is in progress. Elapsed time is displayed as seconds until one minute, after which minutes are displayed. When number of bits is chosen, the number of bits tested is displayed, starting with 10^3 (10^3) and counting to the selected number.

Paragraph 3-11 describes the results of this test.

Press 	to start the test.	10MN 0 BE EXT 2047
Press 	to inject errors any time. (Error count appears on receiving test set)	35 0 BE INJECTD ERRS
Accumulated error count is continuously displayed.		10 47 BE 2400 2047
Press 	to see accumulated error count at any time.	42 3 BLE 2400 2047
Press 	to see accumulated error count at any time.	44 29 ERS 2400 2047
Press 	to stop the test at any time. Testing automatically stops when the selected duration finishes.	4MN 29 BE STOPPED

3-11. BIT ERROR TEST RESULTS

1. Results are determined simultaneously for all Bit Error tests. Pressing the BERT button displays the other test results.

2. Tables 3-9 and 3-10 give samples of test results and descriptions of the data.

Table 3-9. Test Results for Time TEST DURATION Selection

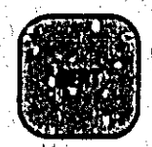
To See the Test Results	Description of Test Results	Sample Display
Press 	In a 10 minute test, 237 bit errors were found.	10 MN 237 BE STOPPED
Press 	In the same 10 minute test, 43 block errors were found.	10 MN 43 BLE STOPPED
Press 	In the same 10 minute test, 19 error seconds were found.	10 MN 19 ERS STOPPED
Press 	The HP 4925B calculated 97.8% error free seconds.	97.8 % ERS STOPPED

Table 3-10. Test Results for Number of Bits TEST DURATION Selection

To See the Test Results	Description of Test Results	Sample Display
Press 	3×10^{-5} is the bit error rate.	3E-5 BER STOPPED
Press 	9×10^{-2} is the block error rate	9E-2 BLER STOPPED

3-12. RESULTS WHEN TESTING IN CCITT ENVIRONMENT

To perform a test in CCITT mode configure the HP 4925B during the test set up, see Appendix A for more information. A quick arithmetic calculation is required to read the data. The number of received bits is always displayed. Subtract three (3) from the exponent to get the block error rate. For example, if the exponent of the number of received bits is 5, then 5-3=2, the number of received blocks.

When testing in a CCITT environment, use the following formulas to calculate the number of received blocks.

511 bit blocks

$$\text{number of received blocks} = \frac{\text{number of received bits x blocks}}{\text{511 bits}}$$

2047 bit blocks

$$\text{number of received blocks} = \frac{\text{number of received bits x blocks}}{\text{2047 bits}}$$

Example: for 10^5 received bits

$$10^5 \times \frac{1}{511} = 196 \text{ received blocks}$$

3-13. OPTIONS AFTER RUNNING A TEST

After a test is complete and the data reviewed, the operator has several options. These options are described in Table 3-11.

Table 3-11. Options After Running A Test

BUTTON	ACTION
DATA RATE	Redisplays instrument set up
PATTERN PARITY DATA BITS TEST DURATION START UP	Set up may be modified at this point
BERT	Displays other Bit Error Test results
BEGIN/END	Begins another test session using current instrument set up.

3-14. TERMINAL AND PRINTER TESTING

3-15. SIMULATING DATA COMMUNICATIONS EQUIPMENT

To perform the Terminal and Printer tests, the HP 4925B Bit Error Rate Test Set must be configured to appear as a DCE source rather than a DTE source. If you are using the RS-232C/V.24 interface, move the XTC, RTS, DTR, TD, ON/OFF switch to the ON position. OPEN Breakout Box Switch lines TD, RD, and if necessary DTR, DSR, RTS, and CTS. Table 3-12 lists the lines to be patched together. Connect the device under test to the DCE connector (TO DCE).

Table 3-12. DCE Simulation Using the Breakout Box

To DCE			From DTE	
(2)	TD	⟷	RD	(3)
(3)	RD	⟷	TD	(2)
(6)	DSR	⟷	DTR	(20)
(20)	DTR	⟷	DSR	(6)
(4)	RTS	⟷	CTS	(5)
(5)	CTS	⟷	RTS	(4)

3-16. TRANSMISSION OF THE FOX MESSAGE

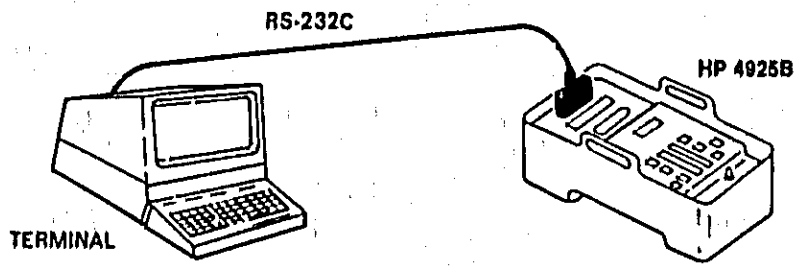


Figure 3-4. Typical Terminal Test

Description

This test checks the ability of asynchronous terminals and printers to receive and display data. The FOX message

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.

is transmitted to the terminal or printer. When the unit under test is 7 bit ASCII, AMZZMAA... is appended. Parity analysis for odd or even parity can also be performed. When 8 data bits per character is set up, only odd, even, or no parity may be selected.

Test Procedure

When using the RS-232C/V.24 interface, first verify that the configuration described in paragraph 3-15 is implemented.

Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		5:MN?BIT:ERR 1200 :511?:N
Press  to select the data rate.	75, 110, 134.5, 150, 200 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 14.4 k, 19.2 k	5:MN?BIT:ERR 2400 :511?:N
Press  to select the FOX message.	FOX	CONT: 2400 :FOX:7:N

TERMINAL AND PRINTER TESTING

Set Up Instructions			Choices	Sample Display
Press		to select the character code compatible with the equipment under test.	5 (BAUDOT) 6 (EBCD) 7 (ASCII) 8 (EBCDIC)	CONT 2400 FOX 7:N
Press		to select parity of equipment being tested.	O (odd) E (even) N (none) M (mark) S (space)	CONT 2400 FOX 8:M

RUNNING THE TEST

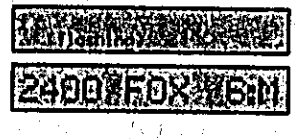
During the test, the TEST DURATION display field flashes to indicate that the test is being performed. Shown below is the FOX message, followed by the 7 bit ASCII FOX message:

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.

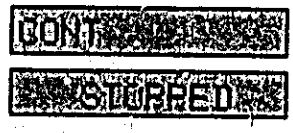
THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.AMZZMAAMZZMAA....

The appropriate message will immediately be printed on the terminal or printer under test.

Press  to start the test.



Press  to stop the test at any time.



3-17. PARITY ERROR COUNTING

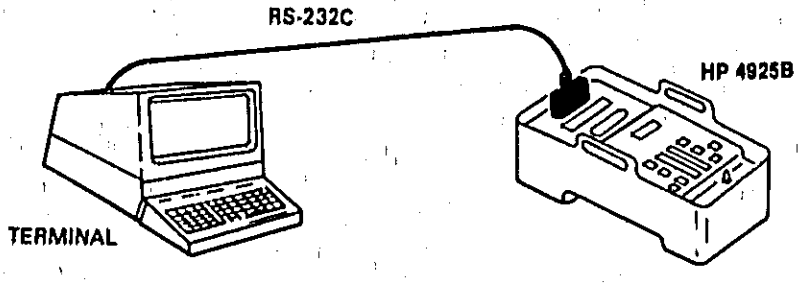


Figure 3-5. Typical Parity Error Counting Test

Description

When odd or even parity is selected with the FOX message, the Bit Error Rate Test Set detects parity errors in received characters on RD (pin 3) while transmitting the FOX message.

Test Procedure

When using the RS-232C/V.24 interface, first verify that the configuration described in paragraph 3-15 is implemented.

Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		5 MIN BIT ERR 1200 5 1 K 7:N
Press DATA RATE to select the data rate.	75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 14.4 k, 19.2 k	5 MIN BIT ERR 2400 5 1 K 7:N
Press PATTERN to select the FOX pattern.	FOX	CONT 2400 FOX 7:N
Press DATA BITS to select the number of bits compatible with equipment being tested.	5 (BAUDOT) 6 (EBCD) 7 (ASCII) 8 (EBCDIC)	CONT 2400 FOX 8:N
Press PARITY to select parity of equipment being tested.	O (odd) E (even)	CONT ERR/ERR 2400 FOX 8:O

TERMINAL AND PRINTER TESTING

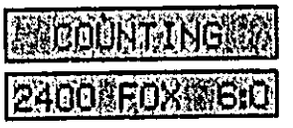
RUNNING THE TEST

During the test, the TEST DURATION display field flashes to indicate that the test is being performed. The FOX message will appear directly on the terminal screen or printer paper. Shown below is the FOX message, followed by the 7 bit ASCII message:

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.AMZZMAAMZZMAA....

Press  to start the test and begin parity error detection.



Press  to stop the test at any time.

Press  to unlock the FOX message test and allow the menu to be changed.

3-18. Parity Error Counting in Bridge Mode

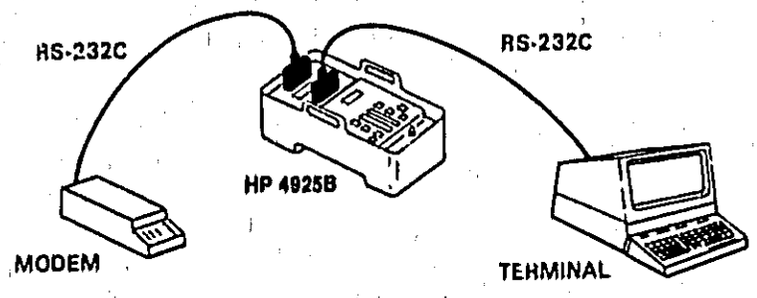


Figure 3-6. Typical Parity Error Counting Test in Bridge Mode

Description

This test counts parity error in bridge mode.

Before selecting the set up conditions, move the XTC, RTS, DTR, and TD, ON/OFF switches to the OFF position. If you are using the RS-232C/V.24 interface, connect the terminal equipment to the FROM DTE connector and the communications equipment to the TO DCE connector. The Bit Error Rate Test Set counts parity errors in the bridge mode. A check for parity errors is performed each time that a character is received.

Test Procedure

Follow the sample test procedure given in paragraph 3-17, Parity Error Counting. During the test the TEST DURATION display field flashes to indicate that the test is being performed.

When using the RS-232C/V.24 interface, first verify that the configuration described in paragraph 3-15 is implemented.

Test Results

Press  to unlock the FOX message test and allow the menu to be changed.

3-19. START UP TESTING

The following paragraphs describe the Start Up Tests. To access the RTS-CTS Delay Time and Start Up test menus, press the START UP button. Each Start Up test procedure format gives necessary set up instructions, error codes, and test results.

NOTE

Start Up tests with RS-232C/V.24 interfaces can not be performed above 9600 bps. RTS-CTS delay time is independent of data rate.

3-20. Request-to-Send - Clear-to-Send Delay Time

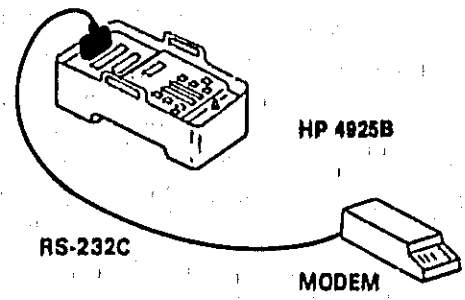


Figure 3-7. Typical RTS-CTS Delay Time Test

Description

This test measures the delay time between a Request-To-Send signal (RTS) asserted by the HP 4925B and a Clear-To-Send (CTS) signal received from the modem under test.

Testing Algorithm

Raise RTS
Start internal timer
Look for CTS
Upon CTS, stop timer
Calculate delay
Repeat algorithm

Test Procedure

Set the XTC, RTS, DTR, and TD switches to the ON position.

Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		
Press [ ] to select test.	RTS-CTS	

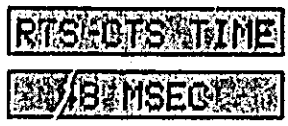
START UP TESTING

Running the Test

Press  to start the test.

Once CTS is detected.

The delay time result is displayed for 2 seconds. The display momentarily blanks, then the test is repeated.



Error Messages

Table 3-13. RTS-CTS Delay Time Error Messages

ERROR MESSAGES	DESCRIPTION
RTS-CTS	Clear-To-Send not received
NO CTS	CTS should be within 1 second of RTS.
RTS-CTS	If this message appears for longer than 1 second, then the RTS switch is open.

Once an error message is indicated, press BEGIN/END to stop the test. Correct the problem and start the test over again.

Test Results

Press  to stop the test any time.

3-21. Request-to-Send - Clear-to-Send Delay Time in Bridge Mode

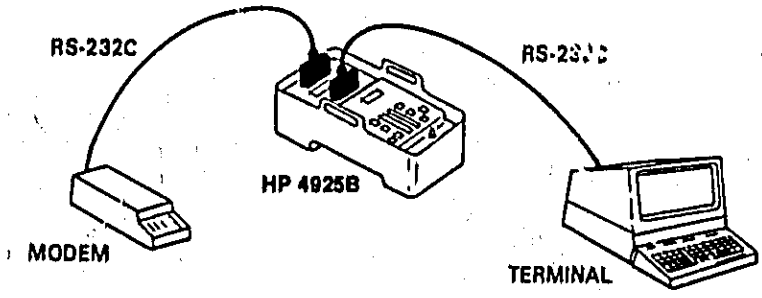


Figure 3-8. Typical RTS-CTS Delay Time in Bridge Mode Test

Description

This test measures the delay time between a Request-To-Send signal (RTS) asserted by the terminal equipment and a Clear-to-Send (CTS) signal received from the modem under test.

Testing Algorithm

Look for RTS
Upon RTS, start internal timer
Look for CTS
Upon CTS, stop timer
Calculate delay
Repeat algorithm

Test Set Up

Move the XTC, RTS, DTR, and TD ON/OFF switches to the OFF position. For the RS-232C/V.24 interface, connect the terminal equipment to the FROM DTE connector and the communications equipment to the TO DCE connector. The Bit Error Rate Test Set will measure the RTS-CTS delay time in the bridge mode. The delay time will be measured each time the handshake occurs.

Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		SUM BIT ERR 1200 8 511 N7 N
Press  to select test.	RTS-CTS TIME	RTS-CTS TIME 1200 [illegible]

Running the Test

Press  to start the test.

RTS-CTS

Once CTS is detected.

RTS-CTS TIME
48 MSEC

The delay time result is displayed for 2 seconds. The display momentarily blanks, then the test is repeated.

RTS-CTS TIME
48 MSEC

Error Messages

Table 3-14. RTS-CTS Delay Time Error Messages

ERROR MESSAGES	DESCRIPTION
RTS-CTS	Clear-To-Send not received
NO CTS	CTS should be within 1 second of RTS.
RTS-CTS	If this message appears for longer than 1 second, the test set is still waiting for RTS from the terminal equipment.

Once an error is indicated, press BEGIN/END to stop the test. Correct the problem and start the test over again.

Test Results

Press  to stop the test any time.

RTS-CTS TIME
48 MSEC

3-22. End-to-End Start Up Test

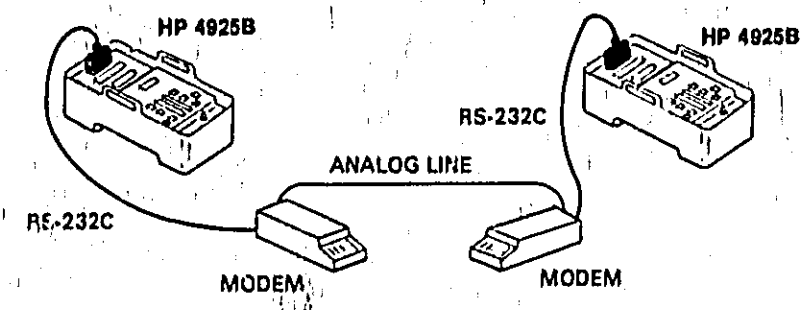


Figure 3-9. Typical End-to-End Start Up Test

Description

This test is used for half duplex, switched carrier networks. Two HP 4925B Test Sets are necessary to perform the test. One Test Set should be configured to transmit first and the other to receive first. The test is complete when 100 messages have been exchanged; however, the user may terminate the test at any time.

Testing Algorithm

Transmit First

Raise RTS
Look for CTS
Upon CTS, transmit random message
Drop RTS
Go to Receive First

Receive First

Look for CD on
Upon CD, receive message
Analyze received message for errors
If error(s), increment error counter
Increment total message counter
Look for CD off
Go to Transmit First

Test Set Up

If you are using the RS-232C/V.24 interface you can not perform Start Up tests above 9600 bps. The XTC, RTS, DTR, TD, ON/OFF switches should be ON for this test procedure.

NOTE

This test requires two HP 4925B Bit Error Rate Test Sets, one for each modem. Set up one Test Set to receive first, the other to transmit first. Press the BEGIN/END button on the set receiving first. Then press the transmitting set BEGIN/END button.

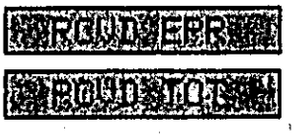
Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		

START UP TESTING

	Set Up Instructions	Choices	Sample Display
Press 	to select the modem data	75, 110, 134.5, 150, 200 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9000, EXT	5 MIN BIT ERR 2400: 5 1 %N
Press 	to select test.	RANDOM MSG XMIT FIRST RANDOM MSG RECV FIRST	RANDOM MSG XMIT FIRST

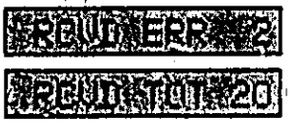
Running the Test

Press  to start the test.



Received message with errors and total transmissions are accumulated on the display as they occur.

Press  to stop the test at any time.



Error Messages

Table 3-15. End-to-End Test Error Messages

ERROR MESSAGES	DESCRIPTIONS
CARRIER	Carrier Detect (CD) is on.
NO CARRIER	Carrier Detect (CD) is off.
NO CTS	CTS is not detected.

Once an error is indicated, press BEGIN/END to stop the test. Correct the problem and start the test over again.

Test Results

When 100 transmissions are complete, or when the BEGIN/END button is pressed, the number of received messages containing one or more errors and total number of exchanges are displayed. The displays should be read as follows: 3 received messages contained one or more errors out of 100 messages received.

3-23. Loopback Test

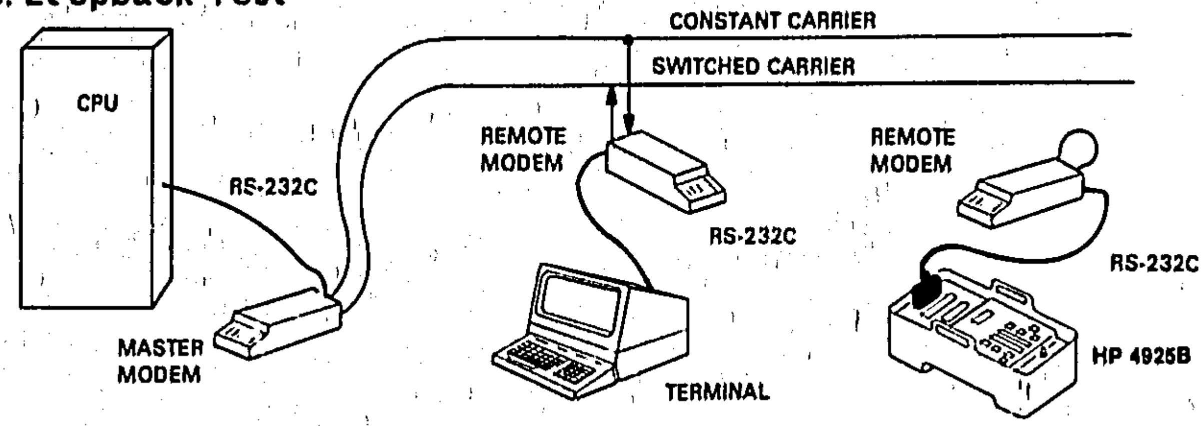


Figure 3-10. Typical Loopback Test

Description

This test checks configurations in which the modem is looped back. For example, a Loopback Start Up test may be performed on a modem in a multidrop network in which the modem is configured for constant carrier in one direction and switch carrier in the other. The test is complete when 100 messages have been exchanged; however, the user may terminate the test at any time.

Testing Algorithm

- Raise RTS
- Look for CTS
- Upon CTS, transmit random message
- Immediately receive message
- Drop RTS
- Analyze received message for errors
- If error(s), increment error counter
- Increment total message counter
- Repeat algorithm

Test Set Up

If you are using an RS-232C/V.24 interface the Start Up tests cannot be performed above 9600 bps. The XTC, RTS, DTR, TD, ON/OFF switches should be ON.

Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		5MIN BIT ERR 1200 5117N

START UP TESTING

Set Up Instructions			Choices	Sample Display
Press		to select the modem data	75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, EXT	EXMN BIT ERR EXT 0511
Press		to select test.	RANDOM MSG LOOPBACK	RANDOM MSG LOOPBACK

Running the Test

Press  to start the test.

RCVD ERR 0
RCVD TOT 0

Received errors and total transmissions are accumulated on the display as they occur.

Press  to stop the test at any time.

RCVD ERR 10
RCVD TOT 25

Error Messages

Table 3-16. Loopback Test Error Messages

ERROR MESSAGE	DESCRIPTION
NO CTS	CTS is not detected.
CLOCK FAULT	No receive clock transitions were detected or receive clock >9600 bps.

Once an error is indicated, press BEGIN/END to stop the test. Correct the problem and start the test over.

Test Results

When 100 transmissions are complete, or when the BEGIN/END button is pressed, the number of received messages containing one or more errors and total transmissions are displayed. The displays should be read as follows: 25 messages were received with errors out of 100 received messages.

RCVD ERR 25
RCVD TOT 100

3-24. Remote Test for Bell 208B Modem

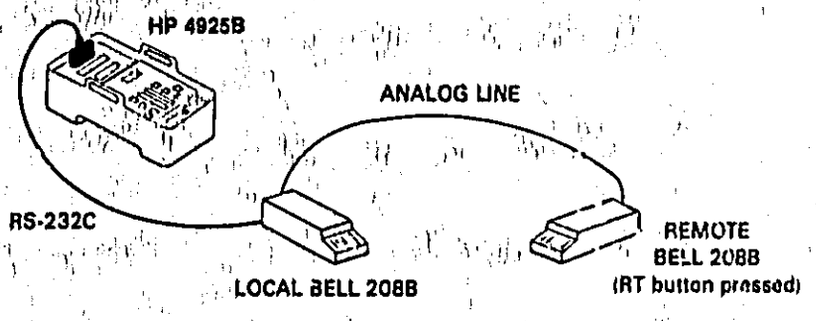


Figure 3-11. Typical Bell 208B Modem Remote Test

Description

This test performs start up tests using the remote test capability of the Bell 208B modem.

Testing Algorithm

Raise RTS
Look for CTS
Upon CTS, transmit mark for 1.5 seconds
Drop RTS
Look for CD on
Upon CD, examine receive data
Analyze receive data as follows:

Table 3-17. Bell 208B Remote Test Results

MESSAGE RECEIVED BY 4925B	208B PERFORMANCE	
	RECEIVER	TRANSMITTER
Mark	good	good
Mark with errors	good	error
Space	error	good
Space with errors	error	error

Repeat the algorithm.

Test Set Up

The XTC, RTS, DTR, TD, ON/OFF switches should be ON.

The data rate is automatically configured by the HP 4925B.

START UP TESTING

HP 4925B Set Up Instructions	Choices	Sample Display
Turn on the HP 4925B		5 MIN BIT ERR 1200 BAUD 7:N
Press  to select test.	MARK MSG REMOTE 208B	MARK MSG REMOTE 208B

RUNNING THE TEST

Press  to start the test.		RCV XMIT
Press  to stop the test at any time		RCV 2275 XMIT 18/75

ERROR MESSAGES

Table 3-18. Remote Test for Bell 208B Modem Error Messages

ERROR MESSAGES	DESCRIPTION
CARRIER	Carrier Detect (CD) is on.
NO CARRIER	Carrier Detect (CD) is off.
NO CTS	CTS is not detected.
CLOCK FAULT	No receive clock transitions were detected or receive clock > 9600 bps.

When an error is indicated, press BEGIN/END to stop the test. Correct the problem and start the test over again.

TEST RESULTS

The remote Bell 208B modem received 15 messages with error(s) and transmitted 1 message that was received with error(s) out of 100 messages exchanged.

RCV 15/100
XMIT 1/100

These results are displayed in terms of the performance of the remote modem.

3-25. TESTING USING THE SPECIAL FEATURES

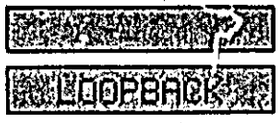
By using the shift function as shown in the following instruction sets, additional test capabilities may be obtained.

3-26. LOOPBACK

This mode puts the Bit Error Rate Test Set into an internal digital Loopback configuration.

Press 

, then 

to select internal Loopback feature. 

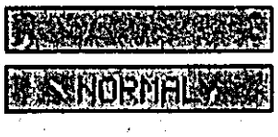
The TEST DURATION button must be pressed while the small SHIFT annunciator is visible on the upper display. If the button is not pressed before SHIFT disappears, the special feature will not be activiated.

Press the BERT button to return to the set up menus. The Bit Error Rate Test Set is now in digital loopback.

To return to normal operation

Press 

, then 

to release internal Loopback feature. 

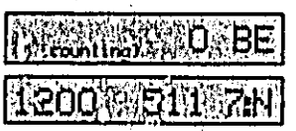
Press the BERT button to return to the set up menus.

3-27. INJECT ERRORS

The INJECT ERRORS feature may be used before or during a test sequence. To inject errors during a test, follow the procedure below.

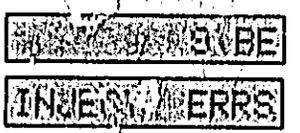
Press 

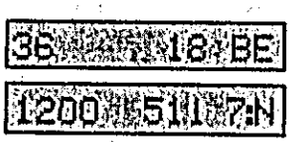
to initiate a test sequence.



Press 

to inject errors during the test.

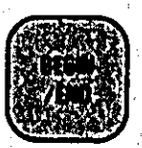




When the DATA RATE button is released, the display will return to the testing display.

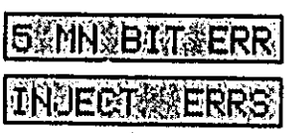
Errors may be injected as frequently as desired.

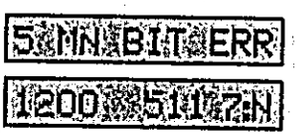
To inject error before initiating a test, for example, when transmitting on a half duplex line, use the following procedure.

Press 

, then 

to inject errors.





The DATA RATE button must be pressed while the small SHIFT annunciator is visible on the upper display. If the button is not pressed before SHIFT disappears, the special feature will not be activated. The display will automatically return to the menu after injecting errors.

3-28. CCITT

Changes the standard 1000 bit block length to block lengths equal to the pattern selected, 511 or 2047.

Press  , then  to change to CCITT.

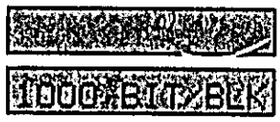
The PATTERN button must be pressed while the small SHIFT annunciator is visible on the upper display. If the button is not pressed before SHIFT disappears, the special feature will not be activated.

Press the BERT button to return to the menus.

PATTERN selections will now be CCITT only (511, 2047, FOX).

To return to the 1000 bit block mode

Press  , then 



Press the BERT button to return to the menus.

SECTION IV
PERFORMANCE VERIFICATION

4-1. INTRODUCTION

Tests in this section verify instrument performance. These tests may be used as part of incoming inspection and can be performed without accessing the instrument's internal circuits. If the instrument fails these tests refer to the Service Section.

4-2. EQUIPMENT REQUIRED

Table 1-2 lists equipment required for the Performance Verifications. Test equipment with equivalent specifications may be substituted.

4-3. TEST RECORD

Test results may be recorded on the test record located at the end of this section. Results of tests recorded during incoming inspection can be used for comparison in maintenance or troubleshooting.

4-4. SELF CHECK

Self check is automatically done each time the instrument is powered up. If the Bit Error Rate Test Set passes, the LCD display reads: SELF TEST PASS.

4-5. PERIODIC PERFORMANCE VERIFICATION

This instrument requires periodic performance verification. The instrument should be checked every six months using the performance tests. Performance tests should also be performed following repair.

4-6. PERFORMANCE VERIFICATION TESTS

4-7. PERFORMANCE VERIFICATION

Description

This test verifies functional operation of 95% of the Bit Error Rate Test Set circuitry. There are five parts to the test.

Self Test
Verification of Interface Monitor Displays
Contiguous Bit Error Test
Asynchronous Bit Error Test
RTS-CTS Delay Test

Equipment Needed

7 ea 22-26 AWG single strand wire
or ET11293 for RS232
or ET25113 for V.35

Test Set Up

Turn on the Bit Error Rate Test Set and set it up as follows:

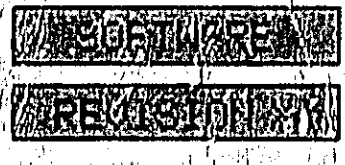
Set the XTC, RTS, DTR, TD, ON/OFF switches to the ON position.
Set the Breakout Box switches to the CLOSED position.

Test Procedure

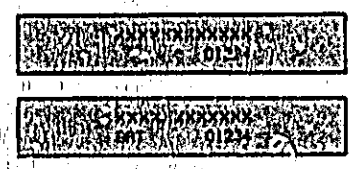
1. To execute the Self Test, quickly press the following buttons in the order shown.

   BEGIN/END
   START UP

2. The first display identifies the Software.

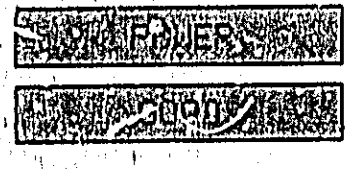


3. A display sequence comes up next. All segments should be lit as shown below. If not, refer to paragraph 8-62 in the Service Section.

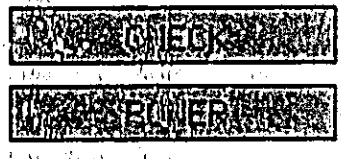


4. Next, the power condition is displayed.

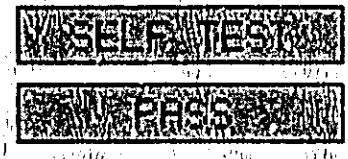
   a. There is sufficient power.



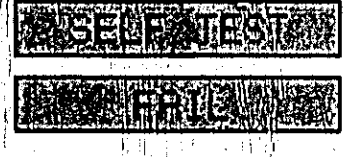
   b. Check the power. Turn off the HP 4925B. If running on batteries, the batteries should be replaced. If running on AC power (using an HP 18185A), there is a fault in the AC line or in the HP 18185A.



5. After performing the self tests, the Bit Error Rate Test set will display:



   a. If the instrument does not pass Self Test, a FAIL message with an error code is displayed. Refer to Table 8-8 in the Service Section for the error code descriptions and paragraph 8-62 for troubleshooting procedures.



4-8. Interface Test Procedure

HP 18183A

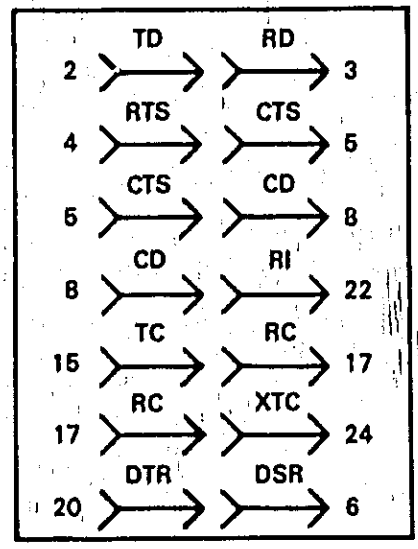
1. If ET11293 is available, follow the set up procedure given in paragraph 4-9 and begin with step 4. If not, follow the procedures below.

2. Loop the pins on the Breakout Box switch as shown in Table 4-1.

NOTE

When the Breakout Box switches are set CLOSED,
the two sides of the Breakout Box header strip are connected together.

Table 4-1. Breakout Box Switch Jumper Configuration



3. Connect pin 3 (RD) of the Breakout Box switch to the MARK/SPACE MONITOR.

HP 18184A: ET 25113 must be used. Set-up for ET 25113 is on page 6-5. Start testing at procedure 4-8, step 4.

4. If any of the following tests fail, go to the Troubleshooting Section in the appropriate appendix (Appendix C for RS-232C/V.24, Appendix D for V.35).

5. After the Bit Error Rate Test Set displays SELF TEST PASS, the instrument will display the top level menu. Press DATA BITS twice and the data bits part of the display will blank.

   a. The following Interface Monitor displays should be flashing:

TD	RD
TC	RC
MARK	SPACE

MARK SPACE on the display will be OFF with the HP 18184A Interface.

b. The following Interface Monitor displays should be on:

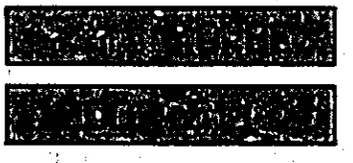
DTR	DSR
RTS	CTS
CD	RI

6. Turn the XTC, RTS, DTR, TD, ON/OFF switches to OFF.

   a. The INTERFACE Monitor Display should blank. MARK LCD will be on if ET is plugged into MARK/SPACE Monitor.

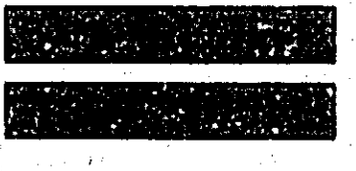
7. Turn the XTC, RTS, DTR, TD, ON/OFF switches to ON.

8. Press BEGIN/END and start a Bit Error test, the following should be displayed.

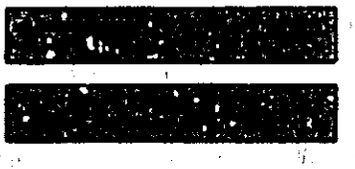


9. Press BEGIN/END to stop the test.

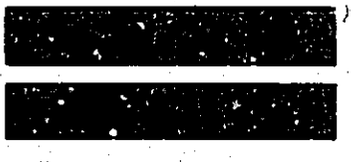
10. Press DATA BITS, the top level menu will be displayed.



11. Press DATA BITS again, select 5 Data Bits.

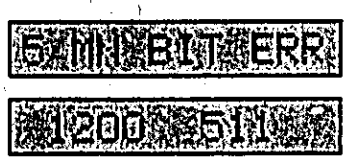


12. Press BEGIN/END to start a Bit error rate Test with asynchornonous framing. The following should be displayed

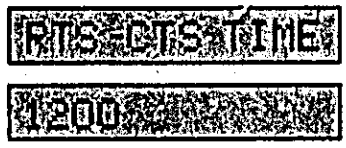


13. Press BEGIN/END to stop the test.

14. Press START UP, the top level menu will be displayed.



15. Press START UP again to select the RTS-CTS Delay Test.



a. The following INTERFACE Monitor Displays should be OFF.

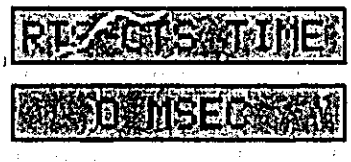
For the HP 18183A:

TD	RD
RTS	CTS
CD	RI

For the HP 18184A:

TD	RD
CD	RI
MARK	SPACE

16. Press BEGIN/END to start the test. The following should be displayed.



"TIME" and "0 MSEC" will be flashing when test is running.

To continue Performance Verification, go the paragraph 4-10.

4-9. PERFORMANCE VERIFICATION USING ET11293

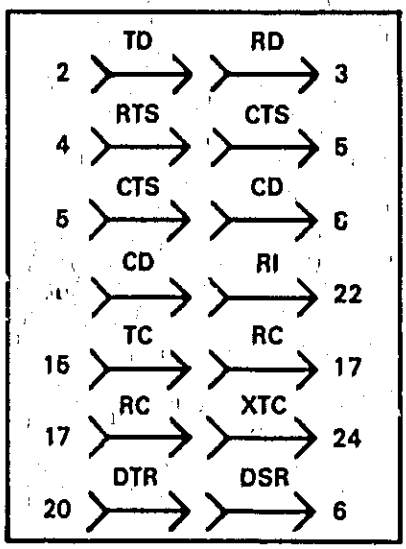
ET11293 is a test connector used to check the interface circuits. Table 4-2 lists the parts.

Table 4-2. Material List for ET11293

1251-0063	1	CONN RP 25M PLUG
1251-0352	1	CONN 145 BUSHING
1251-1438	1	CONN HOOD
1251-4431	1	CONN POT

The wire connections are the same as given in Table 4-3. To assemble the cable connect a 12 inch section of wire to pin 3 of the CONN RP 25M Plug (1251-0063) and attach the other end to the CONN Post. Attach the assembled ET11293 cable to the TO DCE connector on the interface. Plug the other end of the cable into the MARK/SPACE Monitor. Eight leads are required, the eighth lead connects pin 3 (RD) to the MARK/SPACE monitor.

Table 4-3. Breakout Box Switch Jumper Configuration



Return to step 4, paragraph 4-8 and follow the test procedures

4-10. EXTERNAL CLOCK TEST

Description

This test verifies operation of the HP 4925B at 72 kbits/sec.

Equipment Needed

HP 3325A	Function Generator
2 ea	22-26 AWG single strand wire

Test Set Up

1. Set up the Function Generator as follows:

Function	square wave
Amplitude	10 volts peak-to-peak
Frequency	72 kHz
DC Offset	0

HP 18183 (ET 11293 must be removed).

2. Set up the HP 4925B as follows:

   a. Set the XTC/RTS/DTR/TD switches to the ON position.

   b. Set the Breakout Box switches to the CLOSED position.

   c. Place a jumper between the Breakout Box switch pins as listed in Table 4-4.

Table 4-4. External Clock Test Jumpers

2 (TD)	to	3 (RD)
15 (TC)	to	17 (RC)

HP 18184A: ET 25113 must be connected with it's cover removed.

3. HP 18183A: Connect the Signal Generator output to Breakout Box switch at pins 7 (ground) and 15 (TC).
   HP 18184A: Connect the Signal Generator output to pin U (SCTE(A)) and pin B (ground).

Procedure

1. Turn the Bit Error Rate Test Set OFF, then ON.

2. Press the DATA RATE button until EXT is displayed.

3. Press the BEGIN/END button. The top display should read:

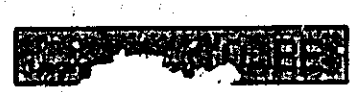


Table 4-5. Performance Verification Test Record

TEST	PASS	FAIL
SELF TEST		
INTERFACE MONITOR DISPLAY		
CONTIGUOUS BIT ERROR		
ASYNCHRONOUS BIT ERROR		
RTS-CTS DELAY		
EXTERNAL CLOCK		

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

The HP 4925B Bit Error Rate Test Set needs no adjustments.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section contains information for ordering replacement parts. Table 6-1 lists the abbreviations used, Table 6-2 is a list of replaceable parts, and Table 6-3 is a manufacturer's code list. Figure 6-1 is an exploded view of the instrument.

6-2 REPLACEABLE PARTS LIST

Table 6-2 lists the replaceable parts in alphanumeric order. Included is the description, quantity (total used in the instrument), HP part number, and manufacturer's part number. Chassis and mechanical parts are listed in Figure 6-1.

6-2. ORDERING INFORMATION

To order a listed part, quote the HP Part Number, indicate the quantity needed and address the order to the nearest Hewlett-Packard office. When ordering a part not listed, include the instrument model number, and serial number with a physical and functional description of the part. Address the order to the nearest Hewlett-Packard office.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	J	= electrical connector (stationary portion), jack	TB	= terminal board
B	= fan; motor	L	= coil, inductor	TP	= test point
BT	= battery	MP	= misc. mechanical part	U	= integrated circuit; microcircuit
C	= capacitor	P	= electrical connector (movable portion); plug	V	= electron tube; glow lamp
CR	= diode; diode thyristor; varactor	Q	= transistor; SCR; triode thyristor	VR	= voltage regulator; breakdown diode
DL	= delay line	R	= resistor	W	= cable
DS	= annunciator; lamp; LED	RT	= thermistor	X	= socket
E	= misc electrical part	S	= switch; jumper	Y	= crystal unit (piezo-electric or quartz)
F	= fuse	T	= transformer		
FL	= filter				
H	= hardware				

ABBREVIATIONS

A	= amperes	DIA	= diameter	K	= kilo (10^3), kilohm
AC	= alternating current	DIP	= dual in-line package	LED	= light emitting diode
ADD	= address	DPDT	= double-pole, double-throw	LFT	= left
ADJ	= adjust, adjustment	DPST	= double-pole, single-throw	LG	= long
AL	= aluminum	DR	= drive	LH	= lefthand
AR	= as required	DRVR	= driver	LKWR	= lockwasher
ASM	= algorithmic state machine	DSPL	= display	LP	= low pass
ASSY	= assembly	DTL	= diode-transistor logic	LS	= low power Schottky
				LSB	= least significant bit
B	= base	E	= emitter		
BCD	= binary coded decimal	ECL	= emitter-coupled logic	M	= milli (10^{-3}), male, mega (10^6), megohm
BeCu	= beryllium copper	ELECT	= electrolytic	MET FLM	= metal film
BIN	= binary	ENCAP	= encapsulated	MET OX.	= metal oxide
BLK	= black	EXT	= external	MHZ	= megahertz
BLU	= blue	EXTR	= extractor	MFR	= manufacturer
BP	= band pass			MINTR	= miniature
BRN	= brown	F	= female, farads	MISC	= miscellaneous
BRS	= brass	FF	= flip-flop	MOM	= momentary
BTU	= British thermal unit	FLM	= film	MOS	= metal oxide semiconductor
		FRNT	= front	MSB	= most significant bit
C	= collector	FXD	= fixed	MTCHD	= matched
CATH	= cathode			MTG	= mounting
CCW	= counterclockwise	G	= giga (10^9)	MTLC	= metallic
CD PL	= cadmium plate	GE	= germanium		
CER	= ceramic	GL	= glass	N	= nano (10^{-9})
CERMET	= ceramic met fln	GND	= ground(ed)	N.C.	= normally closed, no connection
CKTS	= circuits	GP	= General Purpose	NE	= neon
C FLM	= carbon film	GRA	= gray	NO.	= number
CLK	= clock	GRN	= green	N.O.	= normally open
CLR	= clear			NP	= No Polarity
CMOS	= complementary metal oxide semiconductor logic	H	= henries	NPN	= negative-positive-negative
		HDW	= hardware	NPO	= negative-positive zero (zero temperature coefficient)
COM	= common	HEX	= hexagon, hexagonal, six	NRFR	= not recommended for field replacement
COML	= commercial	HP	= high pass	NS	= normally shorting, nanosecond
COMP	= composition	HR	= hour(s)	NSR	= not separately replaceable
COMPL	= complete	HZ	= Hertz	NYL	= nylon
COND	= conductor				
CONN	= connector	IC	= integrated circuit	OBD	= order by description
CONT	= contact	ID	= inside diameter	OD	= outside diameter
CPRSN	= compression	IF	= intermediate frequency	ORN	= orange
CTL	= complementary transistor logic	IN.	= inch, inches		
CW	= clockwise	INCAND	= incandescent		
		INCL	= include(s)		
D	= diameter	INSUL	= insulation, insulated		
DC	= direct current	INT	= internal		
DEPC	= deposited carbon	INTL	= internal		

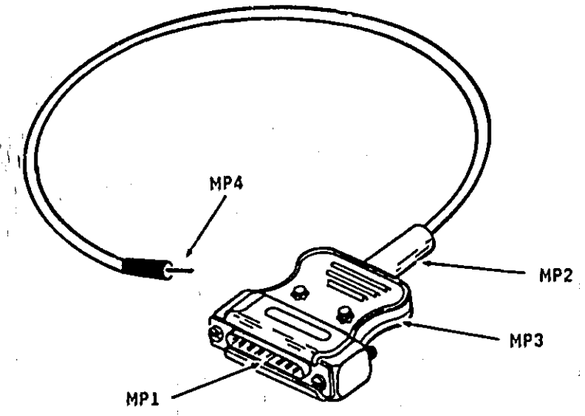
Table 6-1. Reference Designators and Abbreviations (cont)

ABBREVIATIONS

P = pico (10^{-12})	RVT = rivet	TRN = turn
PC = printed circuit	RWV = reverse working voltage	TTL = transistor-transistor logic
PCA = printed-circuit assembly		TYP = typical
PF = picofarad	S = second	
PIV = Peak Inverse Voltage	SB = slow blow	U (μ) = micro (10^{-6})
PK = peak	SCR = silicon controlled rectifier	UF = microfarad
PNL = panel	SE = selenium	US = microseconds
PNP = positive-negative-positive	SGL = single	
P-P = peak-to-peak	SI = silicon	V = volt(s)
PPM = parts per million	SHK = shank	VAR = variable
POLYC = polycarbonate	SIP = single in-line package	VCO = voltage controlled oscillator
POLYE = polyethylene	SKT = socket	VDCW = direct current working volts
POLYSTY = polystyrene	SLDR = solder	VIO = violet
PORC = porcelain	SPCG = spacing	VNP = no polarity voltage
POSN = position(s)	SPDT = single-pole, double-throw	
POZI = pozidrive	SPST = single-pole, single-throw	W = watts
PRV = peak reverse voltage	SST = stainless-steel	WT = weight
PWV = peak working voltage	STL = steel	WW = wirewound
P/O = part of	SZ = size	WHT = white
		WIP = wiper
R = ring	T = tip	WIV = working inverse voltage
RAM = random access memory	TA = tantalum	WSHR = washer
ROM = read only memory	TEL = telephone	
RECT = rectifier	T.C. = Temp. Compensated, temp. coefficient	X = times, multiple
RF = radio frequency		YEL = yellow
RH = right hand	THKNS = thickness	
RMS = root-mean-square	TI = titanium	ZNR = zener
RND = round	TGL = toggle	
RT = right hand	THD = thread	ϕ = phi, phase
RTL = resistor-transistor logic	THK = thick	
RTNT = retainer	TOL = tolerance	
RTRY = rotary	TRMR = trimmer	

Table 6-2. Manufacturer's Code List

Mfr No.	Manufacturer Name	Address	Zip Code
00000	ANY SATISF ICTORY SUPPLIER		
01121	ALLEN BRADLEY CO	MILWAUKEE WI	53204
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
11236	CTS OF BERNE INC	BERNE IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	
32293	INTERSIL INC	CUPERTINO CA	95014
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247



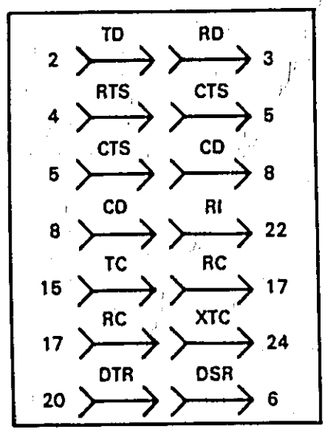
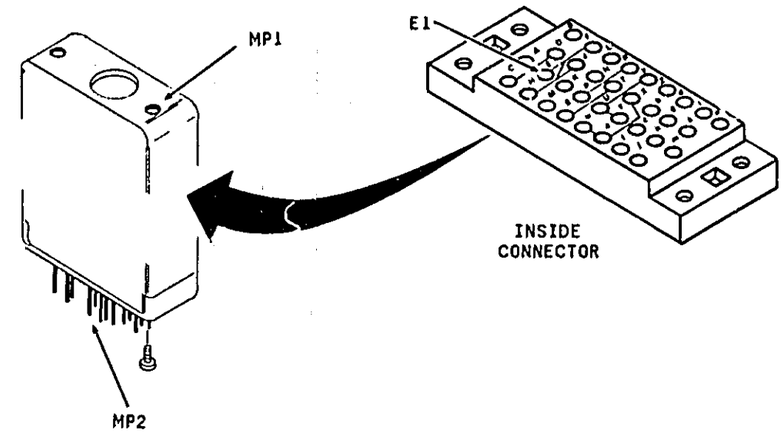


Figure 6-1. ET 11293

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP1	1251-0063	9	1	CONNECTOR RP 25M PLUG	04486	DBM-25P-K75
MP2	1251-0352	9	1	CONNECTOR 145 BUSHING	04486	CA18220-6
MP3	1251-1438	4	1	CONNECTOR HOOD	04507	DB-51226-1-A
MP4	1251-4431	3	1	CONNECTOR POST	03206	47792



Data Lines			Wire Together Connector Pins
RTS	⟶	CTS	C, D
DTR	⟶	CD, DSR, RI	H, F, E, J
SD(A)	⟶	RD(A)	P, R
SD(B)	⟶	RD(B)	S, T
SCTE(A)	⟶	SCR(A), SCT(A)	U, V, Y
SCTE(B)	⟶	SCR(B), SCT(B)	W, X, a

Figure 6-2. ET 25113

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP1	1251-4378	7	1	CONN 34-PIN M	05002	MRAC34PITC6H
MP2	1251-4588	1	16	CONTACT-CONN M	05002	100-2524P
E1	8150-0447	6	8	WIRE 24AWG (ANY COLOR ACCEPTABLE)	00000	ORDER BY DESCRIPTION

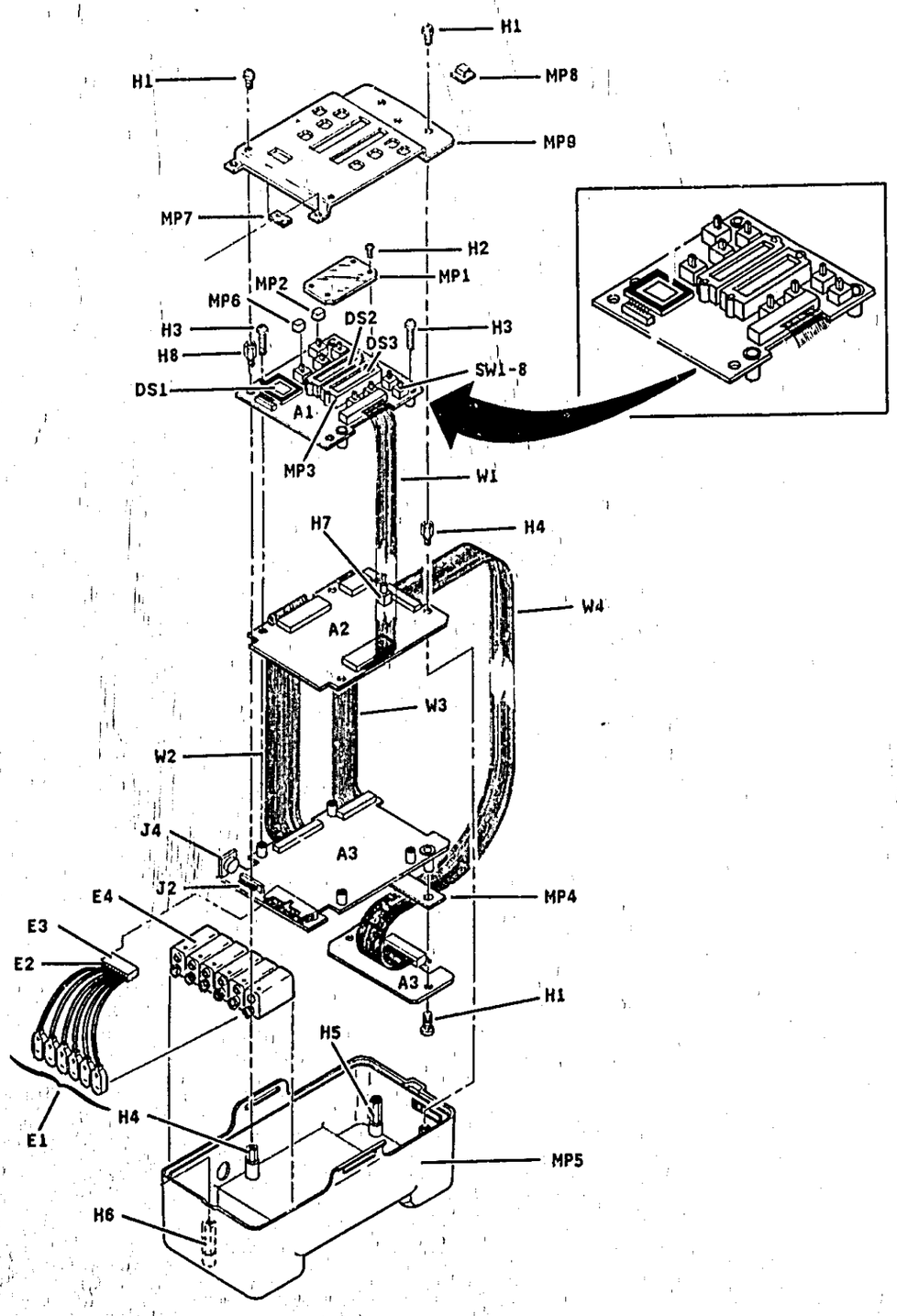


Figure 6-3. Exploded View HP 4925B

Table 6-3. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	04925-60021	3	1	A1 DISPLAY BOARD	28480	04925-60021
A2	04925-60022	4	1	A2 CONTROL BOARD	28480	04925-60022
A3	04925-60023	5	1	A3 TRANSMITTER/RECEIVER BOARD	28480	04925-60023
DS1	1990-0883	7	1	LCD BARGRAPH	02577	48613310
DS2	00041-60912	4	1	DISPLAY, 41C	28480	00041-60912
DS3	00041-60912	4	1	DISPLAY, 41C	28480	00041-60912
	04925-6[illegible]01	1		BATTERY ASSEMBLY (SEE E1-4FOR PART S)	28480	04925-62601
E1	1251-8056	6	6	BATTERY SNAPS	01674	CBS-301-01
E2	1251-3476	4	1	CONNECTOR	01380	66306-1
E3	1251-4745	2	1	CONN-POST-TP-BODY	03418	10-30-2121
E4	1420-0082	1	6	BATTERIES, 9V ALKALINE	05469	MN1604
H1	2360-0193	8	1	SCREW, 6-32,.25IN	05610	ORDER BY DESCRIPTION
H2	0520-0168	5	1	SCREW,2-56,.5IN	04771	ORDER BY DESCRIPTION
H3	2360-0250	8	2	SCREW-MACH, 6-32, 1IN	0000	ORDER BY DESCRIPTION
H4	0380-1823	3	2	STANDOFF, HEX SCREW .375-in	28480	0380-1823
H5	0380-1822	2	1	STANDOFF, HEX SCREW .75-in	02170	9741-B-0632-28
H6	0380-1824	4	1	STANDOFF, HEX	05108	8258
H7	3101-2620	7	1	SWITCH DPDT	02332	T201-V3-LH9CGE
H8	0590-0533	5	1	WIRE CLIP, PRESS ON	28480	0590-0533
J2	1251-4058	0	1	CONNECTOR 26 PIN M	04726	3429-1002
J4	1252-0431	7	1	CONNECTOR	28480	1252-0431
MP1	04925-20006	0	2	DISPLAY WINDOW	28480	04925-20006
MP2	3131-0469	7	2	KEYCAP, BLUE	28480	3131-0469
MP3	4040-2142	5	2	LCD CARRIER	08665	OMM-WD 76-MIN-LG BLK
MP4	5040-4478	5	2	LCD WINDOW	28480	5040-4478
MP5	04925-40021	0	1	HP 4925B HOUSING	28480	04925-40021
MP6	3131-0465	3	4	KEYCAP, BROWN	28480	3131-0465
MP7	04925-20009	3	1	COVER PLATE	28480	04925-20009
MP8	1400-0510	8	1	CABLE CLAMP	01924	8511-28-00-9909
MP9	04925-62621	3	1	HP 4925B FRONT PANEL	28480	04925-62621
SW1-8	3101-2603	2	8	SWITCH, LOW PROFILE, SPST	06257	M81E-0600
W1	04925-61604	0	1	W1, CABLE	28480	04925-61604
W2	04925-61603	9	1	W3, CABLE	28480	04925-61603
W3	04925-61601	3	1	W4 CABLE	28480	04925-61601
W4	04925-61606	2	1	W2 CABLE	28480	04925-61606

Table 6-3. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	04925-60021	9	1	DISPLAY BOARD ASSEMBLY	28480	04925-60021
A1C1	0160-5332	1	3	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5322
A1C2	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C3	0160-5312	7	2	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-5312
A1C4	0160-5312	7		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-5312
A1C5	0160-5332	1		CAPACITOR-FXD .1UF +-20% 100VDC CER	28480	0160-5322
A1CR201	1906-0074	1	1	DIODE ARRAY	28480	1906-0074
A1DS1	1990-0883	7	1	LCD BARGRAPH	28480	1990-0883
A1DS2	00041-60912	7	1	LCD BARGRAPH	28480	00041-60912
A1DS3	1990-0883	7	1	LCD BARGRAPH	28480	1990-0883
A1DS4	1990-0883	7	1	LCD BARGRAPH	28480	1990-0883
A1E1	1258-0141	8	1	REMOVEABLE JUMPER	28480	1258-0141
A1E1	1251-5285	7	1	CONNECTOR-POST-TP-HDR	28480	1251-5285
A1J4	04925-61604	8	1	CABLE TRANSITION	28480	04925-61604
MP1	04925-20006	0	2	LCD WIDOW	28480	04925-20006
MP2	4040-2142	5	2	LCD CARRIER	28480	4040-2142
MP3	4040-2142	5		LCD CARRIER	28480	4040-2142
A1R1	0757-0467	8	1	RESISTOR 121K 1% .125W F TC=0+-100	24546	CS-1/8T0-1213-F
A1R2	0757-0458	7	1	RESISTOR 61.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6112-F
A1R301	1810-0037	3	1	RESISTOR-NETWORK 8-DIP 1.0K X 8	11236	761-3-R1K
A1R401	1810-0208	0	1	RESISTOR-NETWORK 8-SIP 68K X 7	01121	208A683
A1S1	3131-0469	7	1	KEYCAP-BLUE	28480	3131-0469
A1S2	3131-0465	3	7	KEYCAP-BROWN	28480	31310465
A1S3	3131-0465	3		KEYCAP-BROWN	28480	31310465
A1S4	3131-0465	3		KEYCAP-BROWN	28480	31310465
A1S5	3131-0465	3		KEYCAP-BROWN	28480	31310465
A1S6	3131-0465	3		KEYCAP-BROWN	28480	31310465
A1S7	3131-0465	3		KEYCAP-BROWN	28480	31310465
A1S8	3131-0465	3		KEYCAP-BROWN	28480	31310465
A1SW1	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1SW2	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1SW3	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1SW4	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1SW5	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1SW6	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1SW7	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1SW8	3101-2603	2	8	SWITCH-LOW PROFILE	28480	3101-2603
A1TP1	1251-8360	5	3	CONNECTOR-SEL CONTACT	28480	1251-6947
A1TP2	1251-8360	5		CONNECTOR-SEL CONTACT	28480	1251-6947
A1TP3	1251-8360	5		CONNECTOR-SEL CONTACT	28480	1251-6947
A1U101	1820-2466	7	1	IC TIMER CMOS	32293	ICM7555IPA
A1U200	1820-1672	6	3	IC GATE CMOS EXCL-NOR QUAD 2 INP	3L585	CD4077BE
A1U300	1820-1672	6		ICGATE CMOS EXCL-NOR QUAD 2 INP	3L585	CD4077BE
A1U400	1820-1672	6		IC-GATE CMOS EXCL-NOR QUAD 2 INP	3L585	CD4077BE
A1XDS1	1200-0863	7	14	SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-086
A1XDS2	1200-0863	7		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-086
A1XDS3	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-086
A1XDS4	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-086
A1XDS5	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS6	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS7	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS8	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS9	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS10	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS11	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS12	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS13	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
A1XDS14	1200-0868	6		SOCKET STRP 7-CONT DIP-SOLDR	28480	1200-0868
	0520-0168	5	4	SCREW MACH 2-56 .5IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
	0590-0533	5	4	THREADED INSERT-NUT 2-56 .06-IN-LG SST	28480	0590-0533
	04925-20021	9	1	DISPLAY WINDOW BLANK	28480	04925-20021

Table 6-3. Replaceable Parts (cont)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	04925-60002	0	1	CONTROL BOARD	28480	04925-60002
A2C1	0160-5332	1	14	CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C2	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C3	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C4	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C5	0160-5332	9		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C6	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C7	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C8	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C9	0160-3508	2	1	CAPACITOR-FXD 1UF +-5% 100VDC CER	28480	0160-3508
A2C10	0160-5309	2	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A2C11	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A2C12	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C13	0180-1746	5	1	CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
A2C14	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C15	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C16	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C17	0180-0374	3	1	CAPACITOR-FXD 10UF +-10% 20%VDC TA	56289	150D106X9020B2
A2C18	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A2C19	0160-5322	9		CAPACITOR-FXD 10pF 5% C	28480	0160-5322
A2C20	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0165-5332
A2C21	0160-5322	9		CAPACITOR-FXD 10pF 5% DC	28480	0165-5322
A2CR1	1901-0050	3	1	DIODE-SWITCHING 80V 200MA 1NS DO-35	02237	FDH6308
A2E2	1258-0141	8	4	JUMPER-REM	2848	1258-0141
A2E1-CCITT	1251-5285	7	2	CONECTOR-POST-TP-HDR	28480	1251-5285
A2E1	1258-0141	8		JUMPER-REMOVABLE	28480	1258-0141
A2XE2	1251-8360	5	25	CONNECTOR POST	28480	1251-8360
A2E3	1258-0141	8		JUMPER-REM	2848	1258-0141
A2XE3	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2XE4	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2XE5	1200-0607	0	1	SOCKET-IC 16 CONT DIP DIP-SLDR	28480	1200-0607
A2E5	1251-4787	2	1	SHUNT-8 POSITION	28480	1251-4787
A2E6	1251-5285	7		CONNECTOR-POST-TP-DBR	28480	1251-5285
A2E7	1258-0141	8		JUMPER REMOVABLE	28480	1251-0141
A2XE7	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2XE8	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2J3	1251-0475	7		CONNECTOR-SEL CONTACT	28480	1251-0475
A2J4	1251-0476	7		CONNECTOR-SEL CONTACT	28480	1251-0475
A2J12	1251-0475	7		CONNECTOR-SEL CONTACT	28480	1251-0475
A2U506	1826-1005	0	1	VOLTAGE REGULATOR	28480	1826-1005
A2R1	0757-0280	3	4	RESISTOR 1K 1% .125w F TC=0+-100	24546	C4-1/8-TO-1001-F
A2R2	0698-3458	7	1	RESISTOR 348K 1% .125w F TC=0+-100	28480	0698-3458
A2R3	0757-0438	3	2	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1.8-TO-5111-F
A2R4	0757-0438	3	2	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1.8-TO-5111-F
A2R5	0698-3359	7	1	RESISTOR 12.7K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1272-F
A2R6	0837-0220	1	1	THERMISTOR ROD	28480	0837-0220
A2R7	0698-3457	6	7	RESISTOR 316K 1% .125W F TC=0+-100	05524	CMF-55-1,T-1
A2R8	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	05524	CMF-55-1,T-1
A2R9	0757-0465	6	4	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1003-F
A2R10	0757-0470	3	1	RESISTOR 162K 1% .125w F TC=0+-100	24546	C4-1/8-TO-1623-F
A2R11	0757-0466	7	1	RESISTOR 110K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1103-F
A2R12	0757-0458	7		RESISTOR 51.1K 1% .125w F TC=0+-100	24546	C4-1/8-TO-5112-F
A2R13	0683-1555	0	2	RESISTOR 1.5M 5% .25w FC TC=-900/+1100	01121	CB1555
A2R14	0683-1555	0	2	RESISTOR 1.5M 5% .25w FC TC=-900/+1100	01121	CB1555
A2R15	0757-0465	6		RESISTOR 100K 1% .125w F TC=0+-100	24546	C4-1/8-TO-1003-F
A2R16	0757-0465	6		RESISTOR 100K 1% .125w F TC=0+-100	24546	C4-1/8-TO-1003-F
A2R17	0698-3454	3	1	RESISTOR 215K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2153-F
A2R18	0757-0465	6		RESISTOR 100K 1% .125w F TC=0+-100	24546	C4-1/8-TO-1003-F
A2R19	0683-1565	2		RESISTOR 15M 15% .25w FC TC=900/M200	01121	CB1565
A2R20	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A2R21	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A2R22	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A2R101	1810-0208	0	2	RESISTOR-NETWORK 8-SIP 6.8 X 7	01121	208A683
A2R106	1810-0208	0	2	RESISTOR-NETWORK 8-SIP 6.8 X 7	01121	208A683
A2R205	1810-0453	7	3	RESISTOR-NETWORK 10 SIP 56.0k X 9	28480	1810-0453
A2R301	1810-0208	0	2	RESISTOR-NETWORK 8-SIP 6.8 X 7	01121	208A683
A2R406	1810-0453	7	3	RESISTOR-NETWORK 10 SIP 56.0k X 9	28480	1810-0453
A2R601	1810-0560	7	1	RESISTOR-NETWORK 16DIP 5.6K X 8	28480	1810-0560
A2R603	1810-0453	7	3	RESISTOR-NETWORK 10 SIP 56.0k X 9	28480	1810-0453
A2SW1	3101-2620	3	1	SWITCH	28480	3101-2620
A2TP104	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP105	1251-8360	5		CONNECTOR POST	28480	1251-8360

Table 6-3. Replaceable Parts (cont)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2TP106	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP107	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP108	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP109	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP110	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP401	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP403	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP504	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP406	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP602	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP603	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP705	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2TP707	1251-8360	5		CONNECTOR POST	28480	1251-8360
A2U101	1820-0939	5	5	IC FF CMOS D-TYPE POS-EDGE-TRIG DUAL	28480	1251-1820-0939
A2U104	1826-0501	9	2	IC MULTIPLXR 2-CHAN-ANLG TRIPLE 16 DIP-P	04713	MC14053BCP
A2U106	04925-10021	5	1	EPROM-PROGRAMMED	28480	04925-10021
A2XU106	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A2U201	1820-1970	6	3	IC GATE CMOS OR QUAD 2-INP	04713	MC14071BCP
A2U202	1820-0939	5		IC FF CMOS D-TYPE POS-EDGE-TRIG DUAL	3L585	CD4013BE
A2U203	1820-3082	6	1	IC MC74HC374N	28480	1820-3082
A2U204	1826-0501	9		IC MULTIPLXR 2-CHAN-ANLG TRIPLE 16 DIP-P	04713	MC14053BCP
A2U301	1820-0939	5		IC FF CMOS D-TYPE POS-EDGE-TRIG DUAL	3L585	CD4013BE
A2U302	1820-1150	4	2	IC CNTR CMOS BIN SYNCHRO DUAL 4-BIT	04713	MC14520BCP
A2U303	1820-2998	0	2	IC-MC74HC373N	28480	1820-2998
A2U304	1820-2812	3	1	IC NSC810 RAM I/O	28480	1820-2812
A2XU304	1251-0475	7		CONNECTOR-SEL CONTACT	28480	1251-0475
A2U306	1820-2998	0		IC-MC74HC373N	28480	1820-2998
A2U401	1820-1970	6		IC GATE CMOSOR QUAD 2-INP	04713	MC14071BCP
A2U402	1820-1150	4		IC CNTR CMOS BIN SYNCHRO DUAL 4-BIT	04713	MC14520BCP
A2U403	1820-1241	4	3	IC MUXR/DATA-SEL CMOS 8 TO 1 LINE 8-INP	3L585	CD4512BE
A2U404	1820-1241	4	3	IC MUXR/DATA-SEL CMOS 8 TO 1 LINE 8-INP	3L585	CD4512BE
A2U405	1820-0946	4	1	ICGATE CMOS NOR QUAD 2-INP	3L585	CD4001UBE
A2U406	1820-2970	8	1	MICROPROCESSOR	28480	1820-2970
A2U501	1820-2466	7	1	IC TIMER CMOS	32293	ICM7555IPA
A2U502	1820-0939	5		IC FF CMOS D-TYPE POS-EDGE-TRIG DUAL	3L585	CD4013BE
A2U503	1820-1779	3	1	IC GEN CMOS	04713	MC14411P
A2U504	1820-2924	2	1	ICMC74HC02N	28480	1820-2924
A2U505	1820-1970	6		IC GATE CMOS OR QUAD 2-INP	04713	MC14071BCP
A2U506	1826-1005	1	1	IC-VOLTAGE REGULATOR 4.5/5.5 V	03406	LM2930P-5.0TB
A2U602	1820-1356	2	1	IC HV CMOS MONOSTBL RETRIG/RESET DUAL	04713	MC14528BCP
A2U604	1820-0939	5		ICFFCMOS D-TYPE POS-EDGE-TRIG DUAL	3L585	CD4013BC
A2U605	1820-1544	0	1	ICFF CMOS D-TYPE COM CLOCK QUAD	3L585	CD4076BF
A2U704	1820-1241	4		IC MXR/DATA-SEL CMOS 8 TO 1 LINE 8-INP	3L585	CD4512BE
A2U705	1826-0759	9	1	IC COMPARATOR GP QUAD 14 DP-C PKG	04713	LM339J
A2X1	0410-1004	7	1	CRYSTAL 1.8432 MHZ	28480	0410-1004
A2X2	0410-0726	8	1	CRYSTAL 6.00000 MHZ	28480	0410-0726
A2XU304	1200-0475	2	1	SOCKET	28480	1200-0475
	04925-61606	2		CABLE ASSEMBLY, J13, J14	28480	04925-61606
	2200-0103	2	1	SCREW, MACHINE 4-40 .250	00000	ORDER BY DESCRIPTION
	2260-0002	6	1	NUT, HEX .187	00000	ORDER BY DESCRIPTION

Table 6-3. Replaceable Parts (cont)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	04925-60023	1	1	TRANSMITTER/RECIEVER BOARD ASSEMBLY	28480	04925-60023
A3C1	0160-5332	1	14	CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C2	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C3	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C4	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C5	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C6	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C7	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C8	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C9	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C12	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C13	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C14	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3C15	0160-5332	1		CAPACITOR-FXD .1 UF 20% 50VDC	28480	0160-5332
A3CR1	1901-1080	1	6	DIODE-SCHOTTKY IN5817 20V 1A	28480	1901-1080
A3CR2	1901-1080	1		DIODE-SCHOTTKY IN5817 20V 1A	28480	1901-1080
A3CR3	1901-1080	1		DIODE-SCHOTTKY IN5817 20V 1A	28480	1901-1080
A3CR4	1901-1080	1		DIODE-SCHOTTKY IN5817 20V 1A	28480	1901-1080
A3CR5	1901-1080	1		DIODE-SCHOTTKY IN5817 20V 1A	28480	1901-1080
A3CR6	1901-1080	1		DIODE-SCHOTTKY IN5817 20V 1A	28480	1901-1080
A3CR101	1906-0074	1		DIODE ARRAY	28480	1906-0074
A3CR102	1906-0074	1	2	DIODE ARRAY	28480	1906-0074
A3E1	1251-5295	7	4	CONNECTOR-POST-TP-HDR	28480	1251-5285
A3E1	1258-0141	8	4	JUMPER-REM	28480	1258-0141
A3E2	1258-0141	8		JUMPER-REM	28480	1258-0141
A3E3	1251-5285	7		CONNECTOR-POST-TP-HDR	28480	1251-5285
A3E3	1258-0141	8		JUMPER-REM	28480	1258-0141
A3E2	1251-5285	7		CONNECTOR-POST-TP-HDR	28480	1251-5285
A3E4	1251-5285	7		CONNECTOR-POST-TP-HDR	28480	1251-5285
A3E4	1258-0141	8		JUMPER-REM	28480	1258-0141
A3J1	1251-5288	0	1	CONNECTOR-POST-TP-HDR	28480	1251-5288
A3J2	1251-4056	0	1	CONNECTOR-26 PIN (MALE)	28480	1251-4056
A3J4	1251-0431	7	1	CONNECTOR, 3-PIN	28480	1251-0431
A3R201	1810-0157	3		RESISTOR-NETWORK 16-DIP 1.0K X 8	11236	761-3-R1K
A3R400	1810-0280	8	6	RESISTOR-NETWORK 8-SIP 10.0k X 9	28480	1810-0280
A3R401	1810-0280	8		RESISTOR-NETWORK 8-SIP 10.0k X 9	28480	1810-0280
A3TP1	1281-8360	0	7	CONNECTOR-POST .025 SA	28480	1281-8360
A3TP2	1281-8360	0		CONNECTOR-POST .025 SA	28480	1281-8360
A3TP3	1281-8360	0		CONNECTOR-POST .025 SA	28480	1281-8360
A3TP4	1281-8360	0		CONNECTOR-POST .025 SA	28480	1281-8360
A3TP5	1281-8360	0		CONNECTOR-POST .025 SA	28480	1281-8360
A3TP302	1281-8360	0		CONNECTOR-POST .025 SA	28480	1281-8360
A3TP405	1281-8360	0		CONNECTOR-POST .025 SA	28480	1281-8360
A3TP400	1281-8360	0		CONNECTOR-POST .025 SA	28480	1281-8360
A3U103	1820-1328	8	3	IC CNTR CMOS BIN 4-BIT	04713	MC14526BCP
A3U104	1820-2031	2	1	IC SHF-RGTR CMOS ASYNCHRO PRL-IN	3L585	CD4021BE
A3U202	1820-1960	4	2	IC GATE CMOS NAND DUAL 4-INP	04713	MC14012BCP
A3U203	1820-0939	5	3	IC FF CMOS D-TYPE POS EDGE TRIG DUAL	3L585	CD4013BE
A3U204	1820-1471	2	3	IC MUXR/DATA-SEL CMOS 4 TO 1 LINE DUAL	04713	MC14539BCP
A3U205	1820-2204	1	1	IC UART CMOS	32293	IM6402-1IPL
A3U301	1820-0949	7	3	IC DIGITAL GATE	3L585	CD4011UBE
A3U302	1820-1150	4	3	IC CNTR CMOS BIN SYNCHRO DUAL 4-BIT	04713	MC14520BCP
A3U303	1820-2014	1	2	IC INV CMOS HEX 04713	04713	MC14069UBCP
A3U304	1820-0939	5		IC FF CMOS D-TYPE POS EDGE TRIG DUAL	3L585	CD4013BE
A3U305	1826-0501	9	1	IC MULTIPLXR 2-CHAN-ANLG TRIPLE 16-DIP-P	04713	MC14053BCP
A3U306	1820-2232	5	3	IC RGTR CMOS 8-BIT	04713	MC14034BCP
A3U401	1820-1150	4		IC CNTR CMOS BIN SYNCHRO DUAL 4-BIT	04713	MC14520BCP
A3U402	1820-2014	1		IC INV CMOS HEX	04713	MC14069UBCP
A3U403	1820-1486	9	1	IC GATE CMOS AND QUAD 2-INP	3L585	CD4081BE
A3U404	1820-0976	0	2	IC SHF-RGTR CMOS D-TYPE SERIAL-IN	3L585	CD4015BE
A3U405	1820-0976	0	2	IC SHF-RGTR CMOS D-TYPE SERIAL-IN	3L585	CD4015BE
A3U408	1820-1601	0	3	IC GATE CMOS EXCL-OR QUAD 2-INP	3L585	CD4070BE
A3U501	1820-1960	4		IC GATE CMOS NAND DUAL 4-INP	04713	MC14012BCP
A3U502	1820-2268	5	1	IC FF CMOS D-TYPE POS-EDGE-TRIG COM	04713	MC14174BCP
A3U503	1820-1328	8		IC CNTR COMOS BIN 4-BIT	04713	MC14526BCP
A3U601	1820-3146	2	1	IC MV CMOS MNOSTBL RETRIG/RESET DUAL	04713	MC74HC175N
A3U602	1820-1150	4		IC CNTR CMOS BIN SYNCHRO DUAL 4-BIT	04713	MC14520BCP
A3U603	1820-0949	7		IC GATE CMOS NAND QUAD 2-INP	3L585	CD4011UBE
A3U604	1820-2232	5		IC RGTR CMOS 8-BIT	04713	MC14034BCP
A3U605	1820-1601	0		IC GATE CMOS EXCL-OR QUAD 2-INP	3L585	CD4070BE
A3U606	1820-1471	2		IC MUXR/DATA-SEL CMOS 4 TO 1 LINE DUAL	04713	MC14539BCP
A3U702	1820-0939	5		IC FF CMOS D-TYPE POS-EDGE-TRIG- DUAL	3L585	CD4013BE

Table 6-3. Replaceable Parts (cont)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U703	1820-1328	8		IC CNTR CMOS BIN 4-BIT	04713	MC14526BCP
A3U704	1820-2232	5		IC RGTR CMOS 8-BIT	04713	MC14034BCP
A3U705	1820-1471	2		IC MUXR/DATA-SEL CMOS 4 TO 1 LINE SUAL	04713	MC14539BCP
A3U706	1820-1601	0		IC GATE CMOS EXCL-OR QUAD 2-INP	3L585	CD4070BE
	1251-5595	2	2	POLARIZING KEY	28480	1251-5595
	0380-0159	6	4	STANDOFF	28480	0380-0159
	0360-0809	3	2	STANDOFF	28480	0380-0809
	04925-61601	7	1	CABLE J12	28480	04925-61601
	04925-61603	9	1	CABLE J3	28480	04925-61603
	5040-4478	5	1	LENS	28480	5040-4478
				MISCELLANEOUS PARTS		
	04925-62601	9	2	BATTERY ASSEMBLY	28480	04925-62601
	1251-3476	4	12	CONNECTOR-SC IF RECEPTACLE	28480	1251-3476
	1251-8056	6	6	BATTERY SNAPS	28480	1251-8056
	1420-0082	1	6	BATTERY 9V	28480	1420-0082
	1251-4745	2	2	CON-POST-TP-BD4		
	0380-0388	3	6	STNNJOFF-HEX .375 IN LG 6-32 THD	28480	0380-0388
	0360-0570	5	1	STANDOFF	00000	ORDER BY DESCRIPTION
	0380-0150	9	2	STANDOFF-HEX .75 IN	00000	ORDER BY DESCRIPTION
	2360-0193	8	6	SCREW-MACH 6-32 .25IN LG PAN HD-POZI	00000	ORDER BY DESCRIPTION
	2360-0705	3	4	SCREW-MACH 6-32 .75 IN LG PAN HD POZI	00000	ORDER BY DESCRIPTION
	04925-0201	9	1	BATTERY ASSEMBLY	28480	04925-62601
	04925-62602	0	1	FRONT PANEL ASSEMBLY	28480	04925-62602
	04925-90001	2	1	OPERATING/SERVICE MANUAL	28480	04925-90001
	5040-4478	5	1	LCD WINDOW	28480	5040-4478
	04925-40001	9	1	SOFT CARRYING CASE	28480	04925-40001
	04925-61608	0	7	PATCH WIRE	28480	04925-61608
	04925-20007	1	1	COVER PLATE	28480	04925-20007
	04925-20005	9	1	PANEL PLUG	28480	04925-20005

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

This section contains information to backdate this manual for instruments with serial prefix numbers lower than the number listed on the Title Page. It may also contain information about compatibility with other Bit Error Rate Test Set software.

7-2. MANUAL CHANGES

To adapt this manual to your instrument, make the changes listed in Table 7-1. Changes are listed by serial prefix number, make the changes in the order they are described.

For instruments with serial prefixes greater than the one shown on the Title Page, any changes are described in a yellow Manual Changes supplement.

Table 7-1. Manual Changes

Instrument Serial No.	Make Changes
There are no changes at this time	

SECTION VIII
SERVICE

8-1. INTRODUCTION

This section provides information to troubleshoot and repair the HP 4925B Bit Error Rate Test Set. Information includes a theory of operation, assembly procedures, troubleshooting techniques, component locators, and schematics. Information for the interfaces is contained in Appendix C (HP 18183A) and Appendix D (HP 18184A). The AC power module is described in Appendix E.

8-2. MAINTENANCE

Maintenance is divided between Periodic Maintenance and Troubleshooting to repair.

8-3. PERIODIC MAINTENANCE

Periodic maintenance on the HP 4925B should be done semi-annually. It is a two step procedure consisting of preventive maintenance and Performance Verification.

Preventive Maintenance consists of incorporating any modifications made to the instrument since the last periodic maintenance, and overall cleaning of the assemblies to minimize leakage paths, etc. After performing any preventive maintenance, complete the tests in Section IV, Performance Tests.

8-4. THEORY OF OPERATION

The theory of operation contains an assembly-by-assembly description of the instrument. Detailed block diagrams are located just before the schematics.

8-5. TROUBLESHOOTING

This manual provides two methods to isolate a problem to a particular assembly. The first method is to use the results of the Performance Tests. The second method uses the overall block diagram and the block diagrams to isolate a problem to a particular assembly. Troubleshooting procedures are divided into three parts: Troubleshooting without the Display, Troubleshooting with Self Test, and Signature Analysis.

8-6. RECOMMENDED TEST EQUIPMENT

Test equipment recommended to perform the troubleshooting procedures for the Bit Error Rate Test Set is listed in Table 1-2. Equipment with equivalent characteristics may be used.

8-7. GENERAL HANDLING OF STATIC SENSITIVE DEVICES

Observe the following guidelines when handling static sensitive devices.

1. Wear a wrist strap which contacts the bare skin and is properly grounded.
2. All equipment, such as soldering irons, fixtures, storage containers, shelving, and so on must be grounded.
3. Work areas must be clear of non-conductive material. No plastics, polyurethane bags, coffee cups, candy wrappers, cigarette packs, or untreated trays should be near the work station.
4. Clothing should never come in contact with components or assemblies. Wear short sleeves or rolled up long sleves, or preferably an antistatic smock.
5. Use antistatic solution on all work benches, table mats, hand tools, storage containers, chair seat, and back rests.
6. Static sensitive devices must be protected at all times. Keep the devices in their antistatic packaging.
7. All work must be performed at a static safe work station. A static safe work station has the following.

   a. Conductive tablemat connected to ground through 1 M resistor.

   b. Wrist strap grounded through 1 M resistor.

   c. All test equipment tied to one common ground.

8-8. DISASSEMBLY/ASSEMBLY PROCEDURES

Proceed with the disassembly/assembly procedures after reading paragraph 8-7, General Handling of Static Sensitive Devices.

Equipment

1 #1 posidrive screwdriver
1 1/4" nutdriver
1 slotted screwdriver
static safe work area
ground strap

8-9. DISASSEMBLY PROCEDURE

1. Remove the four 6-32 screws from the HP 4925B front panel and the two 6-32 screws from the interface. Figure 8-1 shows the screw locations.

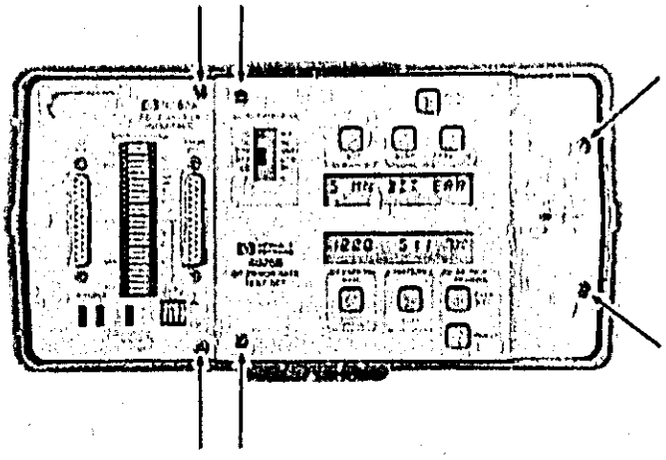


Figure 8-1. Front Panel Screw Location

2. Loosen the captive screw on the interface and lift up the interface assembly.
3. Disconnect W5 the cable connecting the interface to the HP 4925B. Take the interface out of the unit. Follow steps a-c to disassemble the interface.
   a. Remove the 4-40 screws securing the interface front panel to its printed circuit assemblies.
   b. Turn the interface printed circuit boards over and remove the four screws.
   c. The two boards will unfold and lie flat for easy troubleshooting.
4. Disconnect W7, the battery cable and remove the batteries.
5. Lift the Bit Error Rate Test Set panel out of the unit. It may be necessary to slightly separate the sides of the case to remove the panel.
6. Use the nutdriver and remove the 4 hex standoff screws.
7. Hold the edges of the top board (A1) and lift the board assemblies out of the case.

CAUTION

Place the board assemblies on a static protected work area only.

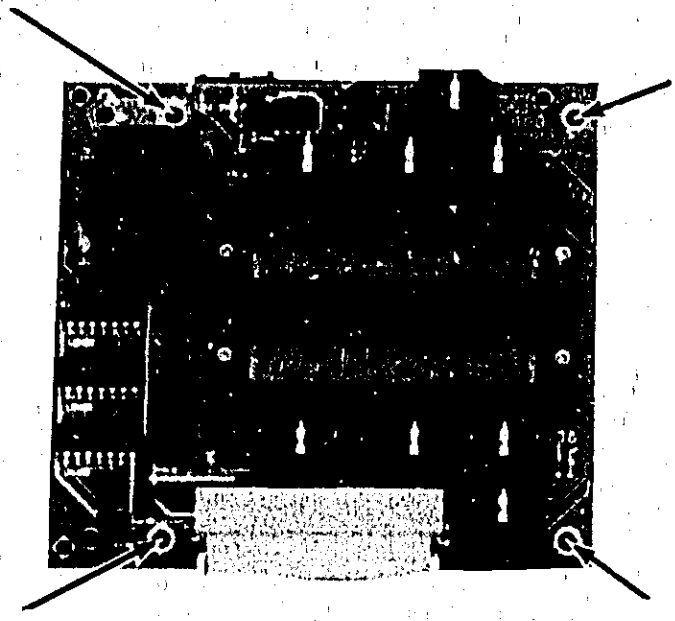


Figure 8-2. Display Board Screw Locations

8. Separate the PC boards for testing.

   a. Orient the printed circuit boards so that the LCD displays lay face down.

   b. Remove the two screws holding A3(b) in place.

   c. Turn the boards so that the LCD displays face up.

   d. Remove the four screws on the A1 Display Board as shown in Figure 8-2.

   e. Unfold the boards and lay them flat on the bench for troubleshooting.

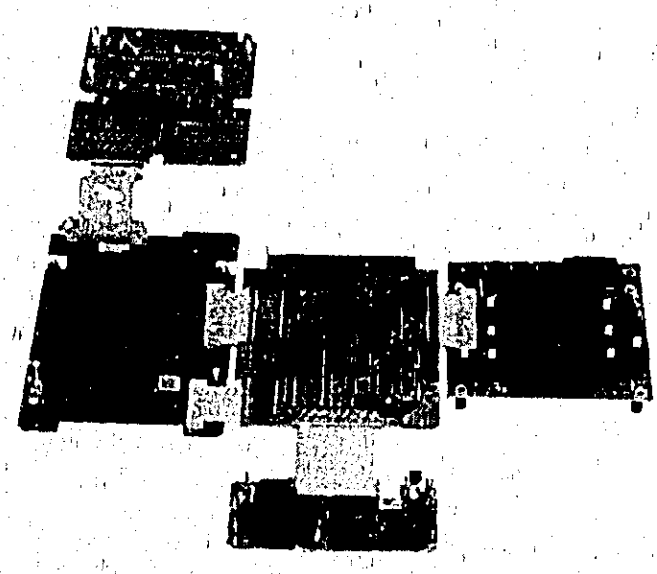


Figure 8-3. Printed Circuit Boards Ready for Troubleshooting

f. If necessary W1, W3, and W4 may be disconnected for isolated board troubleshooting.

CAUTION

When the boards are separated, terminate the connectors with a piece of conductive foam.

8-10. ASSEMBLY

1. Assemble the PC boards.

   a. Connect W1, W3, and W4 if necessary.

   b. Fold the boards back up. A1, the Display Board goes on top, fold A2, the Control Board under it, put A3, the Transmitter/Receiver Board under A2. Secure the shield under A3. Figure 8-4 illustrates the correct board sequence.

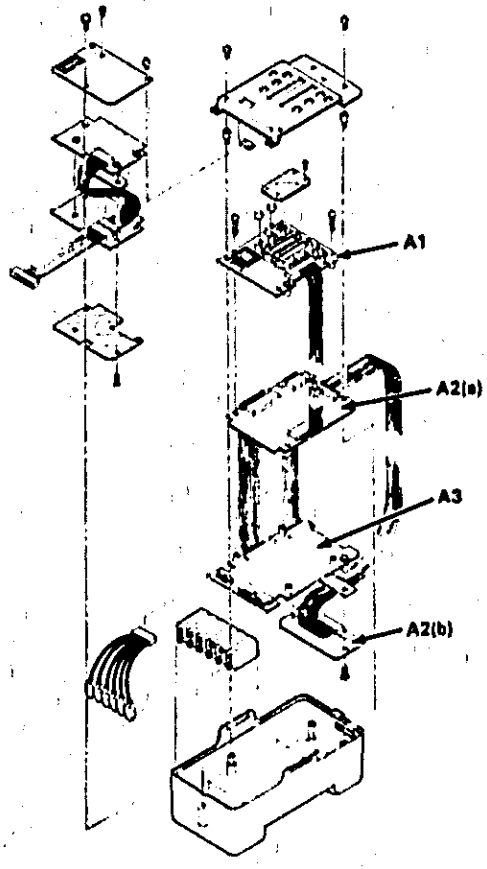


Figure 8-4. Board Assembly Sequence HP 4925B

c. Insert and secure to finger-tight the screws on the A1, Display Board.

d. Turn the printed circuit assemblies so that the LCD display is face down on the static protected work station.

e. To replace A2(b) bend W2 under A3 the Control Board. Insert and secure the two 6-32 screws.

f. Turn the boards so that the LCD display is face up.

2. Place printed circuit assemblies A1, A2, and A3 into the case. If necessary slightly separate the sides of the case to drop the boards into place.

3. Insert the four hex standoff screws and secure finger tight with the nutdriver. If the holes do not line up, press the board assembly as close to the side of the case as possible.

4. Replace and attach the Bit Error Rate Test Set front panel. Once again, it may be necessary to separate the case slightly to seat the panel.

a. If the panel still doesn't seat correctly, push the Display board around gently until it seats.

5. Replace the batteries and cable. Orient the battery cable with the red wire towards the HP label on the Bit Error Rate Test Set panel.

6. Connect W3 to A2, the Control board.

7. Press the Interface assembly into place, it should fit snugly.

8. Replace and tighten the two 6-32 screws on the Interface. Secure the captive screw.

9. To verify operation, complete the Performance Verification tests given in Section IV.

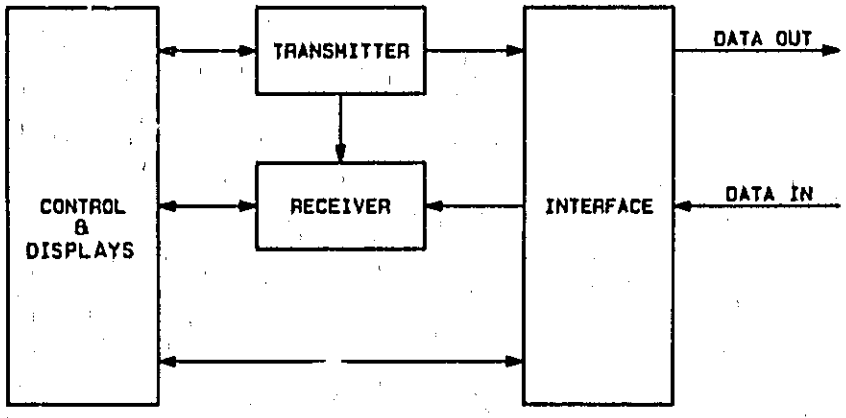


Figure 8-5. Overall HP 4925B Block Diagram

8-11. THEORY OF OPERATION

The HP 4925B is a portable Bit Error Rate Test Set. The circuits are primarily CMOS technology. Three multilayer PC boards make up the three major functional assemblies described below.

8-12. Control Board.

This board contains the microprocessor, program memory, I/O expansion, RAM, bit rate generator, and bit error event buffers. All instrument control, data collection, and computation is initiated from the microprocessor.

8-13. Transmitter/Receiver Board.

This random logic assembly generates, transmits, receives, synchronizes to, and detects errors in framed and unframed Pseudo Random Bit Sequences (PRBS).

8-14. Display Board.

The Display Board contains three LCDs. Two of the displays are integrated modules from the HP 41C calculator while the third is a custom dual six segment bargraph driven by random logic. The assembly also contains the 8 key switches that form a keyboard matrix serviced by the microprocessor.

8-15. A1 DISPLAY BOARD THEORY OF OPERATION

8-16. INTERFACE ACTIVITY DISPLAY

LCD bargraph display DS1 indicates the status of several key interface lines. The following lines are monitored:

TD	-	Transmit Data	RD	-	Receive Data
TC	-	Transmit Clock	RC	-	Receive Clock
DTR	-	Data Terminal Ready	DSR	-	Data Set Ready
RTS	-	Request To Send	CTS	-	Clear To Send
CD	-	Carrier Detect	RI	-	Ring Indicator

There are two other indicators which display the status of a non-dedicated monitor input. The space indicator turns on when the input is greater than +3.0 V. The mark indicator turns on when the input is less than -3.0 V. The monitor input impedance is the minimum RS-232C termination of 3 Kohms. It fully loads any transmitter connected to it and helps identify marginal interface drivers.

8-17. DYNAMIC INDICATORS

Flasher circuits for the dynamic indicators are located on the A2 Control Board, but are described here for clarity.

The six dynamic indicators respond to rapidly changing signals. Flasher circuits convert these signals to the 2 Hz signal visible on the interface activity monitor. Four of the dynamic indicators are hard wired to TD, RD, TC, and RC. The other two are connected to the spare input monitor. The positive edges of the buffered, level converted signals from the Interface Board continuously set D Flip Flops. Timer A2U501 generates a 2 Hz square wave which resets the flip flops. Both the interface signal and the flip flop outputs are fed to OR gates. When the reset waveform is low, the OR gate output is the inverted interface signal. When the reset waveform is high, the OR gate output is low.

8-18. DISPLAY DRIVERS

Timer A1U101 generates a 60 Hz square wave, the AC source required to drive the backplane of the interface activity display. The 60 Hz signal is fed to the inputs of exclusive NOR gates A1U200, A1U300, and A1U400 and the backplane of the LCD. The result is a +-5 V waveform across the LCD segment. When the remaining input to the exclusive NOR gate is low, the segment is off. When it is high or rapidly changing (> 10 Hz), the segment is on. The display responds as shown in Table 8-1.

Table 8-1. Display Segment Status

Interface Signal				Display
Static	MARK, Control OFF, SPACE, Control ON,	Negative Voltage, Positive Voltage,	or Binary 1 or Binary 0	Off On
Dynamic	Data or Clock			Flashes at 2 Hz rate

8-19. STATIC INDICATORS

Six static indicators respond to the status on the interface lines that carry control information.

DTR - Data Terminal Ready
DSR - Data Set Ready
RTS - Request to Send
CTS - Clear To Send
CD - Carrier Detect
RI - Ring Indicator

These six lines only show static conditions, so they bypass the flasher circuits and control the interface activity LCD directly through exclusive OR gates A1U200 and A1U300.

8-20. INTERFACE ACTIVITY LCD

CAUTION

Do not touch the LCD glass without protective gloves!
Do not squeeze the glass plates together!

8-21. ALPHANUMERIC DISPLAYS

Two liquid crystal display (LCD) modules, DS2 and DS3 display the test set up and results. The LCD's are self contained hybrid driver modules controlled directly by the microprocessor. They have no ESD protection and should only be handled in areas in which ESD precautions are employed.

CAUTION

There is no protective electrostatic discharge circuitry.
Handle only in static safe areas. For procedures, see paragraph 8-7.

8-22. KEYBOARD

Eight low profile key switches, S1-S8 form a 2 by 4 matrix read by microprocessor software. The switches set up and control the instrument.

8-23. A2 CONTROL BOARD THEORY OF OPERATION

8-24. INTRODUCTION

The Control Board configures the instrument to perform the various tests and compiles and displays the test results.

8-25. MICROPROCESSOR

The microprocessor has three general purpose eight bit wide ports, port 1, port 2, and bus. Bus is similar in function to the address/data bus in a conventional 8 bit microprocessor. Data and Address information is multiplexed into the bus port, when reading and writing to external data memory, it is also used to fetch instructions from external ROM.

Port 2 has two functions. The lower 4 bits act as the upper 4 address bits when the processor fetches an instruction from external ROM; therefore if an external ROM is used, the lower 4 bits of port 2 must be latched. The HP 4925B uses an 8K by 8 bit EPROM, since only 4K bytes of program memory can be accessed at a time, we bank select the two 4K blocks.

8-26. I/O Lines

The lower 7 bits of port 1 drive the LCD modules. All clocks, serial instructions, and serial data necessary to drive the displays are generated by the microprocessor software.

The lower four bits of port 2 perform two functions, they act as the upper 4 bits of the address bus and they contain valid port 2 data on the positive edge of ALE. The upper four bits select the area of memory to be accessed, reset the timer and UART, set the clock line, and read the buffered receive data.

There are three dedicated inputs, T0, T1, and INT. Their descriptions and input constraints are described in Table 8-2.

Table 8-2. Dedicated Input Line Configurations

Line	Description	Input
T0	a. Software testable flag b. Or configured as an output for the state counter. The state counter output is equal to the oscillator frequency divided by 4 (2 MHz with a 6 MHz clock).	OUT of LOCK, when not transmitting the FOX message
T1	a. Software testable flag b. Or input to the internal timer	Input selected by A2U704 which is controlled by the lower 3 bits of port 2
INT	a. Flag or interrupt to processor	Active low signal is set by the T1 counter output on the timer, it corresponds to the seconds counter

8-27. Bit Rate Generator

The bit rate generator consists of A2U503 bit rate generator and two, 8 to 1 multiplexers. The bit rate generator divides down the reference oscillator (1.8432 MHz) to fifteen simultaneous outputs. All standard data rates are produced by programming the bit rate generator and the multiplexers simultaneously.

The bit rate generator is programmed to always produce a x16 output. This clock is fed directly to the UART for the transmit and receive clock frequencies as well as to a four bit counter which derives the x1 and x2 clocks. The transmit clock source is selected from either the internal or external clock and is switched by a 2 to 1 multiplexer controlled by the microprocessor.

8-28. CLOCK GENERATOR

The clock generator is programmed by the microprocessor through the I/O expander, to select one of 16 possible clock frequencies. The x16 clock output is divided down to the x1 clock by A2U402 a divide-by-sixteen counter. Table 8-3 shows the I/O expander output required to program each bit rate.

Table 8-3. I/O Expander Outputs

BR - MODE	BR3	BR2	BR1	BR0	FREQUENCY
0	0	0	0	0	75 Hz
0	0	0	0	1	110 Hz
0	0	0	1	0	134.5 Hz
0	0	0	1	1	150 Hz
0	0	1	0	0	200 Hz
0	0	1	0	1	300 Hz
0	0	1	1	0	600 Hz
0	0	1	1	1	1200 Hz
0	1	0	0	0	1800 Hz
0	1	0	0	1	2400 Hz
0	1	0	1	0	3600 Hz
0	1	0	1	1	4800 Hz
0	1	1	0	0	7200 Hz
0	1	1	0	1	9600 Hz
1	1	0	1	0	14.4 kHz
1	1	0	1	1	19.2 kHz

8-29. I/O Expander

A2U304, the I/O expander provides additional I/O ports for the microprocessor as well as extra RAM and two programmable counters. The microprocessor programs the bit rate generator and reads the keyboard through the I/O expander.

Port A's lower five bits program the bit rate generator and the clock recovery circuit. The upper two bits are inputs and are used for sync latch reset, RTS, and transmitter output on/off.

Port B, the lower 6 bits drive and scan the keyboard.

The FOX control line sets up the instrument to transmit the FOX message. PC1 and PC2 output PRBS patterns A and B respectively. PC3 is the latched synch input. PC4 is the timer 1 (T1) input. PC5 is not used.

Counters T0 and T1 in the I/O expander generate outputs for each second used during error second counting. Timer T1 counts the number of received bits and generates a pulse every time one block is received. This pulse clocks the block counter which is read by the microprocessor. Other I/O ports serve as miscellaneous control lines and signal inputs.

8-30. External Data Latch

The microprocesser uses A2U203 the external data latch to write control signals to the Transmitter/Receiver Board and to the error event buffer. The external data latch controls:

1. the type of data to be transmitted or received,
2. the number of data bits per asynchronous framed character, and
3. resetting the error event buffer.

8-31. Error Event Buffer

The Error Event buffers spool occurrences of blocks, block errors, error seconds, drop outs. They also synchronize the receiver shift registers until the microprocessor has time to record this information. The microprocessor accesses the first three error events by reading 8 bit latch A2U303 via the data bus. It accesses the last two by reading A3U604 via the I/O lines. The error event buffers are defined as follows:

Blocks	A block is equal to 1000 received bits in the United States versions of the HP 4925B. In CCITT units, a block is equal to 511 bits if the 511 bit PRBS was selected and 2047 bits if the 2047 bit PRBS was selected.
Block Errors	A block error has occurred if a received block contains one or more bit errors.
Error Seconds	An error second has occurred if one or more bit errors have occurred in a one second period.
Drop Out	A drop out has occurred if more than 16 data element times have passed without a transition.
Synchronization	The receiver shift registers initially synchronize on receive data at the beginning of a test. The registers also resynchronize after a clock slip or a drop out.

8-32. Error Second Events

The bit error event line clocks D flip flop A3U502. Monostable multivibrator A3U602 outputs a 1 microsecond pulse each time the output of T0 (I/O Expander A3U305) indicates a second has passed, this pulse resets the error event latch (A3U502). Each error second that passes is counted by the error second counter A3U402. The microprocessor can read the state of the lower two bits via the error event latch A2U303; in this way up to 3 error seconds can occur before information is lost.

8-33. Clocks

Monostable multivibrator A2U602 outputs a 1 microsecond pulse each time a block length elapsed signal comes from I/O expander A2U305. The blocks are counted by block counter A2U302.

8-34. Block Error Events

The Bit error event line clocks D flip flop A2U502, which is reset when a block passes through monostable A2U602. Block error events are captured, and counted by 4 bit counter A2U302.

8-35. Drop Out Latch

D flip flop A2U604 latches when there is a drop out. It is reset by the Synch Latch Reset line.

8-36. Synch Latch

D flip flop A2U604 latches when the receiver shift registers synchronize. It is reset by the Synch Latch Reset line.

8-37. Error Event Latch

The error event latch is maped into location 3000 in external data memory. The inputs are determined by the output of the error second counter, the block counter, and the block error counter.

It is defined as follows:

D1	Q0 of block error counter
D2	Q1 of block error counter
D3	Q2 of block error counter
D4	Q0 of block counter
D5	Q1 of block counter
D6	Q2 of block counter
D7	Q0 of error seconds counter
D8	Q1 of error seconds counter

8-38. Microprocessor Input Mux (T1 Multiplexer)

Multiplexer A2U704 feeds the T1 input on the microprocesser which is programmed by P20, P21, and P22. Since data on the lower 4 bits of port 2 is valid only on the positive edge of ALE, we latch it with A2U605. The outputs of A2U605 in turn program the multiplexer to select the input that will be gated into T1.

bit errors	RTS monitor
transmitter shift register clock	low battery
receiver clock	start pulse
CTS	DCD

8-39. POWER SUPPLY

Both of the interfaces can be run by batteries. However it is recommended that the V.35 interface be used only with the AC power module.

8-40. HP 18183A, RS-232C/V.24

Power is supplied by the AC Power Module or by six 9V alkaline batteries. Ideally all 6 batteries are installed. There are four batteries connected in parallel forming the positive supply voltage. The other two batteries are also connected in parallel forming the negative supply. The unregulated supplies power the Interface Board output drivers. The positive supply drives a three terminal regulator which provides a 5 volt supply for most of the circuits.

8-41. HP 18184A, V.35

The 9V batteries can power the V.35 interface; however, it will nominally have power for only 15 minutes. HP recommends that you use the AC Power Module. Refer to Appendix E for more information on the AC Power Module.

8-42. A3 TRANSMITTER/RECEIVER THEORY OF OPERATION

The Transmitter/Receiver has two basic modes of operation.

1. Transmitting and receiving contiguous unframed pseudo random bit sequences (PRBS).

2. Transmitting and receiving asynchronous framed pseudo random bit sequences (PRBS).

When transmitting contiguous PRBS, the transmitter shift register generates a stream of PRBS. This is sent through the interface to the line under test. When transmitting asynchronous framed PRBS, the transmitter shift register generates only 5, 6, 7, or 8 bits of PRBS at a time. This byte of PRBS is then transferred to the UART which frames it with stop, start, and parity bits. The framed PRBS byte is sent through the interface to the line under test.

When receiving contiguous PRBS, the data stream comes from the line under test through the interface to the receiver shift registers. When receiving asynchronous framed PRBS, the data byte comes from the line under test, through the interface to the UART. The UART strips the framing bits from the received PRBS byte and sends it to the receiver shift registers through the asynchronous framing receiver buffer.

The transmitter can operate in a third mode and send the FOX message.

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 0123456789.

The characters of the FOX message are sent from memory by the microprocessor to the UART through A3U306. The UART adds framing bits and transmits each byte in the same manner as asynchronous framed PRBS.

Some Transmitter/Receiver circuits are only used for asynchronous framing. These are:

Character Idle Time Generator

Transmitter Data Bit Counter

Data Ready Shift Register

Receiver Data Bit Counter

Asynchronous Framing Receiver Buffer

The UART is used for asynchronous framing and the FOX mode. Clock recovery is used only for contiguous mode.

8-43. TRANSMITTER SHIFT REGISTER

The transmitter shift register is a closed loop, feedback shift register that generates Pseudo Random Bit Sequences (PRBS). Sequence data is right shifted through serial shift registers A3U306 and A3U405. Three pairs of parallel outputs are compared by A3U406, one pair for each (PRBS) generated. The PRBS requested by the operator is selected by data multiplexer A3U606 and fed back to the serial data input of A3U306. Serial sequence data is taken from the high order output of A3U405, the transmitter shift register. Parallel sequence data is taken from the parallel outputs of A3U306 and sent to the UART (Universal Asynchronous Receiver Transmitter).

The processor uses control lines PRBS select 0 and PRBS select 1 to select the pattern requested by the operator. PRBS pattern selections are given in Table 8-4.

Table 8-4. PRBS Pattern Selections

PRBS SELECT 1	0	Pattern Selected
0	0	2047 bit PRBS
0	1	511 bit PRBS
1	0	63 bit PRBS
1	1	+5V or mark

When transmitting the FOX pattern, characters are passed to the UART through A3U306. The FOX control line enables parallel data transmission.

8-44. TRANSMITTER ERROR GENERATOR

When enabled by the processor through control line Xmit Errors, A3U304, A3U603, A3U303, A3U406, and binary up counter A3U401 insert one error every 16 clocks in the transmit data.

8-45. RECEIVER SHIFT REGISTERS

The receiver shift register consists of a feed forward shift register and a feed back shift register. The feed forward shift register detects valid PRBS in the receive data. The feed back shift register detects actual bit errors.

8-46. Feed Forward Shift Register

Receive data is right shifted through serial shift registers A3U404 and A3U405. Three pairs of parallel outputs are compared by A3U605, one pair for each PRBS selected by data multiplexer A3U705. Data in the register predicts the next bit in the PRBS. The prediction and next bit are compared by A3U605. Feed forward errors are generated if the predicted bit and the bit actually received are different.

8-47. Feed Back Shift Register

The feed back shift register duplicates the function of the transmitter shift register. Received data is right shifted through the serial shift registers and compared by A3U706. Data multiplexer A3U705 selects the appropriate PRBS. Control lines PRBS select 1 and PRBS select 0 control the feed forward and feed back data multiplexers. Table 8-4 describes the line states for each pattern selection. The PRBS is compared with the receive data by A3U706. A bit error is generated each time the predicted bit and the actual bit are different.

8-48. ERROR DETECTION AND SYNCHRONIZATION CONTROL

Feed forward and feed back errors yield several results. Bit errors and data drop outs are detected, the feed back shift register is synchronized to incoming receive data and the out of lock condition is established.

8-49. Synchronization Controller

Binary up counter A3U302 accepts feed forward errors from feed forward error buffer A3U702 and feed back errors from the feedback error buffer A3U702. A3U302 resets each time a feed forward error is detected. When A3U302 is 1111 (binary), A3U202 goes to a 0 logic level. The synchronization controller requires several steps to synchronize the shift register. Receive data is shifted into the feed forward shift register. When the receive data is error free, the feed forward shift register stops generating feed forward errors. After the synchronization controller counts 16 more feed back errors, A3U202 sends a 0 logic level pulse for one clock period. A3U303 inverts this pulse which enables a parallel load of valid PRBS data from the feed forward shift register to the feed back shift register. This synchronizes the feed back shift register with the receive data and latches a D flip flop. This enables the processor to detect when initial synchronization, a clock slip, or resynchronization has occurred following a data drop out.

8-50. Drop Out Detector

A3U605 compares two successive parallel outputs of the feed forward shift register. It indicates data transition activity in the receive data. Binary up counter A3U302 increments one for each clock period that there is no transition activity. Sixteen clock periods without activity is considered a drop out and a logic 0 is clocked into A3U203. A logic 1 is clocked into A3U203 when data transitions occur. The synchronization controller remains in the reset state during a drop out to prevent synchronization of the feedback shift register from occuring. The FOX control line controls the set input of A3U203 which inhibits drop out detection when the FOX message is sent. If drop out detection were allowed to occur, received characters containing all 1 or all 0 data would cause an out of lock condition and falsely inhibit parity error events.

8-51. Data Ready Shift Register

A3U502, A3U303, and A3U403 synchronize the the UART data ready flag, synchronized data ready pulse enables shift register A3U104, which accepts parallel receive data from the UART. A3U104 shifts the data serially into the receiver shift registers. The synchronized data ready pulse also resets the UART data ready flag through control line Data Ready Reset.

8-52. Out of Lock Detector

Several components create the out of lock detector, A3U501, A3U301, A3U402, and binary up counter A3U401. The out of lock state occurs when the drop out detector detects a drop out in the receive data. Since synchronization occurs following a drop out, the out of lock detector remains in the out of lock state for 16 clock periods after the drop out and feed forward errors cease. The out of lock state also inhibits bit error event pulses through A3U501, the bit error detector.

8-53. Bit Error Detector

A bit error occurs when a feed forward error and a feed back error occur simultaneously. For example, following a clock slip, feed forward errors stop; however, feed back errors continue since the feed back shift register is out of synchronization with the receive data. These are feed back errors only, they are not considered bit errors and are therefore suppressed by A3U501. Only true bit errors pass through A3U501. The A2 Control Board produces an event pulse for each bit error detected. These pulses are fed to the microprocessor to increment the cumulative bit error counter. When jumper A3E3 is removed, feed forward errors are ignored; bit errors are then produced for each feed back error.

8-54. ASYNCHRONOUS FRAMING TRANSMIT CLOCK GENERATOR

When selected, the transmit clock generator advances the transmitter shift register a fixed number of states. For example, when transmitting asynchronously framed PRBS data, only 5, 6, 7, or 8 bits of the sequence are used for each character transmitted. The transmit clock generator also inserts 12 bits of idle time between each PRBS character. This prevents loss of framing in the receiver due to a bit error in a character start bit.

8-55. Character Idle Time Generator

The idle time generator produces idle time before loading a group of PRBS data bits into the UART. The wait period is 12.5 bit times. Binary up counter A3U602 begins counting the idle time after receiving a transmitter register empty pulse from the UART. This pulse is synchronized by A3U502, A3U402, and A3U403. When the idle time period is done, A3U502, A3U402, and A3U603 send a transmitter buffer register load pulse enabling the UART to load the next group of PRBS data bits. The pulse also starts the asynchronous framing data bits counter which allows the transmitter shift register to generate another group of PRBS data.

8-56. Asynchronous Framing Transmitter Data Bits Counter

Four control lines, Data Bits Select program the divide-by-N counter A3U503 to count the number of bits in the asynchronously framed PRBS character data field. For each count, a clock pulse is gated to the transmitter shift register to advance it the proper number of states.

8-57. Clock Selection

The processer controls analog multiplexer A3U305 through control line Rcvr Data Select A. A3U305 selects contiguous or gated clock to drive the transmitter shift register.

8-58. Asynchronous Framing Receive Clock Generator

When selected, the receive clock generator allows the receiver shift registers and the error detection and synchronization control to advance a fixed number of states to asynchronously receive framed PRBS.

Receive data is sampled by flip flop A3U601 which is clocked in by the x16 clock. Once a positive to negative transition of data is detected, A3U603 produces a pulse which lasts one x16 clock period. This pulse presets programmable 4 bit counter A3U703 to a count of 4 and will count down at a x16 clock rate. Recovered clock is the 8 input of A3U703 whose rising edge nominally indicates the center of a received bit. A3U703 continues to count, producing the recovered clock until again preset by the received data.

8-59. UART (Universal Asynchronous Receiver/Transmitter)

Asynchronous communication is accomplished via A3U205,the UART. The UART can be programmed for 1 or 2 stop bits, 5, 6, 7, or 8 data bits, and odd even, or no parity. This is accomplished by the processor writing a word, via the bus to the UART control register at location 6000(hex) in external data memory space.

Table 8-5. UART Control Register Definitions

bit 0	CLS1
bit 1	CLS2
bit 2	EPE (even parity enable)
bit 3	PI (parity enable)
bit 4	SBS (stop bit select)

8-60. Asynchronously Framed PRBS

When the Bit Error Rate Test Set is programmed for asynchronous framing, the transmitter and receiver shift registers pass data to and from the UART.

8-61. THE FOX MESSAGE

When the Bit Error Rate Test Set sends the FOX message, the microprocessor sends message characters to the UART for transmission via the Universal Bus Register A3U306. Control of the transmitter buffer register load line on the UART is switched from the transmitter clock controller to the microprocessor by multiplexer A2U204. A2U204 is controlled by the FOX control line. Character movement from the microprocessor to the UART occurs when the microprocessor writes to the universal bus register at location 5000(hex) in external data memory space. The character is strobed into the UART when the microprocessor performs a read operation from location 6000(hex).

8-62. TROUBLESHOOTING PROCEDURES

This troubleshooting guide is divided into three parts:

Part I:	Troubleshooting Without the Display
Part II:	Troubleshooting With Self Test
Part III:	Interface Troubleshooting

The Bit Error Rate Test performs a Self Test at power up when the power supply, kernel, and alphanumeric displays are functional. Failures during Self Test are indicated by codes displayed on the annunciators. If this happens, go to paragraph 8-59. Part II: Troubleshooting With Self Test where isolation and troubleshooting procedures are given. If the display blanks or displays random characters after power up, go to paragraph 8-63, Part I: Troubleshooting without the Display.

Before starting any troubleshooting procedures, check that the patch wires listed in Table 8-6 are placed for normal operation.

Table 8-6. Jumper Placement for Normal Operation

Board	Jumpers
A1	E1
A2	E1 (CCITT), E2, E3, E5, E6, E7
A3	E1, E2, E3, E4
A4	none

8-63. PART I: TROUBLESHOOTING WITHOUT THE DISPLAY

1. Turn the Bit Error Rate Test Set ON and verify that microprocessor A2U406 (pin 40) has +5 volts.
2. If there is no voltage on pin 40 of A2U406, troubleshoot voltage regulator A2U405, the batteries, and the interconnecting cables.
3. If +5 V is present, use the Signature Analysis LCD/Kernel routine to verify the operation of A2U406 the microprocessor, A2U306 the address latch, and A2U106 the EPROM.
4. Check the signatures on data bus DB0-DB7.
   a. If any signatures are incorrect troubleshoot the Kernel.
   b. If all data bus signatures are correct go to step 5.

5. Turn OFF the Bit Error Rate Test Set and disconnect the A1 Display Board.

CAUTION

The alphanumeric displays have no electrostatic protection. Insert W1 the Display Board connector into conductive foam to protect the displays when it is disconnected from the rest of the instrument.

6. Short A2U506 pin 3 to A2TP108. Power up the Bit Error Rate Test Set.

7. Check the signatures on the display control bus, A2U406 pins 27-33 using the LCD/Kernel Routine.

   a. If all signature are correct go to step 8.

   b. If any signatures are incorrect replace A2U406.

8. Turn the Bit Error Rate Test Set OFF and reconnnect the Display Board. Use the Signature Analysis LCD/Kernel routine and verify that the correct signatures and voltages appear on each pin of DS2 and DS3 as shown in Table 8-7.

Table 8-7. DS2 and DS3 Voltage and Signatures

DS2 and DS3 Pin Number	Signal Name	Voltage or Signature
1	V3	3.2V +-10%
2	V2	2.2V +-10%
3	V1	1.1V +-10%
4	N/C	
5	INA	2A01
6	NONE	H5H
7	02	F64C
8	01	00F4
9	PWOB (DS2)	PC75
	PWOA (DS3)	518F
10	SYN	2588
11	ISA	F454
12	NONE	CH5H
13	INA	2A01
14	V REG	+5 V
15	GND	0 V
16	OSCC	
17	N/C	

9. One possible display failure mode is when one display input shorts to ground. The displays are in parallel, with the exception of pins 9 and 16. Thus both displays will appear to fail, even is only one is bad.

10. If an incorrect signature or voltage is found, power down and unsolder one of the display leads to that line. Power up and check the signature again. If it is correct, replace the display attached to the unsoldered lead. If the signature is still wrong, repeat the procedure with the other display. If unsoldering a lead on the second display corrects the signature, replace that display. If the signature is still wrong, trace that signal path back to the A2 Board.

8-64. REPLACING ALPHANUMERIC DISPLAYS DS2 OR DS3.

When replacing the alphanumeric displays, review and closely follow the static handling procedures given in paragraph 8-7, the displays are extremely suspectable to damage by electrostatic discharge.

CAUTION

Wear eye protection when replacing the alphanumeric displays. The leads have a tendency to splatter molten solder.

1. When removing and replacing an alphanumeric display, cover the back of the other display with conductive foam to prevent any solder splatter from entering the display and causing intermittant failures.

2. Heat each lead of the display and lift it clear of the pad using small jewelers screwdriver.

3. When all leads are disconnected, unscrew the display carrier and remove the display.

4. Add a small amount of RMA solder to each of the display pads.

5. Install the new display into the display carrier.

CAUTION

Do not touch display faces. Fingerprints will destroy the polarizer.

6. Use a jewelers screwdriver to hold each lead down while soldering it into place. Be careful not to overheat the display lead as it may separate from the display.

7. Clean any loose solder between the display pads with the screwdriver. Be careful to avoid dropping any loose solder onto the back of the display.

8-65. PART II: TROUBLESHOOTING WITH SELF TEST

Table 8-8 lists the tests performed by Self Test and the resultant error codes.

If a failure occurs in the Bit Error Rate Test Set, one or more error codes may be displayed. If test 2, 3, or 4 fail, testing stops and an error message is displayed. If any of tests 5 through 14 fail, Self Test is complete and error codes are displayed.

Determine which test failed by looking up the error code in Table 8-8. Refer to the troubleshooting procedure following this section for the correct test and troubleshooting procedure. If more than one error code is displayed, troubleshoot the error codes starting with the top display, left to right, then the bottom display, left to right.

When Self Test fails, the HP 4925B "locks up". To obtain normal keyboard operation, press BEGIN/END, then quickly press BERT. The top level menu should appear.

Table 8-8. Self Test Error Codes

TEST NUMBER	TEST NAME	ERROR CODE
8-66	Power Up Test	CHECK POWER
8-67	Microprocessor Ram	RAM FAILURE
8-68	Transmit Clock	NO XMTR CLK
8-69	Receiver Clock	NO RCVR CLK
8-70	Transmit Clock Specification	0 (top display)
8-71	Transmitter	1 (top display)
8-72	FFSR/Synch	2 (top display)
8-73	FBSR	3 (top display)
8-74	Dropout	4 (top display)
8-75	Out of lock	0 (bottom display)
8-76	Error Count	1 (bottom display)
8-77	Error Event	2 (bottom display)
8-78	Asynchronous Loopback	3 (bottom display)
8-79	UART	none
8-80	FOX	4 (bottom display)

The following Troubleshooting procedures are based on the Self Test test results. Each test description includes set up conditions, cause of failure and, troubleshooting procedure.

8-66. ROWER UP TEST

Test Failure Code

CHECK POWER

Description

Low battery is monitored through T1 of the microprocessor.

Internal Setup

None Applicable

Test Fails If

Low battery line is HIGH.

Troubleshooting Procedure

Replace the batteries, if applicable.

If the test continues to fail, troubleshoot the battery check circuit. The low battery line should only go high if the positive and negative battery voltages drop below +- 5.6 V. This procedure also applies to instruments using the HP 18185A AC Power Module

8-67. MICROPROCESSOR RAM TEST

Test Failure Code

RAM FAILURE

Test Description

The microprocessor verifies its internal RAM.

Internal Set Up

None applicable

Test Fails If

Any bit of microprocessor RAM is defective.

Troubleshooting Procedure

Replace A2U406, the microprocessor.

8-68. TRANSMIT CLOCK TEST

Test Failure Code

NO XMIT CLK

Test Description

The transmitter clock is monitored through T1 of the microprocessor.

Internal Set Up

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	PRBS 63

Fails Test If

The transmitter clock is not working.

Troubleshooting Procedure

If this test fails, the HP 4925B locks up in the XMIT CLK test condition to permit troubleshooting. Check the XMIT CLK signal path from the clock generator to T1 pin 39 of the microprocessor.

8-69. RECEIVER CLOCK TEST

Test Failure Code

NO RCVR CLK

Test Description

The receiver clock is monitored through T1 of the microprocessor.

Internal Test Setup

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	63 PRBS

Test Fails If

The receiver clock is not working.

Troubleshooting Procedure

If this test fails, the HP 4925B locks up in the receiver clock test condition to permit troubleshooting.

Check the RCVR clock path from the recovered clock to T1 pin 39 of the microprocessor.

8-70. TRANSMIT CLOCK SPECIFICATION TEST

Test Failure Code

0 (top display)

Test Description

The transmitter clock frequency is monitored through T1 of the microprocessor.

Internal Set Up

Clock	1200 Hz
Run time	Contiguous Loopback
Pattern	63 PRBS

Test Fails If

There is a frequency error greater than +- 2 Hz.

Troubleshooting Procedure

1. The output of the clock generator should be greather than +- 2 Hz. Verify that the clock generator is programmed for 1200 Hz, refer to Table 8-3.

2. Check the microprocessor clock frequency. It should be 6 MHz +- 1 kHz.

NOTE

If using a 5005A Signature Multimeter to check the frequency, change the threshold to 5 V.

8-71. TRANSMITTER TEST

Test Failure Code

1 (top display)

Test Description

The Transmitter Test checks that each PRBS pattern is correctly generated by the transmitter. The microprocessor reads an 8 bit segment of each PRBS pattern through port 2 bit 7 (pin 38).

Internal Set Up

Clock	1200 Hz
Routine	Contiguous LB
Pattern	+5 V
	PRBS 63
	PRBS 511
	PRBS 2047

Test Fails If

The incorrect pattern is read by the microprocessor.

Troubleshooting Procedure

1. Press BEGIN/END, then BERT to obtain the top level menu.
2. Check that A3U606 is programmed correctly for each PRBS pattern. Refer to Table 8-9.

Table 8-9. A3U606 Pattern Programing

PATTERN	pin 2	pin 14
2047	0	0
511	0	1
63	1	0
FOX	0	0

3. If A3U606 is correctly programmed, connect a data probe or Scope to A3U405 pin 2. Check that data activity occurs at A3U405 pin 2 for each pattern selected except FOX. If correct go to step 5.

4. If data activity does not occur for patterns 63, 511, or 2047, troubleshoot the Transmitter Shift Register.

   a. Check that the control lines of A3U306 are as follows:

pin 9	low
pin 15	clock
pin 13	low

5. Since the feedback path is in the Transmitter Shift Register, Signature Analysis is not effective for troubleshooting. Use the following procedure.

   a. Remove A3E4.

   b. Momentarily ground A3U306 pin 10. This sends a pulse of lows through the Transmitter Shift Register.

   c. Check all nodes in the Transmitter Shift Register using this technique.

   d. If all nodes have the correct logic transitions, replace A3U606.

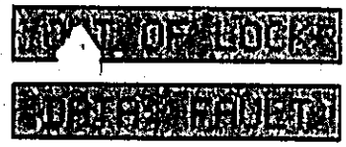
6. Set the HP 4925B to Loopback mode, see Section III for set up procedures. Check that data activity occurs at A2U406 pin 38, for each pattern except FOX.

7. If data activity does not occur for patterns 63, 511, and 2047 troubleshoot the Rcv Data Signal path back to the Receiver Mux and the Contiguous Loopback path, back to the Transmitter Shift Register.

8. If data activity does occur for patterns 63, 511, and 2047 determine if the correct pattern is being transmitted for each PRBS with the following test.

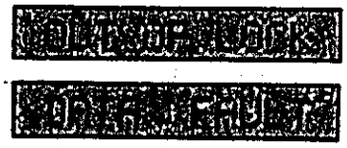
   a. Start a Bit Error Rate Test using Loopback set up for each of the PRBS patterns 63, 511, and 2047.

   b. If



   is displayed for any pattern, then the Transmitter Shift Register is transmitting the wrong pattern or the Error Generator is ON. Check A2U406 pin 12. It should be low. If not, troubleshoot the Error Generator. If A2U406 is low, troubleshoot the Transmitter Shift Register using the technique in step 5.

   If



   is not displayed for any of the PRBS patterns and the FOX test failed, replace A2U406.

8-72. FFSR/SYNCH TEST

Test Failure Code

2 (top display)

Test Description

Latched synch is monitored by the microprocessor through the I/O Expander. Latched synch is reset after each PRBS pattern is sent or received.

Internal Set Up

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	63 PRBS
	+5 V
	511
	2047

Fails Test If

Synchronization does not occur during each PRBS pattern.

Troubleshooting Procedure

Use the Contiguous Signature Analysis routine to troubleshoot the Synchronization Controller, the Feed Forward Shift Register, and the Synchronization Latch.

8-73. FBSR TEST

Test Failure Code

3 (top display)

Test Description

Latched synchronization is monitored by the microprocessor through the I/O Expander. Latched synchronization is reset after each PRBS pattern is sent or received.

Internal Set Up

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	63 PRBS
	+5 V
	511
	2047

Fails Test If

Synchronization occurs more than once during each PRBS pattern.

Troubleshooting Procedure

Use the Contiguous Signature Analysis routine, loop B to troubleshoot the receiver Feed Back Shift Register. If good signatures are found in the Feed Back Shif. Register, replace A3U705. The Signature Analysis routine only uses 63 PRBS and +5 V patterns and will not detect a fault in the other two channels of A3U705.

8-74. DROP OUT TEST

Test Failure Code

4 (top display)

Test Description

Drop out is monitored by the microprocessor through the I/O expander.

Internal Set Up

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	63 PRBS
	+5 V

Test Fails If

Drop out does not go high during the +5 V pattern or low during the 63 PRBS pattern.

Troubleshooting Procedure

Use Contiguous Signature Analysis routine to troubleshoot the drop out detector, and the drop out signal path to the I/O expander.

8-75. OUT OF LOCK TEST

Test Failure Code

0 (bottom display)

Test Description

Out of lock is monitored through TO of the microprocessor.

Internal Set Up

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	63 PRBS and +5 V

Test Fails If

Out of Lock does not go high during the +5 V pattern or does not go low during the 63 PRBS pattern.

Troubleshooting Procedure

Use the Contiguous Signature Analysis routine to troubleshoot the out of lock detector and the out of lock signal path to TO (pin 1) of the microprocessor.

8-76. ERROR COUNT TEST

Test Failure Code

1 (bottom display)

Test Description

When the Bit Error Generator is turned on, 128 data bits are transmitted. Bit errors are monitored through T2 of the microprocessor.

Internal Set Up:

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	63 PRBS

Fails Test If

Eight (8) errors are not counted.

Troubleshooting Procedures

Use the Contiguous Signature Analysis routine to check the error generator, the bit error detector, and the bit error signal path to pin 1 of A2U704, the microprocessor input mux.

8-77. ERROR EVENT TEST

Test Failure Code

2 (bottom display)

Test Description

The microprocessor reads the Error Event Latch after it is reset and again after a time delay.

Internal Set Up

Clock	1200 Hz
Routine	Contiguous Loopback
Pattern	63 PRBS
	+5 V

Test Fails If

The Error Event Latch is not set to 00H after reset or is not set to FFH after the time delay.

Troubleshooting Procedure

Use the Contiguous Signature Analysis routine to troubleshoot the error event buffer.

8-78. ASYNCHRONOUS LOOPBACK TEST

Test Failure Code

3 (bottom display)

Test Description

The latched synch signal is monitored through the I/O expander and the transmitter clock is monitored through T1 of the microprocessor.

Internal Set Up

Clock	4.8 kHz
Routine	Asynchronous framed data, loopback
Pattern	63 PRBS
Data Bits	6, 7, and 8

Test Fails If

Synchronization does not occur while transmitting 63 PRBS with 6, 7, and 8 data bits. Also if the microprocessor senses that the wrong number of data bits transmitted.

Troubleshooting Procedure

Use the Framed Data Signature Analysis routine to troubleshoot the circuitry unique to asynchronous framing.

Character Idle Time Generator

Transmitter Data Bit Counter

Data Ready Shift Register

Receiver Data Bit Counter

Asynchronous Framing Receiver Buffer

It is possible for the Framed Data Signature Analysis routine not to detect some failures that are detected by the Self Tests. This is because the Framed Data Signature Analysis routine uses a 600 Hz clock and 7 data bits while Self Test uses a 4.8 kHz clock and tests 6, 7, and 8 data bits. If the asynchronous test fails, but the Signature Analysis routine does not show any incorrect signatures, check that the HP 4925B will operate correctly at 4.8 kHz and 5, 6, 7, and 8 data bits. This can be done by initiating a Bit Error Test in Loopback mode using 4.8 kHz DATA RATE and 5, 6, 7, and 8 DATA BITS. If the HP 4925B displays OUT OF LOCK and DATA FAULT, or bit errors occur for all data bits, check the 4.8 kHz clock. If the test works for some data bits and not for others, check that the receiver and transmitter data bit counters are being programmed correctly. Table 8-10 describes the correct programming.

Table 8-10. Data Bit Select

DATA BITS	DBS-3	DBS-2	DBS-1	DBS-0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

8-79. UART TEST

Test Failure Code

3 or 4 (Bottom Display)

Test Description

Check that the UART, A3U205 is operating correctly. This test is not apart of the Self Test Routine.

Internal Set Up

Clock	4.8 kHz
Routine	Asynchronous framed data, loopback
Pattern	63 PRBS
Data Bits	6, 7, and 8

Test Fails If

The correct signals are not present.

Troubleshooting Procedure

1. The input signals given in Table 8-11 must be present for the UART to work.
2. Refer to Table 8-22 to verify that the UART is operating correctly.

Table 8-11. UART (A3U205) Signal Verification

Pin Number	Line	Status
17 and 40	x 16 clk	toggling
21	MR	low
23	TBRL	toggling
34	CL2	low
35-39	DB0-DB4	toggling

8-80. FOX TEST

Test Failure Code

4 (bottom display)

Test Description

The microprocessor sends an 8 bit word to the UART through the Transmitter Shift Register. The UART transmits and receives the 8 bit word then loads it into the receiver Feed Forward Shift Register. The processor reads the word through port 2 bit 7 (pin 38). See paragraph 8-79 to verify UART operation.

Internal Set Up

Clock	600 Hz
Routine	Asynch Framing Loopback
Pattern	semi-Fox
Data Bits	8

Fails Test If

The incorrect word is received by the microprocessor.

Troubleshooting Procedure

Initiate the FOX test using 8 data bits and verify that the FOX control line is high. Verify that A3U306 pin 9 has a 1.3 us pulse with a 100 Hz repetition rate.

If the FOX control line is high and A3U306 pin 9 is pulsing, verify that data is being loaded through A3U306. If data activity is not occuring on XMIT 0 through XMIT 7, replace A3U306.

Refer to paragraph 8-79 to verify UART operation.

8-81. PART III: SIGNATURE ANALYSIS

8-82. INTRODUCTION

There are four Signature Analysis routines:

LCD/Kernel
I/O Test
Contiguous
Framed Data

For some routines different set ups are required to check the components. Before each Signature Analysis routine, the correct set up is described.

8-83. LCD/KERNEL SIGNATURE ANALYSIS ROUTINE

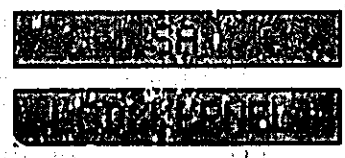
The LCD/Kernel Signature Analysis routine provides signatures to check the microprocessor, address latch, EPROM, and alphanumeric displays.

NOTE

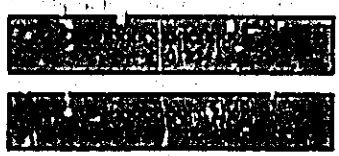
Be careful when checking Data Bus signatures. If two bus lines are momentarily shorted, the LCD/Kernel routine will halt. If this occurs, the display will stop flashing.

To access the LCD/Kernel Signature Analysis routine, perform the following steps in order.

1. Remove jumper A2E5.
2. Remove jumper A2E7 and set it on A2E8.
3. Power up the Bit Error Rate Test Set.
4. Remove jumper A2E8.
5. The display should read



6. The display will change and flash at a 4 Hz rate.



8-84. SIGNATURE ANALYSIS TABLES

Table 8-12. LCD/Kernel Signature Analysis for Set Up A

LOOP: LCD/KERNAL SET UP: A PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP108	A2 Control Board
CLOCK	+	TP107	A2 Control Board

Vh = CH5H

U406 21 = 8A99
22 = 8C02
23 = 8702
24 = U804
27 = 00F4
28 = 2A01
29 = F454
30 = 2588
31 = F64C
32 = 518F
33 = PC75
35 = 0000
36 = 37F4
37 = 019C

Table 8-13. LCD/Kernel Signature Analysis for Set Up B

LOOP: LCD/KERNAL SET UP: B PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	+	TP107	A2 Control Board

Vh = CH5H

U605
1 = low
2 = low
3 = 26CU
4 = 2672
5 = 2072
6 = 1UU1
8 = low
9 = low
10 = low
11 = U804
12 = 8702
13 = 8CO2
14 = 8A99
15 = low
16 = high

Table 8-14. LCD/Kernal Signature Analysis for Set Up C

LOOP: LCD/KERNAL SET UP: C PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	+	U406-10	A2 Control Board

Vh = 00UP

U406 12 = 0081
13 = 0040
14 = 0020
15 = 0010
16 = 0008
17 = 0004
18 = 0002
19 = 0001
20 = low

Table 8-15. LCD/Kernel Signature Analysis for Set Up D

LOOP: LCD/KERNAL SET UP: D PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	+	U406-10	A2 Control Board

Vh = 00UP

U504
1 = 00UH
2 = 0003
3 = 0000
4 = 00U7
5 = 0000
6 = 0009
7 = low
8 = 0005
9 = 0000
10 = 00UC
11 = 00UH
12 = 00UH
13 = 0003
14 = high

U505
1 = 0008
2 = 0001
3 = 0009
4 = 0005
5 = 0001
6 = 0004
7 = low
8 = 0002
9 = 0001
10 = 0003
11 = high
12 = 0009
13 = high
14 = high

U406
1 = high
3 = 00UP
4 = high
7 = high
8 = high
10 = 0000
11 = 0000
13 = 0040
14 = 0020
17 = 0004
18 = 0002
20 = low

Table 8-16. LCD/Kernel Signature Analysis for Set Up E

LOOP: LCD/KERNAL SET UP: E PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	-	U406-10	A2 Control Board

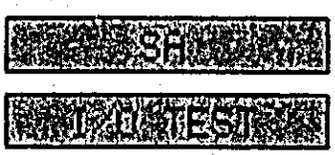
Vh = 00UP

U306 2 = 0081
5 = 0040
6 = 0020
9 = 0010
12 = 0008
15 = 0004
16 = 0002
19 = 0001

8-85. I/O TEST SIGNATURE ANALYSIS ROUTINE

To access the I/O Signature Analysis Test routine, perform the following steps in order.

1. Turn off the Bit Error Rate Test Set.
2. Check that jumper A2E5 is installed.
3. Short A2E7.
4. Short A2E8.
5. Power up the Bit Error Rate Test Set.
6. Remove the short from A2E8.
7. The display should read



8. Remove A2E7.

Table 8-17. I/C Signature Analysis Test for Set Up A

LOOP: I/O TEST SET UP: A PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	+	U406-10	A2 Control Board

Vh = UP73

U203		U304	
1	= low	1	= low
2	= 0U19	2	= low
3	= U194	4	= low
4	= 0U19	5	= low
5	= 00U1	6	= high
6	= 000U	7	= high
7	= 00U1	8	= 000U
8	= 000U	9	= UP73
9	= U194	10	= 0000
10	= low	11	= 0000
11	= PU49	12	= U194
12	= 0U19	13	= 0U19
13	= U194	14	= 00U1
14	= 0U19	15	= 000U
15	= 00U1	16	= U194
16	= 000U	17	= 0U19
17	= 00U1	18	= 00U1
18	= 000U	19	= 000U
19	= U194	20	= low
20	= high		

Table 8-18. I/O Signature Analysis Test for Set Up B

LOOP: I/O TEST SET UP: B PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	-	U406 pin 10	A2 Control Board

Vh = UP73

U304 21 = U980
22 = 078F
23 = 0078
24 = 0007
25 = U980
26 = 078F
27 = 0078
28 = 0007
29 = high
30 = high
31 = high
32 = high
33 = 1P32
34 = P05P
35 = low
36 = low
37 = 3F65
38 = 03F6
39 = 003F
40 = high

Table 8-19. I/O Signature Analysis Test for Key Scan Set Up

LOOP: I/O TEST SET UP: KEY SCAN PCA: A2 Control Board

SIGNATURE		QUALIFIER MODE	
START/STOP	-/+	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	-	U406-10	A2 Control Board

Vh = UP73

A2U304	DEPRESS KEY	SIGNATURE
29	NONE	high
29	DATA RATE	1P32
30	NONE	high
30	PATTERN	1P32
31	NONE	high
31	DATA BITS	1P32
31	START UP	P05P
32	NONE	high
32	PARITY	IP32
32	BEGIN/END	P05P
33	NONE	1P32
34	NONE	P05P

8-86. CONTIGUOUS SIGNATURE ANALYSIS TEST ROUTINE

To access the Contiguous Signature Analysis Test routine, perform the following steps in order.

1. Turn off the Bit Error Rate Test Set.
2. Short A2E7.
3. Short A2E8.
4. Power up the Bit Error Rate Test Set.
5. Remove the short from A2E8.
6. The display should read

7. Remove A2E7.
8. Press TEST DURATION.

Table 8-20. Contiguous Signature Analysis for Set Up A

LOOP: CONTIGUOUS SET UP: A PCA: A3 XMTR/RCVR Board

SIGNATURE		QUALIFIER MODE	
START/STOP	+/-	TP707	A2 Control Board
QUALIFIER	-	U104-7	A2 Control Board
CLOCK	+	TP105	A2 Control Board
GROUND		U104-7	A2 Control Board

Vh = CP75

A2U302	1 = 1742	A3U202	1 = 90F1
	2 = high		2 = FP9A
	3 = 34H5		3 = H103
	4 = U655		4 = 7495
	5 = 8624		5 = CP24
	7 = 0000		9 = 4695
	9 = 0000		10 = 63H2
	10 = high		11 = 2555
	11 = 2397		12 = CC32
	12 = 77H9		13 = F89U
	13 = 4P18		
	15 = 0000		
A2U402	9 = 1742	A3U203	1 = 0500
	10 = high		2 = CC75
	11 = 34H5		3 = 0000
	15 = 0000		4 = low
			5 = F89U
A2U405	1 = CP75	A3U204	1 = low
	2 = 709H		2 = low
			3 = low
A2U502	1 = 1742		4 = high
	3 = 0000		5 = low
	4 = 0000		6 = 069P
	5 = high		7 = 069P
	6 = low		14 = low
	8 = low		
	9 = high		
	11 = 0000		
	13 = 1742		

Table 8-20. Contiguous Signature Analysis for Set Up A (cont)

A3U301
1 = 6UHH
2 = F89U
3 = 937F
4 = 6P05
5 = HC70
6 = 90F1
8 = 31A8
9 = H1A8
10 = CP75
11 = CC75
12 = CP75
13 = 0500

A3U302
1 = CP75
2 = 6P05
3 = FP9A
4 = H103
5 = 7495
6 = CP24
7 = 937F
9 = CP75
10 = F89U
11 = 4695
12 = 63H2
13 = 2555
14 = CC32
15 = 6726

A3U303
1 = P274
2 = 5F01
10 = 2PC4
11 = 90F1
12 = 0000
13 = CP75

A3U304
1 = 06P9
3 = CP75
4 = low
5 = 06P9
6 = low
8 = low
9 = C469
10 = low
11 = 0000
12 = P441

A3U305
9 = low
10 = low
11 = low
12 = CP75
14 = CP75

A3U306
1 = U7A2
2 = 2HHA
3 = 992C
4 = U0F9
5 = 230F
6 = 8487
7 = FC90
8 = 55CP
9 = low
10 = 69P2
11 = high
12 = low
13 = low
14 = low
15 = 0000

A3U401
1 = CP75
2 = 31A8
3 = 834C
4 = 5612
5 = 8CF8
6 = 8FFP
9 = 0000
10 = high
14 = C469
15 = 6309

A3U402
8 = 8UHH
9 = 31A8

Table 8-20. Contiguous Signature Analysis for Set Up A (cont)

A3U404	1	= CP75	A3U501	1	= 709H
	2	= C6FH		2	= H1A8
	3	= A966		3	= 6P05
	4	= 9052		4	= 8UHH
	5	= P23C		5	= high
	6	= low		9	= 834C
	7	= 069P		10	= 5612
	9	= CP75		11	= 8CF8
	10	= 35UF		12	= 8FFP
	11	= AU04		13	= 31A8
	12	= 9F97			
	13	= UCC1	A3U601	1	= high
	14	= low		5	= C89F
				6	= 06P9
A3U405	1	= 0000		7	= C89F
	2	= 5AP8		9	= CP75
	3	= 0P8A		10	= 06P9
	4	= 1H14		11	= C89F
	5	= 3A29		12	= 06P9
	6	= low		13	= CP75
	7	= C6FH		14	= 0000
	9	= CP75		15	= CP75
	11	= 774U			
	13	= 9A9P	A2U602	4	= 0000
	15	= U7A2		6	= 0000
				10	= 0000
				11	= 0000
A3U406	1	= 774U			
	2	= 9A9P			
	3	= PHH1	U603	1	= 06P9
	4	= 6A57		2	= C89F
	5	= 9A9P		3	= CP75
	6	= U0F9		8	= C469
	8	= U0F9		9	= P441
	9	= 992C		10	= P274
	10	= 69P2			
	11	= 06P9			
	12	= 5F[illegible]1			
	13	= 5AP8			

Table 8-20. Contiguous Signature Analysis for Set Up A (cont)

A3U605	1	= 0P8A
	2	= 3A29
	3	= 34A3
	4	= F198
	5	= 3A29
	6	= UCC1
	8	= UCC1
	9	= 9F97
	10	= 6726
	11	= 61FU
	12	= 06P9
	13	= 6726
A3U606	1	= low
	2	= high
	3	= high
	4	= 69P2
	5	= 6A57
	6	= PHH1
	7	= 69P2
	14	= 0000
A3U702	1	= HIA8
	2	= 6UHH
	3	= CP75
	4	= low
	5	= 61FU
	6	= low
	8	= low
	9	= HF0C
	10	= low
	11	= CP75
	12	= H070
	13	= 6P05

8-87. CONTIGUOUS LOOP B SIGNATURE ANALYSIS ROUTINE

To access the Contiguous Loop B Signature Analysis Test routine, leave the HP 4925B in the Contiguous Loop set up. There are two changes given under Set Up Instructions below.

Table 8-21. Contiguous Signature Analysis for Set Up B

LOOP: CONTIGUOUS SET UP: B PCA: A3 XMTR/RCVR Board

SET UP INSTRUCTIONS: Remove A3E2.
Connect A3U304 pin 5 to A3U604 pin 10.

SIGNATURE		QUALIFIER	MODE
START/STOP	+/-	TP707	A2 Control Board
QUALIFIER	-	U104 pin 7	A2 Control Board
CLOCK	+	TP105	A2 Control Board
GROUND		U104 pin 7	A2 Control Board

Vh = CP75

U604		U704	
1	= 7A6F	1	= F26F
2	= HH09	2	= AH09
3	= 788F	3	= 73F2
4	= 3386	4	= FP54
5	= 4PHF	5	= 9FA8
6	= 5U26	6	= H21P
7	= 979F	7	= 4U73
8	= 06P9	8	= 5F79
9	= high	9	= high
10	= 06P9	10	= 7A6F
11	= high	11	= high
12	= low	12	= low
13	= PC4U	13	= PC4U
14	= low	14	= low
15	= CP75	15	= CP75
16	= 06P9	16	= C6FH
17	= P23C	17	= 3A29
18	= 9052	18	= 1H14
19	= A966	19	= low
20	= 35UF	20	= low
21	= UCC1	21	= low
22	= 9F97	22	= low
23	= AU04	23	= low
24	= high	24	= high

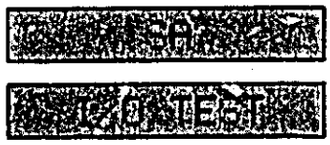
Table 8-22. Contiguous Signature Analysis for Set Up B (cont)

U705	1	low
	2	high
	3	low
	4	6726
	5	F198
	6	34A3
	7	6726
	8	low
	9	4C0A
	10	8P67
	11	6UUU
	12	4C0A
	13	high
	14	0000
	15	low
	16	high
U706	1	H21P
	2	5F79
	3	8P67
	4	6UUU
	5	5F79
	6	3386
	7	low
	8	3386
	9	788F
	10	4C0A
	11	4HP3
	12	06P9
	13	4C0A
	14	high

8-88. FRAMED DATA SIGNATURE ANALYSIS TEST ROUTINE

To access the Framed Data Signature Analysis Test routine, perform the following steps in order.

1. Turn off the Bit Error Rate Test Set.
2. Connect A2TP105 to A2U704 pin 6.
3. Short A2E7.
4. Short A2E8.
5. Power up the Bit Error Rate Test Set.
6. Remove A2E8.
7. The display should read



8. Remove A2E7.
9. Press BERT.

Table 8-23. Framed Data Signature Analysis

LOOP: FRAMED DATA — PCA: A3 XMTR/RCVR Board

SIGNATURE

		QUALIFIER MODE	
START/STOP	+/-	TP707	A2 Control Board
QUALIFIER	-	TP109	A2 Control Board
CLOCK	-	U402 pin 1	A2 Control Board
GROUND		U402 pin 8	A2 Control Board

Vh = 2721

U103
1 = 2F63
2 = high
3 = F8P3
4 = 393F
5 = low
6 = 3164
7 = 36A8
9 = UU57
10 = low
11 = low
12 = 393F
13 = high
14 = low
15 = 4C19

U104
1 = 6P98
2 = 5217
3 = 8P42
4 = 6P98
5 = 49C9
6 = 6P98
7 = 49C9
9 = F8P3
10 = P5F2
11 = low
12 = 788C
13 = 49C9
14 = 6P98
15 = 49C9

U203
1 = high
2 = low
3 = F2P3
4 = low
5 = high
6 = high
8 = low
9 = 393F
10 = low
11 = 1645
12 = C9PU
13 = 9PFD

Table 8-23. Framed Data Signature Analysis (cont)

U205	1 = high	U402	1 = 3164
	3 = low		2 = 1645
	4 = low		3 = P943
	5 = 49C9		4 = FP62
	6 = 6P98		5 = 2FA9
	7 = 49C9		6 = 0C88
	8 = 6P98		8 = low
	9 = 49C9		9 = high
	10 = 6P98		10 = P48F
	11 = 49C9		11 = F3AH
	12 = 6P98		12 = 297C
	13 = low		13 = 0P5A
	14 = low		
	15 = low		
	16 = low		
	17 = 2721		
	18 = PUF2		
	19 = 8P95		
	20 = 6CF8		
	21 = low		
	22 = A1A6		
	23 = 2721		
	24 = 496H		
	25 = 6CF8		
	26 = 23HC		
	27 = 04UA		
	28 = 23HC		
	29 = 04UA		
	30 = 23HC		
	31 = 04UA		
	32 = 23HC		
	33 = 04UA		
	34 = low		

Table 8-23. Framed Data Signature Analysis (cont)

U403	1 = 9HP9	U601	1 = high
	2 = F8P3		5 = P000
	3 = F8P3		6 = 6390
	4 = P5F2		7 = 44C1
	5 = C9PU		9 = 2721
	6 = 3164		10 = F721
	8 = FP62		11 = P000
	9 = 45UH		12 = 8P42
	10 = 3HHC		13 = 72U1
	11 = C519		14 = 2AP8
	12 = 3164		15 = 0HF9
	13 = P48F		
U502	1 = high	U603	1 = 6390
	2 = F8P3		2 = P000
	3 = 8P95		3 = 72U1
	4 = F8P3		4 = 1U28
	5 = CAF8		5 = 0C88
	6 = 496H		6 = 297C
	7 = 45UH		8 = low
	9 = 1645		9 = high
	10 = P943		10 = high
	11 = 45UH		11 = 0P5A
	12 = 2FA9		12 = 39C4
	13 = 297C		13 = 360C
	14 = 6UPP		
	15 = F3AH		
U503	1 = 5C89	U703	1 = 77FC
	2 = high		2 = low
	3 = 3809		3 = 2AP8
	4 = 6UPP		4 = low
	5 = low		5 = low
	6 = 3164		6 = 2721
	7 = 4109		7 = 10H6
	9 = 050F		9 = H3H4
	10 = low		10 = low
	11 = low		11 = low
	12 = 6UPP		12 = 0603
	13 = high		13 = high
	14 = low		14 = high
	15 = H5A0		15 = 3164

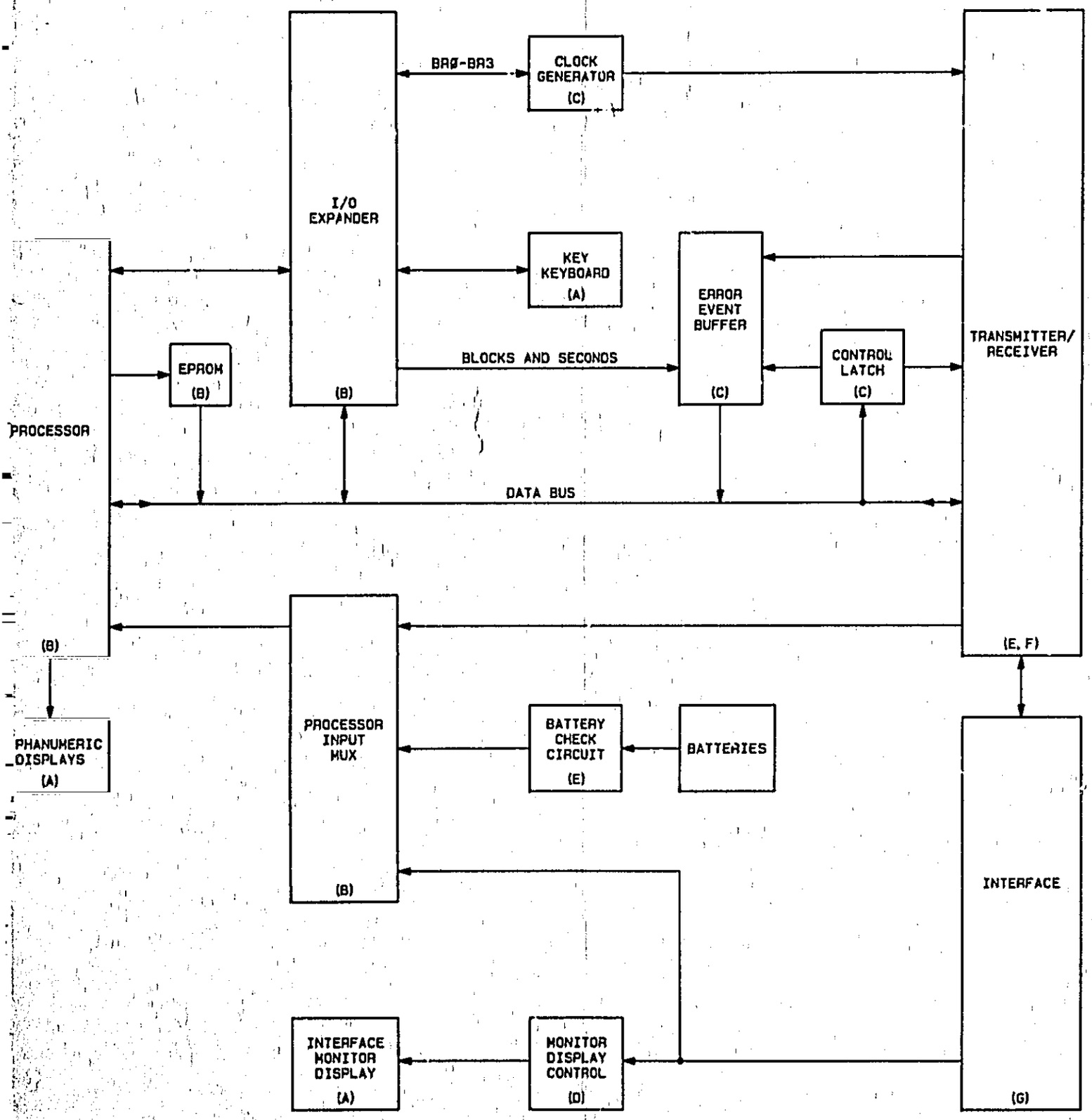


Figure 8-6.
Control and Displays Circuit Block Diagram

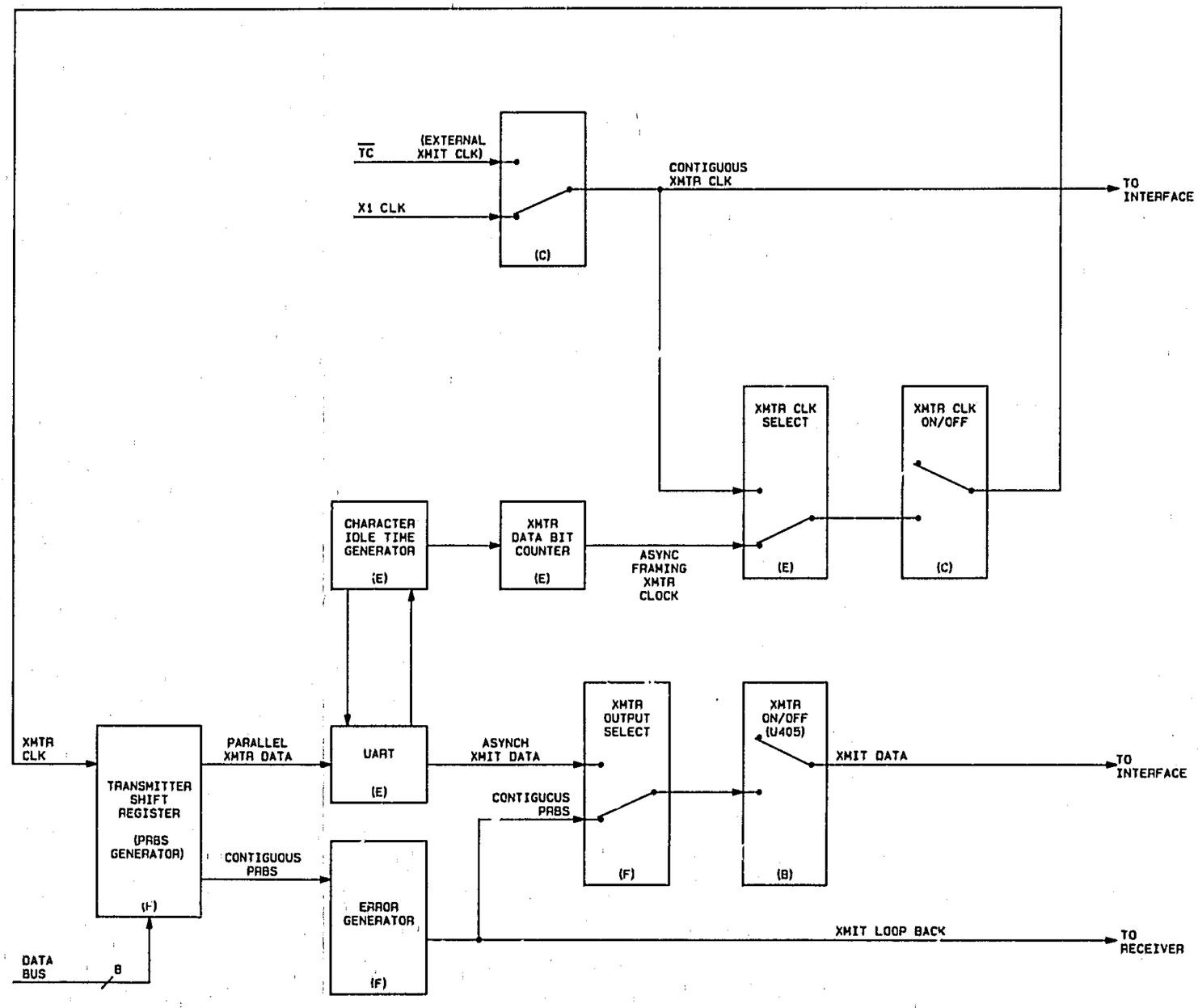


Figure 8-7. Transmitter Block Diagram

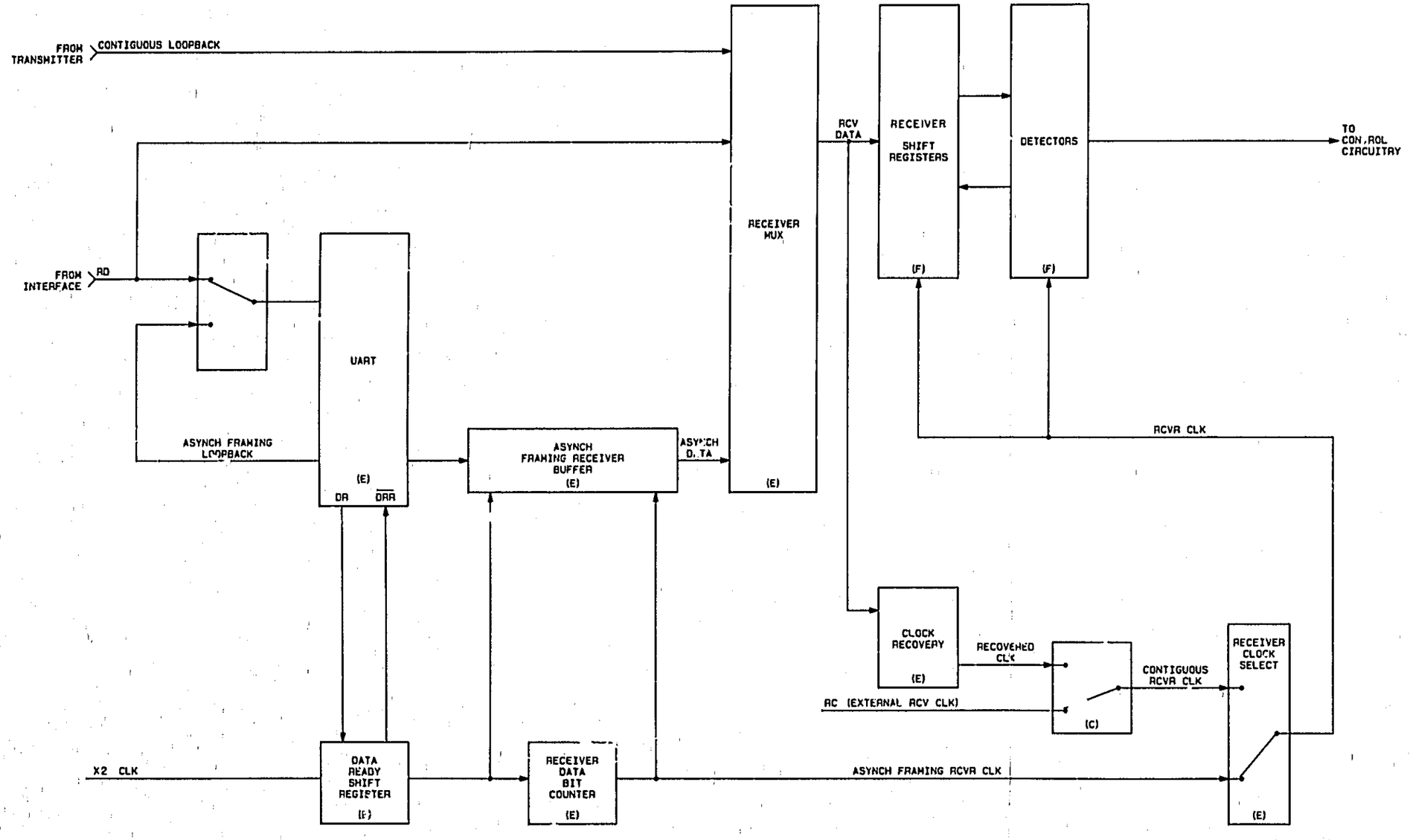


Figure 8-8.
Receiver Block Diagram

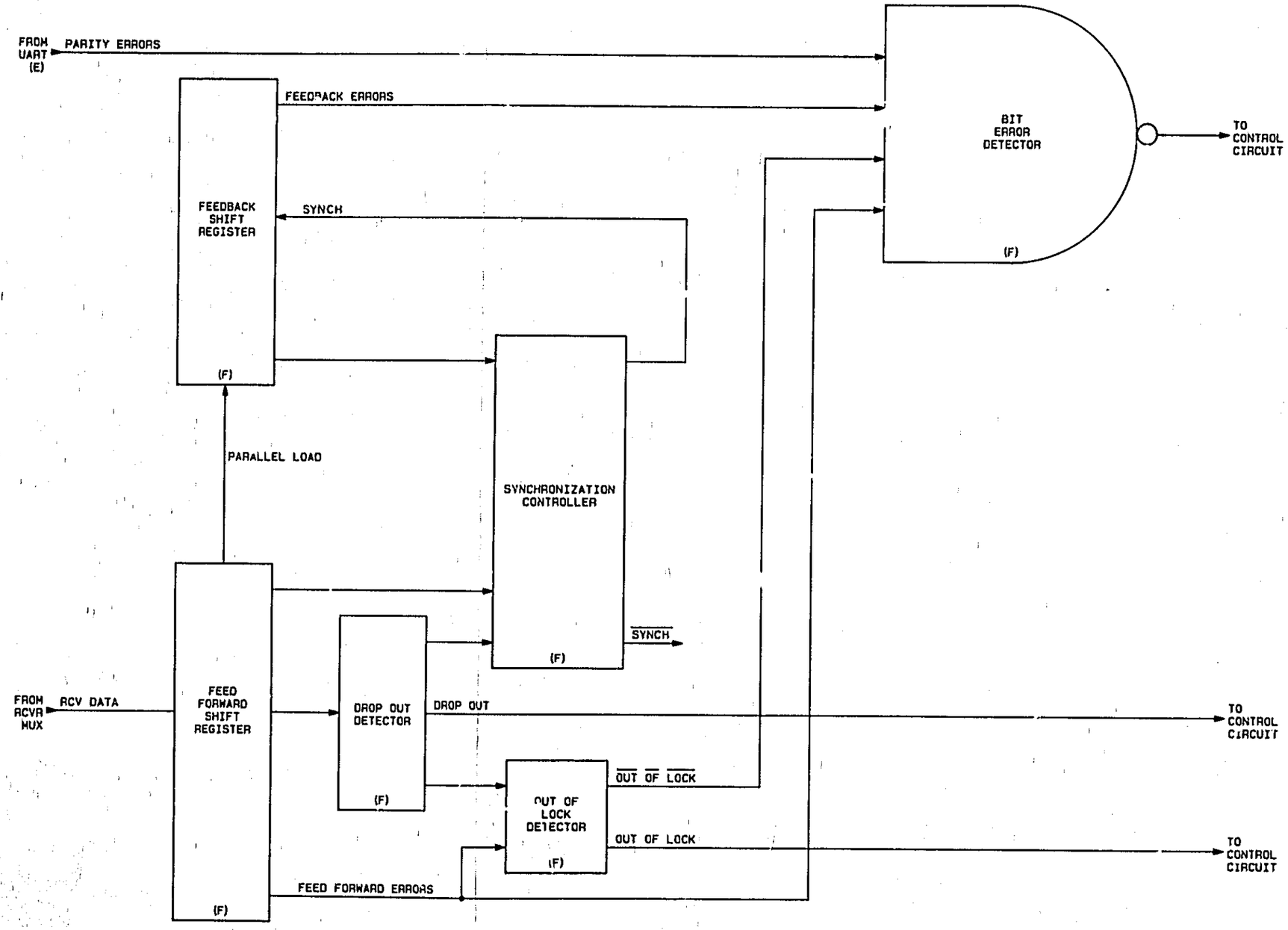
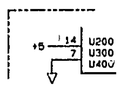


Figure 8-9. Receiver Shift Registers/Detectors Block Diagram

Power and Grounds



DISPLAY BOARD

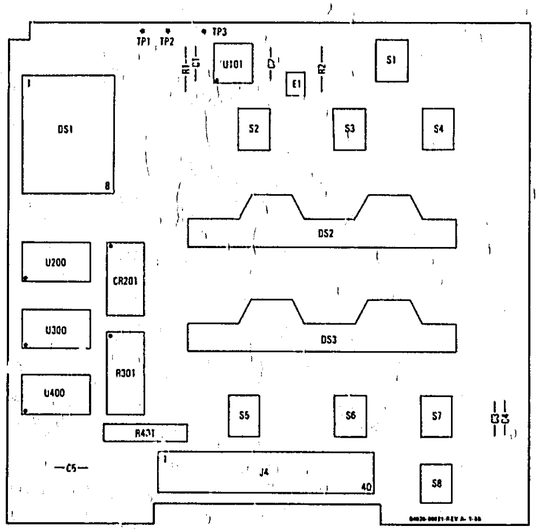


Figure 8-10. A1 Display Board Component Locator

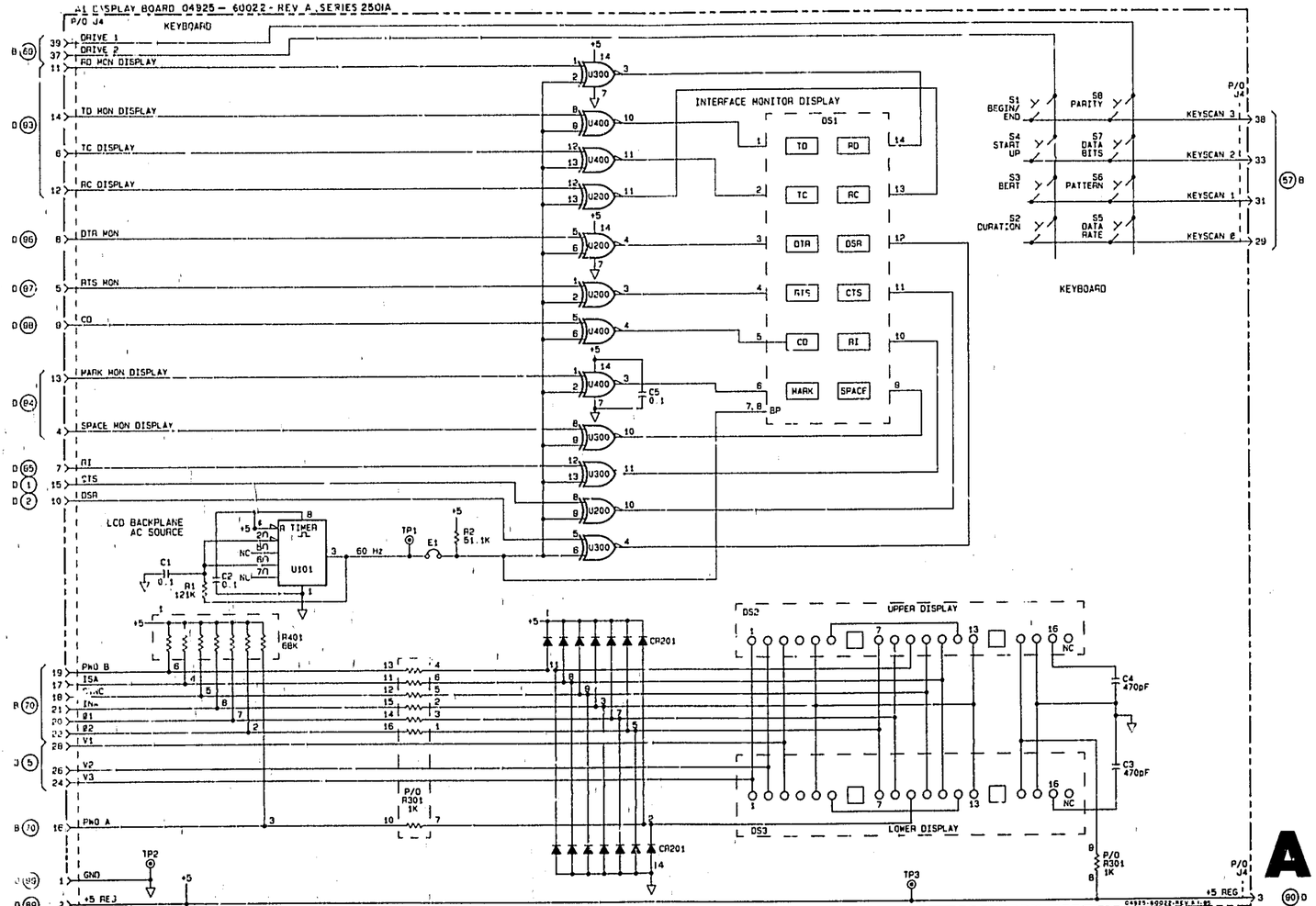


Figure 8-11.
A1 Display Board Schematic Diagram
8-67

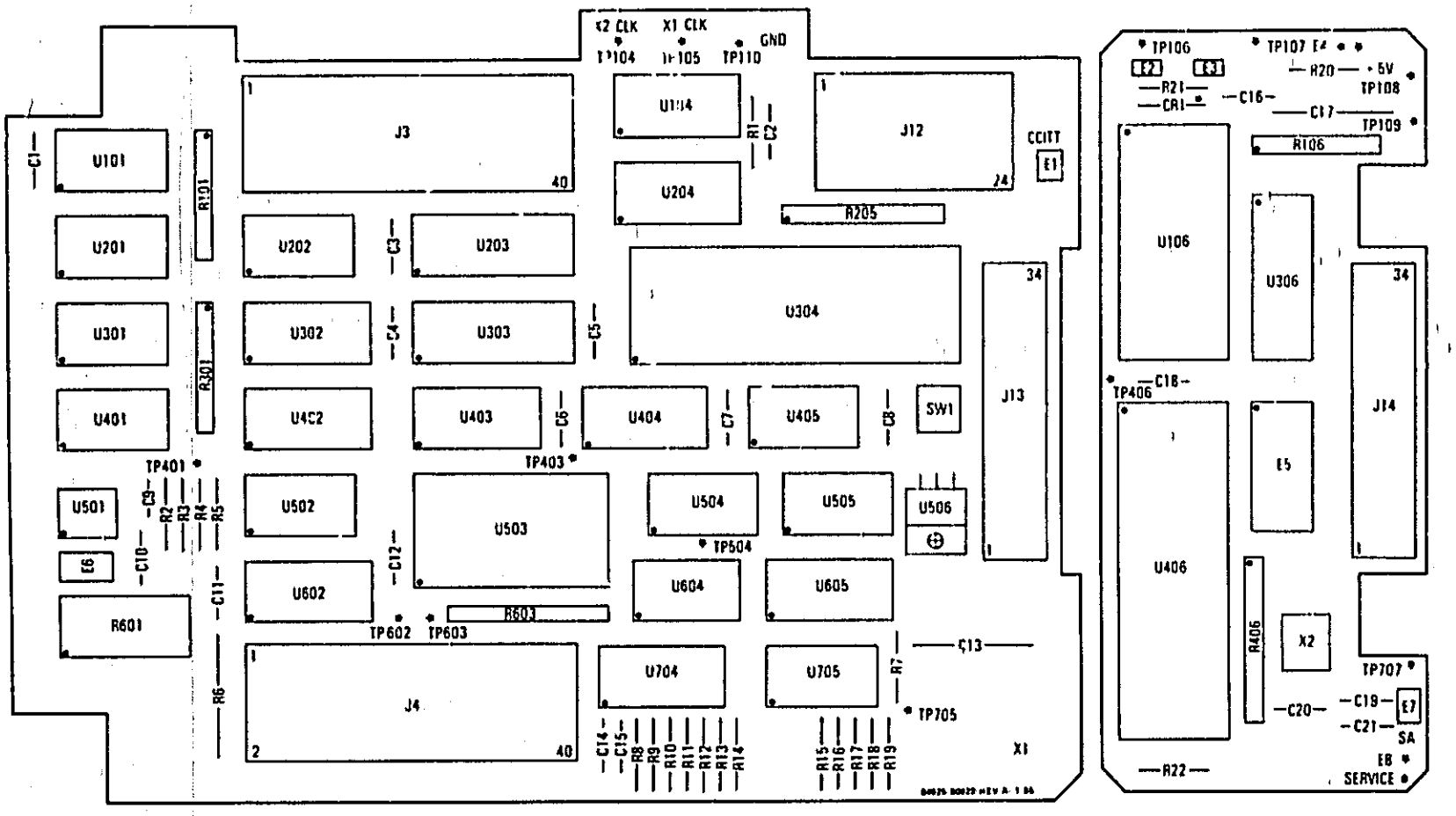
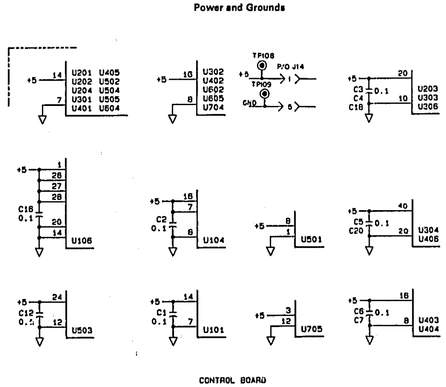


Figure 8-12. A2 Control Board Component Locator



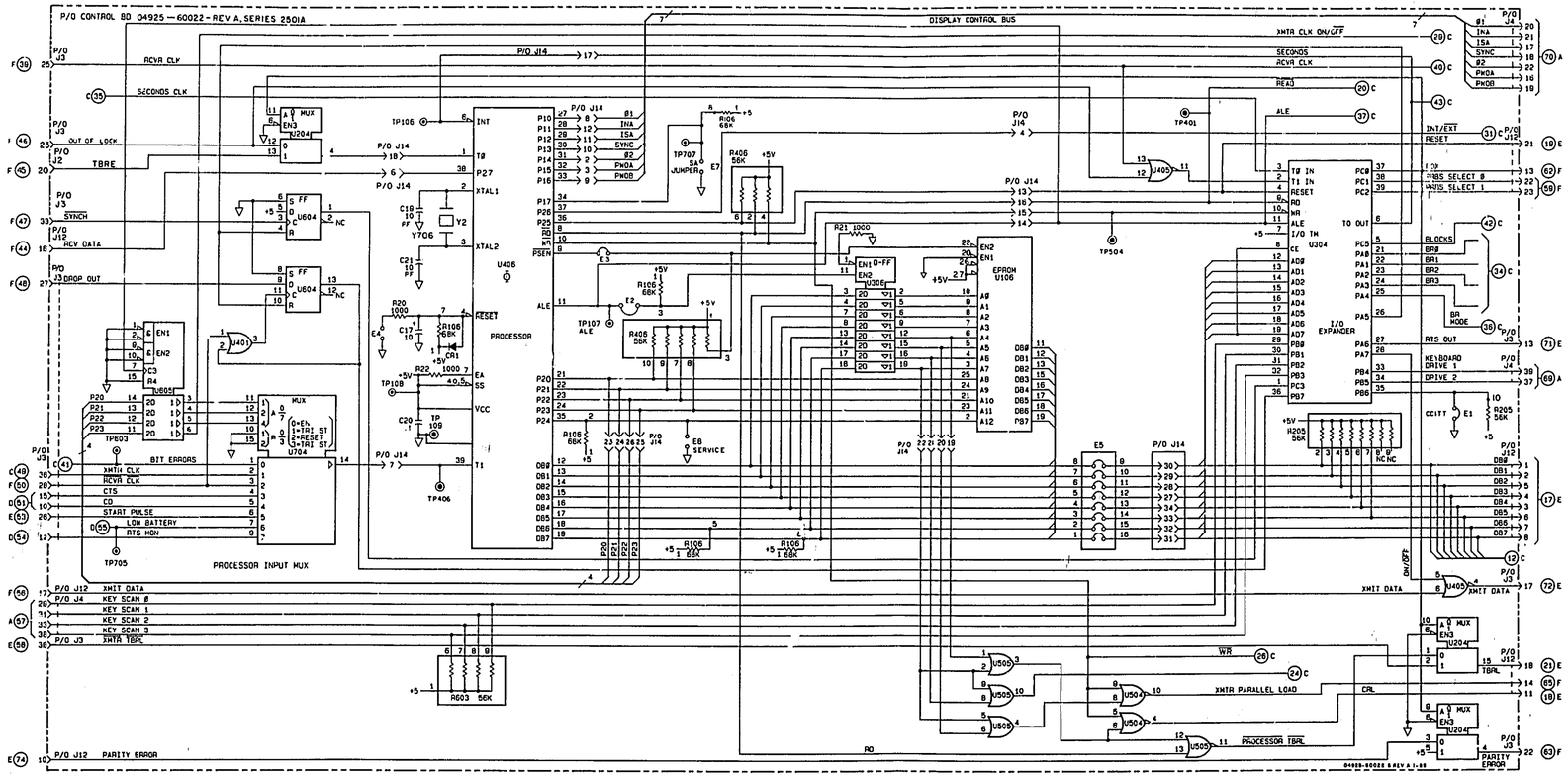
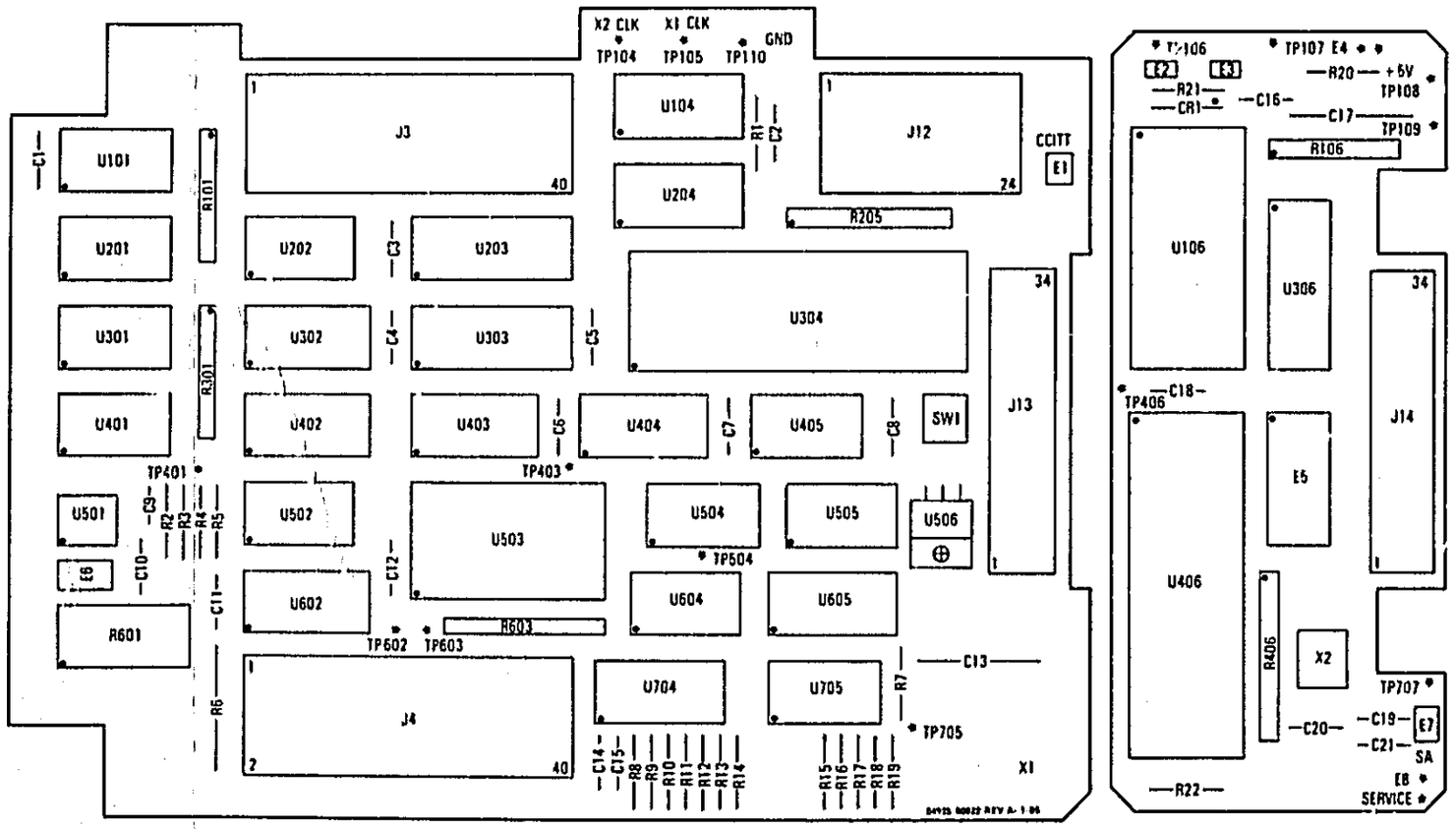


Figure 8-13.
A2 Control Board
Schematic Diagram (sheet 1 of 3)



A2 Control Board Component Locator

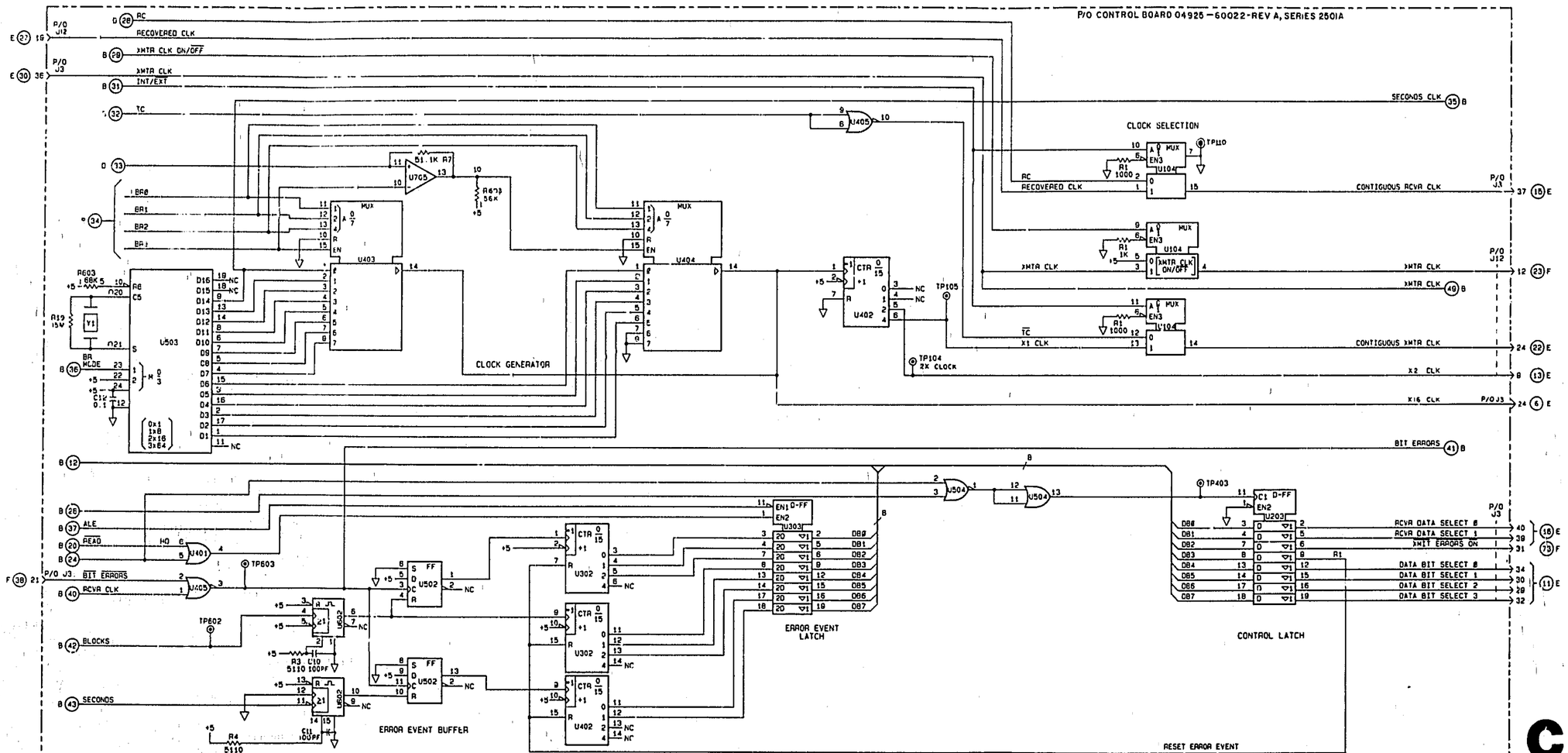
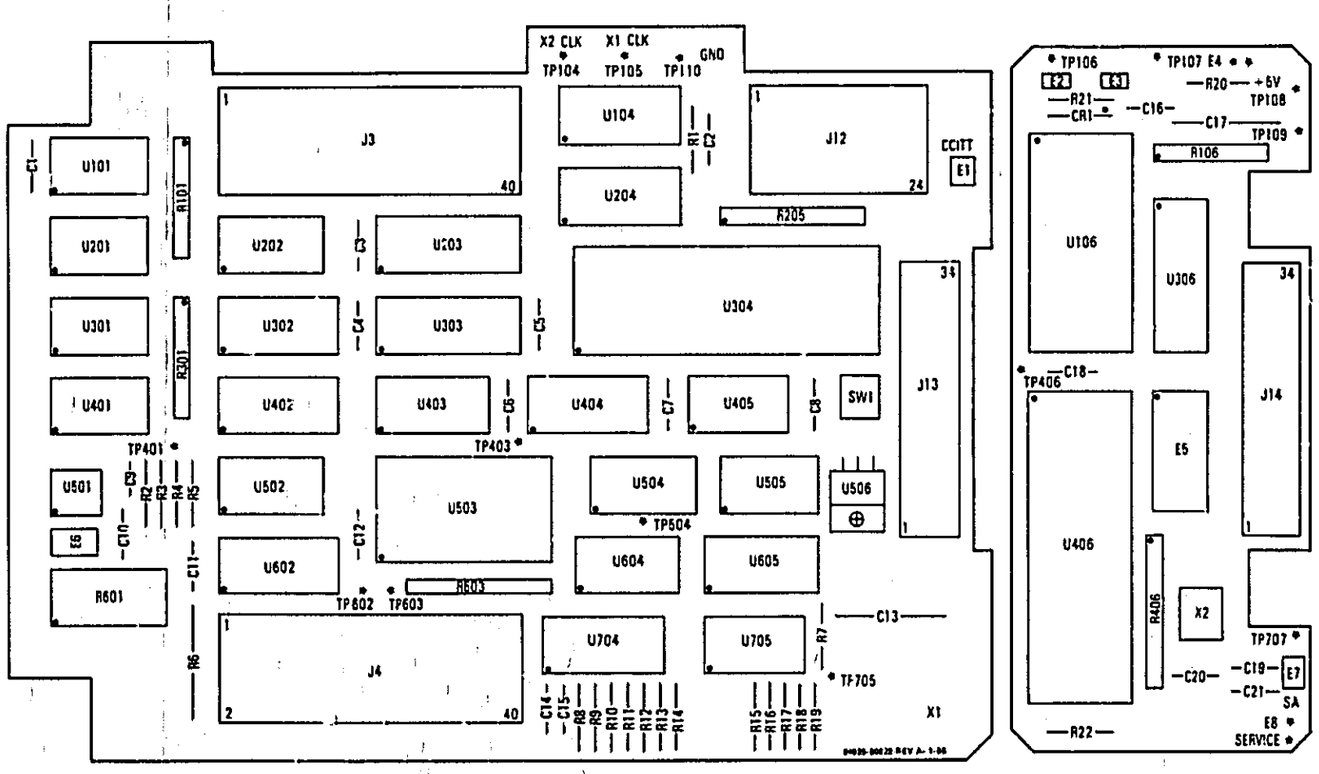


Figure 8-14.
A2 Control Board
Schematic Diagram (sheet 2 of 3)
8-71



A2 Control Board Component Locator

P/O A2 CONTROL BD 04925-60022 - REV A, SERIES 2301A

FLASHER CIRCUITS

FLASH RATE GENERATOR

BATTERY CHECK

DISPLAY VOLTAGE REFERENCE

D

Figure 8-15.
A2 Control Board
Schematic Diagram (sheet 3 of 3)

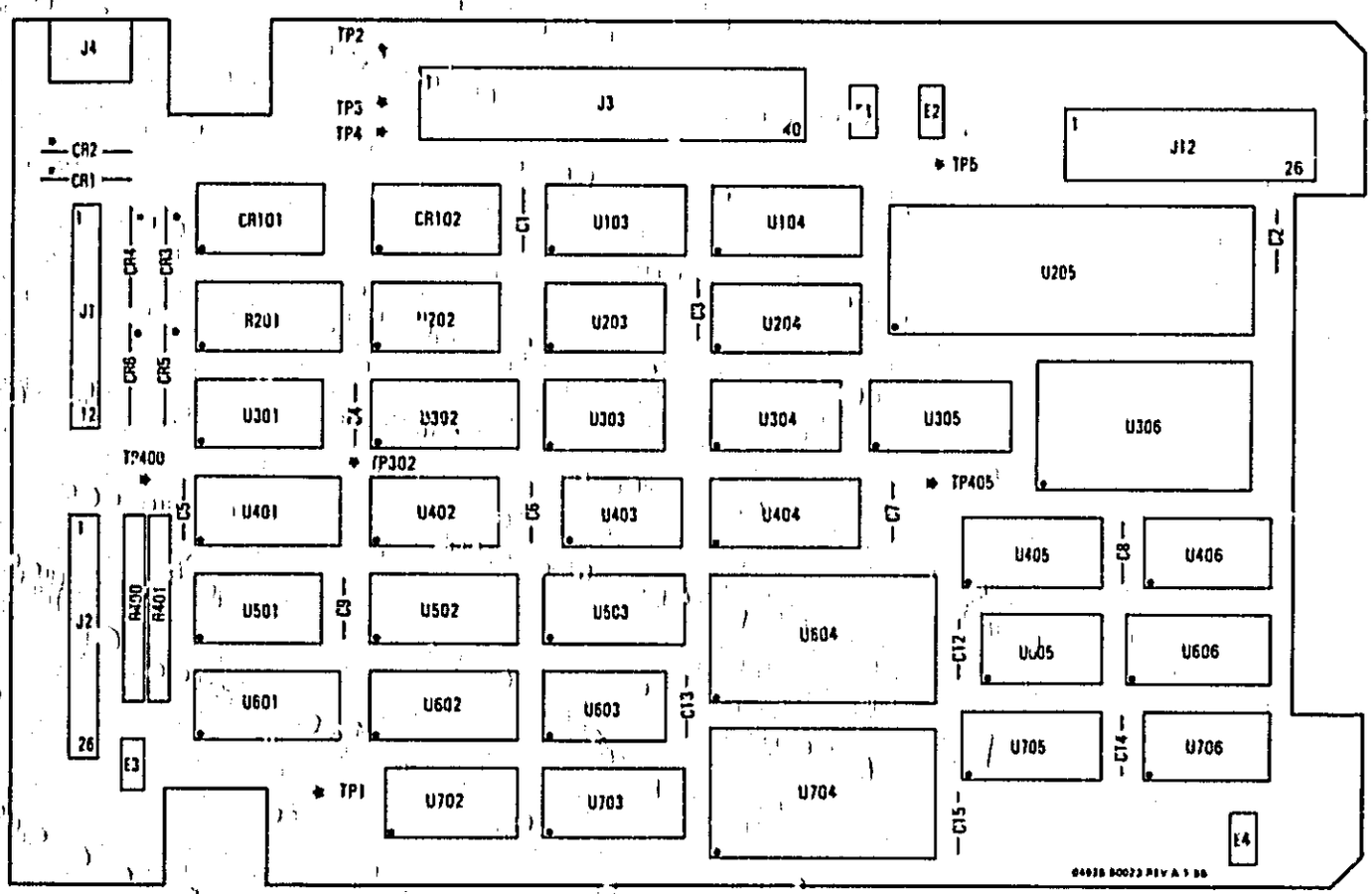
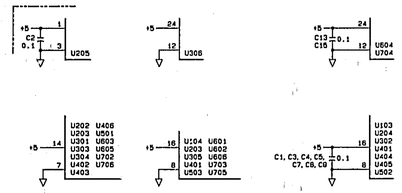


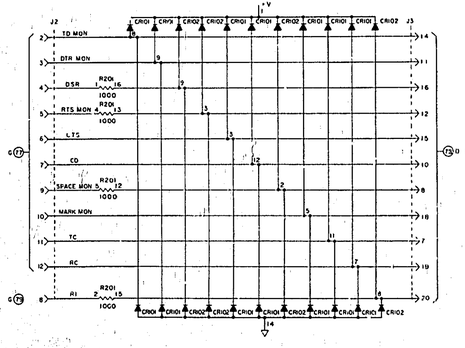
Figure 8-16. A3 Transmitter/Receiver Board Component Locator

Power and Grounds

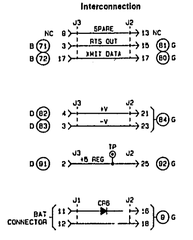


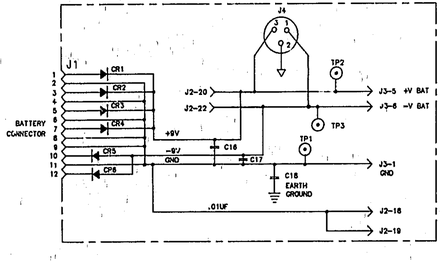
TRANSMITTER/RECEIVER BOARD

Interconnnection



Interconnection





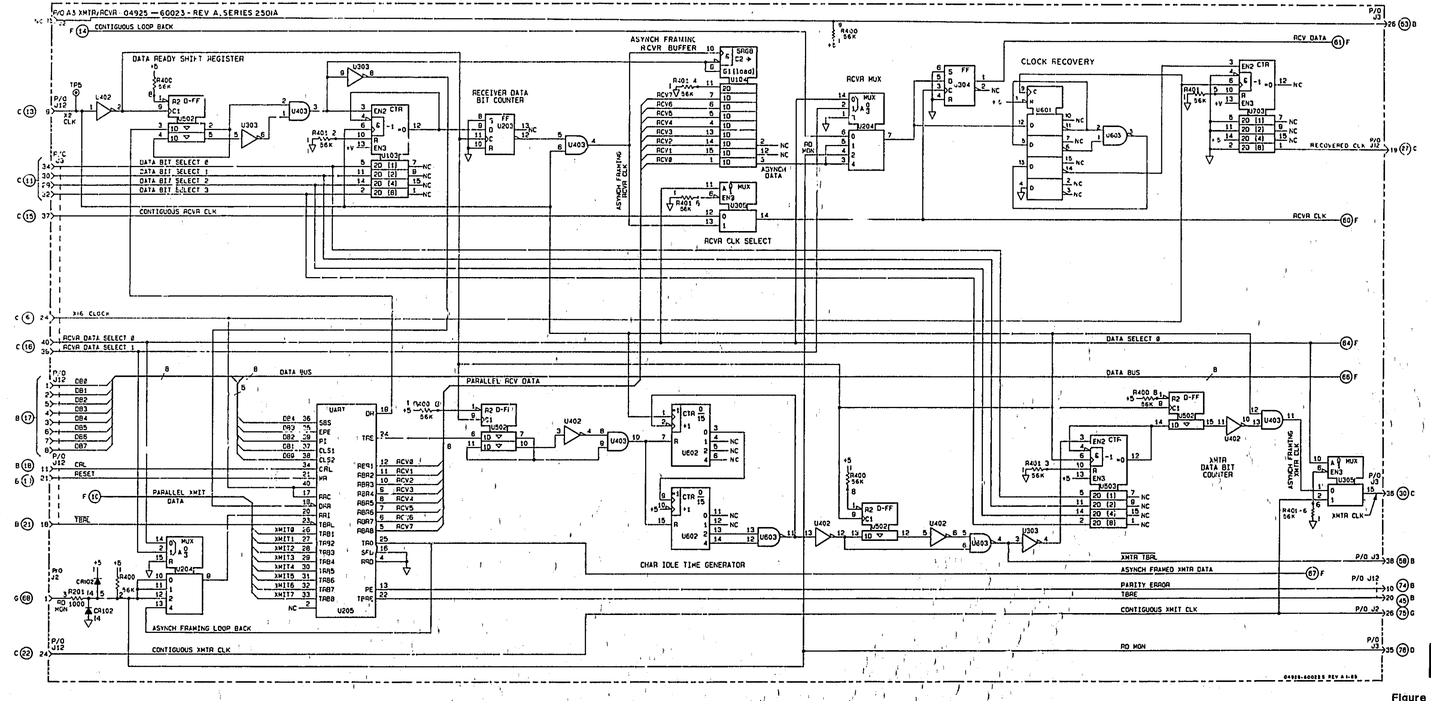
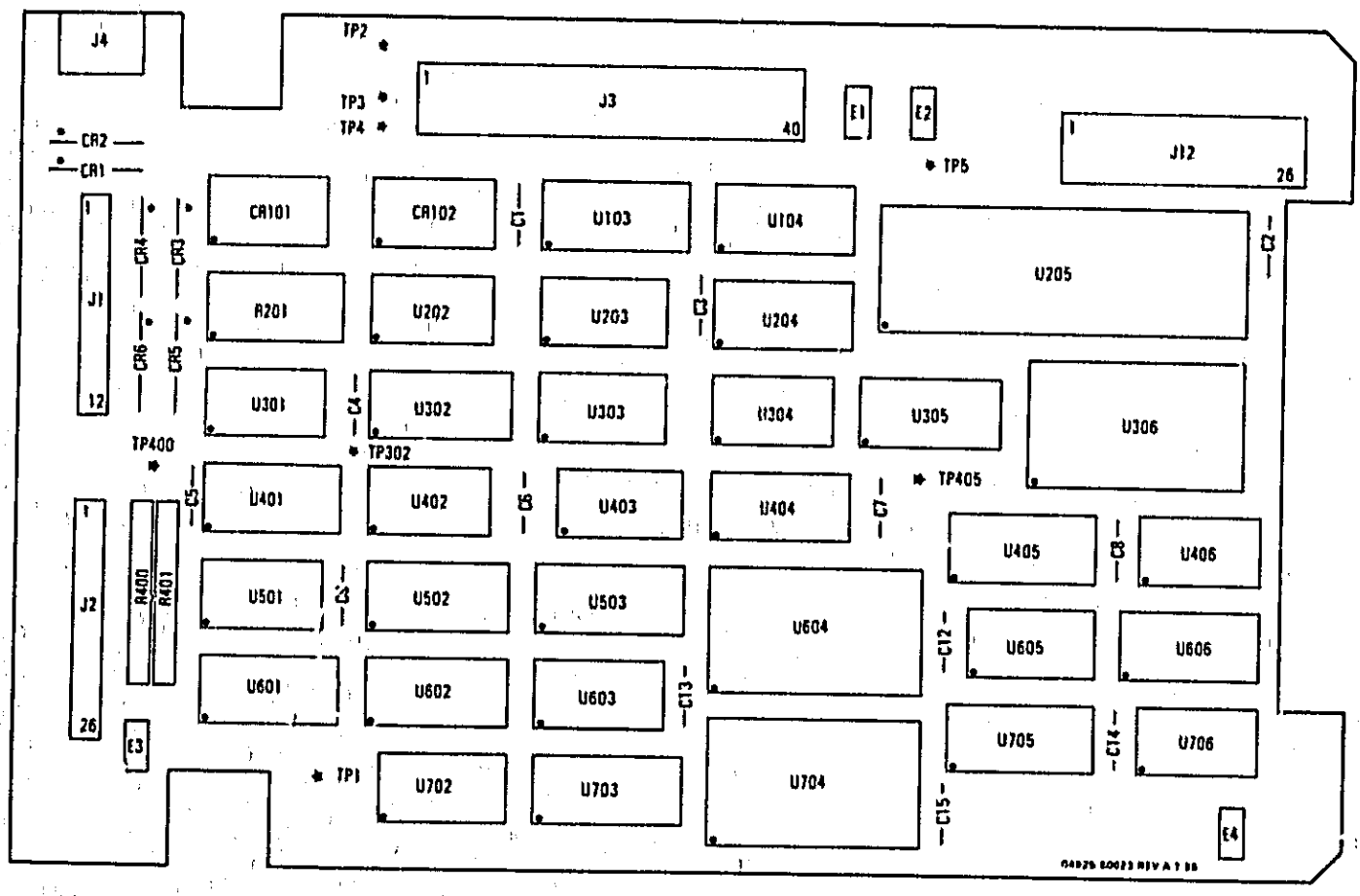


Figure 8-17.
A3 Transmitter/Receiver Board
Schematic Diagram (sheet 1 of 2)
8-75



A3 Transmitter/Receiver Board Component Locator

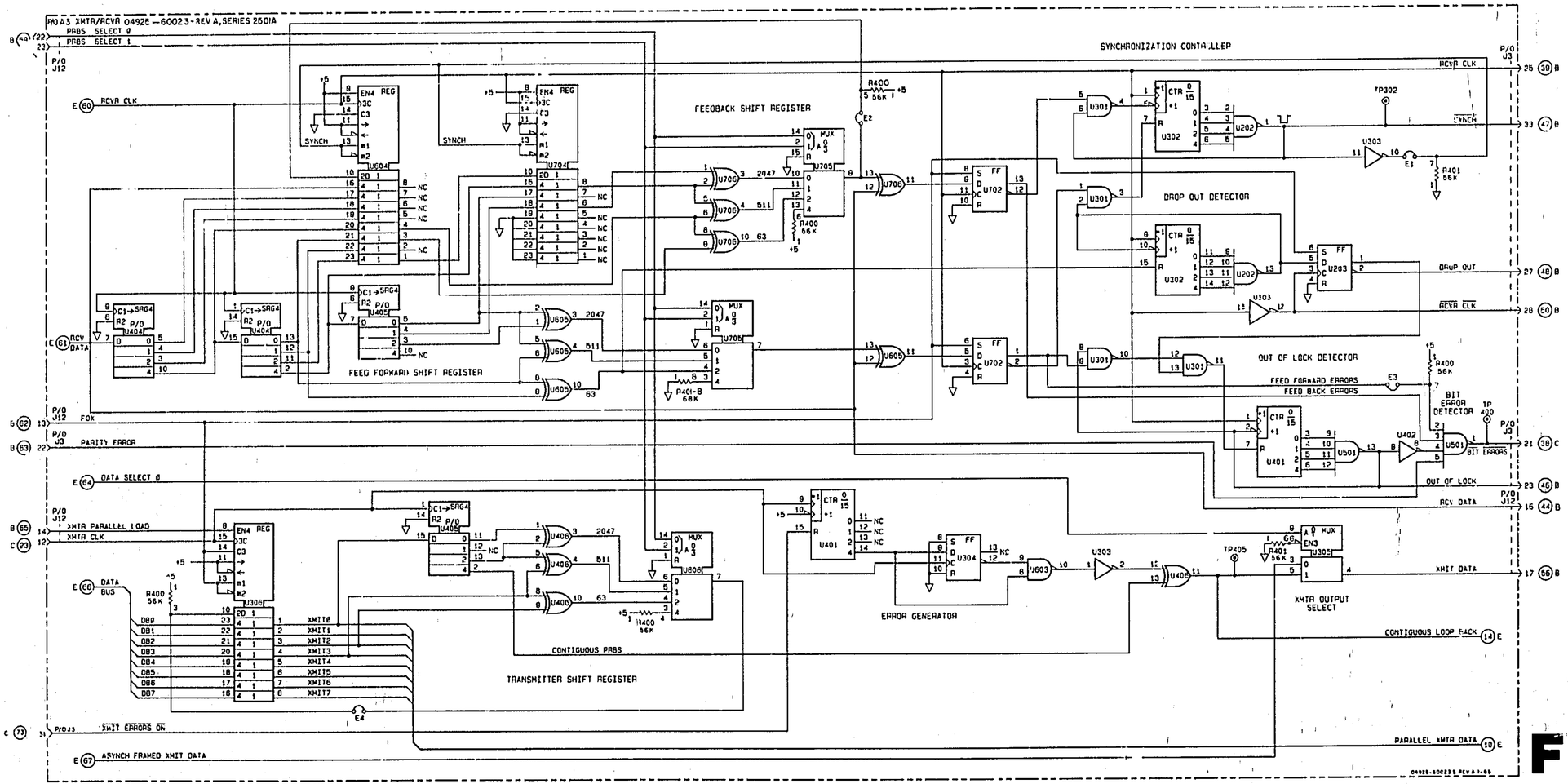


Figure 8-18.
A3 Transmitter/Receiver Board
Schematic Diagram (sheet 2 of 2)
8-77

APPENDIX A
HP 4925B IN CCITT MODE

A-1. INTRODUCTION

The HP 4925B Bit Error Rate Test Set may be configured to power on in CCITT mode rather than the standard 1000 bits/block. CCITT recommedations state that the block size for Bit Error testing should be 511 bits when sending 511 bit PRBS and 2047 bits when sending 2047 bit PRBS.

Jumper E1 configures the power up mode. If the modification procedure below has been performed, the test set will power up in CCITT mode. This means that if a test with 1000 bits/block must be performed, press BEGIN/END, then PATTERN to change the configuration to 1000 bits/block.

A-2. MODIFICATION PROCEDURE

By following the steps below, the procedure for pressing BEGIN/END, then PATTERN to put the test set into CCITT configuration will not be necessary.

1. Follow the disassembly procedure in paragraph 8-9, steps 1-8.
2. Remove E1, the CCITT jumper on the A2, Control Board. The jumper location is shown in Figure A-1 below.

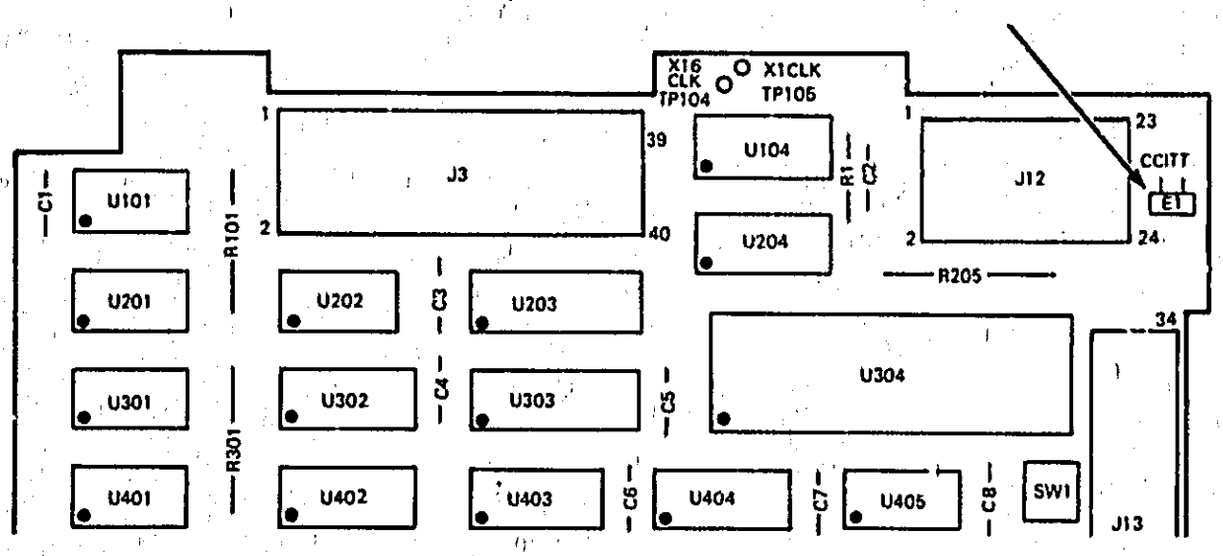


Figure A-1. E1 Jumper Location

3. Reassemble the test set following the procedure given in paragraph 8-10.

NOTE

The jumper may be replaced at anytime, to return to the standard 1000 bits/block configuration at power up.

4. Turn on the HP 4925B. CCITT appears momentarily on the display just before the top level menu.

A-3. READING CCITT TEST RESULTS

When testing in the CCITT environment, use the following formula to compute the number of received blocks:

511 bit block

$$\text{number of received blocks} = \text{number of received bits} \times \frac{\text{block}}{511 \text{ bits}}$$

2047 bit block

$$\text{number of received blocks} = \text{number of received bits} \times \frac{\text{block}}{2047 \text{ bits}}$$

A-4. EXAMPLE

For 10^5 received bits

$$10 \times \frac{1}{511} = 195.695 \text{ received blocks}$$

APPENDIX B
GUIDE TO INTERPRETING ANSI

1. INTRODUCTION.

The Institute of Electrical and Electronics Engineers (IEEE) is developing ANSI symbol notation. The symbols used in this manual's schematics are designed according to IEEE Draft 91PR79-16 N. Some basic elements are similar to conventional symbology, inputs on left and outputs on the right. Where conventional symbology gives a signal mnemonic, ANSI describes the functional behavior of the logic circuit, and the signal's relationship to other signals. The interpretation of this effort in our schematics is to describe the truth table of each component using the ANSI symbology. Including this information reduces need for component data and other support documents. Definitions of mnemonics and symbols, as well as illustrations are provided. Table 3 located after the symbol descriptions is a quick reference for ANSI symbols and notation.

2. SYMBOL OUTLINE

The physical layout of each symbol is simple, Figure 1 shows two variations. The style used depends on the function of the component. The difference between 1(a) and 1(b) is the control block. The control block visually emphasizes the difference between control and data inputs.

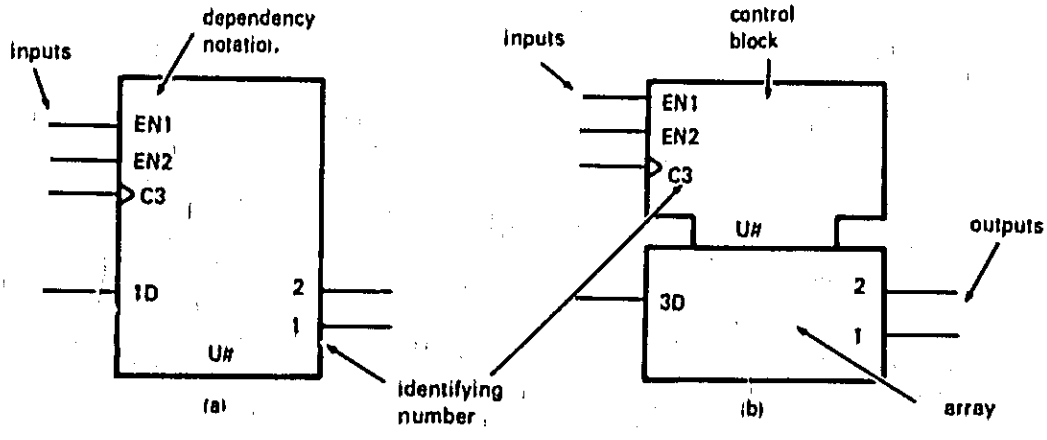


Figure 1. ANSI Symbol Outline

3. General Rules:

1. Inputs enter from the left side of the symbol. Elements modifying the inputs are shown with input notation.
2. Outputs leave from the right side of the symbol. Elements modifying the outputs are shown with output notation.
3. A symbol may have input or output notation, or both.
4. Symbols contain two essential ingredients: data and signals which modify the data.
   a. Data is shown coming into or leaving from the lower part of the symbol.
   b. Signals modifying data or other signals are described with DEPENDENCY NOTATION. These signals are input to the control block when symbol outline shown in Figure 1(b) is used.

4. DEPENDENCY NOTATION

Dependency notation defines relationships between internal logic states. It does not show all elements or interconnections and is written in alphanumberic form, A2 for example. The letter is a dependency notation symbol and the number is used for identification. There are two types of dependency notation.

1. Dependency notation at inputs describes conditions which permit action.

2. Dependency notation at outputs describes conditions which cause the outputs to be active.

5. General Rules

1. The component's truth table is described as accurately as possible through the combination of dependency notation used.

2. If input or output dependency notation is not present, then all inputs must be at their active state for the output to be active.

3. When an output has no label, its normally defined state is dependent on the inputs (low outputs will have low or negation symbol on the output line).

4. Labels describing the function of inputs or outputs are prefixed by identifying number(s) of any affecting input.

5. When an input or output is affected by more than one input, the identifying numbers of each affecting input will be in the label, separated by commas. The notation is read left to right.

6. The complement of an internal logic state which affects an input or output has a bar placed over the identifying numbers at the affected inputs or outputs.

7. When two or more combinations of inputs make an output or input valid, they are separated by a slanted line (/, solidi).

8. Labels may be factored using algebraic techniques.

$$A + B = A \text{ or } B$$
$$A \cdot B = A \text{ and } B$$

NOTE

For explanation and illustration in this text, the normally defined state of components in this Appendix follows positive logic conventions.

6. SEQUENCE OF INPUT LABELS

1. Labels are written left-to-right, in order (left has the first affect) according to their order of effect on the input.

2. If an input with a single function is affected by other inputs, the qualifying symbol is preceded by the identifying number(s) of the affecting inputs.

3. If an input performs several different functions, each may be described on separate input lines or on the same line with each effect separated by a slanted line (/). Figure 2 illustrates these two formats. In Figure 2(a) input c,

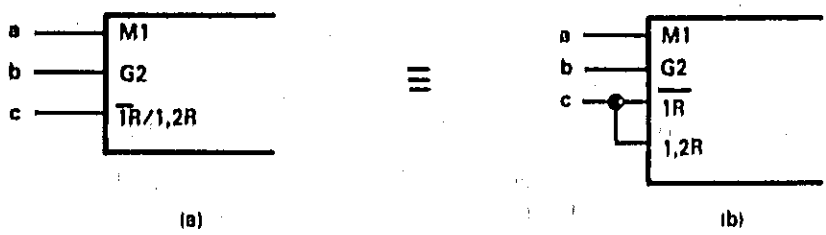


Figure 2. Dependency Notation Layout

a reset line is active when input a is high or (/) when inputs a and b are high. Figure 2(b) illustrates the same idea, but separates the two conditions showing them as separate inputs rather than combining them.

4. All affecting inputs must be in their respective active state for output or input notation to be valid.

5. Each condition imposed on an input by dependency notation must be valid for that input to be active. When an input is disabled, its contents are not changed and the respective outputs remain at their existing internal logic states.

6. Two adjacent identifying number notations not separated by a non-numeric character should be separated by a comma.

7. Sequence Of Output Labels

1. Outputs with several different labels, are shown in the following order (left to right):

   a. the postponed output symbol, when used,

   b. labels which indicate when the internal logic state of the output is affected, in left-to-right order,

   c. labels which indicate an effect of the output on inputs or other outputs of the element,

   d. finally, symbols for open circuit or tristate outputs are placed just inside the boundary.

2. If an output symbol has several sets of labels representing different functions (i.e., dependent on mode) these sets may be shown on different output lines connected outside the symbol outline (similar to the input examples shown in Figure B-2, only placed on the outputs).

   a. In cases when this method of presentation is not advantageous, the output may be shown once and each different set of labels should be separated by a slanted line (/).

3. Two adjacent identifying number notations not separated by a nonnumeric character should be separated by a comma.

8. DEPENDENCY NOTATION DESCRIPTION

To date IEEE has defined ten types of dependency notations. Table 1 gives a brief description of each type.

Table 1. ANSI Dependency Notation

Type of Dependency	Letter Symbol	Affecting Input At Its 1-State	Affecting Input At Its 0-State
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs outputs off outputs at external high impedance, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S=0, R=1	No effect
SET	S	Affected output reacts as it would to S=1, R=0	No effect
OR	V	Imposes 1 state	Permits action
Inter-connection	Z	Imposes 1 state	Imposes 0 state

9. ADDRESS (A)

Represents address inputs of a device. In particular, memories and similar devices which use addresses to select specified sections of a multidimensional array. Each address input is labeled with an A, followed by an identifying number which corresponds to the address selected by the input. Figure 3 illustrates address dependency notation.

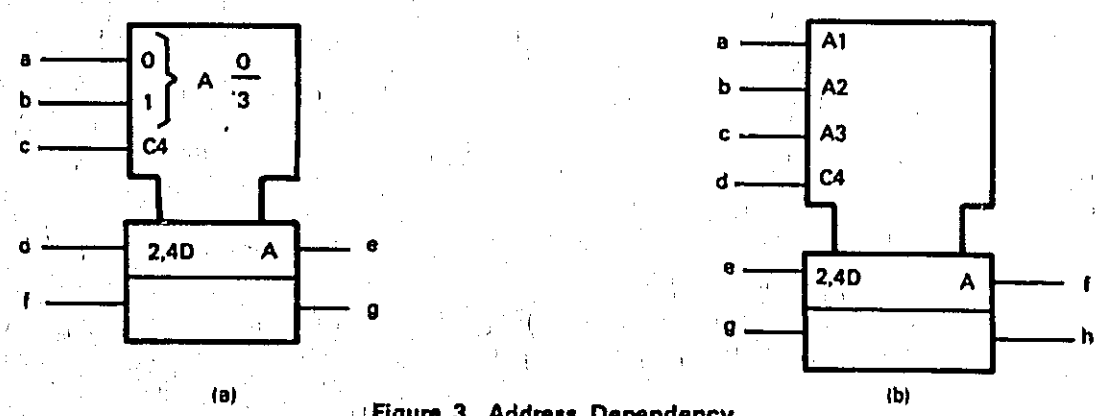


Figure 3. Address Dependency

INPUTS: In example (a) inputs b and c illustrate address lines which form a binary code address to select an output.

NOTE

Anytime that the form 3 or A0-3 is used in an ANSI symbol, it refers to the binary truth table. This means that there are four possible conditions (0-3) dependent on the state of the line. For example, if line a is high and line b is low, then address two (10) will be active. In other cases, with different dependency notation, it could be mode 2.

	a	b
0	0	0
1	0	1
2	1	0
3	1	1

The c input is a clock. The d input is a data input. Read the dependency notation as follows: mode 2 (10) and (,) the clock (4) must be active for data to enter the component.

Example (b) has three separate address lines. Each address is followed by an identifying number. Input e shows that when input b (identifying number 2) and input d, the clock (4) are active, data can be clocked into the component.

OUTPUTS: In this example there are no output dependencies. When the appropriate input lines are addressed, data will appear at the respective output.

10. CONTROL (C)

Control dependency identifies inputs that initiate actions, for example, an edge-triggered clock. These inputs can enable or disable data inputs of stored elements. An internal 1 state enables the affected inputs.

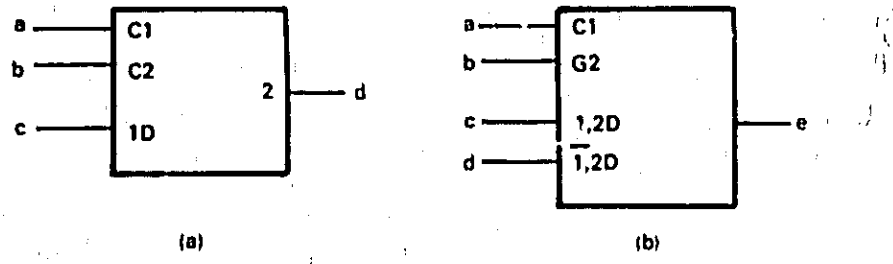


Figure 4. Control Dependency

Inputs: In example (a), both a and b are control inputs. They have different identifying numbers to show that they control different functions of the component. Thus input c is controlled by only input a.

In example (b), input c or d will be enabled dependent on the state of input a. When a is a 1, input c will be enabled; when it is a 0, input d will be enabled. The 2D shows that the affected input will be ANDed with input b (input b shows AND function).

Outputs: In example (a), for output d to be active, input b must be enabled (1 state).

In example (b), since no dependency notation is shown, the output is dependent on the inputs. When the inputs are active, the output is enabled.

11. ENABLE (EN)

Identifies enable inputs. When the EN input is at an internal 1 state, the inputs affected are enabled. When the EN input is at its internal 0 state, the inputs and outputs affected are disabled, open collector outputs are turned off, three-state outputs are at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem pole outputs) stand at their internal 0 states.

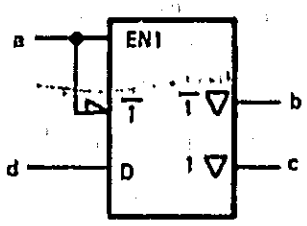


Figure 5. Enable Dependency

INPUT: Input a enables an output in either state. To emphasize this aspect, the signal is shown as two enable inputs. The second input has the identifying number 1 to show that it is dependent and in this case a part of EN1. Input d is a data input with dependencies.

OUTPUTS: When input a is low (0), output c is disabled and output b is enabled. When input a is high (1), output b is disabled and output c is enabled. The inverted triangle by the output indicates that it is a tri-state output.

12. AND (G)

Two inputs or outputs ANDed together is a common relationship. Traditionally AND gates are drawn as a part of the component outline with the signal input connected to the gate. G dependency notation describes this relationship as shown in Figure 6. When an input or output stands at its internal 1 state, all inputs and outputs affected are enabled.

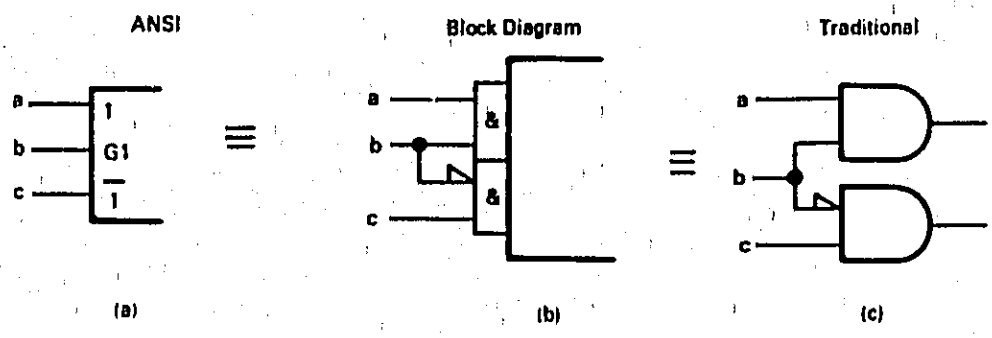


Figure 6. AND Dependency

INPUTS: Example (a) describes a component with two 2-input AND gate. Inputs a and c are dependent on input b. To show this dependency inputs a and c are labeled with a "1", which refers to the 1 of input b. To make input a active, input b must be at a 1 state (high); for input c to be active, input b must be at a 0 state (low).

OUTPUTS: Although no outputs are shown in the above examples, when a G dependency appears, they should be read the same way as inputs.

13. MODE (M)

Mode dependency identifies one or more inputs which select the operation mode of a component. When an M dependency identifies several modes or functions, the appropriate identifying number is placed in the label of the affected input or output. Each function applying to an input is seperated by a slanted line (/). When the M input or output is at its internal 1 state, the affected inputs or outputs are enabled.

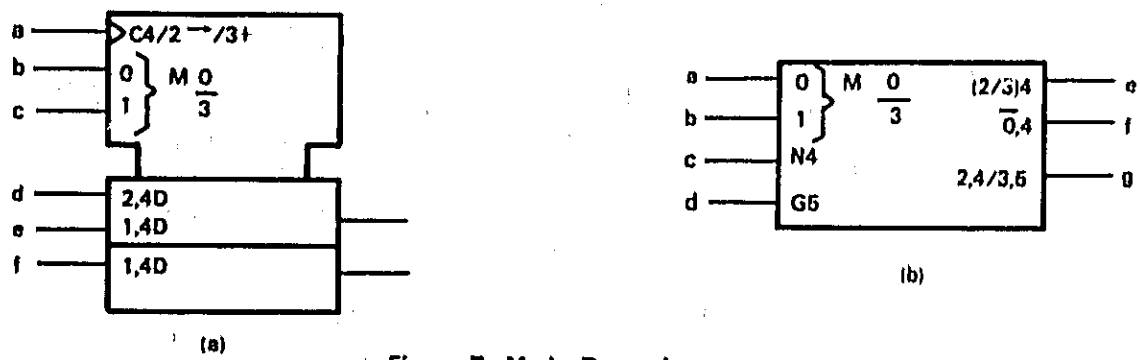


Figure 7. Mode Dependency

INPUTS: In example (a), input a is the control input. It controls three functions. It is a clock for entering data. In mode 2 it causes data to shift right once and in mode 3 the contents of the register are incremented by 1 count. Inputs b and c form a binary number. The mode or state which is created identifies the operation mode of the component. In this case:

Mode 0 (b=0,c=0), inputs do not affect outputs, so the outputs remain at their existing state
Mode 1 (b=1,c=0), inputs e and f are active, data enters the component
Mode 2 (b-0,c=1), shifting down and serial loading through input d takes place
Mode 3 (b=c=1), counts up by 1 count per clock pulse

NOTE

Any time that the form 3 or M0-3 is used in an ANSI symbol, it refers to the binary truth table. This means that there are four possible conditions (0-3) dependent on the state of the line. For example, if line a is nigh and line b is low then mode 2 (10) will be active.

	a	b
0	0	0
1	0	1
2	1	0
3	1	1

Input d is enabled in mode 2 when the control (4) is active.
Input e is enabled in mode 1 when the control (4) is active.
Input f is enabled in mode 1 when the control (4) is active.
In example (b), inputs a and b should be combined to represent a binary number. Each binary number enables a different mode. Input c forms an exclusive OR relationship with any input or output it modifies. Input d forms an AND relationship with anything it modifies.

OUTPUTS: In example (a) the outputs are determined by the inputs, so no further dependency notation is needed.

In example (b), output e may also be read 2,4/3,4. When mode 2 or mode 3 is negated by input c, this output will be active. Output f is active whenever the mode is not 0 and negated by input c. When output g is active, mode 2 is negated by input c or mode 3 is ANDed with input d.

14. NEGATE (N)

Each input or output affected by N inputs or outputs has an exclusive OR relationship with that input or output. When an N input or output stands at its internal 1 state, the internal logic state of each input and output stands at its internal 0 state.

Figure 8. Negate Dependency

INPUT: The a input indicates that there is an exclusive OR relationship.

OUTPUTS: Output b is not affected by input a. Output c has an exclusive OR relationship with input a. If a = 0, then c = b; if a = 1, then c = b.

Table 8. Exclusive OR Truth Table

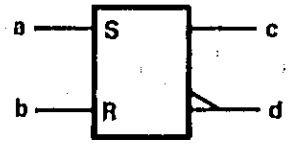
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

15. RESET (R) and SET (S)

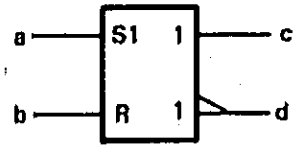
SET AND RESET dependencies specify the effect of a combination of R and S elements in a bistable component. R and S dependencies affect outputs only.

When S input stands at its internal 1 state, the outputs will take on the internal logic states for the combination S=1 and R=0, regardless of the state of any R input. At an internal 0 state the S dependency has no effect.

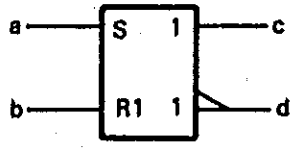
An R input at its internal 1 state causes the outputs to take on the internal logic state for the combination S=0 and R=1, regardless of any S state input.



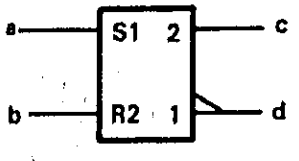
a	b	c	d
0	0	no change	
0	1	0	1
1	0	1	0
1	1	not specified	



a	b	c	d
0	0	no change	
0	1	0	1
1	0	1	0
1	1	1	0



a	b	c	d
0	0	no change	
0	1	0	1
1	0	1	0
1	1	c	c



a	b	c	d
0	0	no change	
0	1	0	1
1	0	1	0
1	1	0	0

NOTE

0 = external 0 state
1 = external 1 state

Figure 9. RESET/SET Dependency

16. OR (V)

V dependency shows a Boolean relationship between inputs and outputs. When a V input or output is at an internal 1 state, all inputs and outputs affected are at their internal 1 state. When a V input or output is at an internal 0 state, all inputs and outputs affected are at their normally defined internal logic states.

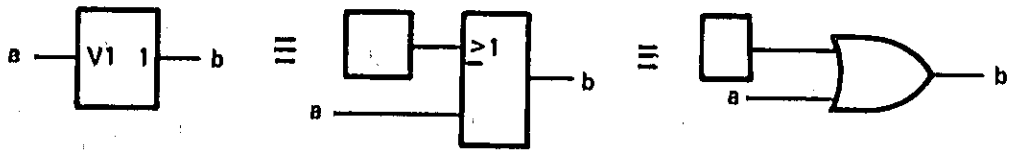


Figure 10. Or Dependency

INPUT: The a input indicates that there is an OR relationship to the output.

OUTPUT: The a input is ORed with internal state of the b output.

17. TRANSMISSION (X)

Transmission dependency indicates controlled bidirectional connections between affected input and output ports. When an X input or output is at its internal 1 state, all input and output ports affected are bidirectionally connected and are at the same internal logic state or analog signal level. When an X input or output is at its internal 0 state, the connection associated with this dependency notation is broken.

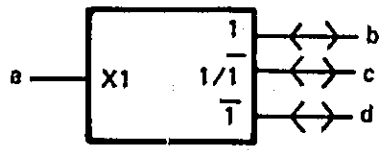


Figure 11. Transmission Dependency

INPUT: Input a indicates that a transmission dependency exists between outputs.

OUTPUT: When input a is at a 1 state, there is a bidirectional internal connection between outputs b and c. If input a is at a 0 state there is a bidirectional connection between outputs c and d.

18. INTERCONNECTION (Z)

Indicates connections between inputs, outputs, internal inputs, and internal outputs in any combination inside the symbol. The internal logic state of an input or output affected by a Z input or output remains the same, unless modified by additional dependency notation.

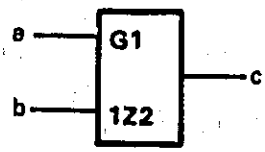


Figure 12. Interconnection Dependency

INPUTS: Input a indicates an AND relationship. When input a is ANDed with input b there is an internal connection which will not affect the output state.

OUTPUT: Notice that there is no output dependency, this means that any output is dependent on the inputs. Output c is active if input b makes the internal connection. The output state is the same as the internal logic state.

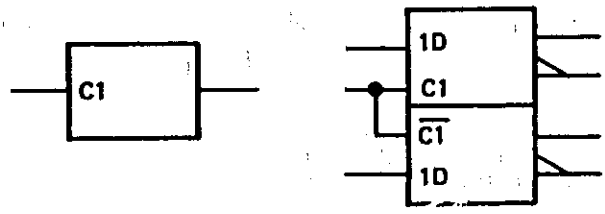
19. BISTABLE ELEMENTS

The four types of bistable elements use the dynamic input symbol, the postponed symbol, and dependency notation.

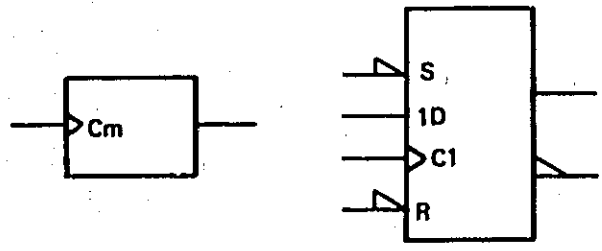
1. Transparent latch inputs are level-operated. The D input is active while the C input is at its internal 1 state.
2. Edge-triggered components accept data from D, J, K, R, or S inputs on the active transition of the C input.
3. Pulse-triggered components require data to be setup before the control pulse starts. The C input is static since the output is postponed
4. The data-lock-out component is similar to the pulse triggered. The C input is dynamic since after input C goes through its active transition, the data inputs are disabled and data is not held. The output is postponed until the C input returns to its initial external level.

Synchronous inputs are identified by their dependency labels (1D, 1J, 1K, 1S, 1R), whereas asynchronous inputs (S,R) are not dependent on C inputs.

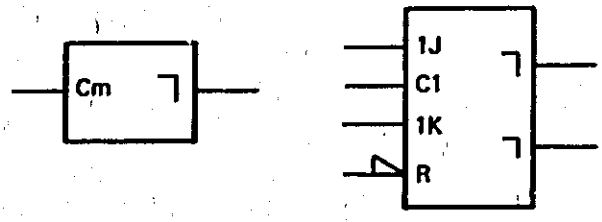
Transparent Latches



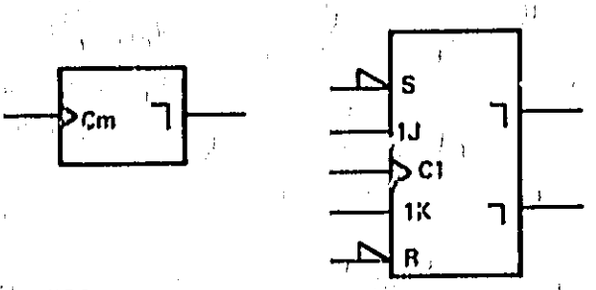
Edge Triggered Bistable



Pulse Triggered Bistable



Data-Lock-Out Bistable



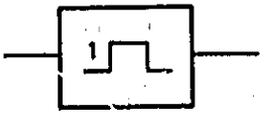
20. MONOSTABLE ELEMENTS

There are two types of monostable elements: retriggerable and non-retriggerable. The first retriggers during the output pulse. The second can not be retriggered during the output pulse.

21. Retriggerable Monostable

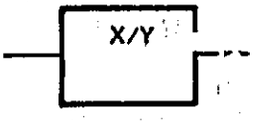
When the input changes to a 1 state the output changes to or remains at a 1 state. After a period of time characteristic to the device, the output returns to 0 state.

22. Non-retriggerable Monostable



When the input changes to 1 state, the output changes to 1 state. The output returns to 0 state after a period of time characteristic of the device, regardless of any input variable changes.

23. CODERS



X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and outputs respectively.

For each input code, the internal input logic state determines an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

Relationships between internal logic states of inputs and the internal value is indicated one of two ways.

1. Labeling the inputs with numbers, the internal value equals the sum of the weights associated with the inputs at their internal 1 state.

2. Replacing X with an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

Relationships between the internal value and the internal logic states of the output are indicated in one of two ways.

1. The output label is a list of numbers which represent the internal values leading to the internal 1-state of the output. Each number in the list is separated by a slanted line (/). This labeling may be used when Y is replaced by a letter denoting a type of dependency. If a continuous range of internal values produces the internal 1 state of an output, this is indicated by two numbers. The beginning and the end of the range are separated by three dots.

2. Replace Y with an appropriate indication of the output code and label the outputs with characters that refer to this code.

Table 3. General Qualifying Symbols

Symbol	Description
&	And gate or function.
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.
=1	Exclusive OR. One and only one input must be active to activate the output.
=	Logic identity. All inputs must stand at same state.
2k	An even number of inputs must be active.
2k+1	An odd number of inputs must be active.
1	The one input must be active.
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).
⊓	Schmitt trigger; element with hysteresis.
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).
MUX	Multiplexer/data selector.
DMUX or DX	Demultiplexer.
Σ	Adder.
P−Q	Subtracter.
CPG	Look-ahead carry generator.
π	Multiplier.
COMP	Magnitude comparator.
ALU	Arithmetic logic unit.
⌐⌐	Retriggerable monostable.
1 ⌐⌐	Non-retriggerable monostable (one-shot).
G ⌐⌐	Astable element. Showing waveform is optional.
IG ⌐⌐	Synchronously starting astable.
GI ⌐⌐	Astable element that stops with a completed pulse.
SRGm	Shift register. m = number of bits.
CTRm	Counter. m = number of bits; cycle length = 2m.
CTR DIVm	Counter with cycle length = m.
ROM	Read-only memory.
RAM	Random-access read/write memory.
FIFO	First-in, first-out memory.

*Not all of the general qualifying symbols have been used in this manual but they are included here for the sake of completeness.

Table 3. General Qualifying Symbols (cont'd.)

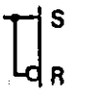
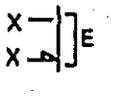
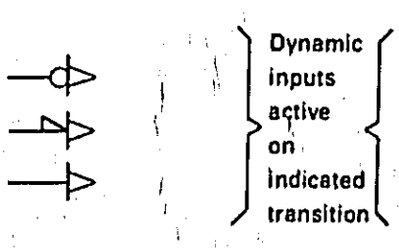
Symbol	Description
⌐|	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level.
—|⊓	Bi-threshold input (input with hysteresis).
Ω|	NPN open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection.
⟐|	Passive-pull-up output is similar to NPN open-collector output but is supplemented with a built-in passive pull-up.
▽|	NPN pen-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection.
⟐|	Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down.
▽|	3-state output.
—|	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off. Three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem poles) are at the internal 0-state.
	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
—|D	Data input to a storage element equivalent to: 
—|→ m —|← m	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
—|+m —|−m	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.
—| CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT = 9 |—	The content output is active if the content of the register is as indicated.
	Input line grouping. . . indicates two or more terminals used to implement a single logic input.
	e.g., The paired expander inputs of SN7450. 
"1" |—	Fixed-state output always stands at its internal 1 state.

Table 3. General Qualifying Symbols (cont'd.)

Symbol	Description
	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to  in positive logic.
	Active-low output. Equivalent to  in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.
	Dynamic inputs active on indicated transition. POSITIVE LOGIC: 1→0; not used; 0→1. NEGATIVE LOGIC: 0→1; not used; 1→0. POLARITY INDICATION: not used; H→L; L→H.
	No logic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

APPENDIX C
HP 18183A
RS-232C/V.24 INTERFACE

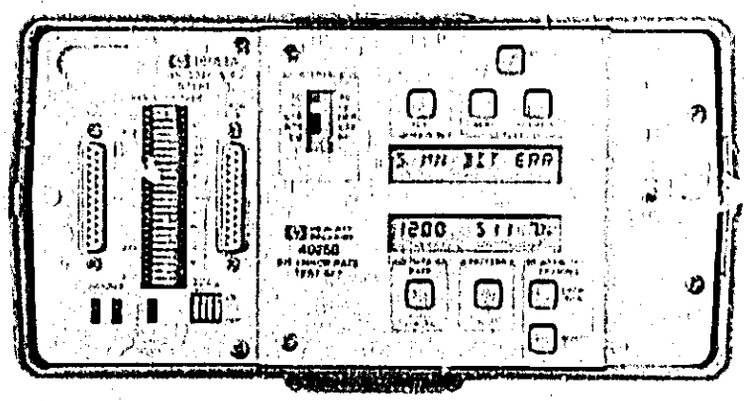


Figure C-1. HP 18183A Interface Pod

C-1. INTRODUCTION

The HP 18183A is an RS-232C/ V.24 interface designed to provide connection between the HP 4925B Bit Error Rate Test Set and the system under test.

This appendix includes information to install, operate, and service the HP 18183A.

C-2. DESCRIPTION

Level I protocol describes the overall interchange between terminal equipment and modems on a digital interface. This includes control priorities, timing sequences, and absolute voltage levels. The most common data interface is recommended by CCITT V.24, the international standard for low speed data communication. EIA standard RS-232C incorporates the V.24 recommendations and further specifies the mechanical connector type and pin configurations for each of the signals on the low speed data interface. The interface contains a Breakout Box which provides the following test capabilities.

Individual Line Tests interrupts the line, monitors the status, or allow you to patch any line from the DCE to the DTE side of the interface.

EIA Voltage Sources, a set of voltage sources used to force a line to a desired state (mark or space).

Passive Bridge Monitor provides a way to disable the HP 4925B line drivers. This allows the interface to be used as a breakcut box to bridge the line and monitor EIA status or measure RTS-CTS delay time.

C-3. SPECIFICATIONS

Table C-1. HP 18183A Specifications

*	Individual switches for line isolation
*	test points for line monitoring, forcing or patching
*	One non-dedicated mark/space tristate activity monitor for user patching to any line
*	10 Hard-wired activity indicators
*	Bridging impedance: 20 Kohms
*	Dedicated mark/space monitor: impedance 3 Kohms
*	Interface surge protection: 50 V maximum
*	Interface monitors: LCD's driven by nominal +2.5 volt level detector to accept a wide variety of interface levels
*	Tristate Mark/Space activity monitor driven by nominal +-2 volt level detector

C-4. INSTALLATION

This section provides information to install and provide power for the HP 18183A interface.

C-5. INITIAL INSPECTION. Inspect the interface for any physical damage sustained in transit. If the unit is received in a damaged condition, notify the nearest HP Sales and Service Office.

C-6. TAGGING FOR SERVICE. If the instrument is returned to Hewlett-Packard for service, complete one of the blue repair tags located in the back of this manual and attach it to the instrument. Follow the packaging instructions described in Section II of the HP 4925B Operating and Service Manual.

C-7. INSTALLATION PROCEDURE

This section covers installation of the Patch Wire Holder and the interface.

Installation of the Patch Wire Holder

Remove the wire holder (HP 1400-0510) from the storage bag. Peel off the protective strip on the back. Firmly press the wireholder to any flat surface. Slip the patch wires into place.

The HP 18183A interface fits into the HP 4925B case. Follow the procedures below to install the interface.

Remove the interface currently in the HP 4925B (if necessary).

a. Remove the three screws securing the interface.

b. Grasp the interface by the connectors and captive screw and lift it out of the HP 4925B case.

c. Disconnect the cable between the interface and the HP 4925B.

Install the Interface

a. Connect the interface cable to J2 on the A3, Transmitter/Receiver Board.

b. Place the interface into the HP 4925D case.

c. Insert and tighten the three screws that hold the interface in the case.

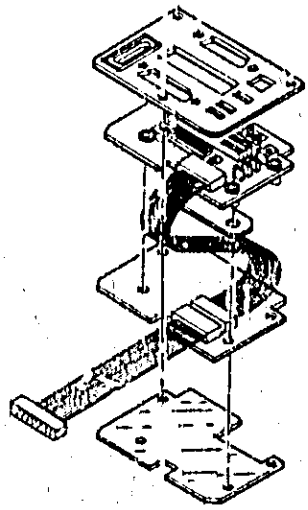


Figure C-2. Board Assembly Sequence

C-8. OPERATION

This section describes the front panel controls, indicators, and connectors, as well as operation of the HP 18183A Interface.

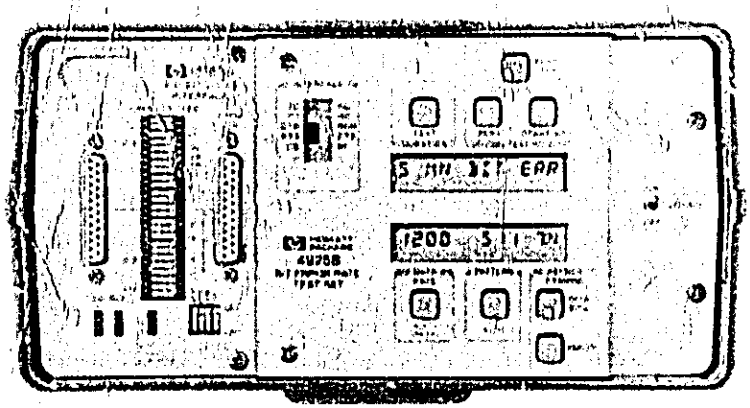


Figure C-3. HP 18183A Front Panel

Breakout Box Switch — Interrupt switches used to break and patch individual lines. The switches are between two 25 pin connectors labeled TO DCE and FROM DTE.

TO DCE — An RS-232C/V.24 connector connecting the Bit Error Rate Test Set to a modem, terminal, or printer under test.

FROM DTE — Provides RS-232C/V.24 connection from the terminal equipment DTE when a line is to be bridged.

SOURCE Sockets — These are voltage source sockets. The positive and negative voltages +-6 to +-12 (if HP 18185A is power source) volts respectively and may be used to force any line to a high or low state.

MARK/SPACE MONITOR — An input connector used to monitor any EIA line. All three socket holes are common.

XTC,RTS,DTR TO,ON/OFF — These switches interrupt the External Transmit Clock (XTC), Request to Send (RTS), Data Terminal Rady (DTR), or Transmit Data (TD) drivers. The switches should be in the ON position for most testing. Turn the switch to OFF when the Bit Error Rate Test Set passively bridges a line.

C-9. PERFORMANCE VERIFICATION

Performance Verification testing is performed during the instrument self test at turn on.

C-10. ADJUSTMENTS

There are no adjustments for the HP 18183A.

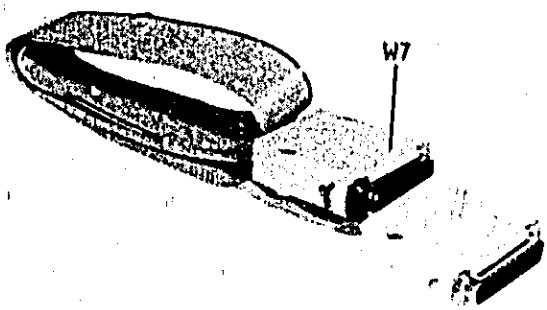
C-11. REPLACEABLE PARTS

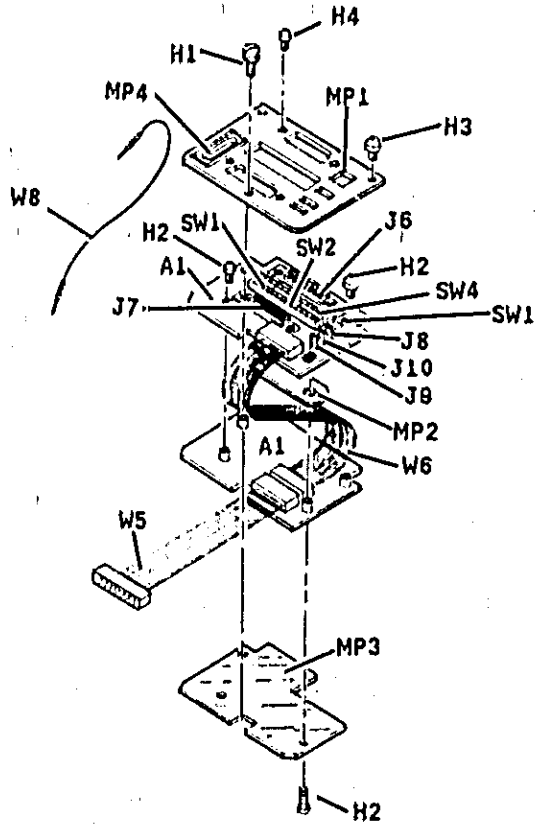
The following tables and figure give information for ordering replacement parts. Table C-2 is the Manufacturer's Code List. Table C-3 lists the replaceable parts in alphanumeric order. Information is given for the Description, Quantity, HP Part Number, and Manufacturers Part Number. Chassis and mechanical parts are listed in Figure C-3. To order a listed part, quote the HP Part Number, indicate the quantity needed, and send the order to the nearest Hewlett-Packard office.

When ordering a part not listed, include the instrument model number, serial number, and a physical and functional description of the part. Send the order to the nearest Hewlett-Packard office.

Table C-2. Manufacturers Code List

Mfr No.	Manufacturer Name	Address	Zip Code
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN BRADLEY CO	MILWAUKEE WI	53204
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
11236	CTS OF BERNE INC	BERNE IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	
32293	INTERSIL INC	CUPERTINO CA	95014
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247





Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	18183-60001	6	1	RS-232C/V.24 INTERFACE BOARD	28480	18183-60001
H1	1390-0429	6	1	SCREW,CAPTIVE 6-32	03901	PS10-632-40
H2	2200-0592	3	7	SCREW, 4-40	04771	ORDER BY DESCRIPTION
H3	2200-0193	8	2	SCREW, MACH, 6-32 .25IN,POZI	28480	2200 0193
H4	2200-0137	2	3	SCREW,MACH 4-40,.188	28480	2200-0137
J6	1251-4946	6	1	CONNECTOR	04507	DB-25SV
J7	1251-4946	6	1	CONNECTOR	04507	DB-25SV
J8	1251-7989	2	3	CONN-POST TYPE-SKT	03206	76308-203
J9	1251-7989	2	3	CONN-POST TYPE-SKT	03206	76308-203
J10	1251-7989	2	3	CONN-POST TYPE-SKT	03206	76308-203
MP1	18183-00001	4	1	FRONT PANEL	28480	18183-00001
MP2	04925-20010	6	1	COVER PLATE	28480	04925-20010
MP3	5020-5262	5	1	PLASTIC SHIELD	28480	5020-5262
MP4	4040-2143	6	1	PANEL PLUG	28480	4040-2143
SW1	3101-2664	6	1	SWITCH, 4-POSITION DIP, ROCKER	05735	240004GB
SW2	3101-2619	9	2	SWITCH, 10 POSITION, ROCKER	05735	240010GB
SW3	3101-2619	9		SWITCH, 10 POSITION, ROCKER	05735	240010GB
SW4	3101-2619	0	1	SWITCH, 5 POSITION, ROCKER	05735	240005GB
W5	04925-61602	8	1	W5, CABLE	28480	04925-61602
W6	04925-61605	1	1	W6, CABLE	28480	04925-61605
W7	04925-61607	3	1	RS-232C/V.24 INTERFACE CABLE	28480	04925-61607
W8	04925-61608	4	6	PATCH WIRES	28480	04925-61608

See introduction to this section for ordering information

Figure C-4. HP 18183A Exploded View

Table C-3. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	18183-60001	2	1	RS-232C/V.24 INTERFACE ASSEMBLY	28480	18183-60001
A1C1	0160-5332	1	11	CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C2	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C3	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C4	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C5	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C6	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C7	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C8	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C9	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1C11	0160-5332	1		CAPACITOR-FXD .1UF 20% 50VDC	28480	0160-5332
A1CR202	1906-0074	1	2	DIODE ARRAY	28480	1906-0074
A1LR302	1906-0074	1	2	DIODE ARRAY	28480	1906-0074
A1J6	1251-4946	5	2	CONNECTOR-25 PIN FEMALE	28480	1251-4946
A1J7	1251-4946	5		CONNECTOR-25 PIN FEMALE	28480	1251-4946
A1J8	1251-7989	2	3	HEADER	28480	1251-7989
A1J9	1251-7989	2		HEADER	28480	1251-7989
A1J15	0362-0390	9		CONECTOR-26 PIN PC	28480	0362-0390
A1J17	1251-7988	1	2	HEADER	28480	1251-7988
A1J18	1251-7988	1	2	HEADER	28480	1251-7988
A1JU1	1251-5285	7	1	DIP POST-TP-HDR	03206	65521-102
A1JU1	1258-0141	8	1	JUMPER, REMOVEABLE	03206	65474-004
A1U507	1258-0086	2	2	TRANSISTOR, ARRAY 14-PIN	02037	MPQ6700
A1U704	1258-0086	2		TRANSISTOR, ARRAY 14-PIN	02037	MPQ6700
A1R1	0699-1084	3	3	RESISTOR-FXD 270 OHM 5% 2w	28480	0699-1084
A1R2	0699-1084	3		RESISTOR-FXD 270 OHM 5% 2w	28480	0699-1084
A1R3	0698-3410	1	1	RESISTOR 3.16K 1% .5W F TC=0+-100	28480	0698-3410
A1R4	0757-0289	2	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MFAC1/8 TO 1332 T
A1R5	0757-0461	2	1	RESISTOR 68.1K 1% .125 F TC=0+-100	24546	C4-1/8-TO 6812-F
A1R6	0698-3160	8	1	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4 1/8 TO 3162-F
A1R7	0757-0458	7	2	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4 1/8 TO 5112-F
A1R8	0698-8827	4	4	RESISTOR 1M 1% .125W F TC=0+-100	28480	8827
A1R9	0698-3457	6	3	RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A1R10	0698-3460	1	1	RESISTOR 422K 1% .125w F TC=0+-100	28480	0698-3457
A1R11	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5112-F
A1R12	0757-0464	5	2	RESISTOR 90.9K 1% .125W F TC=0+-100	24546	C4-1/8-TO-90092-F
A1R13	0757-0464	5		RESISTOR 90.9K 1% .125W F TC=0+-100	24546	C4-1/8-TO-90092-F
A1R14	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A1R15	0698-3453	2	2	RESISTOR 196K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1963-F
A1R16	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A1R17	0698-3453	2	2	RESISTOR 196K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1963-F
A1R18	0698-8827	4		RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A1R19	0698-8827	4		RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A1R20	0698-8827	4		RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A1R21	0699-1083	2	5	RESISTOR-FXD 220 OHM 5% 2w	28480	0699-1083
A1R22	0699-1083	2		RESISTOR-FXD 220 OHM 5% 2w	28480	0699-1083
A1R23	0699-1083	2		RESISTOR-FXD 220 OHM 5% 2w	28480	0699-1083
A1R24	0699-1083	2		RESISTOR-FXD 220 OHM 5% 2w	28480	0699-1083
A1R25	0699-1083	2		RESISTOR-FXD 220 OHM 5% 2w	28480	0699-1083
A1R26	0699-1084	3		RESISTOR-FXD 270 OHM 5% 2W	28480	0699-1084
A1R27	0699-1083	2		RESISTOR-FXD 220 OHM 5% 2w	28480	0699-1083
A1R101	1810-0637	9	8	CUSTOM RESISTOR	28480	1810-0637
A1R102	1810-0638	0	3	CUSTOM RESISTOR	28480	1810-0638
A1R103	1810-0638	0		CUSTOM RESISTOR	28480	1810-0638
A1R104	1810-0638	0		CUSTOM RESISTOR	28480	1810-0638
A1R105	1810-0207	9	2	RESISTOR-NETWORK 8 SIP 22.0K X 7	01121	208A223
A1R201	1810-0637	9	8	CUSTOM RESISTOR	28480	1810-0637
A1R202	1810-0637	9		RESISTOR, CUSTOM	28480	1810-0637
A1R203	1810-0637	9		RESISTOR, CUSTOM	28480	1810-0637
A1R204	1810-0207	9		RESISTOR-NETWORK 22.0K X 7	01121	2081223
A1R601	1810-0637	9		RESISTOR, CUSTOM	28480	1810-0637
A1R602	1810-0637	9		RESISTOR, CUSTOM	28480	1810-0637
A1R701	1810-0637	9		RESISTOR, CUSTOM	28480	1810-0637
A1R702	1810-0637	9		RESISTOR, CUSTOM	28480	1810-0637
A1R704	1810-0207	9		RESISTOR-NETWORK 22.0K X 7	01121	2081223
A1R705	1810-0224	0		RESISTOR-NETWORK 33.0K X 4	01607	20883333
A1SW1	3101-2664	5	1	SWITCH	28480	3101-2664
A1SW2	3101-2618	9	2	DIP SWITCH	28480	3101-2618
A1SW3	3101-2618	9		DIP SWITCH	28480	3101-2618
A1SW4	3101-2619	0	1	DIP SWITCH	28480	3101-2619
A1U101	1826-0759	9	4	IC COMPARATOR GP QUAD 14-DIP C PKG	04713	LM339J
A1U201	1826-0759	9		IC COMPARATOR GP QUAD 14-DIP C PKG	04713	LM339J

Table C-3. Replaceable Parts (Cont)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U203	1826-0759	6	1	IC COMPARATOR GP QUAD 14-DIP C PKG	04713	LM339J
A1U501	1820-1146	6		IC BFR CMOS NON-INV HEX	3L685	CD4050BE
A1U701	1826-0759	6		IC COMPARATOR GP QUAD 14-DIP C PKG	04713	LM339J
		6	4			
TP1 -VB	1281-8360		4	CONNECTOR-POST .025	28480	1281-8360
TP4 +VB	1281-8360	6	4	CONNECTOR-POST .025	28480	1281-8360
TP3 GND	1281-8360	8	4	CONNECTOR-POST .025	28480	1281-8360
TP2 +5	1281-8360	6		CONNECTOR-POST .025	28480	1281-8360

C-12. SERVICE

The following sections contains service information for the HP 18183A. Included is the Theory of Operation, RS-232C Signal Mnemonics, Troubleshooting, Component Locators, and Schematics.

C-13. RECEIVERS. The RS-232C Interface Board contains twelve receivers which monitor ten EIA lines. The following lines are monitored:

Transmit Data	Receive Data
Transmit Clock	Receive Clock
Data Terminal Ready	Data Set Ready
Request to Send	Clear to Send
Data Carrier Detect	Ring Indicator

All receivers are inverting, except the two receiver of the spare indicator which form a tristate EIA line indicator.

All receivers except the spare indicator have an input impedance of approximately 10 Kohms. The spare indicator input impedance is approximately 3 Kohms. Trip points for the receivers are aproximately 3.0 volts, except for the mark monitor which is approximately -3.0 volts.

C-14. TRANSMITTERS. The Bit Error Rate Test Set transmits on four lines:

(TD) Transmit Data	(RD) Receive Data
(RTS) Request to Send	(DTR) Data Terminal Ready

Three of the transmitters are comparators driving a discrete output stage to provide the necessary current driving capabilities. The fourth transmitter (DTR) is the positive voltage source in series with a 220 ohm resistor.

C-15. BREAKOUT BOX

The Breakout Box is integral to the RS-232C interface, it has 25 DIP switches allowing the user to make or break connections with any of the 25 lines. On the interface Board there are two RS-232C connectors.

C-16. RS-232C SIGNAL MNEMONICS

The HP 18183A is designed to accommodate two similar interface standards, RS-232C and V.24. Table C-4 describes RS-232C Signal Mnemonics. The label "Common" under "Signal Mnemonics" lists mnemonics used in the Service Section of the HP 4925B manual and in the schematics.

Table C-4. RS-232C/V.24 Signal Mnemonics

Connector Pin Number	Signal Mnemonics EIA	CCITT	Common	Description	DCE DTE
1	AA	101		Protective Ground	
2	BA	103	TD	Transmitted Data	<--
3	BB	104	RD	Received Data	-->
4	CA	105	RTS	Request To Send	<--
5	CB	106	CTS	Clear To Send	-->
6	CC	107	DSR	Data Set Ready	-->
7	AB	102	GND	Signal Ground	
8	CF	109	CD	Carrier Detect (Received line Signal Detector)	-->
9				unassigned	
10				unassigned	
11				unassigned	
12	SCF	122	SRR	Secondary Carrier Detect	-->
13	SCB	121	SCS	Secondary Clear to Send	-->
14	SBA	118	STX	Secondary Transmitted Data	<--
15	DB	114	TC	Transmit Signal Elements Timing (transmit clock)	-->
16	SBB	119	SRX(SRD)	Secondary Received Data	-->
17	DD	115	RC	Receiver Signal Element (Receive Clock)	-->
18				unassigned	
19	SCA	120	SRS	Secondary Request to Send	<--
20	CD	108.2	DTR	Data Terminal Ready	<--
21	CG	110	SQ	Signal Quality	-->
22	CE	125	RI	Ring Indicator	-->
23	CH/CI	111/112	DSR	CH=Data Signal Rate Selector, DTE	<--
				CI=Data Signal Rate Selector, DCE	-->
24	DA	113	XTC	Transmit Signal Element Timing (DTE source)	<--
25				unassigned HP 4925B Service	

C-17. TROUBLESHOOTING

Equipment

HP 1740A Oscilloscope
ET 11293
or use the configuration procedure below

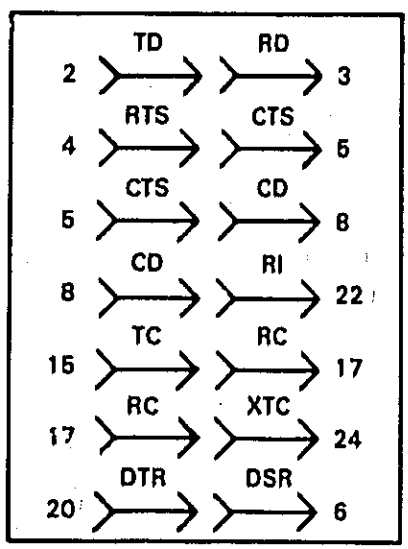
Configuration Procedure - If not using ET 11293

1. Loop the pins on the Breakout Box switch as shown in Table C-5.

NOTE

When the Breakout Box switches are set CLOSED,
the two sides of the Breakout Box header strip are connected together.

Table C-5. Breakout Box Switch Jumper Configuration



3. Connect pin 3 (RD) of the Breakout Box switch to the MARK/SPACE MONITOR.

Set Up

1. Follow the procedures in paragraph C-7 to remove the interface, if necessary refer to Section VIII of this manual for procedures to remove the HP 4925B.

2. All of the test points used in the procedure are located on Interface Board 18183-60001 (lower board).

Procedure

1. With the interface out of the case, turn on the HP 4925B.

2. Press TEST DURATION and select CONT.

3. Press BEGIN/END.

4. Use an Oscilloscope to verify the status of the lines given in Table C-6.

Table C-6. Troubleshooting Verification Table

LINE	TEST POINT	STATE
DTR	A4U701 pin 1	low (0 V)
DSR	A4U101 pin 1	low (0 V)
RTS	A4U701 pin 13	low (0 V)
CTS	A4U201 pin 2	low (0 V)
CD	A4U701 pin 14	low (0 V)
RI	A4U201 pin 1	low (0 V)
TD	A4U701 pin 2	toggling
RD	A4U501 pin 11	toggling
TC	A4U501 pin 3	toggling
RC	A4U501 pin 6	toggling
MARK	A4U201 pin 14	toggling
SPACE	A4U201 pin 13	toggling

5. Troubleshoot any lines that do not have the same reading as shown in Table C-6.

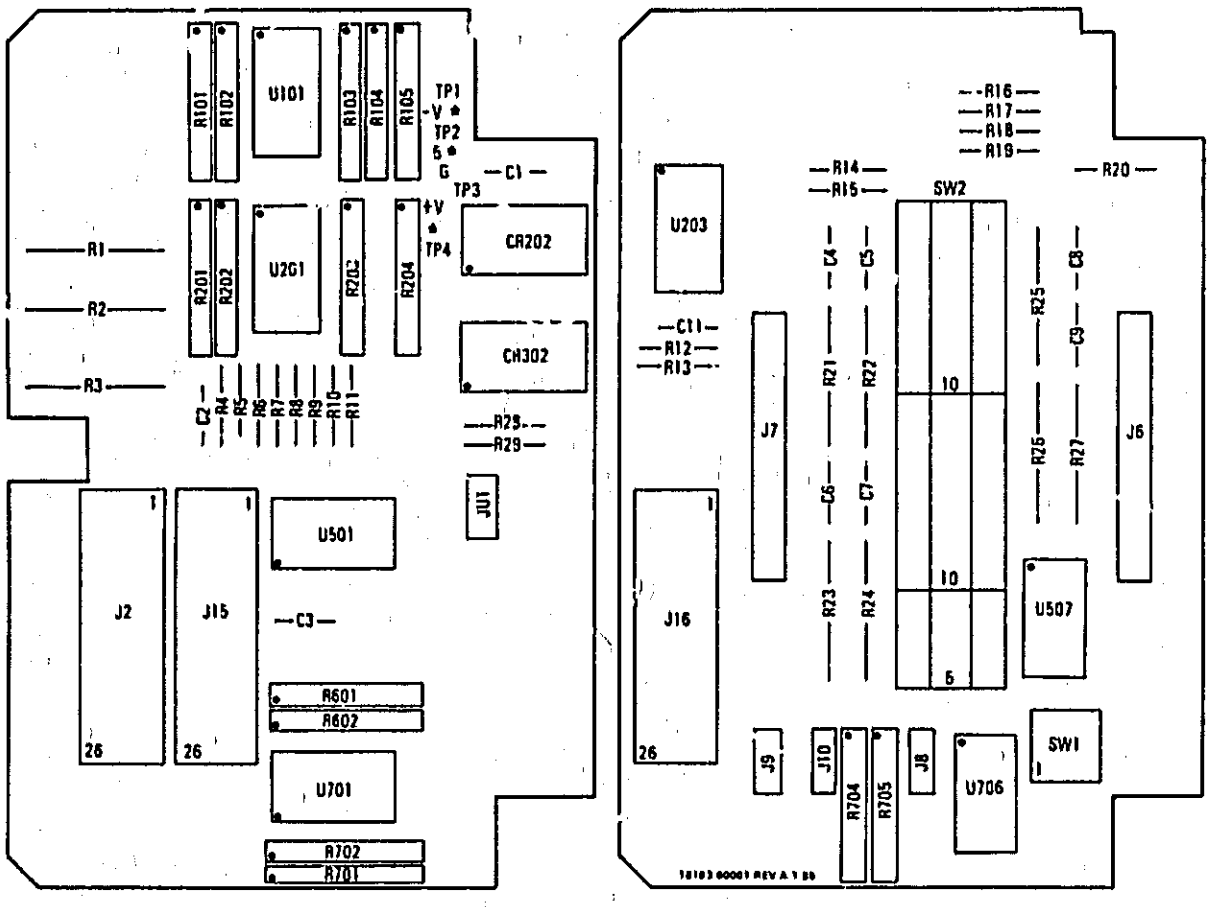
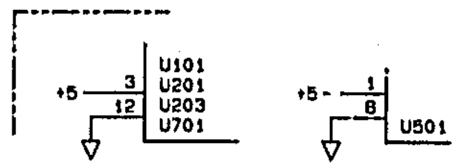
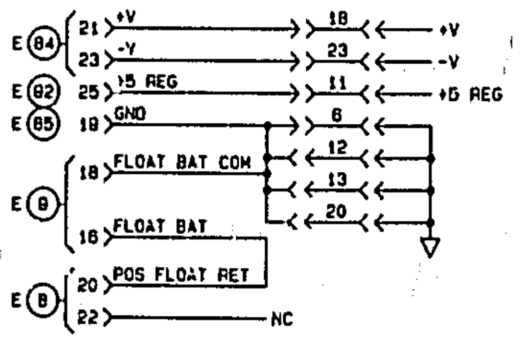


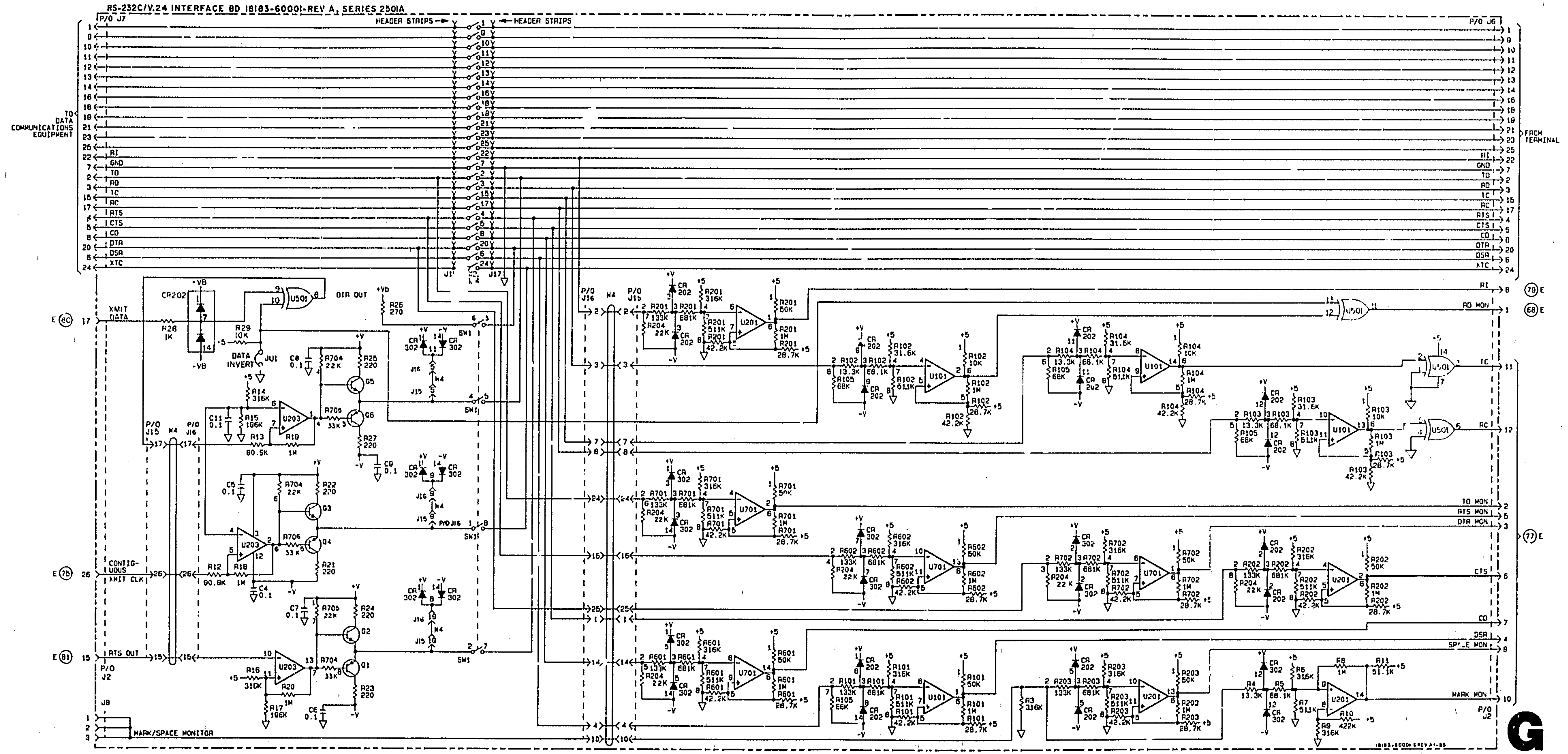
Figure C-5. HP 18183A Component Locator

Power and Grounds



Interconnections





G

Figure C-6. HP 18183A Schematic Diagram

APPENDIX D
HP 18184A
V.35 INTERFACE

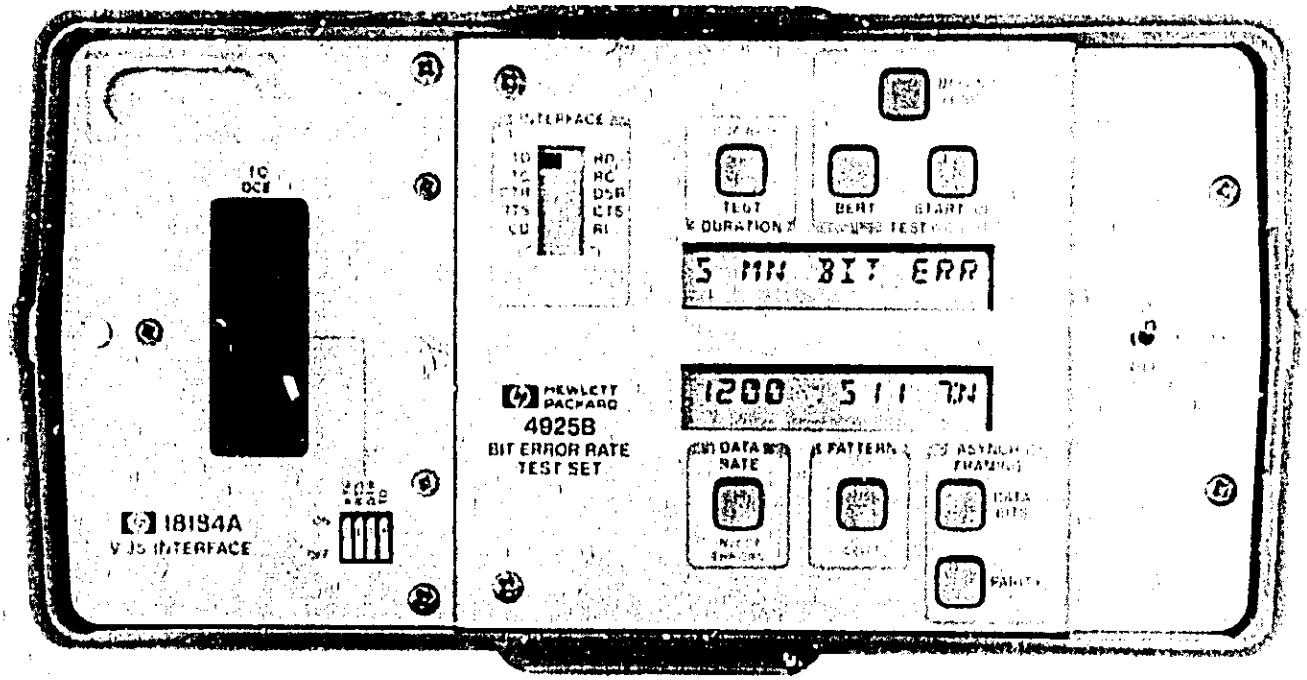


Figure D-1. HP 18184A Interface Pod

D-1. INTRODUCTION

The HP 18184A V.35 Interface provides high speed test capabilities for the HP 4925B Bit Error Rate Test Set. It is particularly important for Digital Data Service (DDS) testing.

This appendix includes information to install, operate, and service the HP 18184A.

D-2. DESCRIPTION

The V.35 Interface is configured to appear as a DTE for direct connection to a modem and is a pseudo balanced interface. The data and clock lines are balanced and operate a current mode. The control leads are single ended and referenced to a single common ground point. Typical operating speeds are 56K, 64K, and 72K bits/second.

D-3. SPECIFICATIONS

Table D-1. HP 18184A Specifications

Measurements	Operates up to 72K bits/sec
Power	May use batteries or AC Power Module (HP 18185A or HP 18194A)

NOTE

Due to the high power consumption of the V.35 interface, it will nominally run for only 15 minutes; therefore we recommend that you use the AC Power Module.

- Disconnect switches for TD, XTC, DTR, and TRS
- Balanced interface leads present a standard V.35 load
- Uses AC power supply (HP 18185A or HP 18194A)
- Control lead receivers have an input impedance of about 20K ohms
- Thresholds are TTL level compatible

D-4. INSTALLATION

This section provides information to install and provide power for the HP 18184A interface.

D-5. INITIAL INSPECTION. Inspect the interface for any physical damage sustained in transit. If the unit is received in a damaged condition, notify the nearest HP Sales and Service Office.

D-6. TAGGING FOR SERVICE. If the instrument is returned to Hewlett-Packard to service, complete one of the blue repair tags located in the back of this manual and attach it to the instrument. Follow the packaging instructions described in Section II of the HP 4925B Operating and Service Manual.

D-7. INSTALLATION PROCEDURE

The HP 18184A interface fits into the HP 4925B case. Follow the procedures below to install the interface.

1. Remove the interface currently in the HP 4925B (if necessary).
   a. Remove the screws securing the interface.
   b. Grasp the interface by the connectors and lift it out of the HP 4925B case.
   c. Disconnect the cable between the interface and the HP 4925B.

2. Install the Interface

   a. Connect the interface cable to J2 on the A3, Transmitter/Receiver Board.

   b. Place the interface into the HP 4925B case.

   c. Insert and tighten the three screws that hold the interface in the case.

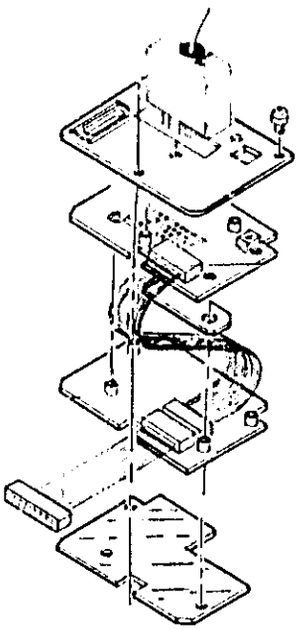


Figure D-2. Board Assembly Sequence

D-8. OPERATION

This section describes the front panel controls, indicators, and connectors, as well as operation of the HP 18184A Interface.

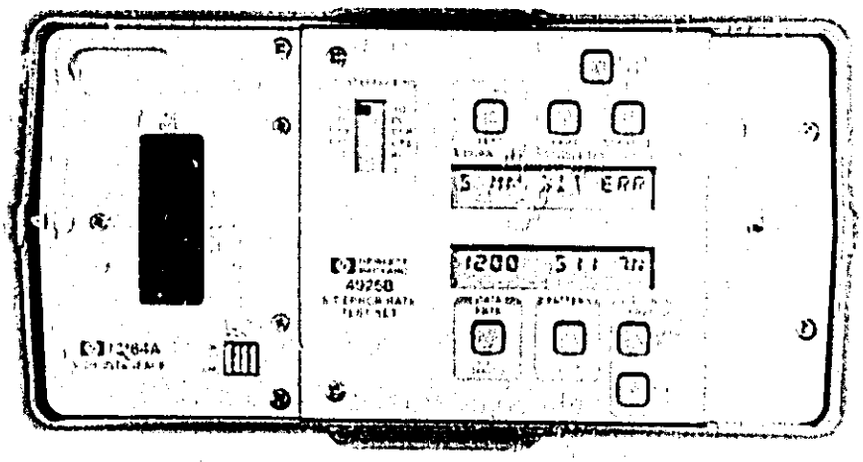


Figure D-3 HP 18184A Front Panel

XTC,RTS,DTR, TO, ON/OFF These switches interrupt the External Transmit clock (XTC), Request to Send (RTS), Data Terminal Ready (DTR), or Transmit Data (TD) drivers. The switches should be in the ON position for most testing. Turn the switch to OFF when the Bit Error Rate Test Set passively bridges a line.

TO DCE A V.35 connector which connects the Bit Error Rate Test set to the modem, terminal, or printer under test.

D-9. PERFORMANCE VERIFICATION

Performance Verification for the HP 18184A is performed simultaneously with the HP 4925B. A description of the tests is located in Section 4 of this manual.

D-10. ADJUSTMENTS

There are no adjustments for the HP 18184A.

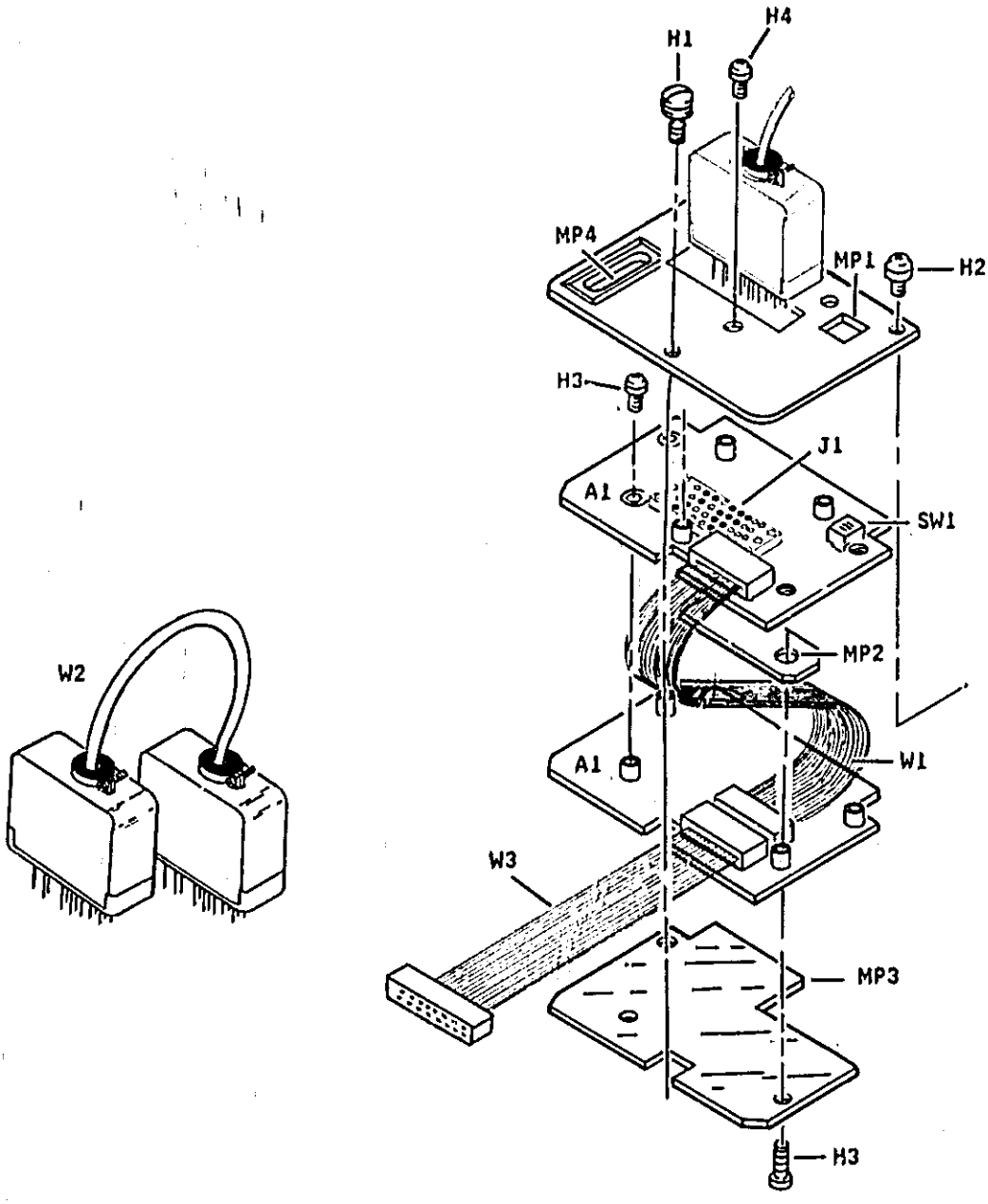
D-11. REPLACEABLE PARTS

The following tables and figure give information for ordering replacement parts. Table D-2 is the Manufacturer's Code List. Table D-3 lists the replaceable parts in alphanumeric order. Information is given for the Description, Quantity, HP Part Number, and Manufacturers Part Number. Chassis and mechanical parts are listed in Figure D-3. To order a listed part, quote the HP Part Number, indicate the quantity needed, and send the order to the nearest Hewlett-Packard office.

When ordering a part not listed, include the instrument model number, serial number, and a physical and functional description of the part. Send the order to the nearest Hewlett-Packard office.

Table D-2. Manufacturers Code List

Mfr No.	Manufacturer Name	Address	Zip Code
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN BRADLEY CO	MILWAUKEE WI	53204
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
11236	CTS OF BERNE INC	BERNE IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	
32293	INTERSIL INC	CUPERTINO CA	95014
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247



Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	18184-60001	5	1	V.35 INTERFACE BOARD	28480	18183-60001
H1	1390-0429	5	1	SCREW, CAPTIVE 6-32	03901	PS10-632.40
H2	2200-0193	8	2	SCREW,MACH,6-32 .25 IN,POZI	0000	ORDER BY DESCRIPTION
H3	2200-0592	8	7	SCREW,MACH,4-40 .188 IN	28480	2200 0592
H4	2200-0137	2	3	SCREW,MACH 4-40,188	28480	2200-0137
MP1	18184-00001	5	1	FRONT PANEL	28480	18184-00001
MP2	04925-20010	6	1	COVER PLATE	28480	04925-20010
MP3	5020-5262	6	1	PLASTIC SHIELD	28480	5020-5262
MP4	4040-2143	6	1	PANEL PLUG	28480	4040-2143
SW1	3101-2664	5	1	SWITCH, 4-POSITION DIP, ROCKER	05735	240004GB
W1	04925-61605	1	1	W1, CABLE	28480	04925-61605
W2	10388-61601	9	1	V.35 INTERFACE CABLE	28480	10388-61601
W3	04925-61602	9	1	W3, CABLE	28480	04925-61602

Figure D-4. HP 18184A Exploded View

Table D-3. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	018184-60001		1	V.35 INTERFACE BOARD	28480	18184-60001
A1C1	0160-0576	5	14	CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C2	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C3	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C4	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C5	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C6	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C7	0180-1746	5	1	CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
A1C8	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C9	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C10	0180-1746	5	1	CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
A1C11	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C12	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C13	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C14	0160-0576	5		CAPACITOR .1UF 20% 50V	02010	SR205C104MAA
A1C15	0180-1746	5	1	CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
A1CR101	1906-0074	1	1	DIODE ARRAY 50V MAX,	02237	FSA3157P
A1Q204	1826-0122	0	1	IC-VOLTAGE REGULATOR +4.8/5.2V	01406	LM340T-5
A1Q504	1826-0284	7	1	IC-VOLTAGE REGULATOR +4.8/5.2V TO 220 PKG	02037	MC7905CT
A2R1	0757-0280	3	3	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A2R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R3	0698-3446	3	4	RESISTOR 383 OHM .1% .125W	03292	CT4-1/8-TO-383R-F
A1R4	0757-0317	7	4	RESISTOR 1.33K 1% .125W	03292	CT4-1/8-TO-1331-F
A1R5	0757-0317	7		RESISTOR 1.33K 1% .125W	03292	CT4-1/8-TO-1331-F
A1R8	0757-0403	2	5	RESISTOR 121 1% .125W	03292	CT4-1/8-TO-121R-F
A2R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R8	0698-3446	3		RESISTOR 383 OHM .1% .125W	03292	CT4-1/8-TO-383R-F
A1R9	0757-0317	7		RESISTOR 1.33K 1% .125W	03292	CT4-1/8-TO-1331-F
A1R10	0698-3446	3		RESISTOR 383 OHM .1% .125W	03292	CT4-1/8-TO-383R-F
A1R11	0757-0317	7		RESISTOR 1.33K 1% .125W	03292	CT4-1/8-TO-1331-F
A1R12	0698-3446	3		RESISTOR 383 OHM .1% .125W	03292	CT4-1/8-TO-383R-F
A1R13	0757-0403	2		RESISTOR 121 1% .125W	03292	CT4-1/8-TO-121R-F
A1R14	0757-0407	6	7	RESISTOR 200 OHM 1% .125W	03292	CT4-1/8-TO-201-F
A1R15	0757-0465	6	5	RESISTOR 100K 1% .125W	03292	CT4-1/8-TO-1003-F
A1R16	0757-0442	9	5	RESISTOR 10K 1% .125W	03292	CT4-1/8-TO-1002-F
A1R17	0757-0442	9		RESISTOR 10K 1% .125W	03292	CT4-1/8-TO-1002-F
A1R18	0757-0442	9		RESISTOR 10K 1% .125W	03292	CT4-1/8-TO-1002-F
A1R19	0757-0442	9		RESISTOR 10K 1% .125W	03292	CT4-1/8-TO-1002-F
A1R20	0757-0465	6		RESISTOR 100K 1% .125W	03292	CT4-1/8-TO-1003-F
A1R21	0757-0403	2		RESISTOR 121 1% .125W	03292	CT4-1/8-TO-121R-F
A1R22	0757-0407	6	7	RESISTOR 200 OHM 1% .125W	03292	CT4-1/8-TO-201-F
A1R23	0757-0407	6	7	RESISTOR 200 OHM 1% .125W	03292	CT4-1/8-TO-201-F
A1R24	0757-0465	6		RESISTOR 100K 1% .125W	03292	CT4-1/8-TO-1003-F
A1R25	0757-0403	2		RESISTOR 121 1% .125W	03292	CT4-1/8-TO-121R-F
A1R26	0757-0407	6	7	RESISTOR 200 OHM 1% .125W	03292	CT4-1/8-TO-201-F
A1R27	0757-0407	6	7	RESISTOR 200 OHM 1% .125W	03292	CT4-1/8-TO-201-F
A1R28	0757-0465	6		RESISTOR 100K 1% .125W	03292	CT4-1/8-TO-1003-F
A1R29	0757-0403	2		RESISTOR 121 1% .125W	03292	CT4-1/8-TO-121R-F
A1R30	0757-0407	6	7	RESISTOR 200 OHM 1% .125W	03292	CT4-1/8-TO-201-F
A1R31	0757-0407	6	7	RESISTOR 200 OHM 1% .125W	03292	CT4-1/8-TO-201-F
A1R32	0757-0465	6		RESISTOR 100K 1% .125W	03292	CT4-1/8-TO-1003-F
A1R33	0757-0442	9		RESISTOR 10K 1% .125W	03292	CT4-1/8-TO-1002-F
A1R34	0699-1084	3	1	RESISTOR 270 5% 2W	02499	GS-3
A1R200	1810-0637	9	6	RESISTOR NETWORK, CUSTOM	28480	1810-0637
A1R201	1810-0637	9		RESISTOR NETWORK, CUSTOM	28480	1810-0637
A1R202	1810-0637	9		RESISTOR NETWORK, CUSTOM	28480	1810-0637
A1R203	1810-0637	9		RESISTOR NETWORK, CUSTOM	28480	1810-0637
A1R402	1810-0637	9		RESISTOR NETWORK, CUSTOM	28480	1810-0637
A1R403	1810-0637	9		RESISTOR NETWORK, CUSTOM	28480	1810-0637
A1R502	1810-0767	6	2	RESISTOR NETWORK 22.0K X 7	05524	CSC08A01-223G
A1R703	1810-075	7	1	RESISTOR NETWORK 100 X 7	05524	CSC08A01-101G
A1R704	1810-0767	6		RESISTOR NETWORK 22.0K X 7	05524	CSC08A01-223G
A1SW1	3101-2664	3	1	SWITCH-PKR DIP-PKR-ASSY, 4-1A	05735	240004GB
A1U202	1820-1826	1	1	IC GATE	28480	1820-1826
A1U300	1826-0759	9	2	IC-COMPARATOR QUAD	03406	LM339J
A1U301	1826-0759	9		IC-COMPARATOR QUAD	03406	LM339J
A1U302	1820-3297	4	1	IC-DRIVE OCTL BUS, CMOS	02037	MC74HC244N
A1U601	1826-0915	9	1	IC-OPAMP, LOW BIAS, HIGH IMP	02037	MC34001BU
A1U703	1826-0792	0	1	IC-COMPARATOR QUAD	03799	HA1-4905-5
A1XDS1	1200-0868	6	14	SOCKET STRP 7-CONT DIP-SOLDR	28480	120J-0868

D-12. SERVICE

The following sections contains service information for the HP 18184A. Included is the Theory of Operation, V.35 Signal Mnemonics, Troubleshooting, Component Locators, and Schematics.

D-13. THEORY OF OPERATION

The V.35 interface for the HP 4925B is configured to appear as a DTE. There are four transmitters, two balanced and two single ended. The interface monitors ten lines, four are balanced and the rest are single ended.

V.35 is a pseudo balanced interface. Not all lines operate in a balanced manner. Data and clock lines are balanced but the control leads are single ended and referenced to a single common ground point. The balanced lines operate in current mode rather than in voltage mode as with the RS-232C. The line drivers are current sinks rather than voltage sources. V.35 specifies the input and output impedances of the balanced lines. The sources have a nominal output impedance of 100 ohms. The transmission cable impedance measured at 100K Hz must be 100 ohms and resistive. The balanced receivers have a nominal input impedance of 100 ohms. This makes a 100 ohm balanced transmission line. The unbalanced control leads have thresholds, voltage levels, input and output impedances exactly the same as RS-232C. Table D-4 describes the lines used in the HP 18184A.

Table D-4. V.35 Interface Lines

Interface Lead	Type	How Used by HP 18184A
TD (SD)	balanced	driven/monitored
RD (RD)	balanced	monitored
TC (SCT)	balanced	monitored
RC (SCR)	balanced	monitored
XTC (SCTE)	balanced	driven
RTS	single	driven/monitored
CTS	single	monitored
DTR	single	driven/monitored
DSR	single	monitored
DD	single	monitored
RI	single	monitored

D-14. RECEIVERS. The balanced receivers have an impedance matching network at the inputs with the following chacteristics:

Input impedance	100 +-10 ohms
Resistance to signal ground	150 +-15 ohms

The input impedance for the single ended receivers is about 18K, the thresholds are set to +2.5 for a space and +0.25 for a mark. The receivers also include protection diodes for signals up to 50 VDC.

D-15. TRANSMITTERS. The balanced transmitters have a current sink line driver and resistor network with the following characteristics:

Source impedance	100 +-10 ohms
Resistance between short-circuited terminals and ground	150 +-15 ohms
Open circuit voltage	1.1 to 2.5 volts
Common mode voltage	<0.6 volts

Single ended transmitter RTS is implemented with an op amp and a current limiting resistor. The single ended transmitter DTR has a 270 ohm resistor to the +12 V supply.

Each transmitter can be disabled by means of a DIP switch on the front panel. Balanced drivers are prevented from sinking current and are not physically disconnected from the line. The associated resistor network is on-line and has an offset voltage of about 3.88 VDC. The signal ended transmitters are actually disconnected from the line.

The inputs of the balanced transmitters and the outputs of the balanced receivers are buffered to insure fast rise times when operating at high data rates.

D-16. POWER DISTRIBUTION

Local regulators on the V.35 interface take the switched +-12 V power from the HP 4925B and produce +-5 VDC to supply the upper interface board. The +5 V regulator supplies the drivers and op amps exclusively. All of the parts on the lower interface board use +5 V supplied by the HP 4925B.

D-17. TROUBLESHOOTING

Equipment

ET 25113
HP 1740A Oscilloscope
HP 3466A Multimeter

Set Up

1. Follow the procedures in paragraph D-7 to remove the interface, if necessary refer to Section VIII of this manual for procedures to remove the HP 4925B.

2. Attach ET 25113 to the V.35 connector on the HP 18184A interface.

NOTE

Figure 6-2 describes ET 25113 and its connections.

Procedure

1. Turn on the HP 4925B

2. Press TEST DURATION and select CONT.

3. Press BEGIN/END.

4. All of the test points used in this procedure are located on the interface Board 18184-60001.

5. Use a Multimeter to check Q204 and Q504.

Transistor	Voltage
Q204	+5 V
Q504	-5 V

6. Use an Oscilloscope and check the signal and monitor lines in Table D-5.

Table D-5. Troubleshooting Verification Table

Line	Test Point	State
DTR	U300 pin 14	low (0 V)
DSR	U301 pin 1	low (0 V)
RTS	U300 pin 13	low (0 V)
CTS	U301 pin 2	low (0 V)
CD	U301 pin 14	low (0 V)
RI	U301 pin 13	low (0 V)
TD	U302 pin 5	toggling
RD	U302 pin 7	toggling
TC	U302 pin 14	toggling
RC	U302 pin 9	toggling

7. Troubleshoot any lines that do not have the same reading as shown in Table D-5.

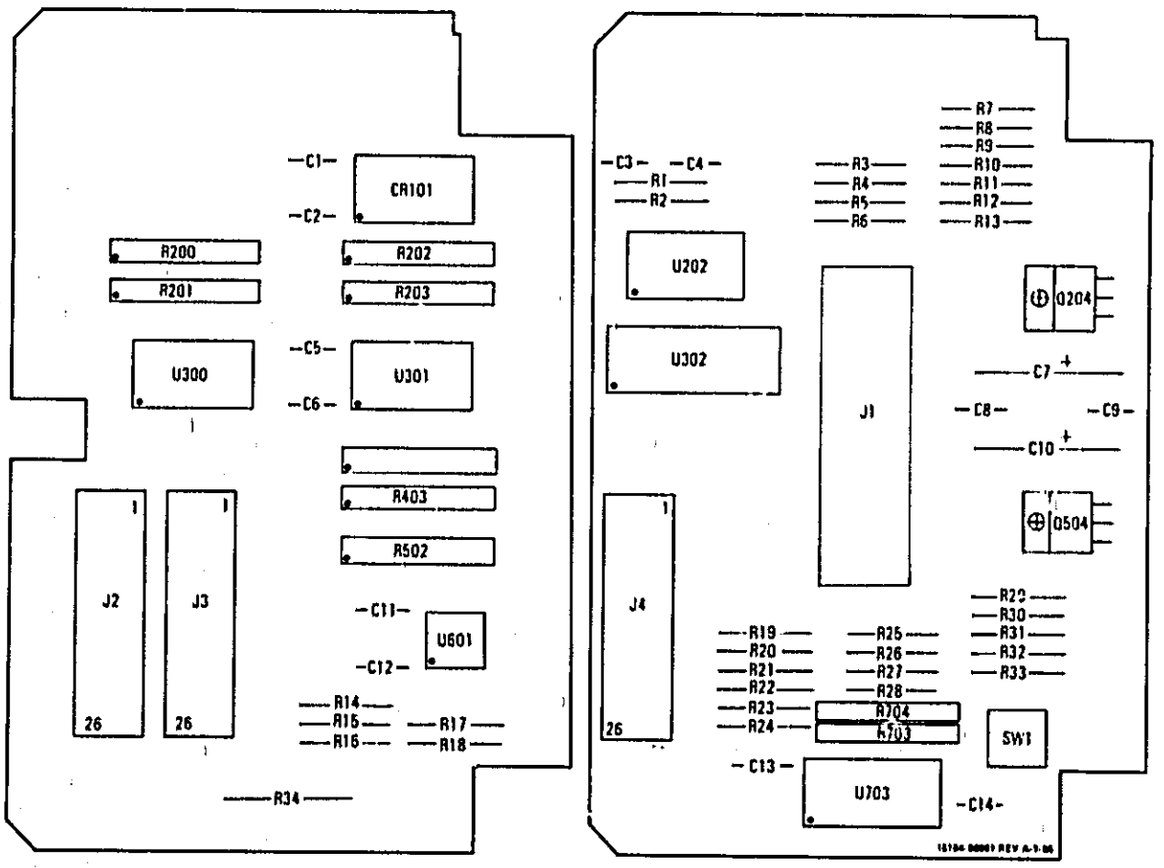


Figure D-5. HP 16184A Component Locator

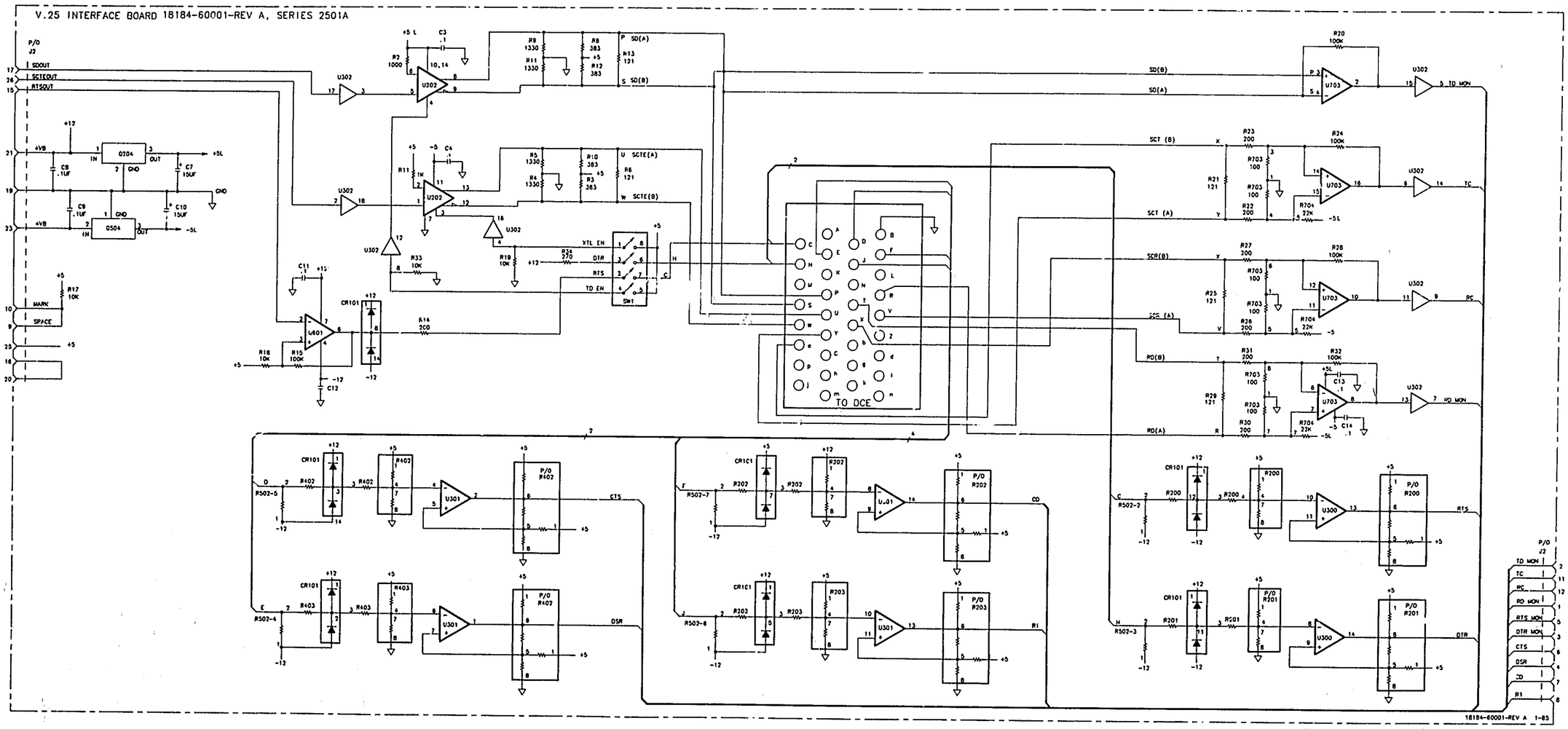


Figure D-6.
HP 18184A Schematic Diagram

APPENDIX E
HP 18185A
AC POWER MODULE

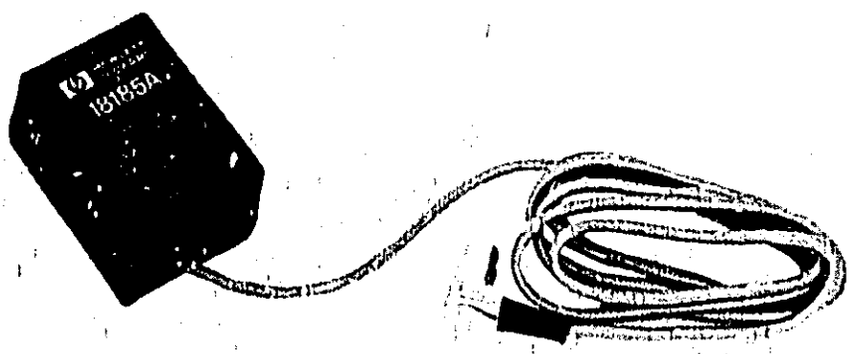


Figure E-1. HP 18185A AC Power Module

E-1. INTRODUCTION

The HP 18185A AC Power Module is the primary power source for the HP 18184A V.35 Interface. This appendix includes information to install and operate the HP 18185A.

E-2. DESCRIPTION

This AC Power Module will supply continuous power to the HP 4925B as opposed to the 9 volt batteries which have a nominal runtime of only 15 minutes (for the V.35 Interface). It is specifically designed for use in North America.

The AC Power Module can also supply power for the HP 18183A, RS-232C/V.24 Interface. Applications include bench top, rack mount or long term testing.

E-3. SPECIFICATIONS

Table E-1. HP 18185A Specifications

* Input voltage:	90-130 V, 50-60 Hz
* Output voltage:	+/-12 VDC, 200 mA
* 5% line/load regulation	
* For use in North America and Japan only	
* Regulated Power Supply	
* 10 mV RMS max ripple	
* Thermally protected	

E-4. INSTALLATION

This section provides information to install the HP 18185A AC Power Module.

CAUTION

The HP 18185A is intended to be used only with the HP 4925B.
Plugging anything else to the HP 4925B or the HP 18185A may cause equipment damage

E-5. INITIAL INSPECTION. Inspect the AC Power Module for any physical damage sustained in transit. If the unit is received in a damaged condition, notify the nearest HP Sales and Service Office.

E-6. SERVICE. The HP 18185A is non-repairable. If the unit is returned to Hewlett-Packard for any reason, complete one of the blue repair tags located in the back of this manual and attach it to the instrument. Follow the packaging instructions described in Section II of the HP 4925B Operating and Service Manual.

E-7. INSTALLATION PROCEDURE

The HP 18185A AC Power Module plugs into the HP 4925B case. The jack on the HP 18185A has three prongs. Turn off the HP 4925B line switch. Line up these prongs with the connector holes in the HP 4925B and insert.

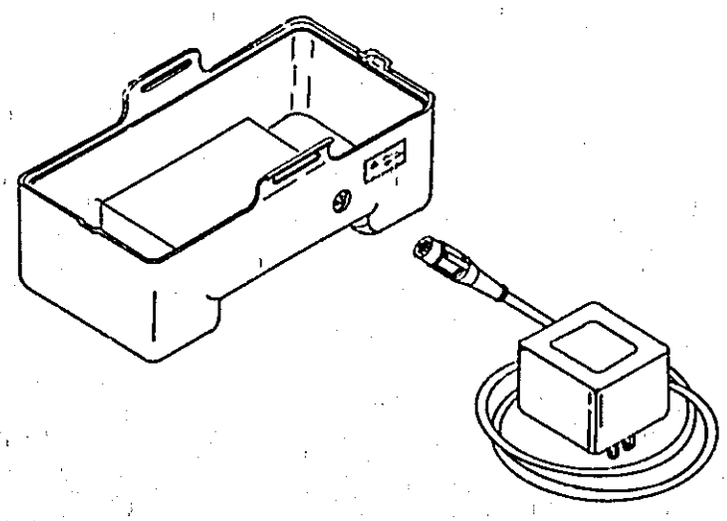


Figure E-2. Connect the HP 18185A to the HP 4925B

E-8. REPLACEABLE PARTS

Figure E-3 is an illustration of the AC Power Module and Table E-2 lists the replaceable parts.

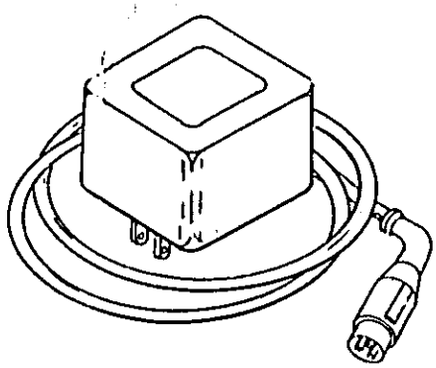


Figure E-3. HP 18185A AC Power Module

Table E-2. HP 18185A Replaceable Parts

HP Part No	CD	QTY	Description	MFR Code	MFR No
0950-1735	5	1	AC Power Module	28480	0950-1735

APPENDIX F
HP18191A
RACK MOUNT KIT

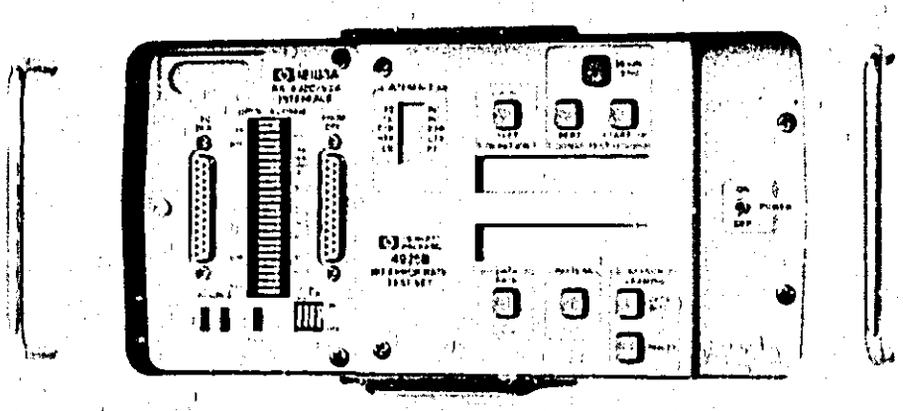


Figure F-1. HP 18191A Rack Mount Kit

F-1. INTRODUCTION

The HP 18191A is a rack mount kit for the HP 4925B. It converts the HP 4925B into a rack mounted instrument.

F-2. INSTALLATION

1. Secure the handles to the front panel with the lock nuts.
2. Hold the HP 4925B face forward with the AC power socket on top. Slide the HP 4925B into the front panel.
3. Place the bracket over the back of the HP 4925B and onto the threaded posts on the front panel. Secure the HP 4925B to the front panel with lock washers.

F-3. REPLACEABLE PARTS

Figure F-2 is an exploded view of the Rack Mount Kit and Table F-1 lists the replaceable parts.

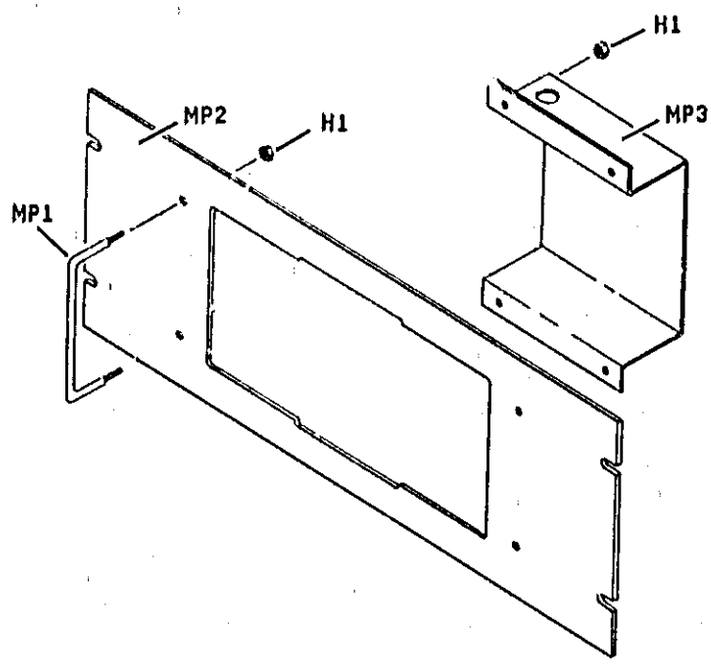


Figure F-2. HP 18191A Exploded View

Table F-1. HP 18191A Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
H1	2580-0003	5	8	NUT, HEX 8-32	00000	ORDER BY DESCRIPTION
MP1	1440-0134	6	2	HANDLE-SST 4.25-LG	02170	10734-55-0832-7
MP2	04925-00003	5	1	ADAPTER FRAME	28480	04925-00003
MP3	18191-00001	4	1	RACK MOUNT HOLDER	28480	18191-00001

APPENDIX G
HP 18194A
AC POWER MODULE

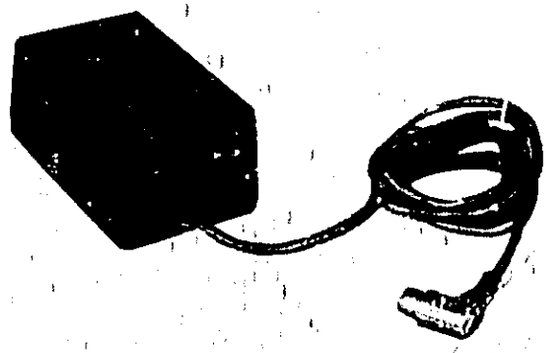


Figure G-1. HP 18194A AC Power Module

G-1. INTRODUCTION

The HP 18194A AC Power Module is the primary power source for the HP 18184A V.35 Interface. This appendix includes information to install and operate the HP 18194A.

G-2. DESCRIPTION

This AC Power Module will supply continuous power to the HP 4925B as opposed to the 9 volt batteries which have a nominal runtime of only 15 minutes (for the V.35 interface). It is specifically designed for use in countries where the primary power is 175 to 270 VAC, 47-67 Hz.

The AC Power Module can also supply power for the HP 18183A, RS-232C/V.24 Interface. Applications include bench top, rack mount or long term testing.