HP 69720A

Voltage Converter Card

In Stock

New From Surplus Stock

Open Web Page

https://www.artisantg.com/86076-1

Section IV
THEORY OF OPERATION

4-1 INTRODUCTION

4-2 This section explains the theory of operation for the 69720A and 69721A D/A cards. The theory is written with the assumption that the reader is familiar with the instructions set and the basic operation of the 6942A Multiprogrammer. First, a brief description is given covering the basic operation and features of the D/A cards. A detailed block diagram discussion covering both cards follows. This selection concludes with an example of the processing of an Output Sequential instruction.

4-3 OVERALL OPERATION

4-4 Power Turn-On

4-5 When power is applied to the D/A Card, the circuits on the card are cleared. A self-test is then initiated by the Multiprogrammer to test part of the circuits of the D/A card. The self-ID, data type, size, and LSB parameters of the card are read and stored in Multiprogrammer memory as part of the wake-up sequence. Card Enable (CEN) holds the card output at zero until the first cycling operation (see paragraph 4-8).

4-6 First Rank Storage

4-7 When the D/A card is addressed in any output type instruction (OP, OS, OB, OI, WC, or WF), a 16-bit data word is sent to the card and is stored in a register called first rank storage. The data word in first rank storage can be read at any time with a Read Value (RV) instruction. If a WF output instruction were issued at the controller, this instruction would be completed with the loading of first rank storage. For any other output instruction, a "cycle" operation (described in the next paragraph) automatically begins after the data word is loaded into first rank storage.

4-8 Cycling the Card

4-9 In a cycle operation, the 12 LSB's of the data word in first rank storage are transferred to a second register called second rank storage. Immediately after this transfer, several events take place simultaneously as part of the cycling operation:

a. A CARD ENABLE (CEN) signal goes high (if not already high from a previous cycle) and allows the data word in second rank storage to be transferred to the Digital to Analog Converter (DAC) so that it can produce an analog output. The MSB (bit 11) of this word is inverted to supply the DAC module with a data word compatible with its internal format. The output will remain at the programmed level until: (1) the card is re-programmed, (2) a power up reset occurs, (3) A System Disable (SD) instruction is issued, or (4) the External Enable (EEN) line at the external edge connector is made low.

b. The BUSY (BSY) signal goes high and is sent to the external edge connector. This signal indicates that the data word is currently selecting the analog output.

c. A 6 μs timer begins running.

4-10 As mentioned previously, a cycle operation occurs automatically for all output instructions except a WF instruction. When a WF instruction is issued, the cycle operation is normally initiated in one of two ways (see Figure 4-1):

1. By the controller issuing a Cycle (CY) instruction to specifically cycle the card, or
2. Externally at the external interface connector by applying an EXTERNAL TRIGGER signal. When an External Trigger is applied, an additional signal called TRIGGER POLARITY SELECT determines whether cycling will occur on the low-to-high or high-to-low transition of the EXTERNAL TRIGGER pulse. More information on external triggering can be found in Section III under "External Trigger Switch".

4-11 End-of-Process

4-12 An End-of-Process (EOP) signal is generated when the 6μsec timer times out. The EOP signal is sent to the external interface connector and is also used to generate a Multiprogrammer interrupt request.

4-13 Interrupt Request

4-14 When the End-of-Process (EOP) signal occurs and the card is armed, an Interrupt Request ($\overline{IRQ}$) is returned to the Multiprogrammer to indicate the completion of the output operation. OB, OI, OP, and OS output instructions arm the card when the first rank storage register is loaded. For WF, WC and CY instructions, the card must be armed before an interrupt can be generated. This can be done with a separate Arm Card (AC) instruction issued at the controller. After a program interrupt request is made, the Multiprogrammer will respond by disarming the card, clearing EOP and the group address flag (GAFF).

4-15 The GAFF flag is internal to the Universal Control Chip on the card and is set by instructions, such as; WC, OI, OP, to allow multiple cards to be cycled in parallel. Refer to Chapter 4 in the 6942A Multiprogrammer User's Guide for more information on cycling cards in parallel.

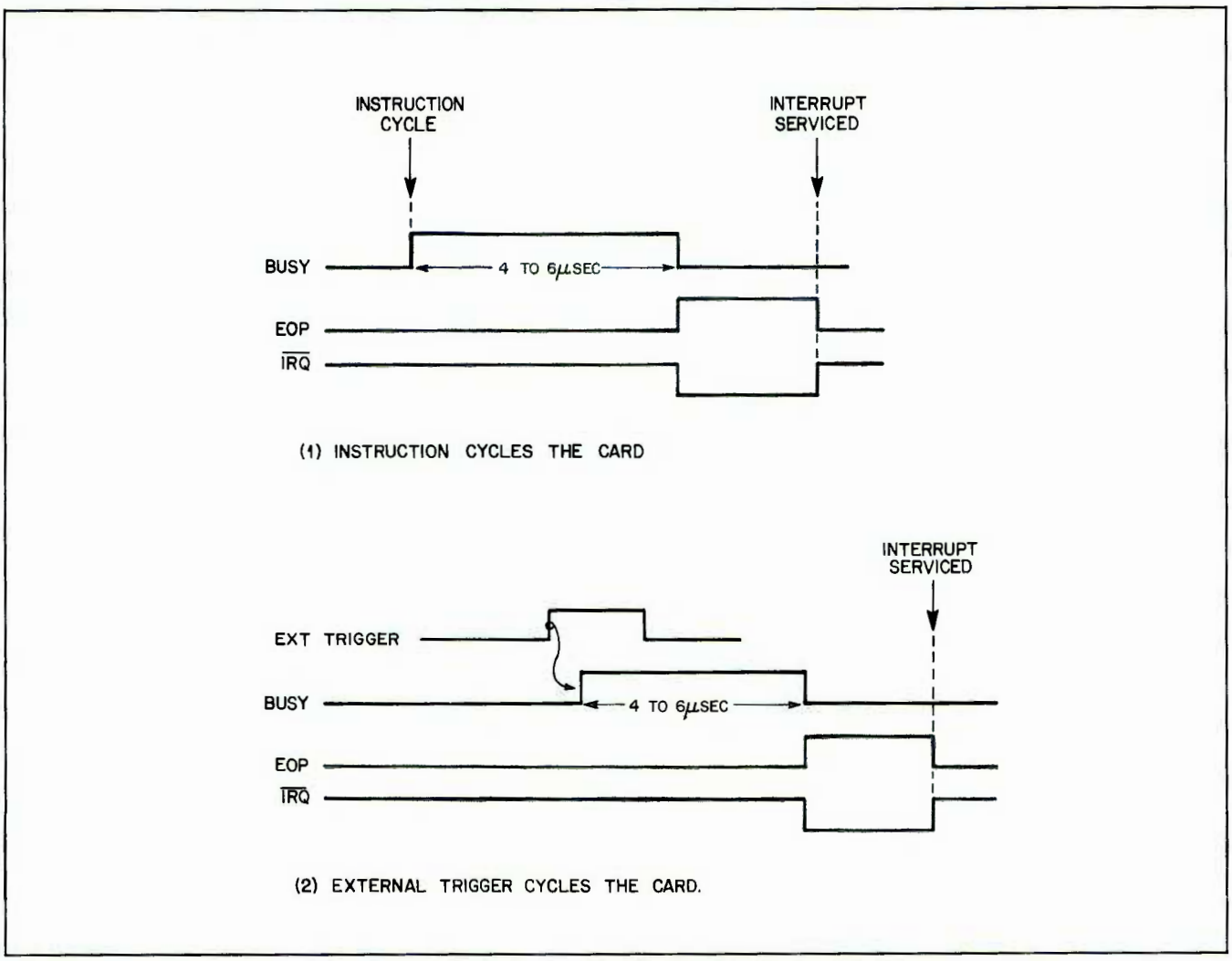


Figure 4-1. Card Cycling and Busy/EOP Timing

4-16 Output Quick-Disconnect

4-17 This feature permits either the controller or the customer interface logic to force the DAC output to zero. The controller can do this by issuing a System Disable (SD) instruction. The external interface logic can do this by making the External Enable signal low. If the controller issues an SE instruction and the EXTERNAL ENABLE signal is high, the DAC output will return to the level which was present prior to issuing SD or making EEN low.

4-18 Self-ID/Status Word

4-19 When the Multiprogrammer performs a self test, or when the controller issues a Read Status (RS) instruction, the D/A card returns a 16-bit status word to the Multiprogrammer. This word contains information on the operational status of the card and shows how the card is hardware configured. The status word is discussed in more detail in the detailed block diagram discussion.

4-20 DETAILED BLOCK DIAGRAM DISCUSSION

4-21 Figure 4-2 is a block diagram of both the 69720A and the 69721A. The voltage-to-current converter circuit applies only to model 69721A D/A cards. The D/A card consists of the following functional circuits:

a. Universal Control Chip (UCC).
b. Tri-state bidirectional data transceivers.
c. First rank storage register.
d. Data multiplexer
e. Data isolators.
f. Second rank storage register.
g. Output enable gates.
h. D/A converter.
i. Voltage to current converter (69721A only)
j. Six-μsec Timer.
k. First rank return buffers.
l. Self-ID/Status return buffers.

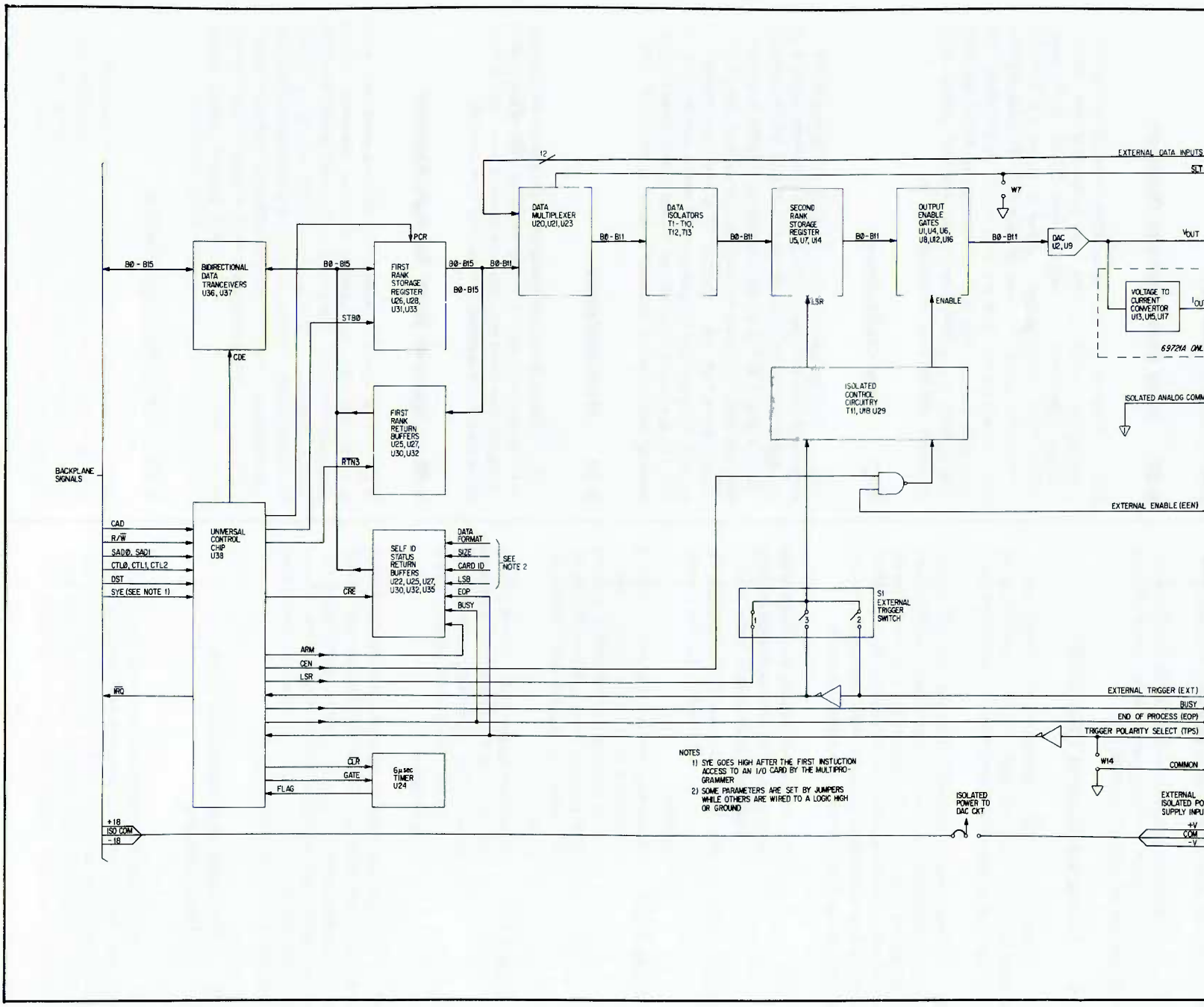


Figure 4-2. D/A Output Card, Detailed Block Diagram

4-22 When the D/A Output card is installed in a slot position in the Multiprogrammer, 6942A, or in the Extender chassis, 6943A, the card is assigned the address of that slot position. Once installed, the card connects to the data lines (B0-B15), the control lines, and to the power input lines of the backplane.

4-23 The following paragraphs describe the functional circuits shown in Figure 4-2. The functional schematic in Section VII should also be used as reference

4-24 Universal Control Chip (UCC)

4-25 Control chip (U38) supervises all the operations taking place on the D/A Output card. The UCC establishes the timing sequence for the various control signals used on the card.

4-26 When power is applied to the card, the PCR control signal goes high and clears all control circuits and first rank register on the card. The card is then ready to process any instruction issued at the controller that addresses the card. When an output type instruction is issued, the following input control lines set up the UCC for a particular operation:

CAD - This is the card address line which goes high to select the D/A card when the card is addressed in an output instruction.

R/$\overline{W}$ - This is the read/write line. It is high for a read operation and is low for a write operation.

SAD0, SAD1 - These two lines are decoded to select a subaddress on the card during a read or a write operation. For example, during a write to subaddress 0, binary 00 is sent; for a read from subaddress 3, binary 11 is sent.

CTL0, CTL1, CTL2 - These lines supply a 3-bit control code to the UCC to indicate what operation is to be performed. Depending on the instruction issued, one or more codes are sent in succession.

4-27 The data values on the above control lines are loaded into the UCC when a DATA STROBE (DST) pulse occurs. This data is then decoded to produce the various control signal outputs required for the indicated operation. A description of these control signals as they relate to the function being performed is included in the following paragraphs.

4-28 Tri-State Bidirectional Data Transceivers

4-29 The tri-state bidirectional tranceivers control the direction of data flow to and from the card over the B0-B15 data lines. During a write operation, CARD DRIVER ENABLE (CDE) is low and the B0-B15 data lines are connected to the input of the first rank storage register. During a read operation, CDE goes high and the B0-B15 data lines are connected to the output of the first rank return buffer and to the output of the self-ID/status return buffer. Although the transceivers are tri-state logic, jumper W21 establishes pin 19 at ground so that the open state condition is never used.

4-30 First Rank Storage Register

4-31 When any output instruction is executed, a data word is placed on the B0-B15 data lines to the first rank storage register. Subaddress 0 is decoded from SAD0, SAD1 lines; CTL0, CTL1, and CTL2 are decoded to produce a STROBE ZERO (STB0) pulse. The leading edge of STB0 loads the first rank storage register with the data on the B0-B15 lines. The data word stored in first rank storage can be read at any time with a Read Value (RV) instruction. The first rank storage register is cleared only on power turn on.

4-32 Data Multiplexers

4-33 The digital data word to the DAC can be supplied from either first rank storage or the J2 edge connector (pins A to N), depending on the state of the EXTERNAL DATA SELECT ($\overline{SLT}$) input. If $\overline{SLT}$ is a logic low level or shorted to ground, the data word furnished to the DAC will be from the J2 connector; if it is high, bits 0 through 11 of first rank storage will be used. External data may also be selected by installing jumper W7. For the card to function over its full bipolar output range, external data must be supplied in two's complement form.

4-34 Data Isolators

4-35 This bank of pulse transformers isolates the analog output circuitry from the +5 V data common. When the card is cycled the data word from the multiplexer is transferred across the isolators and latched into second rank storage.

4-36 Second Rank Storage Register

4-37 This register is loaded with the data word only when a cycle operation is initiated. A cycle operation occurs automatically as part of any output instruction except for a WF output instruction. Shortly after STB0 occurs, a LOAD SECOND RANK (LSR) strobe pulse is produced to begin the cycle sequence. The LSR signal is transferred through a pulse transformer and its leading edge loads the second rank storage register. For information on how the external trigger switch (S1) affects the cycling of the card, refer to Section III.

4-38 Output Enable Gates

4-39 These gates have two purposes: first, they prevent the data word from reaching the DAC until the programmed data word is loaded into second rank storage. Second, they can disconnect the data lines to the DAC (thus forcing it's output

to zero) when either the EXTERNAL ENABLE (EEN) signal or the CARD ENABLE (CEN) signal goes low. CEN goes high after the first LSR pulse occurs and remains true until either a System Disable (SD) instruction is issued or a power reset occurs. The D/A output returns to the value stored in the second rank register when both CEN and EEN return high.

4-40 Voltage DAC

4-41 The voltage DAC takes the digital word from second rank storage and converts it into a proportional output voltage. The voltage DAC consists of a 12-bit D/A converter module U2 and an associated operational amplifier U9 (see Figure 7-2.) The 24 pin D/A module provides an output current which is proportional to the digital word at its input. The operational amplifier is used as a current-to-voltage converter. The current from the D/A module drives the summing junction of the operational amplifier to produce a bipolar output voltage at J2-W within the range of −10.24 V to +10.235 V. Voltage gain adjustments may be made with potentiometer R4; R10 is used to adjust voltage offset. Refer to Section V for calibration procedures.

4-42 Voltage-to-Current Circuit (69721A only)

4-43 This circuit (refer to Figures 4-3 and 7-2) supplies a constant output current that is proportional to the input voltage at U9 pin 6. The circuit monitors the output current by sensing the voltage drop (Vb-Vc) across R23. If the output current attempts to change, U17 and U13 will immediately detect this change and generate a correction voltage (Vd) which causes U15 to drive the power amplifier (Q1 and Q2) in such a way as to "pump" more or less current to the output as needed.

4-44 The effective resistance of R23 can be changed by adjusting R15, thereby altering the gain of the entire converter circuit. Since the buffer Amplifier (U13) has unity voltage gain and a high input impedance, it does not draw significant current through sense resistor R23. Offsets for the entire circuit may be nullified by adjusting R17. The differential amplifier (U17) produces an inverted output voltage (Vd) which is five times the voltage across the sense resistance. Since the inverting input of U15 is essentially at ground potential, the non-inverting input must be essentially at ground potential also. Given that no current can flow into the input of an ideal amplifier, the ground potential at the non-inverting input of U15 is maintained as long a $I_{in} = I_{fdbk}$.

4-45 6-Microsecond Timer

4-46 The 6 μsec timer begins running when a cycle operation is initiated. The output of the timer goes low when GATE is generated by the UCC and returns to a logic high 6 μs later. This low-to-high transition sets the END-OF-PROCESS (EOP) output and resets the BUSY output. EOP going high indicates that the analog output has stabilized and the instruction has completed.

4-47 First Rank Return Buffers

4-48 These buffers are used to place the contents of the first rank storage register on the B0-B15 data lines. When a Read Value (RV) instruction is issued, subaddress 3 is decoded from the SAD0, SAD1 lines and this information along with CTL0, CTL1, CTL2 and the R/ $\overline{W}$ line produce a low $\overline{\text{RETURN 3}}$ (RTN3) logic level. This control signal enables the tri-state output of the first rank return buffers. CDE is also high and the data word in first rank storage is sent to the Multiprogrammer via the first rank return buffers.

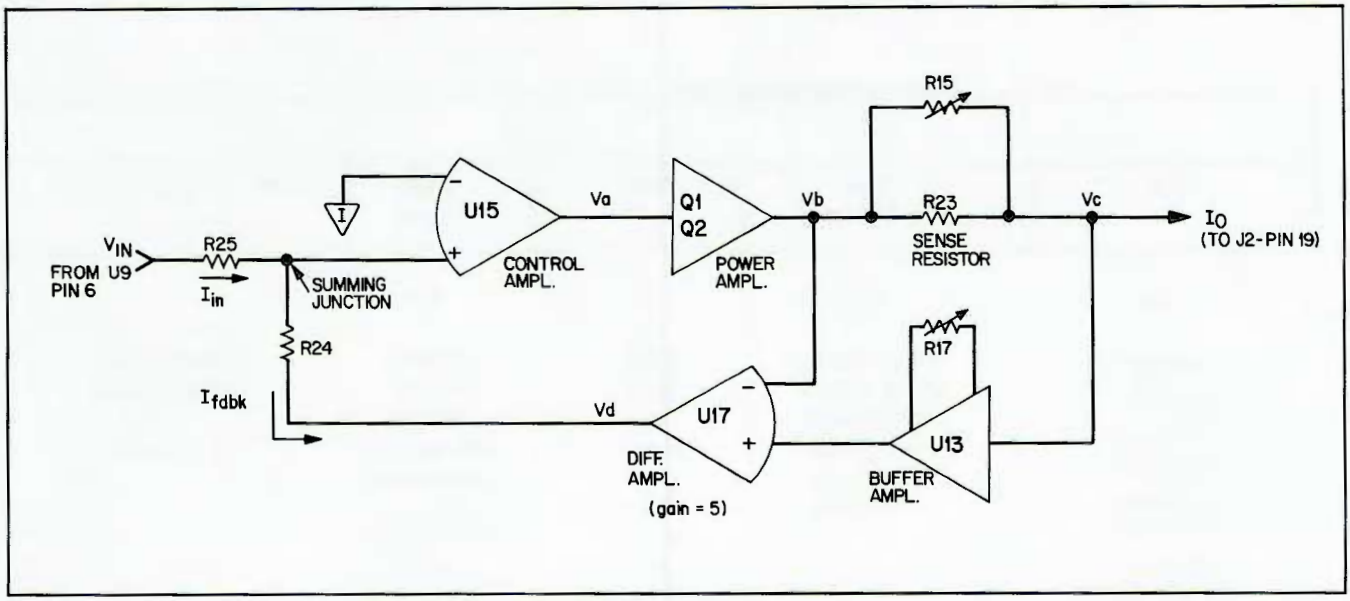


Figure 4-3. Simplified Voltage-to-Current Converter Circuit

4-49 Self-ID/Status Return Buffers

4-50 These buffers are also tri-state and their outputs are held in an open condition while the CRE control line is high. When a self-ID or status operation is decoded from the control lines, CRE goes low and RTN3 is high. This connects the inputs of the self-ID/status return buffers to the B0-B15 data lines. The self-ID/status word sent to the Multiprogrammer is shown below.

4-51 The 16-bits (B0-B15) are read back during self-test or when an Read Status (RS) instruction is programmed. During self-test, bits B3-B15 are read and stored in Multiprogrammer memory while status bits B0-B2 are ignored. A Read Format (RF) instruction is used to read B3-B15 from Multiprogrammer memory. When a Read Status (RS) instruction is issued, status bits B0-B2 are read while bits B3-B15 are ignored.

4-52 The self-ID bits B3-B15 specify the "wake-up" values of the LSB, card ID, size, and data type parameters. The values of the parameters determine how the Multiprogrammer firmware will process the data it sends to or receives from the card. Status bits, B0-B2, are used by the Multiprogrammer to check the status of the card during operation. The status information is provided by UCC outputs, BSY, ARM, and EOP.

4-53 PROCESSING AN OUTPUT SEQUENTIAL (OS) INSTRUCTION

4-54 This discussion explains the processing of a typical output type instruction. Assume that an Output Sequential (OS) instruction is issued by the controller which addresses a 69720A card in slot 1. Assume that data to be sent is +1.28 V. The format of the controller instruction is...

"OS1, +1.28T"

4-55 When this instruction is executed, the following operations occur in the sequence indicated:

a. **Addressing the D/A Card** -the slot position (slot 1 specified by the OS instruction is decoded and the CAD line to the D/A card goes high. In addition, the R/ $\overline{W}$ line, SAD0, SAD1 lines, and the three-bit control code lines (CTL0,1,2) are decoded.

b. **Loading First Rank Storage** - next, a 12-bit data word with a 1 in bit position 8 ($1.28/.005 = 256_{10} = 400_8 = 100000000_2$ is placed on the B0-B11 data lines to the first rank storage register; bits 12 to 15 are set to zero by the Multiprogrammer firmware. CDE and the R/ W line are low, and the subaddress lines SAD0 and SAD1 are zero. Decoding these lines along with CTL0,1,2 results in the STB0 strobe pulse going high and loading the first rank storage with the 16-bit data word. Also, at this time, EOP is cleared and the ARM control line is set.

c. **Cycling the Card** - shortly after STB0, an LSR strobe pulse occurs and transfers the 12 LSB's of data from first rank storage to second rank storage. BUSY goes high and the 6μs timer starts running. CEN and SYE both go high and if EXTERNAL ENABLE is high the DAC output goes to 1.28 volts.

d. **End-of-Process and Interrupt Request** - At the end of the 6μsec time out, EOP goes high and BUSY is cleared. Since ARM is also high, a program interrupt request ($\overline{IRQ}$) is sent to the Multiprogrammer to indicate that the card is ready to process another instruction.

e. **Clearing the UCC** - After the Multiprogrammer services the interrupt request, a control code is returned which will clear the ARM, EOP, and GAFF lines. The storage registers and DAC output are not cleared.

SELF-ID PARAMETERS				STATUS		
LSB	**Card Identification**	**Size**	**Data Type**	**Arm**	**Busy**	**EOP**
15-13	12-7	6	5-3	2	1	0
Jumpers set this field to 110 (.005 LSB code) on a 69720A or 100 (.01 LSB code) on a 69721A.	Hardwired to binary code of 110000 which corresponds to an ID of decimal 48.	Hard-wired to binary 0 which signifies a 12-bit data word.	Jumpers set this field to 000 which is incremented to 1 by the program (two's complement)	These are one bit flags where 1 = true 0 = false		

Section III
PRE-OPERATING INSTRUCTIONS

3-1 INTRODUCTION

3-2 The purpose of this section is to provide the User with additional information that may be required for any of the following reasons:

- The User wishes to change the External Trigger Switch or card jumpers from their "as shipped" positions to some new configuration.
- The User requires additional information on the edge connector I/O signals.
- External power supplies are required instead of the Multiprogrammer isolated supplies.

3-3 Since any of the above reasons affect the operation of the card, the information in this Section should be read before implementing any change. The following topics are covered in the order mentioned:

- Definition of all card jumpers.
- Card's External Edge Connector.
- I/O Control Signals.
- External Trigger Switch (S1).
- External Data Input.
- External Bias Supplies.

3-4 CARD JUMPERS (See Figure 3-1)

3-5 As mentioned in Section II, the D/A card is shipped with certain jumpers in place. When the User wishes to change a jumper, the information in the following paragraphs should be referenced to find the location of the applicable jumper(s) and also what jumper arrangements are possible. The jumpers are described in the following order:

a. Bidirectional Data Transceivers.
b. Current Converter Jumper, W6
c. External I/O Control Signal Jumpers.
d. Wake-Up Code Jumpers.
e. Isolated Supply Jumpers.

3-6 Bidirectional Data Transceivers Jumper, W21

3-7 This jumper is installed at the factory and, normally, is never removed. It establishes pin 19 of tri-state integrated cricuits U36 and U37 (see Figure 7-2) at ground. With pin 19 grounded, the open or isolated state of the transceivers is not used. Jumper W21 is temporarily removed during factory testing to allow the outputs of the transceivers to assume an open state for test purposes.

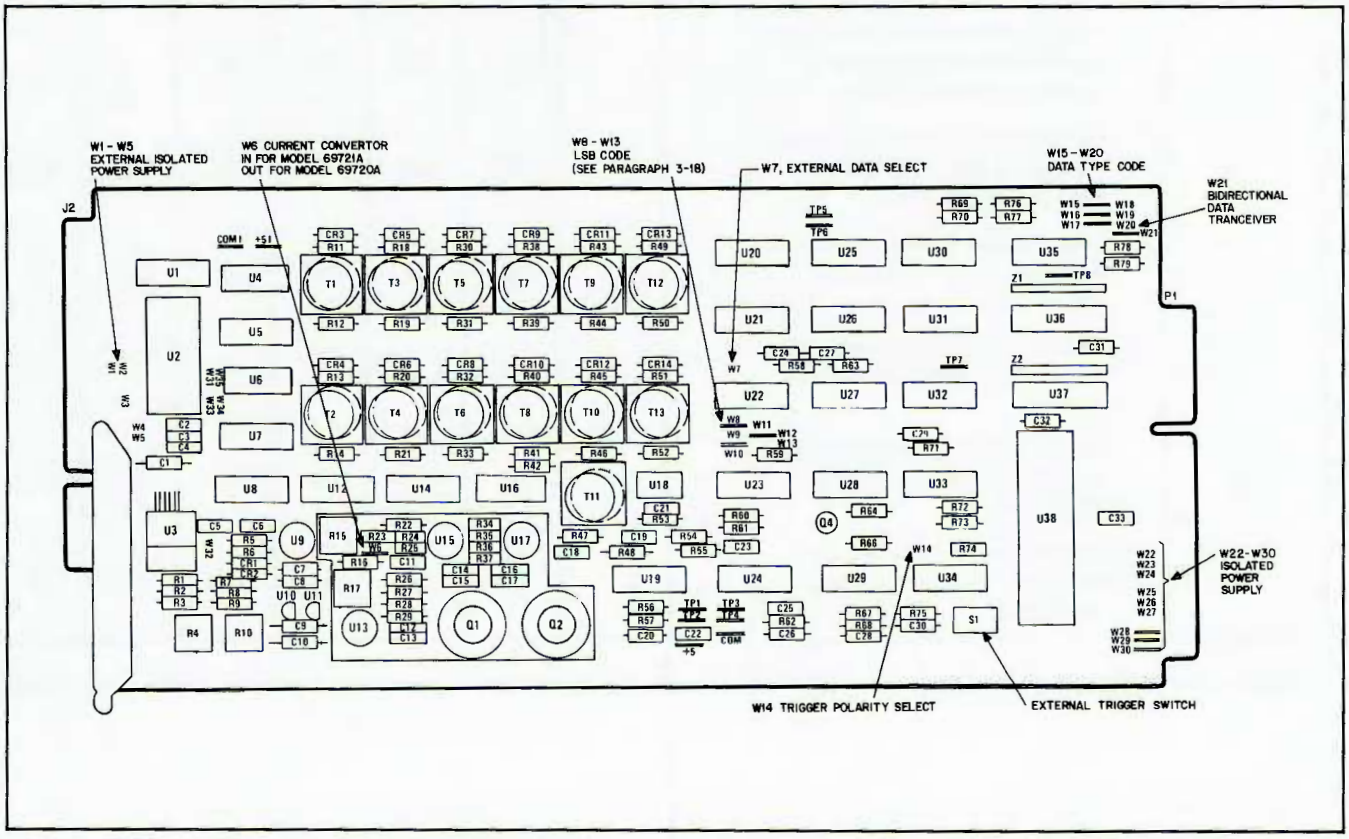


Figure 3-1. Digitial-to-Analog Voltage and Current Converters, Jumper Locations

3-8 Current Converter Jumper, W6 (Model 69721A Only)

3-9 This jumper is installed at the factory and is normally not removed. Jumper W6 is temporarily removed during factory testing allowing the isolation of the voltage output circuit from the Voltage-to-Current converter circuit.

3-10 External I/O Control Signal Jumpers

3-11 The following paragraphs describe those jumpers that affect the control signals at the external edge connector.

3-12 Trigger Polarity Select Jumper, W14. This jumper is removed prior to shipment making the Trigger Polarity Select (TPS) control line a logic high. If this jumper is installed, the TPS control line is held at a logic low level. The purpose of the Trigger Polarity Select signal is discussed in a later paragraph in this Section under "External I/O Control Signals".

3-13 $\overline{\text{External}}$ $\overline{\text{Data}}$ $\overline{\text{Select}}$ ($\overline{\text{SLT}}$) Jumper, W7. This jumper is also removed prior to shipment making the ($\overline{\text{SLT}}$) control line a logic high. If this jumper is installed, the TPS control line is held at a low logic level. The purpose of the $\overline{\text{SLT}}$ signal is discussed in a later paragraph in this Section under "External I/O Control Signals".

3-14 Wake-Up Code Jumpers

3-15 Programming Different Data Type and LSB Codes. As an alternative to changing these jumpers, it is also possible to program a card's data type or LSB value to be different from those established by the jumpers by using a Set Format (SF) instruction. Any of the data types of Table 3-1 can be used. Programmed LSB values are not limited to those in Table 3-2. Any desired LSB value between 0.001 and 65.535 with a 0.001 resolution can be programmed. This allows the user to express programmed data in units appropriate to the process to which the card is dedicated.

Table 3-1. Data Type Code Jumpers

DATA TYPE CODE	DESCRIPTION	JUMPER ARRANGEMENT					
		W18	W19	W20	W15	W16	W17
1*	Programmed positive or negative number is stored on card in two's complement form.	OUT	OUT	OUT	IN	IN	IN
2	Programmed positive or negative number is stored on card in sign-magnitude form.	OUT	OUT	IN	IN	IN	OUT
3	Programmed positive number is stored on card in unsigned binary form.	OUT	IN	OUT	IN	OUT	IN
4	(Special autorange code used only with 69736A Timer/Pacer card).	--	--	--	--	--	--
6	Programmed Positive number is stored on card in unsigned BCD form.	IN	OUT	IN	OUT	IN	OUT
7	Programmed octal integer is stored on card in unsigned binary form.	IN	IN	OUT	OUT	OUT	IN

*When the card is shipped, its jumpers are arranged to select the two's complement data type when power is applied to the system.

3-16 Data Type Code Jumpers, W15 through W20. These jumpers specify the data type code sent to the Multiprogrammer as part of the wake-up sequence. Both D/A cards are shipped with jumpers W15, W16, and W17 installed and, jumpers W18, W19, and W20 removed. The Multiprogrammer interprets these jumpers as data type code = 1 specifying a two's complement format.

3-17 These jumpers can be changed to specify a different data type code. For example, data type code = 7 could be selected to program a bit pattern in octal form. Table 3-1 shows which jumper must be in and which jumpers must be removed to select other data type codes.

3-18 LSB Code Jumpers, W8 through W13. The 69720A D/A card is shipped with LSB Code jumpers W8, W12, and W13 installed which specifies a 5 mV LSB code. The 69721A card is shipped with W8, W10 and W12 installed, specifying a 10 mA LSB code. Table 3-2 shows the other valid LSB Codes and required jumpers.

3-19 ±18 V Isolated Power Supply Jumpers

3-20 The 6942A and 6943A mainframes each contain three ±18 V supplies with outputs isolated up to 250 Vdc or 250 ac peak from digital common and each other. These supplies are used to power the analog circuitry of many I/O cards. Three separate supplies are provided so that individual cards or groups of cards can be electrically isolated from each other when necessary. All models of cards that use these supplies are equipped with jumpers so that any one of the three supplies can be used to power the specific card. When shipped from the factory, all D/A cards are jumpered to ±18 V supply No. 1. Jumpers may have to be changed on one or more cards if several are to be installed in one mainframe of if some cards must be isolated from others. The jumpers used for ±18 V supply selection are identified in Table 3-3. The ±18 V power requirements of all the present I/O card models are given in the applicable I/O card Operating Manuals. The maximum current that is available from each isolated supply is as follows:

Output Voltage	+18 V	−18 V
Supply No. 1	1.0 A	0.6 A
Supply No. 2	0.4 A	.25 A
Supply No. 3	0.2 A	.15 A

Table 3-2. LSB Code Jumpers

LSB CODE	LSB VALUE	JUMPER ARRANGEMENT					
		W12	W13	W11	W9	W10	W8
0	0.001	OUT	OUT	OUT	IN	IN	IN
1	0.025	OUT	OUT	IN	IN	IN	OUT
2	0.1	OUT	IN	OUT	IN	OUT	IN
3	0.5	OUT	IN	IN	IN	OUT	OUT
4*	0.01	IN	OUT	OUT	OUT	IN	IN
5	0.05	IN	OUT	IN	OUT	IN	OUT
6*	0.005	IN	IN	OUT	OUT	OUT	IN
7	1.0	IN	IN	IN	OUT	OUT	OUT

*When the card is shipped, its jumpers are arranged to select LSB code #6 for the 69720A and LSB code #4 for the 69721A when power is applied to the system.

Table 3-3. Isolated Power Supply Jumper Selection.

Jumper	W22	W23	W24	W25	W26	W27	W28	W29	W30
±18 V Supply No. 1	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	IN
±18 V Supply No. 2	OUT	OUT	OUT	IN	IN	IN	OUT	OUT	OUT
±18 V Supply No. 3	IN	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT

3-21 When configuring a Multiprogrammer system, the power supply requirements of the cards using the ±18 V supplies should be added up. If the total exceeds the capacity of the ±18 V supply being used, some of the cards should be rejumpered to one of the other supplies.

3-22 Isolated power can also be supplied to a D/A card externally. Jumper changes are required to implement this feature. Since this is a special application, it is treated separately at the end of Section III.

3-23 CARD'S EXTERNAL EDGE CONNECTOR

3-24 The pin assignments of the input and output signals available at the card's external edge connector are shown in Figure 3-2. (The lettered pins are on the component side of the card.) One dual 36-pin edge connector is supplied with each I/O card for interfacing field wiring to the card. Instructions for making up the mating connector and hood assembly are provided in Chapter 2 of the 6942A User's Guide.

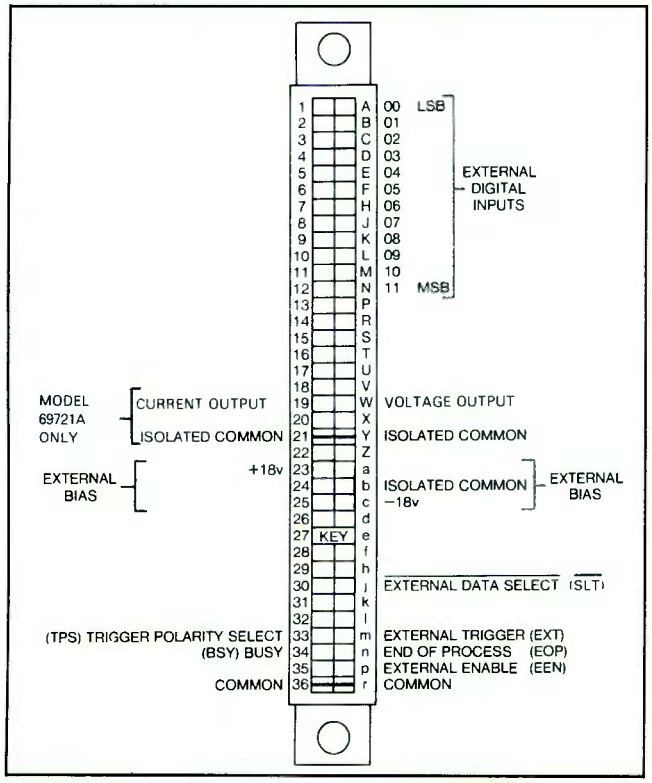


Figure 3-2. D/A Card External Edge Connector

3-25 EXTERNAL I/O CONTROL SIGNALS

3-26 Table 3-4 describes the control signals which interconnect between the D/A card and the Customer's equipment. The electrical specifications for thse signals are given in Table 1-1 of Section I.

3-27 EXTERNAL TRIGGER SWITCH (See Figure 3-3)

3-28 The External Trigger input signal at the D/A card's edge connector can be used to start a D/A conversion cycle. The external trigger switch (S1) is used to speed up the time required for the card to respond to an External Trigger pulse. Switch assembly S1 consists of four individual open/close type switches designated S1-1 through S1-4. Switches S1-1 through S1-3 affect the External Trigger input signal; S1-4 is not used. The card is shipped from the factory with only S1-1 closed.

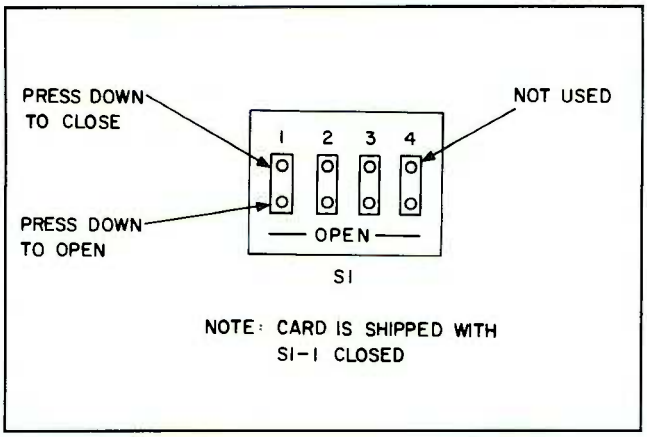


Figure 3-3. External Trigger Switch

3-29 With switch S1-1 closed, the card can be cycled either internally by the controller (e.g., a CY instruction) or by the External Trigger input. With S1-1 closed, there is a 13 to 20 microsecond delay between the time that the External Trigger signal arrives and the time that the D/A conversion is started. In some applications, the delay does not allow sufficiently close synchornization with the external event, nor fast enough trigger rates. This delay can be reduced to seven microseconds by opening S1-1 and closing either S1-2 or S1-3. With S1-1 open the card can be triggered *only* by the External Trigger input and not by the controller. If S1-2 is closed, the External Trigger input is actuated by a positive-going signal; if S1-3 is closed, the input is actuated by a negative-going signal.

CAUTION

Only one of the three switches, designated S1-1, S1-2, or S1-3, should be in the closed position at any one time.

3-30 Notice that neither the TPS input nor jumper W14 will affect the external trigger's input logic sense when either S1-2 or S1-3 is closed.

Table 3-4. Card's External I/O Control Signals

I/O Control Signal	J-2 Pin No.	TTL Level	Description
EXTERNAL ENABLE also EEN (card input)	p	High	If pin p is left unconnected, EEN remains at a logic high level and the analog output will be the value stored in Second Rank.
		Low	If pin p is forced low, the D/A output immediately goes to zero until EEN is made high again.
TRIGGER POLARITY SELECT also TPS (card input)	33	High	If pin 33 is left unconnected, TPS remains high. With TPS high, a low-to-high transition of the EXTERNAL TRIGGER line cycles the card.
		Low	If pin 33 is made low (or jumper W2 is installed), a high-to-low transition of the EXTERNAL TRIGGER line cycles the card.
EXTERNAL TRIGGER also EXT (card input)	m	edge sensitive	This signal is used to cycle the card externally after a Write First (WF) rank instruction has been issued at the controller. The TRIGGER POLARITY SELECT line determines the triggering edge.
BUSY (card output) also BSY	34	High	Busy goes high when the card is cycled. BUSY is high when the DAC output is changing to the value in Second Rank Storage.
		Low	BUSY goes low when EOP goes high.
END-OF-PROCESS also EOP (card output)	n	High	Goes high 6 μsec. after Busy goes high. EOP remains high for a minimum of 2 μsec. and stays high for a time dependent on the firmware. Pin n going high can be used as an indication that the operation has completed and the output has settled.
		Low	EOP is set low by the Multiprogrammer in response to an interrupt request or a Clear Card (CC) instruction.

Table 3-4. Card's External I/O Control Signals (Cont.)

I/O Control Signal	J-2 Pin No.	TTL Level	Description
EXTERNAL DATA SELECT also SLT (card input)	j	High	Normally high, this input selects First Rank Storage as the source of data with which Second Rank is loaded.
		Low	When pulled low, externally supplied data is used to load Second Rank when the card is cycled. By installing Jumper W7 this input will be forced to a logic low.
COMMON	r, 36		Signal return for all control signals and data lines.

3-31 EXTERNAL DATA INPUTS

3-32 The 12 external input lines available on the J2 edge connector (pins A through N) permit an external device, such as a 69790B Memory card, to supply data to the D/A card. The Most Significant Bit (MSB) input is pin N; the Least Significant Bit (LSB) is pin A. The D/A card will accept only two's complement data from an external source. Data common is at J2-36 and J2-r. The external data port may be selected by pulling the SLT input (J2-j) to a logic low level, by shorting it to ground, or by installing jumper W7. The card still must be cycled in order to load the data into Second Rank Storage and thereby start the D/A conversion.

3-33 EXTERNAL BIAS SUPPLIES

3-34 A regulated or unregulated external power supply can be used to power the card's D/A converter and output amplifier circuits. If a regulated supply with ± 15 V outputs is used, the on-board ± 15 V regulators are bypassed by installing jumpers W4 and W5. A regulated or unregulated supply with ± 17.7 to ± 19.9 volt outputs can be used if the on-board regulators are made operational by removing jumpers W4 and W5. External bias input terminals are provided at the card edge connector (see Figure 3-2). If an external supply is used, the mainframe isolated power supply jumpers (paragraph 3-19) must be removed and external supply jumpers installed as described in Table 3-5 below.

Table 3-5. External Isolated Power Supply Jumpers

Jumper	W1	W2	W3	W4	W5
Regulated or Unregulated ± 17.7 V to ± 19.9 V	IN	IN	IN	OUT	OUT
Regulated ± 15 V*	IN	IN	IN	IN	IN

*Using a ± 15 V external isolated supply to power the 69721A Current Converter Card instead of a normal ± 18 V Supply, may reduce the card's compliance voltage to less than 11 volts.

Section IV
THEORY OF OPERATION

4-1 INTRODUCTION

4-2 This section explains the theory of operation for the 69720A and 69721A D/A cards. The theory is written with the assumption that the reader is familiar with the instructions set and the basic operation of the 6942A Multiprogrammer. First, a brief description is given covering the basic operation and features of the D/A cards. A detailed block diagram discussion covering both cards follows. This selection concludes with an example of the processing of an Output Sequential instruction.

4-3 OVERALL OPERATION

4-4 Power Turn-On

4-5 When power is applied to the D/A Card, the circuits on the card are cleared. A self-test is then initiated by the Multiprogrammer to test part of the circuits of the D/A card. The self-ID, data type, size, and LSB parameters of the card are read and stored in Multiprogrammer memory as part of the wake-up sequence. Card Enable (CEN) holds the card output at zero until the first cycling operation (see paragraph 4-8).

4-6 First Rank Storage

4-7 When the D/A card is addressed in any output type instruction (OP, OS, OB, OI, WC, or WF), a 16-bit data word is sent to the card and is stored in a register called first rank storage. The data word in first rank storage can be read at any time with a Read Value (RV) instruction. If a WF output instruction were issued at the controller, this instruction would be completed with the loading of first rank storage. For any other output instruction, a "cycle" operation (described in the next paragraph) automatically begins after the data word is loaded into first rank storage.

4-8 Cycling the Card

4-9 In a cycle operation, the 12 LSB's of the data word in first rank storage are transferred to a second register called second rank storage. Immediately after this transfer, several events take place simultaneously as part of the cycling operation:

a. A CARD ENABLE (CEN) signal goes high (if not already high from a previous cycle) and allows the data word in second rank storage to be transferred to the Digital to Analog Converter (DAC) so that it can produce an analog output. The MSB (bit 11) of this word is inverted to supply the DAC module with a data word compatible with its internal format. The output will remain at the programmed level until: (1) the card is re-programmed, (2) a power up reset occurs, (3) A System Disable (SD) instruction is issued, or (4) the External Enable (EEN) line at the external edge connector is made low.

b. The BUSY (BSY) signal goes high and is sent to the external edge connector. This signal indicates that the data word is currently selecting the analog output.

c. A 6 μs timer begins running.

4-10 As mentioned previously, a cycle operation occurs automatically for all output instructions except a WF instruction. When a WF instruction is issued, the cycle operation is normally initiated in one of two ways (see Figure 4-1):

1. By the controller issuing a Cycle (CY) instruction to specifically cycle the card, or
2. Externally at the external interface connector by applying an EXTERNAL TRIGGER signal. When an External Trigger is applied, an additional signal called TRIGGER POLARITY SELECT determines whether cycling will occur on the low-to-high or high-to-low transition of the EXTERNAL TRIGGER pulse. More information on external triggering can be found in Section III under "External Trigger Switch".

4-11 End-of-Process

4-12 An End-of-Process (EOP) signal is generated when the 6μsec timer times out. The EOP signal is sent to the external interface connector and is also used to generate a Multiprogrammer interrupt request.

4-13 Interrupt Request

4-14 When the End-of-Process (EOP) signal occurs and the card is armed, an Interrupt Request ($\overline{IRQ}$) is returned to the Multiprogrammer to indicate the completion of the output operation. OB, OI, OP, and OS output instructions arm the card when the first rank storage register is loaded. For WF, WC and CY instructions, the card must be armed before an interrupt can be generated. This can be done with a separate Arm Card (AC) instruction issued at the controller. After a program interrupt request is made, the Multiprogrammer will respond by disarming the card, clearing EOP and the group address flag (GAFF).

4-15 The GAFF flag is internal to the Universal Control Chip on the card and is set by instructions, such as; WC, OI, OP, to allow multiple cards to be cycled in parallel. Refer to Chapter 4 in the 6942A Multiprogrammer User's Guide for more information on cycling cards in parallel.

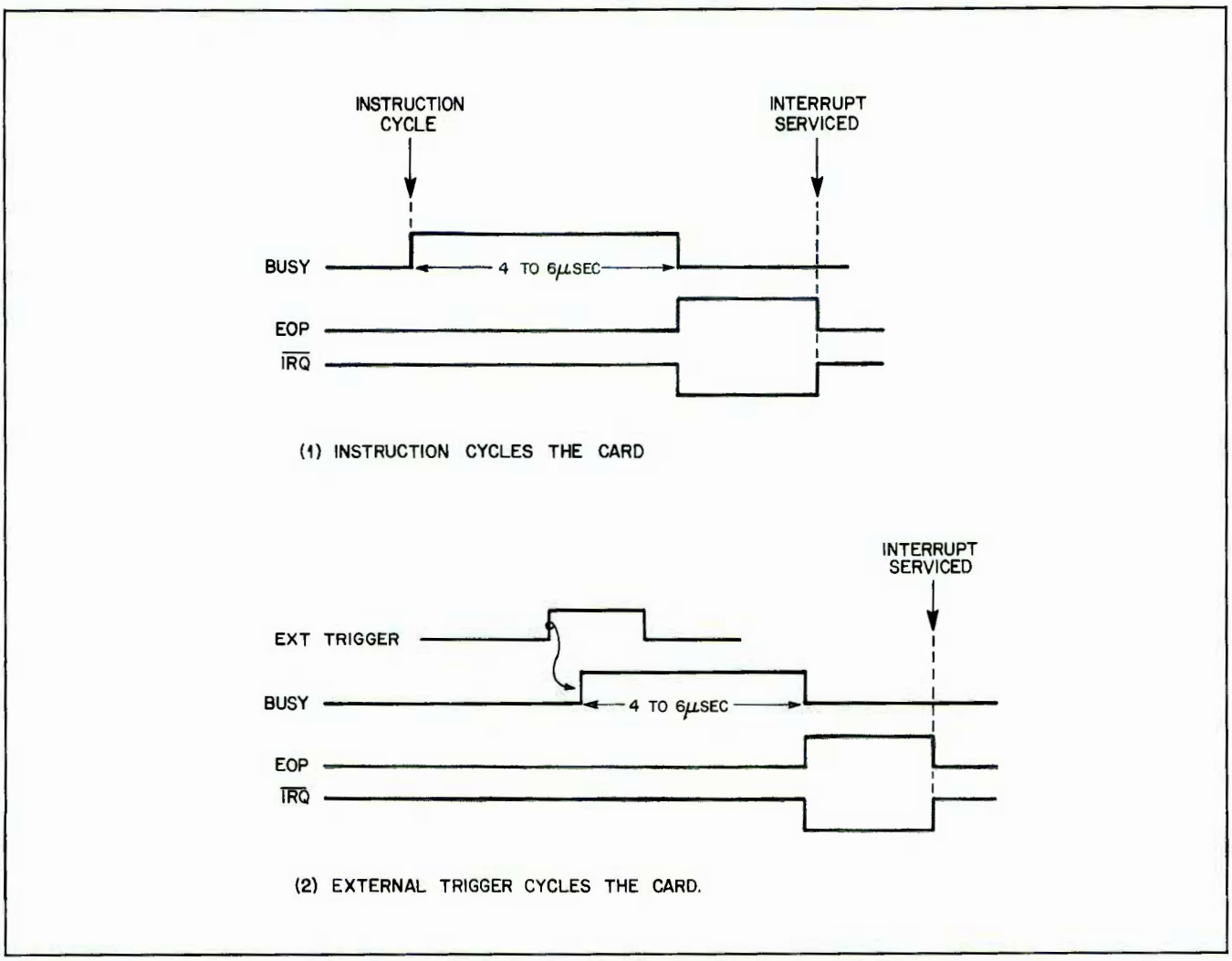


Figure 4-1. Card Cycling and Busy/EOP Timing

4-16 Output Quick-Disconnect

4-17 This feature permits either the controller or the customer interface logic to force the DAC output to zero. The controller can do this by issuing a System Disable (SD) instruction. The external interface logic can do this by making the External Enable signal low. If the controller issues an SE instruction and the EXTERNAL ENABLE signal is high, the DAC output will return to the level which was present prior to issuing SD or making EEN low.

4-18 Self-ID/Status Word

4-19 When the Multiprogrammer performs a self test, or when the controller issues a Read Status (RS) instruction, the D/A card returns a 16-bit status word to the Multiprogrammer. This word contains information on the operational status of the card and shows how the card is hardware configured. The status word is discussed in more detail in the detailed block diagram discussion.

4-20 DETAILED BLOCK DIAGRAM DISCUSSION

4-21 Figure 4-2 is a block diagram of both the 69720A and the 69721A. The voltage-to-current converter circuit applies only to model 69721A D/A cards. The D/A card consists of the following functional circuits:

a. Universal Control Chip (UCC).
b. Tri-state bidirectional data transceivers.
c. First rank storage register.
d. Data multiplexer
e. Data isolators.
f. Second rank storage register.
g. Output enable gates.
h. D/A converter.
i. Voltage to current converter (69721A only)
j. Six-μsec Timer.
k. First rank return buffers.
l. Self-ID/Status return buffers.

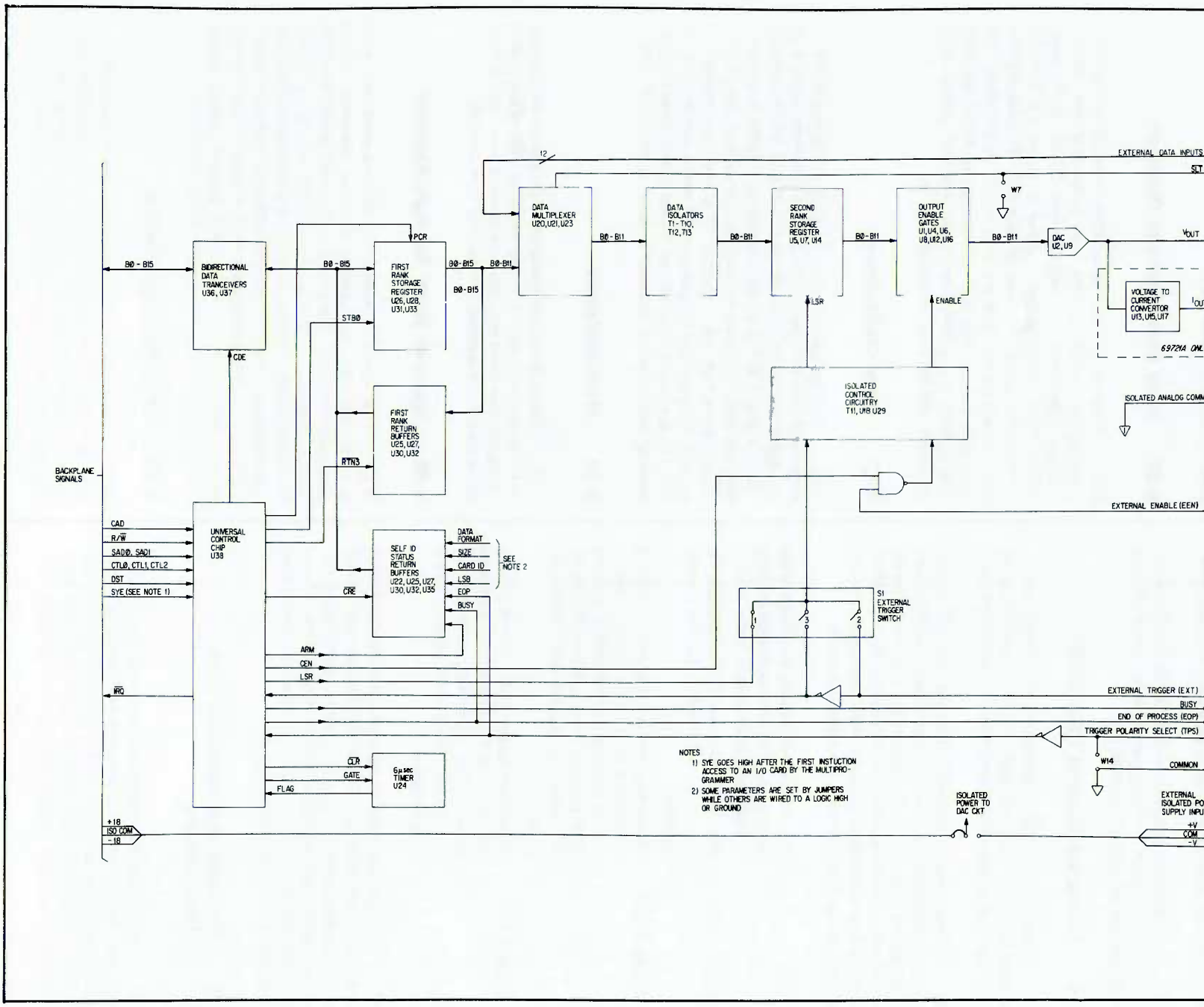


Figure 4-2. D/A Output Card, Detailed Block Diagram

4-22 When the D/A Output card is installed in a slot position in the Multiprogrammer, 6942A, or in the Extender chassis, 6943A, the card is assigned the address of that slot position. Once installed, the card connects to the data lines (B0-B15), the control lines, and to the power input lines of the backplane.

4-23 The following paragraphs describe the functional circuits shown in Figure 4-2. The functional schematic in Section VII should also be used as reference

4-24 Universal Control Chip (UCC)

4-25 Control chip (U38) supervises all the operations taking place on the D/A Output card. The UCC establishes the timing sequence for the various control signals used on the card.

4-26 When power is applied to the card, the PCR control signal goes high and clears all control circuits and first rank register on the card. The card is then ready to process any instruction issued at the controller that addresses the card. When an output type instruction is issued, the following input control lines set up the UCC for a particular operation:

CAD - This is the card address line which goes high to select the D/A card when the card is addressed in an output instruction.

R/$\overline{W}$ - This is the read/write line. It is high for a read operation and is low for a write operation.

SAD0, SAD1 - These two lines are decoded to select a subaddress on the card during a read or a write operation. For example, during a write to subaddress 0, binary 00 is sent; for a read from subaddress 3, binary 11 is sent.

CTL0, CTL1, CTL2 - These lines supply a 3-bit control code to the UCC to indicate what operation is to be performed. Depending on the instruction issued, one or more codes are sent in succession.

4-27 The data values on the above control lines are loaded into the UCC when a DATA STROBE (DST) pulse occurs. This data is then decoded to produce the various control signal outputs required for the indicated operation. A description of these control signals as they relate to the function being performed is included in the following paragraphs.

4-28 Tri-State Bidirectional Data Transceivers

4-29 The tri-state bidirectional tranceivers control the direction of data flow to and from the card over the B0-B15 data lines. During a write operation, CARD DRIVER ENABLE (CDE) is low and the B0-B15 data lines are connected to the input of the first rank storage register. During a read operation, CDE goes high and the B0-B15 data lines are connected to the output of the first rank return buffer and to the output of the self-ID/status return buffer. Although the transceivers are tri-state logic, jumper W21 establishes pin 19 at ground so that the open state condition is never used.

4-30 First Rank Storage Register

4-31 When any output instruction is executed, a data word is placed on the B0-B15 data lines to the first rank storage register. Subaddress 0 is decoded from SAD0, SAD1 lines; CTL0, CTL1, and CTL2 are decoded to produce a STROBE ZERO (STB0) pulse. The leading edge of STB0 loads the first rank storage register with the data on the B0-B15 lines. The data word stored in first rank storage can be read at any time with a Read Value (RV) instruction. The first rank storage register is cleared only on power turn on.

4-32 Data Multiplexers

4-33 The digital data word to the DAC can be supplied from either first rank storage or the J2 edge connector (pins A to N), depending on the state of the EXTERNAL DATA SELECT ($\overline{SLT}$) input. If $\overline{SLT}$ is a logic low level or shorted to ground, the data word furnished to the DAC will be from the J2 connector; if it is high, bits 0 through 11 of first rank storage will be used. External data may also be selected by installing jumper W7. For the card to function over its full bipolar output range, external data must be supplied in two's complement form.

4-34 Data Isolators

4-35 This bank of pulse transformers isolates the analog output circuitry from the +5 V data common. When the card is cycled the data word from the multiplexer is transferred across the isolators and latched into second rank storage.

4-36 Second Rank Storage Register

4-37 This register is loaded with the data word only when a cycle operation is initiated. A cycle operation occurs automatically as part of any output instruction except for a WF output instruction. Shortly after STB0 occurs, a LOAD SECOND RANK (LSR) strobe pulse is produced to begin the cycle sequence. The LSR signal is transferred through a pulse transformer and its leading edge loads the second rank storage register. For information on how the external trigger switch (S1) affects the cycling of the card, refer to Section III.

4-38 Output Enable Gates

4-39 These gates have two purposes: first, they prevent the data word from reaching the DAC until the programmed data word is loaded into second rank storage. Second, they can disconnect the data lines to the DAC (thus forcing it's output

to zero) when either the EXTERNAL ENABLE (EEN) signal or the CARD ENABLE (CEN) signal goes low. CEN goes high after the first LSR pulse occurs and remains true until either a System Disable (SD) instruction is issued or a power reset occurs. The D/A output returns to the value stored in the second rank register when both CEN and EEN return high.

4-40 Voltage DAC

4-41 The voltage DAC takes the digital word from second rank storage and converts it into a proportional output voltage. The voltage DAC consists of a 12-bit D/A converter module U2 and an associated operational amplifier U9 (see Figure 7-2.) The 24 pin D/A module provides an output current which is proportional to the digital word at its input. The operational amplifier is used as a current-to-voltage converter. The current from the D/A module drives the summing junction of the operational amplifier to produce a bipolar output voltage at J2-W within the range of −10.24 V to +10.235 V. Voltage gain adjustments may be made with potentiometer R4; R10 is used to adjust voltage offset. Refer to Section V for calibration procedures.

4-42 Voltage-to-Current Circuit (69721A only)

4-43 This circuit (refer to Figures 4-3 and 7-2) supplies a constant output current that is proportional to the input voltage at U9 pin 6. The circuit monitors the output current by sensing the voltage drop (Vb-Vc) across R23. If the output current attempts to change, U17 and U13 will immediately detect this change and generate a correction voltage (Vd) which causes U15 to drive the power amplifier (Q1 and Q2) in such a way as to "pump" more or less current to the output as needed.

4-44 The effective resistance of R23 can be changed by adjusting R15, thereby altering the gain of the entire converter circuit. Since the buffer Amplifier (U13) has unity voltage gain and a high input impedance, it does not draw significant current through sense resistor R23. Offsets for the entire circuit may be nullified by adjusting R17. The differential amplifier (U17) produces an inverted output voltage (Vd) which is five times the voltage across the sense resistance. Since the inverting input of U15 is essentially at ground potential, the non-inverting input must be essentially at ground potential also. Given that no current can flow into the input of an ideal amplifier, the ground potential at the non-inverting input of U15 is maintained as long a $I_{in} = I_{fdbk}$.

4-45 6-Microsecond Timer

4-46 The 6 μsec timer begins running when a cycle operation is initiated. The output of the timer goes low when GATE is generated by the UCC and returns to a logic high 6 μs later. This low-to-high transition sets the END-OF-PROCESS (EOP) output and resets the BUSY output. EOP going high indicates that the analog output has stabilized and the instruction has completed.

4-47 First Rank Return Buffers

4-48 These buffers are used to place the contents of the first rank storage register on the B0-B15 data lines. When a Read Value (RV) instruction is issued, subaddress 3 is decoded from the SAD0, SAD1 lines and this information along with CTL0, CTL1, CTL2 and the R/ $\overline{W}$ line produce a low $\overline{\text{RETURN 3}}$ (RTN3) logic level. This control signal enables the tri-state output of the first rank return buffers. CDE is also high and the data word in first rank storage is sent to the Multiprogrammer via the first rank return buffers.

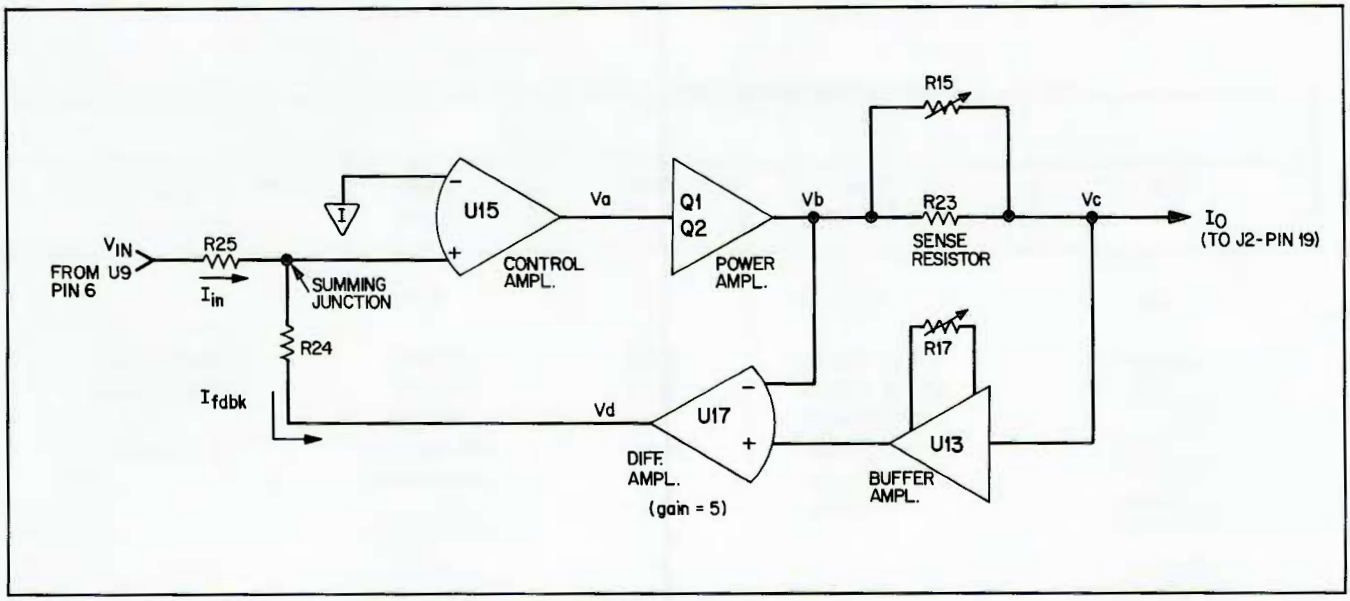


Figure 4-3. Simplified Voltage-to-Current Converter Circuit

4-49 Self-ID/Status Return Buffers

4-50 These buffers are also tri-state and their outputs are held in an open condition while the CRE control line is high. When a self-ID or status operation is decoded from the control lines, CRE goes low and RTN3 is high. This connects the inputs of the self-ID/status return buffers to the B0-B15 data lines. The self-ID/status word sent to the Multiprogrammer is shown below.

4-51 The 16-bits (B0-B15) are read back during self-test or when an Read Status (RS) instruction is programmed. During self-test, bits B3-B15 are read and stored in Multiprogrammer memory while status bits B0-B2 are ignored. A Read Format (RF) instruction is used to read B3-B15 from Multiprogrammer memory. When a Read Status (RS) instruction is issued, status bits B0-B2 are read while bits B3-B15 are ignored.

4-52 The self-ID bits B3-B15 specify the "wake-up" values of the LSB, card ID, size, and data type parameters. The values of the parameters determine how the Multiprogrammer firmware will process the data it sends to or receives from the card. Status bits, B0-B2, are used by the Multiprogrammer to check the status of the card during operation. The status information is provided by UCC outputs, BSY, ARM, and EOP.

4-53 PROCESSING AN OUTPUT SEQUENTIAL (OS) INSTRUCTION

4-54 This discussion explains the processing of a typical output type instruction. Assume that an Output Sequential (OS) instruction is issued by the controller which addresses a 69720A card in slot 1. Assume that data to be sent is +1.28 V. The format of the controller instruction is...

"OS1, +1.28T"

4-55 When this instruction is executed, the following operations occur in the sequence indicated:

a. **Addressing the D/A Card** -the slot position (slot 1 specified by the OS instruction is decoded and the CAD line to the D/A card goes high. In addition, the R/ $\overline{W}$ line, SAD0, SAD1 lines, and the three-bit control code lines (CTL0,1,2) are decoded.

b. **Loading First Rank Storage** - next, a 12-bit data word with a 1 in bit position 8 ($1.28/.005 = 256_{10} = 400_8 = 100000000_2$ is placed on the B0-B11 data lines to the first rank storage register; bits 12 to 15 are set to zero by the Multiprogrammer firmware. CDE and the R/ W line are low, and the subaddress lines SAD0 and SAD1 are zero. Decoding these lines along with CTL0,1,2 results in the STB0 strobe pulse going high and loading the first rank storage with the 16-bit data word. Also, at this time, EOP is cleared and the ARM control line is set.

c. **Cycling the Card** - shortly after STB0, an LSR strobe pulse occurs and transfers the 12 LSB's of data from first rank storage to second rank storage. BUSY goes high and the 6μs timer starts running. CEN and SYE both go high and if EXTERNAL ENABLE is high the DAC output goes to 1.28 volts.

d. **End-of-Process and Interrupt Request** - At the end of the 6μsec time out, EOP goes high and BUSY is cleared. Since ARM is also high, a program interrupt request ($\overline{IRQ}$) is sent to the Multiprogrammer to indicate that the card is ready to process another instruction.

e. **Clearing the UCC** - After the Multiprogrammer services the interrupt request, a control code is returned which will clear the ARM, EOP, and GAFF lines. The storage registers and DAC output are not cleared.

SELF-ID PARAMETERS				STATUS		
LSB	**Card Identification**	**Size**	**Data Type**	**Arm**	**Busy**	**EOP**
15-13	12-7	6	5-3	2	1	0
Jumpers set this field to 110 (.005 LSB code) on a 69720A or 100 (.01 LSB code) on a 69721A.	Hardwired to binary code of 110000 which corresponds to an ID of decimal 48.	Hard-wired to binary 0 which signifies a 12-bit data word.	Jumpers set this field to 000 which is incremented to 1 by the program (two's complement)	These are one bit flags where 1 = true 0 = false		

Section V
CALIBRATION PROCEDURES

5-1 INTRODUCTION

5-2 Separate calibration procedures are provided in this section for Model 69720A and 69721A cards. The card is calibrated and ready for use when shipped, but calibration may be required if the card's output(s) are observed to exceed specification accuracy limits. The sample test program in Chapter 7 of the 6942A User's Guide can be used to check the card. The card must be recalibrated following the replacement of components in the D/A voltage converter, the voltage output amplifier, or the current output amplifier.

5-3 Equipment Required

1. Digital voltmeter with minimum accuracy of 0.005% of reading (HP Model 3455A or equivalent).
2. Desktop computer with HP-IB Interface card.
3. Precision resistor, 500 Ω ±0.005% (needed to calibrate Model 69721A only).

5-4 Test Set-Up

5-5 Install the 69720A or 69721A card in slot 1 of a 6942A mainframe with no other cards installed, or else mount it on a 6942A PC Board Extender card (HP Part No. 5060-2792) installed in slot 1. Connect the controller to the Multiprogrammer through the HP-IB Interface card.

5-6 Model 69720A Calibration Procedure

1. Connect the DVM across the 69720A card's voltage output between pins J2-W (Voltage Output) and J2-Y (Isolated Common).
2. Energize the 6942A and the DVM and allow them to warm up for at least 20 minutes.
3. Program the card output to its negative full-scale value of −10.240 volts by programming an Output Parallel instruction as follows:

   "OP,1,−10.240T"

4. Adjust voltage offset potentiometer R10 for a DVM display of −10.240 volts.
5. Program the card to its positive full-scale value of +10.235 volts by programming:

   "OP,1,10.235T"

6. Adjust voltage gain adjust potentiometer R4 for a DVM display of +10.235 volts.
7. Program the card to negative full-scale again and repeat the procedure starting at step 4, if required.

5-7 Model 69721A Calibration Procedure

1. Connect the DVM across the 69721A card's voltage output between pins J2-W (Voltage Output) and J2-Y (Isolated Common).
2. Energize the 6942A and the DVM and allow them to warm up to at least 20 minutes.
3. Program the card to its negative full-scale current of −20.48 milliamps by programming an Output Parallel instruction as follows:

   "OP,1,−20.48T"

4. Adjust voltage offset potentiometer R10 for a DVM display of −10.240 volts.
5. Program the card to its positive full-scale current of +20.47 milliamps by programming:

   "OP,1,20.47T"

6. Adjust voltage gain adjust potentiometer R4 for a DVM display of +10.235 volts.
7. Program the card to its negative full scale current again and repeat the procedure starting at step 4, if required.
8. Connect the 500Ω 0.005% resistor between current output pins J2-19 and J2-21.
9. Program the card for zero output:

   "OP,1,0T"

10. Record the voltage displayed on the DVM.
11. Move the DVM's positive lead from the voltage output at J2-W to the current output at J2-19.
12. Adjust current offset potentiometer R17 for a DVM display equal to the one recorded in step 10.

NOTE

If the resistor used is not within 0.005% of 500 Ω, adjust for a DVM display based on the actual resistor value as follows:

$$V_{DISPLAYED} = \frac{R_{ACTUAL}}{500} \; V_{RECORDED}$$

13. Program the card to its positive full-scale current of +20.47 milliamps by programming as in step 5.
14. Adjust current gain adjust potentiometer R15 for a DVM display of +10.235 volts. (Adjust for 10.235 volts multiplied by $R_{ACTUAL} \div 500$ if resistor is not within 0.005% of 500Ω.)
15. Program the card to its negative full-scale current of −20.48 milliamps by programming as in step 3.
16. Check the DVM display for a reading of −10.240 volts. (Check for reading of −10.240 volts multiplied by $R_{ACTUAL}/500$ if resistor is not within 0.005% of 500Ω.) If further adjustment is required, repeat steps 9 through 16.

Section VI
PARTS LIST

6-1 INTRODUCTION

6-2 This section contains information on ordering replacment parts for the D/A card. Table 6-1 lists the electrical and mechanical components of the 69720A card and Table 6-2 lists the components for the 69721A. Table 6-3 lists the parts comprising the external I/O connector assembly supplied with the card. Figure 6-1 illustrates how the parts in Table 6-3 are assembled.

6-3 HOW TO ORDER PARTS

6-4 You can order parts from your local Hewlett-Packard sales office. Refer to the list of sales offices at the end of this manual for the office nearest you. When ordering parts include the following information:

a. the Hewlett-Packard part number.
b. a description of the part.
c. the quantity desired.
d. the model nubmer of the card (69720A or 69721A) on which the part is used.

6-5 If you wish to order a part directly from the manufacturer, locate the manufacturer's Federal Supply Code in Table 6-1 or Table 6-2 and use this code to find the manufacturer's address in Table 6-4.

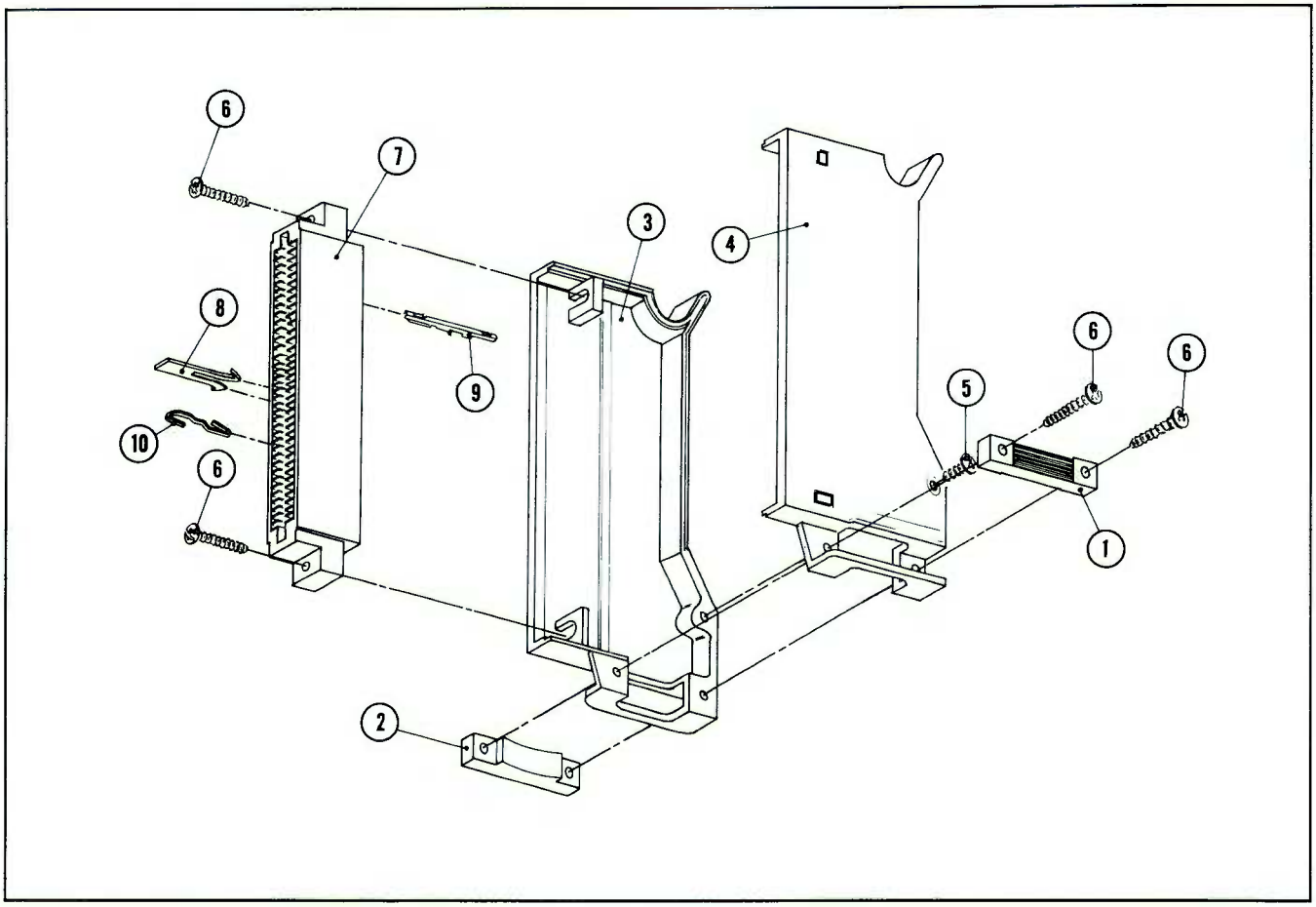


Figure 6-1. External I/O Connector Assembly, (HP, P/N 5060-2806) Exploded View

Table 6-1. 69720A Parts List

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
C1	0180-0291	4	fxd TA luf +-10% 35Vdc	56289	150D105X9035A2
C2-4	0160-0127	6	fxd cer luf +-20% 25Vdc	28480	
C5	0150-0093	1	fxd cer .01uf +80-20% 100Vdc	28480	
C6	0160-0949	1	fxd mica 68pf +-5% 300Vdc	28480	
C7,8	0160-0127		fxd cer luf +-20% 25Vdc	28480	
C9,10	0180-0291		fxd TA luf +-10% 35Vdc	56289	150D105X9035A2
C11-17			NOT ASSIGNED		
C18,19	0160-3070	4	fxd mica 100pf +-5% 300Vdc	28480	
C20	0160-4722	9	fxd cer 0.1uf +80-20% 50Vdc	28480	
C21	0160-0127		fxd cer luf +-20% 25Vdc	28480	
C22,23	0160-3070		fxd mica 100pf +-5% 300Vdc	28480	
C24	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C25	0160-2735	1	fxd mica 1000pf +-5% 100Vdc	28480	
C26-32	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C33	0180-0291		fxd TA luf +-10% 35Vdc	56289	150D105X9035A2
CR1-14	1901-0033	14	gen prp 180V 200mA	28480	
Q1-3			NOT ASSIGNED		
Q4	1854-0477	1	NPN SI	04713	2N2222A
R1,2	0698-3455	2	fxd film 261K 1% 1/8W	24546	C4-1/8-T0-2613-F
R3	0757-0435	1	fxd film 3.92K 1% 1/8W	24546	C4-1/8-T0-3921-F
R4	2100-0558	2	trmr 20K 10% 1-turn	28480	
R5	0698-3493	1	fxd film 4.12K 1% 1/8W	24546	C4-1/8-T0-4121-F
R6	0757-0408	1	fxd film 243 1% 1/8W	24546	C4-1/8-T0-243R-F
R7,8	0757-0472	2	fxd film 200K 1% 1/8W	24546	C4-1/8-T0-2003-F
R9	0757-0442	1	fxd film 10k 1% 1/8W	24546	C4-1/8-T0-1002-F
R10	2100-0558		trmr 20K 10% 1-turn	28480	
R11	0683-2025	14	fxd comp 2K 5% 1/4W	01121	CB2025
R12	0683-1025	14	fxd comp 1K 5% 1/4W	01121	CB1025
R13	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R14	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R15-17			NOT ASSIGNED		
R18	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R19	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R20	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R21	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R22-29			NOT ASSIGNED		
R30	0682-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R31	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R32	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R33	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R34-37			NOT ASSIGNED		
R38	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R39	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R40	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R41,42	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R43	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R44	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R45	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R46	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R47	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R48	0686-1815	1	fxd comp 180 5% 1/2W	01121	EB1815
R49	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R50	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025

Table 6-1. 69720A Parts List (cont.)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
R51	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R52	0683-1025		fxd comp 1K 5% 1/4W	01121	CB2025
R53	0683-2725	1	fxd comp 2.7K 5% 1/4W	01121	CB2725
R54,55	0683-6825	3	fxd comp 6.8K 5% 1/4W	01121	CB6825
R56	0698-3558	1	fxd film 4.02K 1% 1/8W	24546	C4-1/8-T0-4021-F
R57	0683-5125	13	fxd comp 5.1K 5% 1/4W	01121	CB5125
R58	0683-1035	6	fxd comp 10K 5% 1/4W	01121	CB1035
R59	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R60	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R61	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R62	0683-6825		fxd comp 6.8K 5% 1/4W	01121	CB6825
R63,64	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R65			NOT ASSIGNED		
R66,67	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R68	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R69-72	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R73,74	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R75-78	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R79	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
S1	3101-2368	1	Switch Rocker 4-1A 0.1A	28480	
T1-13	5080-1924	13	Pulse Transformer	28480	
U1	1820-1746	2	IC BUFFER CMOS INV HEX	04713	MC14049UBCP
U2	1813-0094	1	IC D/A CONVERTER	28480	
U3	1826-0144	1	IC VOLTAGE REGULATOR	04713	MC7805CP
U4	1820-1486	3	IC GATE CMOS AND QUAD	3L585	CD4081BE
U5	1820-1544	7	IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U6	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U7	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U8	1820-1746		IC BUFFER CMOS INV HEX	04713	MC14049UBCP
U9	1826-0528	1	IC OP AMP	27014	LF356BH
U10	1826-0281	1	IC VOLTAGE REGULATOR	04713	MC79L15ACP
U11	1826-0274	1	IC VOLTAGE REGULATOR	04713	MC78L15ACP
U12	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U13			NOT ASSIGNED		
U14	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U15			NOT ASSIGNED		
U16	1820-0949	1	IC GATE CMOS' NAND QUAD	3L585	CD4011UBE
U17			NOT ASSIGNED		
U18	1990-0455	1	IC OPTO-ISOLATOR (6N135)	28480	
U19	1820-1437	2	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U20,21	1820-1438	3	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U22	1820-2257	6	IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U23	1820-1438		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U24	1820-1437		IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U25	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U26	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF

Table 6-1. 69720A Parts List (cont.)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
U27	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U28	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U29	1820-1209	1	IC BUFFER TTL LS NAND QUAD	01295	SN74LS38N
U30	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U31	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U32	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U33	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U34	1820-1416	1	IC SCHMITT-TRIG TTL LS INV HEX	01295	SN74LS14N
U35	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U36,37	1820-2075	2	IC MISC TTL LS	01295	SN74LS245N
U38	1820-2302	1	IC CONTROL CHIP	28480	
Z1,2	1810-0280	2	NETWORK RESISTOR 10K (9)	01121	210A103
			MECHANICAL PARTS		
	69720-80001	1	CARD EXTRACTOR	28480	
	1480-0059	1	..PIN ROLL (.062 IN)	28480	
	5060-2806	1	EXTERNAL EDGE CONNECTOR	28480	
	1200-0552	1	IC SOCKET 40-PIN (U38)	28480	
	1200-0634	1	IC SOCKET (U2)	28480	
	1205-0011	2	HEAT SINK (Q1,2)	28480	
	0340-0453	2	INSULATOR (Q1,2)	28480	
	14703-90001	1	INSTRUCTION SHEET	28480	
	5950-1955	1	OPERATING MANUAL	28480	
	9211-4189	1	SHIPPING CARTON	28480	
	9222-0665	1	ANTI-STATIC BAG	28480	
	7121-0850	1	STATIC WARNING LABEL	28480	

Table 6-2. 69721A Parts List

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
C1	0180-0291	4	fxd TA luf +-10% 35Vdc	56289	150D105X9035A2
C2-4	0160-0127	12	fxd cer luf +-20% 25Vdc	28480	
C5	0150-0093	1	fxd cer .01uf +80-20% 100Vdc	28480	
C6	0160-0949	1	fxd mica 68pf +-5% 300Vdc	28480	
C7,8	0160-0127		fxd cer luf +-20% 25Vdc	28480	
C9,10	0180-0291		fxd TA luf +-10% 35Vdc	56289	150D105X9035A2
C11	0160-4457	1	fxd mica 51pf +-5% 300Vdc	28480	
C12-17	0160-0127		fxd cer luf +-20% 25Vdc	28480	
C18,19	0160-3070	4	fxd mica 100pf +-5% 300Vdc	28480	
C20	0160-4722	9	fxd cer 0.luf +80-20% 50Vdc	28480	
C21	0160-0127		fxd cer luf +-20% 25Vdc	28480	
C22,23	0160-3070		fxd mica 100pf +-5% 300Vdc	28480	
C24	0160-4722		fxd cer 0.luf +80-20% 50Vdc	28480	
C25	0160-2735	1	fxd mica 1000pf +-5% 100Vdc	28480	
C26-32	0160-4722		fxd cer 0.luf +80-20% 50Vdc	28480	
C33	0180-0291		fxd TA luf +-10% 35Vdc	56289	150D105X9035A2
CR1-14	1901-0033	14	gen prp 180V 200mA	28480	
Q1	1853-0037	1	PNP SI	28480	
Q2	1854-0271	1	NPN SI	28480	
Q3			NOT ASSIGNED		
Q4	1854-0477	1	NPN SI	04713	2N2222A
R1,2	0698-3455	2	fxd film 261K 1% 1/8W	24546	C4-1/8-T0-2613-F
R3	0757-0435	1	fxd film 3.92K 1% 1/8W	24546	C4-1/8-T0-3921-F
R4	2100-0558	2	trmr 20K 10% 1-turn	28480	
R5	0698-3493	1	fxd film 4.12K 1% 1/8W	24546	C4-1/8-T0-4121-F
R6	0757-0408	1	fxd film 243 1% 1/8W	24546	C4-1/8-T0-243R-F
R7,8	0757-0472	3	fxd film 200K 1% 1/8W	24546	C4-1/8-T0-2003-F
R9	0757-0442	1	fxd film 10k 1% 1/8W	24546	C4-1/8-T0-1002-F
R10	2100-0558		trmr 20K 10% 1-turn	28480	
R11	0683-2025	14	fxd comp 2K 5% 1/4W	01121	CB2025
R12	0683-1025	15	fxd comp 1K 5% 1/4W	01121	CB1025
R13	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R14	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R15	2100-3252	1	trmr 5K 10% 1-turn	28480	
R16	0757-0440	1	fxd film 7.5K 1% 1/8W	24546	C4-1/8-T0-7501-F
R17	2100-3214	1	trmr 100K 10% 1-turn	28480	
R18	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R19	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R20	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R21	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R22	0698-4444	1	fxd film 4.87K 1% 1/8W	24546	C4-1/8-T0-4871-F
R23	0699-0291	1	fxd film 101 0.1% 0.225W	28480	
R24,25	0699-0762	2	fxd film 100K .01% 0.3W	28480	
R26	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R27,28	0683-5115	2	fxd comp 510 5% 1/4W	01121	CB5115
R29	0757-0472		fxd film 200K 1% 1/8W	24546	C4-1/8-T0-2003-F
R30	0682-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R31	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R32	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R33	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R34	0699-0289	2	fxd film 10K .01% 0.15W	28480	
R35,36	0698-3950	2	fxd film 2K .01% 0.15W	28480	
R37	0699-0289		fxd film 10K .01% 0.15W	28480	

Table 6-2. 69721A Parts List (cont.)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
R38	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R39	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R40	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R41,42	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R43	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R44	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R45	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R46	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R47	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R48	0686-1815	1	fxd comp 180 5% 1/2W	01121	EB1815
R49	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R50	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R51	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R52	0683-1025		fxd comp 1K 5% 1/4W	01121	CB2025
R53	0683-2725	1	fxd comp 2.7K 5% 1/4W	01121	CB2725
R54,55	0683-6825	3	fxd comp 6.8K 5% 1/4W	01121	CB6825
R56	0698-3558	1	fxd film 4.02K 1% 1/8W	24546	C4-1/8-TO-4021-F
R57	0683-5125	13	fxd comp 5.1K 5% 1/4W	01121	CB5125
R58	0683-1035	6	fxd comp 10K 5% 1/4W	01121	CB1035
R59	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R60	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R61	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R62	0683-6825		fxd comp 6.8K 5% 1/4W	01121	CB6825
R63,64	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R65			NOT ASSIGNED		
R66,67	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R68	0683-2025		fxd comp 2K 5% 1/4W	01121	CB2025
R69-72	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R73,74	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R75-78	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R79	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
S1	3101-2368	1	Switch Rocker 4-1A 0.1A	28480	
T1-13	5080-1924	13	Pulse Transformer	28480	
U1	1820-1746	2	IC BUFFER CMOS INV HEX	04713	MC14049UBCP
U2	1813-0094	1	IC D/A CONVERTER	28480	
U3	1826-0144	1	IC VOLTAGE REGULATOR	04713	MC7805CP
U4	1820-1486	3	IC GATE CMOS AND QUAD	3L585	CD4081BE
U5	1820-1544	7	IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U6	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U7	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U8	1820-1746		IC BUFFER CMOS INV HEX	04713	MC14049UBCP
U9	1826-0528	2	IC OP AMP	27014	LF356BH
U10	1826-0281	1	IC VOLTAGE REGULATOR	04713	MC79L15ACP
U11	1826-0274	1	IC VOLTAGE REGULATOR	04713	MC78L15ACP
U12	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U13	1826-0672	2	IC OP AMP	24355	AD518KH
U14	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U15	1826-0528		IC OP AMP	27014	LF356BH
U16	1820-0949	1	IC GATE CMOS NAND QUAD	3L585	CD4011UBE
U17	1826-0672		IC OP AMP	24355	AD518KH

Table 6-2. 69721A Parts List (cont.)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
U18	1990-0455	1	IC OPTO-ISOLATOR (6N135)	28480	
U19	1820-1437	2	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U20,21	1820-1438	3	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U22	1820-2257	6	IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U23	1820-1438		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U24	1820-1437		IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U25	1820-2257		IC BUFFER CMOS BUD DRVR HEX	04713	MC14503BCP
U26	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U27	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U28	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U29	1820-1209	1	IC BUFFER TTL LS NAND QUAD	01295	SN74LS38N
U30	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U31	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U32	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U33	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U34	1820-1416		IC SCHMITT-TRIG TTL LS INV HEX	01295	SN74LS14N
U35	1820-2257		IC BUFFER CMOS BUS DRVR HEX	04713	MC14503BCP
U36,37	1820-2075	2	IC MISC TTL LS	01295	SN74LS245N
U38	1820-2302	1	IC CONTROL CHIP	28480	
Z1,2	1810-0280	2	NETWORK RESISTOR 10K (9)	01121	210A103
			MECHANICAL PARTS		
	69721-80001	1	CARD EXTRACTOR	28480	
	1480-0059	1	..PIN ROLL (.062 IN)	28480	
	5060-2806	1	EXTERNAL EDGE CONNECTOR	28480	
	1200-0552	1	IC SOCKET 40-PIN (U38)	28480	
	1200-0634	1	IC SOCKET (U2)	28480	
	1205-0011	2	HEAT SINK (Q1,2)	28480	
	0340-0453	2	INSULATOR (Q1,2)	28480	
	14703-90001	1	INSTRUCTION SHEET	28480	
	5950-1955	1	OPERATING MANUAL		
	9211-4189	1	SHIPPING CARTON	28480	
	9222-0665	1	ANTI-STATIC BAG	28480	
	7121-0850	1	STATIC WARNING LABEL	28480	

Table 6-2. 69721A Parts List (cont.)

PARTS LIST FOR EXTERNAL CONNECTOR ASSEMBLY* (HP PART NO. 5060-2806)

HP PART NO	INDEX NO	DESCRIPTION	QTY
1251-6307		HOOD ASSEMBLY**	
	1	**STRAIN RELIEF	
	2	**CABLE CLAMPS	
	3	**RIGHT HOOD ASSEMBLY	
	4	**LEFT HOOD ASSEMBLY	
	5	**SCREW, 7/16 INCH	
	6	**SCREWS, 11/16 INCH	
1251-6059	7	CONNECTOR PIN HOUSING	1
1251-6056	8	CONNECTOR KEY	1
1251-6183	9	SOLDER PINS, PLATED	45
1251-6380	10	SPRINGS, RETAINING	6

* CAN BE ORDERED AS MODEL 14703A, CARD EDGE CONNECTOR
** ITEM 1251-6307 CONSISTS OF INDEX ITEMS 1 THROUGH 6.

Table 6-4. Manufacturer's Federal Supply Codes

01121	Allen-Bradley Co.	Milwaukee, WI
01295	Texas Instruments, Inc. Semiconductor-Components Division	Dallas, TX
04713	Motorola Semiconductor Products, Inc.	Phoenix, AZ
24355	Analog Devices, Inc.	Norwood, MA
24546	Corning Glass Works	Bradford, PA
27014	National Semiconductor Corp.	Santa Clara, CA
28480	Hewlett-Packard Co.	Palo Alto, CA
3L585	RCA Corp. Solid State Division	Somerville, NJ
56289	Sprague Electric Co.	North Adams, MA

Section VII
DIAGRAMS

7-1 COMPONENT LOCATION

7-2 Figure 7-1 shows the D/A card and identifies the various test points and location of components shown in the functional schematic diagram, Figure 7-2.

7-3 SCHEMATIC DIAGRAM

7-4 Figure 7-2 is the schematic diagram of the D/A card. The schematic diagram uses the ANSI Y32.14 and IEEE standard 91 for the representation of logic elements. A brief summary of this notation is given in Table 7-1.

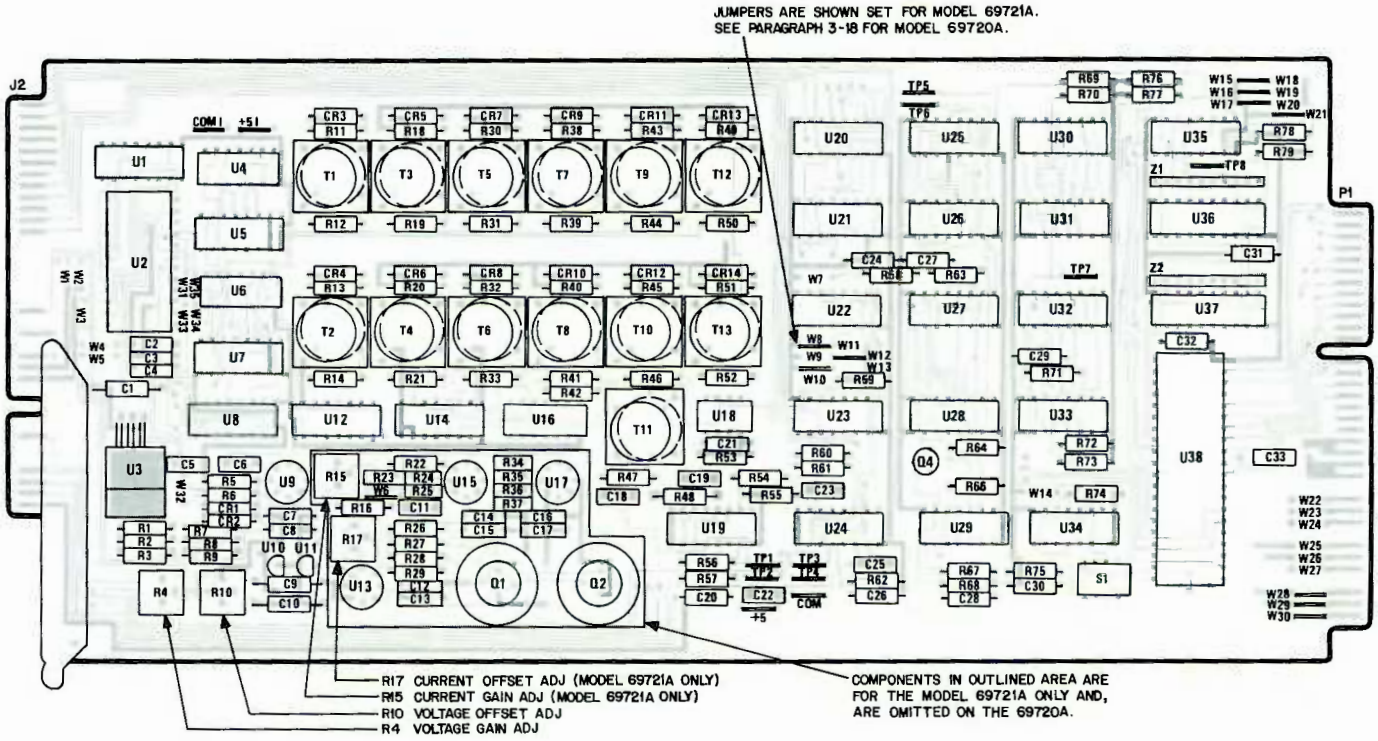


Figure 7-1. Component Locations

Table 7-1. Abbreviated List of ANSI Y32.14 Schematic Symbols

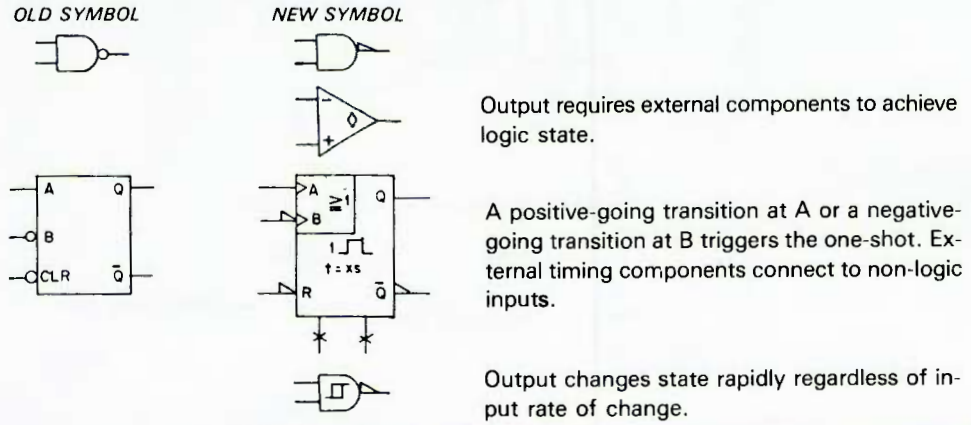
Definitions:

High = more positive
Low = less positive

True = logical "1" state
False = logical "0" state

Indicator and Qualifier Symbols

Σ	Adder
≥	OR FUNCTION
= 1	exclusive OR function
&	AND function
▽	3-state output
EN	enable Device output
◺	(polarity indicator, shown outside logic symbol) Any marked input or output is active low; any unmarked input or output is active high.
▷	(dynamic indicator) Any marked input is edge-triggered, ie, active during transition between states; any marked input is level sensitive.
⊓	(Schmitt trigger) indicates that hysteresis exists in device.
*	(non-logic indicator) Any marked input or output does not carry logic information.)
◇	open-collector or open emitter output
1 ⊓	non-retriggerable monstable (one-shot) multivibrator
⊓	Retriggerable monostable multivibrator
t = xSec	indicates pulse width (usually determined by external RC network)
G	gate input (a number following G indicates which inputs are gated);also, astable element
C	control input (clock)
R	reset (clear)
S	set (preset)
D	data input to storage element
▷	buffered element with extra output capacity



Appendix A
BACKDATING

A-1 This section contains information on how to convert the basic Model 69720A/69721A manual to a manual usable for early model D/A cards. Check Tables A-1 and A-2 for your card's serial number and enter any listed change(s) in the manual.

Table A-1. Changes for 69720A Voltage D/A cards.

SERIAL		MAKE CHANGE
Prefix	Number	
1909A	00101-00450	1

Table A-2. Changes for 69721A Current D/A Cards

SERIAL		MAKE CHANGE
Prefix	Number	
1918A	00101-00155	1,2,3
2030A	00156-00215	2,3
2052	00216-00415	3

CHANGE 1

a. Delete Jumper options W31 through W35 and connect U2 pin 17 to U2 pin 15. Also, connect U2 pin 19 to R6.

b. Make the following changes to the parts list in Section VI.
   -Add Q3 XSTR NPN 2N2222A, HP Part No. 1854-0477
   -Add R65 RES 5.1K 5% .25W, HP Part No. 0683-5125
   -Change U29 to IC SN74LS03, HP Part No. 1820-1198

c. The schematic in Section VII, Figure 7-2 should be modified as shown in Figure A-1.

CHANGE 2

On schematic and in parts list for the 69721A card, change resistors R24, R25 to 10K, .01% .15W, HP Part No. 0699-0289.

CHANGE 3

On schematic and parts list for the 69721A card, change capacitors C20, C24,C26-C32 to 1μF 20% 25 V HP Part No. 0160-0127.

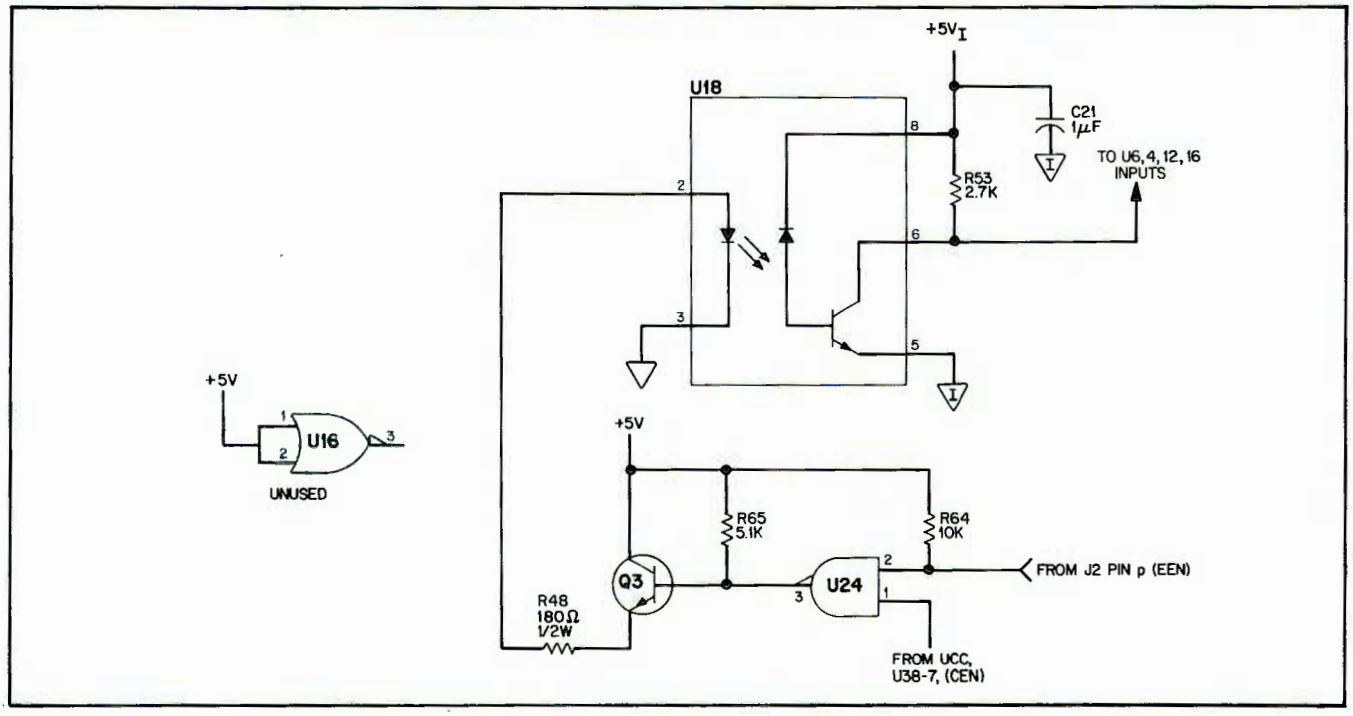


Figure A-1. Enable Circuit for Change 1

Appendix A
BACKDATING

A-1 This section contains information on how to convert the basic Model 69720A/69721A manual to a manual usable for early model D/A cards. Check Tables A-1 and A-2 for your card's serial number and enter any listed change(s) in the manual.

Table A-1. Changes for 69720A Voltage D/A cards.

SERIAL		MAKE CHANGE
Prefix	Number	
1909A	00101-00450	1

Table A-2. Changes for 69721A Current D/A Cards

SERIAL		MAKE CHANGE
Prefix	Number	
1918A	00101-00155	1,2,3
2030A	00156-00215	2,3
2052	00216-00415	3

CHANGE 1

a. Delete Jumper options W31 through W35 and connect U2 pin 17 to U2 pin 15. Also, connect U2 pin 19 to R6.

b. Make the following changes to the parts list in Section VI.
   -Add Q3 XSTR NPN 2N2222A, HP Part No. 1854-0477
   -Add R65 RES 5.1K 5% .25W, HP Part No. 0683-5125
   -Change U29 to IC SN74LS03, HP Part No. 1820-1198

c. The schematic in Section VII, Figure 7-2 should be modified as shown in Figure A-1.

CHANGE 2

On schematic and in parts list for the 69721A card, change resistors R24, R25 to 10K, .01% .15W, HP Part No. 0699-0289.

CHANGE 3

On schematic and parts list for the 69721A card, change capacitors C20, C24,C26-C32 to 1μF 20% 25 V HP Part No. 0160-0127.

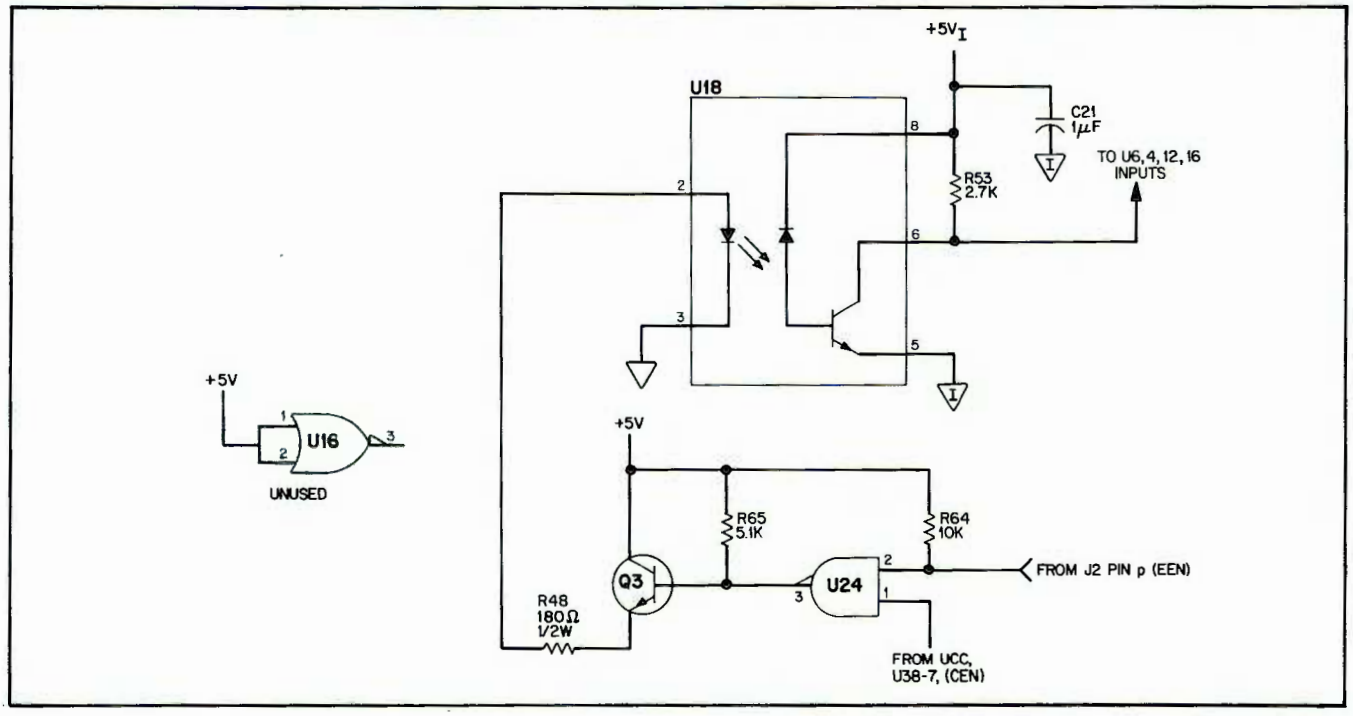
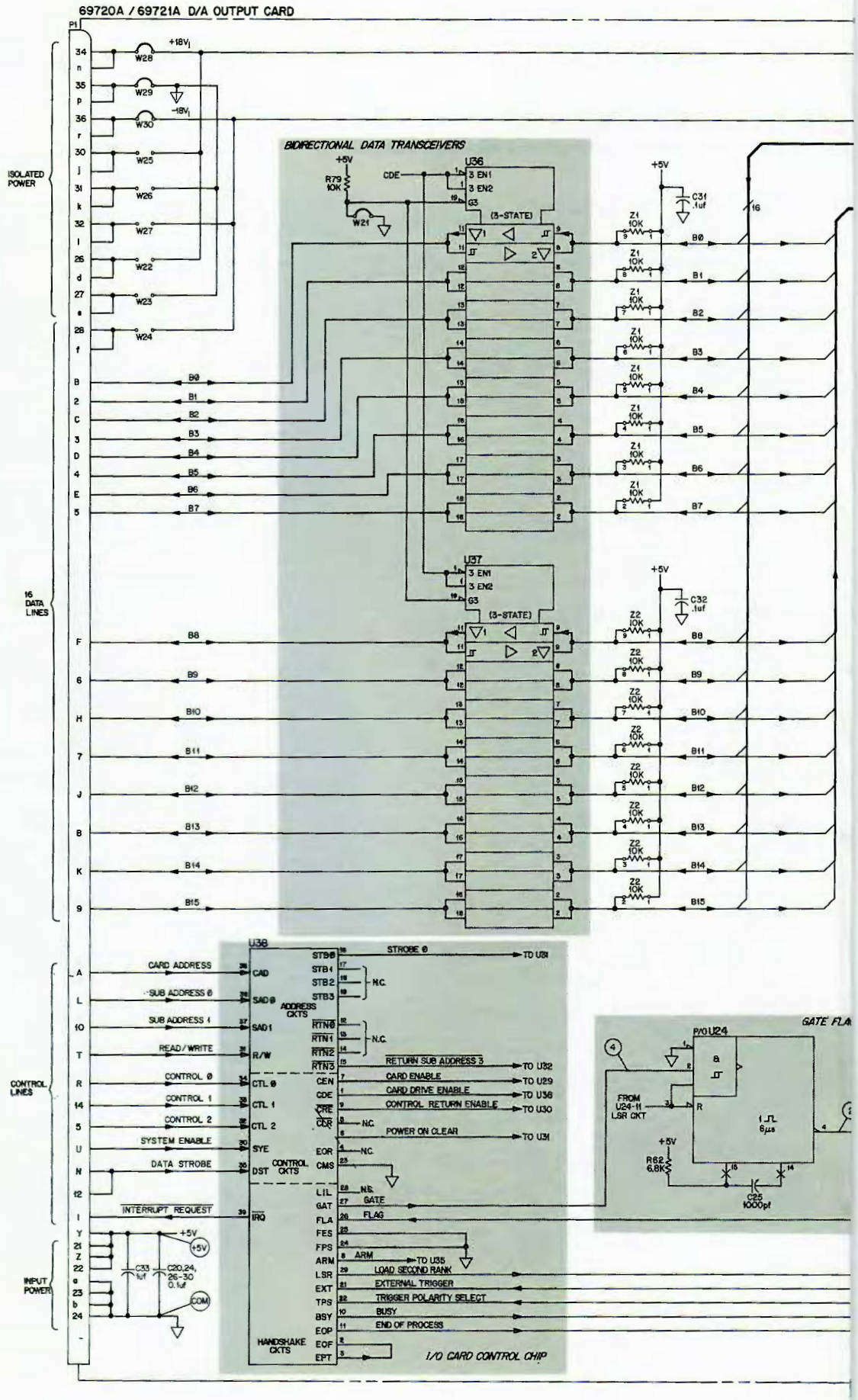
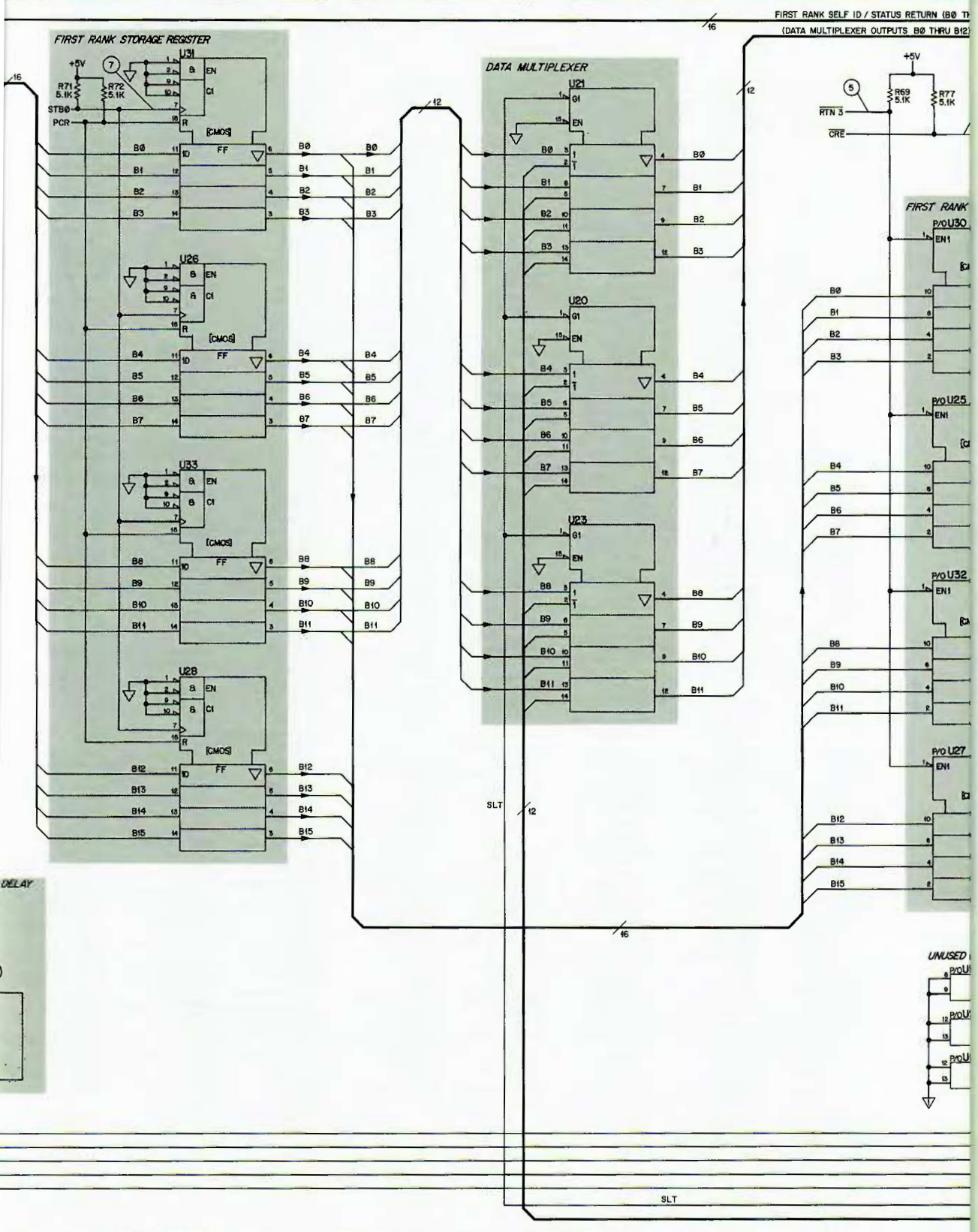
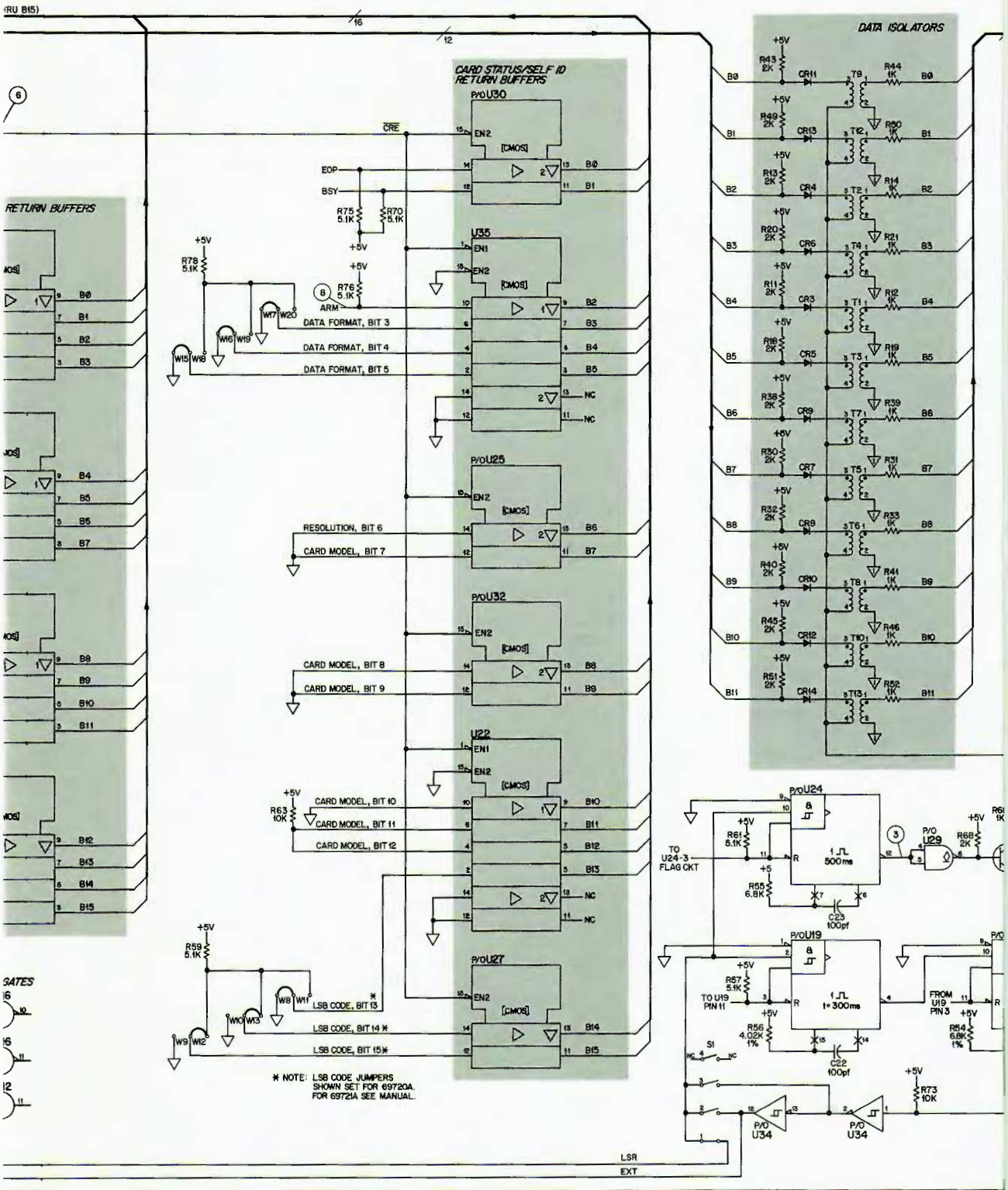
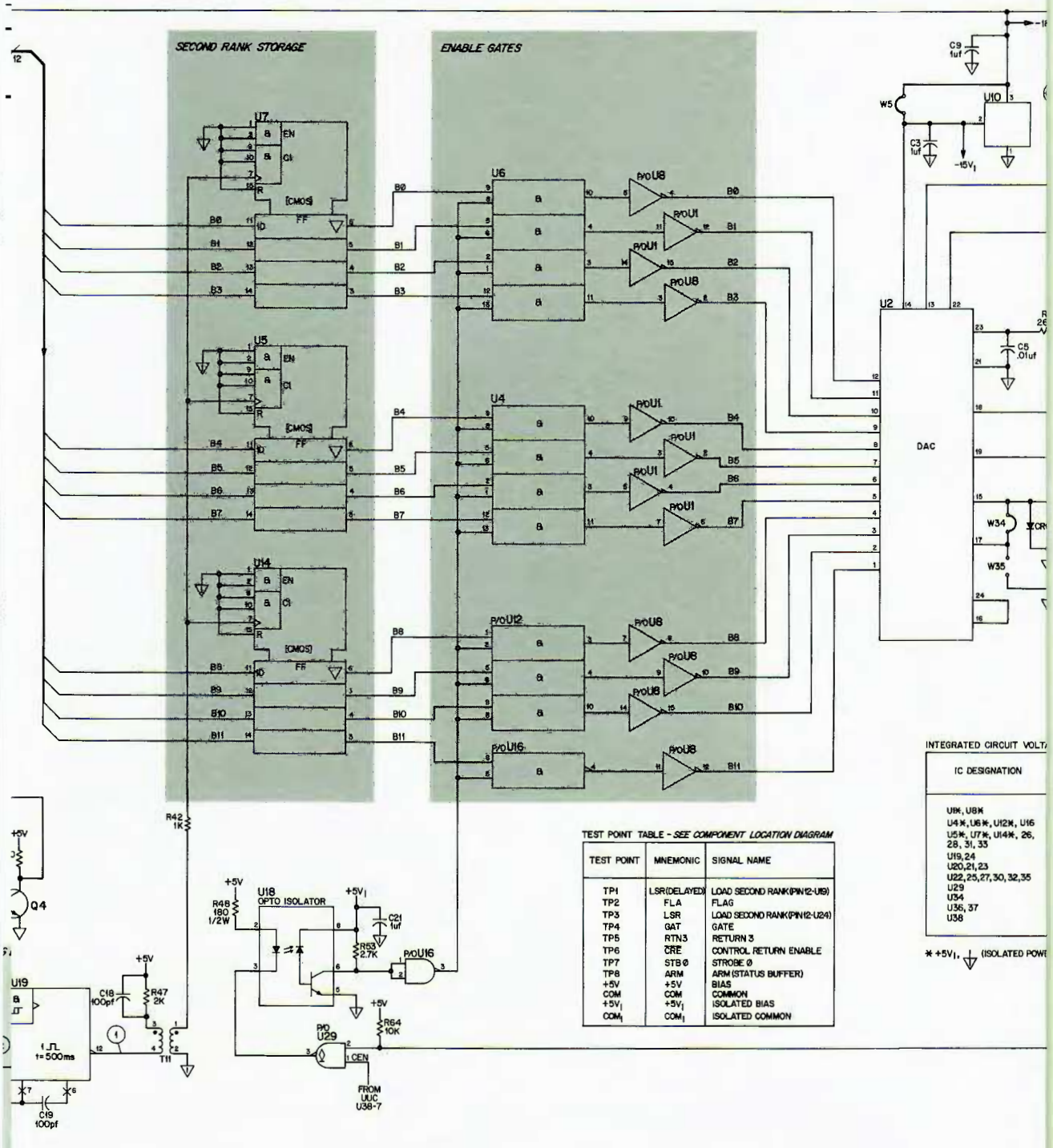


Figure A-1. Enable Circuit for Change 1









TEST POINT TABLE - *SEE COMPONENT LOCATION DIAGRAM*

TEST POINT	MNEMONIC	SIGNAL NAME
TP1	LSR(DELAYED)	LOAD SECOND RANK(PIN12-U19)
TP2	FLA	FLAG
TP3	LSR	LOAD SECOND RANK(PIN12-U24)
TP4	GAT	GATE
TP5	RTN3	RETURN 3
TP6	$\overline{CRE}$	CONTROL RETURN ENABLE
TP7	STB Ø	STROBE Ø
TP8	ARM	ARM (STATUS BUFFER)
+5V	+5V	BIAS
COM	COM	COMMON
$+5V_I$	$+5V_I$	ISOLATED BIAS
COM_I	COM_I	ISOLATED COMMON

INTEGRATED CIRCUIT VOLT

IC DESIGNATION
U1*, U8*
U4*, U6*, U12*, U16
U5*, U7*, U14*, 26, 28, 31, 33
U19,24
U20,21,23
U22,25,27,30,32,35
U29
U34
U36, 37
U38

* $+5V_I$, (ISOLATED POWE

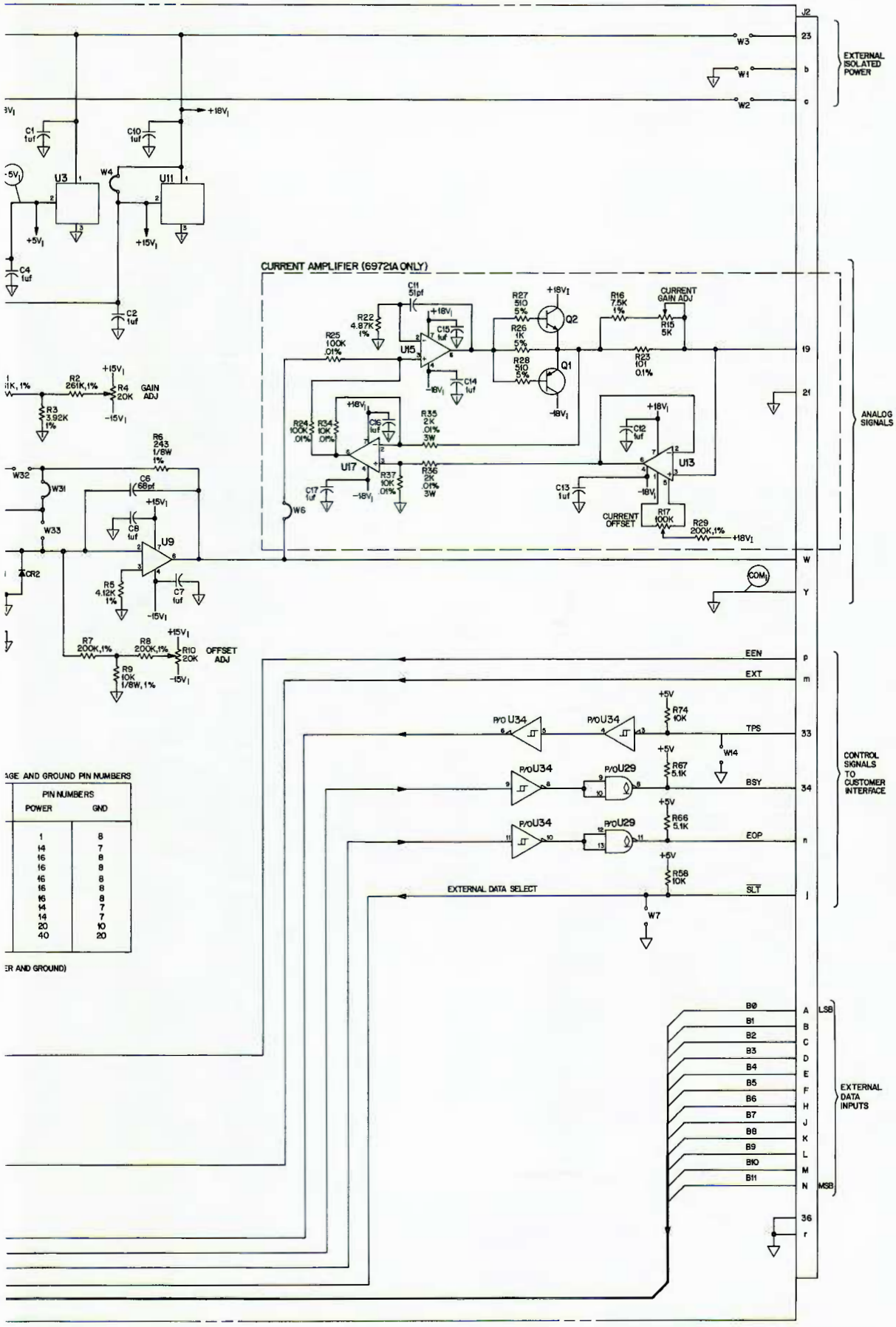


Figure 7-2. D/A Converter Card, Schematic Diagram