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Agilent ParBERT 81250
Parallel Bit Error Ratio Tester

Product Overview
Version 5.66

The only Parallel Bit Error Ratio Solution for Testing at:

- **675 Mb/s**
- **1.65 Gb/s**
- **2.7 Gb/s**
- **3.35 Gb/s**
- **7 Gb/s**
- **10.8 Gb/s**
- **13.5 Gb/s**
- **45 Gb/s**

Agilent Technologies

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Agilent ParBERT 81250 Overview

Agilent ParBERT 81250 is a modular parallel electrical and optical bit error ratio (BER) test platform, which works up to 45 Gb/s. The ParBERT 81250 platform comprises modules that work at 675 Mb/s, 1.65 Gb/s, 2.7 Gb/s, 3.35 Gb/s, 7 Gb/s, 10.8 Gb/s, 13.5 Gb/s and 45 Gb/s. The system generates pseudo random word sequences (PRWS), standard pseudo random binary sequences (PRBS) and user-defined patterns on parallel lines. You can analyze bit error ratios with user defined patterns, PRBS/PRWS or mixed data (a combination of userdefined patterns and PRBS).

ParBERT 81250 is a perfect fit for parallel-to-serial, serial-to-parallel, serial-to-serial and multiple serial BER test. Examples are multiplexer and demultiplexer (Mux/Demux) - or SerDes (serializer/deserializer) - testing used in telecom and storage area network (SAN) ICs, multiple transmitter and receiver testing in manufacturing, amplifiers as well as 10GbE and forward error correction (FEC) device testing.

It is also an ideal extension for the high-speed channels of an IC-tester.

ParBERT 81250 also provides data and control signals for the DUT if required.

The ParBERT software suite is a ready-to-use package, which offers different levels of measurement analysis:

1. Fast pass/fail measurements ideal for production
2. Output timing measurements provide results for setup & hold times, skew between channels, phase margins, detailed jitter results (RJ/DJ/TJ), and eye opening specification results
3. Output level measurements provide results for high/low levels, amplitudes, threshold margins and Q-factor analysis
4. Graphical results for detailed root cause analysis - see trends clearly and fast, e.g. color and contour plots.
5. “Fast Eye” mask measurement.
6. Comprehensive “Jitter” measurement applications, e.g spectral decomposition of jitter.
7. “Eye Opening” measurement applications

Agilent ParBERT 81250 is particularly suitable for the following applications:

1. 10GbE device testing
2. Multiplexer and demultiplexer testing
   - OC-768 device testing: You can test 16:1 and 4:1 40G devices using the ParBERT 81250 45G and either 3.3 Gb/s or 10.8 Gb/s modules
   - OC-192 device testing: the ParBERT 81250 10.8 Gb/s modules enable testing of the serial high-speed side of Muxes/DeMuxes. Combined with 675 Mb/s, 1.6 Gb/s, 2.7 Gb/s or 3.3 Gb/s modules you can test both sides of multiplexers/demultiplexers
   - OC-48 device testing
3. Characterization of SAN ICs
4. Manufacturing test of multiple transmitters, receivers, transceivers and amplifiers
5. FEC device test

For more information on these applications, please see product number for related literature mentioned on the back page. This document focuses on the ParBERT platform.

The Ideal Solution for High-Speed Parallel Bit-Error-Ratio (BER) Tests

Selection guide for ParBERT 81250 platform generator, analyzer, front-ends and modules

Data rate range	333.334 kb/s – 675 Mb/s (1)	333.334 Mb/s – 1.65 Gb/s	333.334 Mb/s – 2.7 Gb/s	20.834 MHz – 3.35 Mb/s (1)	620 Mb/s – 7 Gb/s	620 Mb/s – 13.5 Gb/s
Technology addressed	TTL, PECL, LVDS	CML, PECL,ECL, LVDS,SSTL-2	CML, PECL,ECL, LVDS,SSTL-2	CML, PECL,ECL, LVDS,SSTL-2	LVDS, CML, PECL, ECL, CMOS	LVDS, CML, PECL, ECL,CMOS
Memory depth expected & acquisition	PRBS/PRWS/ 2 Mb memory	PRBS/PRWS/ 8 Mb memory	PRBS/PRWS/ 8 Mb memory	PRBS/PRWS/ 16 Mb memory	PRBS/PRWS/ 64 Mb memory	PRBS/PRWS/ 64 Mb memory
Generator	**Front-end E4838A**	**Front-end E4864A**	**Front-end E4862A**	**Front-end E4862B**	**Modules N4874A**	**Modules N4872A**
Transition times (20% - 80%)	0.5 to 4.5 ns– (10% 90%) var.	90 ps typ	90 ps typ	< 75 ps	< 20 ps	< 20 ps
Amplitude/ resolution	0.1 – 3.5 Vpp 10 mV	0.05 – 1.8 Vpp 10 mV	0.05 – 1.8 Vpp 10 mV	0.05 – 1.8 Vpp 10 mV	0.1 – 1.8 Vpp 5 mV	0.1 – 1.8 Vpp 5 mV
Window	-2.2 to +4.4 V	-2.0 to +3.0 V	-2.0 to +3.0 V	-2.0 to +3.5 V	-2.0 to +3.0 V	-2.0 to +3.0 V
Analyzer	**Front-end E4835A**	**Front-end E4865A**	**Front-end E4863A**	**Front-end E4863B**	**Module N4875A**	**Module N4873A**
Maximum input voltage range	0 to +5 V -2 to +3 V	-2 V to +1 V -1 V to +2 V 0 V to 3 V	-2 V to +1 V -1 V to +2 V 0 V to 3 V	-2 V to +1 V -1 V to +2 V 0 V to 3 V	-2 V to +3 2 V window	-2 V to +3 2 V window
Input sensitivity	50 mV typ diff	50 mV typ	50 mV typ	< 50 mV	< 50 mV	< 50 mV
Delay resolution	2 ps	1 ps	1 ps	1 ps	100 fs	100 fs
Data module	**E4832A**	**E4861A**	**E4861A**	**E4861B**	–	–
CentralClk	Slots / frame	Slots / frame	Slots / frame	Slots / frame	Slots / frame	Slots / frame
E4805B/8A/9A	11/11/10	11/11/–	11/11/–	–/11/10	–/–/10	–/–/10
Channels/slot	4	2	2	2	1	1
Channels/frame	44	22	22	22	10	10
Base VXI frame +	$37,000.00	$37,000.00	$37,000.00	$44,000.00	$52,000.00	$52,000.00
Generator/channel	$3,100.00	$7,300.00	$9,100.00	$13,300.00	$38,300.00	$56,100.00
Analyzer/channel	$4,500.00	$8,500.00	$10,900.00	$16,000.00	$38,300.00	$56,100.00

[1] RZ support

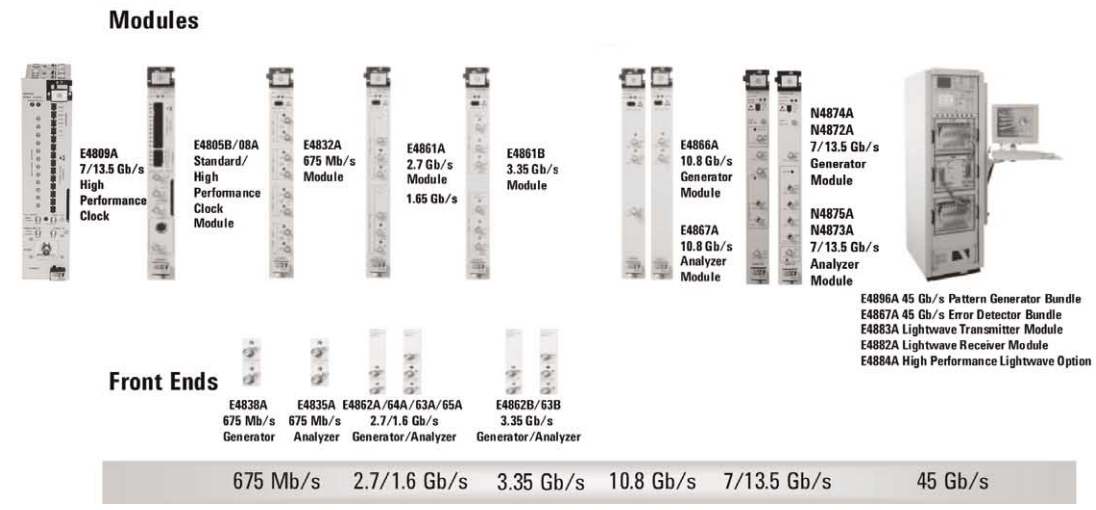


Figure 1. ParBERT product family

ParBERT 81250 key features & benefits

Table 1. Features and benefits

Features	Benefits
Modular, flexible and scalable platform architecture • Up to 128 channels @ 675 Mb/s • Up to 64 channels @ 3.35 Gb/s, 2.7 Gb/s • Up to 30 channels @13.5 Gb/s, 10.8 Gb/s, 7 Gb/s	• Grows with customer's test and application needs • Covers a wide range of technologies and applications
Generator and analyzer modules available from 675 Mb/s up to 45 Gb/s	Allows system configurations perfectly meeting customer's application needs
Mix of channels (generator/analyzer) and speed classes	Provides unique flexibility to test complex devices with many channels and/or frequencies, e.g., serial bus applications, Mux/Demux (SerDes), FEC
Generate pseudo random word sequences (PRWS) and standard PRBS up to 2^{31}-1; analyze bit error ratios with user- defined data, PRBS or mixed data from parallel ports	Perform parallel BER measurements - ideal for Mux/Demux applications
Generate and analyze single-ended and differential signals - including true differential	• Test logic technologies e.g. LVDS, ECL, PECL, SSTL-2 • Generate the necessary signals to perform margin tests, emulate frequency and level changes and stress your device as far as possible
Data generation and analysis with sequencing and looping	• Generate complex sequences that contain memory-based (up to 64 Mbit) and/or PRBS/PRWS data • Generate data packets with header and payload • React to control signals from the DUT
Auto phase & auto delay alignment	• Auto alignment of expected data with incoming data • Save time as you do not need to find the correct sample point manually - typically takes just 100 ms
Each generator or analyzer channel has independent programmable control of voltage levels and timing delay	Allows device characterization for a wide range of technologies/applications in the semiconductor and communication industry
Interrupt-free change of analyzer delay/generator delay (13.5 Gb/s, 7 Gb/s and 3.35 Gb/s; other speed classes generator only)	Continuous running signals for measurements where changing analyzer/generator delay is necessary
Jitter modulation (13.5 Gb/s, 7 Gb/s and 3.35 Gb/s)	Allows jitter tolerance testing to be performed
Variable cross (13.5 Gb/s, 7 Gb/s and 3.35 Gb/s)	Provides real-world stress
Windows XP®/Windows 2000® operating systems	Popular industry standard operating system
Plug and play drivers	Allows remote access and simplifies remote program development
Measurement suite	• DUT output timing measurement - bathtub curve with jitter analysis (RJ/DJ separation), skew between channels, setup and hold times • Output level measurement - amplitude information, high/low level and Q-factor • Eye opening measurement - color and contour plots • Fast eye mask measurement - automatic threshold adjust, fast and efficient insights for manufacturing test • Comprehensive BER measurement - actual and accumulated BER, errors of ones and zeros, total bits transferred and file capturing for post-processing analysis. • Spectral jitter

Key features

Perform parallel BER measurements up to 13.5 Gb/s

ParBERT 81250 makes testing of Mux/Demux (serializer/deserializer) devices easier. Only ParBERT 81250 is able to generate pseudo-random-word sequences (PRWS) on the parallel side and analyze bit-error ratios with user-defined patterns, PRBS up to $2^{31} - 1$ or both combined.

PRBS/PRWS and memory capability

The polynomial $2^n - 1$, the PRBS algorithm and the parallel bus width define PRWS. The bits of the PRWS are assigned to parallel lines and are then multiplexed to form a PRBS (see Figure 3).

Auto phase and auto delay alignment

As the latency from the input to the output is often not known exactly, or it is not deterministic, synchronization between incoming data and outgoing data has to be carried out. ParBERT 81250 has three capabilities to synchronize/align the incoming data automatically (see Figures 4 and 5):

1) Data shift bit-by-bit if PRBS is used
2) Detect word if user-defined patterns are used
3) Moving of the sampling point delay of the analyzer up to 10 ns without stopping the instrument. Moving of the sampling point delay can also be used in addition to the alignment of data patterns (1 and 2) to refine the synchronization.

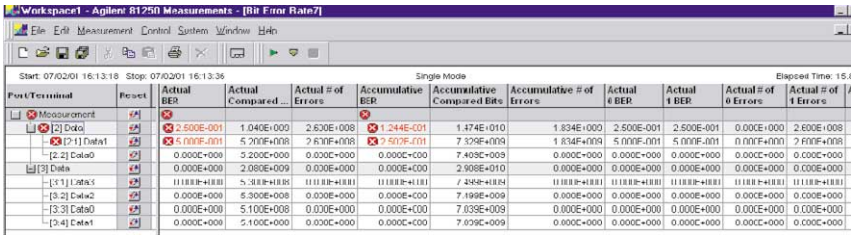


Figure 2. BER results screen

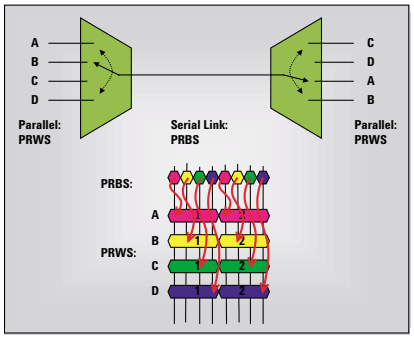


Figure 3. MUX/DEMUX application: relationship between PRBS and PRWS

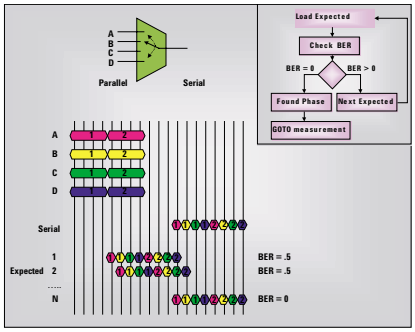


Figure 4. Mechanism of auto-phase and auto-delay assignment

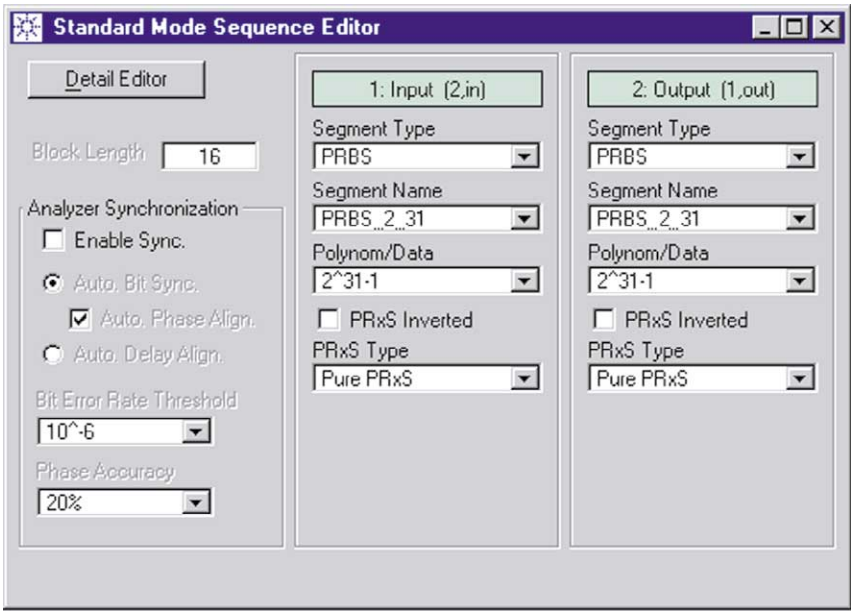


Figure 5. Standard view when choosing PRBS/PRWS patterns and data synchronization mode

Interrupt-free change of analyzer delay

The analyzer delay can be changed ±1 period while the instrument is running without causing it to stop (see Figure 6).
The 13.5 Gb/s, 7 Gb/s and 3.35 Gb/s modules can do this on both the analyzer and generator.

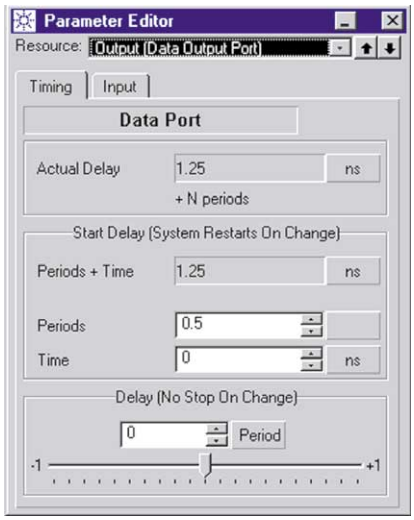


Figure 6. Parameter editor for analyzer timing

With the two clock groups any frequency ratio m/n, n = 1,2,...,256 is possible. The 'application examples' show some 'two-clock system' configurations.

Multiple frequencies

The modular architecture of ParBERT allows the use of different channels at different speeds. Therefore it is possible to combine channels of different speed classes in one ParBERT system. A ParBERT system can be configured with one or more clock groups. Each clock group is controlled from one clock module. Within one clock group (one clock module controls a group of channels) a frequency ratio of 2^n, n = 1,2,....10 is possible, see Figure 7.

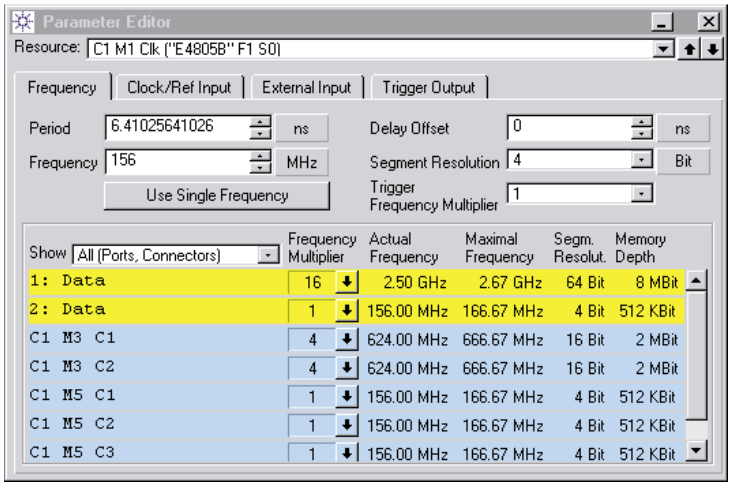


Figure 7. Parameter editor for setting multiple frequencies in one system

Platform description

The fundamental idea of the ParBERT 81250 product structure is to offer an instrument, which meets your measurement needs exactly. The ParBERT modularity includes modules and front-ends. At 13.5 Gb/s, 10.8 Gb/s and 7 Gb/s, there are dedicated modules for generators and analyzers. At 3.35 Gb/s, 2.7 Gb/s, 1.6 Gb/s and 675 Mb/s the modules carry 2/4 front-ends.

Front-ends determine the speed and input/output capabilities of your instrument. A mix of front-ends is possible within the modules. The front-ends are placed in **data modules**, which are responsible for sequencing, generating and analysing of data patterns including PRBS/PRWS. These modules, plus at least one **clock module**, which generates the common system frequency of the instrument, are installed in the mainframe.

The VXI frame offers 13 slots. Assuming the use of the FireWire interface and one clock module in place, the mainframe can hold up to 10 channels at 13.5 Gb/s and 7 Gb/s, 11 channels at the data rate of 10.8 Gb/s, 22 channels at 3.35 Gb/s, 2.7 Gb/s and 1.65 Gb/s or 44 channels at 675 Mb/s. If more channels are needed there is the possibility of adding up to two expander frames to reach the maximum number of channels within one clock group. Additional clock modules are needed to set up systems which work with different clock speeds that are not divisible or multipliable by the factors 2, 4, 8, 16 (if E4832A is used) and 2 and 4 (if E4861A is used). For example, for testing 1:7 or 1:10 Mux/ Demux devices two clock modules are required. Please check the application examples within the next chapter. The **ParBERT 81250 software suite** runs on an external PC, or a laptop, which is connected to the system via an IEEE 1394 PC link to VXI.

The operating system is MS Windows® 2000 or XP.
The ParBERT 81250 software suite consists of:

- Graphical user interface
- Measurement suite
- Software tools (10GbE tool, SONET/SDH frame generator
- VXI *Plug&Play* driver

At runtime the software consists of several processes. The firmware server controls the hardware and is the link between the graphical user interface and the hardware modules. The measurement software or any custom remote program can communicate with the firmware server. Remote access is established either by using the *Plug&Play* drivers from Agilent VEE Pro or from a C/C++/Visual Basic program or by a SCPI based language via GPIB. This allows the building of a customized VXI system including other standard VXI modules.

Table 2

	675 Mb/s	**1.65 Gb/s 2.7 Gb/s, 3.35 Gb/s**	**10.8 Gb/s**	**13.5 Gb/s, 7 Gb/s**
Data rate range	333.3 Kb/s .. 675 Mb/s	333.4 Mb/s .. 2.7 Gb/s 20.8 Mb/s .. 3.35 Gb/s	9.5 .. 10.8 Gb/s	620 Mb/s .. 7 Gb/s 620 Mb/s .. 13.5 Gb/s
Number of channels within 1 frame/+ 2 expander frames with ext. PC	44/132	22/66	11/33	10/30
inputs/outputs	differential & single ended	differential & single ended	differential & single ended	differential & single ended
Data capability	PRBS/PRWS/ 2 MB memory	PRBS/PRWS/ 8/16 MB memory	PRBS/PRWS/ 32 MB memory	PRBS/PRWS/ 64 bit memory
Generator formats	DNRZ, RZ, R1	2.7G:DNRZ 50% clock DNRZ, R1, RZ	DNRZ, separate clock output	NRZ, DNRZ
Technology addressed	TTL, (P)ECL, LVDS	CML, (P)ECL, LVDS, SSTL-2	CML, ECL,LVDS, SSTL-2	LVDS, CML, PECL, ECL, low voltage CMOS

ParBERT 81250 measurement software

The ParBERT measurement software includes the following measurements:

1. **BER measurement**
2. **Fast eye mask measurement**
3. **DUT output timing measurement**
4. **Spectral decomposition of jitter**
5. **DUT output level measurement**
6. **Eye opening**

The ParBERT 81250 measurement software is a ready-to-use measurement user interface, which aids you with the verification and characterization of high-speed digital components and modules.

The measurement software offers three different levels of measurement analysis:

1. Fast pass/fail measurements ideal for production.

If you work in production you can test against limits, e.g., the BER is set at a given threshold. The fast pass/fail measurements allow you to test devices at up to ten times faster than with previous test methods - it typically takes less than one second!

2. Fast clock out to data out (setup and hold times), skew and eye opening specification results - no need to calculate values

3. Graphical results for detailed root cause analysis - see trends clearly and fast, e.g., pseudo color plot and contour plots.

If you are in R&D you can characterize your device under test (DUT), find the limits and specifications of the DUT and results can be viewed graphically. With its easy-to-use Windows XP or Windows 2000 based GUI and graphical results, it simplifies test development and allows easy test execution. Data can be exported and the graphical and numerical results printed.

You can create a test executive around the measurement software using Agilent VEE Pro, National Instruments' LabVIEW, Excel, Agilent TestExec, C/C++, C# and Microsoft VisualBasic.

The measurement software is included in the standard software package which comes with each ParBERT 81250 system.

Table 3

General	
Store/recall	Workspace Single measurements
Copy/paste	Measurement data to compare between measurements
Print	Various print-out functions
Export of measurement data	ASCII
Online help	Extensive applications
Remote interface	P&P driver, Ready to use active X components to integrate complete measurements in VEE, Visual C++, VB, C#, Labview, Matlab and Excel

BER measurement

The bit error ratio measurement measures the total number of bits transferred and the number of errored bits, bits which don't meet the decision threshold. You can now view the actual 0 and 1 BER, actual 0 and 1 errors, accumulative 0 and 1 BER and accumulative 1 and 0 errors at once.

Measurement results provided:

- Displayed errored ones and zeros at the same time
- Log file
- Resynchronization
- Pass/fail results

The bit error ratio measurement can be run as a single shot or repeatedly. Several run and error counting options and stop criteria can be defined. Repetitive mode offers automatic resynchronization. It is the ideal mode for characterizing your device. In R&D, for example, you can change the temperature and measure how it affects the BER. Single mode is particularly useful for manufacturing as you can stop the measurement after a specified number of errors and/or seconds.

Table 4. BER measurement

Measurement parameters	BER Compared bits Errors from expected 0s Errors from expected 1s Total errors Parameters from last measurement period Accumulated parameters
Measurement mode	Single or repetitive Repetition rate is programmable in seconds (In this mode resynchronization can be enabled)
Pass/fail	For actual and accumulated parameters
Log file	Logs all measured parameters

Fast eye mask

The fast eye mask measurement is ideal for use in manufacturing as a measurement typically takes just one second (including synchronization). This measurement records the BER of a predefined number of points (1 to 32), not the whole eye, defined by a threshold and timing value relative to the starting point of the measurement. You enter the pass/fail criteria of the measurement and the BER threshold, find the middle point of the eye with the sequence and then run the BER. For example, you can define a threshold and the ParBERT will find the optimal sample point and the high and low levels automatically, e.g, 20% and 80%.

Measurement results provided:
- BER at predefined sample points
- pass/fail results

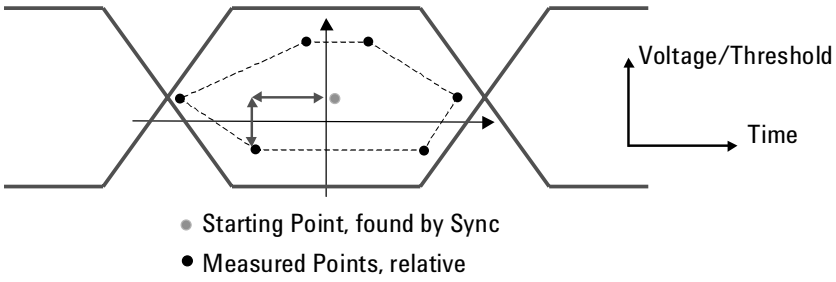


Figure 8. How the fast eye mask measurement works

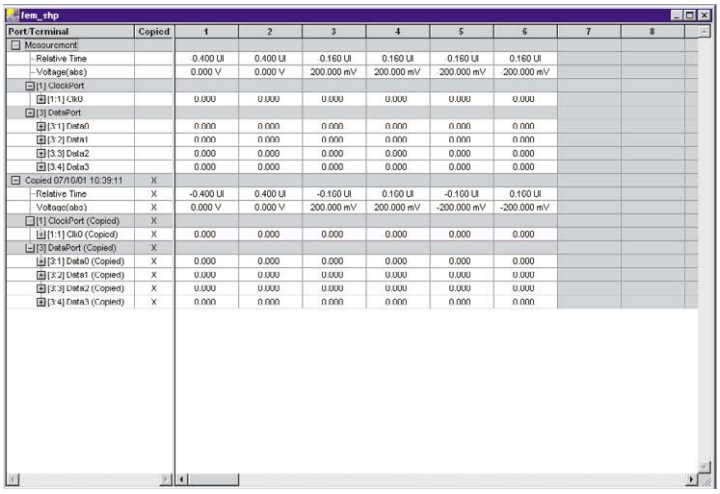


Figure 9. The fast eye mask setup and results window

Table 5. Fast eye mask measurement time examples (run on a system via IEEE 1394 PC link)

Frequency	# channels	# points measured	Compared bits	Time taken
2.7 Gbit/s	2	6	106	< 1 sec
2.7 Gbit/s	2	32	106	~ 1 sec
675 MHz	16	6	106	~ 6 sec
675 MHz	16	32	106	~ 6 sec

DUT output timing measurement

This measurement measures the BER of a DUT's output versus sample point delay, which is shown graphically as a bath tub curve. The delay is always centered to the optimum sampling delay point of the port (terminals). If a clock is defined the clock to data alignment is measured. If the absolute delay can be measured it will also be displayed. Relative timing, where edges are compared, is also possible.

Measurement results provided:

- Clock out to data out timing relationships (setup/hold time)
- Skew between outputs
- Delay at optimum sample point
- Phase margin
- Pass/fail results
- Jitter results for total jitter, random jitter and deterministic jitter

There is also a numerical view that shows the "numerical return values" for the selected BER threshold only.

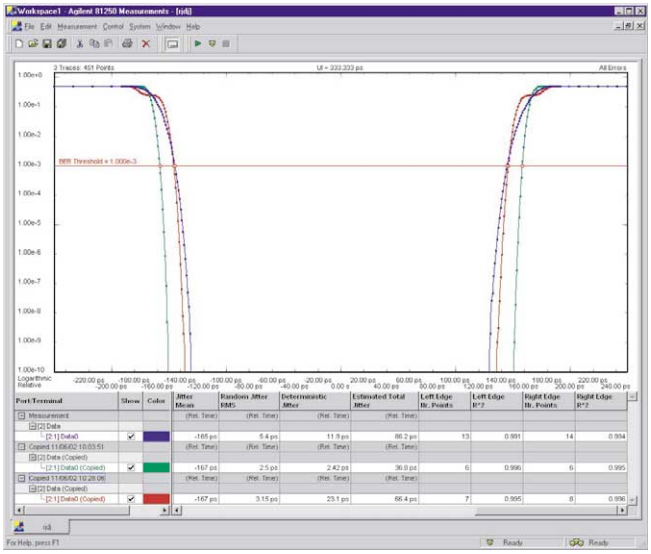


Figure 10a. View the DUT output measurement results as a bathtub curve

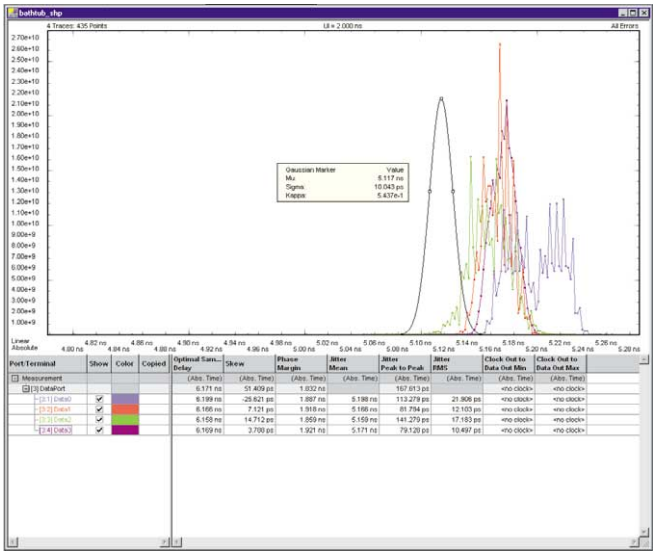


Figure 10b. Jitter can be directly equated from the bathtub curve. View the jitter as a histogram

Table 6. DUT output timing measurement

Timing parameters	Optimum sample point delay
	Phase margin
	Clock to data out minimum
	Clock to data out maximum
	Skew between channels
Jitter parameters	RMS jitter
	Mean value
	Peak peak jitter for specific BER
Pass/fail	For all timing and jitter parameters
	Each parameter can be individually enabled
Graph	View of BER versus sample delay
	2 Markers: delay, BER

Spectral decomposition of jitter

This measurement provides a technique for the spectral decomposition of jitter components, which helps debugging as well as design verification and characterization of devices. This measurement uses the RJ/DJ Separation provided by the output timing measurement.

The decomposition technique allows inband and outband characterization of circuits and devices including PLLs and CDRs.

While debugging designs, the new measurement allows the thorough exploration of the various components of deterministic jitter, helping to separate even the smallest amounts of periodic jitter (for example) from the random jitter floor. Measurement results provided:

- Top 10 frequency/power spots
- Total power
- Noise power

Table 7. Spectral decomposition of jitter

Parameters	Data segment length FFT windowing
Pass/fail	Power factor
Graphs	Spectrum graph (power vs. frequency)

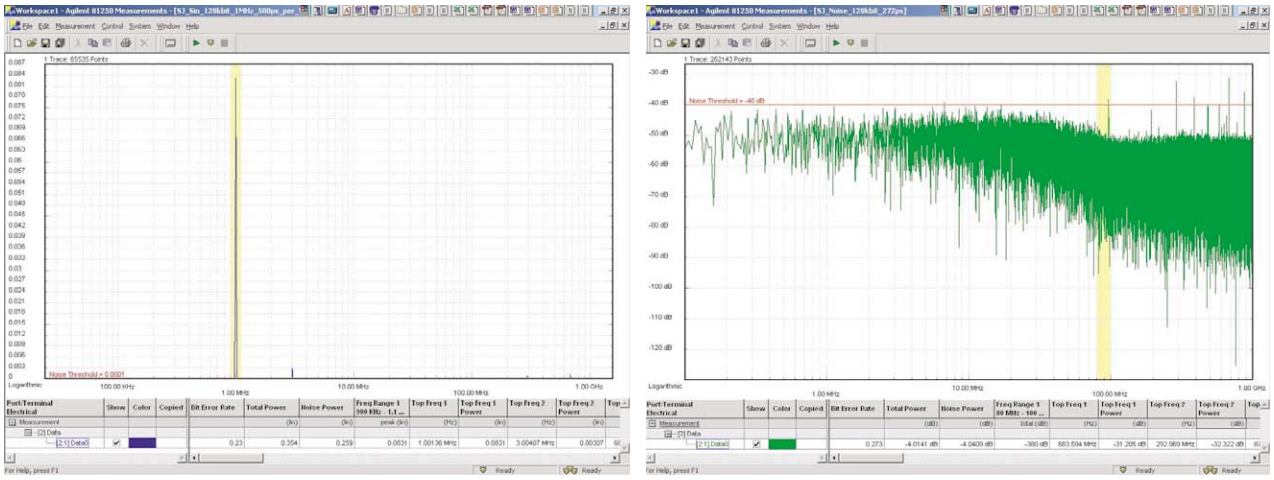


Figure 11. Spectral decomposition of jitter

Output level measurement

This measurement performs a sweep of the analyzer threshold. It is shown graphically as a bathtub curve, with the threshold on the Y-axis and BER on the X-axis (see Figure 12a). From the data a histogram showing BER versus threshold can be derived (Figure 12b) which can be used to calculate one/zero level means and standard deviations. Also a graph showing Q-factor from BER versus threshold (Figure 12c) can be derived, which shows the result of two tail fitting operations for the innermost gaussian distributions in the BER histogram.

Table 8. Output level measurement

Measurement parameters	High/low level
	Mean level
	Amplitude
	Threshold margin
	High/low level standard deviation
	Peak peak noise
	Signal/noise ratio (rms & peak-to-peak)
	Q factor
Pass/fail	For all parameters
	Each parameter can be individually enabled
Graphs	BER versus threshold
	BER histogram versus threshold
	Q from BER versus threshold

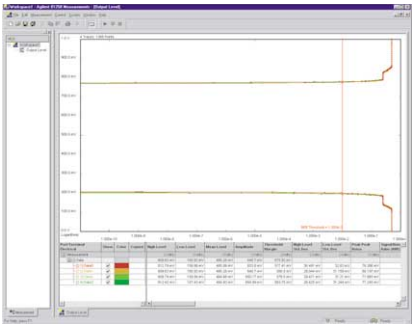
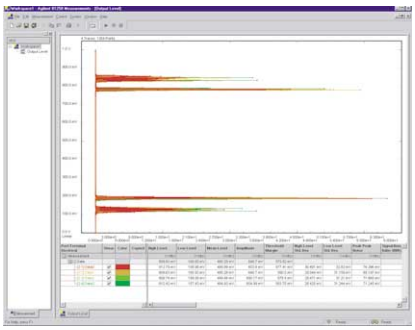
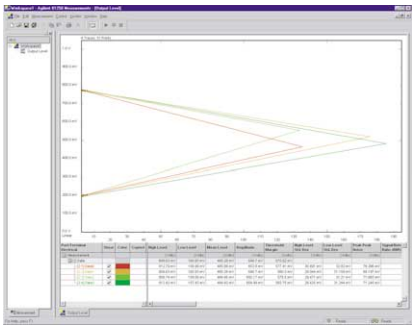


Figure 12a. BER versus threshold



12b. BER histogram versus threshold



12c. Q from BER versus threshold

Eye opening

To measure the eye opening the sampling delay and the threshold of the receiving channels are swept.

Measurement results provided:
- Eye opening (voltage and timing)
- Optimum sample point

Table 9. Eye opening

Measurement parameters	Optimum sample
	Point delay
	Optimum threshold
	Eye opening (Volt)
	Phase margin
Pass/fail	For all parameters
	Each parameter can be individually enabled
Graph	Two markers: voltage, delay, BER

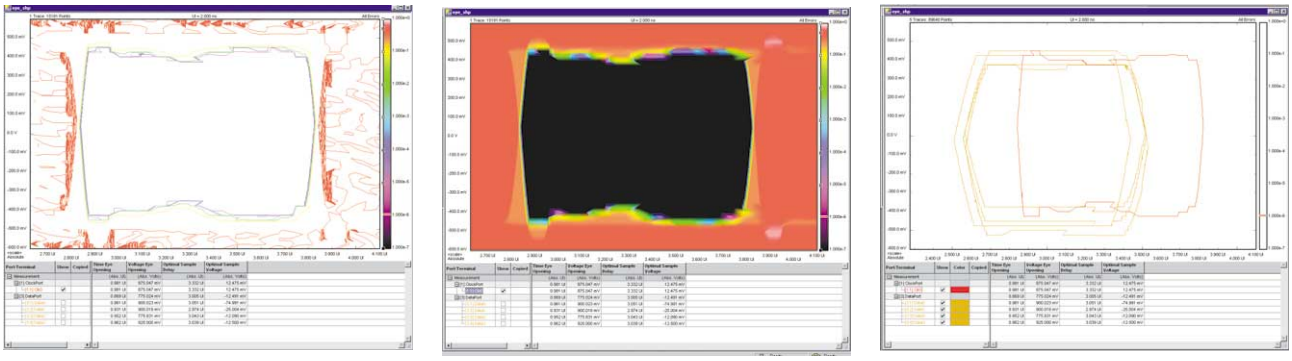
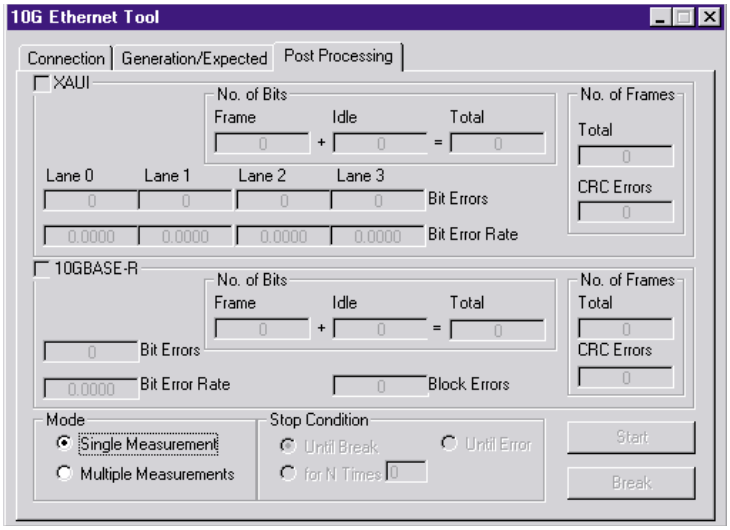


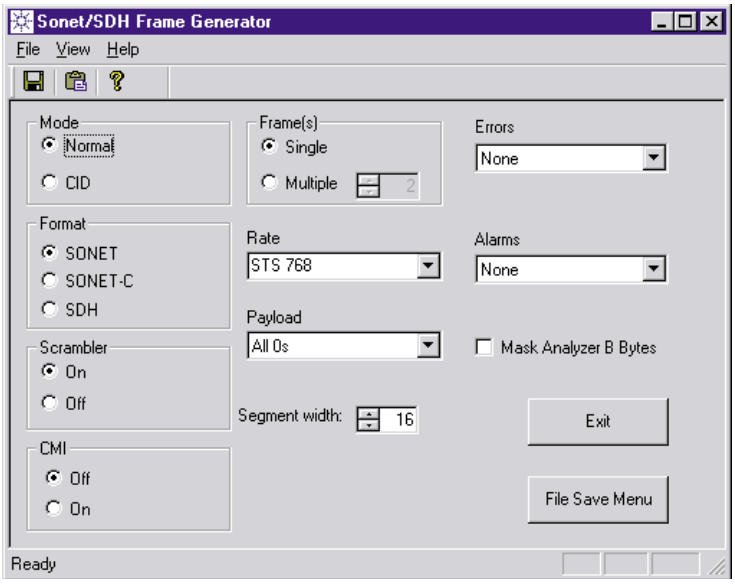
Figure 13 a/b/c. View the BER for one terminal as a pseudo color plot or contour plot or equal BER at BER threshold

The software offers various processing tools



Post processing for 10Gb Ethernet applications

Figure 14a. 10GbE processing tool



SONET/SDH Editor e.G Setup for synchronous architecture Frame Generator applications

Figure 14b. SONET/SDH editor

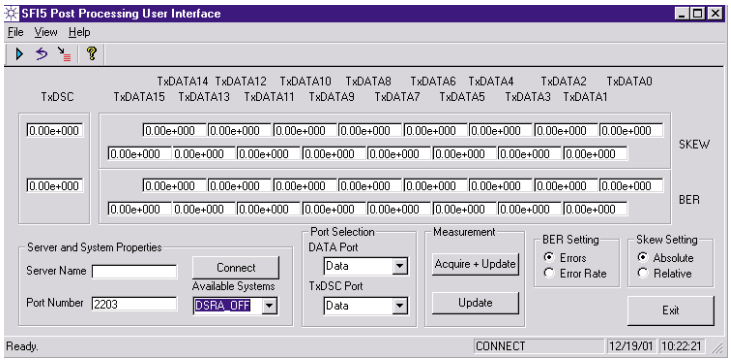


Fig 14c. SFI5 post processing

Analyzing the data & the DSC (17th) bit

- Ensure that the 16 data channels are valid (valid PRBS 2^7 - 1 or 2^{11} - 1) streams
- Ensure that the 16 data channels are within skew specification
- Ensure that the DSC (17th) bit is valid
  -correct header
  -match to the 16 data channels

ParBERT 81250 Application examples

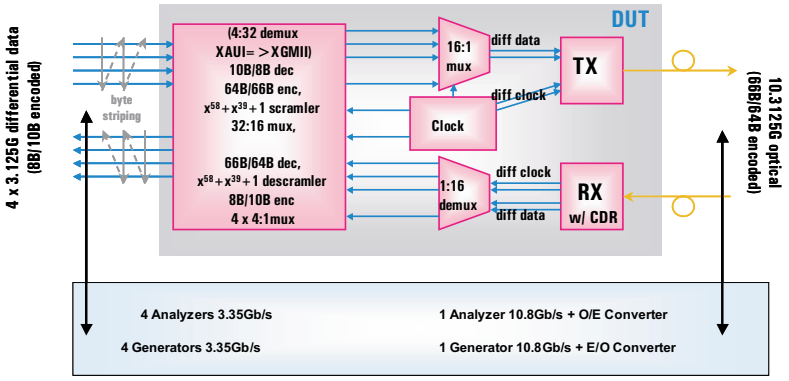


Figure 15a. 10GbE

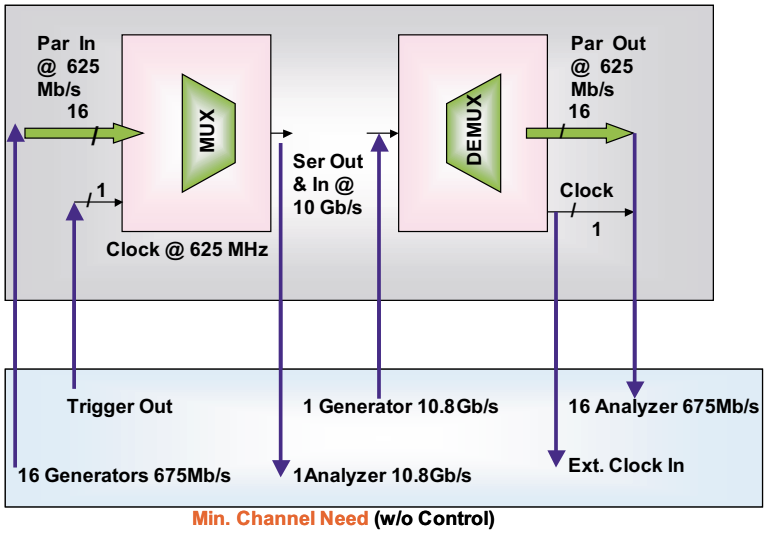


Figure 15b. OC 192 example

10GbE

10GbE parts are used in the LAN area. The DUT is a module with 4 x 3.125 Gb/s electrical inputs and outputs each and 1 x 10.3125 Gbit/s optical input and output. The DUT supplies a clock of 156.25 MHZ to all systems. The optical signals are converted to electrical.

The configuration of the ParBERT 81250 for 10GbE testing includes four clock groups and E/O and O/E converters for the optical signals at 10.3125 Gb/s.

OC 192

OC 192 parts are used in telecom applications. Here the DUT consists of two chips, one TX and one RX. There is no clock at the serial side. For testing 16x 675 Mb/s Generators and Analyzers on the parallel side are needed. The serial side needs 1x 13.5 Gb/s or 10.8 Gb/s generator and analyzer.

The 81250 configuration to the left contains all necessary resources to test the Mux/Demux. Both parts of the DUT can be tested at one run-time, regardless of whether memory-based data or PRBS/PRWS are used.

The 13.5 Gb/s or 10.8 Gb/s channels can be used together with the 675 Mb/s channels, as the multiplier is 16 (another multiplier would require separation into 2 clock groups, similar to the other two examples). The combination of all generators and analyzers in individual clock groups eliminates the synchronization limitations.

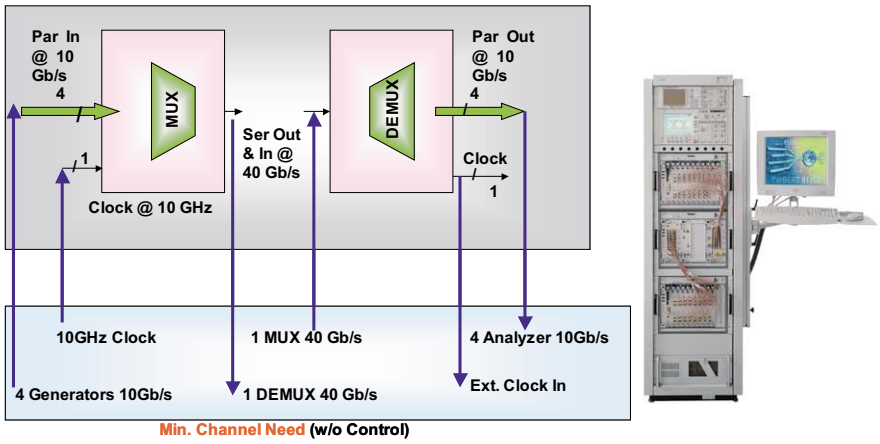


Figure 16a. OC-768 example

OC 768, 1:4 Mux/DeMux

DUT consists of two chips, one TX one RX. There is no clock at the serial side. This will require 4 x 10.8 Gb/s or 13.5 Gb/s generator and analyzer channels for the parallel side and 1 x 43.2 Gb/s generator and error detector bundle E4894B and E4895B. The 81250 configuration, shown in Figure 16, contains all the necessary resources to test a Mux/Demux. Both parts of the DUT could be tested at once using PRBS/PRWS data.

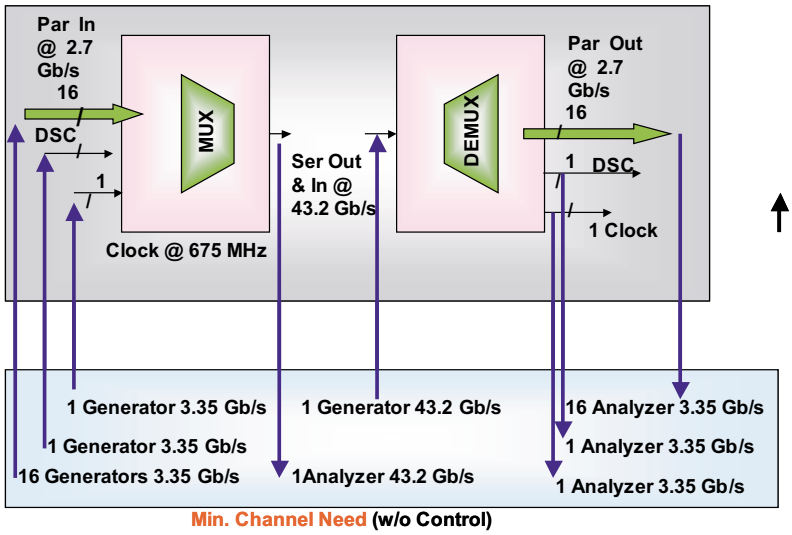


Figure 16b. OC-768 SFI-5 MUX and DeMUX

OC 768, SFI-5 (1:17) Mux/DeMux

The DUT consists of two parts: a TX and RX part. Characteristic for SFI-5 is the 17th bit, called the DSC signal. This carries specific timing alignment data. The modular ParBERT 81250 architecture allows the easy addition of a 17th generator and analyzer channel to handle the DSC signal. The 81250 configuration, shown in Figure 16a, contains all the necessary resources to test a SFI-5 Mux and Demux. Both parts of the DUT can be tested but not at one run-time. The parallel side (3.35 Gb/s) includes 18 generators and 18 analyzers, so in addition to the 16 data bits, the test system can handle the DSC signal (17th bit) and any clock if necessary.

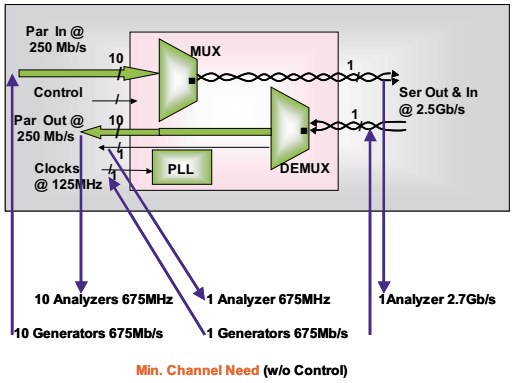


Figure 17a. Gigabit ethernet example

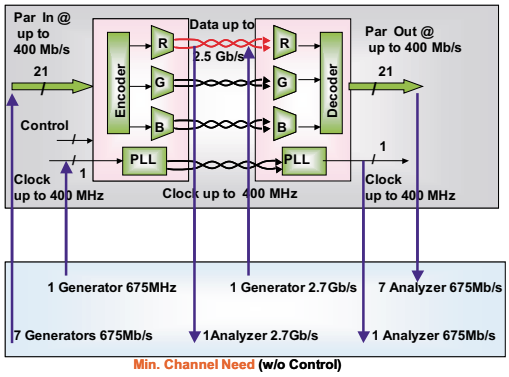


Figure 17b. Video (DVI) example

Digital video

For transferring data between a CPU and display, a digital video interface was created. The picture shown here is a simple example as there are several implementations created with more or less serial interconnections (up to 8). It is very common that the Mux/Demux ratio is 1:7 with these video interfaces. The DUT consists of two chips, one TX and one RX. Besides 3x serial there is also the clock at the speed of parallel side transferred. For a minimum test of this device, the number of channels needed is counted to stimulate and analyze one of the three Mux/Demux paths. So this would need a total of 8 x 675 Mb/s generators and analyzers (1x for clock, 7x for data) and 1 x 2.7 Gb/s generator and analyzer for the serial side. The 81250 configuration, shown in Figure 18, contains all necessary resource to test a Mux/Demux. Testing is limited to one serial interface (either R, G or B). As long as PRBS/PRWS data are used both parts of DUT could be tested at one run-time. If memory-based data is used, (due to synchronization limitations) only one part can be tested at one run-time.

Gigabit ethernet

Gigabit ethernet tranceivers take care of physical transreceiving data between a PC and a local network. The implementation consists of one chip, containing one TX and one RX. There is no clock at the serial side. (For 10 Gigabit ethernet there would be signals running at 3.125 Gb/s) For testing this device without the control inputs, 11 x 675 Mb/s generator and analyzer channels (1x clock and 10x data) would be needed for the parallel side. On the serial side 1x 2.7 Gb/s generator and analyzer are needed. The 81250 configuration, shown in Figure 17, contains all necessary resources to test this Mux/Demux. As long as PRBS/PRWS data are used, both parts of the DUT can be tested at one run-time.
If memory-based data is used, (due to synchronization limitations) only one part can be tested at one run time.

Agilent ParBERT 81250

Agilent N4872A ParBERT 13.5 Gb/s Generator
Agilent N4873A ParBERT 13.5 Gb/s Analyzer

Technical Specifications

General

The N4872A generator and N4873A analyzer modules are each one VXI slot wide and operate in a range from 620 Mb/s up to 13.5 Gb/s. The ParBERT 13.5 Gb/s modules require the E4809A 13.5 GHz central clock module, which is two VXI slots wide. All specifications, if not otherwise stated, are valid at the end of the recommended N4910A cable set (24" matched pair 2.4 mm).

The N4872A generator module generates hardware-based PRBS up to 2^{31} - 1, PRWS and user-defined patterns and provides a memory depth of 64 Mbit. The N4873A can synchronize on a 48 bit detect word, or on a pure PRBS pattern without detect word.

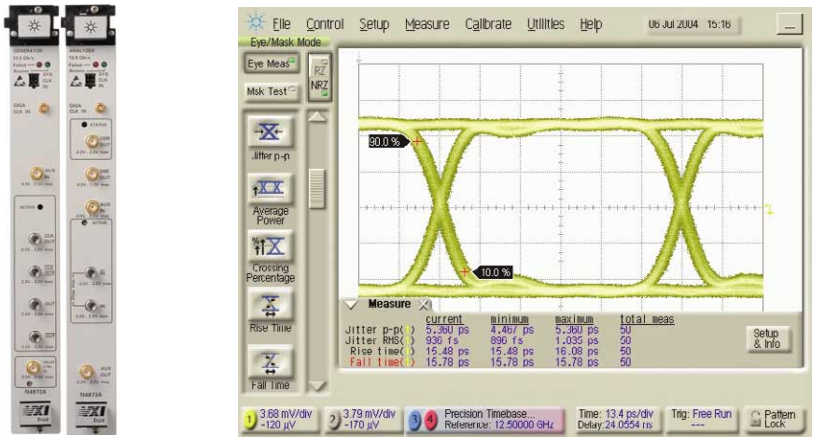


Figure 18. N4872A & N4873A and waveform

Table 10. N4872A data generator timing specifications (@ 50% of amplitude, 50 Ω to GND)

Frequency range	620 Mb to 13.500 Gb
Delay = start delay + fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 100 ns
Fine delay range	± 1 period (can be changed without stopping)
Delay resolution	100 fs
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement. (@ 25 °C - 40 °C ambient temp.)
Relative delay accuracy	±2 ps ± 2% typ. (@ 25 °C - 40 °C ambient temp.)
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency. (@ 25 °C - 40 °C ambient temp.)

Timing specifications

The ParBERT 13.5 Gb/s modules are able to work with three different clock modes.

- *Internal clock mode:* The common clock mode is provided by the E4809A 13.5 GHz central clock module, which generates clock frequencies up to 13.5 GHz.
- *External clock mode:* The system also works synchronously with an external clock, which is connected to the E4809A clock module.
- *CDR mode:* To use the N4873A 13.5 Gb/s analyzer CDR capabilities, connect the analyzer's CDR out to the E4809A clock module's clock in.

Sequencing

The sequencer receives instructions from the central sequencer and generates a sequence. The channel sequencer can generate a sequence with up to 60 segments.

An analyzer channel generates feedback signals that can control the channel sequencer and/or the central sequencer. With parallel analyzer channels, the feedback is routed to the central sequencer to allow a common response of all parallel channels. With a single receive channel, the channel sequencer itself handles the feedback signals.

Pattern generation

The data stream is composed of segments. A segment can be made up of a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 64 Mbit (at segment length resolution 512 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to $2^{15} - 1$ or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio.

A zero substitution pattern extends the longest zero series by a user selectable number of additional zeroes. The next bit following these zero series will be forced to 1. Mark ratio is the ratio of 1 s and 0 s in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4 and 7/8.

Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 512 the number of repetitions is also 512. That means that a $2^{15} - 1$ PRBS uses up to 16 Mbit of the memory. Hardware-based PRBS can be a polynomial up to $2^{31} - 1$. No memory is used for hardware-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a 0 a 1 is generated and vice versa.

Table 11. N4872A pattern and sequencing

Patterns:	
Memory based	Up to 64 Mbit
PRBS/PRWS	$2^n - 1$, n = 7, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at $2^n - 1$, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	$2^n - 1$, n = 7, 9, 10, 11, 15
Extended ones or zeros	$2^n - 1$, n = 7, 9, 10, 11, 15
PRWS port width	1, 2 , 4, 8, 16

Table 12. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range, Mb/s	Segment length resolution	Maximum memory depth, bits
620 ... 1.350,000	32 bits	4.194,304
620 ... 2.700,000	64 bits	8.388,608
620 ... 5.400,000	128 bits	16.777.216
620 ... 10.800,000	256 bits	33.554.432
620 ... 13.500,000	512 bits	67.108.864

N4872A generator module

The N4872A generates differential or single-ended data and clock signals operating from 620 Mb/s up to 13.5 Gb/s. The output levels are able to drive high-speed devices with interfaces like LVDS, ECL, PECL, CML and low voltage CMOS. The nominal output impedance is 50 Ω typical. The delay control IN has a single-ended input with 50 Ω impedance. The input voltage allows modulation of a delay element up to 1 GHz (200 ps) within the generator's differential output. See figure 25c - 26c on page 36.

The AUX IN has a single-ended input with a 50 Ω impedance. The AUX IN allows injecting gating signals.

An active (TTL high) signal at the auxiliary input forces (gates) the data to a logic zero.

Data OUT

Table 13. Parameters for N4872A ParBERT 13.5 Gb/s generator

Data output	1, differential or single ended, 2.4 mm(f)	**(1)**
Range of operation	620 Mb/s - 13.5 Gb/s	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	-2.00 to +3.00 V	
Short circuit current	72 mA max.	
External termination voltage	-2 V to +3 V	**(2)**
Data formats	Data: NRZ, DNRZ	
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3 V/0 V/-2 V) low voltage CMOS	
Transition times (20% - 80%)	< 20 ps	
Jitter	9 ps peak-peak typ.	**(3)**
Cross-point adjustment (Duty cycle distortion)	20%...80% typ.	

(1) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(2) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(3) Clock out to data out

Clock OUT

Table 14. Parameters for N4872A ParBERT 13.5 Gb/s generator

Clock output	1, differential or single-ended, 2.4 mm(f)	**(1)**
Frequency	620 MHz - 13.5 GHz	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	-2.00 to +2.80 V	
Short circuit current	72 mA max.	
External termination voltage	-2 V to +3 V	**(2)**
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3 V/0 V/-2 V) low voltage CMOS	
Transition times (10% - 90%)	< 25 ps	
Jitter	1 ps RMS typ.	
SSB phase noise (10 GHz @ 10 kHz offset, 1 Hz bandwidth)	< - 75dBc with clock module E4809A typ.	

(1) In single-ended mode, the unused output must be terminated with 50 W to GND.
(2) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.

Delay control IN

Table 15. Parameters for N4872A ParBERT 13.5 Gb/s generator

Delay control input	Single-ended; DC-coupled; SMA(f)
Input voltage window	-250 mV ... +250 mV (DC-coupled)
Input impedance	50 Ωtyp.
Data rate	
Delay range	-100 ps ... +100 ps
Modulation bandwidth	DC ... 1 GHz @ < 10.5 Gb/s

AUX IN

Table 16. Parameters for N4872A ParBERT 13.5 Gb/s generator

Interface	DC coupled, 50 Ω nominal
Levels	TTL levels
Minimum pulse width	100 ns
Connector	SMA female

N4873A analyzer module

The analyzer features are:

- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the bit-error-ratio.

Receive memory for acquired data is up to 64 Mbit deep, depending on segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum segment resolution (32, 64, 128, 256, 512).

The analyzer is able to synchronize on a received data stream by means of a user selectable synchronization word. The sync. word has a length of 48 bits and is composed of zeros, ones and Xs ("don't cares"). The detect word must be unique within the data stream. Synchronization on a pure PRBS data-stream is done without a detect-word, instead by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity of 50 mV and the common mode range of the comparator allow the testing of all common differential high-speed devices. The user has the choice of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

Table 17. N4873A analyzer timing: all timing parameters are measured at ECL levels, terminated with 50 Ω to GND

Sampling rate	620 MHz to 13.500 GHz
Sample delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 100 ns
Fine delay range	± 1 period (can be changed without stopping)
Delay resolution	100 fs
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement. **(1)**
Relative delay accuracy	±2 ps ± 2% typ. **(1)**
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency. **(1)**

(1) 25 °C - 40 °C ambient temperature

Table 18. N4873A pattern and sequencing

Analyzer auto-synchronization	On PRBS or memory-based data manual or automatic by: bit synchronization(2) with or without automatic phase alignment automatic delay alignment around a start sample delay (range: ± 10 ns) BER threshold: 10^{-4} to 10^{-9}

(2) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect word at the beginning of the segment, and the generators must be on a separate system clock. Don't cares within detect word are possible. If several inputs synchromize, the delay difference between terminals must be smaller than ±5 segment length resolution.

Table 19. Parameters for N4873A ParBERT 13.5 Gb/s analyzer

Number of channels	1, differential or single ended, 2.4 mm (f)
Range of operation	620 Mb/s - 13.5 Gb/s
Max input amplitude	2 Vpp
Input sensitivity	50 mVpp typical @ 10 Gb/s, PRBS 2^{31} - 1, and BER 10^{-12}
Input voltage range	-2V ... +3 (selectable 2 V window)
Internal termination voltage (can be switched off)	-2.0 to +3.0 V (must be within selected 2 V window)
Threshold voltage range	-2.0 to + 3.0 V (must be within selected 2 V window)
Threshold resolution	0.1 mV
Minimum detectable pulse width	25 ps typ.
Phase margin (Source: N4872A)	1 UI - 12 ps typ.
Impedance	50 Ω typ. (100 Ω differential, if termination voltage is switched off)

Clock data recovery

The analyzer module has integrated CDR capabilities, which allow the recovery of either clock or data. Before the CDR can lock onto the incoming data stream, the data rate must be defined within the user interface; common data rates are pre-defined. In CDR mode, phase alignment to the center of the eye is done automatically during synchronization. For correct operation, the CDR output must be connected to the clock input of the E4809A 13.5 GHz central clock module. In addition the generator clock source and the analyzer clock source must be independent.

AUX OUT

The AUX OUT provides data or recovered clock signals.

AUX IN

Gating functionality: If a high level is applied at AUX IN, comparison is disabled and internal counters are stopped. After resuming a low level at AUX IN, comparison is enabled and internal counters continue. The internal sequencing is not stopped.

ERROR OUT

Whenever one or more bit errors are detected, the error out signal is high for one segment resolution. A high period is always followed by a low period (RZ-format) in order to ensure trigger possibility on continuous errors.

Table 20. Parameters for N4873A ParBERT 13.5 Gb/s analyzer - clock data recovery

Common data rates	OC-192:	9.953 Gb/s
	10GbE:	10.3125 Gb/s
	Fiber channel:	10.51875 Gb/s
	G.709/G.975:	10.664 Gb/s/10.709 Gb/s
	S-ATA/FireWire:	6.4 Gb/s
	PCI-Express:	6.4 Gb/s
	OC-48:	2.488 Gb/s
	10GbE:	3.125 Gb/s
	SAN:	3.187 Gb/s
	S-ATA/FireWire:	3.2 Gb/s
Frequency ranges	9.9 GHz ...10.90 GHz	
	4.23 GHz ...6.40 GHz	
	2.115 GHz... 3.20 GHz	
	1.058 GHz....1.6 GHz	**(1)**

The CDR works with specified PRBS patterns up to 2^{31} - 1,
The CDR expects a DC balanced pattern,
The CDR expects a transition density of one transition for every second bit.

(1) Available for hardware S/N : DE43A00401 and software rev. 5.62

Table 21. Parameters for N4873A 13.5 Gb/s analyzer - AUX OUT

Interface	AC coupled, 50 Ω nominal
Amplitude	600 mV nominal
Output jitter (clock @ AUX OUT)	0.01 UI rms typical
Connector	SMA female

Table 22. Parameters for N4873A 13.5 Gb/s analyzer - AUX IN

Resolution	Segment resolution
TTL compatible	Internal 500 Ωtermination to GND
Threshold	@ 1.5 V
Connector	SMA female
Low (0...1 V)	Internal counters are enabled
High (2 V...4 V)	Internal counters are stopped
Open	Same as low

Table 23. Parameters for N4873A 13.5 Gb/s analyzer - ERROR OUT

Format	RZ; active high
Output high level	0 V ± 100 mV
Output low level	+1 V ± 100 mV
Connector	SMA female

Ordering information

N4872A
ParBERT 13.5 Gb/s generator module
N4873A
ParBERT 13.5 Gb/s analyzer module
E4809A
13.5 GHz central clock module

Accessories:

N4910A
2.4 mm matched cable pair
N4912A
2.4 mm 50 Ωtermination male connector
N4913A
4 GHz deskew probe for E4809A

Technical specifications

All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10 to 40 °C ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ω to ground at ECL levels if not specified otherwise.

Agilent ParBERT 81250

Agilent E4866A ParBERT 10.8 Gb/s Generator Module
Agilent N4868A ParBERT Booster Module
Agilent E4867A ParBERT 10.8 Gb/s Analyzer Module

Technical Specifications

General

The E4866A is a 10.8 Gb/s generator module. The N4868A is a booster module for the E4866A. The E4867A is a 10.8 Gb/s analyzer module.

Clock timing

The generator provides complementary data and single-ended clock output. Both clock out and data out can be moved with the variable delay; it is the same delay for both. The analyzer also has a variable sampling delay. This consists of two parts:

1) the start delay with a large range
2) the time delay of the ±1 period without stopping.

Data capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator for a stimulating pattern. On an analyzer it defines the expected pattern where the incoming data are compared to. The expected pattern can be setup with mask bits. The segment length resolution is the resolution to which the length of a pattern segment can be set. The segment length resolution is 256 bits for a total of 32 MB memory.

Fig 19. E4866A generator module

Table 24. E4866A timing specifications (@ 50% of amplitude, 50 Ω to GND)

Data range	9.5 Gb/s to 10.8 Gb/s
Clock range	9.5 GHz to 10.8 GHz
Delay range	0 to 300 ns
Delay resolution	1 ps
Accuracy	±20 ps ± 50 ppm relative to the zero-delay placement.
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency

Table 25. E4866A pattern and sequencing

Segment length resolution	256 bits
Patterns:	
Memory based	up to 32 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15

AC coupling behind sampling circuit

The AC coupling does not impact the performance of the analyzer as long as the input data is balanced or the following limitations are not exceeded:

1. For infinite time period a mark density from 9/10 to 10/9 is tolerated.
2. All zero or all one patterns must not be longer than 20000 bits or 2 µs.
3. When data recovers from imbalanced pattern to a balanced pattern a settling time of maximum 200 µs takes effect.

Table 26. Parameters for clock output E4866A 10.8 GHz

Output	1, single ended, AC coupled, to be used into 50 Ω
duty cycle	50% typical;
Maximum external voltage	-2.2 V to +3.3 V
Amplitude/resolution	0.5 Vpp fixed typ.
Transition times (20% - 80%)	sine wave
Clock jitter	< 2 ps RMS

Booster N4868A

The N4868A delivers either 1 differential channel or 2 single-ended channels. The N4868A-001 delivers either 2 differential or 4 single-ended channels. For differential operation it is recommended that the N4869A cable kit be used with phase adjustment capability for the differential path. For the N4868A -001 two cable kits would be needed if both are used as differential. The N4868A-001 can also be used 1x differential and 2x single-ended to boost the clock output of the E4866A.

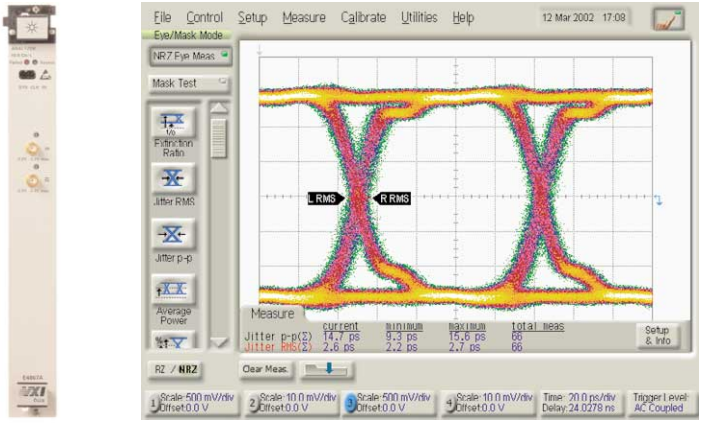


Fig 20. E4868A booster and wave diagram

Table 27. Parameters for data output E4866A 10.8 Gb/s with N4868A booster(1)

Outputs	1, differential, 50 Ω typ.	1, differential or 2, single-ended
Data formats	NRZ	NRZ
Amplitude/resolution	0.3 V to 1.8 V/10 mV	1.0 V to 2.5 V
Accuracy hi level/amplitude	±2% ±10 mV	±5% ±50 mV
External termination voltage	-2 V to +1.5 V	AC coupled
Output voltage window	-2.0 to +2.7 V	
Maximum external voltage	-2.2 V to +3.3 V	
Enable/disable	Relay	-
Transition times (20% - 80%)	< 60 ps	< 20 ps (15 ps typ.)
Overshoot/ringing	10% +20 mV typ.	-
Jitter	< 25 ps peak-to-peak (20 ps typ.)	< 25 ps peak-to-peak

(1) Booster input to be driven with 1.8 V amplitude from E4866A generator

E4867A analyzer module

The E4867A is a 10.8 Gb/s analyzer module which is one VXI slot wide and operates in a range from 9.5 Gb/s up to 10.8 Gb/s. The ParBERT 10.8 Gb/s modules requires the E4808A central clock module.

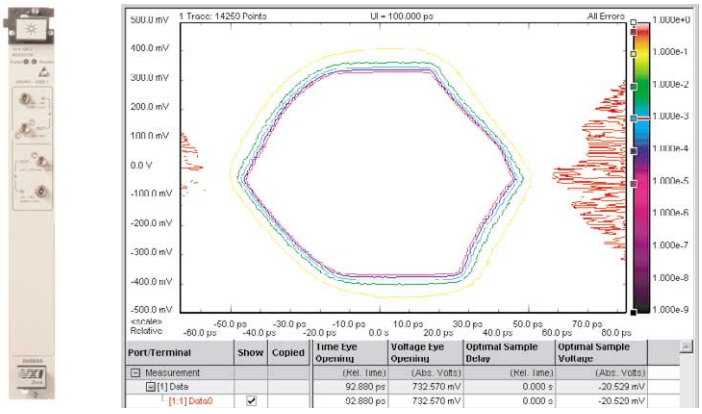


Figure 21. E4867A analyzer with eye diagram

Table 28. E4867A timing specifications (@ 50% of amplitude, 50 Ω to GND)

Data range	9.5 Gb/s to 10.8 Gb/s
Delay (between channels)	Can be specified as leading edge delay (start delay) in fraction of bits in each channel, fine delay can be changed without stopping the instrument
Start delay range	0 to 300 ns (not limited by period)
Fine delay range	±1 period (without stopping)
Resolution	1 ps
Accuracy	±20 ps ±50 ppm relative to the zero-delay placement.
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency
Sampling delay resolution	100 ps

Table 29. E4867A pattern and sequencing

Segment length resolution	256 bits
Patterns:	
Memory based	Up to 32 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
User	Data editor, file import
Analyzer expected data	
Mark density	9/10...10/9
Max consecutive 0 or 1	20000 or 2 µs
Data recovery from imbalanced	200 µs
Analyzer auto-synchronization	on PRBS or memory-based data manual or automatic by: Bit synchronization(1) with or without automatic phase alignment. Automatic delay alignment around a start sample delay Range ± 10 ns BER threshold: 10^{-4} to 10^{-9}

(1) Bit synchronization on data is achieved by detecting a 48 bit unique word at the beginning of the segment. ("Don't care" can be programmed within the detect word). In this mode memory-based data cannot be sent within the same system. If several inputs synchronize, the delay difference between the terminals must be smaller ±5 segment length resolution.

Table 30. Parameters for analyzer module E4867A 10.8 Gb/s

Inputs	1, differential or single-ended	
Impedance	50 Ω typ. 100 Ω differential if termination voltage is switched off	
Input sensitivity	100 mV typ., single-ended and differential	
Internal termination voltage	-2.0 to +2.0 V, can be switched off	
Threshold voltage range	-2.0 to + 2.0 V	
Threshold resolution	1 mV	
Threshold accuracy	± 2% ±20 mV	
Maximum input voltage range		
Three ranges selectable:	-2 V to + 0 V, -1 V to +1 V, 0 V to 2 V	
Maximum differential voltage	1.2 V	
Enable/disable	Relay	
Bandwidth, equivalent transition time (20% - 80%)	35 ps typ.	
Minimum detectable pulse width	Data:	80 ps typ.
	Continuous clock:	40 ps typ.
Phase margin with ideal input signal with E4866A generator.	> 1 UI -15 ps > 1 UI -33 ps	

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The synchronization can be performed on PRBS/PRWS and memory-based data (it is not possible with a mix of PRxS and memory-based data). There are two types of sychronization:

- Bit synchronization
- Auto delay alignment

Memory-based bit synchronization is able to cover a bit aligment for a totally unknown number of cycles. Using data, the first 48 bit within the expected data segment will work as a DETECT word where the incoming data are compared to. When the incoming data match with this "detect word", further analysis is started.

Auto delay aligment is performed using the analyzer sampling delay. The sampling delay range is ±10 ns.

Using auto delay alignment provides synchronization with an absolute timing relation between a group of analyzer channels. Therefore skew measurements will be possible.

Input/output

Addressable technologies:

CML, SSTL-2, ECL (terminated to 0 V/-2 V), LVPECL, (terminated to 1.3 V)

Generator out

The generator output can be used as single-ended or differential. Enable/disable relay provides on/off switching. Switched off provides internal termination. It is recommended either to turn off or externally terminate unused outputs.

The generator outputs can work into 50 Ω center tapped termination or 100 Ω differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

Analyzer input

The analyzer input provides excellent performance with more than a 90% eye opening with an "ideal" input signal (10 ps transition time).

The analyzer channels can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ω connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ω differential termination. Independently of the selected termination, one can select whether the analysis of the incoming signal is performed on the input, the complimentary input or true differential.

Agilent ParBERT 81250

Agilent N4874A ParBERT 7 Gb/s Generator
Agilent N4875A ParBERT 7 Gb/s Analyzer

Technical Specifications

General

The N4874A generator and N4875A analyzer modules are each one VXI slot wide and operate in a range from 620 Mb/s up to 7 Gb/s. The ParBERT 7 Gb/s modules require the E4809A 13.5 GHz central clock module. All specifications, if not otherwise stated, are valid at the end of the recommended N4910A cable set (24" matched pair 2.4 mm).

The N4874A generator module generates hardware-based PRBS up to 2^{31} - 1, PRWS and user-defined patterns and provides a memory depth of 64 Mbit. The N4875A can synchronize on a 48bit detect word, or on a pure PRBS pattern without detect word.

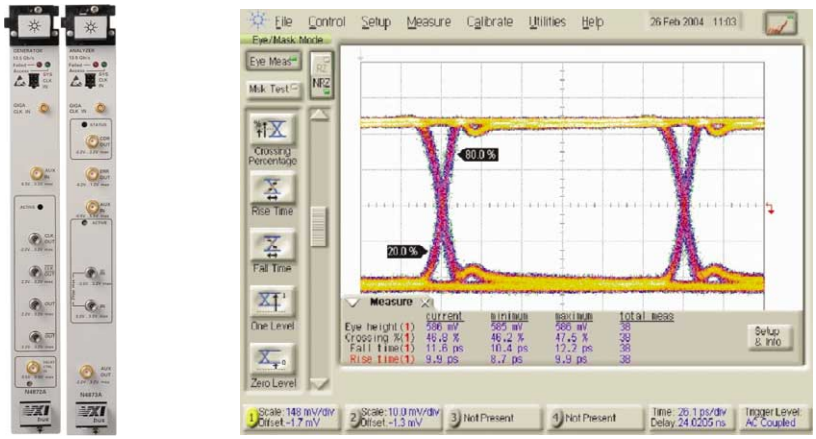


Figure 22. N4874A & N4875A and waveform

Table 31. N4874A data generator timing specifications (@ 50% of amplitude, 50 Ω to GND)

Frequency range	620 MHz to 7 GHz
Delay = start delay + fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 100 ns
Fine delay range	± 1 period (can be changed without stopping)
Delay resolution	100 fs
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement. (@ 25 °C - 40 °C ambient temp.)
Relative delay accuracy	±2 ps ± 2% typ. (@ 25 °C - 40 °C ambient temp.)
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency. (@ 25 °C - 40 °C ambient temp.)

Timing specifications

The ParBERT 13.5 Gb/s modules are able to work with three different clock modes.

- *Internal clock mode:* The common clock mode is provided by the E4809A 13.5 GHz central clock module, which generates clock frequencies up to 13.5 GHz.
- *External clock mode:* The system also works synchronously with an external clock, which is connected to the E4809A clock module.
- *CDR mode:* To use the N4875A 7 Gb/s analyzer CDR capabilities, connect the analyzer's CDR out to the E4809A clock module's clock in.

Sequencing

The sequencer receives instructions from the central sequencer and generates a sequence. The channel sequencer can generate a sequence with up to 60 segments.

An analyzer channel generates feedback signals that can control the channel sequencer and/or the central sequencer. With parallel analyzer channels, the feedback is routed to the central sequencer to allow a common response of all parallel channels. With single receive channel, the channel sequencer itself handles the feedback signals.

Pattern generation

The data stream is composed of segments. A segment can be made up of a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 64 Mbit (at segment length resolution 512 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to $2^{15} - 1$ or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio.

A zero substitution pattern extends the longest zero series by a user selectable number of additional zeroes. The next bit following these zero series will be forced to 1. Mark ratio is the ratio of 1 s and 0 s in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4 and 7/8.

Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 512 the number of repetitions is also 512. That means that a $2^{15} - 1$ PRBS uses up to 16 Mbit of the memory. Hardware-based PRBS can be a polynomial up to $2^{31} - 1$. No memory is used for hardware-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a 0 a 1 is generated and vice versa.

Table 32. N4874A pattern and sequencing

Segment length resolution	512 bit
Patterns:	
Memory based	up to 64 Mbit
PRBS/PRWS	$2^n - 1$, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at $2^n - 1$, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	$2^n - 1$, n = 7, 9, 10, 11, 15
Extended ones or zeros	$2^n - 1$, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
PRWS port width	1, 2 , 4, 8, 16

Table 33. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range (Mbit/s)	Segment length resolution	Maximum memory depth (bits)
620 ... 1.350,000	32 bits	4.194,304
620 ... 2.700,000	64 bits	8.388,608
620 ... 5.400,000	128 bits	16.777.216
620 ... 7.000,000	256 bits	33.554.432
620 ... 7.000,000	512 bits	67.108.864

N4874A generator module

The N4874A generates differential or single-ended data and clock signals operating from 620 Mb/s up to 7 Gb/s. The output levels are able to drive high-speed devices with interfaces like LVDS, ECL, PECL, CML and low voltage CMOS. The nominal output impedance is 50 Ω typical. The delay control IN has a single-ended input with 50 Ω impedance. The input voltage allows modulation of a delay element up to 1 GHz (200 ps) within the generator's differential output. See figure 25c - 26c on page 36.

The AUX IN has a single-ended input with a 50 Ω impedance. The AUX IN allows injecting gating signals. An active (TTL high) signal at the auxiliary input forces (gates) the data to a logic zero.

Data OUT

Table 34. Parameters for N4874A ParBERT 7 Gb/s generator

Data output	1, differential or single ended, 2.4 mm(f)	**(1)**
Range of operation	620 Mb/s - 7 Gb/s	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	-2.00 to +3.00 V	
Short circuit current	72 mA max.	
External termination voltage	-2 V to +3 V	**(2)**
Data formats	Data: NRZ, DNRZ	
Addressable technologies	LVDS, CML PECL - 3.3 V; ECL (terminated to 1.3 V/0 V/-2 V) low voltage CMOS, LVDS, CML	
Transition times (20% - 80%)	< 20 ps	
Jitter	9 ps peak-peak typ.	**(3)**
Cross-point adjustment	20%...80% typ.	

(1) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(2) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(3) Clock out to data out.

Clock OUT

Table 35. Parameters for N4874A ParBERT 7 Gb/s generator

Clock output	1, differential or single-ended, 2.4 mm(f)	**(4)**
Frequency	620 MHz - 7 GHz	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	-2.00 to +2.80 V	
Short circuit current	72 mA max.	
External termination voltage	-2 V to +3 V	**(5)**
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3V/0 V/-2 V) low voltage CMOS	
Transition times (10% - 90%)	< 25 ps	
Jitter	1 ps RMS typ.	
SSB phase noise (10 GHz @ 10 kHz offset, 1 Hz bandwidth)	< - 75 dBc with clock module E4809A typ.	

(4) In single-ended mode, the unused output must be terminated with 50 W to GND.
(5) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.

Delay control IN

Table 36. Parameters for N4874A ParBERT 7 Gb/s generator

Delay control input	Single-ended; DC-coupled; SMA(f)
Input voltage window	-250 mV ... +250 mV (DC-coupled)
Input impedance	50 Ω typ.
Delay range	-100 ps ... +100 ps
Modulation bandwidth	DC ... 1 GHz @ data rate < 10.5 Gb/s

AUX IN

Table 37. Parameters for N4874A ParBERT 7 Gb/s generator

Interface	DC coupled, 50 Ω nominal
Levels	TTL levels
Minimum pulse width	100 ns
Connector	SMA female

N4875A analyzer module

The analyzer features are:

- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the bit error ratio

Receive memory for acquired data is up to 64 Mbit deep, depending on segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum segment resolution (32, 64, 128, 256, 512).

The analyzer is able to synchronize on a received data stream by means of a user selectable synchronization word. The sync. word has a length of 48 bits and is composed of zeros, ones and Xs ("don't cares"). The detect word must be unique within the data stream. Synchronization on a pure PRBS data-stream is done without a detect-word, instead by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity of 50 mV and the common mode range of the comparator allow the testing of all common differential high-speed devices. The user has the choice of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

Table 38. N4875A analyzer timing: all timing parameters are measured at ECL levels, terminated with 50 Ω to GND

Sampling rate	620 MHz to 7 GHz
Sample delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 100 ns
Fine delay range	± 1 period (can be changed without stopping)
Delay resolution	100 fs
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement **(1)**
Relative delay accuracy	±2 ps ± 2% typ. **(1)**
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency. **(1)**

(1) 25 °C - 40 °C ambient temperature

Table 39. N4875A pattern and sequencing

Analyzer auto-synchronization	On PRBS or memory-based data Manual or automatic by: Bit synchronization(2) with or without automatic phase alignment Automatic delay alignment around a start sample delay (range: ± 10 ns) BER Threshold: 10^{-4} to 10^{-9}

(2) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect Word at the beginning of the segment, and the generators must be on a separate system clock. Don't cares within detect word are possible. If several inputs synchromize, the delay diffference between terminals must be smaller than ±5 segment length resolution.

Data IN

Table 40. Parameters for N4875A ParBERT 7 Gb/s analyzer

Number of channels	1, differential or single ended, 2.4 mm (f)
Range of operation	620 Mb/s - 7 Gb/s
Max input amplitude	2 Vpp
Input sensitivity	50 mVpp typical @ 10 Gb/s, PRBS 2^{31} - 1, and BER 10^{-12}
Input voltage range	-2V ... +3 (selectable 2V window)
Internal termination voltage (can be switched off)	-2.0 to +3.0 V (must be within selected 2 V window)
Threshold voltage range	-2.0 to + 3.0 V (must be within selected 2 V window)
Threshold resolution	0.1 mV
Minimum detectable pulse width	25 ps typ.
Phase margin (source: N4874A)	1 UI - 12 ps typ.
Impedance	50 Ω typ. (100 Ω differential, if termination voltage is switched off)
Sampling delay resolution	100 fs

Clock data recovery

The analyzer module has integrated CDR capabilities, which allow the recovery of either clock or data. Before the CDR can lock onto the incoming data stream, the data rate must be defined within the user interface; common data rates are pre-defined. In CDR mode, phase alignment to the center of the eye is done automatically during synchronization. For correct operation, the CDR output must be connected to the clock input of the E4809A central clock module. In addition the generator clock source and the analyzer clock source must be independent.

AUX OUT

The AUX OUT provides data or recovered clock signals.

AUX IN

Gating functionality: if a high level is applied at AUX IN, comparison is disabled and internal counters are stopped. After resuming a low level at AUX IN, comparison is enabled and internal counters continue. The internal sequencing is not stopped.

ERROR OUT

Whenever one or more bit errors are detected, the error out signal is high for one segment resolution. A high period is always followed by a low period (RZ-format) in order to ensure trigger possibility on continuous errors.

Table 41. Parameters for N4875A ParBERT 7 Gb/s analyzer - clock data recovery

Common data rates	S-ATA/FireWire:	6.4 Gbit/s	
	PCI-Express:	6.4 Gbit/s	
	OC-48:	2.488 Gbit/s	
	10GbE:	3.125 Gbit/s	
	SAN:	3.187 Gbit/s	
	S-ATA/FireWire:	3.2 Gbit/s	
Frequency ranges	4.23 GHz ... 6.4 GHz		
	2.115 GHz ... 3.2 GHz		
	1.058 GHz....1.6 GHz		**(1)**
The CDR works with specified PRBS patterns up to 2^{31} - 1,			
The CDR expects a DC balanced pattern,			
The CDR expects a transition density of one transition for every second bit.			

(1) Available for hardware S/N: DE43A00401 and software rev. 5.62

Table 42. Parameters for N4875A 7 Gb/s analyzer - AUX OUT

Interface	AC Coupled, 50 Ω nominal
Amplitude	600 mV nominal
Output jitter (clock @ AUX OUT)	0.01 UI rms typical
Connector	SMA female

Table 43. Upgrades 7 Gb/s - 13 Gb/s

Order No.	Feature
E4860AS-290	Upgrade N4874A to 13.5 Gb/s
E4860AS-291	Upgrade N4875A to 13.5 Gb/s

Table 44. Parameters for N4875A 13.5 Gb/s analyzer - AUX IN

Resolution	Segment resolution
TTL compatible	Internal 500 Ω termination to GND;
Threshold	@ 1.5 V
Connector	SMA female
Low (0...1 V)	Internal counters are enabled
High (2 V...4 V)	Internal counters are stopped
Open	Same as low

Table 45: Parameters for N4875A 13.5 Gb/s analyzer - ERROR OUT

Format	RZ; active high
Output high level	0 V ± 100 mV
Output low level	+1 V ± 100 mV
Connector	SMA female

Ordering information

N4874A ParBERT 7 Gb/s generator module
N4875A ParBERT 7 Gb/s analyzer module
E4809A Central clock module

Accessories:

N4910A 2.4 mm matched cable pair
N4912A 2.4 mm 50 termination male connector
N4913A 4 GHz deskew for E4809A

Technical specifications

All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10 to 40 °C ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ω to ground at ECL levels if not specified otherwise.

Agilent E4861B ParBERT 3.35 Gb/s Data Module
Agilent E4862B ParBERT 3.35 Gb/s Generator Front-End
Agilent E4863B ParBERT 3.35 Gb/s Analyzer Front-End

Technical Specifications

General

A ParBERT 3.35 Gb/s module can house up to two front-ends, either two generators or analyzers or any mix. ParBERT 3.35 Gb/s modules work with the E4808A or E4890A clock modules. The key specifications of ParBERT 3.35 Gb/s modules are:

- 21 MHz ... 3.350 GHz clock/data rate
- 16 Mbit memory depth at each channel
- HW-based PRBS generation up to the polynomial of $2^{31} - 1$
- Analyzer can synchronize on a 48 bit detect word (memory-based data)
- Analyzer can synchronize on a pure PRBS pattern without detect word

Timing capabilities

The frequency range of the modules is 21 MHz ... 3.350 GHz. The ParBERT 3.35 Gb/s front-ends use a multiplying PLL that multiplies system master clock by 4 or 8. Through the clock module, an external clock source can be used. This external clock must run continuously. If the clock signal is interrupted, the multiplying PLLs typically needs 100 milliseconds to lock onto the clock again.

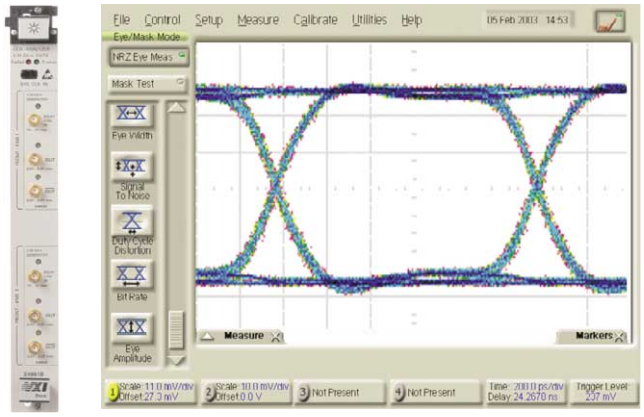


Figure 23. E4861B data module and E4862B generator front-end with waveform

Table 46. E4861B data generator timing specification (@ 50% of amplitude, 50 Ω to GND)

Frequency range	20.834 MHz to 3.350 GHz
Delay = start delay + fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 200 ns (not limited by period)
Fine delay range	±1 period (can be changed without stopping)
Delay resolution	1 ps
Accuracy data mode	±25 ps ±50 ppm relative to the zero-delay and temperature change within ±10 °C after autocalibration
Clock mode	±50 ps ±50 ppm relative to the zero-delay
Skew between modules of same type (data mode)	50 ps typ. after deskewing at customer levels and unchanged system frequency

The variable delay is available in data mode and pulse mode. In clock mode the timing is fixed.

Sequencing

The sequencer receives instructions from the clock module. The channel sequencer can generate a sequence with up to 60 segments. An analyzer channel can generate feedback signals which are combined in the clock module for a common response of all parallel channels. With a single receiver channel the channel sequencer itself handles the feedback signals.

Table 47. E4861B analyzer timing all timing parameters are measured at ECL levels, terminated with 50 Ω to GND

Sampling rate	20.834 MHz to 3.350 GHz
Sample delay	Same as delay = start delay + fine delay
	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 200 ns (not limited by period)
Fine delay range	±1 period (can be changed without stopping)
Resolution	1 ps
Accuracy	±25 ps ±50 ppm relative to the zero-delay and temperature change within ±10 °C after autocalibration
Skew	50 ps typ. after deskewing at customer levels and unchanged system frequency

Table 48. E4861B pattern and sequencing

Patterns	
Memory based	Up to 16 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
Analyzer auto-synchronization	On PRBS or memory-based data Manual or automatic by: Bit synchronization(1) with or without automatic phase alignment. Automatic delay alignment around a start sample delay (range: ± 10 ns) BER threshold: 10^{-4} to 10^{-9}

(1) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect word at the beginning of the segment, and the generators must be on a separate system clock. "Don't cares" within detect word are possible. If several inputs synchromize, the delay diffference between terminals must be smaller than ±5 segment length resolution.

Table 49. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mb/s	Segment length	Maximum memory resolution depth, bits
20.834 ... 41.666	1 bit	131,072
20.834 ... 82.333	2 bits	262,144
20.834 ... 166.666	4 bits	524,288
20.834 ... 333.333	8 bits	1,048,576
20.834 ... 666.666	16 bits	2,097,152
20.834 ... 1,333.333	32 bits	4,194,304
20.834 ... 2,700.000	64 bits	8,388,608
20.834 ... 3,350.000	128 bits	16,777,216

Table 50. Dependancy of PRWS generation and port width.

Almost all the combinations are possible except the following:

PRWS	Port width
2^7 - 1	No restriction
2^9 - 1	7
2^{10} - 1	3, 11, 31, 33
2^{11} - 1	23
2^{15} - 1	7, 31
2^{23} - 1	47
2^{31} - 1	No restriction

Pattern generation

The data stream is composed of segments. A segment can be a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 16 Mbit (at segment length resolution 128 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15} - 1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio. A zero substitution pattern extends the longest zero series by a user-selectable number of additional zeros. The next bit following these zero-series will be forced to 1. Mark ratio is the ratio of ones and zeros in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4, 7/8. Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 128 the number of repetitions is also 128. That means that a 2^{15} - 1 PRBS uses up to 4 Mbit of the memory. Hardware-based PRBS can be any polynomial up to 2^{31} - 1. No memory is used, so the total memory is free for memory-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a '0' a '1' is generated and vice versa. Single errors can be inserted by pod or via instruction from the central sequencer. The user can trigger an error with a signal supplied to the qualifier pod of the central module. An error insertion with a fixed rate and a fixed distribution is supported. The user software allows the selection of errored and error-free segments.

Generator front end (E4862B)

The amplifier generates a differential output signal. Each output can be individually switched on and off. The output levels are sufficient to drive typical high-speed devices with interfaces like ECL, PECL, LVDS and DVI levels. The nominal output impedance is 50 Ω. The delay control In has a single-ended input with 50 Ω impedance. The input voltage modulates a delay element within the generator's differential output. The user has the option of turning the delay control in feature on or off. Additionally the user can select between two delay ranges.

Table 51. Parameters for generator front-ends E4862B 3.35 Gb/s

Outputs	1, differential or single-ended	
Impedance	50 Ω typ.	
Data formats	Data: NRZ, DNRZ, RZ, R1	
Pulse mode		
Range	150 ps to (1UI - 150 ps)	
Sampling delay resolution	1 ps	
Width accuracy	40 ps typ.	
Output voltage window	-2.00 to +3.5 V	**(1)**
Ext. term. voltage	-2.00 to +3.5 V	**(2)**
Absolute maximum external voltage	-2.2 V to +3.2 V	
Addressable technologies	LVDS, CML, PECL, ECL low voltage CMOS	
Amplitude/resolution	0.05 Vpp ... 1.8 Vpp/10 mV	
Accuracy hi level/amplitude	±2% ±10 mV	
Short circuit current	72 mA max.	
Transition times (20% - 80%)	< 75 ps; 60 ps typ.	
Overshoot/ringing	5% +10 mV typ.	
Jitter, NRZ data mode	< 30 ps peak-peak	**(3)**
Clock mode	< 2 ps rms	**(3 & 4)**
Pulse, RZ, R1 mode	30ps peak-peak typ.	**(3 & 4)**
Cross-point adjustment (Duty cycle distortion)	30% ... 70% (in NRZ mode only)	

(1) For output voltages > 3 V the termination voltage ≥ 3 V needs to be applied.
(2) External termination voltage must be less than 3 V below VOH. and less than 3 V above VOL. Termination into AC is possible.
(3) Measured with E4808A clock module.
(4) Specified as intra channel jitter.

Table 52. Delay control in

Input voltage window	-500 mV to +500 mV (DC-coupled)
Delay range 1	-250 ps to +250 ps
Delay range 2	-25 ps to +25 ps
Modulation bandwidth	DC to 200 MHz
Input impedance	50 Ω (typ.)

Analyzer front end (E4863B)

The analyzer features are:
- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the bit error ratio

The receive memory for acquired data is up to 16 Mbit deep, depending on the segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum granularity.

The analyzer is able to synchronize on a received data stream by means of a user-defined detect word. The detect word is defined by the first bits within the expected segment, it has a length of 48 bits and is composed of zeros, ones and Xs ("don't cares"). The detect word must be unique within the data stream. Synchronization on a pure-PRBS data-stream is done without a detect-word, by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity is down to 50 mV and the common mode range of the comparator allows the testing of all common differential high-speed devices.The user has the option of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

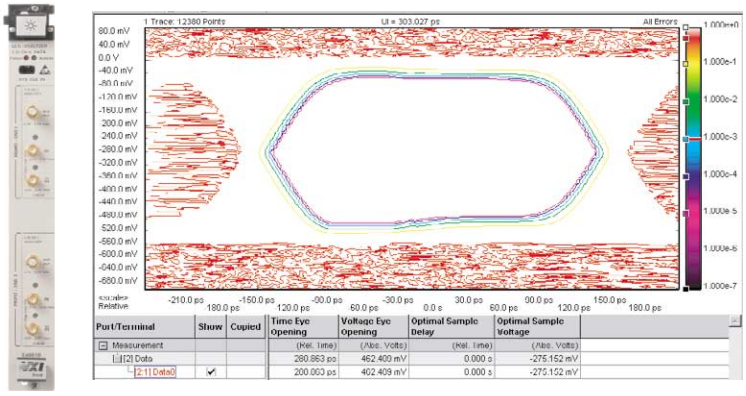


Figure 24. E4861B Data module and E4863B analyzer with eye diagram

Table 53. Parameters for analyzer front-ends E4863B 3.35 Gb/s

Number of channels	1, differential or single-ended	
Impedance	50 Ω typ. (100 Ω differential if termination voltage is switched off)	
Internal termination voltage (can be switched off)	-2.0 to +3.0 V	
Threshold voltage range	-2.0 to +3.0 V	
Threshold resolution	1 mV	
Threshold accuracy	±20 mV ±1%	
Input sensitivity (single-ended and differential)	< 50 mV	
Minimum detectable pulse width	< 150 ps	
Maximum input voltage range	Three ranges selectable: -2 V to +1 V -1 V to +2 V 0 V to 3 V	
Maximum differential voltage	1.8 V	
Phase margin with ideal input signal	> 1 UI - 30 ps	**(1)**
Phase margin with E4862B generator	> 1 UI - 50 ps	**(1)**
Auxilary out	V out: 350 mV pp typ., AC coupled	**(2)**
Sampling delay resolution	1 ps	

(1) Measured with E4808A central module
(2) Terminate with 50 Ω to GND, if not used

Protection

Input and output relays switch off automatically, if the absolute maximum voltage window is exceeded.

Typical waveform pictures

Eye Plots

The 3.35 Gb/s generator output is designed for clean and fast output signals. It offers a swing of 50 mV to 1.8 V within the voltage window suited for testing LVDS, CML, (P)ECL and SSTL 0 - 3.3 V technologies.

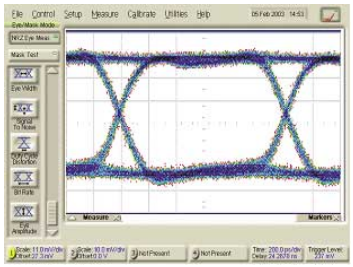


Figure 25a. 3.35 Gb/s Generator: 50 mVpp

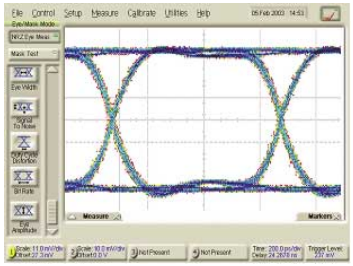


Figure 25b. 3.35 Gb/s Generator: 1.8 V pp

Crossing Point

The 3.35 Gb/s generator allows a variable cross-over for differential signals. The cross-over can be programmed by the user interface or remote program between 30 and 70%.

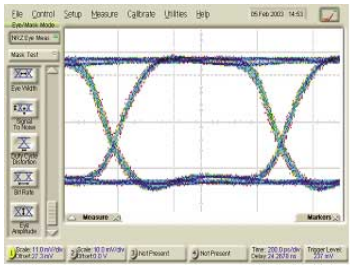


Figure 25c. 3.35 Gb/s Generator @30%

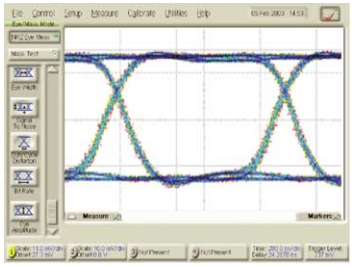


Figure 25d. 3.35 Gb/s Generator @70%

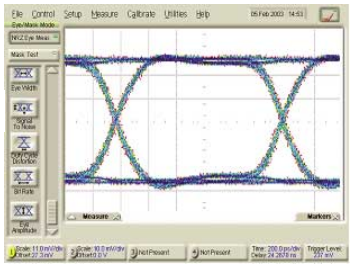


Figure 25e. 3.35 Gb/s Generator @50%

Jitter Modulation Examples

The 3.35 Gb/s generator has a control input for modulating the delay with the help of an external signal. This modulation can be used to emulate jitter. The picture shows this modulatioin for different types of control voltages. The modulation can be used to test a DUT for jitter tolerance.

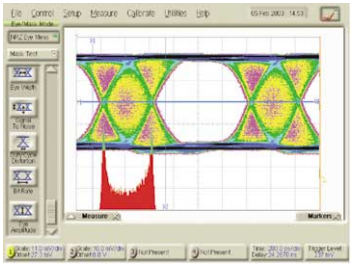


Figure 26a. Jitter modulated with sine wave

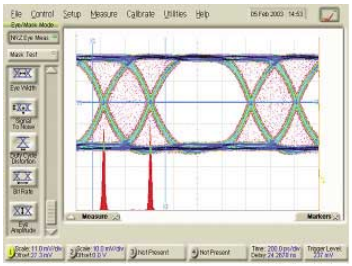


Figure 26b. Jitter modulated with rectangle wave

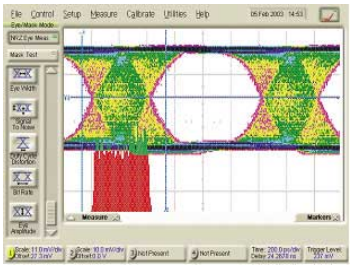


Figure 26c. Jitter modulated with triangle wave

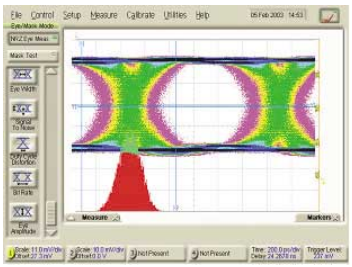


Figure 26d. Jitter modulated with noise generator

Agilent E4861A ParBERT 2.7 Gb/s / 1.65 Gb/s Data Module
Agilent E4862A ParBERT 2.7 Gb/s Generator Front-End
Agilent E4863A ParBERT 2.7 Gb/s Analyzer Front-End

Agilent E4864A ParBERT 1.65 Gb/s Generator Front-End
Agilent E4865A ParBERT 1.65 Gb/s Analyzer Front-End
Technical Specifications

E4861A generator/analyzer module

This module holds any combination of up to two analyzer front-ends (E4863A, E4865A) and generator front-ends (E4862A, E4864A).

With front-ends E4864A and E4865A the maxiumum speed is limited to 1.65 Gbit/s. The maximum speed of 2.7 Gbit/s is achieved with front-ends E4862A and E4863A.

Clock module/data mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a pulse port. Data mode is achieved when using it as a data port. In Clock mode there is a fixed duty cycle of 50%. In data mode there is NRZ format with variable delay. The analyzer always works as data port with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ±1 period without stopping.

Figure 27. E4861A module

Table 54. E4861A data generator timing specifications (@ 50% of amplitude, 50 Ω to GND)

Frequency range(1)	Clock/data mode 333.334 Mb/s to 2.70 Gb/s (1.65 Gbit/s E4864A, E4865A)
Delay (between channels)	Can be specified as leading edge delay in fraction of bits in each channel
Range	0 to 300 ns (not limited by period)
Resolution	1 ps
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement. (From 20 °C to 35 °C without autocol)
	±80 ps ±50 ppm typ. relative to the zero-delay placement and temperature change within ±5 °C after autocalibration
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency
Pulse width	50% of period typ. in clock mode

(1) See tables for front-end deratings

Data capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator for a pattern stimulating. on an analyzer it defines the expected pattern which the incoming data are compared to. The expected pattern can be set up with mask bits.

The segment length resolution is the resolution to which the length of a pattern segment or mask can be set. The maximum memory per channel of the E4861A can be set in steps of 64 bits up to a length of 8192 kbits. If the 64 bit segment length resolution is too coarse, memory depth and frequency can be traded.

Table 55. E4861A analyzer timing all timing parameters are measured at ECL and levels, terminated with 50 Ω to GND

Sample delay = start delay + fine delay, fine delay can be changed without stopping	
Sampling rate(1)	Same as generator
Fine delay range	±1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

(1) See tables for front-end de-ratings

Table 56: E4861A pattern and sequencing

Patterns:	
Memory based	Up to 8 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
User	Data editor, file import
Analyzer auto-synchronization:	On PRBS or memory-based data manual or automatic by: Bit synchronization (2) with or without automatic phase alignment Automatic delay alignment around start sample delay (range: ±10 ns) BER threshold: 10^{-4} to 10^{-9}

(2) Bit synchronization on data is achieved by detecting a 48 bit unique word at the beginning of the segment. "Don't cares" within the detect word are possible. In this mode no memory-based data can be sent within the same system. If several inputs synchronize, the delay difference between the terminals must be smaller than ±5 segment length resolution. Not supported for mark density, errored PRBDS/PRWS and extended ones or zeroes patterns.

Table 57. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range M/bits	Segment length resolution	Maximum memory depth, bits
333.334...666.666	16 bits	2,097,152
666.667...1,333.333	32 bits	4,194,304
1,333.334...2,666.667	64 bits	8,388,608

In general it is possible to set higher values for the segment length resolution and also at lower frequencies than are indicated in the table.

Table 58. Depending on the capability of generating PRWS and port width, almost all the combinations are possible except the following:

PRWS	Port width
2^7 - 1	No restriction
2^9 - 1	7
2^{10} - 1	3, 11, 31, 33
2^{11} - 1	23
2^{15} - 1	7, 31
2^{23} - 1	47
2^{31} - 1	No restriction

Sub-frequencies

For applications requiring different frequencies at a fraction of the system clock, the rate can be divided or multiplied by 1, 2 or 4. This influences the dependency between segment length resolution and maximum memory depth.

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The sychronization can be performed on PRBS/PRWS and memory-based data but it is not possible on a mix of PRxs and memory-based data.

There are two types of synchronization
- Bit synchronization
- Auto delay aligment

Bit synchronization is possible to cover a bit alignment for a totally unknown number of cycles. Using memory-based data, the first 48 bits within the expected data segment will work as detect word, which the incoming data is compared to. Analysis begins when the incoming data match the detect word.

Auto delay aligment is performed by using the analyzer sampling delay. The sampling delay range is ±10 ns.

Using auto delay, alignment provides synchronization with an absolute timing relation between a group of analyzer channels. So skew measurements are possible.

Input/output

Addressable technologies

LVDS, ECL (terminated with 50 to 0 V/-2 V), PECL (terminated to +3 V analyzer input requires use of a bias tee).

Analyzer input

The analyzer channel can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ω connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ω differential termination. Independent of the selected termination, there is the choice of whether the anaylsis of the incoming signal is performed on the input or true differential. For connecting to PECL it is recommended that a bias tee is used. The 2.7 Gb/s analyzer offers an auxiliary output, where the differential input signal is available as a single-ended signal. The bandwidth of the Aux output is limited to 2 GHz.

Generator output

The generator output can be used as single-ended or differential. Enable/disable relays provide on/off switching. When switched off, internal termination is provided. It is recommended that unused outputs are either turned off or externally terminated.

The generator outputs can work into 50 Ω center tapped termination or 100 Ω differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

Table 59. Parameters for analyzer front-ends E4863A 2.7 Gb/s (E4865A 1.65 Gb/s)

Number of channels	1, differential or single ended
Impedance	50 Ω typ. 100 Ω differential if termination voltage is switched off
Internal termination voltage (can be switched off)	-2.0 to +3.0 V
Threshold voltage range	2.0 to + 3.0 V
Threshold resolution	2 mV
Threshold accuracy	± 1% ±20 mV
Input sensitivity (single-ended and differential)	50 mV typ
Minimum detectable pulse width	180 ps typ. at ECL levels
Maximum input voltage range	Three ranges selectable: -2 V to + 1 V -1 V to +2 V 0 V to 3 V
Maximum differential voltage	1.8 V operating max. 3 V
Delay resolution	1 ps
Phase margin, with ideal input signal with generator E4862A	> 1 UI - 50 ps > 1 UI - 75 ps
Auxiliary out	Swing: 400 mV pp typ., AC coupled

Table 60. Parameters for generator front-ends E4862A 2.7 Gb/s (E4864A 1.65 Gb/s)

Outputs	1, differential or single ended
Impedance	50 Ω typ.
Formats	Clock: duty cycle 50% ±10% typ. Data: NRZ, DNRZ
Output voltage window	-2.00 to + 3.00 V 3.00 V to 4.5 (terminated to +3V only)
Maximum external voltage	- 2.2 to +4.7 V
External termination voltage	-2 V to +3 V
Amplitude/resolution	low voltage CMOS 0.05 to 1.8 Vpp (1) / 10 mV
Accuracy hi level/amplitude	±2% ±10 mV
Short circuit current	72 mA max
Transition times (20% - 80%)	90ps typ @ ECL,LVDS 110 ps typ @ Vpp max
Overshooting/ringing	20% + 20 mV typ
Jitter, data mode **clock mode**	< 50 ps peak-to-peak < 5 ps, rms

(1) Doubles into open, but outputs may switch off if outside limits

Protection

Input and output relays switch off automatically if maximum voltages are about to be exceeded.

Agilent E4832A ParBERT 675 Mb/s Data Module
Agilent E4838A ParBERT 675 Mb/s Generator Front-End
Agilent E4835A ParBERT 675 Mb/s Analyzer Front-End

Technical Specifications

E4832A 675 Mb/s generator/analyzer module

This module holds any combination of up to two analyzer front-end pairs (E4835A) and four generator front-ends (E4838A).

Clock module/data mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a pulse port. Data mode is achieved with assigning it to a data port. In clock mode it is a fixed duty cycle of 50%. In data mode it is NRZ format with variable delay. The analyzer only works as a data port whenever used with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ±1 period without stopping.

Data capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator, and for stimulating a pattern. On an analyzer, it defines the expected pattern which the incoming data are compared to. The expected pattern can contain mask bits.

The segment length resolution is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4832A can be set in steps of 16 bits up to a length of 2048 Kbit. If the 16-bit segment length resolution is too coarse, memory depth and frequency can be traded.

Sub-frequencies

For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2, 4, 8, or 16. This influences the dependency between segment length resolution and maximum memory depth.

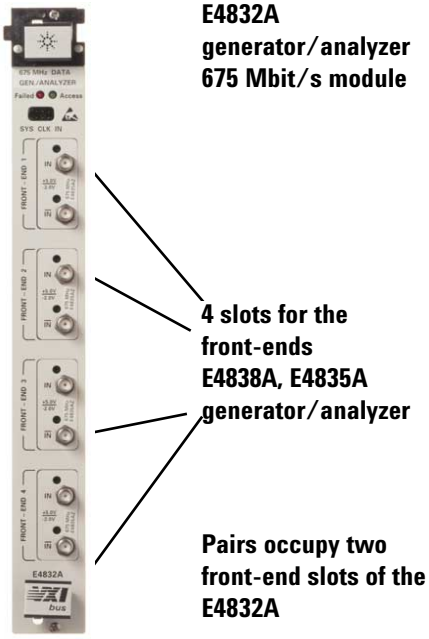


Figure 28. E4832A module

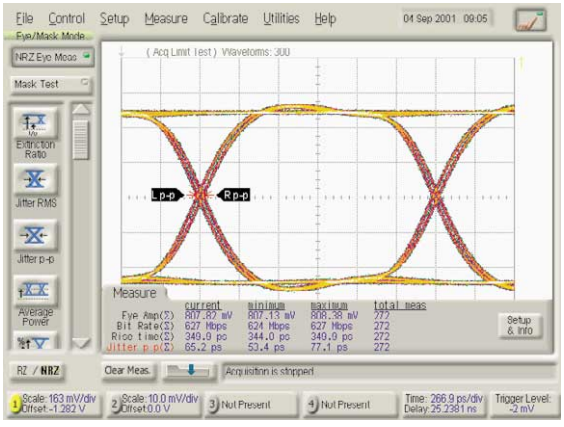


Fig 29. Wave diagram of E4832A generator

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The sychronization can be performed on PRBS/PRWS and memory-based data but it is not possible on a mix of PRxs and memory based data.

There are two types of synchronization:
- Bit synchronization
- Auto delay alignment

Bit synchronization is possible to cover a bit alignment for a totally unknown number of cycles. Using memory-based data, the first 48 bits within the expected data segment will work as a detect word which the incoming data are compared to. When the incoming data match with this detect word, analysis will begin.

Auto delay alignment is performed by using the analyzer sampling delay. The sampling delay range is ±50 ns while this is possible.

Using auto delay alignment provides synchronization with an absolute timing relation between a group of analyzer channels. This makes skew measurements are possible.

Table 61. E4832A data generator timing specifications (@ 50% of amplitude, 50 Ω to GND and fastest transition times)

Frequency range	333,334 kHz to 675 MHz
Delay range	0 to 3.0 µs (not limited by period)
Sampling delay resolution	2 ps
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement (1)
Skew	50 ps typ. after deskewing at customer levels
Pulse width	Can be specified as width or % of duty cycle
Range	750 ps to (period -750 ps)
Resolution	2 ps
Accuracy	±200 ps ±0.1%
Duty cycle	1% to 99%, subject to width limits

(1) Valid at 15 to 35 °C room temperature

Table 62. E4832A analyzer timing all timing parameters are measured at ECL and levels terminated with 50 Ω to GND

Sample delay = start delay + fine delay	
Fine delay can be changed without stopping (2)	
Sampling rate (3)	333,334 Kb/s to 675 Mb/s
Fine delay range	±1 period
Sampling delay range	0 to 3.0 µs (not limited by period)
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement (3)
Resolution	2 ps
Skew	50 ps typ. after deskewing at customer levels

(2) Conditions: frequency > 20.8 MHz and by using the finest segment length resolution.
(3) See tables for front-end deratings

Table 63. Pattern and sequencing features of E4832A

Patterns:	
Memory based	Up to 2 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
User	Data editor, file import
Analyzer auto-synchronization (2):	On PRBS or memory-based data manual or automatic by: Bit synchronization (1) with or without automatic phase alignment Automatic delay alignment around start sample delay (range: ±50 ns) BER threshold: 10^{-4} to 10^{-9}

(1) Bit synchronization on data is achieved by detecting a 48 bit unique word at the beginning of the segment. "Don't cares" within the detect word are possible. In this mode no memory-based data can be sent within the same system. If several inputs synchronize, the delay difference between the terminals must be ±5 segment length resolution.
(2) Condition: frequency > 20.8 MHz and by using the finest segment length resolution.

Table 64. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mb/s	Segment length	Maximum memory resolution depth, bits
20.834 ... 41.666	1 bit	131,008
41.667 ... 83.333	2 bits	262,016
83.334 ... 166.666	4 bits	524,032
166.667 ... 333.333	8 bits	1,048,064
333.334 ... 666.667	16 bits	2,097,152

In general, it is possible to set higher values for the segment length resolution and also at lower frequencies than are indicated in the table. In this case the fine delay function and the auto-synchronization function are unavailable.

Table 65. Depending between the capability of generating PRWS and port width, almost all the combinations are possible except the following:

PRWS	Port width
2^7 - 1	No restriction
2^9 - 1	7
2^{10} - 1	3, 11, 31, 33
2^{11} - 1	23
2^{15} - 1	7, 31
2^{23} - 1	47
2^{31} - 1	No restriction

Input/output

Addressable technologies

LVDS, (P)ECL, TTL, 3.3 V CMOS

Analyzer input

The analyzer channel can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ω connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ω differential termination. Independent of the selected termination, there is the choice of whether the anaylsis of the incoming signal is performed on the input or true differential.

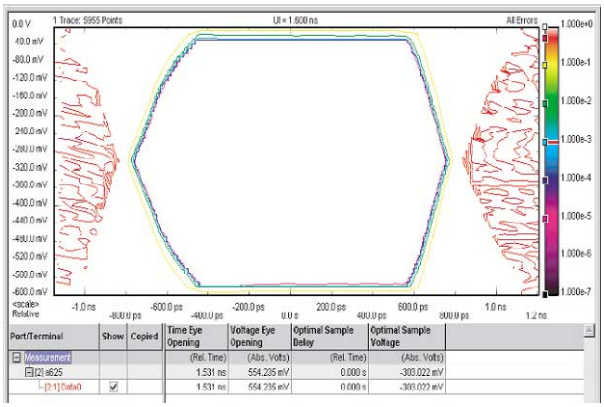


Fig 30. Eye diagram of E4835A analyzer

Table 66. Level parameters for differential generator front-end E4838A 675 Mb/s

Number of channels	1, differential
Impedance	50 Ω typ.
Data formats	RZ, R1, NRZ, DNRZ
Output voltage window	-2.2 to +4.4 V (doubles into open up to max. 5 Vpp)
Amplitude/resolution	0.1 V to 3.50 V / 10 mV
Level accuracy	±3% ± 25 mV typ. after 5 ns settling time
@ LVDS/(P)ECL	±1% ±25 mV typ. after 5 ns settling time
Variable transition time range (10 - 90% of amplitude)	0.5 to 4.5 ns
Accuracy	±5% ±100 ps
@ LVDS/(P)ECL (20 - 80% of amplitude)	0.35 ns typ
Overshoot/ringing	< 7% (< 5% typ).
Jitter	
Data mode	< 100 ps peak to peak (80 ps typ)
Clock mode	8 ps rms typ.
Channel addition	XOR and analog

Table 67. Two differential analyzer front-ends E4835A (1), 667 MSa/s

Number of channels	2, differential or single-ended (switchable)
Impedance	50 Ω typ. 100 Ω differential if termination voltage is switched off
Termination voltage (can be switched off)	-2.0 to +3.0 V
Threshold voltage range/ threshold accuracy	-2.00 to +4.50 V/±1% ±20 mV
Threshold resolution	2 mV
Input sensitivity	Differential 50 mV typ Single-ended 100 mV typ
Minimum detectable pulsewidth	400 ps typ. at ECL levels
Input voltage range	Two ranges selectable: 0 to +5 V and -2 to +3 V
Phase margin with ideal input signal	> 1 UI - 100 ps
with E4838A generator	> 1 UI - 180 ps

(1) Occupy two front-end slots of the E4832A. The E4835A contains two front-ends (E4835AZ) and one common data back end. In this document one front-end is referred to as E4835A.

Agilent ParBERT 81250

Agilent E4809A 13.5 GHz Central Clock Module
Agilent E4808A High Performance Central Clock Module
Agilent E4805B 675 MHz Central Clock Module

Technical Specifications

Each ParBERT 81250 system consists of at least one clock module, which generates the system clock for at least one generator or analyzer or any mix. Please see the table to the right for a complete compatibility overview.

Sequencing
The sequencing can be used to specify the data flow:
- Single
- Looped
- Infinite loop
- Event handling (branch)
- Synchronization

Event handling
With event handling, the flow of data generation and analysis can be controlled with external signals at run time.

Usage of events
- Start and stop of data
- Match loop
- Integration with other equipment (ATE)
- Trigger on error

Table 68. Modules/central clock

	E4805B	E4808A	E4809A
E4832A - ParBERT 675 Mb/s	•	•	•
E4861A - ParBERT 2.7/1.6 Gb/s	•	•	
E4861B - ParBERT 3.35 Gb/s		•	•
E4810A/11A - ParBERT 3.3.5 Gb/s optical		•	
E4866A/67A - ParBERT 10.8 Gb/s		•	
N4872A/73A - ParBERT 13.5 Gb/s			•
E4868B/69B - ParBERT 45 Gb/s		•	
E4874A/75A - ParBERT 7 Gb/s			•

Table 69. E4809A, E4808A and E4805B sequencing features

Number of segments	1 to 30 (every segment looped once) 1 to 60 (no segment looped)
Looping levels	Up to 4 nested loops plus one optional infinite loop Loops can be set independently from 1 to 2^{20} repetitions
Start/stop	External input, manual, programmed (stop with E4832A only)
Event handling	React on internal and external events.

Table 70. E4809A, E4808A and E4805B event handling

Event trigger sources
Events can be defined as any combination of the following sources.
A maximum of 10 events can be defined.
- 8-line trigger input pod for TTL signals
- VXI trigger lines TO and T1
- Any capture error/or no error detected by one of the analyzer channels
- Software command control: an event trigger command issued locally or remotely

Reactions to an event can be set per data segment immediately or deferred and can be any combination of:
- Data segment jump
- Launch trigger pulse at trigger output of the clock module
- VXI trigger lines TO and T1 can be set to 01, 10 or 11

Master slave, multi-mainframe, different clock groups

Up to 3 clock modules can be combined to run in one clock grouping by connecting the master slave cable. This is used to combine channels which do not fit into one frame into one clock group. Omitting the master-slave connection will run the channels as separate clock groups. A system can be a combination of multiple clock groups made up of multiple channels. The frequencies used can be totally asynchronous or m/n ratio (see clock input multiplier/divider). For separated clock groups the master slave is not used. Within one system the modules must be the same type.

Table 71. E4809A, E4808A and E4805B trigger pod characteristics

Input lines	8, single-ended	
Input levels	TTL compatible	
Input threshold	1.5 V	
Input termination	5k Ω pullup to +5 V	
Absolute max ratings for		
input voltages	-1.2 V to + 7.0 V	
Cable delay	11 ns typical	
sampling clock frequency	system frequency/segment length resolution	
	TRIGGER OUTPUT	CLOCK/REF INPUT
Setup time (1)	2.5 ns	-12.5 ns
Hold time (1)	5 ns	20 ns

(1) Includes the cable delay

E4809A 13.5 GHz central clock module

General

E4809A is a 2-slot central clock module with 13GHz clock distribution. ParBERT 81250 13.5 Gb/s modules are designed to run with the E4809A 13.5 GHz central clock module.

Table 72. E4809A clock module specifications

Frequency range	20.834 MHz...13,5 GHz	
Resolution	1 Hz	
SSB phase noise (at 10 kHz offset)	< -75 dBc at 10 GHz	
Latency external start input		
• **Start IN to Trig OUT with 7/13.5 Gb/s**	16 ns + (2 * system clock * segment resolution) ± 1 clock	**(1)**
• **Start IN to Data OUT with 7/13.5 Gb/s**	416 ns + (2 * system clock * segment resolution) ± 1 clock	**(1)**
• **IN to Trig OUT without 7/13.5 Gb/s**	16 ns ± 1 clock	**(1)**
• **IN to Data OUT without 7/13.5 Gb/s**	48 ns ± 1 clock	**(1)**

(1) Add 3 ns if expander frame is used

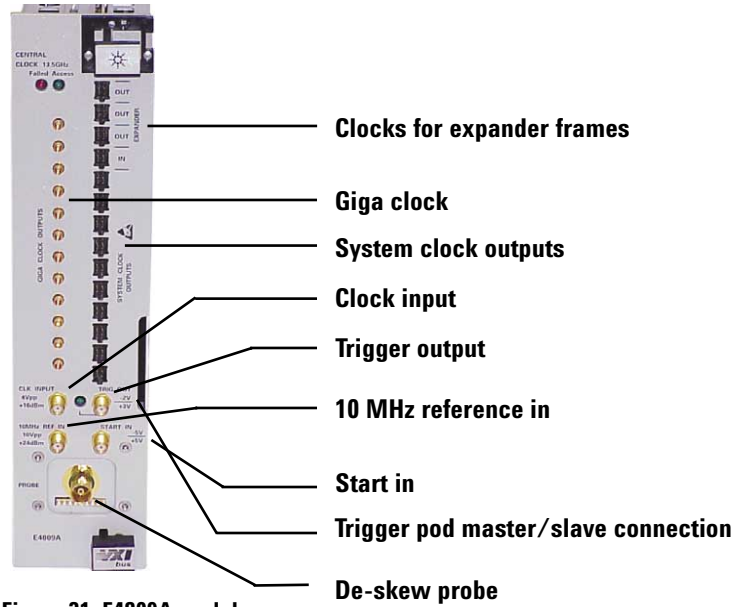


Figure 31. E4809A module

Timing capabilities

The E4809A supports three different operation modes.

E4809A as system clock
The E4809A distributes clock signals to connected modules in the range from 20.834 MHz up to 13.5 GHz. The E4809A provides Giga-clock signals in a range from 500 MHz up to 13.5 GHz to the ParBERT 81250 13.5 Gb/s modules (N4872A, N4873A). All other supported modules work using the E4809A master clock.

External clock mode
The system will run synchronously to an external clock, which is connected to the clock module's clock input. There are two different sub-modes available. In the **direct** clock mode, the PLL (phase locked loop) is bypassed and an external clock signal can be distributed to all Giga-clock connected modules. This direct external clock mode operates in a range from 500 MHz to 13.5 GHz. In this mode the external clock may be FM or PM modulated. In the **indirect** external clock mode, the clock modules' internal PLL is used to generate flexible master clock and Giga-clock signals.

Clock data recovery (CDR) mode
If the CDR is used, the CDR out of the analyzer must be connected to the clock input of the clock module.

Start input

A sequence of generated data can be started by an external signal.

Table 73. Start input

Start input	DC coupled; 3.5 mm (f)
Threshold range	-1.40 V to +3,70 V
Zin/termination voltage	50 Ω typ./-2 V to +3 V
Sensitivity/max. levels	200 mVpp / -3 V...+6 V

Reference input

The reference input allows ParBERT to run synchronously with an external 10 MHz clock. A continuous clock is necessary. A burst clock can not be used as an external clock.

Table 74. Reference input

Reference input	AC coupled; 3.5 mm(f)
Frequency	10 MHz
Input transition time	< 20 ns
Required duty cycle	50% ±10
Imput impedence	50 Ω
Sensitivity	200 mVpp
Required input phase noise	< -137 dBc @ 10 MHz offset

Clock input

This input runs ParBERT synchronously with an external clock. Usage of a continuous clock is necessary. A burst clock can not be used as an external clock. Two modes are selectable: Indirect external clock mode (clock module PLL is used) and Direct external clock mode (clock module is bypassed).

Table 75: Clock input

Clock input	AC coupled; 3.5 mm (f)
Frequency range	
Indirect mode	20.834 MHz...13.5 GHz
Direct mode	620 MHz...13.5 GHz
Clock input (indirect mode only)	m = 1...256; n = 1...256
Multiplier(m)/divider(n)	m x n < = 1024; clock > = 5 MHz
Input transition/slope	30 ps typ.
Zin	50 Ω
Sensitivity	< 150 mV
Required input phase noise	< 75 - 20 log (13.5 GHz / input frequency) dBc / Hz

Trigger output

The trigger output is used to deliver a trigger signal to a DUT, a digital communication analyzer (Agilent 86100A/B/C Series) or as a stimulus for the analyzer de-skew.

Table 76. Trigger output

Trigger output	DC coupled, SMA (f)
Frequency	Up to 675 MHz
Output transition/slope	70 ps typ. 10/90
Zout/termination voltage	50 Ω/-2 to +3 V
Output voltage window	-2 V to +3 V
Output level	0.1 to 1.8 Vpp

E4805B and E4808A central clock modules

The central clock module includes a PLL (phase-locked loop) frequency generator to provide a system clock. Depending on the frequency chosen, the data modules can be clocked at a ratio of 1, 2, 4, 8, 16, 32, 64 or 256 times higher or lower than the system clock.

External start/stop: The data can be started by an external signal applied to the external input. When using the E4832A module, a stop mode and a gate mode is also available.

Ext. clock/ext. reference: This input runs ParBERT 81250 synchronously with an ext. clock, or when a more accurate reference is needed than the internal oscillator. A continuous clock is necessary. A burst clock cannot be used as an external clock. Maximum external clock is 2.7 GHz for the E4805B and 10.8 Gb/s for the E4808A. (Note: no improvement of jitter specifications will be achieved with an external clock).

Guided de-skew: Individual semi-automatic deskew per channel is available. The 15447A deskew probe 15447A allows deskew on the DUT's (device under test) fixture.

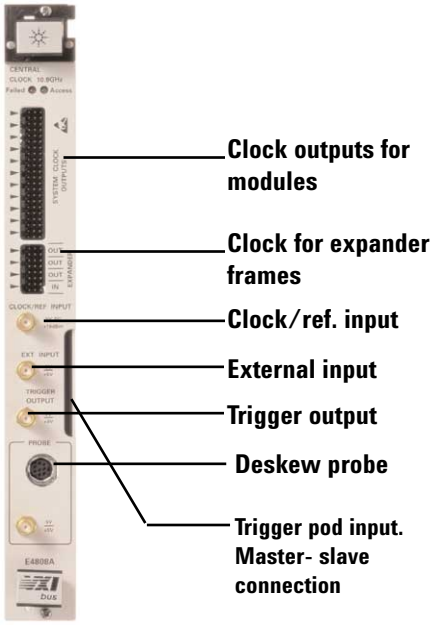


Figure 32: Clock module

Table 77. E4805B and E4808A clock module specifications

	E4805B	E4808A
Frequency range (1) (can be entered as period or frequency)	1 kHz to 675 MHz	170 kHz to 675 MHz
will run with	• E4861A in range of 334 MHz to 2.7GHz • E4832A in range of 334 KHZ to 675 MHz	• E4866A/E4867A in range of 9.5 GHz to 10.8 GHz • E4861B in range of 20.834 MHz to 3.35 GHz • E4861A in range of 334 MHz to 2.7 GHz • E4832A in range of 334 KHZ to 675 MHz
Resolution	1 Hz	1 Hz
Accuracy	±50 ppm with internal PLL reference	±50 ppm with internal PLL reference

(1) May be limited or enhanced by modules or frontends

Table 78. External input and ext. clock/ext. ref. input

	E4805B		E4808A	
Zin/termination voltage	50 Ω/-2.10 V to 3.30 V		50 Ω /-2.10 V to 3.30 V	
Sensitivity/max levels	400 mVpp/-3 V to + 6 V		200 mVpp/-3 V to + 6V for < 9.5 Gbit/s 300 mVpp/-3 V to+ 6 V for > 9.5 Gb/s	
Coupling **Ext. input:**	dc, Threshold range: -1.40 V to +3.70 V		dc, -1.40 V to +3.70 V	
Ext. clock/ext. ref:	ac		ac	
Input transitions/slope	< 20 ns. ext. input active edge is selectable		< 20 ns. ext. input active edge is selectable	
Clock input multiplier(m)/divider (n)	m = 1...256; n = 1...256 m*n < = 1024 m/n * input frequency must fit data range input frequency/n > = 1.3 MHz			
PLL lock time	100 ms		100 ms	
Input frequency/period **Ext. clock**	170 kHz - 2.7 GHz		170 kHz - 10.8 GHz	
Ext. ref	1(1), 2(1), 5, or 10 MHz		1(1), 2(1), 5, or 10 MHz	
Required duty cycle **Latency (typical):** **Ext. input** **Ext. clock**	50 ±10 % to trigger output 16ns ±1 clock 15 ns	to channel output 46ns ±1 clock 45 ns	50 ±10 % to trigger output 16 ns ±1 clock 15 ns	to channel output 46 ns ±1 clock(2) 45 ns
	Add 3 ns if an expander frame is used		Add 3 ns if an expander frame is used	

(1) Jitter performance may be degraded
(2) If frequency = 667 MHz

Trigger ouput

Can be used in:

- Clock mode
- Sequence mode

In sequence mode a pulse will be set to mark the start of any segment.

In clock mode, the trigger output can supply a clock output of up to 675 MHz. If a higher speed performance clock is needed:

- A 2.7 Gb/s generator can be can be used to supply a clock output up to 2.7 GHz
- A 10.8 Gb/s generator can be can be used to supply a clock output up to 10.8 GHz.

Technical specifications

All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10° to 40° ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ω to ground at ECL levels unless specified otherwise.

Table 79. Trigger output characteristics E4805B and E4808A

Trigger output signals	• Clock mode (up to 675 MHz). • Sequence mode
Output impedance	50 Ω typ.
Output level	TTL (frequency < 180 MHz), 50 Ω to GND ECL 50 Ω to GND/-2 V, PECL 50 Ω +3 V
Trigger advance	30 ns typ. between trigger output and data output /sampling point (delay set to zero in both cases)
Maximum ext voltage	-2 V to +3.3 V
Jitter (int. reference/int. clock)	< 10 ps rms (5 ps typ.)

General Characteristics

Mainframes: See table on page 52.

Save/recall: Pattern segments, settings and complete settings plus segments can be saved and recalled. The number of settings that can be stored is limited only by disk space.

Vector import/export: Pattern files can be imported/exported via a 3.5 inch floppy disk, LAN or GPIB (IEEE 488.2). File format is ASCII using a STIL subset.

Programming interface: GP-IB (IEEE 488.2) and LAN. The interface to applications such as C, Visual Basic, or VEE must be installed. Use the Agilent 81200 *Plug&Play* drivers for easy programming.

Programming language:
SCPI 1992.0

Programming times: Vector transfer from memory to hardware depends on the amount of data. See the table for examples.

On-line help: Context-sensitive.

Print-on-demand: Getting started and programming guides can be printed from .pdf files included in the ParBERT 81250 software.

Self-test: Module and system selftests can be initiated.

Modules

Module size:
VXI C-size, 1 slot.

Module type:
Register-based; requires ParBERT 81250 user software E4875A supplied with the mainframes.

Weight:
(including front-ends) Net: 2kg.

Shipping: 2.5 kg.

Warranty:
1 year return to Agilent

Re-calibration period: 1 year.

Agilent Technologies quality standards
The ParBERT 81250 is produced to the ISO 9001 international quality system standard as part of Agilent Technologies' commitment to continually increasing customer satisfaction through improved quality control.

Table 80. Programming times

	Programming time
Change of levels	6 ms typ.
Change of delay	16 ms typ. Not applicable in run mode
Change of period	60 ms typ. For one E4805 with one E4832A. Not applicable in run mode. Increases with the number of modules but
Stop & start	32 ms typ.
Synchronization	50 ms typ. (without phase alignment) 110 ms typ. with 20% phase accuracy @ 660 MHz 650 ms typ. with 1% phase accuracy @ 660 MHz
Download values	
System with 4 channels	< 1.5 s typ. 1000,000 bit each
System with 120 channels	< 20 s typ. 1 Mbit each
System with 40 channels	< 10 s typ. 1 Mbit each
+ Add numbers for each synchronzing analyzer within one module	

Table 81: Cooling requirements for modules with front-ends installed

Modules	ΔP mm H20	Air flow liter/s	Max Δtemp
E4805B	0.25	3.6	10 °C
E4808A	0.25	3.6	10 °C
E4809A	1.08	3.7	12 °C
E4832A	0.30	4.7	15 °C
E4861A	0.40	5.2	10 °C
E4861B	0.40	6.6	15 °C
E4866A	0.30	5.2	10 °C
E4867A	0.30	5.5	15 °C
N4872A/74A	1.20	7.5	13 °C
N4873A/75A	0.85	5.4	12 °C

Table 82. Power Requirements of Modules and Front-Ends

	DC Volts	+24V	+12V	+5V	-2V	-5.2V	-12V	-24V
Modules (These specifications are valid for the module with the front-ends installed)								
E4805B Central	DC Current	0.15A	0.2A	1.8A	1.4A	3.8A	0.2A	–
Clock module	Dynamic current	0.015A	0.02A	0.18A	0.14A	0.38A	0.02A	–
E4808A	DC Current	0.2A	0.3 A.	1.8A	1.9A	3.9A	0.2A	–
	Dynamic current	0.02A	0.03A	0.18A	0.19A	0.39A	0.02A	–
E4809A	DC Current	0.35A	1.25 A	2.0A	2.4A	6.8A	0.5A	0.55
	Dynamic current	0.05A	0.15A	0.2A	0.3A	0.7A	0.05A	0.06
N4872A/74A	DC Current	0.5A	0.75A	3.8A	0.6A	2.6A	1.2A	0.8
	Dynamic current	0.05A	0.08A	0.38A	0.06A	0.26A	0.12A	0.08
N4873A/75A	DC Current	0.2A	0.5A	4.6A	0.7A	2.3A	0.3A	0.7
	Dynamic current	0.02A	0.05A	0.46A	0.07A	0.23A	0.03A	0.07
E4866A	DC Current	0.2A	1.0A	5.0A	1.2A	2.6A	0.5A	0.9
	Dynamic Current	0.02A	0.1A	0.5A	0.12A	0.26A	0.05A	0.09
E4867A	DC Current	0.2A	1.0A	7.0A	1.5A	3.0A	0.8A	0.2
	Dynamic current	0.02A	0.1A	0.7A	0.15A	0.3A	0.08A	0.02
E4861B	DC Current	0.02A	0.03A	2.2A	0.4A	0.4A	–	–
	Dynamic current	0.01A	0.01A	0.2A	0.04A	0.04A	–	–
E4862B Generator	DC Current	0.2A	0.2A	1.0A	0.2A	0.5A	0.21A	0.48
	Dynamic Current	0.02A	0.02A	0.07A	0.02A	0.05A	0.02A	0.05
E4863B Analyzer	DC Current	0.2A	0.2A	2.0A	0.2A	0.45A	0.21A	0.48
	Dynamic Current	0.02A	0.02A	0.2A	0.02A	0.05A	0.02A	0.05
E4861A 2.7 Gb/s	DC Current	0.10	0.50A	5.20A	1.80A	4.00A	0.90A	0.01
Gen./An.Module	Dynamic current	0.01A	0.05A	0.52A	0.18A	0.40A	0.09A	–
Remark: The power requirements of E4861A include the power requirements of any two front ends								
E4832A 675 Mb/s	DC Current	0.10A	0.10A	2.60A	0.60A	3.60A	0.10A	0.1
Gen./An. Module	Dynamic Current	0.01A	0.01A	0.26A	0.06A	0.36A	0.01A	0.01
Remark: For the module E4832A, the power specifications of the chosen front-ends (E4835A, E4838A or E4843A) have to be added to the power specifications of the E4832A module to get the overall value of the power specifications								
E4838A	DC Current		0.45A	0.18A	0.07A	0.38A	0.41A	–
Differential	Dynamic Current		0.045A	0.018A	0.007A	0.038A	0.041A	–
Generator 675 Mb/s								
Front-ends								
E4835A two differential	DC Current		0.2A	1.2A	0.2A	0.3 A	0.3A	–
Analyzer 675 Mb/s	Dynamic Current		0.02A	0.12A	0.02A	0.03A	0.03A	–

Table 83. General mainframe characteristics

	81250A mainframe
Description	E8403A 13 slot VXI C-size frame
Order description	81250A-149 (entry frame) 81250A-152 (expander frame) E8404A-148
Number of slots for ParBERT 81250 data/clock modules	12
Operating temperature	10 °C to 40 °C
Storage temperature	-20 °C to +60 °C
Humidity	80% rel. humidity at 40 °C
Power requirements	90 - 264 Vac ± 10%, 47 - 66 Hz 90 - 264 Vac ± 10%, 300 - 440 Hz (not recommended: leakage current may exceed safety limits @ > 132 Vac)
Power available for modules	950 W for 90 - 110 Vac supplies 1000 W for 110 - 264 Vac supplies
Electromagnetic compatibility	EN 55011/CISPR 11 group 1, class A + 26 dB
Acoustic noise	48 (56) dBA sound pressure at low (high fan speed)
Safety	IEC 348, UL 1244, CSA 22.2 #231, CE-mark
Physical dimensions	W: 424.5 mm, 16.71 inches H: 352 mm, 13.85 inches D: 631 mm, 24.84 inches
Weight (net)	26.8 kg (25.3 kg)
Weight (shipping) (max.)	72 kg (67 kg)

Quick ordering guide - overview

The ParBERT 81250 is a modular instrument, which can be tailored to your specific needs. There are generator and analyzer channels at different speed classes. The ParBERT 81250 channels consist of data modules and front-ends. The 13.5 Gb/s, 10.8 Gb/s, 7 Gb/s and 3.35 Gb/s optical are dedicated data modules for generators and analyzers. At 3.35 Gb/s and 2.7 Gb/s the data module houses 2 front-ends, at 675 Mb/s the data module houses 4 front-ends. The data modules operate in conjunction with a clock module. The combination of data modules with a clock module is called 'clock group' and is represented in the ParBERT 81250 software within one user interface. The following table lists the combination of data modules and front-ends together with usable clock modules.

Table 84. Ordering guide

Data module/front-ends		Generator	Analyzer	Clock module
13.5 Gb/s data module		N4872B	N4873	E4809A
10 Gb/s data module		E4866A	E4867A	E4808A
7 Gb/s data module		N4874A	N4875A	E4809A
3.35 Gb/s data module	**(1)**	E4861B	E4861B	E4808A
3.35 Gb/s front-end		E4862B	E4863B	or E4809A
2.7 Gb/s/1.65 Gb/s data module	**(1)**	E4861A	E4861A	E4805B
2.7 Gb/s/1.65 Gb/s front-end		E4862A/E4864A	E4863A/E4865A	or E4808A
675 MHz data module	**(2)**	E4832A	E4832A	E4805B
675 MHz front-end	**(3)**	E4838A	E4835A	or E4808A
				or E4809A

(1) Houses 2 front-ends
(2) Houses 4 front-ends
(3) E4835A provides a pair of analyzers

Entry system

The VXI frame offers 13 slots. Besides data modules and clock modules, there is the need for a computer interface. The ParBERT 81250 works with an IEEE 1394 FireWire interface, which works with an external PC (81250 #013, #014) or a laptop (81250 #015). The IEEE 1394 FireWire card consumes one VXI slot. Assuming the use of the Firewire interface and one clock module in place, the entry system can hold up to:

10 channels at 13.5 Gb/s, 7 Gb/s
11 channels at 10.8 Gb/s and 3.35 Gb/s optical
22 channels at 3.35 Gb/s or 2.7 Gb/s
44 channels at 675 Mb/s.

In some circumstances these maximum numbers cannot be achieved due to power restrictions. Before finalizing a configuration, it is necessary to calculate the power budget. The 675 Mb/s Analyzer E4835A always comes as a pair and need to be configured side by side, providing two fully independent analyzer channels.

Table 85. Entry system

Max # of channels	3.35 Gb/s or 675 Mbits	13.5 Gb/s 2.7 Gb/s or 1.65 Gb/s	10.8 Gb/s	7 Gb/s
FireWire				
1 frame	44	22	11	10
2 frames	88	44	22	20
3 frames	132	66	33	30
4 frames	176	88	44	40

More than 3 frames require more than one clock group.

Multi-mainframe/master-slave

If the number of channels exceeds the number of available slots in the “entry” frame, it is possible to add expander frames. To add channels within one clock group, there is the limit of a maximum of two expander frames. If data modules are housed in an expander frame they need an additional clock module. This clock module must be connected to the clock module in the entry frame (master frame) with the help of the master-slave connection. This connection carries the clock and data flow synchronization between the frames. The master-slave connection hardware is delivered with the expander frames. The master-slave connection is only possible between clock modules of the same type.

Aside from the master-slave connection between the clock modules, the controller interface also needs an extension into the expander frames:
• The FireWire interface, consuming one slot, can be “daisy-chained” from frame to frame. This would allow the configuration of a ParBERT 81250 system with virtually an unlimited number of channels (within different clock groups, see above limitation of max. channels per clock group).

Different clock groups

A clock group consists of a clock module, one or more data modules and the graphical user interface to set the parameters. Within one clock group there can be data modules with generators and analyzer front-ends from different speed classes combined using the binary frequency multipliers (..., 1/16, 1/8, 1/4, 1/2, 1 , 2 ,4 ,8 , 16, ...) the data rate range possible for each data module can be achieved. The configuration of more than one clock group is possible. This will combine a clock module with one or more data modules. Several clock groups may be housed in one frame or using expander frames. Each clock group will be operated from its own graphical user interface. The user interface will actually be assigned to a certain hardware set. If there is more than one clock group, the user interfaces may run from separate PCs, connected via LAN. A configuration of more than one clock group is recommended:
• To run different speeds (non binary ratio) between generators and/or analyzers
• To run independent phase ratio between generators and/or analyzers
• To make flexible use of data rate range when combining different speed classes
• To use custom (memory) based data and use of bit synchronization for the analyzer(s).

Using different clock groups reduces the maximum number of channels given in the table on the previous page. Within one system using different clock groups, all clock modules must be of the same type. A master-slave connection must not be installed between the clock modules if different clock groups are desired.

Order information entry system

1 x 81250A	System reference
1 x 81250-149	Mainframe
1 x E4805B/E4808A/ E4809A	1st clock module

Add data modules/front-ends

Decide on controller:

1 x 81250A-013	FireWire (IEEE 1394) PC Link to VXI
1 x 81250A-014	Ext. PC
or	
1 x 81250A-015	Laptop including PCMCIA IEEE 1394 card

Decide on controller accessories:

1 x 15444A	Monitor
1 x 15445A	Ext. CD-ROM

Order information multi mainframe:

1 x 81250-152	FireWire (IEEE 1394) expander frame
1 x E4805B/E4808A/	Clock module

E4809A
Add data modules/front-ends

Order information master-slave/different clock groups

E4805B:	Clock module (usable with 675Mb/s and 2.7 Gb/s module)
E4808A:	Clock module (usable with 675 Mb/s, 1.65 Gb/s, 2.7 Gb/s, 3.35 Gb/s, 10.8 Gb/s and 45 Gb/s modules)
E4809A:	Clock module (usable with 675 Mb/s, 3.35 Gb/s, 7 Gb/s and 13.5 Gb/s modules)
Specific rules:	Do not mix E4809A, E4808A and E4805B: • Slave connection is possible only between clock modules of the same type • One system must be configured with one type of clock module

Table 86. Cable kit accessories

P/N description	Cable kit	No. of cables	Connectors	To be used with	Bandwidth	Matching	Length included	Addl. parts
15441A	SMA to SCI	10	SMA (m) - SCI (f)	675 Mb/s	tt ≥ 500 ps	No	1.5 m	4 SCI adapters
15442A	SMA	4	SMA (m) - SMA (m)	675 Mb/s/ 2.7/(3.35) Gb/s	tt ≥ 100 ps	No	1 m	-
15443	SMA matched pair	2	SMA (m) - SMA (m)	675 Mb/s/ 2.7/(3.35) Gb/s	tt ≥ 100 ps	Yes	1 m	-
N4869A	SMA & phase shifter	3	SMA (m) - SMA (m)	E4866A out to N4868A in	tt ≥ 50 ps	Adjustable	0.4 m	Mech. phase Shifter + -50 ps
N4870A	1.85 mm matched	2	1.85/2.4 mm 1.85/2.4 mm	N4868A out E4868A/B out E4869A/B in	tt ≥ 15 ps	± 1.5 ps	0.63 m	-
N4871A	SMA matched	2	SMA (m) - SMA (m)	3.35/10.8 Gb/s front-ends	tt ≥ 50 ps	± 1.5 ps	1 m	-
N4910A	2.4 mm matched pair shifter	2	2.4 mm - 2.4 mm	7 Gb/s, 13.5 Gb/s		0.60 m		-

Product structure - ParBERT 81250

Part #/Option	Description
81250A	ParBERT 81250
81250A-013	IEEE 1394 PC link to VXI
81250A-014	External PC
81250A-015	Laptop including PCMCIA IEEE 1394 card
81250A-149	Mainframe
81250A-152	IEEE 1394 'FireWire' expander frame
81250A-0B0	Do not include tutorial CD ROM
81250A-AX4	Rack flange kit

Software

E4875A	One licence and software CD ROM for ParBERT 81250

Clock modules

E4805B	675 MHz central clock module
E4805B-UK6	Commercial cal. certificate w/test data
E4808A	High performance central clock module
E4808A-UK6	Commercial cal. certificate w/test data
E4809A	13.5 GHz central clock module
E4809A-UK6	Commercial cal. certificate w/test data

Data modules & front ends

E4832A	675 Mb/s generator/analyzer module
E4832A-UK6	Commercial cal. certificate w/ test data
E4835A	Two differential analyzer front-ends, 675 Mb/s
E4838A	Differential generator front-end, 675 Mb/s
E4861A	2.7 Gb/s generator/analyzer module
E4861A-UK6	Commercial cal. certificate w/test data
E4864A	Generator front-end 1.65 Gb/s
E4864A-UK6	Commercial cal. certificate w/test data
E4865A	Analyzer front-end 1.65 Gb/s
E4865A-UK6	Commercial cal. certificate w/test data
E4862A	Generator front-end 2.7 Gb/s
E4862A-UK6	Commercial cal. certificate w/test data
E4863A	Analyzer front-end 2.7 Gb/s
E4863A-UK6	Commercial cal. certificate w/test data
E4861B	3.35 Gb/s generator/analyzer module
E4861B-UK6	Commercial cal. certificate w/test data
E4862B	Generator front-end 3.35 Gb/s
E4862B-UK6	Commercial cal. certificate w/test data
E4863B	Analyzer front-end 3.35 Gb/s
E4863B-UK6	Commercial cal. certificate w/test data
E4810A-001	3.35 Gb/s 850 nm electrical/optical generator module
E4810A-UK6	Commercial cal. certificate w/test data
E4811A-001	3.35 Gb/s 750 - 1610 nm Optical/electrical analyzer module (calibrated @ 850 nm)
E4811A-UK6	Commercial cal. certificate w/test data
N4874A	Generator module 7 Gb/s
N4875A	Analyzer module 7 Gb/s
E4866A	Generator module 10.8 Gb/s
E4866A-UK6	Commercial cal. certificate w/test data
N4868A	10 Gbit/s booster module (1 diff. or 2 single ended ch.)
N4868A-UK6	Commercial cal. certificate w/test data
N4868A-001	10 Gbit/s booster module (2 diff. or 4 single ended ch.)
N4868A-U01	Commercial cal. certificate w/test data for N4868A-001
E4867A	Analyzer module 10.8 Gb/s
E4867A-UK6	Commercial cal. certificate w/test data
N4872A	Generator module 13.5 Gb/s
N4872A-UK6	Commercial cal. certificate w/test data
N4873A	Analyzer module 13.5 Gb/s
N4873A-UK6	Commercial cal. certificate w/test data
E4868B	45/43.2 Gbit/s multiplexer module
E4868B-UK6	Commercial cal. certificate w/test data
E4869B 4	5/43.2Gbit/s demultiplexer module
E4869B-UK6	Commercial cal. certificate w/test data

Warranty & services

All components automatically have 1 year return to Agilent warranty, if bought as separate pieces.

All systems have 1 year on-site warranty.

Start up assistance for first time users is included.

40G bundles

E4894B	43.2 Gb/s pattern generator bundle
E4894B-UK6	Commercial cal. certificate w/test data
E4895B	43.2 Gb/s error detector bundle
E4895B-UK6	Commercial cal. certificate w/test data
E4896A	45 Gbit/s & 3.35 Gbit/s pattern generator bundle
E4896A-UK6	Commercial cal. certificate w/test data
E4897A	45 Gbit/s & 3.35 Gbit/s error detector bundle
E4897A-UK6	Commercial cal. certificate w/test data

Accessories

15440A	Adapter kit: 4* SMA (M) I/O adapters
15441A	Cable kit: 10*SMA (m) to SCI connector
15442A	Cable kit: 4*SMA (m) to SMA (m)
15443A	Matched cable pair
15444A	Monitor
15445A	External CD-ROM
15446A	8-line trigger input pod
15447A	Deskew probe
E4839A	Test fixture
15448A	Pogo cable kit: 4*SMA(m) & 2 pogo adapter
15449A	DUT board 50 Ω impedance
N4869A	Cable Kit: 3 cables with phase adjuster for connecting E4866A with N4868A
N4870A	Cable kit: 2.4 mm for N4868A output
N4871A	Cable kit: SMA matched pair, 50 ps
N4910A	Cable kit: matched cable pair for 13.5 G
N4911A-002	Adapter 3.5 mm female to 2.4 mm male
N4912A	2.4 mm 50 Ω termination, male connector
N4913A	4 GHz deskew probe

Storage of Customer Specific Data in Agilent ParBERT 81250 Parallel Bit Error Ratio Tester Data Generator/Analyzer Modules and Front Ends

This statement is to certify that none of Agilent Technologies' ParBERT 81250 clock modules, data generator / analyzer modules or front ends store customer specific data in any non-volatile memory. As a general rule it can be said that after electrical power has been turned off, the modules will not store any data or settings.

Data storage across power down / power up cycles will only appear in the ParBERT's PC Controller where access to the data can be controlled via generic Microsoft ® Windows ® security mechanisms.

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Related literature	Publication number
• Need to Test BER? Brochure	5968-9250E
• Agilent ParBERT 81250, Mux/Demux Application, Application Note	5968-9695E
• Agilent ParBERT 81250 13.5 Gb/s Parallel Bit Error Ratio Test Platform, Photocard	5988-9201EN
• Agilent Productivity Assistance	5980-2160E
• Agilent ParBERT 81250 43.2/45 G, Product Overview	5988-3020EN
• Agilent ParBERT 81250 Parallel Bit Error Ratio Test Platform, Data Sheet	5988-5901EN
• Agilent 81250 ParBERT Product Note (The influence of Generator Transition times on Characterization Measurements)	5988-5948EN

For more information, please visit us at **www.agilent.com/find/parbert**

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