Micro Memory MM-6390/512

# High Performance VME / VSB Expansion Memory Module

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# MM-6390D

## 512 MBYTE, 80 MBYTE/SEC TRANSFER RATE, DUAL-PORT VME/VME64/VSB DRAM MEMORY MODULE

A high-speed, dual-port, single card slot, high-density memory module, the MM-6390D provides up to 512 Mbytes for VME/VME64/VSB systems. It is intended for high performance applications employing Block Transfer at data rates greater than 80 Mbytes/sec. It also supports sequential access (BLT/MBLT) of 256/2K bytes on the VME/VME64 and 1 Kbytes on the VSB bus.

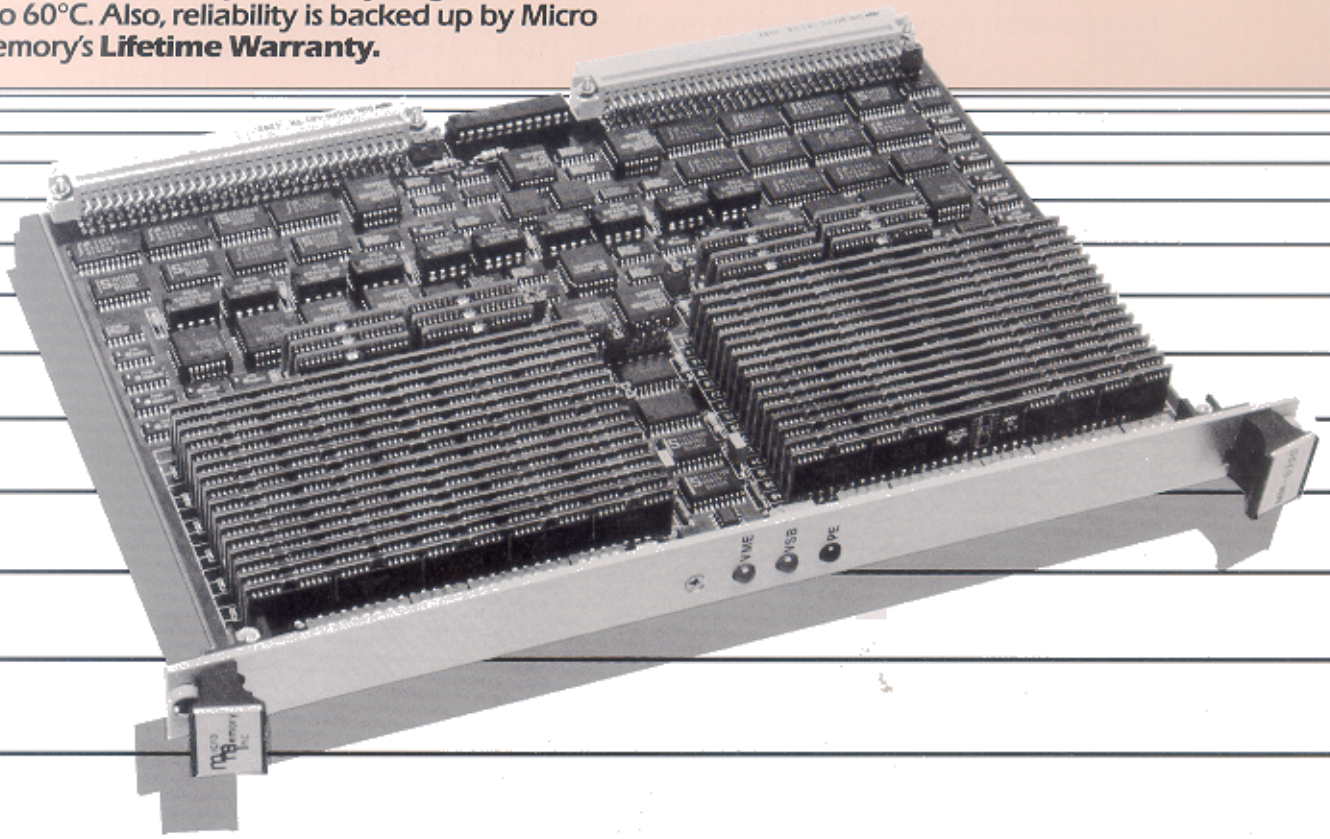
The Control Status Register (CSR), located in the short I/O address space, stores and reads byte-wide parity errors detected on the VME/VSB buses. The other bits enable Write-Wrong parity for diagnostics, disable the VME-port and determine whether the memory is CACHEable on the VSB bus.

Parity generation and checking are provided for each byte; parity status is stored and transmitted via BERR*.

Reliability is ensured by burn-in and running memory diagnostics that check operation for 48 hours while temperature-cycling boards from 0 to 60°C. Also, reliability is backed up by Micro Memory's **Lifetime Warranty.**

### FEATURES:

- Capacity: 32M, 64M, 128M, 256M, 512M bytes
- Cycle/Access Time (nsec):
  Block Transfer (BLT/MBLT)
  Write: 100/30, Read: 100/30
- Data Transfer Rate:
  VME64: 80 Mbytes/sec
  VME/VSB: 40 Mbytes/sec
- Compatible with VMEbus Rev D and VSBbus Rev C with A32/A24/D64/D32/D16/D8 (UAT) for VME/VME64 and A32/D32 for VSB
- Block transfer (BLT) 256 bytes for VME, MBLT of 2 Kbytes for VME64, and 1 Kbytes for VSB
- Parity generation and checking for error detection on each byte
- Write-Wrong parity for diagnostics under software control
- Module selection on 1 Mbyte boundaries, switch-selectable for lower and upper limits on each bus
- VMEbus Control Status Register (CSR) for parity reporting and control
- **Lifetime Warranty**

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# MM-6390D SPECIFICATIONS

| Parameter | Specification |
|---|---|
| Capacity | 32M, 64M, 128M, 256M, 512M bytes |
| Cycle/Access Time (nsec) | Block Transfer (BLT/MBLT) - Write: 100/30, Read: 100/30 |
| Data Transfer Rate | VME64: 80 Mbytes/sec, VME/VSB: 40 Mbytes/sec |
| Address | 32 bits for VMEbus, 32 bits multiplexed with 32 data bits for the VSBbus |
| Data In/Data Out | 8, 16, 32, 64 bits (UAT) for VMEbus, 32-bit slave for VSBbus |
| Sequential Access | Block transfer (BLT/MBLT) of 256/2K bytes, 8 Kbytes on the VME/VME64bus, 1K bytes on the VSBbus |
| Address Modifiers | AM0-AM5 decoded by socketed PLD with the following codes:<br>A24: 39, 3A, 3D and 3E<br>A32: 09, 0A, 0D and 0E<br>A24 with MBLT: 3B, 3C<br>A24 with BLT: 3B, 3F<br>A32 with BLT: 0B, 0F<br>with MBLT: 08, 0C |
| Parity Checking | Byte-wide parity generation and checking; parity output stored and transmitted via CSR, Write-Wrong parity for diagnostics |
| Control Status Register (CSR) | Read/Write, 8 bits wide, jumper-selectable in VME short I/O space (A16) with VMEbus low limit address tracking |
| CSR Format | D0 Enable Parity Out<br>D1 Write-Wrong Parity<br>D2 Memory CACHEable for VSB<br>D6 VMEbus Disable<br>D7 Parity Error<br>Others: Don't Care |
| Interface | VME Rev D and VSB Rev C |
| Modes of Operation | Read, write, read-modify-write, and refresh |
| Memory Selection | Two independent memory ports, switch-selectable on 1 Mbyte ($100000_H$) boundaries for each port by setting the upper and lower limits |
| Operating Temperature | 0 to +60°C |
| Storage Temperature | −40 to +85°C |
| Relative Humidity | Up to 95% without condensation |
| Power Requirements | 5V @ 5.5A |

# ORDERING INFORMATION

| Part Number | Memory Capacity |
|---|---|
| MM-6390D/XXX | XXX = 32M, 64M, 128M, 256M, 512M bytes |

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