

Matrix MD-CPU860

## Multiprotocol Processor CPU Board



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# MD-CPU860

# MX-CPU860

# MR-CPU860

# MM-CPU860

## Multiprotocol Processor Engine

### MPC860 PowerQUICC

#### Two PMC Locations

- ▼ PowerQUICC I/O Fully Supported via [I/O Configuration Modules \(IOCMs\)](#)
- ▼ Two PMC Sites for Flexibility and Expansion
- ▼ 0, 16, 32 or 64 MB DRAM
- ▼ 0, 512, or 1 MB SRAM
- ▼ 1 MB Boot Flash EPROM
- ▼ Flashfile EPROM Array uses 28F016 Devices for 0, 4, or 8 MB
- ▼ Real-Time Clock (RTC) and Watchdog Timer - Part of PowerQUICC
- ▼ RTC and SRAM Power Backup Provided by Onboard Battery, External Power Connector, or +5VSTBY
- ▼ Ethernet Capable
- ▼ Background Debug Port
- ▼ 33-MHz PCI Interface
- ▼ VMEbus Master and Slave Interface
- ▼ Front Panel Switches and Status LEDs
- ▼ Industrial, Extended Temperature, Rugged, and Militarized (Conduction-Cooled) Versions Available
- ▼ Convection-Cooled Versions Use 3-Row DIN Connectors; Conduction-Cooled Version Uses 5-Row DIN Connectors
- ▼ Non-VMEbus Version Also Available

The CPU860 is a 6U MPC860-based (PowerQUICC) CPU board. The board takes advantage of the I/O capabilities of the PowerQUICC by routing the I/O lines directly to the P2 connector and to a serial mezzanine card connector. The direct routing of I/O lines to P2 eliminates any pre-assignment of functionality, so the customer is free to add his own specific I/O interface or use the variety of interfaces available from MATRIX. The P2 I/O signal routing uses the MATRIX standard pinout for the MC68360-based MD-CPU360 board. Any single-function I/O Configuration Module (IOCM), including Ethernet, designed for the MC68360 will work without modification with these signal assignments.

Two PCI mezzanine card (PMC) locations and the serial mezzanine card interface provide for function expansion and flexibility. A VMEbus interface provides both master and slave capabilities to the PCI and to the VMEbus.

mezzanine card in lieu of a PMC card.

### **MPC860 PowerQUICC**

The MPC860 PowerQUICC connects to the local resources via its 32-bit address and 32-bit data local buses. Resources are organized into eight groups selected by means of the QUICC's eight chip select outputs.

When used in a non-VMEbus environment, the host processor has the ability to turn the external power on and off. This capability can be extremely useful in remote locations.

The board supports software development using the BDM Port. This 10-pin header accepts a ribbon cable from a BDM controller attached to a personal computer.

### **Memory**

The board provides an 8-bit data path to 1 MB of boot Flash EPROM. This EPROM is sector-erasable and sector-reprogrammable.

The CPU860 supports up to 64 MB of EDO DRAM, and all DRAM configurations use a 32-bit data path.

The board provides support for 512 KB or 1 MB of SRAM. Both use a 32-bit data path.

Support for 4 or 8 MB of 100 ns Flashfile EPROMs with a 32-bit data path is provided. The Flashfile EPROMs may be programmed in circuit.

### **PCI and VMEbus**

The Tundra Semiconductor QSpan chip provides the interface between the PowerQUICC Host and the PCI.

The PCI operates at 33 MHz and provides a 32-bit address and 32-bit data path. The data organization is little endian, and all signaling is 5V.

The Tundra Semiconductor Universe chip provides communications between the PCI masters and VMEbus slaves and between VMEbus masters and this board's PCI targets. It also provides the VMEbus System Controller functions if the board is located in the backplane's first occupied slot.

All versions of the board support VME64 Auto-slot ID. Additionally, the onboard hardware on the militarized version of the CPU860 supports geographical addressing provided by the 5-row VMEbus P1 connector. Geographical addressing is available on the convection-cooled versions as a custom option.

The PCI option allows each resource connected to the PCI to be a PCI master, target, or both. This includes the host MPC860, each of the PMC sites, and the VMEbus. Each PMC site and the host MPC860 may map some of their local resources so that they may become PCI target resources. These PCI target resources are then available to other PCI masters. If these targets are also mapped into VMEbus space, then they also become VMEbus slave resources.

The VMEbus resource map may also be mapped into the onboard PCI map. When this happens, any PCI master may become a VMEbus master.

### **PMC I/O**

The board supports two PMCs that use either front-panel I/O for convection-cooled versions or rear-panel I/O for the militarized version. The militarized version routes the PMC #1 I/O lines to P2 rows D and Z and to P0. All of PMC #2's I/O lines are routed to P0. PMC site #1 can support an I/O

mezzanine card in lieu of a PMC card.

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