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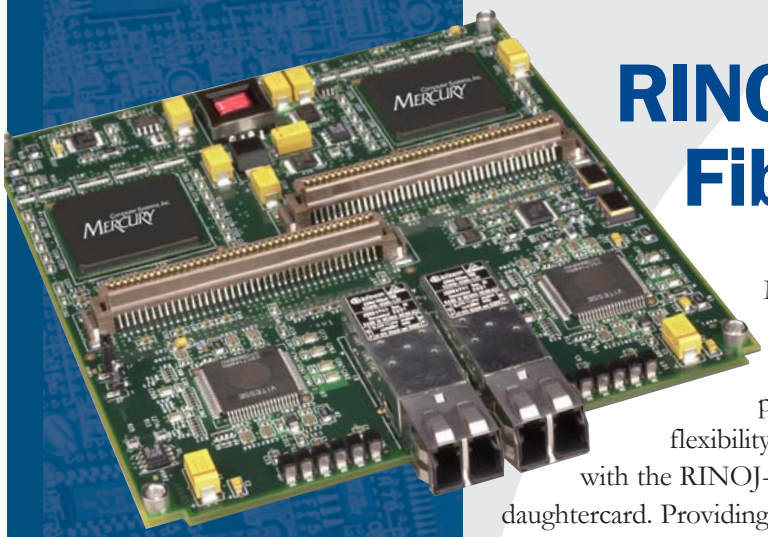
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Computer Systems, Inc.
MERCURY

RINOJ-F-2.5 Dual Channel Fiber I/O Daughtercard



Dual Channel Fiber-Optic FPDP

247 MB/s Peak Input or Output per Channel

Connections Up to 150m Distance

Real-Time Latency as Low as 4 µs

Supports All Four FPDP Data Modes

Ideal For Streaming Data Input

DMA Engine with Chaining and Branching

Mercury Computer Systems brings enhanced performance and flexibility to external I/O with the RINOJ-F-2.5 I/O daughtercard. Providing 2.5 Gbaud of input or output bandwidth per channel and two channels per card, the RINOJ-F-2.5 offers new levels of speed and connection density. Connected by fiber up to 150 meters with a latency as low as 4 µs, it is ideally suited as the real-time digital interface for sensor input or data output in a RACE++® system.

Full Compatibility

The RINOJ-F-2.5 implements the Serial Front Panel Data Port (FPDP) protocol (VITA 17.1-2003) and supports all four FPDP framing modes. This broad implementation of the standard makes the RINOJ-F-2.5 compatible with all products supporting any subset of the VITA 17.1-2003 protocol.

The RINOJ-F-2.5 is fully compatible with previous RINOJ-F RACE++ products, easing migration from the legacy I/O daughtercards while offering significant improvements in speed as well as configuration flexibility.

Products from Mercury's partners are available for VITA 17.1-2003 interfaces to sensors, or to PCs to support development and testing.

I/O Intelligence

The RINOJ-F-2.5 is more than an ordinary digital interface – each channel can be programmed for data distribution without processor intervention. The interface can sense signals in the input data stream that indicate sensor mode changes, and route data appropriately for each different mode. Each mode can be made to correspond with an application-defined DMA command packet (CP) chain. These command packets cause the channel's DMA controller to route the data to a predefined destination anywhere within the RACE++ switch fabric. This data-driven distribution takes advantage of information available at the source.

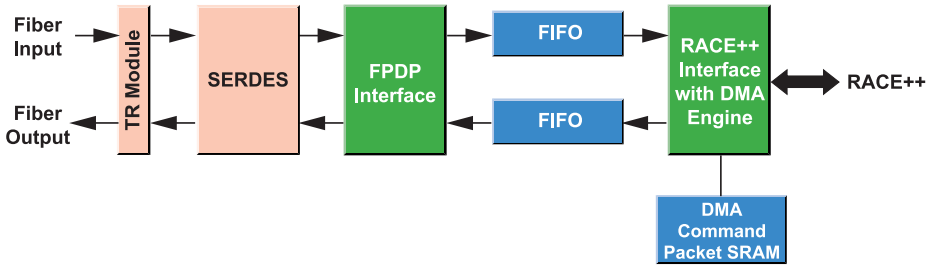
DMA command packets can be chained together to automatically distribute sequential data packets to different processors or endpoints on the RACE++ fabric. This feature can be combined with RACE++ broadcast and multicast features that can send the same data packet to multiple processors, providing complete flexibility in intelligent data distribution.

Advantages of Fiber

Optical cables and their connectors take up less space than their copper-based counterparts, making it easier to package a large number of them in a single chassis. Optical fiber is immune to electromagnetic interference (EMI) and is not susceptible to ground loops. Fiber allows connections that can span hundreds of meters, making it the preferred solution for sensors separated by long distances from processing chassis, or for environments in which EMI is an issue.

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Figure 1 Channel Block Diagram



Serial FPDP Interface

Serial FPDP supports a mapping of the FPDP protocol onto the Fibre Channel physical layers (FC-0 and FC-1). Serial data is transmitted at 2.500 Gbaud over the fiber. The RINOJ-F-2.5 achieves a sustained data rate of 247 MB/s when the data packets are kept large on both the fiber side and the RACE++ side of the interface.

The serial protocol provides error checking and optional flow control. Error checking is accomplished with a CRC (cyclic redundancy check) included in each packet sent over the serial line. The optional flow control feature enables the receiving end of the fiber interface to send flow control command through its output port back to the data transmitter. If flow control is not used, only a single fiber per data channel is required.

The RINOJ-F-2.5 brings two FPDP data streams into a RACE++ system. Each channel provides separate connections to the RACE++ switch fabric and can operate in either direction (see Figure 1).

Linked-List DMA Controller

The RINOJ-F-2.5 daughtercard includes a linked-list DMA controller for intelligent control of data distribution. Lists of DMA command packets control the linked-list DMA controller. Since they are constructed once at setup time and can be initiated multiple times within the time-critical portion of the application, such chains of transfer requests are very valuable for repetitive, high-speed transfers. In many applications, once the DMA controller is set up it can run autonomously, scattering or gathering data among a large number of processing nodes with no processor intervention.

The DMA command packets are stored in local SRAM to reduce latency. This local SRAM is 64K x 32 bits, allowing 8,000 command packets to be stored.

I/O Management Software

Mercury provides a data transfer facility layered on top of the standard Mercury MC/OS™ multicomputer operating environment. This facility consists of a set of user-callable I/O control functions. These functions are used to define I/O transfer requests (DMA command packets) and to link such requests into a chain that is then automatically executed by the designated I/O device.

Each CP specifies the RACE++ route, address, and maximum word count for the transfer as well as some control information. The route in each CP can specify either a single RACE++ endpoint or, in the case of an input stream, a multicast to multiple RACE++ endpoints. By chaining command packets together into a linked list, an incoming stream can be parceled out among a large number of endpoints. Transfers of up to 15 MB in length may be implemented.

The requests can be chained, with the option of synchronization at the end of each chain. Synchronization between the RINOJ-F-2.5 and the application program can be accomplished by queuing a transfer request that transfers status information at the desired synchronization point in the DMA chain. This block of status information is written to the local memory of the processor with which it is being synchronized. The processor can then poll on a location in the block of status information. The RINOJ-F-2.5 also can be synchronized with a processor when set up to send a mailbox interrupt to the desired processor.

Data Frame Management

The RINOJ-F-2.5 allows the sensor to frame the data into "epochs." Any sensor can define its own epoch boundary based on what makes sense for that type of sensor and on how the data will be used by the processing system. In the case of radar data, these epochs are likely to be coherent processing intervals. In the case of images, an epoch is likely to be a line or a frame of an image.

Many framing options are available for video and other sensor data.

The RINOJ-F-2.5 supports FPDP framing options as follows:

- **Unframed** - The application uses predetermined data transfer sizes and coordination at the start of the data stream.
- **Single-Frame Data** - Data is framed through the use of the FPDP signal SYNC* before the start of each transmission. The frame is closed when the expected number of words are received.
- **Dynamic-Size Repeating Frame Data** - Data is framed through the assertion of SYNC* and DVALID* together at the end of an FPDP frame of data. Mercury calls this the “end-of-epoch.” The FPDP frame size can vary from one

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frame to the next. The RINOJ-F-2.5 can be configured to end the DMA transfer with the current command packet upon receipt of these end-of-frame signals and be notified of the amount of data actually received. The RINOJ-F-2.5 can also branch to another command packet upon the end of an FPDP packet.

- **Fixed-Size Repeating Frame Data** - Data is framed through either receipt of the programmed number of words or the assertion of SYNC* and DVALID* together at the end of an FPDP frame of data.

Data-Driven Frame Processing

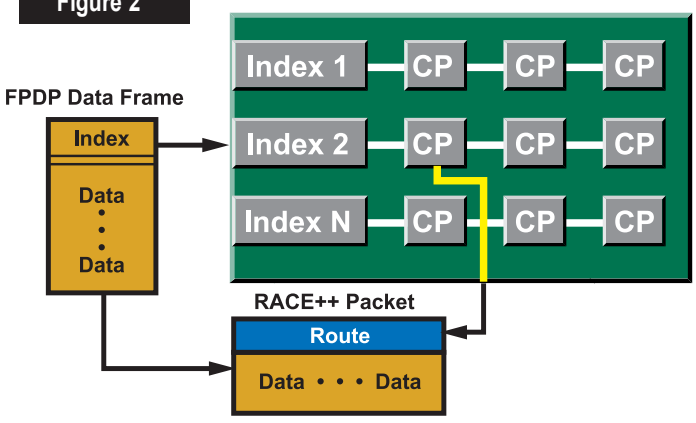
Many modern sensors change modes during operation. When a sensor changes modes, the processing system must make the corresponding mode change at the correct time. The sensor can also use the first word of each epoch to indicate its current mode. The RINOJ-F-2.5 hardware "cable header" may use this word to index to a particular DMA Command packet chain, then initiate the chain without processor intervention (see Figure 2). This allows each mode of the sensor to have a dedicated DMA chain and a completely different data distribution from other modes.

When the sensor mode changes are known in advance, the RINOJ-F-2.5 can be programmed to switch DMA chains for the next mode through the use of branching at the end of an FPDP frame or "epoch." This branching capability can also be used for error handling when the end of the FPDP frame occurs before it is expected.

DMA Command Packet Looping

A chain of command packets can be created that loops on itself. To prevent command packets from overwriting data at the addresses used on the first loop, the RINOJ-F-2.5 DMA controller contains offset registers that can be used for incrementing through a set of buffers on the destination or source nodes. The last CP in the loop can be set up to add a delta to the offset register each time through the loop. This offset register can be added to the address specified by the command packets. In many cases this allows the required number of command packets to be reduced significantly.

Figure 2



Recovering from Input Stream Faults

With some input interfaces, missing or extra data can cause the interface to lose sync with an input data stream until a processor intervenes. The RINOJ-F-2.5 minimizes the system upset by localizing the effects of anomalies in the input stream. To do this, the RINOJ-F-2.5 re-synchronizes its DMA controller to the incoming data at each data frame (epoch boundary). This re-synchronization is done by the hardware, with no processor intervention.

In the event that an end-of-epoch marker is lost due to a media error, the maximum word count in the DMA CP will prevent data from being written past the end of the buffer.

Conquering Latency

The RINOJ-F-2.5 can be configured to give a latency of less than 4 µs from when data arrives at the interface to when it is on a processing node ready to be processed. The main feature that enables this low latency is the linked-list DMA CP processing of the RINOJ-F-2.5's DMA controller. By cycling through lists of DMA commands set up during initialization, the RINOJ-F-2.5 can autonomously distribute the data without any processor intervention.

Two additional features ensure that low-latency operation is maintained. First, a programmable threshold is used to tell the DMA controller when it should start emptying its input FIFO. If the FIFO has more than the specified amount of data, the DMA controller will start emptying the FIFO. Second, the RINOJ-F-2.5 includes a programmable timer that will cause any remaining data to be emptied from the input FIFO if no input data arrives for the specified length of time.

RINOJ-F-2.5 Bi-directional Operation

Although each link is generally operated as either an input or an output device, each link is capable of bi-directional data transfers. On the fiber side of the FIFOs, the RINOJ-F-2.5 is full duplex. The FIFOs are capable of simultaneous input and output (see Figure 1). On the RACEway side of the FIFOs, each link has a single DMA controller that is shared for both input and output.

DMA chains that move data in both directions across a single link can be created with some command packets

moving data in and some moving data out. The direction of data movement is controlled by a bit in the DMA CP. Contact Mercury for more information on the transfer control for bi-directional operation.

RINOJ-F-2.5 Copy Mode

The RINOJ-F-2.5 can also loop any data arriving through its receive fibers directly onto its corresponding transmit fiber. Copy mode is useful for systems in which it is desirable to record the incoming data. When copy mode is enabled, the data can be both distributed to nodes by the RINOJ-F-2.5 as well as passed on to another chassis for recording. Copy mode on the RINOJ-F-2.5 is link-specific. It is possible to put the device into copy/loop mode which supports flow control. Output is disabled in both copy and copy/loop modes. Copy mode is enabled via a bit in a control register that is accessed by the I/O management software.

Connecting Loosely Coupled Systems

In some cases, applications can benefit from having the system split into multiple, loosely coupled chassis to provide isolation among subsystems. RINOJ-F-2.5 interfaces can be used to facilitate the point-to-point connections for such a system.

Generally it is desirable to have a DMA controller at both ends of the connection. One chassis cannot communicate with a remote chassis unless the DMA controller of the remote chassis is set up to take in the data, thereby achieving the desired isolation.

Configuration Options

Media	**62.5/125 or 50/125 Multimode (Wavelength is 850 nm)**
Connector type	**LC**
Distance	**150 meters**
Front Panel	**Each RINOJ-F-2.5 comes with a front panel to adapt to the motherboard: please specify board model (e.g., MCJ6)**
Cables	**Each I/O board includes a "test" cable**

Configuration Requirements

RACE++ Series Motherboards
- **MCJ6, MCJ9, MC8P9**
- **RINOJ-F-2.5 is not compatible with MCH6™**

MC/OS™ Multicomputer Operating Environment
- **MC/OS 5.6 or later**
- **RINOJ-F-2.5 daughtercards include a driver software package for MC/OS**

Electrical

Input and Output FIFO/channel	**16K x 36 bits (input), 2K x 36 bits (output)**
DMA command packets SRAM	**64K x 32 bits**
Data rate	**2.500 Gbaud or 1.0625 Gbaud**
Power Dissipation	**Approximately 16 watts**

Mechanical Specifications

J-Style Daughtercard	**5.000" x 4.435"**
Weight	**0.42 pounds**

Commercial Environmental Specifications

Operating temperature	**0°C to 40°C**
Storage temperature	**-40°C to 85°C**
Humidity	**10-90% non-condensing**
Maximum operating altitude	**10,000 ft**
Airflow requirement	**10 ft^3 /min**
Shock	**Z-axis; 20g, 11ms half sine** **X, Y-axes; 32g, 11ms half sine** **Z-axis; 20g 1ms half sine**

Rugged versions also available.

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