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industry's first computer system based on an open-standard switched-fabric "bus-less" interconnect was introduced today by Mercury Computer Systems, Inc.

The RACEAE-MCH platform capitalizes on an open, heterogeneous hardware and software environment to rapidly integrate off-the-shelf function blocks with the RACEway Interlink switched-fabric interconnect. RACE-MCH's ANSI-standard switched-fabric expedites highly-configurable realtime computing systems development. It provides deterministic, concurrent-transaction network connections among a heterogeneous set of application-preferred processing and I/O elements.

"The RACE-MCH platform represents no less than the beginning of the end of bus-based computers," said Jay Bertelli, CEO and president of Mercury Computer Systems. "We see expanding market opportunity since bus topologies are physically incapable of satisfying realtime interconnect performance needs, and industry-standard switching fabrics easily outperform the highest performance buses at a fraction of the cost."

Easy integration plus high bandwidth

Because it is based on an open standard interconnect, the RACE-MCH platform is expected to advance an industry-wide adoption of switched-fabric networks in lieu of bus-based system architectures.

"Switched-fabric interconnects have been widely acknowledged as the most obvious long-term solution to bus-bandwidth limitations," said Barry Isenstein, Mercury's director of strategic marketing. "Combining the well-established benefits of open standard computing with the performance gains of a switched-fabric interconnect has already compelled numerous third-parties to develop products for RACEway Interlink. With RACEway Interlink, you get both high-bandwidth heterogeneous processing and rapid, off-the-shelf integration."

RACE-MCH motherboards

The new RACE-MCH motherboards use the ANSI-standard RACEway Interlink to implement heterogeneous, switched-fabric computer systems in off-the-shelf VMEbus chassis. Available in both 6U and 9U versions, the motherboards provide two and nine locations respectively, for RACE daughtercards.

Each RACE-MCH daughtercard site is interconnected with other sites, a VME64 bus interface, and the RACEway Interlink interface via six-way, 480 Mbytes-per-second-per-switch crossbar ASICs. The crossbars and the RACEway Interlink form the basis for the switched-fabric interconnect that allows the construction of computers that scale to tens of GFLOPS and hundreds of Gbytes/second of data throughput.

Because RACE-MCH provides a heterogeneous computing environment, off-the-shelf daughtercard nodes, and customer-specific nodes can easily be integrated to optimally match different processor types to particular computation stages of an application.

RACE-MCH daughtercards

RACE-MCH motherboards support the RACE concept of "compute nodes." Each compute node consists of one or more processors, memory, and a support ASIC that provides RACEway mapping logic, DMA controllers, performance metering logic, and realtime OS support hardware.

The first compute-node daughtercards available for the RACE-MCH motherboards are based on the Analog Devices SHARC digital signal processor and on the IBM/Apple/ Motorola PowerPC microprocessor. The SHARC and PowerPC processors join the existing RACE Series product line as heterogeneous complements to the Intel i860 RISC processor.

Based on the 40 MHz, 120 MFLOPS ADSP-21060 processor, two SHARC-based daughtercards are available immediately. The high-density S2T16B integrates six SHARC processors with 32 Mbytes of DRAM, and the large memory S1D64B provides 64 Mbytes of DRAM to support a pair of SHARCs for memory intensive applications. Because the SHARC DSP dissipates only a few watts, it enables more than twice the physical processor density than RISC-based compute nodes.

Two daughtercards based on the 100 MHz, 200 MFLOPS PowerPC 603e are also available now. The P2A16B combines two PowerPC processor nodes with 16 Mbytes of DRAM each (32 Mbytes total), while the P2A8B provides 8 Mbytes of DRAM to each of two processors (16 Mbytes total). The PowerPC's modern superscaler RISC features make it ideal for compiled code scalar- and vector-math-based applications. Also available now are RIN-T-B and ROUT-T- B daughtercards which support VITA-draft-standard front panel data port (FPDP) external I/O connectivity.

Software supports heterogeneity

Mercury's Multicomputer Software Backplane (MSB) provides a complete solution for rapid integration of off-the-shelf hardware and software function blocks into the heterogeneous RACE environment. The MSB establishes an open software infrastructure that eliminates the software complexity of mixed node-type heterogeneous designs by seamlessly integrating different processor types, operating systems, application programming interfaces, and development tools.

Compute node daughtercards are supported by a common development and runtime software environment for multiple processor types. Software support includes the MC/OS realtime operating kernel, ANSI C compilers and linkers, and the Scientific Algorithm Library. Also available are a process-level debugger, a system-level debugger (SuperVision), and the Parallel Application System that enables different processor types to be programmed from one set of software.

Price and availability

U.S. OEM pricing starts at $25,000 for a 1 GFLOP heterogeneous system consisting of six SHARC and two PowerPC processors. Evaluation systems are available immediately and full production systems will be available in the first calendar quarter of 1996.

Mercury Computer Systems, Inc. is a leading supplier of high-performance heterogeneous multicomputers for realtime applications. Its product line ranges from four-processor board-level products to systems with over 1,000 processors. Systems are available in commercial, ruggedized, and MIL-SPEC packaging. These products provide application-specific solutions for a variety of markets ranging from defense and security to medical diagnostic and commercial image processing. More than 30,000 units are installed worldwide. -0-

RACE is a registered trademark and Multicomputer Software Backplane is a trademark of Mercury Computer Systems, Inc.

CONTACT: Leigh McLeod

Mercury Computer Systems, Inc.

(508) 256-1300

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