Mitsubishi AJ71UC24

Melsec-A Computer Link / Multi-Drop Link Module

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MELSEC-A

User's Manual

Computer link/multidrop link module type AJ71UC24 (Supplement)

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REVISIONS

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

COMMON INFORMATION

COMPUTER LINK FUNCTION

COMMON INFORMATION

This part describes the the system configuration, general specifications, checks before test operation, and other information common to the operation of the AJ71UC24 when it is used as a computer link module or multidrop link function module.

1. GENERAL DESCRIPTION

This User's Manual describes how to use the AJ71UC24 type computer link/multidrop module (hereinafter called the AJ71UC24).
This manual covers the specifications and functions that cannot be found in the User's Manual for the AJ71C24-S8 computer link module (IB-66360). For specifications and functions not contained herein, see the User's Manual for the AJ71C24-S8 prior to use of the AJ71UC24.

The AJ71UC24 is a modified version of the conventional AJ71C24-S8, equipped with an inexpensive multidrop link function using an RS-422/485 interface.

The following terminal resistances are packed with the module:

- 330 Ω, 1/2 W (for RS-422 communications)
- 110 Ω, 1/2 W (for RS-485 communications)

1.1 Contents of This Manual

This manual contains the information that is different from the contents of the AJ71C24-S8 User's Manual.
Each section number in this manual corresponds to that in the AJ71C24-S8 User's Manual. Listed below are the section numbers with contents different from those in the AJ71C24-S8 User's Manual. When you reach such section numbers in the AJ71C24-S8 User's Manual, replace them with or refer to the contents of this manual.

(1) The terms which should be replaced in referring to the AJ71C24-S8 User's Manual

- AJ71C24-S8 . . . . . AJ71UC24
- RS-422 . . . . . RS-422/485

(2) Section numbers with different contents

2.4	System Configurations (When Selecting a Multidrop Link Function)
2.5	When Using a Multidrop Link Function and a Computer Link Function Simultaneously
3.2.3	RS-422/485 interface
3.3.1	Functions available using dedicated protocols and commands
3.4	Mode Switching Function While the Computer Link Module is Operating
3.6	I/O Signals List for CPU
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4.2	Nomenclature and LED Signals and Displays
4.3.4	Terminal resistance connections
8.11	Remote Run/Stop of PC CPU and Reading PC CPU Model Name
11.1	NAK Error Codes with Dedicated Protocols
12 to 16	MULTIDROP LINK FUNCTION

REMARK

The section numbers in Chapter 1 and Appendix do not match those in the AJ71C24-S8 User's Manual.

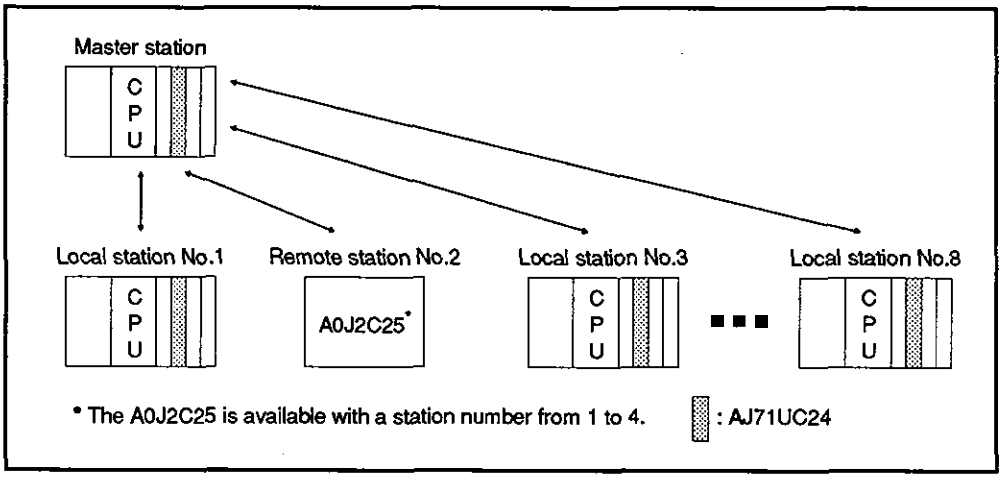
1.2 Features

(1) Storing switch settings in buffer memory

The settings of the switches (mode setting, station number setting and transmission specification setting) on the face of the AJ71UC24 and the RS-232C signal data can be read out of the buffer memory to check.

(2) Multidrop link function added

For the multidrop link function, a flexible, inexpensive input/output signal communications system using an RS-422/485 interface can be set up.
This function permits input/output signal communications between a master station and local or remote stations. Up to eight local or remote stations are connectable to a master station.



(a) When using the AJ71UC24 as a master station

1) A total of eight slave stations (local station: AJ71UC24, A1SJ71C24-R4, A0J2-C214 (S1), remote station: A0J2C25) can be connected to a master station.

2) Up to eight AJ71UC24s can be set as master stations with a PC CPU.

3) The transmission speed in the link, the total extension distance, and the maximum number of link points are 38400 BPS, 500 m, and 512 points (maximum 128 input points and 128 output points per slave station) respectively.

4) If a linking slave station is down, it can be disconnected from the link system to continue normal data link operations or discontinue data transmission to the entire link system.

5) A designated slave station can be isolated (which means the data to be transferred to and from the station will be all OFF).

(b) When using the AJ71UC24 as a local station

1) The AJ71C22 (S1), AJ71UC24, A1SJ71C24-R4 or A0J2-C214 (S1) can be used as the master station.

2) A total of eight AJ71UC24s are connectable as local stations to a master station.

3) The maximum transmission speed in the link is 38400 BPS, however, the maximum number of link points depends on the allocation in the master station.

1.2.1 Control operations using the multidrop link function

The multidrop link function controls the following operations:

(1) When an AJ71UC24 is used as a master station

(a) Writing the bit device status in the PC CPU (master station) to the buffer using a TO instruction.

(b) Writing data via the RS-422 cable to the buffer in a local station.

(c) Reading receive data (in the buffer) in the PC CPU using a FROM instruction.

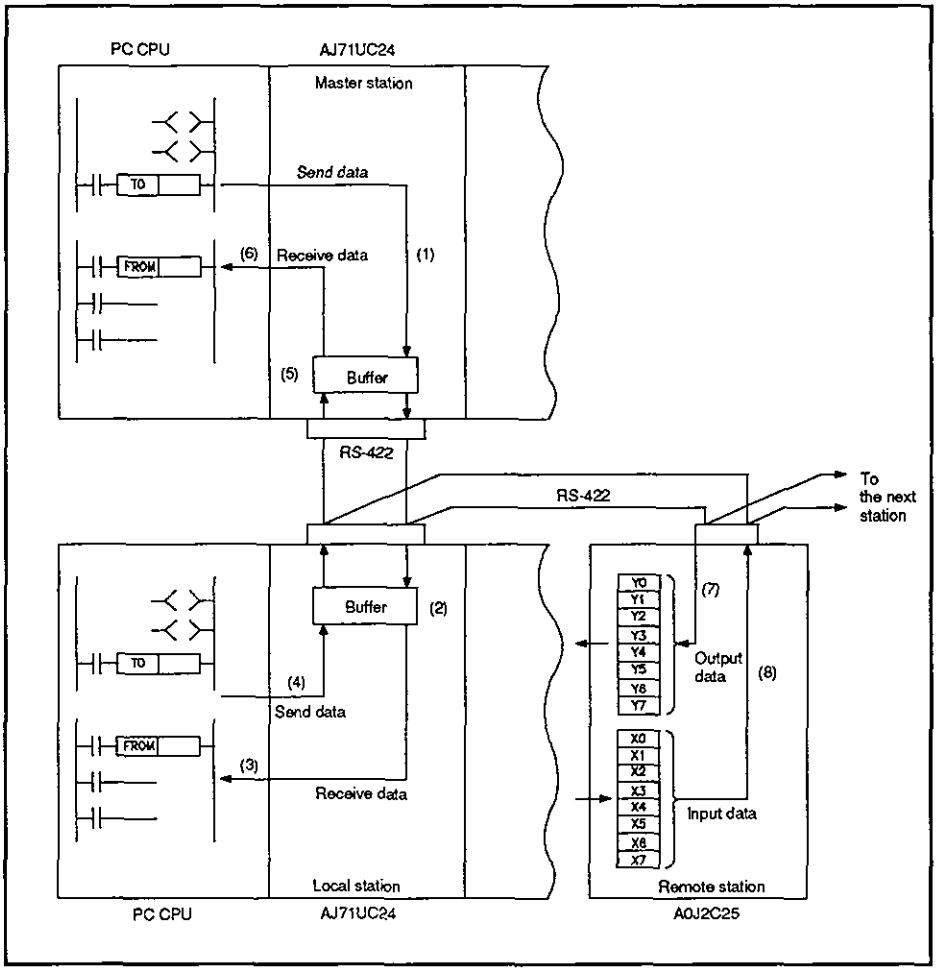
(d) Writing the bit device status in the PC CPU (local station) to the buffer using a TO instruction.

(e) Writing data (in the local or remote station) via the RS-422 cable to the buffer in a master station.

(f) Reading receive data (in the buffer) in the PC CPU using a FROM instruction.

(g) Outputting send data in the buffer (in a master station) to the buffer in a remote station.

(h) Writing data (input from an external device) as the received data to the buffer in a master station.



(2) When an AJ71UC24 is used as a local station

(a) Writing the bit device status in the PC CPU (local station) to the buffer using a TO instruction.

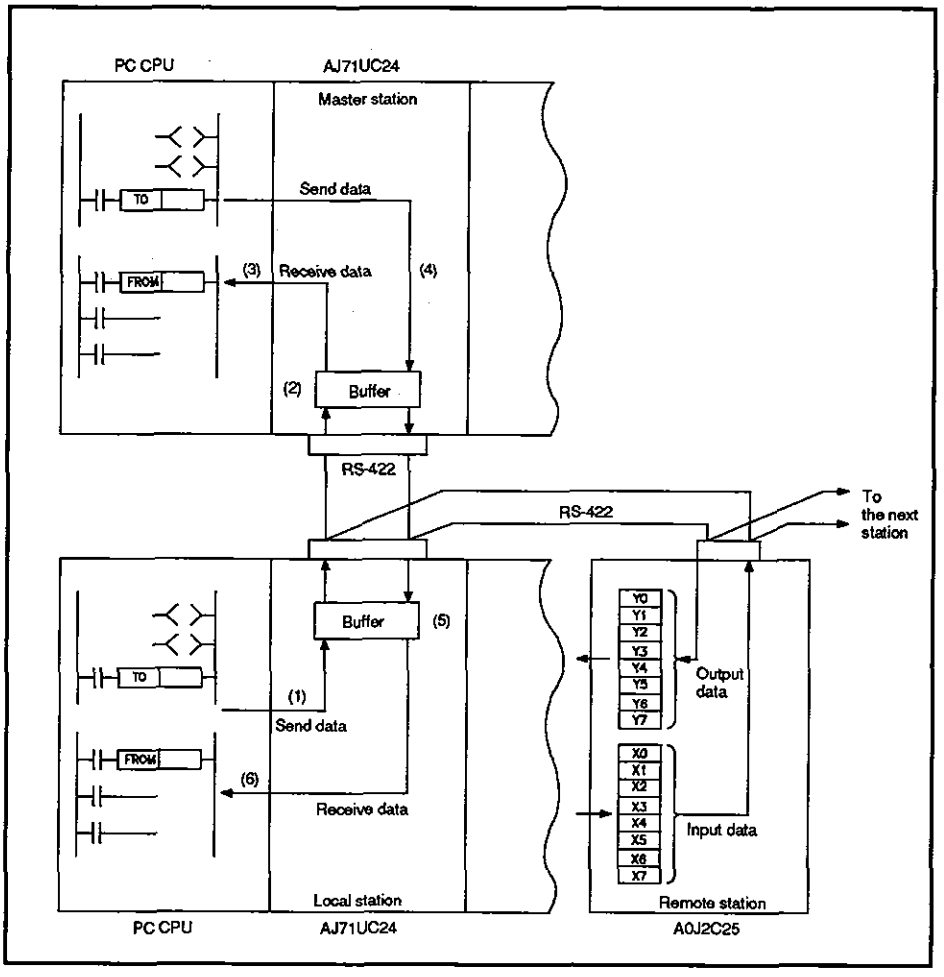
(b) Writing data via the RS-422 cable to the buffer in a master station.

(c) Reading receive data (in the buffer) in the PC CPU using a FROM instruction.

(d) Writing the bit device status in the PC CPU (master station) to the buffer using a TO instruction.

(e) Writing data via the RS-422 cable to the buffer in a local station.

(f) Reading receive data (in the buffer) in the PC CPU using a FROM instruction.



2. SYSTEM CONFIGURATIONS

This chapter describes system configurations compatible with the AJ71UC24.

2.1 Overall Configuration

Fig. 2.1 shows the overall configuration of a system which is loaded with the AJ71UC24.

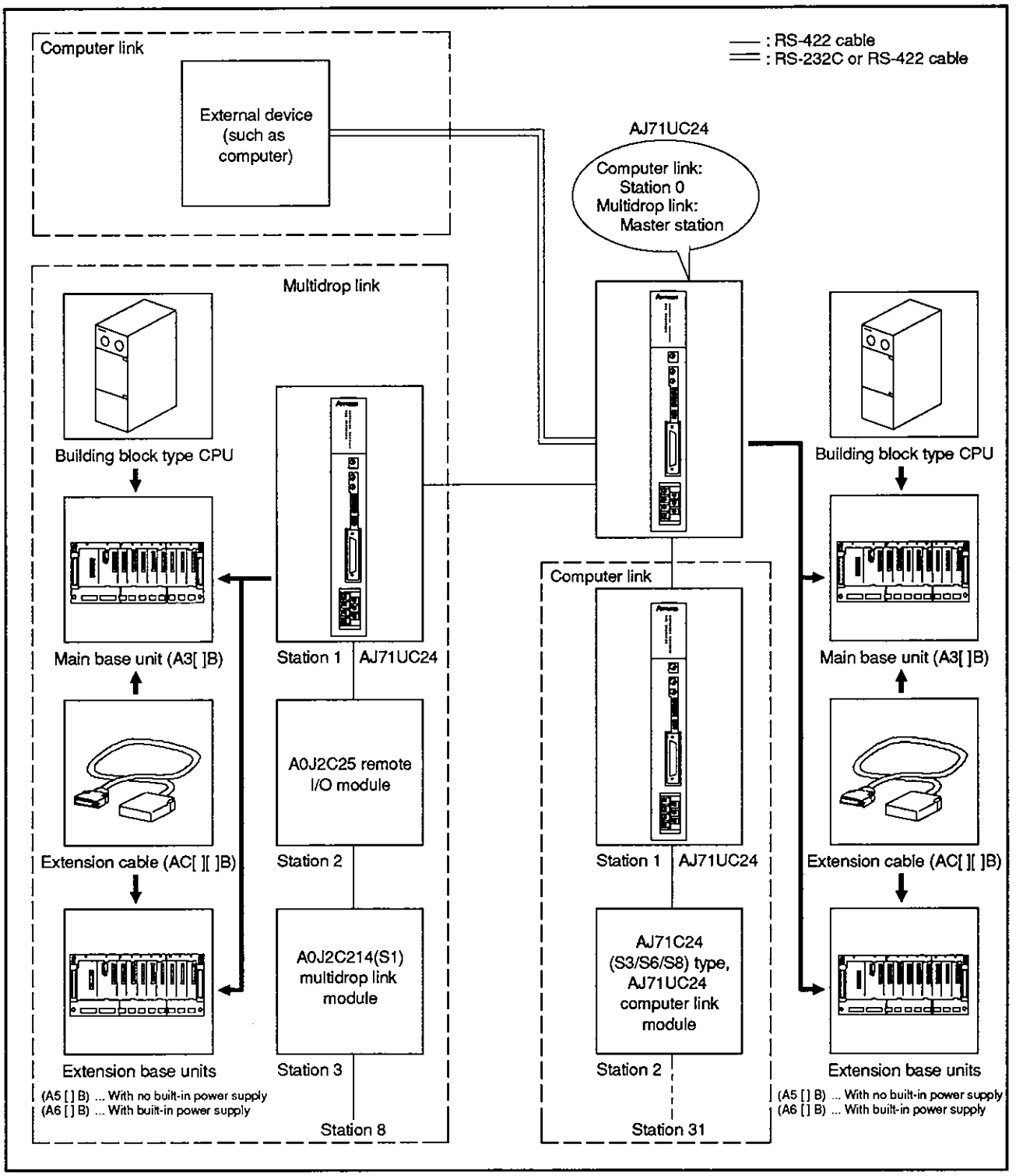


Fig. 2.1 Overall Configuration

2.2 Applicable Systems

The AJ71UC24 can be used with the systems described below.

(1) Applicable PC CPU modules and the number of AJ71UC24 modules to be connected

(a) The table below shows the applicable PC CPU modules for which the AJ71UC24 will be used as the computer link, and the number of AJ71UC24 modules to be connected to the modules.
Each applicable PC CPU module includes a module equipped with an MELSECNET link function.
[e.g. The A2ACPU includes an A2ACPUP21 and an A2ACPUR21 to both of which an AJ71UC24 can be connected.]

Applicable PC CPU Modules	Number of Connectable AJ71UC24s	Remarks
A0J2H A1, A1N A1S A2(-S1), A2N(-S1) A3, A3N A3H, A3M A73 A373 A52G	2	If each of the following modules is used with the AJ71UC24, the maximum number of connectable AJ71UC24 modules to it must not exceed 2 or 6. • AD51(S3) Intelligent Communication Module • AD51H(S3) Intelligent Communication Module • AD51FD External Failure Diagnosis Module • AD57G Graphic Controller Module • AJ71C21(S1) Terminal Interface Module (only in BASIC Program Mode) • AJ71C22(S1) Multidrop Link System Module • AJ71C23 Higher Controller High Speed Link Module • AJ71C24(-S3/S6/S8) Computer Link Module • AJ71P41 SUMINET Interface Module • AJ71E71 Ethernet Interface Module • AJ71UC24 Computer Link/Multidrop Link Module
A2A(-S1) A3A	6	

(The AJ71UC24 is unapplicable to the A0J2CPU and the A2CCPU.)

(2) Applicable base unit

The AJ71UC24 can be inserted into any slot of a main base unit or extension base unit, except for the following two cases:

(a) The power supply capacity of the extension base unit (A55B or A58B) with no built-in power supply may be insufficient to load the AJ71UC24 into it. Wherever possible, avoid loading an AJ71UC24 module into this type of extension base unit.
If such an extension base unit requires an AJ71UC24 module, select a power supply unit and extension cables after due consideration for both the capacity of the power supply unit and the voltage drop in the extension cables.
(For details, see the User's Manual for each applicable PC CPU module (see (1) above).)

(b) The AJ71UC24 should not be loaded into the last slot of the A3CPU extension level 7.

POINTS

- One AJ71UC24 can be loaded into the A81CPU base unit (A78B) also. For available commands, see the A81CPU User's Manual.
- The AJ71UC24 cannot be used in a remote I/O station.

2.3 System Configurations and Available Functions (When Using the Computer Link Function)

2.3.1 1 : 1 ratio of an external device (computer, etc.) to a PC CPU

2.3.2 1 : n ratio of an external device (computer, etc.) to PC CPUs

2.3.3 2 : 1 ratio of external devices (computer, etc.) to a PC CPU

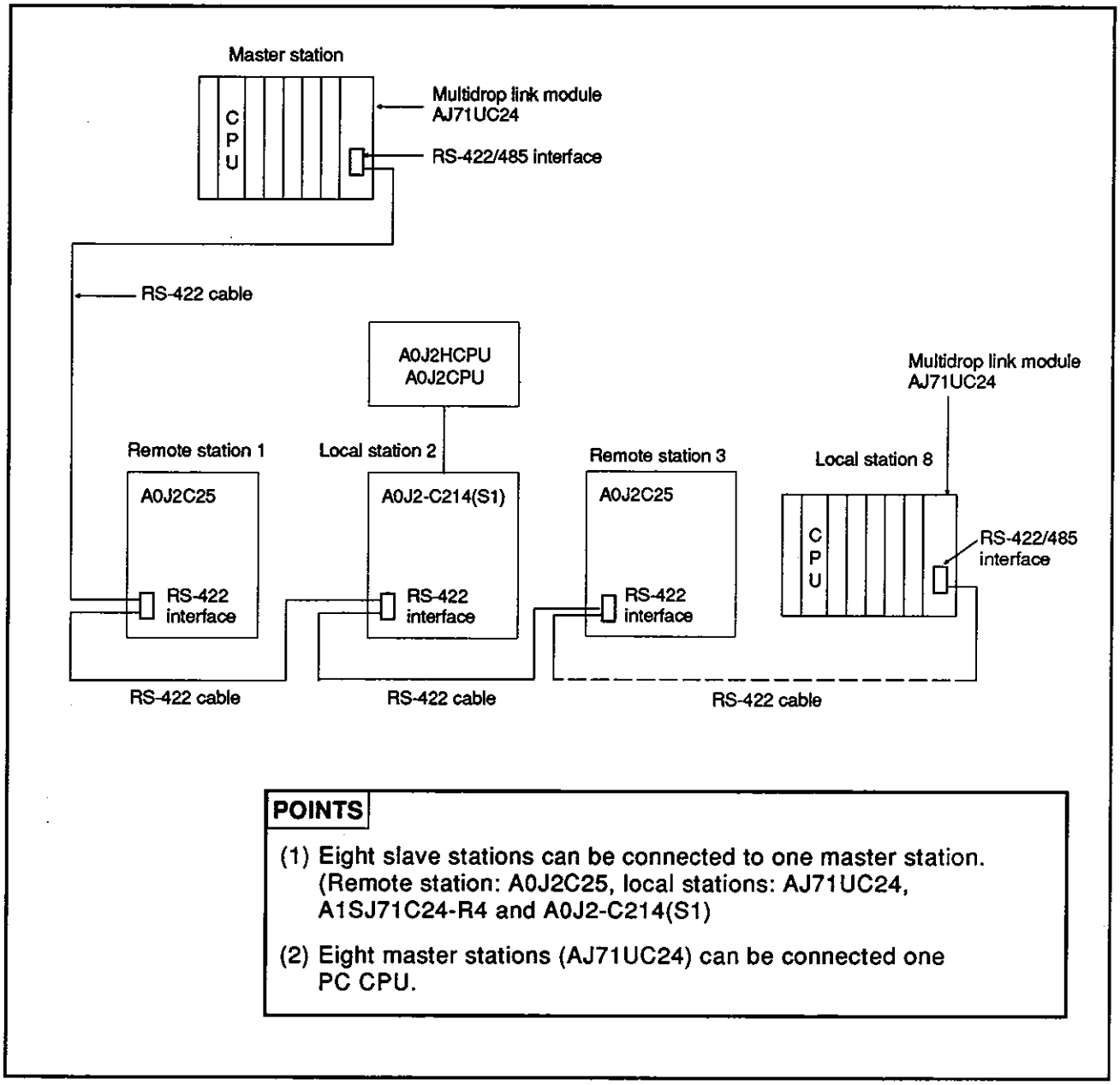
2.3.4 2 : n ratio of external devices (computer, etc.) to PC CPUs

2.3.5 m : n ratio of external devices (computer, etc.) to PC CPUs

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

2.4 When Selecting a Multidrop Link Function

2.4.1 When using an AJ71UC24 as a master station



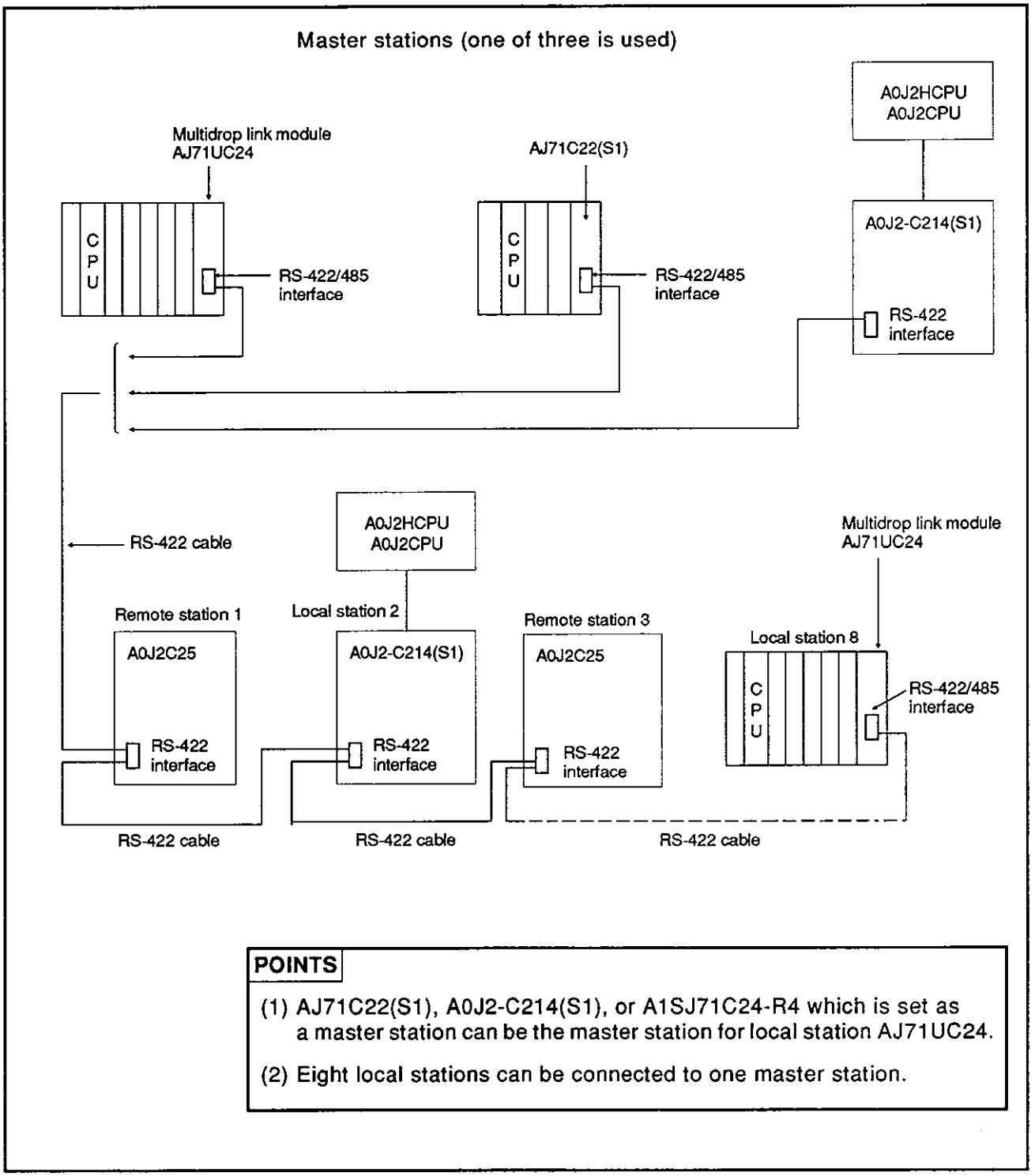
POINTS

(1) Eight slave stations can be connected to one master station. (Remote station: A0J2C25, local stations: AJ71UC24, A1SJ71C24-R4 and A0J2-C214(S1)

(2) Eight master stations (AJ71UC24) can be connected one PC CPU.

Fig. 2.2 System Configurations (IV)

2.4.2 When using an AJ71UC24 as a local station



POINTS

(1) AJ71C22(S1), A0J2-C214(S1), or A1SJ71C24-R4 which is set as a master station can be the master station for local station AJ71UC24.

(2) Eight local stations can be connected to one master station.

Fig. 2.3 System Configurations (V)

2.5 When Using a Multidrop Link Function and a Computer Link Function Simultaneously

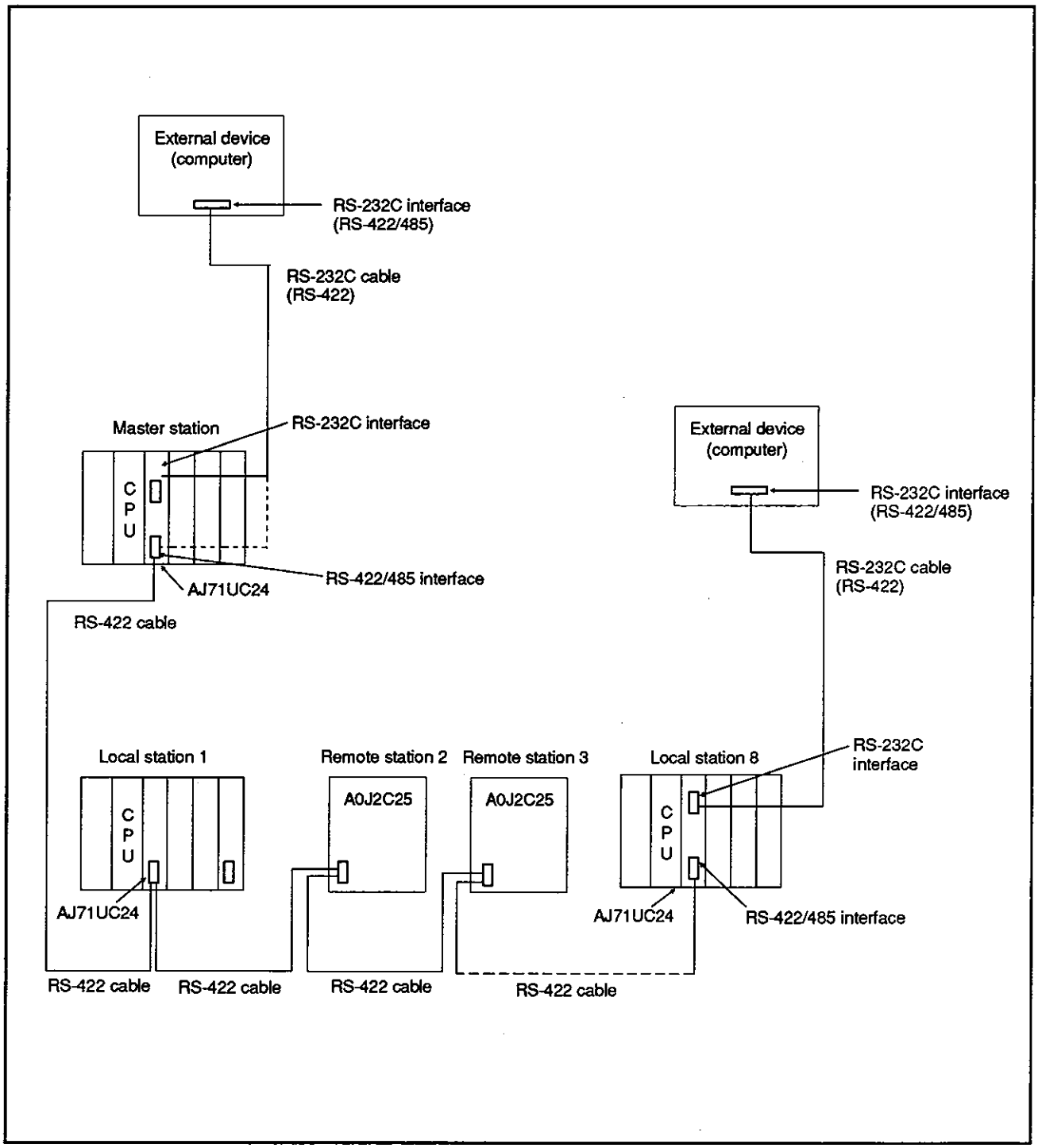


Fig. 2.4 System Configuration (IV)

2.6 Precautions Regarding System Configurations

Described below are the matters requiring consideration in building an AJ71UC24 system.

(1) The applicable modules for local stations with the AJ71UC24 used as a master station are as follows:

- AJ71UC24 computer link module/multidrop link module
- A1SJ71C24-R4 computer link module/multidrop link module
- A0J2-C214(S1) computer link module/multidrop link module

(2) The applicable module for a remote station with the AJ71UC24 used as a master station is as follows:

- A0J2C25 remote I/O module

(3) The applicable modules for master stations with the AJ71UC24 used as a local station are as follows:

- AJ71UC24 computer link module/multidrop link module
- A0J2-C214(S1) computer link module/multidrop link module
- A1SJ71C24-R4 computer link module/multidrop link module
- AJ71C22(-S1) multidrop link module

(4) The following tables show which of RS-422 port and the RS-485 port should be used in the computer and multidrop link modules.

When using the AJ71UC24 in the computer link module

System	RS-422/RS-485 Communications
Computer (RS-422) + AJ71UC24	RS-422
Computer (RS-485) + AJ71UC24	RS-485

When using the AJ71UC24 in the multidrop link module

System	RS-422/RS-485 Communications
AJ71UC24 only	RS-422 or RS-485
AJ71UC24 + A0J2C25	RS-422
AJ71UC24 + A0J2-C214(S1)	RS-422
AJ71UC24 + AJ71C22(S1)	RS-422
AJ71UC24 + A1SJ71C24-R4	RS-422 or RS-485

MEMO

COMPUTER LINK FUNCTION

This part describes the specifications, functions and settings necessary to use the AJ71UC24 as a computer link function module, and commands for data communications with the computer or printer.

3. SPECIFICATIONS

3.1 General Specifications

Table 3.1 General Specifications

<table>
<tr><th>Item</th><th colspan="5">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="5">0 to 55°C (32 to 131°F)</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">–20 to 75° (4 to 167°F)</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="5">10 to 90% RH, no condensation</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90% RH, no condensation</td></tr>
<tr><td rowspan="3">Vibration resistance</td><td rowspan="3">Conforms to **JIS C 0911</td><td>Frequency</td><td>Accelera-tion</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 55 Hz</td><td>—</td><td>0.075 mm (0.003 inch)</td><td rowspan="2">10 times *(1 octave/ minute)</td></tr>
<tr><td>55 to 150 Hz</td><td>9.8 m/s^2 (1 g)</td><td>—</td></tr>
<tr><td>Shock resistance</td><td colspan="5">Conforms to JIS C 0912 (98 m/s^2 (10g) x 3 times in 3 directions)</td></tr>
<tr><td>Noise resistance</td><td colspan="5">By noise simulator 1500 V.P.P. noise voltage, 1 μsec noise width and 25 to 60 Hz noise frequency</td></tr>
<tr><td>Dielectric withstand voltage</td><td colspan="5">500 VAC for 1 minute across batch of DC external terminals and ground</td></tr>
<tr><td>Insulation resistance</td><td colspan="5">50 MΩ or more with 500 VDC insulation resistance tester at the same location as dielectric strength.</td></tr>
<tr><td>Operating ambience</td><td colspan="5">No corrosive gases or dust.</td></tr>
<tr><td>Cooling method</td><td colspan="5">Self-cooling</td></tr>
</table>

REMARK

(1) One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10 Hz to 20 Hz, 20 Hz to 40 Hz, 40 Hz to 20 Hz, and 20 Hz to 10 Hz are referred to as one octave.

(2) The noise durability and dielectric withstand voltage values were obtained with the RS-232C and RS-422 interfaces unconnected.

** JIS: Japanese Industrial Standard

3.2 Performance Specifications

3.2.1 Transmission specifications

Table 3.2 Transmission Specifications

Item		Specifications		
Interface		Conform to RS-232C.		
		Conform to RS-422/485.		
Transmission method		RS-232C	Dedicated protocol	Half-duplex communications system *1
			No-protocol/bidirectional	Full-/half-duplex (buffer memory setting)
		RS-422	Dedicated protocol	Half-duplex communications system *1
			No-protocol/bidirectional	Full-duplex communications system
Synchronous system		Asynchronous system		
Transmission system		300, 600, 1200, 2400, 4800, 9600, 19200 BPS (switch selected)		
Data format	Start bit	1		
	Data bit	7 or 8		Selectable
	Parity bit	1 or none *4		
	Stop bit	1 or 2		
Access cycle		Each request is processed in the END processing of the sequence program. Therefore, access cycle is 1 scan time.		
Error detection		Parity check present (odd/even)/absent		
		Sum check present/absent		
DTR/DSR (ER/DR) control		Present /Absent (RS-232C only)		Selectable
DC1/DC3, DC2/DC4 control		Present /Absent		
System configuration (External device: PC CPU)		Dedicated protocol		1 : 1, 1 : n, m : n *2
		No-protocol		1 : 1, 1 : n *2
		Bidirectional		1 : 1
Transmission distance		Up to 15 m (49.2 ft) for RS-232C		
		Up to 500 m (1640.5 ft) for RS-422/485		
Current consumption		5 VDC, 1.4 A		
Number of occupying I/Os		32 *3		
Weight		630 g (1.39 lb)		
Recommended cable (for RS-422)		RS-422 SPEV(SB)- MPC - 0.2 x 3P		
Recommended RS-232C to RS-422 converter		SC-02N *5		

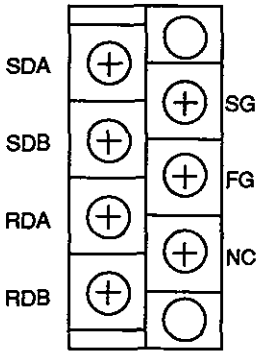
*1: If the on-demand function is used, only full-duplex communications is available when full-duplex communications is enabled.
*2: "n" for 1:n ratio is up to 32. Total of "m" and "n" for m:n ratio is up to 32.
*3: Set the special function modules to have 32 inputs/outputs (F32) when the I/O allocation is set.
Set the type of module to AJ71C24S3 when the AnA dedicated command for AJ71UC24 is used.
*4: Horizontal parity
*5: Recommended equipment. Consult the nearest Mitsubishi representative about the RS-232C to RS-422 converter.

3.2.2 RS-232C connector specifications

The specifications of the RS-232C connector are as described in the corresponding section in the AJ71C24-S8 User's Manual.

3.2.3 RS-422/485 interface specifications

(1) Fig. 3.1 shows the specifications of the RS-422/485 interface for connection with the computer or AJ71UC24.



Signal Abbreviation	Signal Direction AJ71UC24 ↔ Computer	Description
SDA	→	Send data
SDB	→	Send data
RDA	←	Receive data
RDB	←	Receive data
SG	↔	Signal ground
FG	↔	Frame ground
NC	—	Free

Fig. 3.1 RS-422/485 Interface

(2) Fig. 3.2 shows the functional block diagram of the RS-422/485 interface.

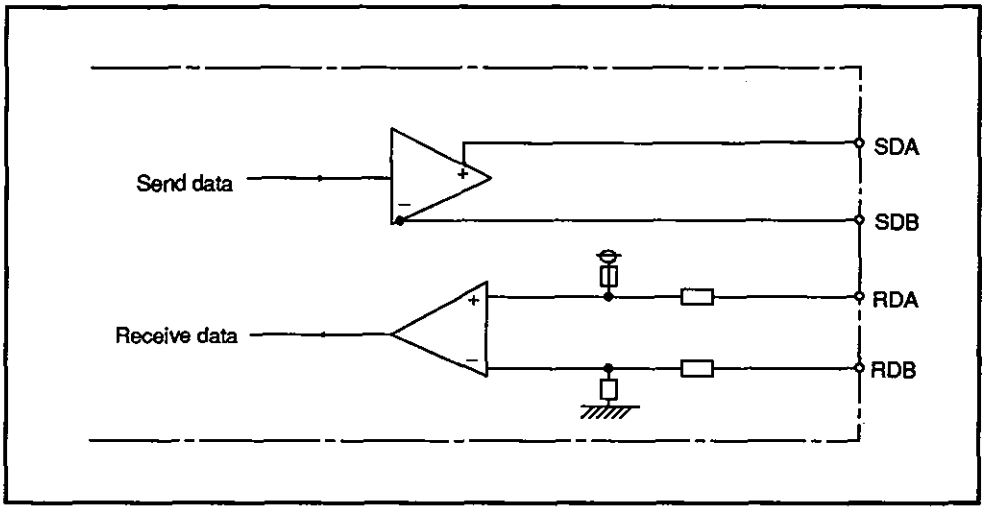


Fig. 3.2 RS-422/485 Interface Functional Block Diagram

3.2.4 RS-422 cable specifications

The specifications of the RS-422 cable are as shown in the corresponding section in the AJ71C24-S8 User's Manual.

3.3 Data Communications Functions

The tables below list the data communications functions available when an external device (such as a computer) and a PC CPU are connected by an AJ71UC24 module.

3.3.1 Functions available using dedicated protocols and commands

The functions available using dedicated protocols 1 to 4 are listed in Tables 3.3 and 3.4.

The commands in Table 3.3 are the ACPU common commands that are employed when a CPU module is used together with an AJ71UC24.

The commands in Table 3.4 are the AnACPU dedicated commands that are employed when the A2ACPU(P21/R21)(-S1) or A3ACPU(P21/R21) is used together with an AJ71UC24.

(1) Functions available with the ACPU common commands

Table 3.3 Functions List When Using a Dedicated Protocol

Function			Command: Symbol	Command: ASCII Code	Description	Number of Point Processed per Communications
Device memory	Batch read	Bit units	BR	42H, 52H	Reads bit devices (such as X, Y, M) in units of 1 device.	256 points
		Word units	WR	57H, 52H	Reads bit devices (such as X, Y, M) in units of 16 devices.	32 words (512 points)
					Reads word devices (such as D, R, T, C) in units of 1 device.	64 points
	Batch write	Bit units	BW	42H, 57H	Writes bit devices (such as X, Y, M) in units of 1 device.	160 points
		Word units	WW	57H, 57H	Writes bit devices (such as X, Y, M) in units of 16 devices.	10 words (160 points)
					Writes word devices (such as D, R, T, C) in units of 1 device.	64 points
	Test (random write)	Bit units	BT	42H, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 1 device at random and sets/resets the device.	20 points
		Word units	WT	57H, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 16 devices at random and sets/resets the device.	10 words (160 points)
					Specifies word devices (such as D, R, T, C) and device number in units of 1device at random and sets/resets the device.	10 points
	Monitor data entry	Bit units	BM	42H, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 1 device.	40 points *1
		Word units	WM	57H, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 16 devices.	20 words *1 (320 points)
					Sets word devices to be monitored (such as D, R, T, C) in units of 1 device.	20 points
	Monitor	Bit units	MB	4DH, 42H	Reads data from devices for which device data registration has been made.	—
		Word units	MN	4DH, 4EH		
Extension file register	Batch read		ER	45H, 52H	Reads extension file registers (R) in units of 1 register.	64 points
	Batch write		EW	45H, 57H	Writes extension file registers (R) in units of 1 register.	64 points
	Test (random write)		ET	45H, 54H	Specifies the extension file registers (R) in units of 1 register using block or device number and makes a random write.	10 points
	Monitor data registration		EM	45H, 4DH	Sets the extension file registers (R) device numbers to be monitored in units of 1 register.	20 points
	Monitor		ME	4DH, 45H	Monitors the extension file register after monitor data registration.	—

PC CPUs with Which the Command can be Executed										PC CPU State			Reference Section
A0J 2H A1S	A1N A1	A2N(S1) A2(S1)	A2A (S1)	A52G	A3N A3	A3A	A3H	A3M	A73	During STOP	During RUN		
											SW22 ON	SW22 OFF	
				o						o	o	o	8.7.2
													8.7.3
				o						o	o	x	8.7.4
													8.7.5
				o						o	o	x	8.7.6
													8.7.7
				o						o	o	o	8.7.8
				o						o	o	o	
o	x	o								o	o	o	8.8.4
o	x	o								o	o	x	8.8.5
o	x	o								o	o	x	8.8.8
o	x	o								o	o	o	8.8.9
o	x	o								o	o	o	

Table 3.3 Functions List When Using a Dedicated Protocol (Continued)

Function				Command: Symbol	Command: ASCII Code	Description		Number of Point Processed per Communications
Buffer memory	Batch read			CR	43H, 52H	Reads data from the AJ71UC24 buffer memory.	Also usable for communications between the sequence program and the external devices when a multidrop link is made.	64 words (128 bytes)
	Batch write			CW	43H, 57H	Writes data to the AJ71UC24 buffer memory.		
Special function module	Batch read			TR	54H, 52H	Reads the contents of the special function module buffer memory.		64 words (128 bytes)
	Batch write			TW	54H, 57H	Writes data to the special function module buffer memory.		
Sequence Program	Batch read	Main	Other than T/C set value	MR	4DH, 52H	Reads main sequence programs.		64 steps
			T/C set value			Reads T/C set values used in main sequence programs.		64 points
		Sub	Other than T/C set value	SR	53H, 52H	Reads subsequence programs.		64 steps
			T/C set value			Reads T/C set values used in subsequence programs.		64 points
	Batch write	Main	Other than T/C set value	MW	4DH, 57H	Writes main sequence programs.		64 steps
			T/C set value			Writes T/C set values used in main sequence programs.		64 points
		Sub	Other than T/C set value	SW	53H, 57H	Writes subsequence programs.		64 steps
			T/C set value			Writes T/C set values used in subsequence programs.		64 points
Micro computer program	Batch read		Main	UR	55H, 52H	Reads main microcomputer programs.		128 bytes
			Sub	VR	56H, 52H	Reads submicrocomputer programs.		
	Batch write		Main	UW	55H, 57H	Writes main microcomputer programs.		
			Sun	VW	56H, 57H	Writes submicrocomputer programs.		
Comment	Batch read			KR	4BH, 52H	Reads comment data.		128 bytes
	Batch write			KW	4BH, 57H	Writes comment data.		
Parameter	Batch read			PR	50H, 52H	Reads parameters from PC CPU.		128 bytes
	Batch write			PW	50H, 57H	Writes parameters to PC CPU.		
	Analysis request			PS	50H, 53H	Causes PC CPU to acknowledge and check rewritten parameters.		—
PC CPU	Remote RUN			RR	52H, 52H	Request remote run/stop of PC CPU.		—
	Remote STOP			RS	52H, 53H			
	PC CPU model name code read			PC	50H, 43H	Reads the model name code of the PC CPU.		
	PC CPU model name/code read			PU	50H, 55H	Reads the model name and its code of the PC CPU.		
Global				GW	47H, 57H	Turns ON and OFF the global signal of the AJ71UC24 loaded in each PC CPU system.		1 point
On-demand				—		Send request is initiated by a PC CPU. (Available in a 1:1 ratio system.)		Data length specified in the sequence program. (Max. 1760 words)
Loopback test				TT	54H, 54H	Echoes unchanged characters back to the computer.		254 characters

PC CPUs with Which the Command can be Executed										PC CPU State			Reference Sections
A0J 2H A1S	A1N A1	A2N(S1) A2(S1)	A2A (S1)	A52G	A3N A3	A3A	A3H	A3M	A73	During STOP	During RUN SW22 ON	During RUN SW22 OFF	
o										o	o	o	8.9.2
													8.9.3
o										o	o	o	8.10.3
o										o	o	x	8.10.4
o										o	o	o	8.12.4
x				o						o	o	o	
o										o	o *2	x	
o										o	o	x	
x				o						o	o *2	x	
x				o						o	o	x	
o			x	o		x		o		o	o	o	8.12.5
x													
o			x	o		x		o		o	o *2	x	
x													
o										o	o	o	8.12.6
o										o	o	x	
o										o	o	o	8.12.3
o										o	x	x	
o										o	x	x	
o										o	o	o	8.11.2
o										o	o	o	8.11.3
o										o	o	o	8.11.4
o										o	o	o	8.13
o										—	o	o	8.14
o										o	o	o	8.15

*1: When the CPU modules other than A3H, A2A(S1), and A3A are used, devices X (input) are allocated with 2 inputs per device.

To include devices X in designated devices, set as follows:

((number of designated X devices x 2) + number of other designated devices) ≤ 40

If only devices X are designated, the number of inputs usable for one communications time is half the value mentioned in the table.

*2: Writing during a program run may be carried out if all the following conditions are met:

(This is different from the write during PC RUN with a MELSEC-A series peripheral device (e.g., A6GPP).)

(a) The PC CPU is type A3, A3N, A3H, A3M, A73 or A3A.

(b) The program is not the currently running program.

(includes subprograms called by the currently running main program)

(c) The PC CPU special relay is in the following states:

1) M9050 signal flow exchange contact .....OFF (A3CPU only)

2) M9051 (CHG instruction disable).....ON

POINT

When the AJ71UC24 is used together with the A2ACPU(S1) or A3ACPU, use the commands in Table 3.4 to perform the following functions:

- Batch read/write, test, monitor data registration, and monitor of device memory
- Batch read/write of extension file registers by designating device numbers (continuous numbers)
- Batch read/write of extension comments

When the commands in Table 3.3 are used, the available functions and the range of devices which can be designated are limited to those available with the A3HCPU.

Accordingly, A2ACPU(S1) and A3ACPU external devices are not accessible.

(2) Functions available with the AnACPU dedicated commands

Table 3.4 Functions List When Using a Dedicated Protocol

Function			Commands: Symbol	Commands: ASCII Code	Description	Number of Point Processed per Communications	PC CPU State: During STOP	PC CPU State: During RUN: SW22 ON	PC CPU State: During RUN: SW22 OFF	Reference Sections
Device memory	Batch read	Bit units	JR	4AH, 52H	Reads bit devices (such as X, Y, M) in units of 1 device.	256 points	o	o	o	8.7.2
		Word units	QR	51H, 52H	Reads bit devices (such as X, Y, M) in units of 16 devices.	32 words (512 points)				8.7.3
					Reads word devices (such as D, R, T, C) in units of 1 device.	64 points				
	Batch write	Bit units	JW	4AH, 57H	Writes bit devices (such as X, Y, M) in units of 1 device.	160 points	o	o	x	8.7.4
		Word units	QW	51H, 57H	Writes bit devices (such as X, Y, M) in units of 16 devices.	10 words (160 points)				8.7.5
					Writes word devices (such as D, R, T, C) in units of 1 device.	64 points				
	Test (random write)	Bit units	JT	4AH, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 1 device at random and sets/resets the device.	20 points	o	o	x	8.7.6
		Word units	QT	51H, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 16 devices at random and sets/resets the device.	10 words (160 points)				8.7.7
					Specifies word devices (such as D, R, T, C) and device number in units of 1 device at random and sets/resets the device.	10 points				
	Monitor data registration	Bit units	JM	4AH, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 1 device.	40 points	o	o	o	8.7.8
		Word units	QM	51H, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 16 devices.	20 words (320 points)				
					Sets word devices to be monitored (such as D, R, T, C) in units of 1 device.	20 points				
	Monitor	Bit units	MJ	4DH, 4AH	Reads data from devices for which device data has been registered.	—	o	o	o	
		Word units	MQ	4DH, 51H						
Extension file register	Direct read	Word units	NR	4EH, 52H	Reads data in units of 1 device by designating the device numbers continuously regardless of the extension file register block numbers.	64 points	o	o	o	8.8.6
	Direct write	Word units	NW	4EH, 57H	Writes data in units of 1 device by designating the device numbers continuously regardless of the extension file register block numbers.	64 points	o	o	x	8.8.7
Extension comment	Batch read		DR	44H, 52H	Reads the extension comment data.	128 bytes	o	o	o	8.12.7
	Batch write		DW	44H, 57H	Writes the extension comment data.		o	o	x	

POINT

The commands given in Table 3.4 can be used when the AJ71UC24 is used together with the A2ACPU(S1) or A3ACPU. The whole range of device memory is accessible using these commands.
For functions other than those listed in Table 3.4, use the commands given in Table 3.3.

3.3.2 Functions available in the no-protocol mode

3.3.3 Functions available in the bidirectional mode

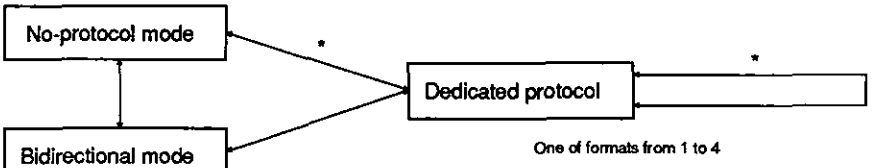
3.3.4 Transmission error data read function

The above functions are as described in the respective corresponding sections of the AJ71C24-S8 User's Manual.

3.4 Mode Switching Function During Computer Link Operations

Read this section carefully prior to switching the mode (changing the transmission control protocol) in the middle of computer link operations to continue data communications with a connected device. It is unnecessary to consult with this section unless the mode must be switched.

Switching can be made between the following two modes from an external device or PC CPU.



*The mode that can be switched from an external device
(Switching from the no-protocol mode to the dedicated protocol mode is impossible.)

The mode switching functions are as follows:

Mode Switching Function	Communication Status When Requesting Switching	Switching Procedure	Switching Requesting Method	
			Switching from External Device	Switching from PC CPU
Normal mode switching	When data communications is being executed	The mode is switched after completing data communications.	Writing to buffer memory address 119H (mode switching request, designated mode)	Writing to buffer memory address 119H (designated mode) The mode switching request flag (Y(n+1)9) is turned ON after writing.
	When data communications is not executed	The mode is switched as soon as mode switching is requested.		
Forced mode switching	When data communications is being executed	The on-going data communications is forced to terminate as soon as mode switching is requested, and the mode is switched.	Writing to buffer memory address 119H (forced mode switching request + designated mode)	
	When data communications is not executed	The mode is switched as soon as mode switching is requested.		

For writing to buffer memory address 119H, see Section 7.6.

POINT

The forced mode switching function switches the mode, irrespective of the data communications status. It, therefore, is useful to avoid communication errors and resume communications.

3.4.1 Precautions when mode switching

This section gives the precautions to take when data communication is continued after switching the AJ71UC24 mode in the middle of computer link operations.

(1) Settings between an external device and a PC CPU

Set the following items required to switch the mode between an external device and a PC CPU.

(a) Is the mode switched from an external device or PC CPU?

Mode Switching Method \ Current Mode	Mode Switchable from Dedicated Protocol (Formats 1 to 4)	Mode Switchable from No-Protocol Mode	Mode Switchable from Bidirectional Mode
Mode switching from external device	• No-protocol mode • Dedicated protocol mode (formats 1 to 4)	—	—
Mode switching from PC CPU	• No-protocol mode • Dedicated protocol mode (formats 1 to 4) • Bidirectional mode	• Dedicated protocol mode (formats 1 to 4) • Bidirectional mode	• Dedicated protocol mode (formats 1 to 4) • No-protocol mode

(b) At what intervals are modes switched for each mode switching pattern (those in the table in (a) above)?

(c) How is an interlock provided for all connected devices?

- Method and message used to notify all connected stations of mode switching.
- Method and message used to notify all connected stations that mode switching has been completed.
- Device number and data description when PC CPU word devices are used.

(2) Mode switching from an external device

(a) After switching the mode, an external device cannot be used to switch set data in the AJ71UC24 buffer memory's special applications area.
If the set data in the area must be changed after switching the mode, write necessary data from the PC CPU. For write timing, see Section 3.4.2.
When the set data is not changed from the PC CPU, communications is established using the default data in the special applications area.

(b) When both the RS-232C and the RS-422/485 are set to the no-protocol mode, the mode cannot be switched afterward by using an external device.

[This is because data cannot be written from the external device to the buffer memory's special applications area.]

POINT

Mitsubishi recommends using a PC CPU for mode switching.

(3) AJ71UC24 operations in mode switching

(a) Set back the data in the AJ71UC24 buffer memory's special applications area (addresses 100H to 11FH) to the default data.

(b) Clear the sent and received data stored in the AJ71UC24 buffer memory and the OS area in the middle of data communications in the no-protocol or bidirectional mode.

(c) When the mode is being switched, turn OFF all the I/O signals to the AJ71UC24.
Turn OFF the signals (Y) issued to the AJ71UC24 during mode switching before the mode is switched.

(d) To switch the mode in the middle of computer link operations, turn the AJ71UC24 READY signal (Xn7) ON, then OFF, and ON again. Change each set data in the AJ71UC24 buffer memory's special applications area (addresses 100H to 11FH) only at the rise of the READY signal in the PC CPU.

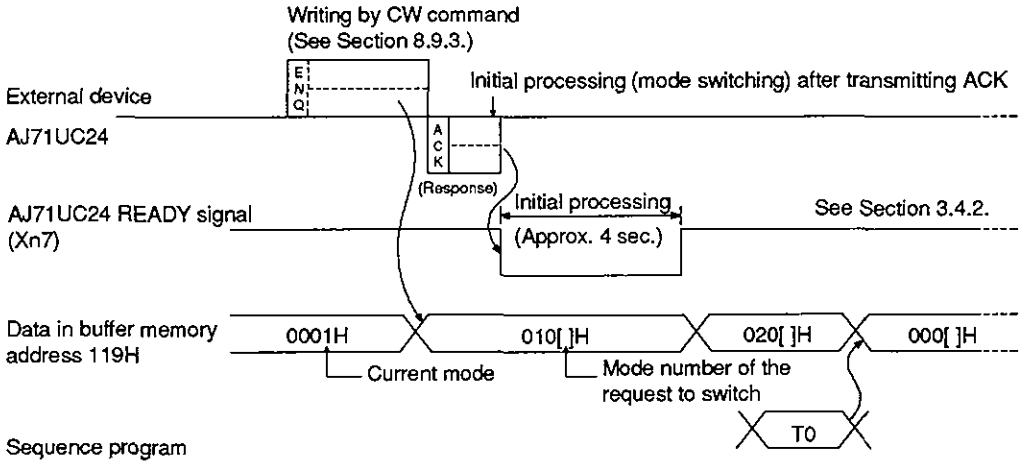
(4) Mode switching timing

(a) Mode switching from an external device

1) Switching from the dedicated protocol mode

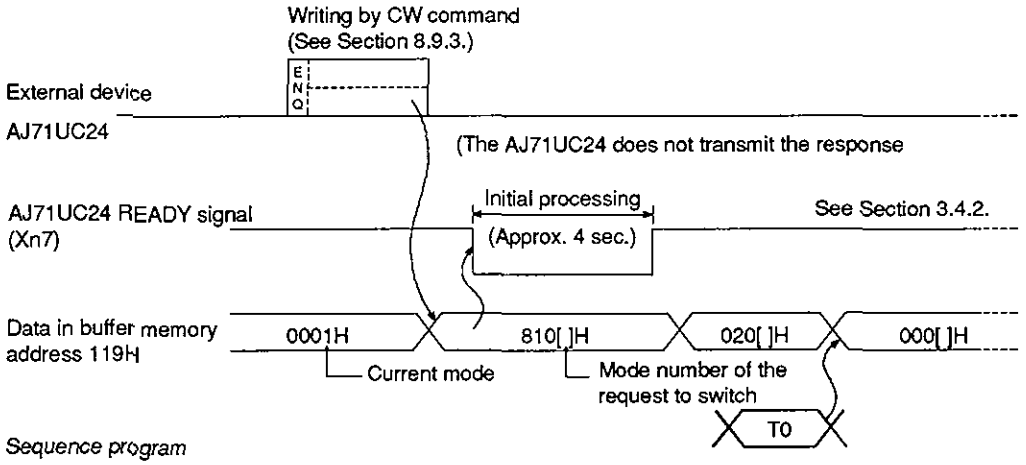
i) Normal mode switching

- With a mode switching request (writing 10[ ]H to buffer address 119H) in the middle of data communications, the mode will be switched (initial processing) after the data communications is completed (after transmitting data in area B (see Section 8.3)).



ii) Forced mode switching

- With a mode switching request (writing 810[ ]H to buffer address 119H) in the middle of data communications, the communications will be forced to terminate immediately to switch the mode (initial processing).



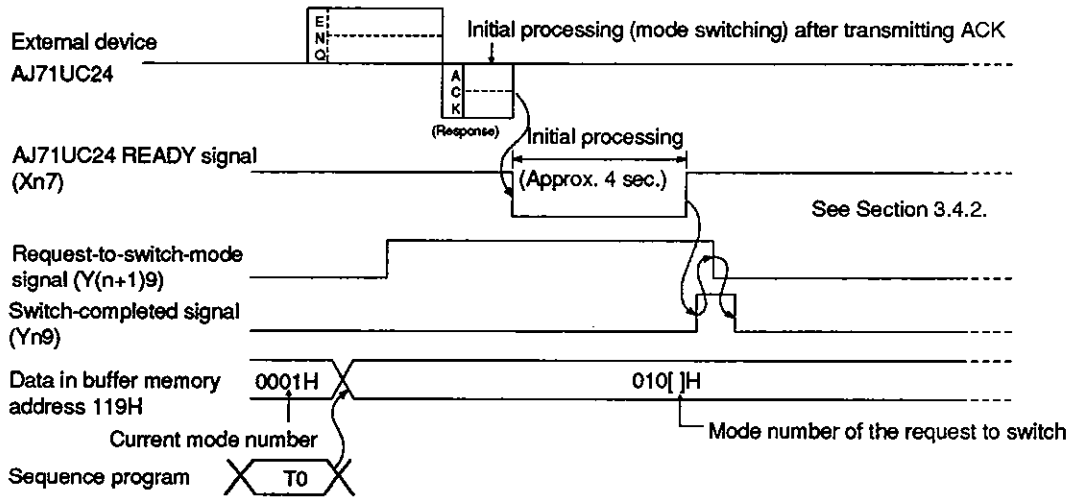
(b) Mode switching from a PC CPU

Mode switching from a PC CPU is possible in any mode.

1) Switching from the dedicated protocol mode

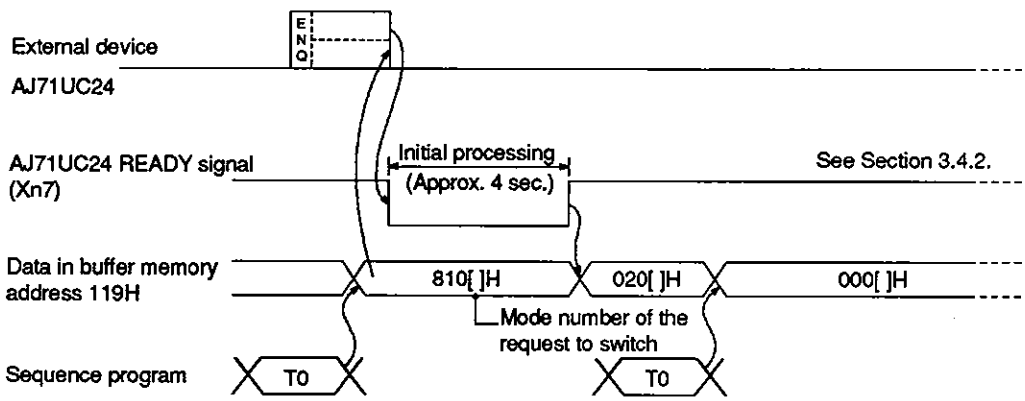
i) Normal mode switching

- With a request-to-switch-mode signal (Y(n+1)9 is turned ON) in the middle of data communications, the mode will be switched (initial processing) after the data communications is completed (after transmitting data in area B (see Section 8.3)).



ii) Forced mode switching

- With a mode switching request (writing 810[ ]H to buffer address 119H) in the middle of data communications, the communications will be forced to terminate immediately to switch the mode (initial processing).

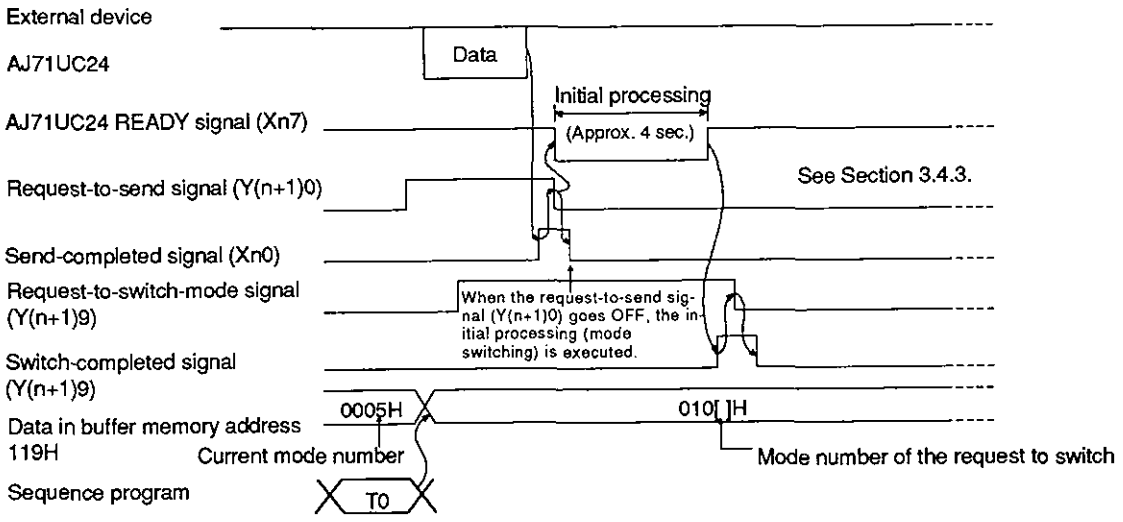


*It is not necessary to turn ON or OFF the request-to-switch-mode signal (Y(n+1)9). (The signal status will be ignored.)

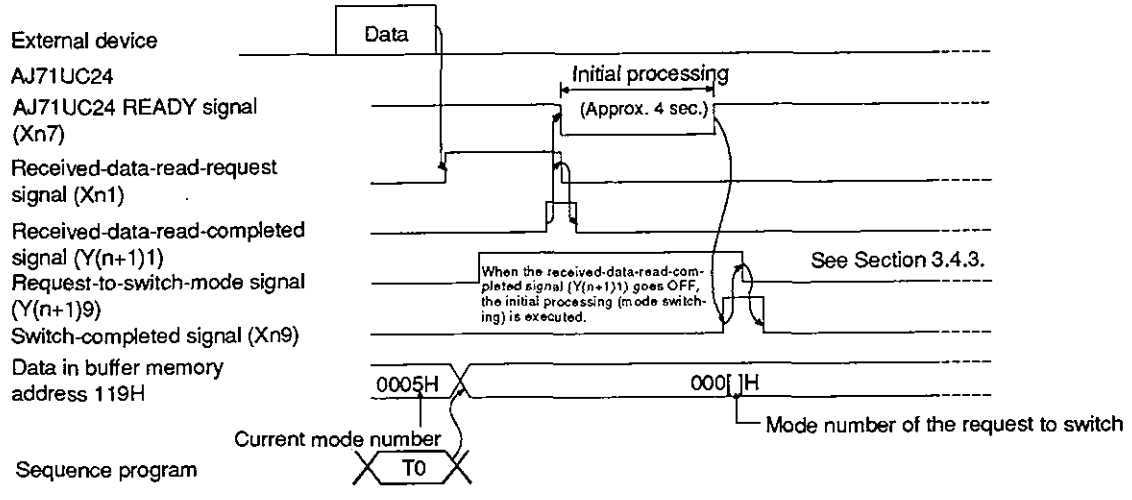
2) *Switching from the no-protocol or bidirectional mode*

i) Normal mode switching

- With a request-to-switch-mode signal (Y(n+1)9 is turned ON) when the AJ71UC24 request-to-send signal (Y(n+1)0) is ON, the mode will be switched (initial processing) after the data is transmitted (Xn0 is turned OFF).

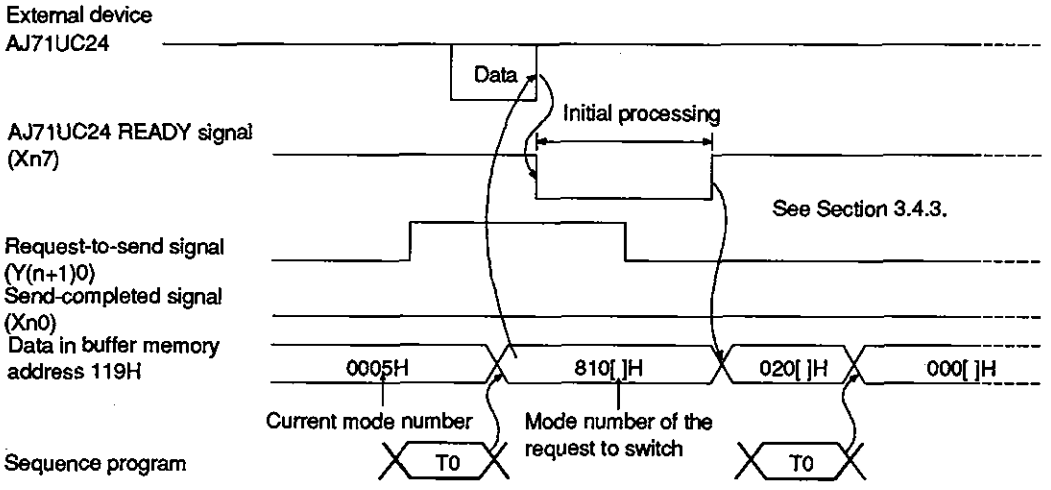


- With a request-to-switch-mode signal (Y(n+1)9 is turned ON) when the AJ71UC24 received-data-read-request signal (Xn1) is ON, the mode will be switched (initial processing) after the reading is completed (Y(n+1)1 is turned ON).

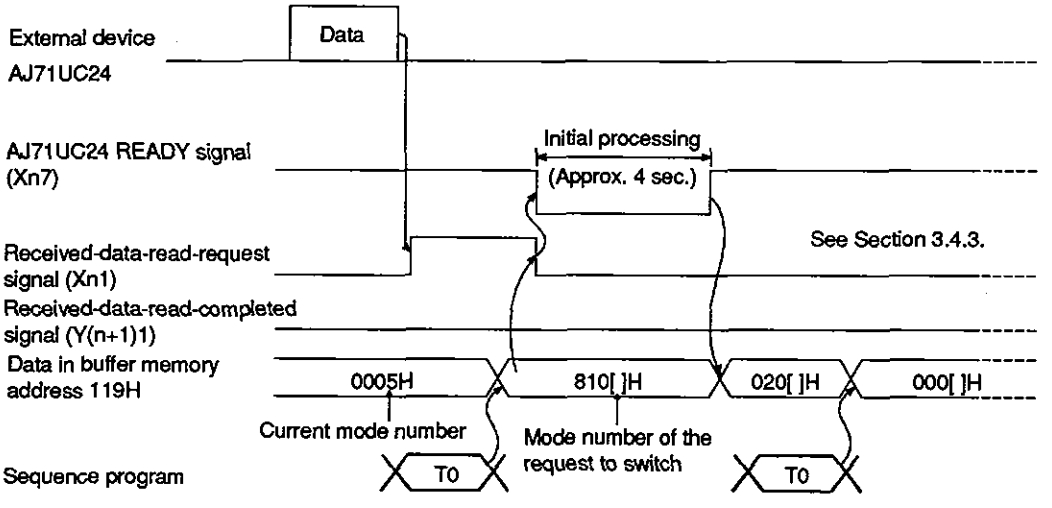


ii) Forced mode switching

- With a mode switching request (writing 810[ ]H to buffer memory address 119H) when the AJ71UC24 request-to-send signal (Y(n+1)0) is ON, the on-going data communications will be forced to terminate immediately to switch the mode (initial processing). (In this case, the send-completed signal (Xn0) will not be turned OFF. Turn OFF the request-to-send signal immediately.)



- With a mode switching request (writing 810[ ]H to buffer memory address 119H) when the AJ71UC24 received-data-read-request signal (Xn1) is ON, the received-data-read-request signal (Xn1) will be forced to turn OFF immediately to switch the mode (initial processing).

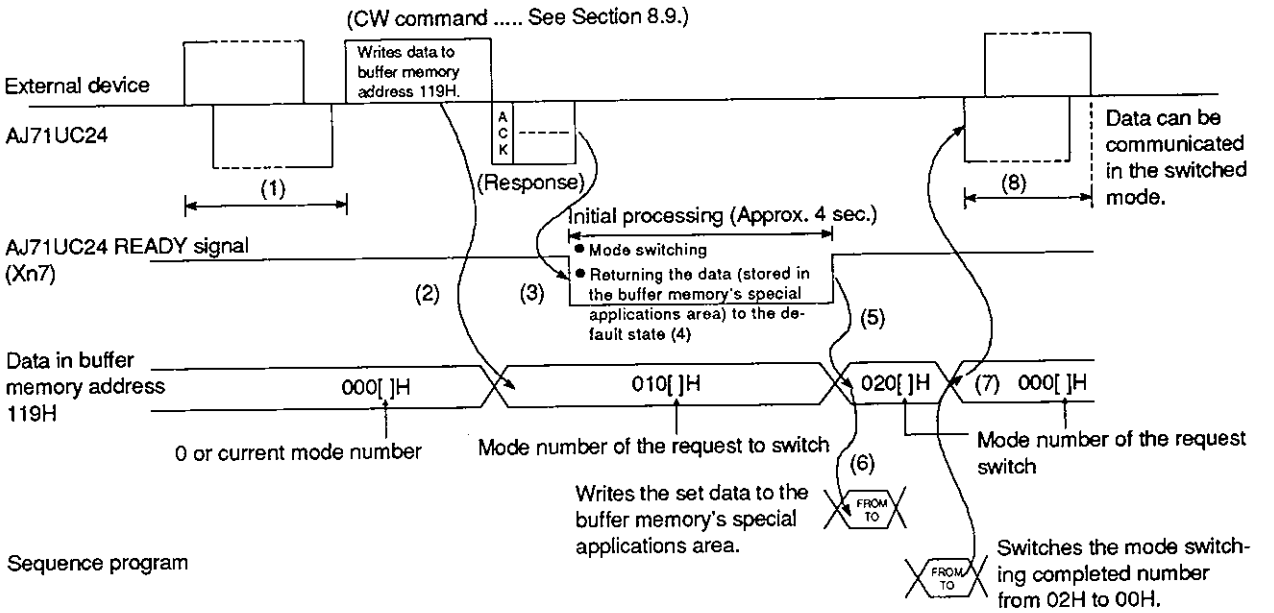


*It is not necessary to turn ON or OFF the request-to-switch-mode signal (Y(n+1)9). (The signal status will be ignored.)

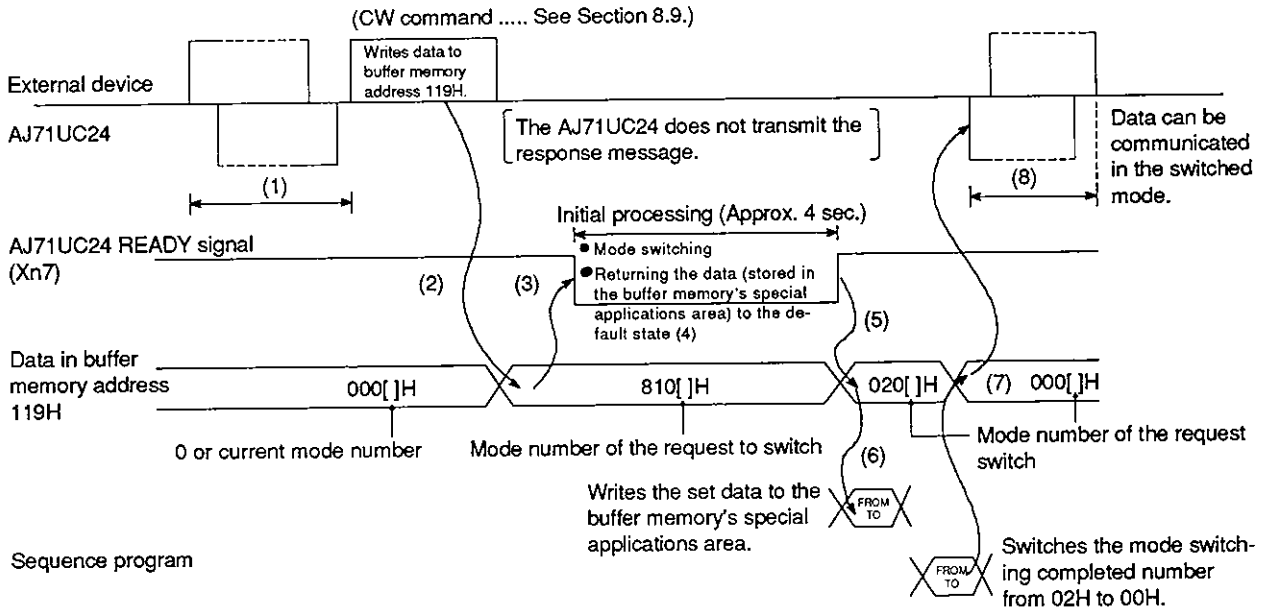
3.4.2 Procedure for switching the mode from an external device

Mode switching is executed via the interface of dedicated protocol (formats 1 to 4) using the "CW" command.
Before and after switching the mode, provide an interlock between sequence program operations and the mode switching operation (see Section 3.4.1(1)-(3)).
The mode switching procedure is shown below.

(1) Normal mode switching



(2) Forced mode switching

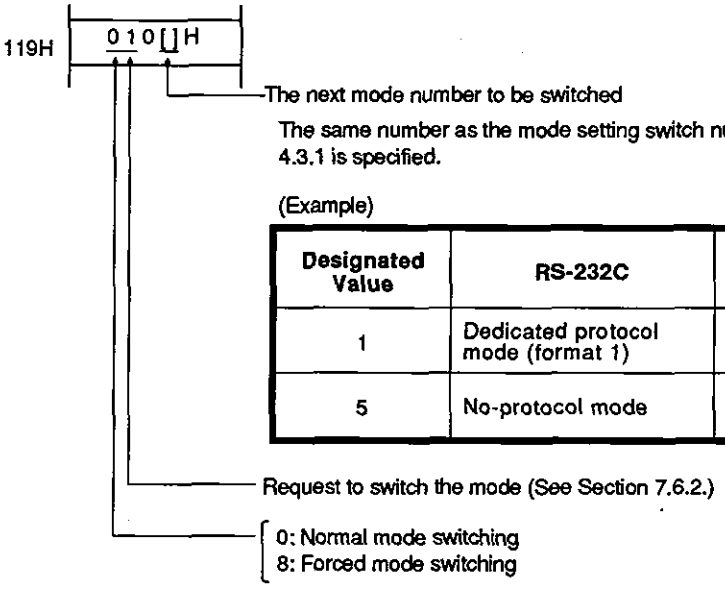


Described below are the operations or processing at the timings from (1) to (8) in the figures on the previous page. (The mode switching pattern concerned is affixed to each number.)

(1) (Normal/Forced) Before switching the mode, communicate the data to provide an interlock between the external device and the AJ71UC24 (sequence program).

[This is because the mode switching conditions must be set for all connected devices.]

(2) (Normal/Forced) By using the CW command, write a mode switching request and the next mode number from the external device to the AJ71UC24 buffer memory's mode switching designation area (address 119H).



(Example)

Designated Value	RS-232C	RS-422/485
1	Dedicated protocol mode (format 1)	No-protocol mode
5	No-protocol mode	Dedicated protocol mode (format 1)

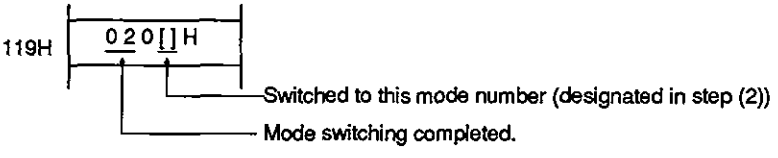
(3) (Normal) The AJ71UC24 completes the CW command execution normally and turns OFF its READY signal (Xn7) after transmitting the response message.

(Forced) On completion of writing data to buffer memory address 119H, the AJ71UC24 turns OFF its READY signal (Xn7).

(4) (Normal/Forced) The AJ71UC24 starts switching the mode, executing the following operations:

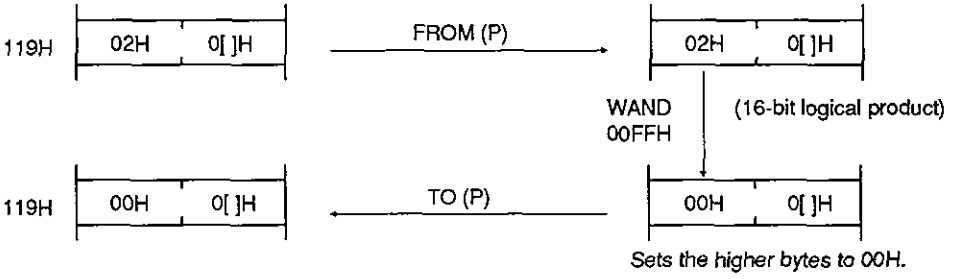
- AJ71UC24 initial processing
- Returning the data in the buffer memory's special applications area to the default state (except for the mode switching designation area (address 119H))
- Received data clear
- Mode switching
- Setting the switched mode number to the buffer memory's mode setting state storage area (address 118H)

(5) (Normal/Forced) After completing step (4), the AJ71UC24 turns ON its READY signal, overwriting 02H to the higher bytes in the buffer memory's mode switching designation area.



(6) (Normal/Forced) In response to the READY signal turned ON and the higher bytes changed to 02H in the mode switching designation area described in step (5), write the set data for data communications in the switched mode to the AJ71UC24 buffer memory's special applications area using the sequence program. However, writing the set data is unnecessary if data can be communicated using the default data in the special applications area.

(7) (Normal/Forced) Use a sequence program to read the data in the AJ71UC24 buffer memory's mode switching designation area and write 00H to the higher bytes in the area.



(8) (Normal/Forced) After switching the mode, communicate data to provide an interlock between an external device and the AJ71UC24 (sequence program).

[This operation notifies all connected devices that the data has been set in the buffer memory's special applications area and that data communications is enabled in the switched mode.]

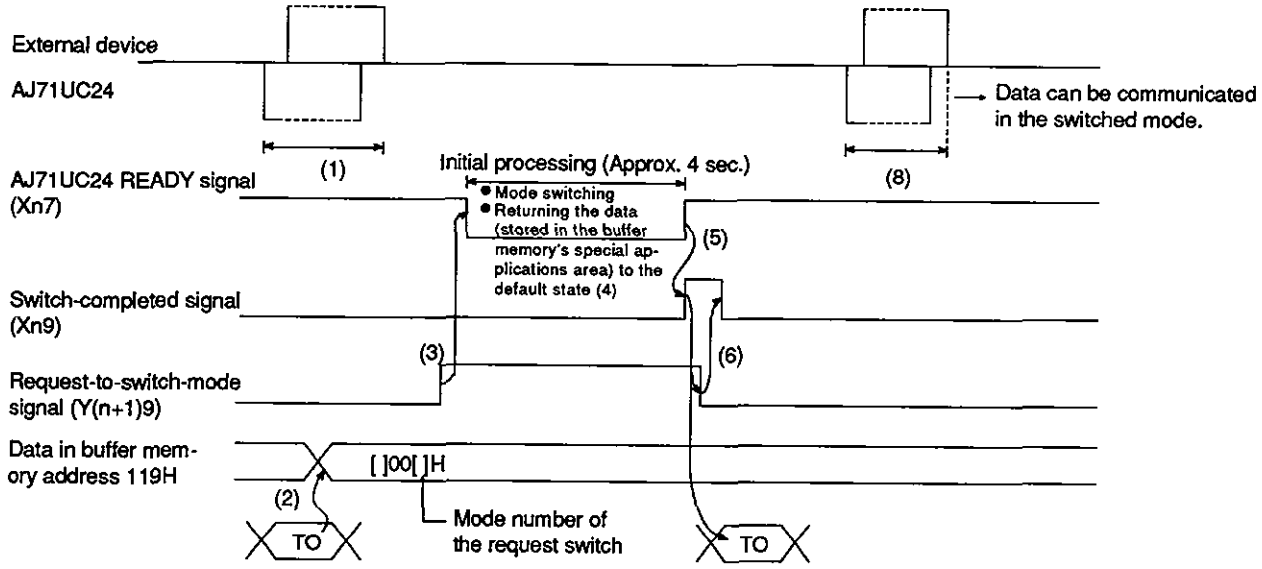
POINT

The AJ71UC24 mode can be switched even when the PC CPU is in the STOP state.

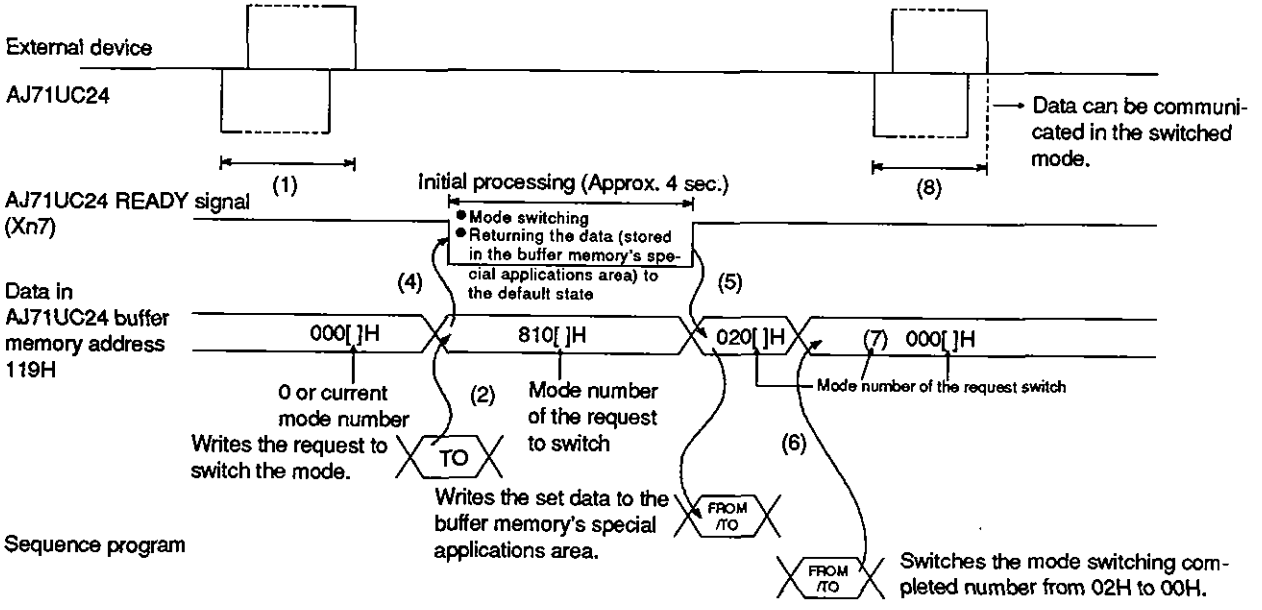
3.4.3 Procedure for switching the mode from a PC CPU

The mode is switched by using a FROM/TO instruction.
Before and after switching the mode, provide an interlock between the external devices connected to the AJ71UC24 via the RS-232 and the RS-422/485 respectively and the mode switching operation, as described in Section 3.4.1(1)-(3).
The mode switching procedure is shown below.

(1) Normal mode switching



(2) Forced mode switching

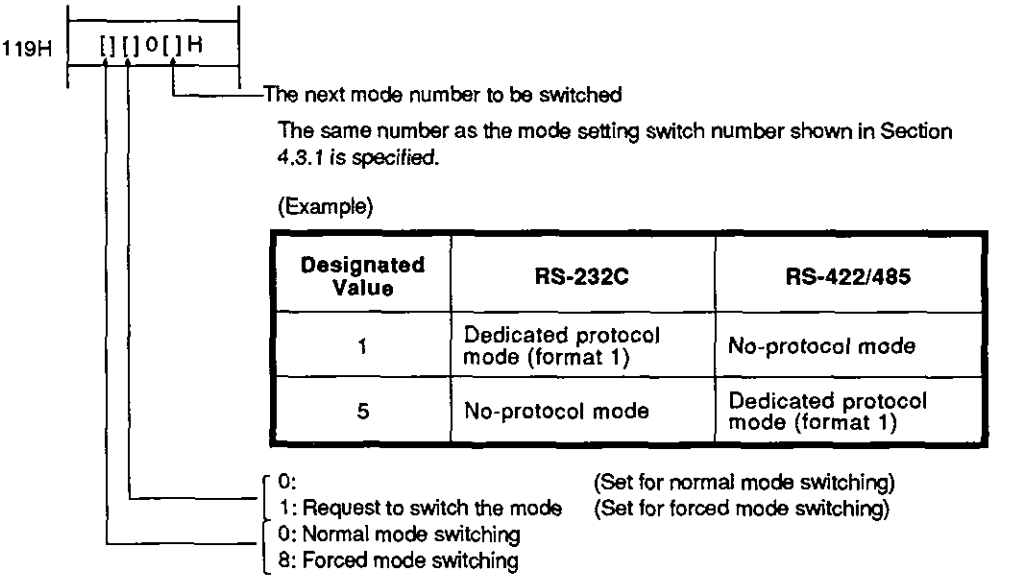


Described below are the operations or processing at the timings from (1) to (7) shown in the figures on the previous page.
(The mode switching pattern concerned is affixed to each number.)

(1) (Normal/Forced) Before switching the mode, communicate the data to provide an interlock between the external device and the AJ71UC24 (sequence program).

[This is because the mode switching conditions must be set for all connected devices.]

(2) (Normal/Forced) Write the next mode number from the sequence program to the AJ71UC24 buffer memory's mode switching designation area (address 119H).



Designated Value	RS-232C	RS-422/485
1	Dedicated protocol mode (format 1)	No-protocol mode
5	No-protocol mode	Dedicated protocol mode (format 1)

(3) (Normal) The request-to-switch-mode signal (Y(n+1)9) is turned OFF from the PC CPU.

(4) (Normal) The AJ71UC24 turns OFF its READY signal (Xn7), executing the following operations:

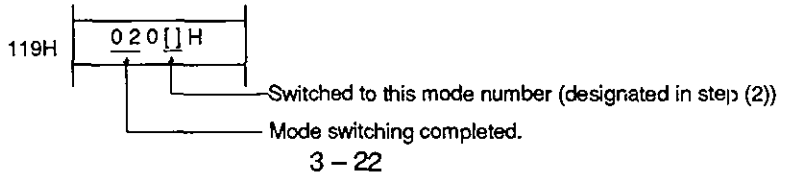
- AJ71UC24 mode switching
- Returning the data in the AJ71UC24 buffer memory's special applications area to the default state
  (except for the mode switching designation area (address 119H))

(Forced) As soon as writing data to buffer memory address 119H has been completed, the AJ71UC24 turns OFF its READY signal (Xn7), executing the following operations:

- AJ71UC24 mode switching
- Returning the data in the AJ71UC24 buffer memory's special applications area to the default state
  (except for the mode switching designation area (address 119H))

(5) (Normal) After completing step (4), the AJ71UC24 turns ON both its READY signal (Xn7) and the switch-completed signal (Xn9).

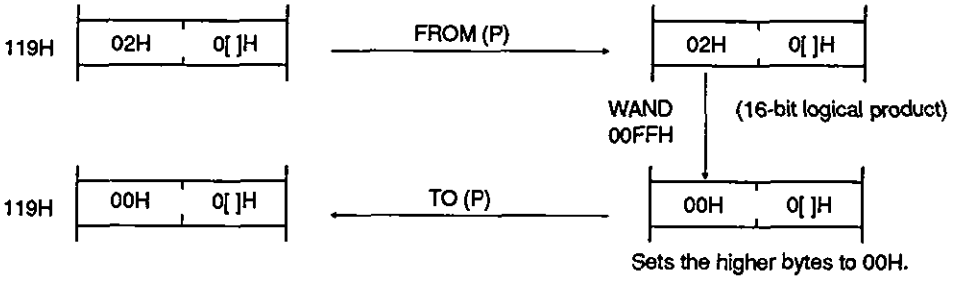
(Forced) After completing step (4), the AJ71UC24 turns ON its READY signal, overwriting 02H to the higher bytes in the buffer memory's mode switching designation area.



(6) (Normal) After the switch-completed and READY signals have been turned ON, the PC CPU turns OFF the request-to-switch-mode signal.
For data communications with the set data in the AJ71UC24 buffer memory's special applications area set to a value other than the default, write the necessary data from the PC CPU to the area at the rise of the AJ71UC24 READY signal (Xn7).

(Forced) In response to the READY signal turned ON and the higher bytes changed to 02H in the mode switching designation area described in step (5), write the set data for data communications in the switched mode to the AJ71UC24 buffer memory's special applications area using the sequence program.
However, writing the set data is unnecessary if data can be communicated using the default data in the special applications area.

(7) (Forced) Use the sequence program to read the data in the AJ71UC24 buffer memory's mode switching designation area and write 00H to the higher bytes.



(8) (Normal/Forced) After switching the mode, communicate data to provide an interlock between the external device and the AJ71UC24 (sequence program).
[This operation notifies all connected devices that the data has been set in the buffer memory's special applications area and that data communications is enabled in the switched mode.]

POINT

To change data other than that stored in the AJ71UC24 buffer memory's special applications area (address 119H) in mode switching, write new data at the rise of the AJ71UC24 READY signal (Xn7) triggered by mode switching.

3.5 Data Communications Transmission Control Function

The details are as described in the corresponding section in the AJ71C24-S8 User's Manual.

3.6 I/O Signals List for CPU

The I/O signals of the AJ71UC24 for the PC CPU are listed below. The numbers (n number) appended to X and Y are determined by the installing position of the AJ71UC24 and the number of I/O signals used by the I/O signal signals used by the I/O modules installed in front of the AJ71UC24. (Example: Xn0 → X0 when the AJ71UC24 is loaded in slot 0 of the main base unit)

(1) Input signals (AJ71UC24 → PC CPU)
There are 16 input signals: Xn0 to XnF are turned ON/OFF by the AJ71UC24.

Table 3.5 Input Signals List

<table>
<tr><th rowspan="2">Input Signal</th><th rowspan="2">Signal Name</th><th colspan="2">Mode</th><th rowspan="2">Description</th><th rowspan="2">Reference Sections</th></tr>
<tr><th>Dedicated protocol</th><th>No-protocol/ Bidirectional</th></tr>
<tr><td>Xn0</td><td>Send completed</td><td>—</td><td>o</td><td>Turns ON when the send from the AJ71UC24 to the external device is completed when Y(n+ 1)0 is turned ON.
Turns OFF when Y(n+ 1)0 is turned OFF.</td><td>9.2, 10.2</td></tr>
<tr><td>Xn1</td><td>Received data read request</td><td>—</td><td>o</td><td>Turns ON when the completed code, fixed length data, or designated data length is received from the external device.
Turns OFF when Y(n+ 1)1 is turned ON.</td><td>9.2, 10.2</td></tr>
<tr><td>Xn2</td><td>Global signal</td><td>o</td><td>—</td><td>Turns ON/OFF according to the message (factor number) when a global command is received from a computer.</td><td>8.13</td></tr>
<tr><td>Xn3</td><td>On-demand function operating</td><td>o</td><td>—</td><td>Turns ON when the on-demand transmission is executed according to the request from the sequence program. Turns OFF when the on-demand transmission is completed.</td><td>8.14</td></tr>
<tr><td>Xn4 to Xn6</td><td>AJ71UC24 message sequence state</td><td>o</td><td>—</td><td>(1) Set values "1" to "8" of the mode setting switches (see Section 4.3.1) indicating the state of communications between the computer connected to the interface on the dedicated protocol side and the AJ71UC24.
Set values "A" to "D" of the mode setting switches indicating the state of communications between the computer connected to the interface on the main channel side (set with SW11, a transmission specification setting switch, see Section 4.3.2) and the AJ71UC24.
(2) Used by a sequence program to check communications status, etc.
<table>
<tr><th>Value</th><th>Xn6</th><th>Xn5</th><th>Xn4</th><th>Message Sequence State</th></tr>
<tr><td>0</td><td>OFF</td><td>OFF</td><td>OFF</td><td>AJ71UC24 initializing after power ON or OFF using protocol 1 to 4</td></tr>
<tr><td>1</td><td>OFF</td><td>OFF</td><td>ON</td><td>Waiting for ENQ</td></tr>
<tr><td>2</td><td>OFF</td><td>ON</td><td>OFF</td><td>Received ENQ</td></tr>
<tr><td>3</td><td>OFF</td><td>ON</td><td>ON</td><td>Received station number (self)</td></tr>
<tr><td>4</td><td>ON</td><td>OFF</td><td>OFF</td><td>Waiting for response from PC after receiving all data</td></tr>
<tr><td>5</td><td>ON</td><td>OFF</td><td>ON</td><td>Waiting for message</td></tr>
<tr><td>6</td><td>ON</td><td>ON</td><td>OFF</td><td>Unused</td></tr>
</table></td><td>—</td></tr>
</table>

Input Signal	Signal Name	Mode		Description	Reference Sections
		Dedicated protocol	No-protocol/ Bidirectional		
Xn7	AJ71UC24 READY signal	o	o	(1) Turns ON when the AJ71UC24 becomes READY after the PC CPU is enabled. (Turns ON a few seconds after the power is turned ON.) Turns OFF when an error (which discontinues the AJ71UC24's operation) occurs. (2) Used for the READY communications signal when the no-protocol mode, bidirectional mode, or the on-demand function of the dedicated protocol is used.	—
Xn8	—	—	—	Unavailable	—
Xn9	Mode change completed	o	o	Goes ON when completing the AJ71UC24 mode change turns ON the Y(n+ 1)9	3.4
XnA to XnC	—	—	—	Unavailable	—
XnD	Watch dog timer error	o	o	Turns ON when the AJ71UC24 watch dog timer error occurs. Remains OFF during normal operation.	11.2
XnE XnF	—	—	—	Unavailable	—

POINT

Y(Yn0 to YnF) corresponding to Xn0 to XnF may be used as internal relays.

(2) Output signals (PC CPU → AJ71UC24)

There are 16 output signals: Y(n+ 1)0 to Y(n+ 1)F are turned ON/OFF by the AJ71UC24.

Table 3.6 Output Signals List

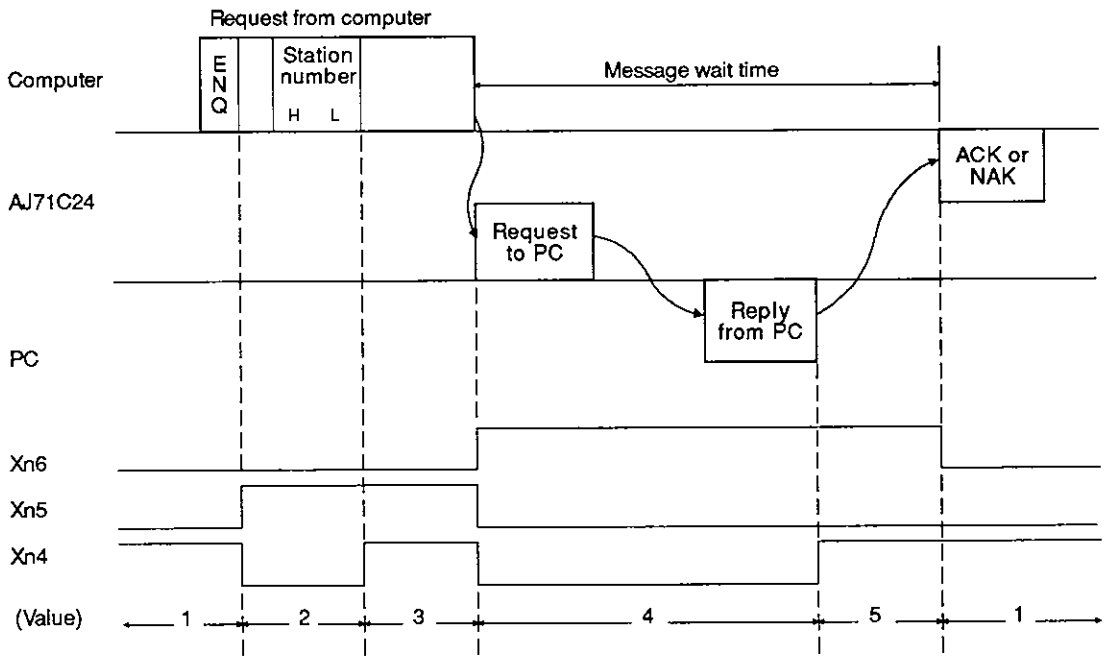
Output Signal	Signal Name	Mode		Description	Reference Sections
		Dedicated protocol	No-protocol/ Bidirectional		
Y(n+ 1) 0	Send request	–	o	When this signal is turned ON by the sequence program in the no-protocol mode/bidirectional mode, data written to the buffer memory is transmitted from the AJ71UC24 to an external device. (After Xn0 is turned ON, Y(n+ 1)0 is turned OFF.	9.2, 10.2
Y(n+ 1)1	Received data read completed	–	o	This signal turns ON in the no-protocol mode/bidirectional mode, when the PC CPU has completed reading the data received from an external device. This data is stored in the AJ71UC24 buffer memory. (After Xn1 is turned OFF, Y(n+ 1)1 is turned OFF.	9.2, 10.2
Y(n+ 1) 2 to Y(n+ 1) 8	–	–	–	Unavailable	–
Y(n+ 1) 9	Mode change request	o	o	Turning this ON (using the sequence program) changes the AJ71UC24 mode, which executes the initial processing. Goes OFF after turning ON Xn9.	3.4
Y(n+ 1) A to Y(n+ 1) F	–	–	–	Unavailable	–

IMPORTANT

Y(n+ 1)2 to Y(n+ 1)F are reserved for system use only. AJ71UC24 functions cannot be guaranteed if these signals are turned ON or OFF by a sequence program.

REMARK

Example: Use of input signals Xn4 to Xn6.



3.7 Buffer Memory Applications and Allocation

The term "buffer memory" used in this manual refers to a memory area of an AJ71UC24 used to store the control and communications data which is transmitted between an external device (e.g., a computer) and a PC CPU.

The buffer memory can be accessed from the sequence program by using the FROM/TO instruction.

The buffer memory can be accessed from an external device by using the buffer memory read/write command (CR, CW) with dedicated protocols 1 to 4.

(1) Buffer memory applications

There are two types of buffer memory area. One area may be used freely by the user, but the other area has a special application.

(a) User area

There are four applications of the user area, which can be categorized as follows.

1) Data receive area in no-protocol mode/bidirectional mode

This area stores data transmitted from an external device in the no-protocol mode or bidirectional mode.

2) No-protocol mode/bidirectional mode data send area

This area stores data from the PC CPU to be transmitted to an external device.

3) On-demand data storage area

This area stores send data to be transmitted from the sequence program to an external device using the on-demand function.

4) Area when using buffer memory read/write commands

This area stores data when communication is made using protocols 1 to 4 for buffer memory read/write commands (CR,CW).

(b) Special applications area

The applications of this memory area are fixed. They are used to determine the data communications format and to change the allocation of the memory area for section (a) above.

When the power is turned ON, the PC CPU is reset or switching the mode, default values are written to this special applications area.

Default values can be changed to suit the purposes and applications of data transmission and the specifications of the external device. Section 7 gives details.

(2) Buffer memory allocation

The buffer memory consists of 16-bit addresses. The buffer memory has no back-up battery.

The buffer memory address names and values for each address are listed in the following table.

IMPORTANT

Buffer memory addresses 10EH is reserved for system use only. Data written to this area will prevent correct operation of the AJ71UC24.

The table in the next page shows the contents of the buffer memory allocation.

The memory areas which are used with the no-protocol mode or the bidirectional mode are listed as those to be used with the no-protocol mode.

The memory areas function the same way in either mode. When the bidirectional mode is required, see the following table, changing "no-protocol" to "bidirectional".

Table 3.7 Buffer Memory

Addresses	Buffer Memory Address Names	Default Values	Dedicated Protocol	No-Protocol	Bidirectional	(Reference Sections)
0H 1H to 7FH 80H 81H to FFH	User area (256 words) / Area for default: No-protocol send data length storage area	No-protocol send area: 0	o *3	o	o	.... 8.14 9 10
	No-protocol send buffer memory area (Send data storage area)			o	o	
	No-protocol received data length storage area.	No-protocol receive area: 0		o	o	
	No-protocol receive buffer memory area (Received data storage area)			o	o	
100H•	Area to specify receive completed code in no-protocol mode	0D0AH (CR, LF)	—	o	—	..... 7.4.1
101H	Error LED display OFF state storage area	0	Δ	Δ	Δ	..... 7.3.1
102H	Error LED turn OFF request area	0	o	o	o	..... 7.3.2
103H•	Area to specify word or byte units in no-protocol mode	0 (words)	o *1	o	o	..... 7.4.3
104H•	Area to specify head address of send buffer memory for no-protocol mode	0	—	o	o	..... 7.4.4
105H•	Area to specify send buffer size for no-protocol mode	80H	—	o	o	
106H•	Area to specify head address of receive buffer memory for no-protocol mode	80H	—	o	o	..... 7.4.5
107H•	Area to specify receive buffer size for no-protocol mode	80H	—	o	o	
108H•	Area to specify receive completion 1 on data length in no-protocol mode	127 (words)	—	o	—	..... 7.4.2
109H	Area to specify head address of on-demand buffer memory	0	o	—	—	..... 8.14
10AH	Area to specify on-demand buffer size	0	o	—	—	
10BH•	Area to specify RS-232C CD terminal check	—	o	o	o	..... 7.1
10CH	Storage area for on-demand errors	0	Δ	—	—	..... 8.14
10DH	Receive data clear request area for no-protocol mode	0	—	o	—	..... 9.5
10EH	System area (unavailable)	—	—	—	—	
10FH•	RS-232C communications mode setting area	0 (Full-duplex transmission)	o	o	o	
110H•	Simultaneous send priority/non-priority setting area*2	0 (Priority)	o	o	o	..... 7.2
111H•	Send method setting area when transmission is resumed*2	0 (No retransmission)	o	o	o	
112H•	Bidirectional mode setting area	0 (No-protocol mode)	—	—	o	..... 7.5
113H•	Time-out check time setting area	0 (Infinite)	—	—	o	
114H•	Simultaneous transmission data valid/invalid setting area	0 (Data valid)	—	—	o	
115H•	Check sum enable/disable setting area	0 (Check sum enabled)	—	—	o	
116H	Data send error storage area	0	—	—	Δ	..... 10.2
117H	Data receive error storage area	0	—	—	Δ	

Addresses	Buffer Memory Address Names	Default Values	Dedicated Protocol	No-Protocol	Bidirectional	(Reference Sections)
118H	Mode setting state storage area	0 (mode 0)	Δ	Δ	Δ	..... 7.6.1
119H	Mode change specification area	0 (no switching) *5	o	o	o	..... 7.6.2
11AH•	Transmission control specification area (DTR/DSR control and DC code control)	0 (DTR/DSR control)	o	o	o	..... 7.7
11BH•	DC1/DC3 control code specification area	1311H	o	o	o	
11CH•	DC2/DC4 control code specification area	1412H	o	o	o	
11DH	RS-232C signal data storage area	—	Δ	Δ	Δ	..... 7.8
11EH•	Mode setting switch/station number setting switch status storage area	—	Δ	Δ	Δ	..... 7.9
11FH•	Transmission specification setting switch status storage area	—	Δ	Δ	Δ	..... 7.10
120H to 7FFH	User area (1760 words)	0	o *3	o *3	o *3	.... 8.14 9 10

*4

The o, Δ, and — symbols in the table indicate the following:

o: PC CPUs and computers can read/write from/to this area.

Δ: PC CPUs and computers can only read from this area.

—: PC CPUs and computers do not need to read/write from/to this area.

*1: The unit of the transmission (send/receive) data in the no-protocol mode or bidirectional mode or of the send data when the on-demand function of the dedicated protocol is used.

*2: Set this when the RS-232C interface is set to half-duplex communications.

*3: Areas should be allocated so that they do not overlap with each other when (a) data is transmitted in the no-protocol mode or bidirectional mode, or (b) when more than one function of data transmission using the on-demand function of the dedicated protocol is used.

*4: Change the default values marked by the dot symbol (•) attached to the right of the address only when the READY signal of the AJ71UC24 is turned ON after the power is turned ON or the PC CPU is reset.

Or change the default values when the higher bytes of the buffer's mode switching designation area (address 119H) change into 02H after the AJ71UC24 READY signal is turned ON by switching the mode of the AJ71UC24.

*5 0 is stored before switching the mode.

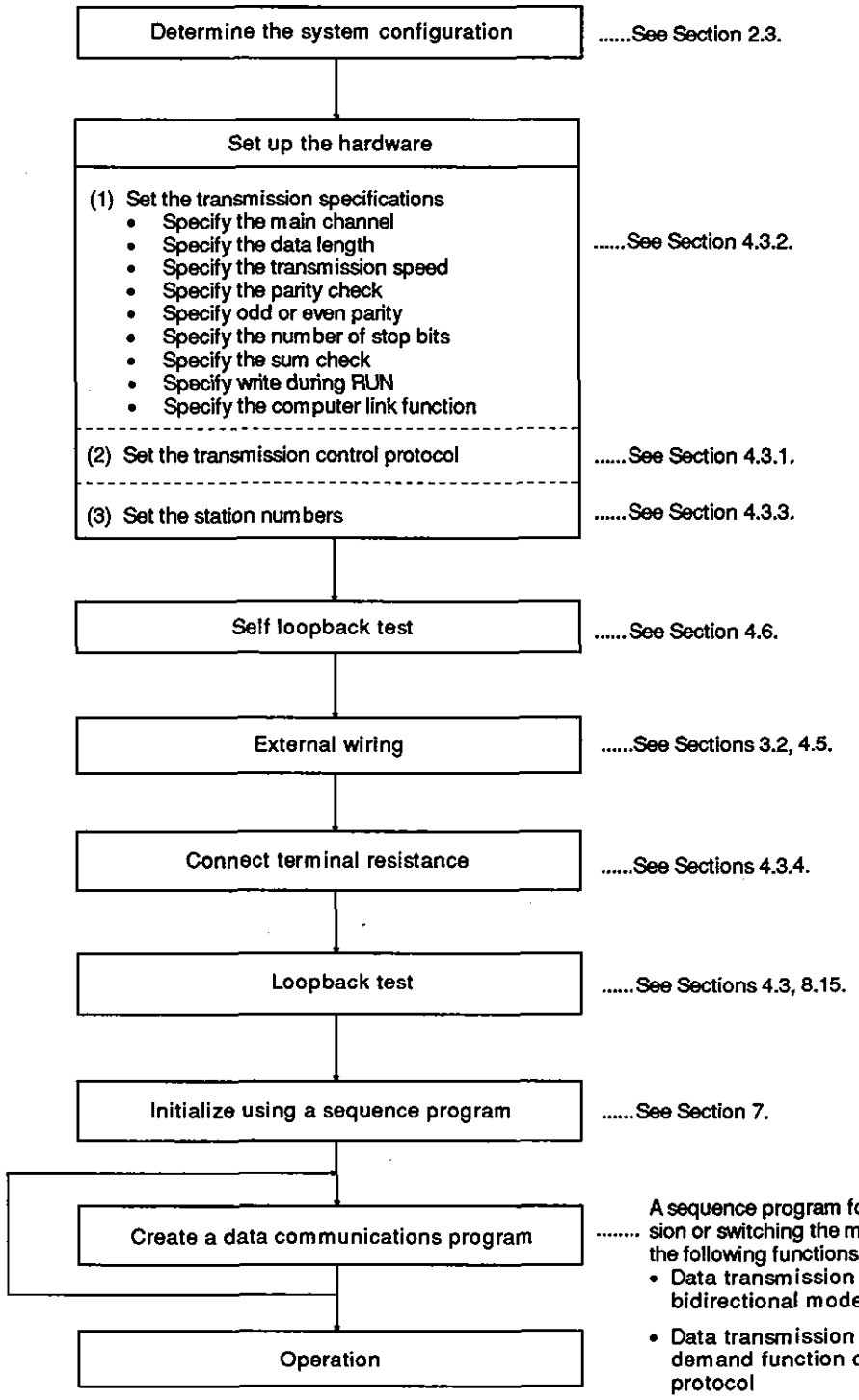
The values (1H to DH) of the mode number that correspond to the current mode are stored after switching the mode.

1H to DH correspond to the set values (1 to D) of the mode setting switch (see Section 4.3.1).

4. SETTINGS AND PROCEDURES BEFORE OPERATION

4.1 Settings and Procedures before Operation

The settings and procedures which have to be done before a system using the AJ71UC24 can be started are described below.



REMARK

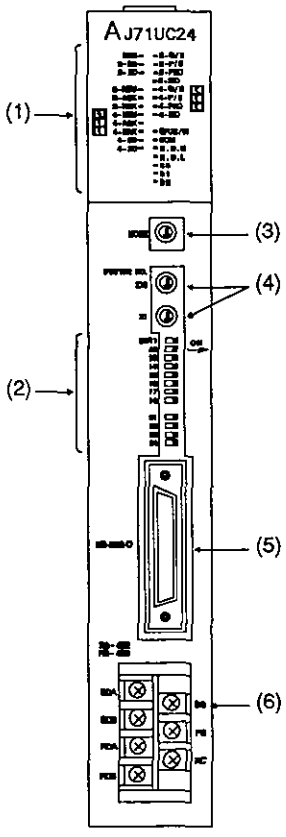
Appendix 10 contains the form sheet for recording the setting values of the AJ71UC24.

4.2 Nomenclature and LED Signals and Dispalys

This section describes the nomenclature and LED signals and displays of the AJ71UC24.

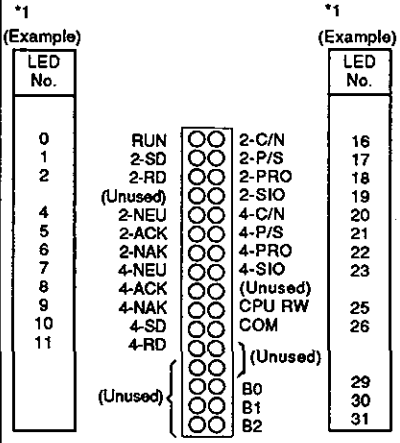
4.2.1 Nomenclature

The following figure and table show the nomenclature of the AJ71UC24.



No.	Name	Description	Reference Sections
(1)	Indicator LEDs	Display the operating status, link communications underway and alarms. What the ON/OFF status indicates depends on each indicator LED.	Section 4.2.2
(2)	Transmission specification setting switches	Used to select the RS-232C or RS-422/485, data bit, parity presence/absence, stop bit, sum check enable/disable, etc. (All switches factory-set to OFF)	Section 4.3.2
(3)	Mode setting switch	Switch for selecting transmission control protocol and RS-232C and RS-422/485 control procedure (Factory-set to F)	Section 4.3.1
(4)	Station number setting switches	Switches to set the AJ71UC24 station number in a computer link system. The station number can be set to any unregistered value between 0 and 31. (Factory-set to 0)	Section 4.3.3
(5)	RS-232C connector	RS-232C connector for linking an AJ71UC24 with an external device (computer, etc.)	Sections 3.2.2 and 4.5.2
(6)	RS-422/485 interface	RS-422/485 interface for linking an AJ71UC24 with an external device (computer, etc.)	Sections 3.2.3, 4.5.3 and 4.5.4

4.2.2 LED signals and displays

LED Area Details	LED No.	LED	Meaning of LED Display	LED ON	LED OFF	Initial Status of LED
	0	RUN	Normal run	Normal	Error	ON
	1	2-SD	RS-232C transmitting	Flashes during data transmission		OFF
	2	2-RD	RS-232C receiving	Flashes during data receive		OFF
	4	2-NEU	RS-232C neutral	Transmission sequence initial state (waiting for ENQ)	ENQ received	*2
	5	2-ACK	RS-232C ACK	After sending ACK	After sending NAK	OFF
	6	2-NAK	RS-232C NAK	After sending NAK	After sending ACK	OFF
	7	4-NEU	RS-422/485 neutral	Transmission sequence initial state (waiting for ENQ)	ENQ received	*2
	8	4-ACK	RS-422/485 ACK	After sending ACK	After sending NAK	OFF
	9	4-NAK	RS-422/485 NAK	After sending NAK	After sending ACK	OFF
	10	4-SD	RS-422/485 transmission status	Flashes during data transmission		OFF
	11	4-RD	RS-422/485 received data status	Flashes during data receive		OFF
	16	2-C/N	Result of RS-232C and PC CPU communications	See (4) in the next page	Normal	OFF
	17	2-P/S	RS-232C parity/sum check errpr	Parity/sum check error	Normal	OFF
	18	2-PRO	RS-232C protocol error	Communica-tions protocol error	Normal	OFF
	19	2-SIO	RS-232C SIO error	Overrun, framing error	Normal	OFF
	20	4-C/N	Result of RS-422/485 and PC CPU communications	Parity/sum check error	See(4) in the next page	OFF
	21	4-P/S	RS-422/485 parity/sum check error	Parity/sum check error	Normal	OFF
	22	4-PRO	RS-422/485 protocol error	Communica-tion protocol error	Normal	OFF
	23	4-SIO	RS-422/485 SIO error	Overrun, framing error	Normal	OFF
	25	CPUR/W	Communications with PC CPU	Flashes during communications with PC CPU (ON at no communications)		ON
	26	COM	Select function	Computer link	Multidrop link	*3

LED No.	LED	Meaning of LED Display	Status of LED							Initial Status of LED
		Baud rate (BPS)	300	600	1200	2400	4800	9600	19200	
29	B0	Baud rate status	OFF	ON	OFF	ON	OFF	ON	OFF	*4
30	B1		OFF	OFF	ON	ON	OFF	OFF	ON	
31	B2		OFF	OFF	OFF	OFF	ON	ON	ON	

*1 : Because these LED numbers are examples, they are not actually printed out.
*2, *3 and *4 vary according to the transmission specifications switch setting as shown in the following tables.

Mode Setting / Main Channel Setting		1 to 4	5 to 8	9	A to D		F
LED No.	LED	RS-232C RS-422 /485	RS-232C RS-422 /485	RS-232C RS-422 /485	RS-232C	RS-422 /485	RS232C RS-422 /485
4	2-NEU	ON	OFF	OFF	ON	OFF	OFF
7	4-NEU	OFF	ON	OFF	OFF	ON	OFF

(1) LEDs 2-C/N to 4-SIO (LED Nos.16 to 23) above light when an error occurs. (Sections 3.5.2 and 3.5.3 also give details about 2-SIO and 4-SIO.)

The ON/OFF status of the LED Nos. 16 to 23 are stored in the buffer memory at address 101H. The status can be read using the PC CPU instruction which permits checking by a sequence program.

(Section 11 gives details about processing when an error is indicated.)

(2) After any LED 2-C/N to 4-SIO (LED Nos. 16 to 23) is ON, they remain ON even when the cause of the error is eliminated.

It is necessary to send a turn-off request to address 102H of the buffer memory using the sequence program TO instruction to turn OFF the LED.

(3) LEDs RUN to 4-RD (LED Nos. 0 to 11) and CPU R/W (LED No.25) above light corresponding to the relevant status.

(4) LEDs 2-C/N and 4-C/N (LED Nos. 16 and 20) above light in the following circumstances:

(a) When the AJ71UC24 attempts to make an illegal access while the PC CPU is running (a write during program execution, for example).

(b) During abnormal PC CPU access.

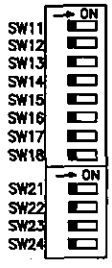
(5) The "initial state" column indicates the status when the power is turned ON or the PC CPU is reset.

4.3 Settings

4.3.1 Setting the dedicated protocol, no-protocol mode, or bidirectional mode

The details are as described in the corresponding section in the AJ71C24-S8 User's Manual.

4.3.2 Setting of transmission specifications, main channels and terminal resistance

Setting of Switches	Setting Switches	Setting Items	Position of Setting Switch		Notes
			ON	OFF	
	SW11	Main channel settings	RS-422/485	RS-232C	Valid for modes A to D
	SW12	Data length	8 bits	7 bits	–
	SW13 SW14 SW15	Baud rate Transmission speed setting	300: OFF / OFF / OFF 600: ON / OFF / OFF 1200: OFF / ON / OFF 2400: ON / ON / OFF 4800: OFF / OFF / ON 9600: ON / OFF / ON 19200: OFF / ON / ON Unusable: ON / ON / ON		–
	SW16	Parity check	Enabled	Disabled	–
	SW17	Parity setting	Even	Odd	Valid only when parity check "enabled" is selected
	SW18	Stop bit	2 bits	1 bit	–
	SW21	Sum check	Enabled	Disabled	–
	SW22	Write during RUN	Enabled	Disabled	–
	SW23	Computer link/ Multidrop link selection	Computer link	Multidrop link	Must be set to ON
	SW24	Unusable	–	–	–

(1) Main channel

The main channel in the above table refers to the interface to which the computer is connected. The main channel setting is valid only for modes A to D.

In other modes, the setting switch may be in the ON or OFF position.

(Section 4.5.4 gives the setting examples for different system configurations.)

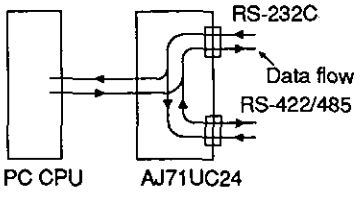
Setting the main channel defines data flow as shown below:

Data received through the main channel is automatically transmitted through the sub channel.

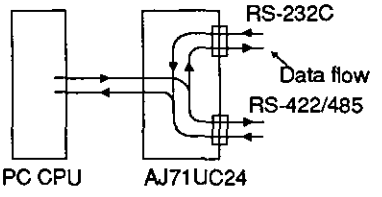
Data received through the sub channel is automatically transmitted through the main channel.

When the mode switch is set to "A" to "D", only the processing request commands, transmitted from other stations and received through the main channel of the self, are valid with the set mode.

The AJ71UC24 executes the requested processing and transmits the result through the main channel.



RS-232C is set to the main channel



RS-422/485 is set to the main channel

(2) Transmission specifications

The RS-232C and RS-422/485 use the same transmission specifications. They cannot operate with two different transmission specifications settings.

Do not set the "unusable" baud rate setting (SW13, 14, and 15 ON).

If these switches are set, the RUN indicator LED (LED No. 0) is turned OFF and operation is not possible.

(3) Sum check

Set whether the sum check code is added or not added to the end of the message, when the computer link operates with the dedicated protocol.

Sections 8.4.1 to 8.4.4 and 8.4.5 (7) give the message structure and sum check code when the sum check setting is "Enabled".

(4) Write during RUN

Set whether a processing requested by the external device is executed or not executed by the PC CPU in the RUN state when the computer link operates with the dedicated protocol.

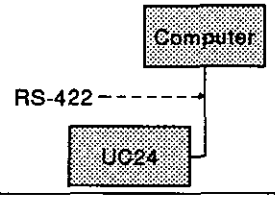
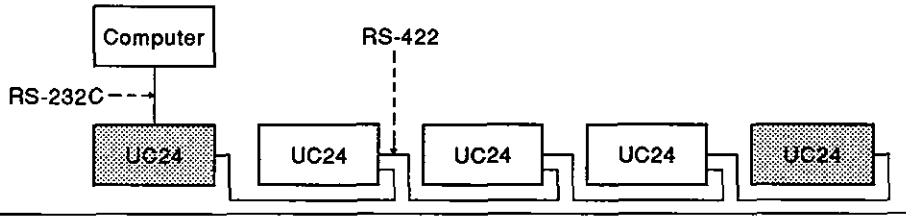
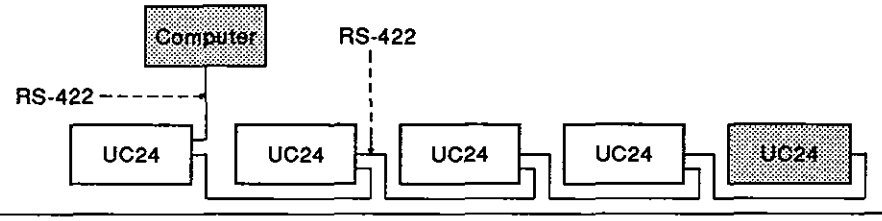
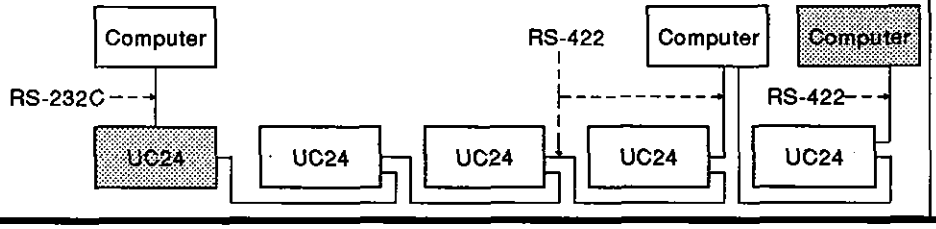
Section 3.3.1 gives the functions available with this setting.

4.3.3 Station number setting

The details are as described in the corresponding section in the AJ71C24-S8 User's Manual.

4.3.4 Terminal resistance connections

For communications via the RS-422/485 interface, connect a terminal resistance to both ends of the connected stations.
Connect a 330 Ω, 1/2 W resistance for communications via the RS-422, or a 110 Ω, 1/2 W resistance for communications via the RS-485 to the stations indicated by hatching in the connection examples below.
(For details of computer settings, see APPENDIX 6.)

System Configuration Ratio Between Computer and PC CPU	System Configuration Example	Terminal Resistance Connecting Terminal
1 : 1		Across SDA - SDB and across RDA - RDB
1 : n		
		
m : n		*1 Across SDA - SDB or across RDA - RDB

*1 Connect the terminal resistance to the same terminals for the system configurations of 2 : 1 and 2 : n ratios.

4.4 Loading and Installation

4.4.1 Handling instructions

Except for the screw tightening torque range specified below, follow the instructions given in the corresponding section in the AJ71C24-S8 User's Manual. (Only instruction (4) in the AJ71C24-S8 User's Manual is changed as follows.)

(4) Tighten the module mounting screws (optional) and the terminal screws with the torques specified in the following table.

Screw	Tightening Torque Range N·cm (kg·cm) [lb·inch]
RS-422/485 terminal block terminal screws (M3.5)	58 to 88 (6 to 9) [5.2 to 7.79]
Module mounting screws (optional) (M4)	78 to 118 (8 to 12) [6.93 to 10.39]

4.4.2 Installation environment

The environmental conditions are as specified in the corresponding section in the AJ71C24-S8 User's Manual.

4.5 External Wiring

4.5.1 Precautions during wiring

The precautions are as described in the corresponding section in the AJ71C24-S8 User's Manual, however, put the "M3.5 screw" in the place of the "M4 screw".

4.5.2 Connecting the RS-232C connectors

The precautions and the connections are as described in the corresponding section in the AJ71C24-S8 User's Manual. (The following is added as "POINT" to (2)(a) in the manual.)

POINT

The CD terminal signal of the AJ71UC24 is treated in different ways in full-duplex and half-duplex transmissions. (See Section 3.2.2.)
Set the AJ71UC24 CD terminal signal on the computer as follows:

- For full-duplex transmission . . .Turn ON the signal in both send and receive data (at all times). (See Section 3.2.2.)
- For half-duplex transmission . . .Turn ON the signal only in send data. (See Chapter 5.)

4.5.3 Connecting the RS-422/485 connectors

The connections are as described in the corresponding section in the AJ71C24-S8 User's Manual.

4.5.4 Connecting a multidrop link and setting modes and terminal resistance

The details are as described in the corresponding section in the AJ71C24-S8 User's Manual, however, to the stations of which the SW23 or SW24 is designated to turn ON connect a terminal resistance instead. (See Section 4.3.4.)

4.6 Self-loopback Test

4.7 Loopback Test

4.8 Maintenance and Inspection

The details of these operations are as described in the respective corresponding sections in the AJ71C24-S8 User's Manual.

5. HALF-DUPLEX COMMUNICATIONS USING THE RS-232C INTERFACE

The details of half-duplex communications using the RS-232C interface are as described in the corresponding chapter in the AJ71C24-S8 User's Manual.

6. DATA COMMUNICATIONS USING AN M : N MULTIDROP LINK

The details of data communications using an m : n multidrop link are as described in the corresponding chapter in the AJ71C24-S8 User's Manual.

7. INITIAL SETTING OF TRANSMISSION CONTROL DATA TO BUFFER MEMORY

7.1 Setting RS-232C CD Terminal Check Enable/Disable

The details of setting RS-232C CD terminal check enable/disable are as described in the corresponding section in the AJ71C24-S8 User's Manual.

7.2 Setting the Transmission Method for RS-232C

7.3 *Reading Transmission Error Data*

7.4 Settings in the No-Protocol Mode

7.5 Settings in the Bidirectional Mode

The details of the these operations are as described in the respective corresponding sections in the AJ71C24-S8 User's Manual.

7.6 Mode Switching Setting

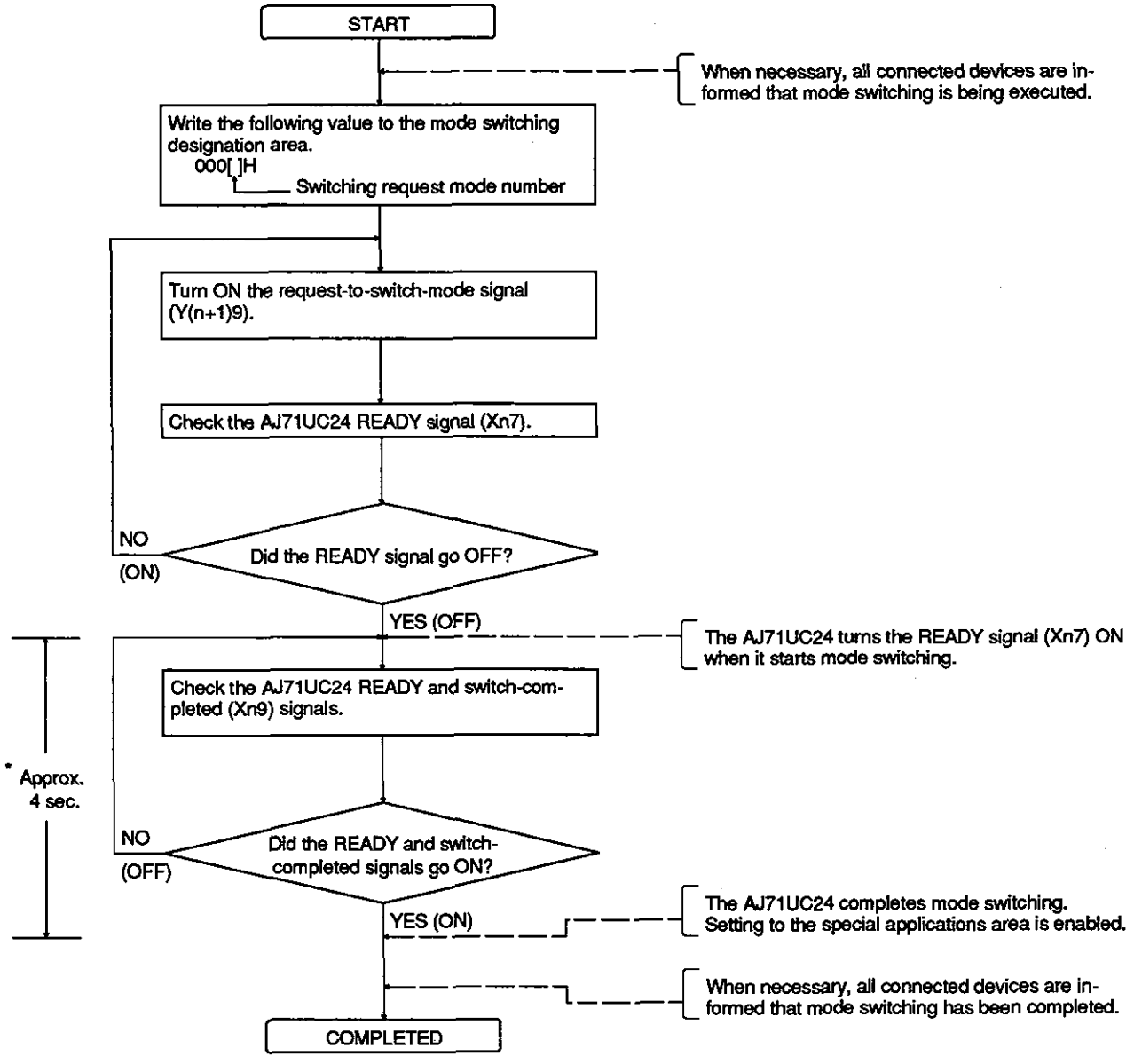
7.6.1 Reading in the mode setting state

The details are as described in the corresponding section in the AJ71C24-S8 User's Manual.

7.6.2 Mode switching designation

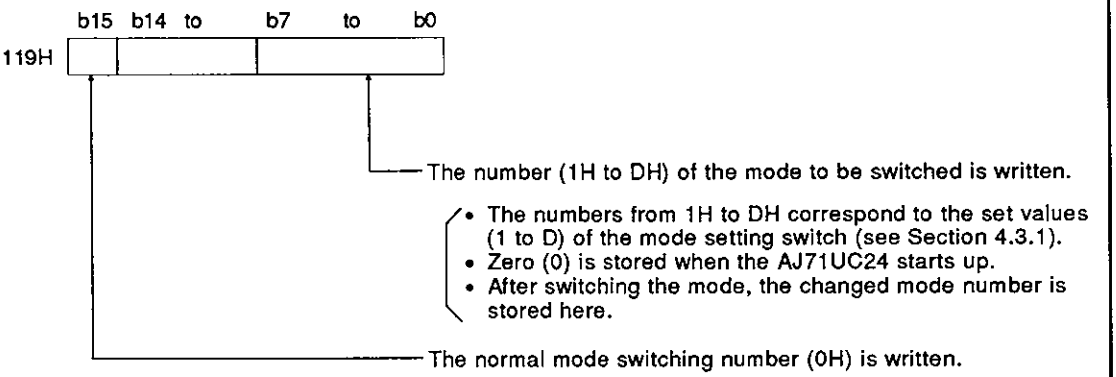
This section shows how to designate mode switching from a PC CPU and a designation example.

(1) Normal mode switching



*: The time slightly varies depending on the PC CPU used.

Designation Method

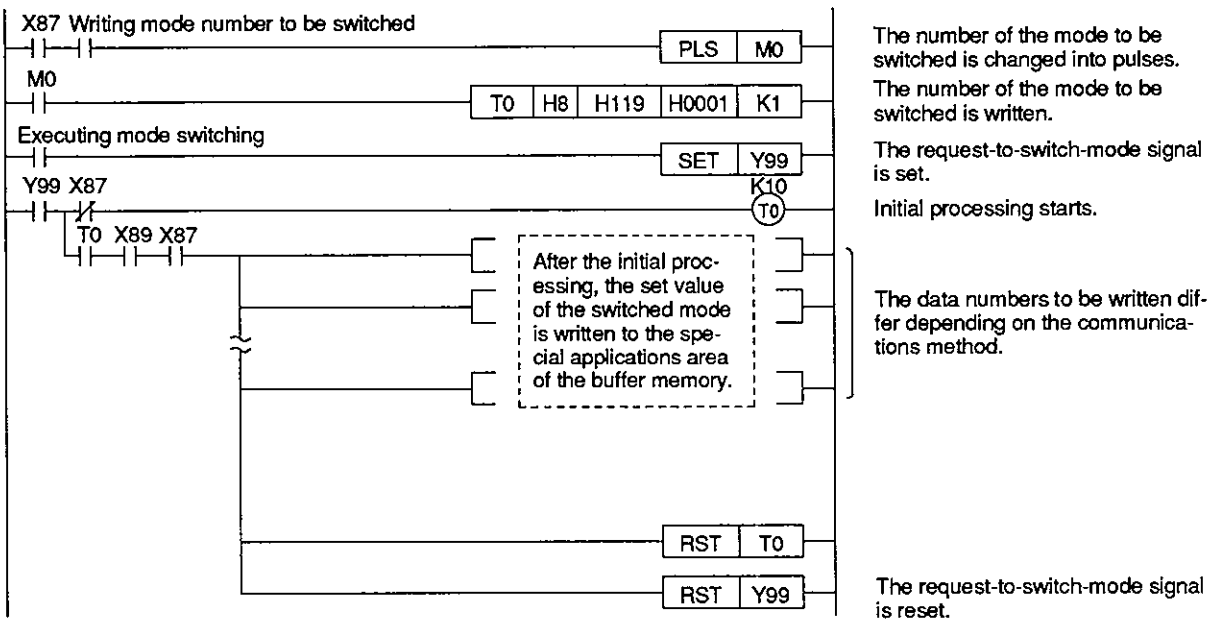


POINT

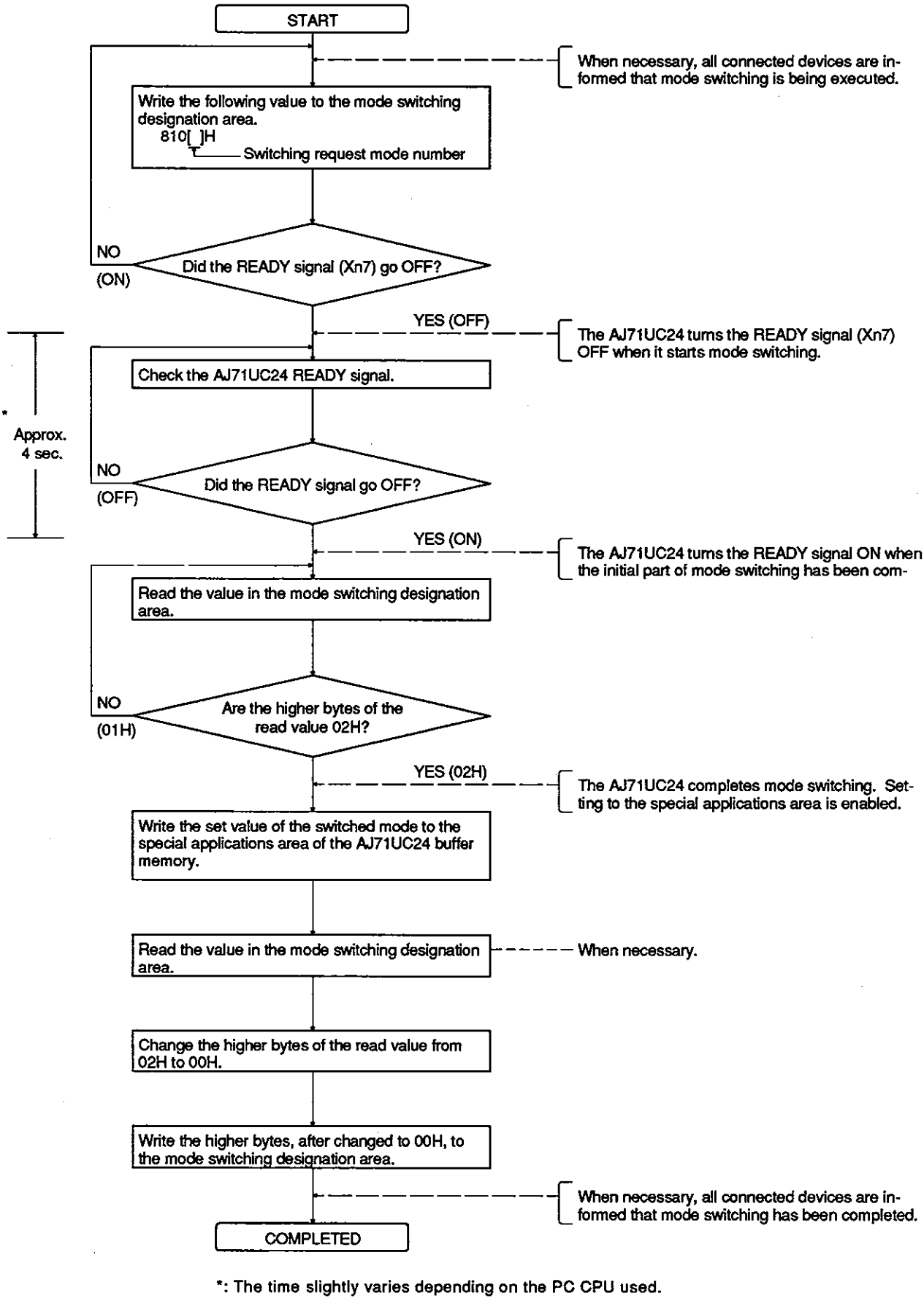
b8 to b14 of address 119H can take either 0 or 1.
(The AJ71UC24 will ignore them.)
But 0 must be set to b15.

Designation Example

When the mode is switched from a PC CPU to mode number 1 by normal mode switching (AJ71UC24 I/O addresses 80 to 9F)

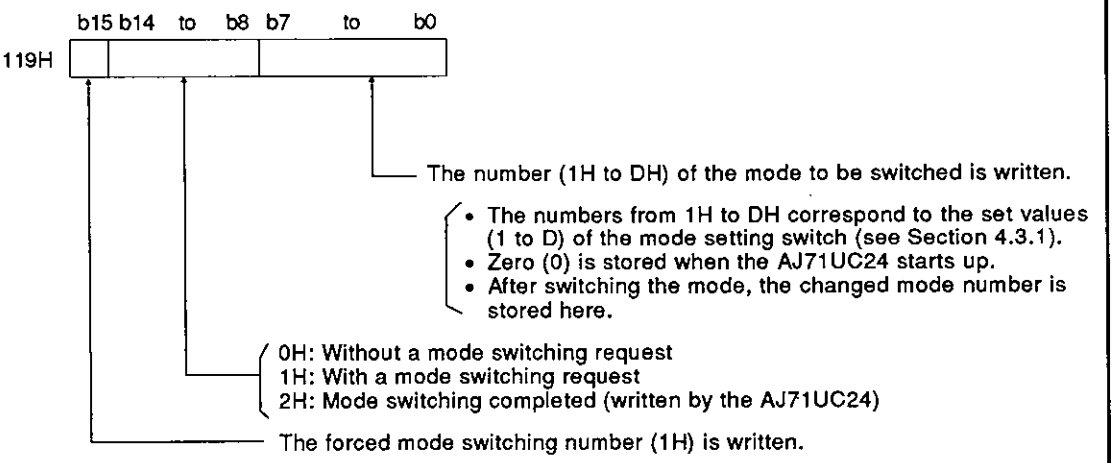


(2) Forced mode switching



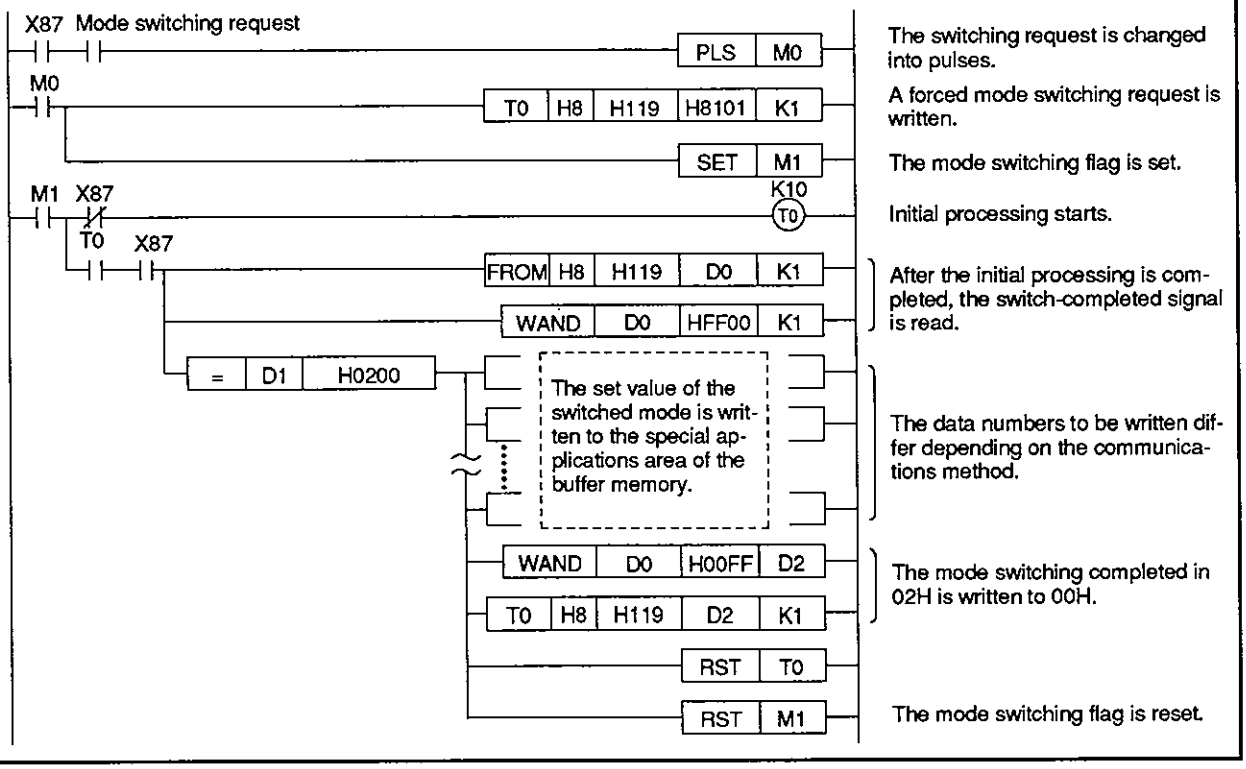
*: The time slightly varies depending on the PC CPU used.

Designation Method



Designation Example

When the mode is switched from a PC CPU to mode number 1 by forced mode switching (AJ71UC24 I/O addresses 80 to 9F)



7.7 Transmission Control Setting

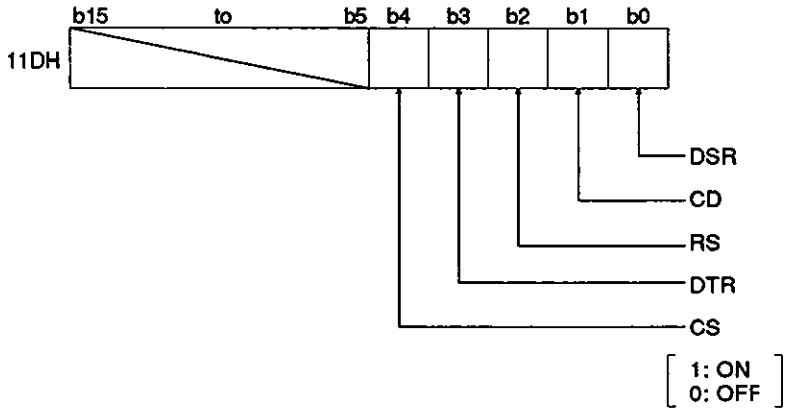
The details are as described in the corresponding section in the AJ71C24-S8 User's Manual.

7.8 Reading RS-232C Signal Data

This section describes the reading of the RS-232C communications signal data stored in the buffer memory.

(1) Signal data indicating area

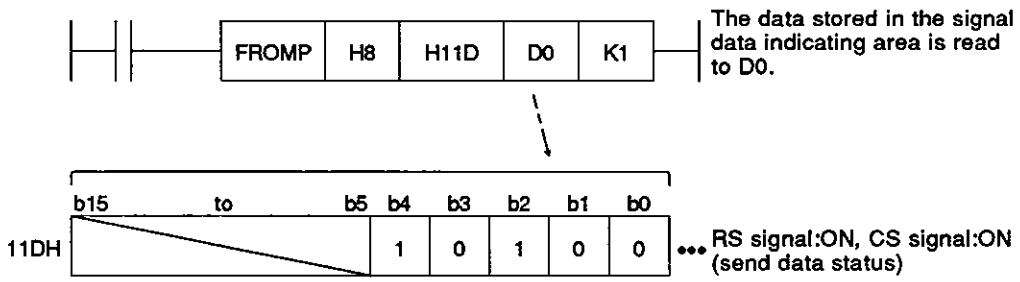
The RS-232C signal data is stored in buffer memory address 11DH, as illustrated below.



(2) Example of a program for reading the signal data indicating area

The following is an example of a program for reading the signal data stored in buffer memory address 11DH.

Example of a program for reading the signal data LED indicating area (AJ71UC24 I/O addresses 80 to 9F)



REMARK

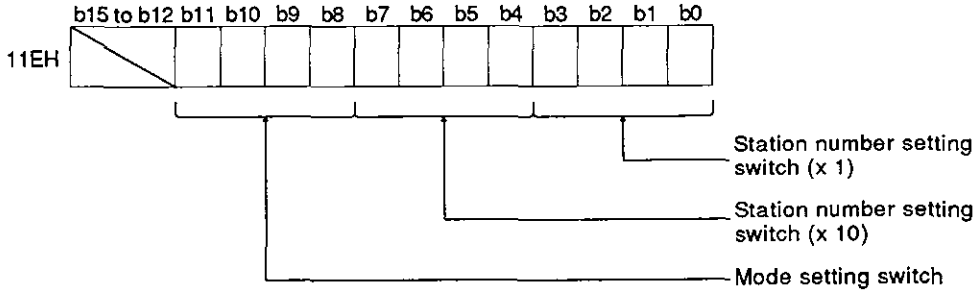
For the data of each bit in the signal data indicating area, see Section 3.2.2.

7.9 Reading the Mode Setting Switch/Station Number Setting Switch Status

This section describes the reading of the status of the mode setting and station number setting switches on the face of the AJ71UC24, stored in the buffer memory.

(1) Switch status indicating area

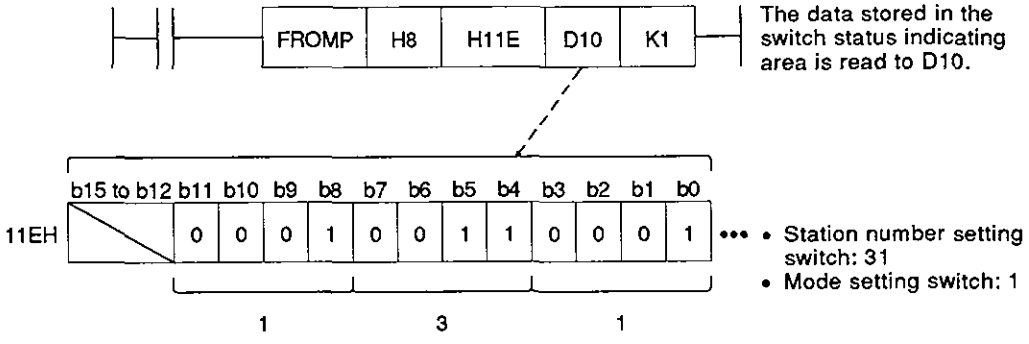
The statuses of the mode setting and station number setting switches are stored in buffer memory address 11EH, as illustrated below:



(2) Example of a program for reading the switch status indicating area

The following is an example of a program for reading the statuses of the mode setting and station number setting switches stored in buffer memory address 11EH.

Example of program (AJ71UC24 I/O addresses 80 to 9F)



REMARK

If the mode during operation is different from that set by the face switch due to mode switching (address 119H), it can be checked at the following addresses:

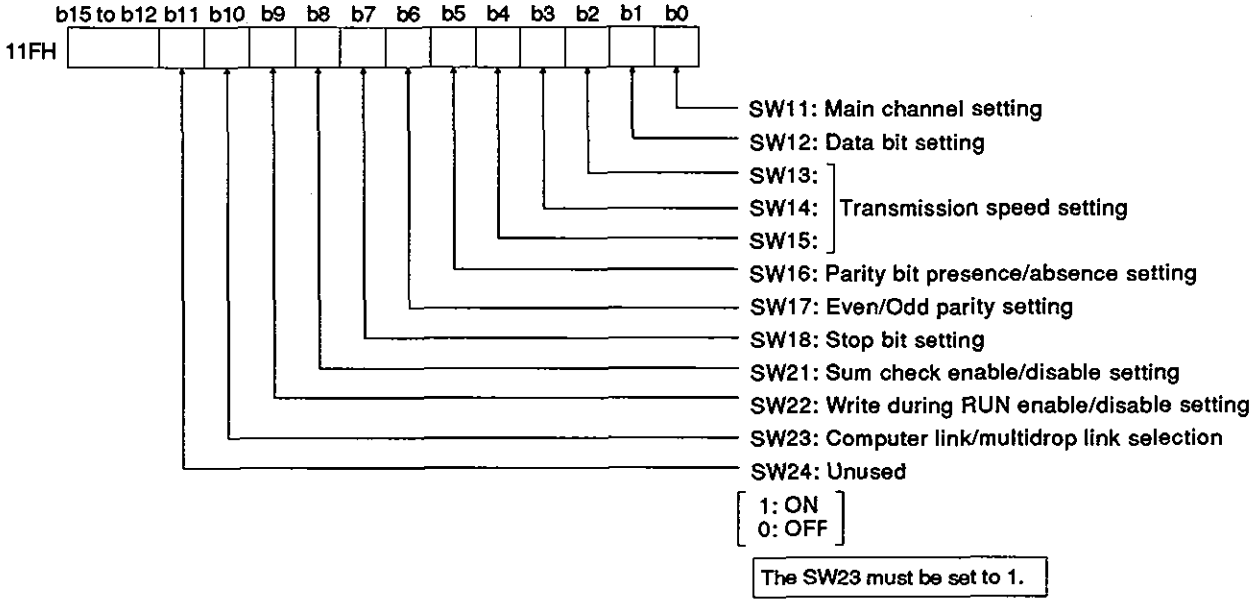
- Mode during operation ..... (Address 118H)
- Mode set by the face switch .... (Address 11EH)

7.10 Reading the Transmission Specification Setting Switch Statuses

This section describes the reading of the statuses of the transmission specification setting switches on the face of the AJ71UC24, stored in the buffer.

(1) Switch status indicating area

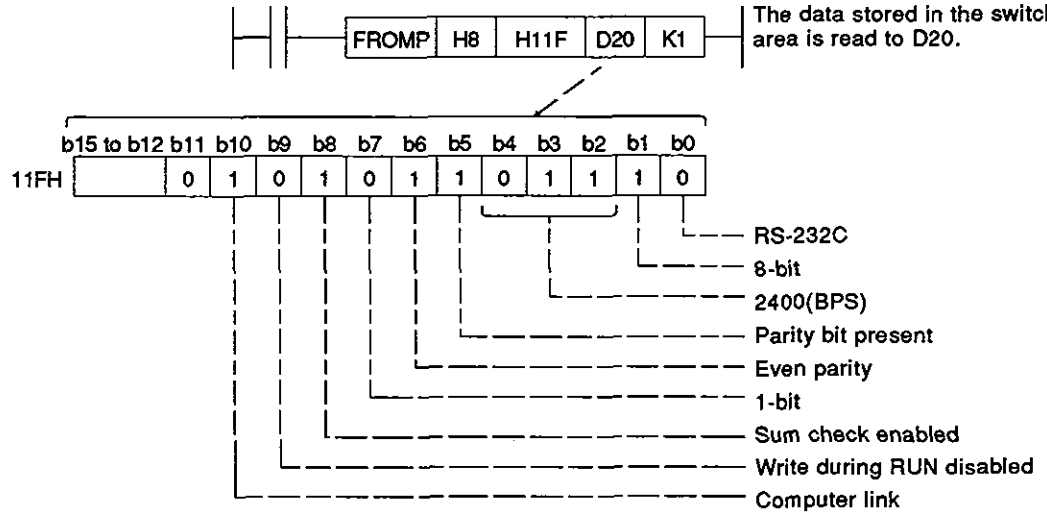
The statuses of the transmission specification setting switches are stored in buffer memory address 11FH, as illustrated below.



(2) Example of a program for reading the switch status indicating area

The following is an example of a program for reading the statuses of the transmission specification setting switches stored in buffer memory address 11FH.

Example of program (AJ71UC24 I/O addresses 80 to 9F)



REMARK

For the data of each bit in the switch status indicating area depends on the settings of the transmission specification setting switches on the face of the AJ71UC24 (see Section 4.3.2).

8. COMMUNICATIONS USING DEDICATED PROTOCOLS

8.1 Data Flow in Communications with Dedicated Protocols

8.2 Programming Hints

8.2.1 To write data to the special applications area in buffer memory

8.2.2 PC CPU operation during data communications

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.2.3 Precautions during data communications

Except for the following, the precautions are all given in the corresponding section in the AJ71C24-S8 User's Manual.

(Precautions (2) and (4) in the manual are changed as follows.)

(2) Framing errors in the computer

A framing error might occur in the computer if nothing is sent from the AJ71UC24 to the computer via the RS-422 interface.
In this case, set the computer to ignore all data sent from the AJ71UC24 until an ENQ, ACK or NAK code is transmitted.

(4) Data link error processing

The AJ71UC24 enters the standby state (see Section 3.6 I/O Signals List for CPU) if a data link or network error occurs during communications with a PC CPU (of a number other than FFH) of another station on MELSECNET (II) or MELSECNET/B.
If such an error is detected by the computer when executing a time check, send a clear command (EOT or CL code, see Section 8.4.5 (1)) to initialize the transmission sequence.

8.3 Basics of Dedicated Protocol Control Procedures

8.4 Basic Formats of Dedicated Protocol

8.4.1 Control format 1

8.4.2 Control format 2

8.4.3 Control format 3

8.4.4 Control format 4

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.4.5 Setting protocol data

Except for the "PC CPU numbers and accessible stations" shown below, the details are as described in the corresponding section in the AJ71C24-S8 User's Manual. (Step (4) in the section in the manual is changed as follows.)

(4) PC CPU numbers and accessible stations

The PC CPU number determines which PC CPU on MELSECNET (II) or MELSECNET/B to access.
The PC CPU number may be FFH or from 00H to 40H (or from 00H to 1FH on MELSECNET/B), which are set in the link module or network module, in a 2-digit ASCII code (hexadecimal).

(a) Accessing PC CPUs equipped with AJ71UC24 to which a computer is connected

Set all PC CPU numbers to "FF" (host) using the computer. Use any function except for the on-demand function.

(b) Accessing from a host station PC CPU equipped with AJ71UC24 to another station PC CPU in the same system

System Name	Computer-Connected AJ71UC24-Equipped PC CPU	Station to be Accessed	PC CPU Number
MELSECNET(II)	Master station	Local station Remote I/O station	Set the corresponding link module station number (1 to 64) in hexadecimal (00H to 40H).
	Local station	Master station	Set 00H.
MELSECNET/B	Master station	Local station	Set the corresponding link module station number (1 to 32) in hexadecimal (01H to 20H).
	Local station	Master station	Set 00H.

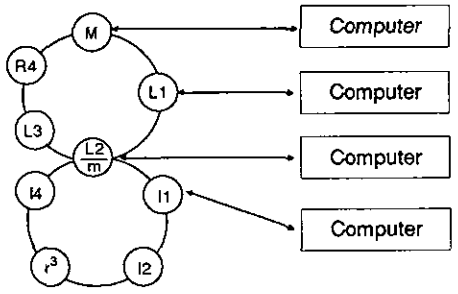
*1: Only the stations of the network number registered in the computer-connected station (host) are accessible. (See Section 8.16.3.)

*2: If the host station is an AnACPU, other normal stations are inaccessible.

(c) The range of the PC CPUs which can be accessed by setting the PC CPU numbers is shown below.

1) MELSECNET (II), MELSECNET/B

[Example: MELSECNET (II)]



M ..... Master station (1st tier)
L1 ..... Local station (2nd tier)
L2/m .. Local station (2nd tier)
Master station (3rd tier)
L3 ..... Local station (2nd tier)
R4 ..... Remote I/O station (2nd tier)
I1 ..... Local station (3rd tier)
I2 ..... Local station (3rd tier)
r3 ..... Remote I/O station (3rd tier)
I4 ..... Local station (3rd tier)

Computer-Connected AJ71UC24-Equipped PC CPU	PC CPUs to Which a Link is Possible (PC CPU Number)									
	Host (FF)	M (0)	L1 (1)	L2/m (2/0)	L3 (3)	R4 (4)	I1 (1)	I2 (2)	r3 (3)	I4 (4)
M	O	—	O	O	O	*1O	X	X	X	X
L1	O	O	—	X	X	X	X	X	X	X
L2/m	O	O	X	—	X	X	O	O	*1O	O
I1	O	X	X	O	X	X	—	X	X	X

O .... Accessible to all devices by setting appropriate PC CPU numbers.
*1O .... Accessible to special function buffer memory by setting appropriate PC CPU numbers.

POINT

Even if MELSECNET (II) is replaced by MELSECNET/B in any of the tiers, the range of accessible PC CPUs remains the same.

8.5 Transmission Sequence Timing Charts and Communications Time

The details are as described in the corresponding section in the AJ71C24-S8 User's Manual.

8.6 Character Area Data Transmission

The details are as described in the corresponding section in the AJ71C24-S8 User's Manual, except that the following "POINT" is added.

POINT

Use A to F (capital) to set characters in the character area.

8.7 Device Memory Read/Write

8.7.1 Commands and device ranges

Except for the following AnACPU common commands and the device ranges, the details are as described in the corresponding section in the AJ71C24-S8 User's Manual. (Step (2) in the section in the manual is changed as follows.)

(2) The AnACPU dedicated commands and device ranges used for device memory read/write are described below.

(a) AnACPU dedicated commands

Item		Command: Symbol	Command: ASCII Code	Processing Contents	Number of Points Processed per Communications	PC CPU Status: During STOP	PC CPU Status: During RUN: SW22 ON	PC CPU Status: During RUN: SW22 OFF	Reference Sections
Batch Read	Bit units	JR	4AH, 52H	Reads bit devices (X, Y, M, etc.) in units of points.	256 points	o	o	o	8.7.2
	Word units	QR	51H, 52H	Reads bit devices (X, Y, M, etc.) in units of 16 points.	32 words (512 points)				8.7.3
				Reads word devices (D, R, T, C, etc.) in units of points.	64 points				
Batch Write	Bit units	JW	4AH, 57H	Writes data to bit devices (X, Y, M, etc.) in units of points.	160 points	o	o	x	8.7.4
	Word units	QW	51H, 57H	Writes data to bit devices (X, Y, M, etc.) in units of 16 points.	10 words (160 points)				8.7.5
				Writes data to word devices (D, R, T, C, etc.) in units of points.	64 points				
Test (Random Write)	Bit units	JT	4AH, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of points by designating the devices and device numbers at random.	20 points	o	o	x	8.7.6
	Word units	QT	51H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of 16 points by designating the devices and device numbers at random.	10 words (160 points)				8.7.7
				Writes data to word devices (D, R, T, C, etc.) in units of points by designating the devices and device numbers at random.	10 points				
Monitor Data Registration	Bit units	JM	4AH, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of points.	40 points	o	o	o	8.7.8
	Word units	QM	51H, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of 16 points.	20 words (320 points)				
				Sets the word devices (D, R, T, C, etc.) to be monitored in units of points.	20 points				
Monitor	Bit units	MJ	4DH, 4AH	Monitors the devices registered for monitoring.	—	o	o	o	
	Word units	MQ	4DH, 51H						

Note : o .... Executable
x .... Not executable

(b) Device ranges when AnACPU dedicated commands are used

The devices and device number ranges that can be used for device memory access operation are described below.

The device designation code consists of 7 characters.

Leading zeros in the device number (underlined zeros in X000070, for example) can be expressed with a blank code (20H).

Device	+	Device number	=7 characters
{ 1 character (2 characters for T/C) }		{ 6 characters (5 characters for T/C) }	

Bit Device			Word Device		
Device	**Device Number Range (Characters)**	**Decimal/ Hexadecimal Expression**	**Device**	**Device Number Range (Characters)**	**Decimal/ Hexadecimal Expression**
Input X	X000000 to X0007FF	Hexadecimal	Timer (present value) T	TN00000 to TN02047	Decimal
Output Y	Y000000 to Y0007FF		Counter (present value) C	CN00000 to CN01023	
Internal relay M	M000000 to M008191	Decimal	Data register D	D000000 to D006143	Hexadecimal
Latch relay L	L000000 to L008191		Link register W	W000000 to W000FFF	
Step relay S	S000000 to S008191	Hexadecimal	File register R	R000000 to R008191	Decimal
Link relay B	B000000 to B000FFF		pecial register D	D009000 to D009255	
Annunciator F	F000000 to F002047	Decimal			
Special relay M	M009000 to M009255				
Timer (contact) T	TS00000 to TS02047				
Timer (coil) T	TC00000 to TC02047				
Counter (contact) C	CS00000 to CS01023				
Counter (coil) C	CC00000 to CC01023				

POINTS

(1) To designate the bit device ranges in units of words, the bit device number must be a multiple of 16.

For special relays M, whose device number is M9000 or greater, designation is possible by using "9000 + multiples of 16".

(2) Although the ranges are designated for M, L, and S, if the range for M is designated by L or S, the same processing occurs. This is also true for the ranges for L and S.

(3) The ranges of special relays (M9000 to M9255) and special registers (D9000 to D9255) are divided into the areas for read only, write only, and system use.

Trying to write data to the ranges outside the write-only area might cause the PC CPU to malfunction.

The ACPU programming manual gives details concerning special relays and special registers.

8.7.2 Batch read in units of bits

8.7.3 Batch read in units of words

8.7.4 Batch write in units of bits

8.7.5 Batch write in units of words

8.7.6 Testing device memory in units of bits (random write)

8.7.7 Testing device memory in units of words (random write)

8.7.8 Monitoring device memory

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.8 Extension File Register Read and Write

8.8.1 ACPU common commands and addresses

8.8.2 AnA dedicated commands and device numbers

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.8.3 Precautions during extension file register read /write

Except for the following, the details are as described in the corresponding section in the AJ71C24-S8 User's Manual. (Step (2) in the section in the manual is changed as follows.)

(2) Some types of memory cassette loaded to the PC CPU are unable to detect an error (character area error 06H) even if an attempt is made to read or write after specifying a block number which does not exist. In this case, data which is read may not be correct and writing such incorrect data may destroy the PC CPU user memory.
Be sure to check the type of memory cassette and the parameter settings before using this function.

Type of Memory Cassette	Block Numbers Which do not Cause a Character Area Error (06H)		
	A0J2H, A2, A3CPU	A2N, A3NCPU	A3H, AnA
A3NMCA-12	No.10 to No.11		
A3NMCA-18	—	No.10 to No.28	
A3NMCA-24	—	No.13 to No.20	No.13 to No.28
A3NMCA-40			No.21 to No.28
A4UMCA-32E			

(For details, see the UTLP-FN1 Operating Manual or the A2A (S1)/A3ACPU User's Manual.)

8.8.4 Batch read of the extension file register (ACPU common command)

8.8.5 Batch write of the extension file register (ACPU common command)

8.8.6 Direct read of the extension file register (AnACPU dedicated command)

8.8.7 Direct write of the extension file register (AnACPU dedicated command)

8.8.8 Testing (random write) the extension file register (ACPU common command)

8.8.9 Monitoring the extension file register

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.9 Buffer Memory Read and Write

8.10 Special Function Module Buffer Memory Read and Write

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.11 Remote Run/Stop of PC CPU and Reading PC CPU Model Name

8.11.1 Commands

(1) The following table shows the ACPU common commands used for remote run/stop and PC CPU model name reading.

Item	Command		Processing	State of PC CPU			Reference Sections
					During RUN		
	Symbol	ASCII Code		During STOP	Write Enable Setting	Write Disable Setting	
Remote RUN	RR	52H, 52H	Requests remote RUN of the PC CPU.	O	O	O	Section 8.11.2
Remote STOP	RS	52H, 53H	Requests remote STOP of the PC CPU.	O	O	O	
PC CPU Model Name Code Read	PC	50H, 43H	Reads the model name code of the PC CPU.	O	O	O	Section 8.11.3
PC CPU Model Name and Code Read	PU	50H, 55H	Reads the model name and its code of the PC CPU.	O	O	O	Section 8.11.4

Note: O..... Executable

8.11.2 Remote RUN/STOP

8.11.3 Reading PC CPU model name

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.11.4 Reading PC CPU model name and its code

This function reads the model name and corresponding code of a PC CPU linking with the computer.

(1) PC CPU model names and corresponding codes to be read

PC CPU Model Name	Code and Model Name To Be Read		PC CPU Model Name	Code and Model Name To Be Read	
	Code (Hexadecimal)	Model Name		Code (Hexadecimal)	Model Name
A0J2HCPU	98H	A0J2H	A3CPU	A3H	A3
A1CPU, A1NCPU	A1H	*1	A3NCPU		*1
A1SCPU(-S1)	98H	A1S	A3ACPU	94H	A3A
A2CPU(-S1)	A2H	A2	A3HCPU	A4H	A3H
A2NCPU(-S1)		*1	A3MCPU		A3M
A2ACPU	92H	A2A	A52GCPU	9AH	A52G
A2ACPU-S1	93H	A2AS1	A73CPU	A3H	*1
A2CCPU	9AH	A2C			

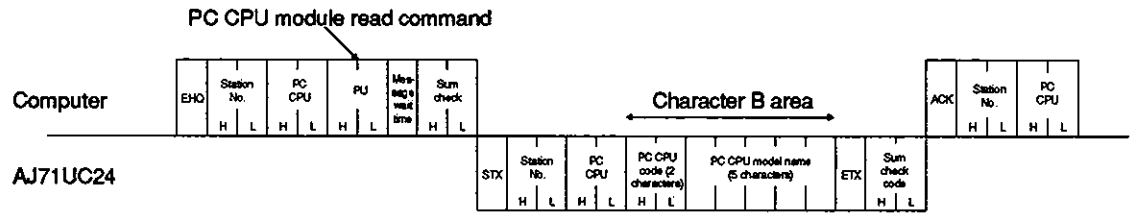
The number "*1" represents a blank (20H).

(2) Reading PC CPU model name (ACPU common commands)

The following is a method and example of designating the control protocol for reading the model name and corresponding code of a PC CPU linking with the computer.

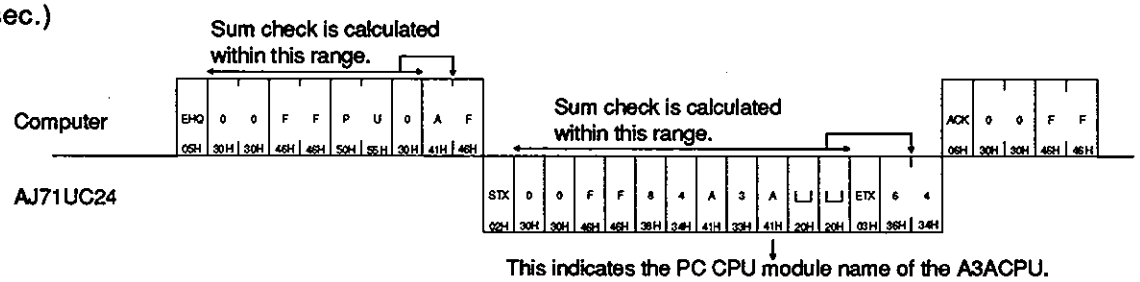
Designation Method

Designation in protocol 1 is shown below.



Designation Example

To read the PC CPU model name at self station (AJ71UC24 station No. 0) (Message wait time is 0 msec.)



8.12 Program Read/Write

8.12.1 Precautions during program read/write

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.12.2 Program read/write control procedures

8.12.3 Parameter memory read/write

8.12.4 Sequence program read/write

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

8.12.5 Microcomputer program read/write

8.12.6 Comment memory read/write

8.12.7 Extension comment memory read/write

8.13 Global Function

8.14 On-demand Function

8.15 Loopback Test

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

9. COMMUNICATIONS WITH A COMPUTER IN THE NO-PROTOCOL MODE

9.1 Basics of the No-Protocol Mode

9.2 Handshake I/O Signals

9.3 Programming Hints

9.3.1 To write data to the special applications area in buffer memory

The descriptions are as given in the corresponding sections in the AJ71C24-S8 User's Manual.

9.3.2 Precautions during data communications

Except for the following, the details are as described in the corresponding section in the AJ71C24-S8 User's Manual. (Step (3) in the section in the manual is changed as follows.)

(1) Framing errors in the external device

A framing error might occur in the external device if nothing is sent from the AJ71UC24 to the device via the RS-422 interface.
In this case, add to the head of the data sent from the AJ71UC24 a code, which helps the external device recognize the head of the data, using a sequence program.

9.4 Basic Program to Read/Write Buffer Memory

9.5 Receiving Data in the No-Protocol Mode (External Device → AJ71UC24)

9.6 Sending Data in the No-Protocol Mode (AJ71UC24 → External Device)

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

10. COMMUNICATIONS IN THE BIDIRECTIONAL MODE

10.1 Bidirectional Mode Basics

10.2 Handshake Signals and Buffer Memory

10.3 Programming Hints

10.3.1 System configuration and communications mode for bidirectional mode communications

10.3.2 To write data to the special applications area in buffer memory

The descriptions are as given in the respective corresponding sections in the AJ71C24-S8 User's Manual.

10.3.3 Precautions during data communications

Except for the following, the details are as described in the corresponding section in the AJ71C24-S8 User's Manual. (Step (7) in the section in the manual is changed as follows.)

(6) Framing errors in the computer

A framing error might occur in the computer if nothing is sent from the AJ71UC24 to the computer via the RS-422 interface.
In this case, set the computer to ignore all data transmitted from the AJ71UC24 until an ENQ, ACK or NAK code is sent.

10.4 Bidirectional Control Procedure Basics

10.5 Bidirectional Communications Basics

10.6 Processing an AJ71UC24 for Simultaneous Send in Full-Duplex Mode

10.7 Basic Program to Read/Write Buffer Memory

10.8 Receiving Data in the Bidirectional Mode (Computer → AJ71UC24)

10.9 Transmitting Data in the Bidirectional Mode (AJ71UC24 → Computer)

The descriptions are as given in the corresponding sections in the AJ71C24-S8 User's Manual.

11. TROUBLESHOOTING

This chapter describes errors which can occur with the computer link function and troubleshooting procedures.

11.1 NAK Error Codes with Dedicated Protocols

Table 11.1 shows the error codes and their descriptions when the NAK code is transmitted between the computer and the PC CPU using dedicated protocols.
The error codes are transmitted as 2-digit ASCII (hexadecimal) between 0H and FFH.
If several errors occur simultaneously, the code with the lowest number takes precedence and is transmitted.
If any of the following errors occurs, the transmission sequences are initialized and LEDs 2-NEU and 4-NEU (LED Nos. 4 and 7) are turned ON.

Table 11.1 Error Code List

Error Code (Hexa-decimal)	Error	Error Description	Indicator LED No.	Corrective Actions
00H	Disable during RUN	Invalid access has been made during RUN. (1) Data has been written to a PC CPU with the SW22 OFF (write disable during RUN). (2) Sequence program and parameters have been written.	2-C/N (LED No.10) 4-C/N (LED No.20)	(1) Start communications after turning ON the SW22. (2) Write parameters after setting the PC CPU to STOP.
01H	Parity error	Parity error (1) With the SW16 ON (parity enabled), the parity check result does not match the state (ON/OFF) of the SW17 (odd/even parity).	2-P/S (LED No.17) 4-P/S (LED No.21)	(1) Check the control protocol, and change the SW setting or data to restart data communications.
02H	Sum check error	Sum check error (1) With the SW21 ON (sum check enabled), the sum check result of the received data does not match the sum check code of the transmitted data, i.e., the sent data is different from the received data.	2-P/S (LED No.17) 4-P/S (LED No.21)	(1) Check the data transmitted from the computer and the sum check result. Correct invalid data, and restart data communications.
03H	Protocol error	The communications protocol is not valid. (1) Communications has been made with a protocol different from the one set by the mode setting switch. Or, the protocol is partly different from the designated one.	2-PRO (LED No.18) 4-PRO (LED No.22)	(1) Check and correct the mode setting switch position and the control protocol, and restart data communications.
04H	Framing error	Framing error (1) The data received does not match the setting of the SW18 (stop bit).	2-SIO (LED No.19) 4-SIO (LED No.23)	(1) Change the setting of the SW18 or the control protocol to restart data communications.
05H	Overrun error	Overrun error (1) New data has been transmitted before the AJ71UC24 received all the preceding data.	2-SIO (LED No.19) 4-SIO (LED No.23)	(1) Decrease the data transmission speed and restart data communications.

Table 11.1 Error Code List (Continued)

Error Code (Hexa-decimal)	Error	Error Description	Indicator LED No.	Corrective Actions
06H	Character area error	Character area A, B or C error, or the designated command does not exist. (1) The designation of the character area A, B or C for the control protocol set with the mode setting switch is not correct. (2) A command used with the control protocol does not exist. The number of processing points is outside the allowable range, or the designated device number does not exist in the designated PC CPU. (3) The device number is not set with the required number of characters. [ACPU common command : 5 characters, AnACPU common command: 7 characters]	2-PRO (LED No.18) 4-PRO (LED No.22)	(1) Check and correct the character area A, B or C, and restart data communications. (2) See the functions list in Section 3.3.1 and the PC CPU User's Manual to correct the designated commands, and restart data communications. (3) See Section 8.7.1 to correct the number of setting characters of the device number, and restart data communications.
07H	Character error	Character error (1) A character other than "A to Z", "0 to 9", "_" and the control codes in Section 8.4.5 (1) has been received.	2-PRO (LED No.18) 4-PRO (LED No.22)	(1) Check and correct the transmitted data, and restart data communications.
08H	PC CPU access error	Buffer memory is unable to make communications with the PC CPU. (1) The PC CPU is not the model mentioned in Section 2.2.	2-C/N (LED No.16) 4-C/N (LED No.20)	(1) Use a PC CPU which can perform data communications.
10H	PC CPU number error	The designated PC CPU number does not exist. (1) The PC CPU number designated with the control protocol was not the self "FF" or a station number set with the MELSECNET link parameters.	2-C/N (LED No.16) 4-C/N (LED No.20)	(1) Change the PC CPU number to the self "FF" or a station number set with the MELSECNET link parameters, and restart data communications.
11H	Mode error	Incorrect communications between an AJ71UC24 and a PC CPU. (1) After the AJ71UC24 has correctly received a request from the computer, normal data communications is not performed between the AJ71UC24 and the PC CPU due to noise or some other reason.	—	(1) Restart data communications. If the error recurs, check for noise and /or other causes, or replace the AJ71UC24. Then, restart data communications.
12H	Special function module designation error	Special function module designation error (1) A special function module, which has buffer memory and is capable of performing data communications, is not placed in the designated special function module number's position. Or the module number is wrong.	2-C/N (LED No.16) 4-C/N (LED No.20)	(1) Change the designated data of the control protocol or the special function module position, and restart data communications.

Table 11.1 Error Code List (Continued)

Error Code (Hexa-decimal)	Error	Error Description	Indicator LED No.	Corrective Actions
13H	Program step number designation error	Error in the designation of a sequence program step number. (1) A step number was designated, which lay outside the program range designated by the PC CPU parameters. (2) A subsequence program that did not exist (or could not be designated) was designated.	2-PRO (LED No.18) 4-PRO (LED No.22)	(1) Designate a step number which lies within the designated range or change the PC CPU parameters, and restart transmission. (2) Check the model name and the set parameter values of the corresponding PC CPU and whether the request is enabled.
18H	Remote error	Remote RUN/STOP is impossible. Remote STOP/PAUSE has already been executed from another module (such as another AJ71UC24).	2-PRO (LED No.18) 4-PRO (LED No.22)	(1) Check whether remote STOP/PAUSE is executed from another module. If executed, cancel it, and restart transmission.
20H	Data link error	Access was made to a station with which communications was discontinued.	2-C/N (LED No.16) 4-C/N (LED No.20)	Check the state of the data link.
21H	Special function module bus error	Memory access to the special function module cannot be made (for commands TR and TW). (1) Special function module control bus error (2) Special function module breakdown	2-C/N (LED No.16) 4-C/N (LED No.20)	The PC CPU, base unit, special function module or AJ71UC24 hardware has broken down. Consult the nearest Mitsubishi representative.
31H	Command error	An AnACPU dedicated command has been used with a PC CPU other than the AnACPU.	2-PRO (LED No.18) 4-PRO (LED No.22)	Use a proper command for the PC CPU concerned.

REMARKS

(1) Error codes 00H to 08H are transmitted to a computer after diagnosis by an AJ71UC24, when access is made by the computer to the AJ71UC24.

(2) Error codes 10H to 21H, 31H to 32H and 41H are transmitted from an AJ71UC24 to a computer after diagnosis by a PC CPU, when access is made by the AJ71UC24 to the PC CPU.

11.2 Bidirectional Mode Error Codes

11.3 Troubleshooting

The details are as described in the respective corresponding sections in the AJ71C24-S8 User's Manual.

MEMO

MULTIDROP LINK FUNCTION

This part describes the specifications, functions, buffer allocation and programming for using the AJ71UC24 as a multidrop link function module.

12. SPECIFICATIONS FOR MULTIDROP LINK FUNCTION

This section describes the transmission and interface specifications of the AJ71UC24.

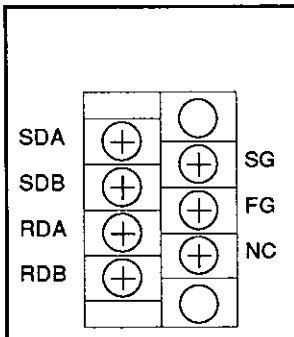
Since the functions, I/O specifications used with the PC CPU, and buffer memory differ with station settings of multidrop link master and multidrop link local, refer to respective section describing station settings.

12.1 Transmission Specifications

Item		Specifications
Interface		Conforms to RS-422/485.
Transmission system		Half duplex communication system
Synchronous system		Asynchronous system
Transmission speed		19200/38400 BPS (selectable)
Data format	Start bit	1
	Data bit	7
	Parity bit	1
	Stop bit	1
Error detection		Parity check (even)
		BCC check
DTR/DSR (ER/DR) control		Absent
DC1/DC3, DC2/DC4 control		Absent
Transmission distance		Total length 500 m (1640 ft)
Current consumption		5 VDC 0.1 A
I/O required		32 points
Recommended cable		SPEV (SB)-MPC-0.2 X 3P

12.2 RS-422/485 Interface Specifications

(1) Fig. 12.1 gives the specifications of the RS-422/485 interface used for connection between a computer and the AJ71UC24 and between the AJ71UC24 modules.



Signal Abbreviation	Signal Direction AJ71UC24 ↔ Computer	Description
SDA	→	Send data
SDB	→	Send data
RDA	←	Receive data
RDB	←	Receive data
SG	↔	Signal ground
FG	↔	Frame ground
NC	—	

Fig. 12.1 RS-442/485 Interface Specifications

(2) Fig. 12.2 shows a function block diagram of the RS-422/485 interface.

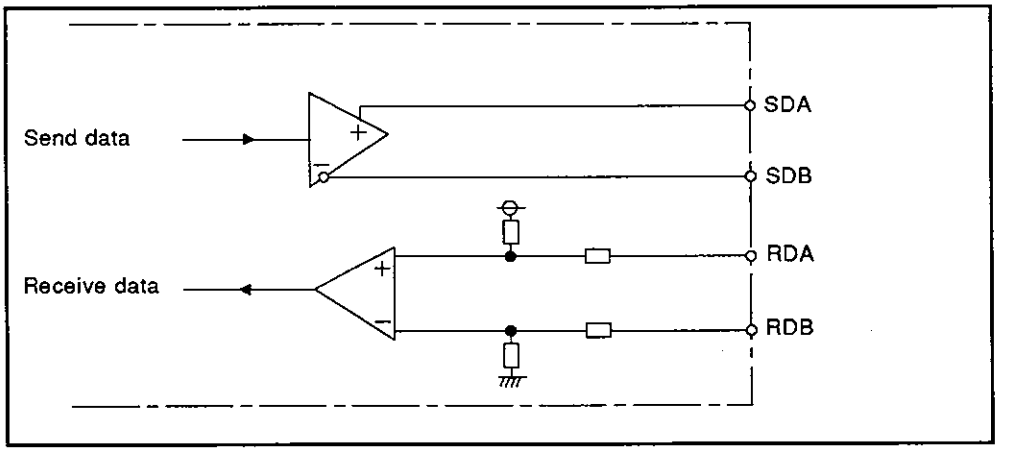


Fig. 12.2 Function Block Diagram of the RS-422/485 Interface

12.3 RS-422 Cable Specifications

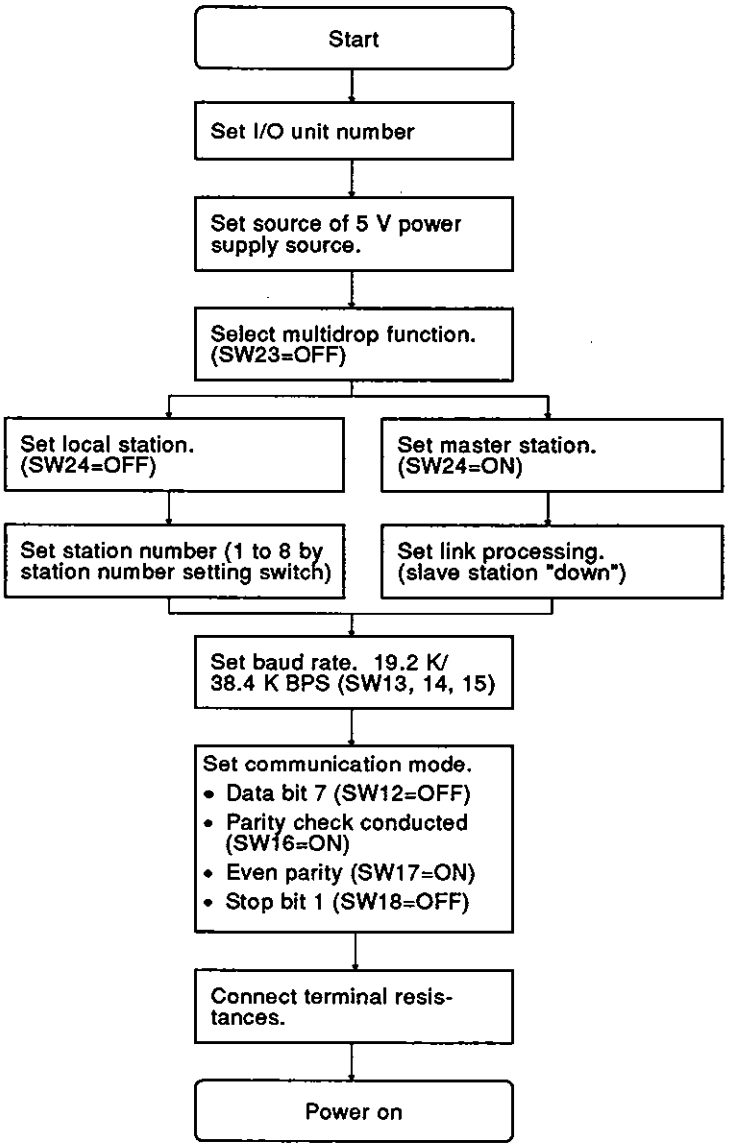
RS-422 cables must conform to the following specifications.

Item	Description
Cable type	Shielded
Number of pins	3 Pairs
Conductor resistance (20ºC)	88.0 Ω/km or less
Insulation resistance	10,000 MΩ km or less
Dielectric strength	500 VDC, 1 minute
Electrostatic capacity (1 KHz)	60 nF/km or less on average
Characteristic impedance (100 KHz)	110 ± 10 Ω

Fig. 12.3 RS-422 Cable Specification

13. SETTINGS AND PROCEDURES BEFORE OPERATION

13.1 Settings and Procedures before Operation

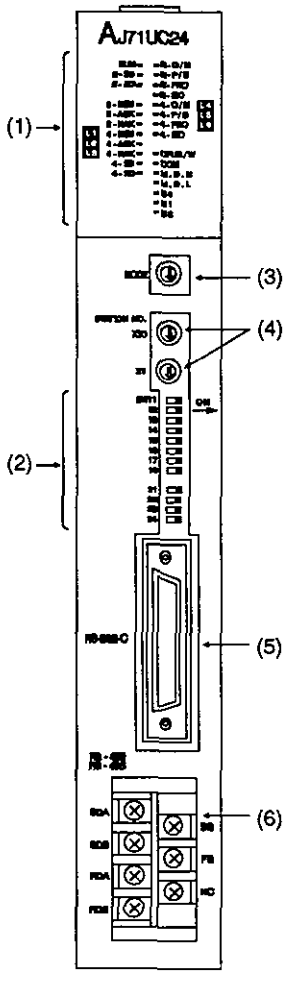


13.2 Nomenclature and LED Signals and Displays

This section shows the nomenclature of the AJ71UC24 and the details of the LEDs.

13.2.1 Nomenclature

This section shows the nomenclature of the AJ71UC24.

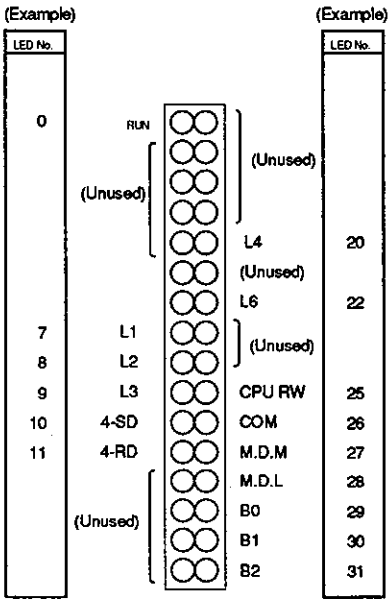


No.	Name	Description	Reference Sections
(1)	Indicator LEDs	Display the operating status, computer communications underway and alarms. What the ON/OFF status indicates depends on each indicator LED.	Section 13.2.2
(2)	Transmission specification setting switches	Used to select data bit, parity presence/absence, stop bit, sum check enable/disable, etc. (All switches factory-set to OFF)	Section 13.3.2
(3)	Mode setting switch	Unusable (Factory-set to 0)	——
(4)	Station number setting switches	Switch to set the station number in a multidrop link system. The X1 rotary switch is valid, and the X10 rotary switch is ignored.	Section 13.3.3
(5)	RS-232C connector	This connector is not used in a multidrop link system.	——
(6)	RS-422/485 interface	RS-422/485 interface for connecting an AJ71UC24 with another station in a multidrop link system.	Section 12.2

13.2.2 LED signals and displays

The following table shows the names and displays of the LEDs on the face of the AJ71UC24.

LED Area Details



LED No.	LED Name	Meaning of LED Display	LED ON	LED OFF	Initial Status of LED
0	RUN	Normal run	Normal	Error	ON
7	L1	Data transmission sequence execution status	Being executed	Not executed	OFF
8	L2	Connection preparation sequence error	Connection preparation sequence error	Normal	OFF
9	L3	Data transmission sequence error	Data transmission sequence error	Normal	OFF
10	4-SD	RS-422/485 send data status	Data being sent	Data not sent	OFF
11	4-RD	RS-422/485 receive data status	Data being received	Data not received	OFF
20	L4	Self-loopback test error	RS-422/485 data communications error	Normal	OFF
22	L6	Error slave station	Transmission being executed at stations other than error slave station	Normal	OFF
25	CPU RW	Result of communications with PC CPU	Flashes during communications with PC CPU (ON when no communications is executed)		ON
26	COM	Function selection	Computer link	Multidrop link	*2
27	M.D.M	Multidrop link master station designation	ON when SW23 is OFF (multidrop link) and SW24 is ON (master station)		OFF
28	M.D.L	Multidrop link local station designation	ON when both SW23 (multidrop link) and SW24 (local station) are OFF		OFF

LED No.	LED Name	Meaning of LED Display	Status of LED				Initial Status of LED
29	B0	Baud rate status	OFF		ON		*2
30	B1		ON	19200	ON	38400	
31	B2		ON		ON		

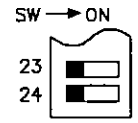
*1 The LED numbers shown above are just examples. They are not printed on the actual module.

*2 The initial status of the LEDs depends on the settings of the transmission specification setting switches (see Section 13.3.2).

13.3 Settings

13.3.1 Setting master/local station

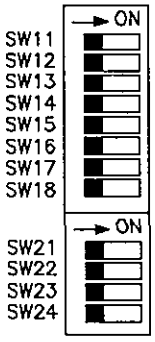
This section describes how to set the AJ71UC24 as a master station or local station.

Setting Switch	Switch Number	Setting Item	Status of Setting Switch	
			ON	OFF
	SW24	Master/Local station setting	Master station	Local station

The setting cannot be changed during operation even if the setting switch is set to the other position. It becomes valid when the power is turned on or the PC CPU connected to the AJ71UC24 is reset.

13.3.2 Settings of transmission specifications

The following table shows the settings of the transmission specifications (data bit, baud rate, etc.) and describes the setting switches.

Setting Switch	Switch Number	Setting Item	Status of Setting Switch							
			ON				OFF			
	SW11	Self-loopback test	Test mode				Data transmission mode			
	SW12	Data bit setting	8-bit				7-bit			
		Baud rate (BPS)	Un-usable	Un-usable	Un-usable	Un-usable	Un-usable	Un usable	19200	38400
	SW13	Transmission speed setting	OFF	ON	OFF	ON	OFF	ON	OFF	ON
	SW14		OFF	OFF	ON	ON	OFF	OFF	ON	ON
	SW15		OFF	OFF	OFF	OFF	ON	ON	ON	ON
	SW16	Parity presence/absence	Present				Absent			
	SW17	Even/Odd parity setting	Even				Odd			
	SW18	Stop bit setting	2-bit				1-bit			
	SW21	Sum check enable/disable setting	Enabled				Disabled			
	SW22	Link processing setting (when slave station is down)	Continued				Discontinued			
	SW23	Computer link/multidrop link selection	Computer link				Multidrop link			

The switches SW16 to SW21 and SW23 must be set to the positions indicated by hatching.

(1) The above settings cannot be changed during operation even if the switches (SW11 to SW23) are set to the other position. They become valid when the power is turned on or the PC CPU connected to the AJ71UC24 is reset.

(2) The SW22 is valid only when the AJ71UC24 is set as the master station. By setting the switch to ON, even if a slave station in the link system goes down in the middle of operation, the AJ71UC24 will disconnect it from the system and continue link processing. And the down slave station, as soon as it is restored to the normal state, will automatically return to the link system.
If the link system has a down slave station with the SW22 OFF, the system discontinues link processing to all stations.

(3) The baud rate can be set to 19200BPS or 38400BPS with the SW13, SW14 and SW15.
Set the baud rate to 38400BPS when the AJ71UC24 is a local station and the AJ71C22 is the master station.

(4) Set the SW21 to OFF at all times.

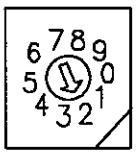
13.3.3 Station number setting

(1) When an AJ71UC24 is used as a master station

Station setting switches are invalid.

(2) When an AJ71UC24 is used as a local station

Only unit's place of station number setting switch is valid.



Station Number Setting Switches	Application
0	Unused
1	Station 1
2	Station 2
3	Station 3
4	Station 4
5	Station 5
6	Station 6
7	Station 7
8	Station 8
9	Unused

13.3.4 Connection of terminal resistance

Connect terminal resistance to the stations at both ends of a system connected by cable.

An example of a connecting terminal resistance is given below.

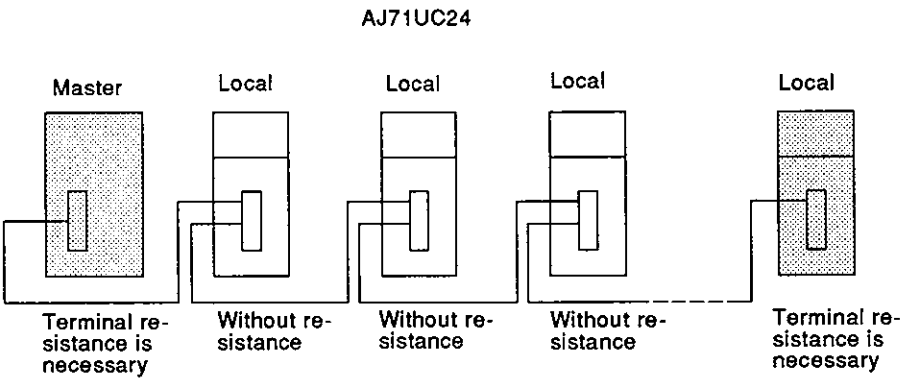
(1) Modules to which a terminal resistance needs to be connected

(a) When the following module is used as a master station:

AJ71UC24 : RS-422 communication (terminal resistance: 330 Ω) or RS-485 (terminal resistance: 110 Ω)

A0J2-C214(S1) : RS-422 communication (terminal resistance: 330 Ω)

AJ71C22(S1) : RS-422 communication (terminal resistance: 330 Ω)



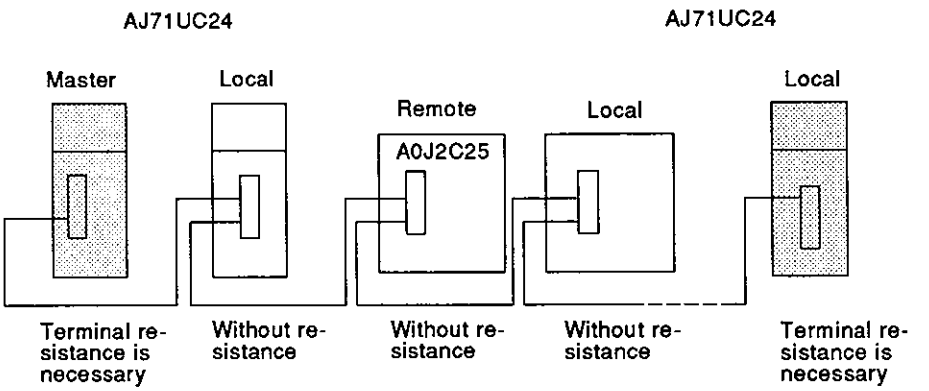
: Connect terminal resistance to the shaded modules.

(b) When the following module is used as a local station:

AJ71UC24 : RS-422 communication (terminal resistance: 330 Ω) or RS-485 (terminal resistance: 110 Ω)

A0J2-C214(S1) : RS-422 communication (terminal resistance: 330 Ω)

A0J2C25 : RS-422 communication (terminal resistance: 330 Ω)

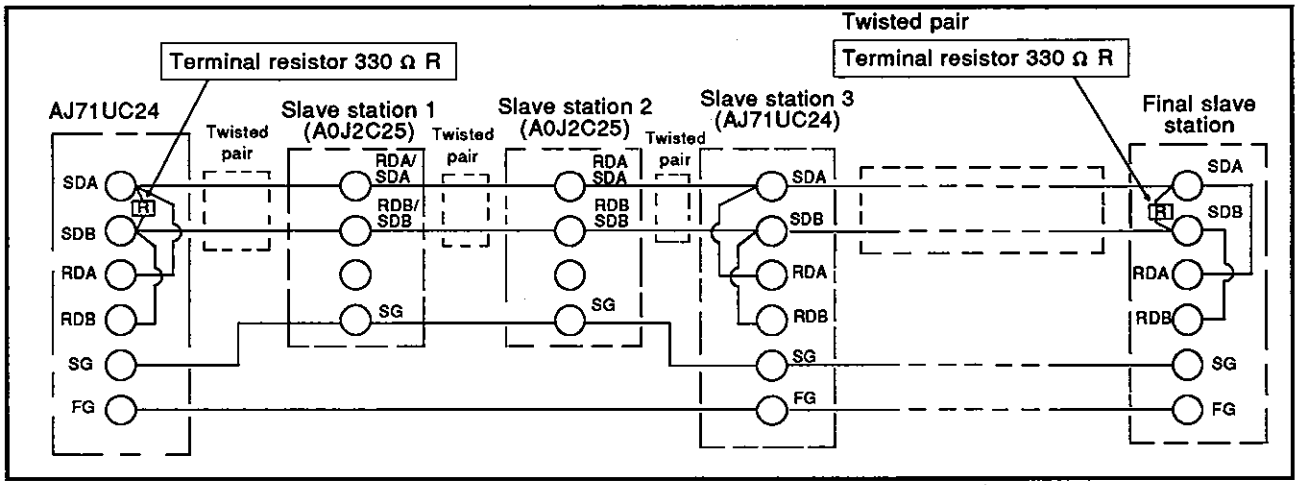


: Connect terminal resistance to the shaded modules.

13.4 External Wiring

13.4.1 Multidrop link connection

Connect the AJ71UC24 and slave stations as shown below.



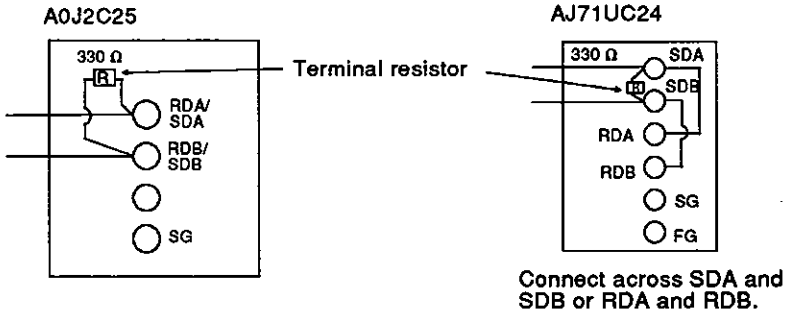
(1) The AJ71UC24 must be at the end as shown above.

(2) Connect AJ71UC24 terminals SDA with RDA and SDB with RDB.

(3) Connect the following terminals between the stations:

- SDA (or RDA) and SDA (or RDA)
- SDB (or RDB) and SDB (or RDB)
- SG and SG
- FG and FG (not provided for the A0J2C25)

(4) Connect a terminal resistor in the final slave station.



The terminal resistor should be used to ensure reliable data communication.

POINT

Communications using RS-422 or RS485 is possible in a multidrop link consisting of AJ71UC24 modules only.

Conect terminal resistances of 330 Ω when RS-422 is used, or 110 Ω when RS-485 is used.

13.5 Self-loopback Test

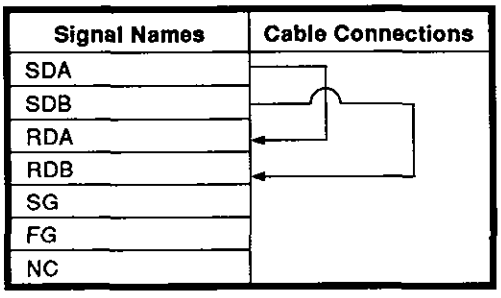
The self loopback test is used to check that the AJ71UC24 module is operating normally. This function is selected when SW11 is ON.

13.5.1 Procedure to carry out self-loopback test

The procedure to carry out the self-loopback test is as follows:

(Step 1) Connect the cables

Connect cables to the RS-422/485 terminal blocks as shown below.



(Step 2) Set the transmission specification setting switch

(a) Master station

- Turn SW24 (master station/local station setting switch) ON.
- Turn SW23 (computer link/mulitdrop link setting switch) OFF.
- Turn SW11 (self-loopback test setting switch) ON.
- Turn SW13 to SW15 (Transmission speed setting) to OFF/ON/ON(19200 BPS) or ON/ON/ON(38400 BPS).

(b) Local station

- Turn SW24 (master station/local station setting switch) ON.
- Turn SW23 (computer link/mulitdrop link setting switch) OFF.
- Turn SW11 (self-loopback test setting switch ON.
- Turn SW13 to SW15 (Transmission speed setting) to OFF/ON/ON(19200 BPS) or ON/ON/ON(38400 BPS).

(Step 3) Execute the self-loopback test

(a) Turn ON power to the PC CPU or reset the PC CPU.

The AJ71UC24 starts checking automatically.

(b) Checking

RS-422/485 is checked.

(The AJ71UC24 executes checking automatically.)

The checking is completed within one second.

(c) Check the LED display status as described in Section 13.2.2.

Normal : Follow procedure (4) to complete the test.

Error : Correct the error and repeat the self-loopback test.

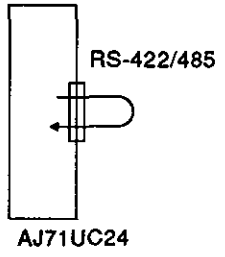
(d) When checks are completed:

1) Turn the power supply OFF.

2) Disconnect the cables. Connect the cables to perform multidrop link.

3) Turn SW11 (self-loopback test setting switch) OFF (data transmission mode).

13.5.2 Self-loopback test operations

Check Items	Check Descriptions	Normal Indicator LED		Error Indicator LED		Information Flow
RS-422/485 communications check	Checks data sent from RS-422/485 connector. If normal, AJ71UC24 changes data and the procedure is repeated. If not normal, an error is indicated. An error is indicated if no cable is connected.	L4 (LED NO.20)	OFF	L4 (LED NO.20)	ON	
		4-SD (LED NO.10)	Flashing			
		4-RD (LED NO.11)				

* The test continues even if an error occurred with a checking item.

14. AJ71UC24 MASTER STATION

14.1 Functions

Item		Function	Ref. Section
Initial setting	Number of slave stations to be accessed	Set the number of slave stations to be accessed.	14.3.1
	Transmission precedence	Set the order in which salve stations are accessed during transmission sequence cycles.	14.3.1
	Amount of data communicated between stations	Set the number of bits to be communicated with each slave station. Maximum for network: 512 (256/512 points selectable) Maximum per slave station: receive 128, transmit 128	14.3.3
Off-communication station setting		Sets all points of send data, to be transmitted to a specified slave station, to OFF and ignores received data. Stores OFF data to buffer memory receive data area.	14.3.4
Pre-transmission sequence		The AJ71UC24 transfers initial data slave stations to check the initial setting. When the response is correct, the AJ71UC24 proceeds to the data transmission sequence.	14.6
Data transmission sequence		The AJ71UC24 communicates with slave stations in accordance with the initial data.	14.7
		In the event that a slave station goes down during communication, + 1) That slave station may disconnected for continued network processing; or 2) Data transmission over the network may be stopped. *: When 1) is selected, the faulty station can return to the link system by a return request	
Transmission time monitoring		The maximum and present transmission times can be monitored in batches to within 10 msec. (From buffer addresses 62H and 63H.)	14.3.7
Loopback self-check		The RS-422/485 port can be self-checked.	13.5

14.2 I/O Signals List for PC CPU

I/O device numbers depend on the AJ71UC24 I/O unit number.

The device numbers indicated in the table below assume that the I/O unit number has been set to 0.

(1) Input signals (AJ71UC24 to PC CPU)

16 points from Xn0 to XnF are provided.

Device	Signal Name	Description
Xn0	During data transmission sequence	• On during normal data transmission sequence. • Off indicates pre-transmission sequence or an error.
Xn1	Pre-transmission sequence error	• On indicates an error during pre-transmission sequence. • Switched off when Y(n+1)1 is turned on.
Xn2	Data transmission sequence error (Valid when link processing setting is STOP (SW22 OFF).)	• On indicates an error during data transmission sequence. • Switched off when Y(n+1)1 is turned on.
Xn3	Data transmission sequence error (Valid when link processing setting is CONTINUE (SW22 ON).)	• On indicates an error during data transmission sequence. • Switched on by a return request when the faulty slave station retunes to the link system.
Xn4 to XnC	—	Reserved
XnD	WDT (Watch dog timer) error	• Switched on when the AJ71UC24 watch dog timer times out.
XnE XnF	—	Reserved

POINT

Yn0 to YnF which are unused by the AJ71UC24 may be used as internal relays.

(2) Output signals (PC CPU to AJ71UC24)

16 points from Y(n+1)0 to Y(n+1)F are provided.

Device	Signal Name	Description
Y(n+1)0	Link start-up	• Switch on to start up the AJ71UC24. Keep this signal on during operation. • Switch off to stop transmission.
Y(n+1)1	Error reset	• Use this signal to turn off Xn1 or Xn2.
Y(n+1)2 to Y(n+1)F	—	Reserved

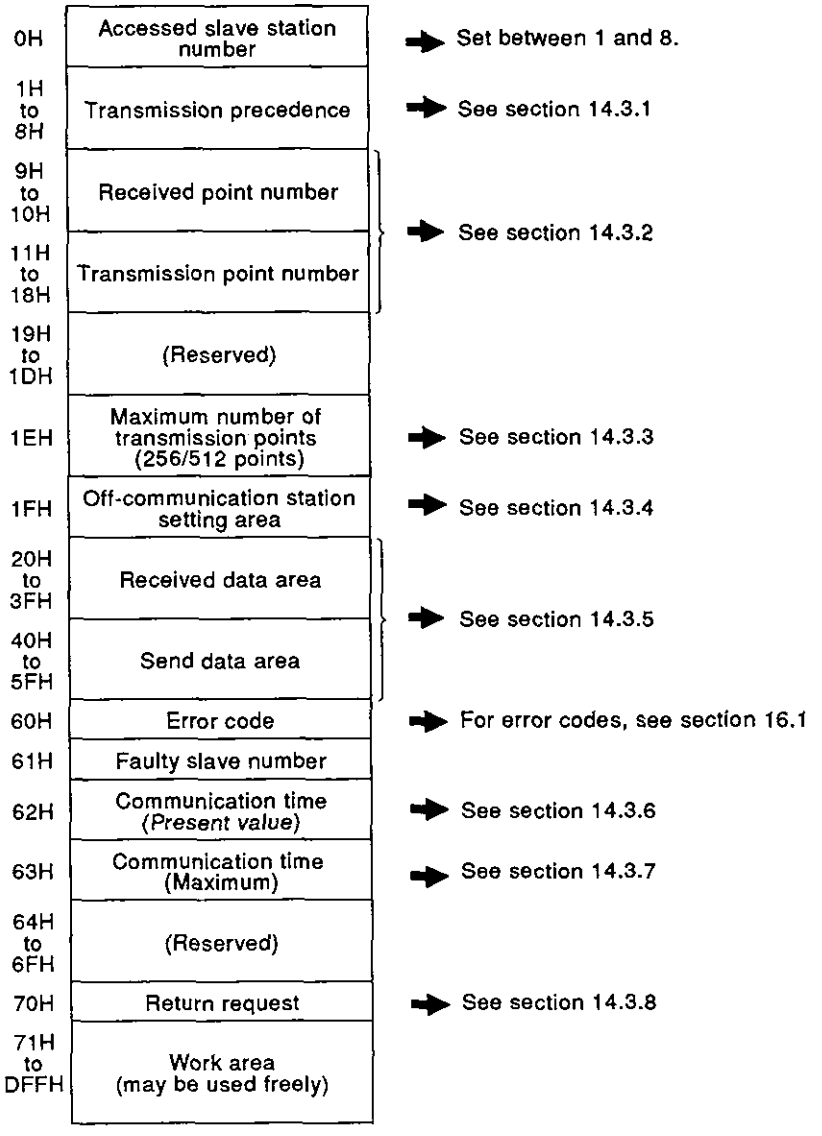
IMPORTANT

Y(n+1)2 to Y(n+1)F are reserved for the use by the system and cannot be used by sequence programs.
If any of these devices in used (ON/OFF) by a sequence program, correct operation of the AJ71UC24 are not guaranteed.

14.3 Buffer Memory

The AJ71UC24 has a buffer memory for data communication with the PC CPU. For data transfer between the PC CPU and buffer memory, use the FROM and TO instructions.

Buffer addresses are 16 bit locations.



POINT

Error codes (address 60H) must be removed from the buffer memory by resetting the PC.

Codes are not cleared when the cause of the error is removed.

The error code in address 60H is always the most recent one.

14.3.1 Accessed slave station/transmission priority

Specify the number of slave stations to be accessed and their corresponding communication priority. Specify the number of slave stations at address 0H and station codes at addresses 1H to 8H.

Data communication in mode in order of address numbers.

0H	Number of accessed slave stations. (max. 8)
1H	1st accessed station
2H	2nd accessed station
3H	
4H	
5H	
6H	
7H	
8H	Final accessed station

Set fixed codes.

	Fixed Code
Station 1	62H
Station 2	63H
Station 3	64H
Station 4	65H
Station 5	66H
Station 6	67H
Station 7	68H
Station 8	69H

POINT

When the power is switched on or the PC CPU is reset, codes 62H to 69H are automatically written to addresses 1H to 8H by the OS as default values.

Example: Specify slave station communication priority as: stations 2, 7, 4, 1 and 5

1H	63H
2H	68H
3H	65H
4H	62H
5H	66H
6H	
7H	
8H	

Set the number of slave stations in buffer address 0H.

POINTS

(1) The "number of accessed slave stations" determines the maximum number of slave stations which may be accessed. If further stations are specified in the priority list, these are ignored.

(2) *Error code "33" is written to address 60H if:*

1) The same station number is repeated;

2) The specified number of slave stations is greater than the number set in the priority list.
(e.g. 5 stations specified at address 0H, but only three stations set to addresses 1H to 3H); or

3) Any code other than 62H to 69H has been used in the priority list.

14.3.2 Number of communication data bits

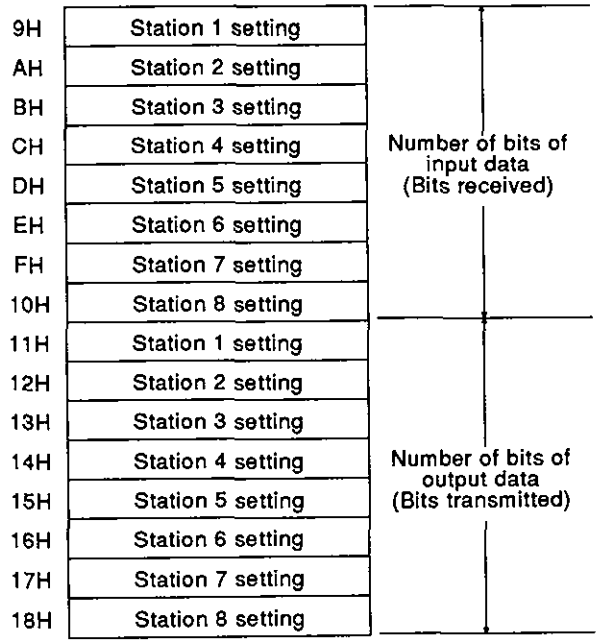
Specifies the number of bits used for transmit and receive data communication. Specify the number of receive bits at addresses 9H and 10H and the number of transmit bits at addresses 11H to 18H.
Note the following restrictions:

(1) The total number of receive plus transmit bits for all stations must not exceed 256 or 512.

(2) The number of receive data points per station must not exceed 128.

(3) The number of transmit data points per station must not exceed 128.

(4) Communication data must be specified in batches of 8 bits.



POINT

If the communication data setting is not a multiple of 8, error code "33" is written to buffer address 60H.

Example:

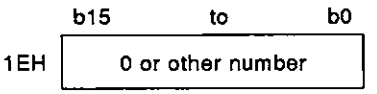
	Station 1	Station 2	Station 4	Station 5	Station 7
Input	8	24	16	0	0
Output	16	8	16	16	16

(Stations 1 and 2 = A0J2C25, stations 4, 5 and 7 = AJ71UC24 local)

9H	8	Bits received
AH	24	
BH	0	
CH	16	
DH	0	
EH	0	
FH	0	
10H	0	
11H	16	Bits transmitted
12H	8	
13H	0	
14H	16	
15H	16	
16H	0	
17H	16	
18H	0	

14.3.3 Maximum number of transmission points setting area

This area is used to set the maximum number of transmission points, to be handled with remote and local stations, at 256 or 512 points.
Write 0 or other number to buffer memory at address 1EH.



0 : 256 points
Other : 512 points

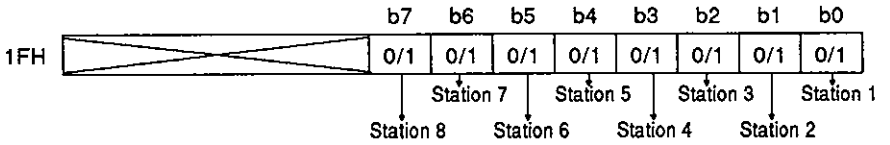
POINT

The transmission data storage procedure differs according to the setting (256 or 512 points).

If the setting is changed, setting of the read and write addresses used with the data transmission program needs to be modified.

14.3.4 Off-communication station setting area

This area is used to set slave stations to the off-communication station.
Write 0 for off-communication cancel or 1 for off-communication set to the lower 8 bits of buffer memory at address 1FH.



0: Off-communication cancel
1: Off-communication set

14.3.5 Communication data area

Communication data between the master and slave stations is written to the lower 8 bits of buffer addresses 20H to 5FH.

Received data is written to addresses 20H to 3FH.
Data for transmission is written to addresses 40H to 5FH and then set to slave stations.

This data area must be assigned to slave stations in order of station numbers (ignoring the transmission priority) in accordance with the number of bits specified for communication, starting at address 20H or 40H.
This is illustrated in the following example:

(1) When the maximum number of transmission points is set at 256.

The following is the example of allocation of the transmission data storage areas when the maximum number of transmission points is set at 256 and the number of transmission points of each slave station is set as shown below.

	Station 1	Station 2	Station 3	Station 4
Receive points	8	24	0	48
Send points	24	16	24	16

	Unused	ON/OFF data: (n+7)th point to "n"th point	
20H		Points 1 to 8 of received data of Station 1	Received data storage area
21H		Points 1 to 8 of received data of Station 2	
22H		Points 9 to 16 of received data of Station 2	
23H		Points 17 to 24 of received data of Station 2	
24H		Points 1 to 8 of received data of Station 4	
25H		Points 9 to 16 of received data of Station 4	
26H		Points 17 to 24 of received data of Station 4	
27H		Points 25 to 32 of received data of Station 4	
28H		Points 33 to 40 of received data of Station 4	
29H		Points 41 to 48 of received data of Station 4	
2AH to 3FH			
40H		Points 1 to 8 of received data of Station 1	Send data storage area
41H		Points 9 to 16 of received data of Station 1	
42H		Points 17 to 24 of received data of Station 1	
43H		Points 1 to 8 of received data of Station 2	
44H		Points 9 to 16 of received data of Station 2	
45H		Points 1 to 8 of received data of Station 3	
46H		Points 9 to 16 of received data of Station 3	
47H		Points 17 to 24 of received data of Station 3	
48H		Points 1 to 8 of received data of Station 4	
49H		Points 9 to 16 of received data of Station 4	
4AH to 5FH			

(2) When the maximum number of transmission points is set at 512.

The following is the example of allocation of the transmission data storage areas when the maximum number of transmission points is set at 512 and the number of transmission points of each slave station is set shown below.

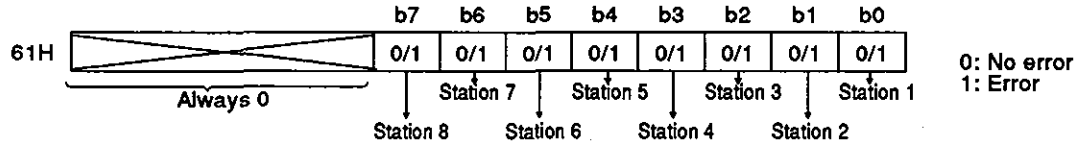
	Station 1	Station 2	Station 3	Station 4
Receive points	8	24	0	48
Send points	24	16	24	16

ON/OFF data

	(n+7)th point to (Higher 8 bit) to "n"th point	(n+7)th point to (Lower 8 bit) to "n"th point	
20H	Points 1 to 8 of received data of Section 2	Points 1 to 8 of received data of Section 1	Received data storage area
21H	Points 17 to 24 of received data of Section 2	Points 9 to 16 of received data of Station 2	
22H	Points 9 to 16 of received data of Section 4	Points 1 to 8 of received data of Station 4	
23H	Points 25 to 32 of received data of Section 4	Points 17 to 24 of received data of Station 4	
24H	Points 41 to 48 of received data of Section 4	Points 33 to 40 of received data of Station 4	
25H to 3FH			
40H	Points 9 to 16 of received data of Section 1	Points 1 to 8 of received data of Station 1	Send data storage area
41H	Points 1 to 8 of received data of Section 2	Points 17 to 24 of received data of Station 1	
42H	Points 1 to 8 of received data of Section 3	Points 9 to 16 of received data of Station 2	
43H	Points 17 to 24 of received data of Section 3	Points 9 to 16 of received data of Station 3	
44H	Points 9 to 16 of received data of Section 4	Points 1 to 8 of received data of Station 4	
45H to 5FH			

14.3.6 Faulty slave station indication

Errors are indicated (0: no error, 1: error) for the appropriate station in the lower 8 bits of address 61H.

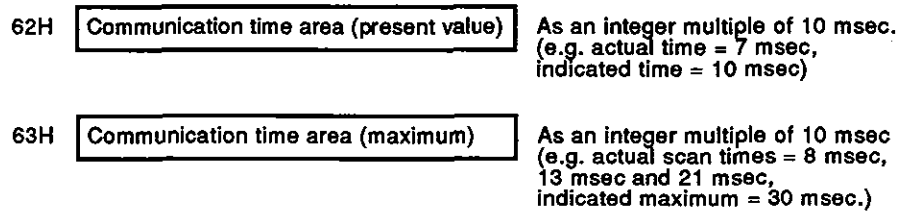


(1) With SW22 ON the faulty station is disconnected from the network which continues communication without that station.

(2) The error indication is cleared when the faulty station returns to the network after a return request is given or when the pre-transmission sequence is restarted after the error has been reset.

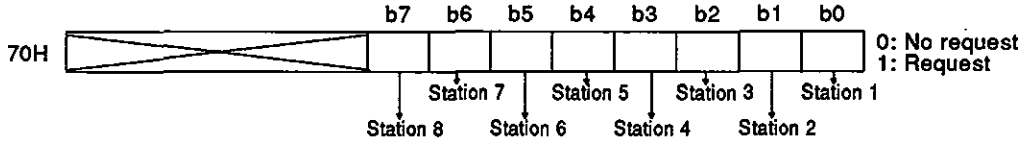
14.3.7 Communication time

Each communication cycle time and the maximum cycle time are written in units of 10 msec.



14.3.8 Return request

With SW22 ON writing 1 to the appropriate bit of address 70H returns the faulty station to the network.

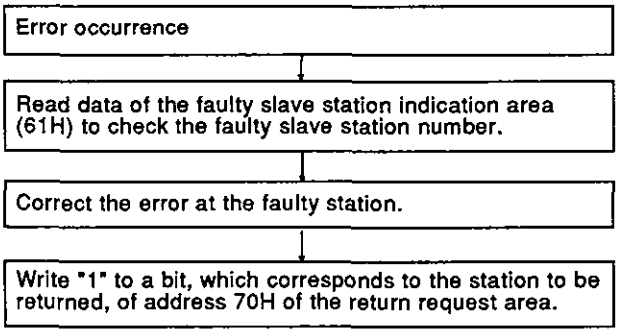


Writing 1 to the corresponding bit causes the pre-transmission sequence to be processed for the appropriate station.

If this is completed normally, the data transmission sequence is executed for the next scan.
(The corresponding bit is cleared when the OS receives the return request.

POINT

The following procedure is used to restore a station to the network when SW22 is ON.

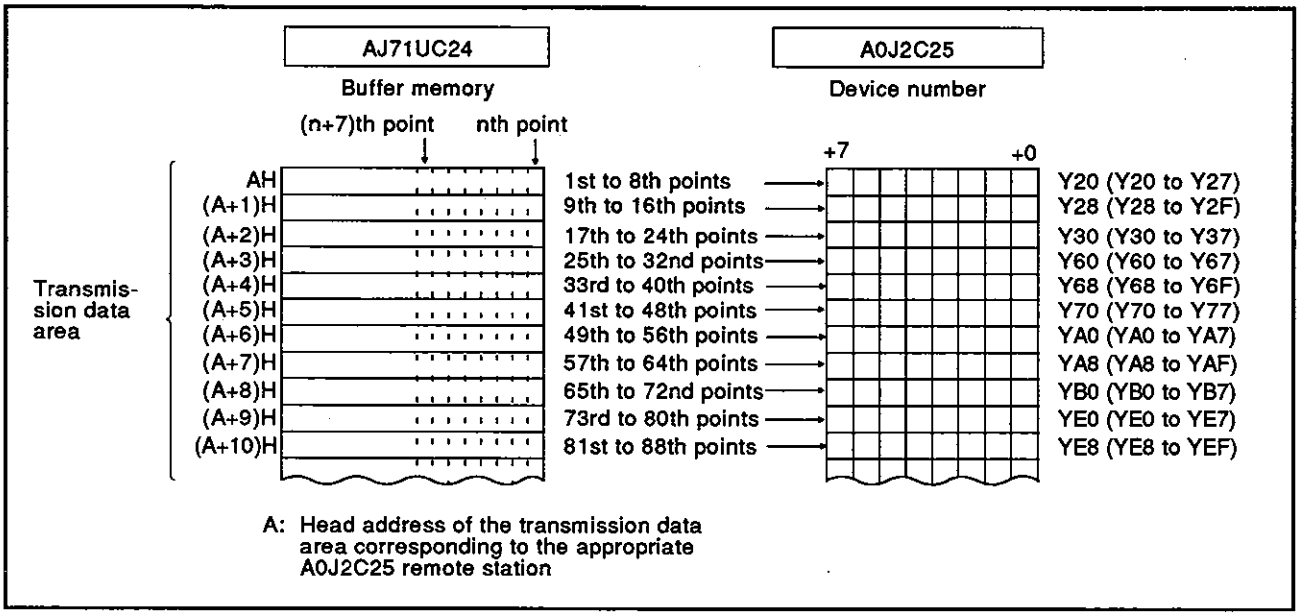


14.4 Data Communications Methods with Slave Stations with the Maximum Communications Point Setting of 256 Points

14.4.1 Communication with A0J2C25

(1) Data transmitted from AJ71UC24 to A0J2C25

Transmitted AJ71UC24 buffer bits correspond to A0J2C25 outputs (Y) as indicated below:

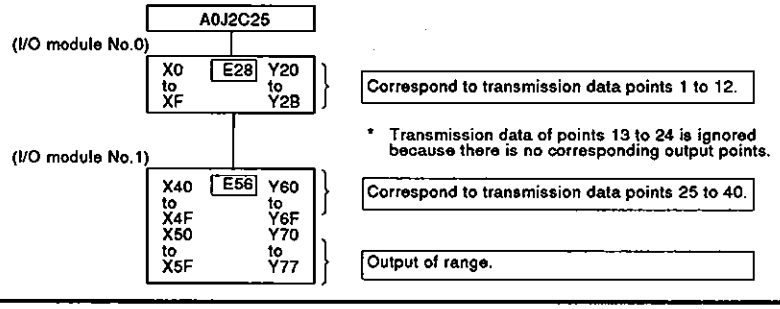


Writing ON/OFF data to the relevant AJ71UC24 buffer transmission data bits switches the corresponding A0J2C25 outputs (Y) on or off, (e.g. "1" written to bit 0 (1st point) of address AH, switches Y20 on at the A0J2C25 station).

POINT

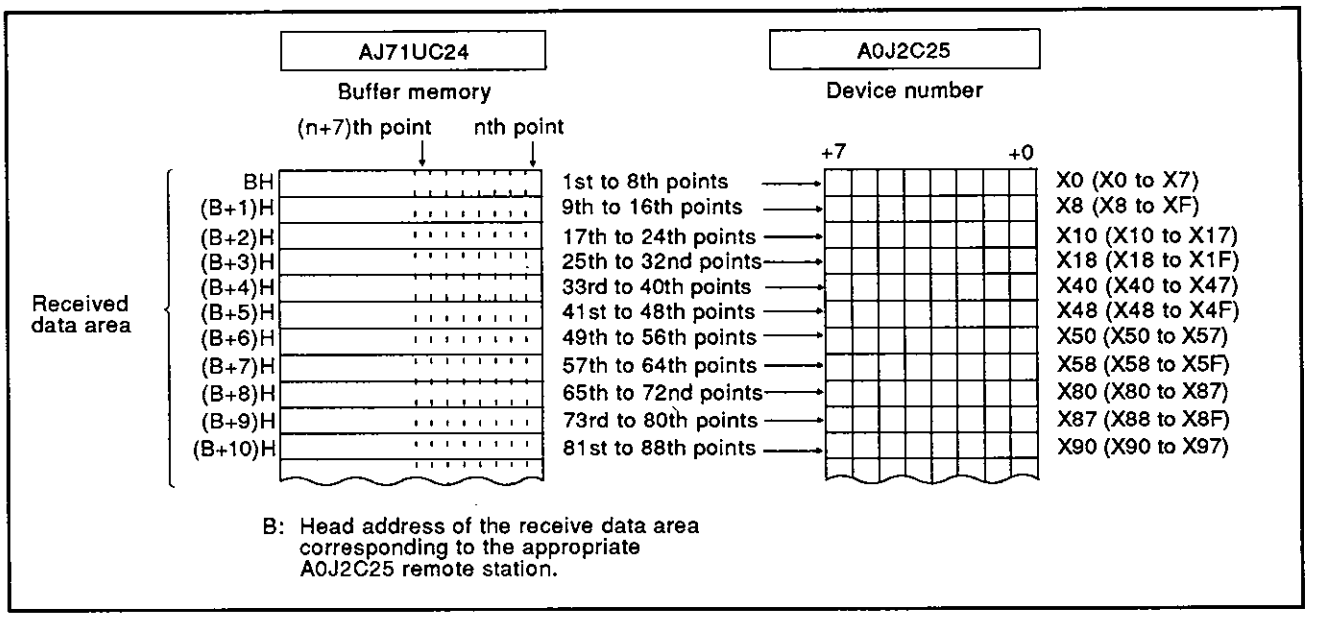
The number of I/O points of I/O modules (A0J2-E56[ ][ ], E28[ ][ ], E32[ ], E24[ ]) connected to the A0J2C25 is fixed to 32 input points and 24 output points per module regardless of the module type.
If a 28-point module is connected to the A0J2C25, the transmission data of the AJ71UC24 which corresponds to 14 output points of the second half is ignored. If an input module is connected to the A0J2C25, the transmission data of the AJ71UC24 which corresponds to 24 output points is ignored because there is no corresponding output points.

Example: When the number of transmission data points is set at 40 points in the system shown below:



(2) Data received from A0J2C25 by AJ71UC24

Bits received by the AJ71UC24 buffer memory correspond to A0J2C25 inputs (X) as shown below:



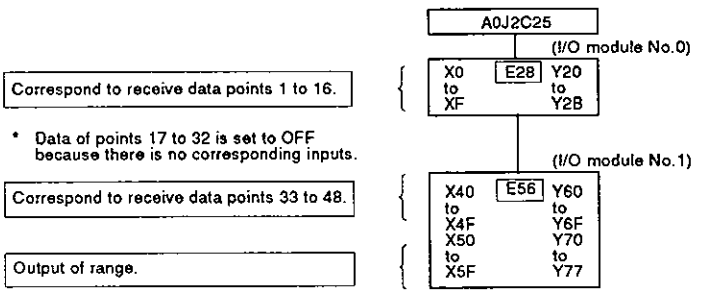
Switching the A0J2C25 inputs on or off causes the corresponding AJ71UC24 buffer bits to switch between 1 and 0 respectively. (e.g. switching X1 on at the remote station, causes bit 1 in buffer address BH to switch on)

POINT

The number of I/O points of I/O modules (A0J2-E56[ ][ ], E28[ ][ ], E32[ ], E24[ ]) connected to the A0J2C25 is fixed to 32 input points and 24 output points per module regardless of the module type.

If a 28-point module is connected to the A0J2C25, the data received by the AJ71UC24 which corresponds to 16 input points of the second half is set to OFF ("0"). If an output module is connected to the A0J2C25, the data received by the AJ71UC24 which corresponds to 32 input points is set to OFF ("0") because there is no corresponding input signals.

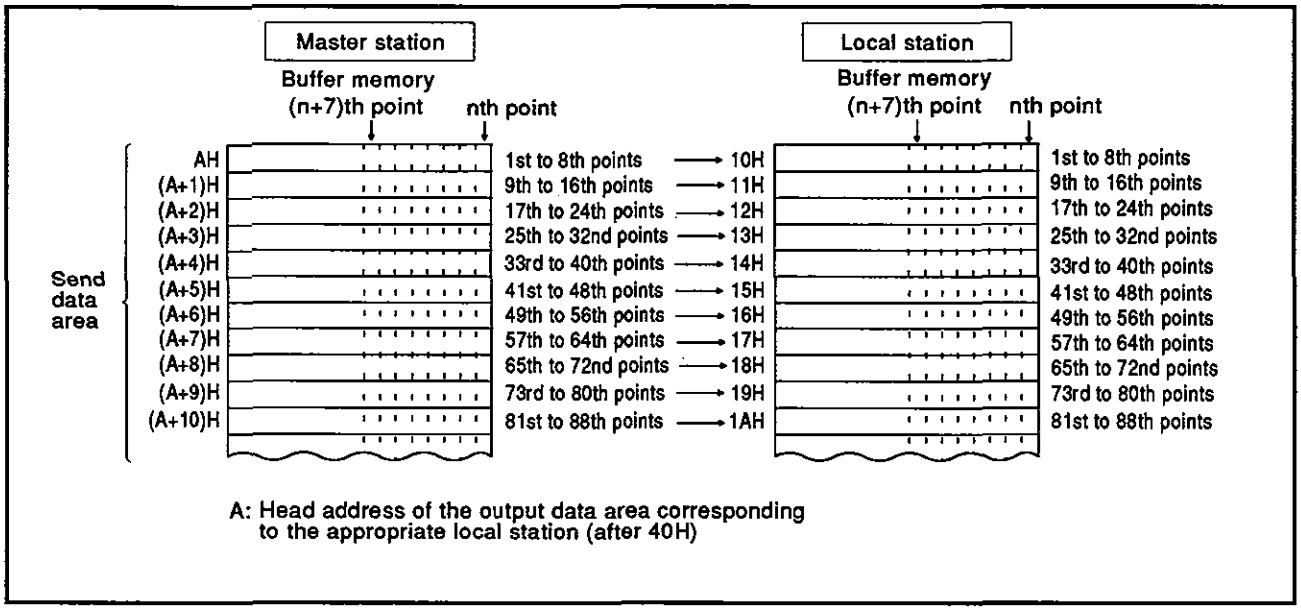
Example: When the number of receive data points is set at 48 points in the system shown below:



14.4.2 Communication with local station (AJ71UC24)

(1) Data output from master to local station

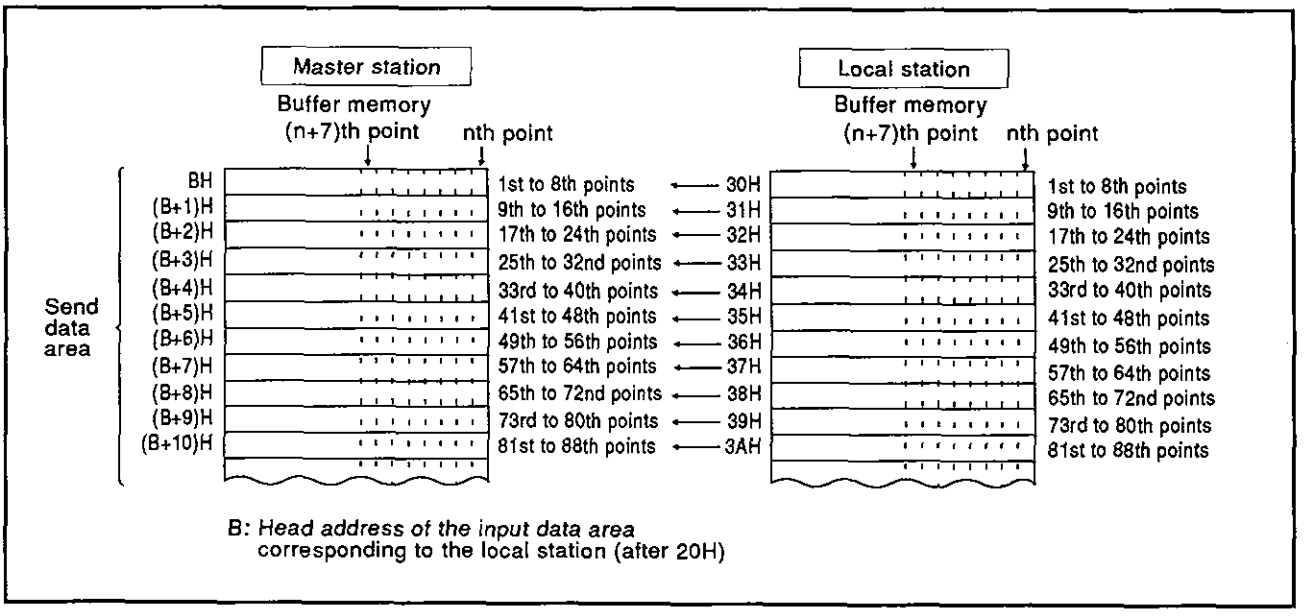
For data transmission from the master to the local station, master buffer bits correspond to local buffer bits as illustrated below.



Writing ON/OFF data to master buffer bits switches the corresponding local buffer bits on/off.
(e.g. "1" written to bit 0 of the master AJ71UC24 buffer address AH, switches bit 0 of the appropriate local AJ71UC24 buffer address 10H "on".)

(2) Data input from the local to the master station

When receiving data from the local station, the master buffer bits correspond to the local buffer bits as shown below:



Writing ON/OFF data to local buffer bits switches the corresponding master buffer bits on/off.
(e.g. "1" written to bit 0 of the local AJ71UC24 buffer address 30H, switches bit 0 of the master AJ71UC24 buffer address BH "on".)

14.5 Data Communication with Slave Stations when the Maximum Number of Transmission Points is Set at 512

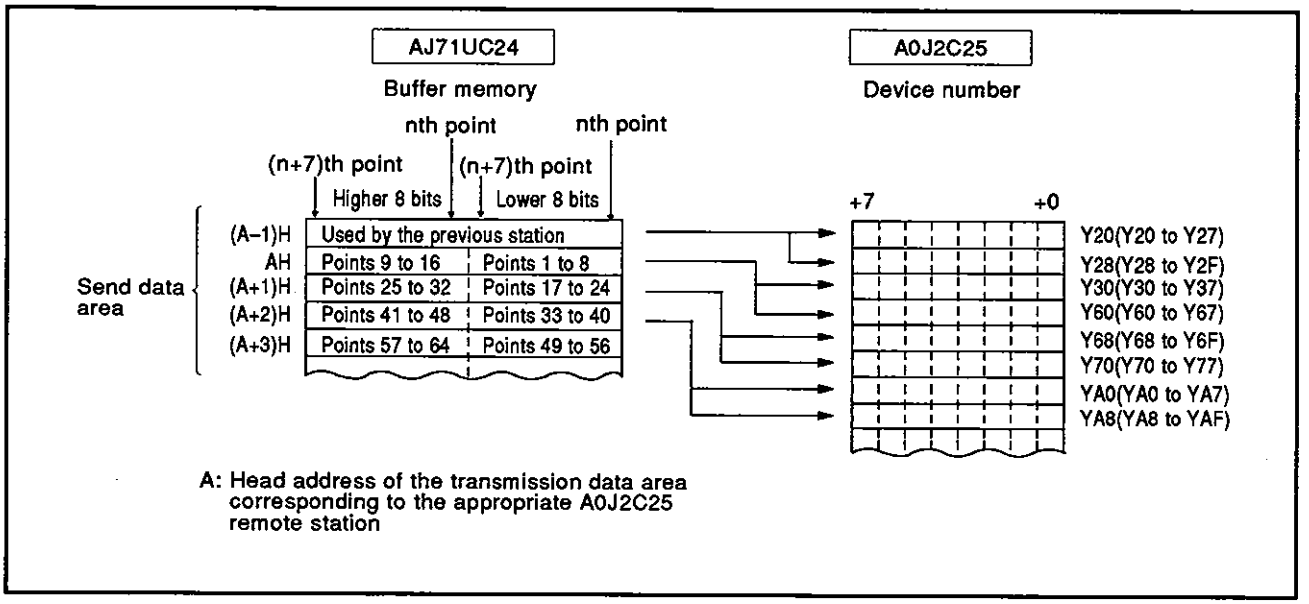
This section describes the data communication between the AJ71UC24 and slave stations (A0J2C25, AJ71UC24 (local station)) when the maximum number of transmission points is set at 512.

14.5.1 Communication with A0J2C25

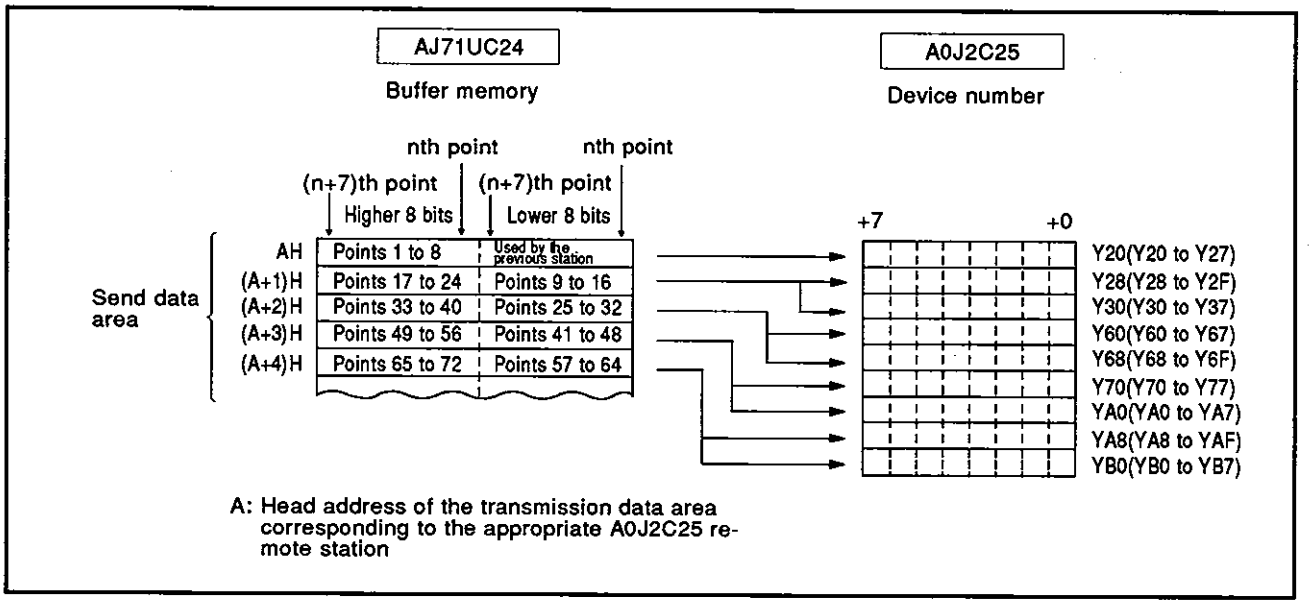
(1) Data transmission from AJ71UC24 to A0J2C25

Transmitted AJ71UC24 buffer bits correspond to A0J2C25 outputs (Y) as indicated below:

(a) When the previous station uses higher 8 bits



(b) When the previous station uses only the lower 8 bits



(c) Writing ON/OFF data to the relevant AJ71UC24 buffer transmission data bits switches the corresponding A0J2C25 outputs (Y) on or off.

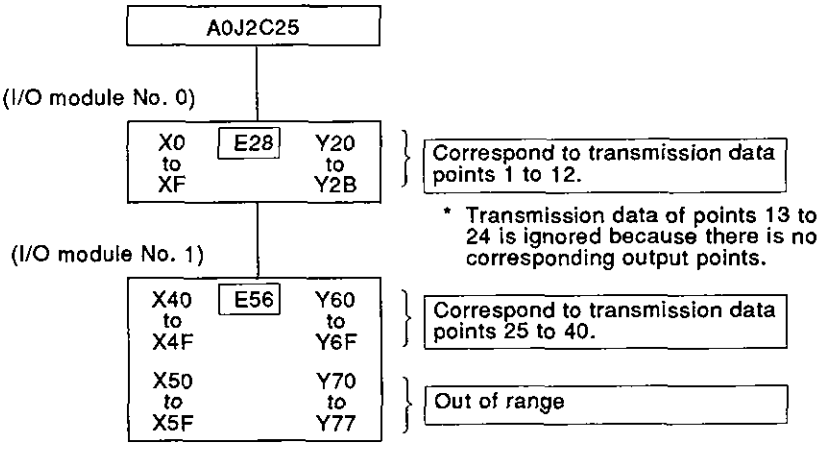
(e.g. if "1" is written to bit 0 of address AH in the condition (a), or if "1" is written to bit 8 of address AH in the condition (b), Y20 at the A0J2C25 is switched on.)

POINT

The number of I/O points of I/O modules (A0J2-E56[ ][ ], E28[ ][ ], E32[ ], E24[ ]) connected to the A0J2C25 is fixed to 32 input points and 24 output points per module regardless of the module type.

If a 28-point module is connected to the A0J2C25, the transmission data of the AJ71UC24 which corresponds to 14 output points of the second half is ignored. If an input module is connected to the A0J2C25, the transmission data of the AJ71UC24 which corresponds to 24 output points is ignored because there is no corresponding output points.

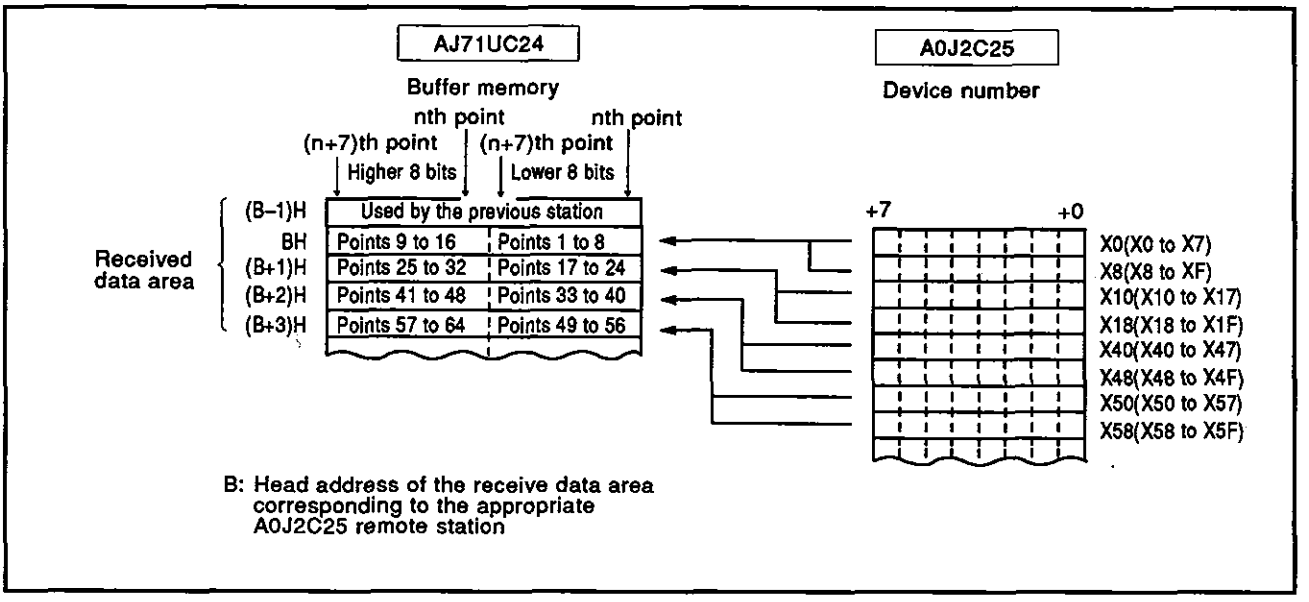
Example: When the number of transmission data points is set at 40 points in the system shown below.



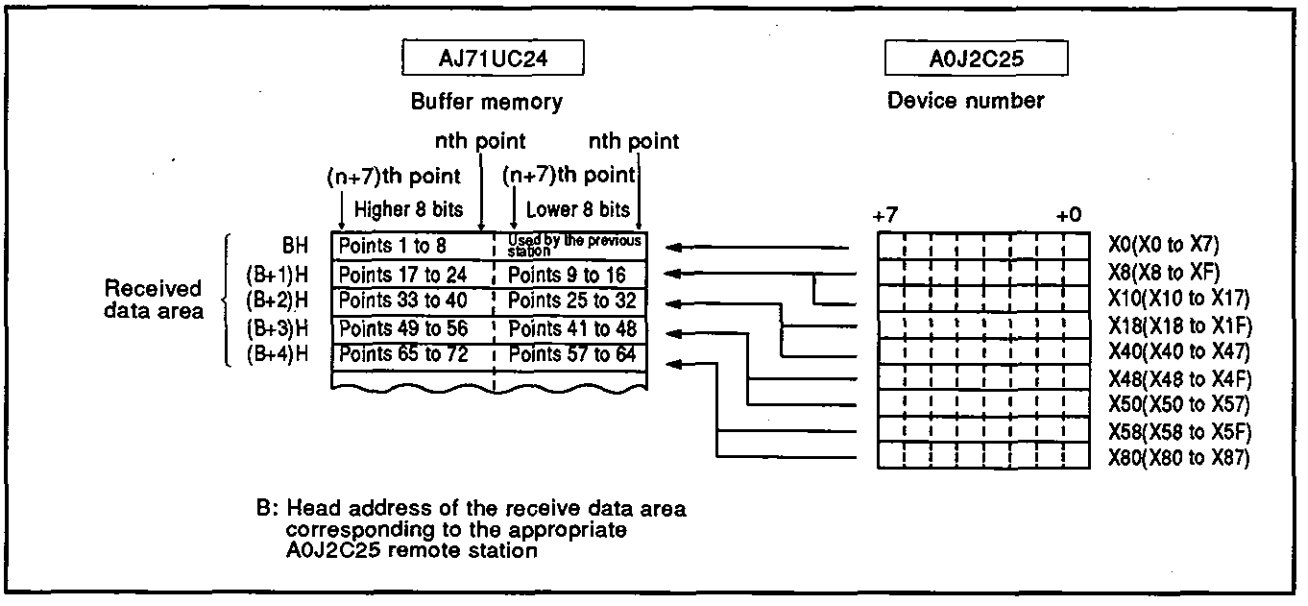
(2) Data received from A0J2C25 by AJ71UC24

Bits received by the AJ71UC24 buffer memory correspond to A0J2C25 inputs (X) as shown below:

(a) When the previous station uses higher 8 bits



(b) When the previous station uses only the lower 8 bits



(c) Writing ON/OFF data to the relevant AJ71UC24 buffer transmission data bits switches the corresponding A0J2C25 outputs (Y) on or off.

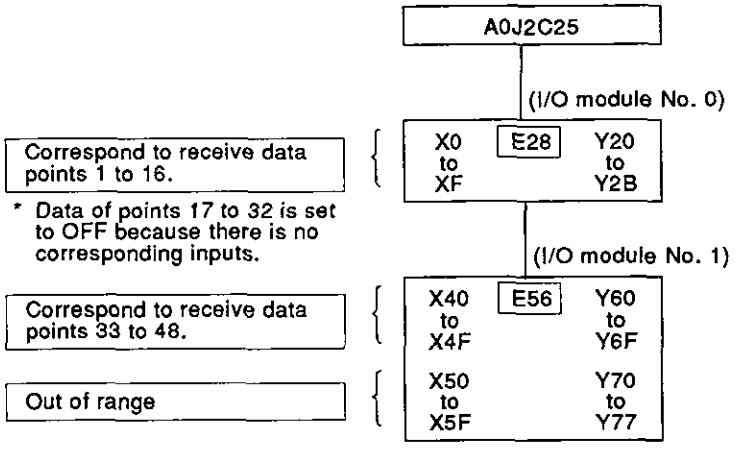
(e.g. when X1 at the A0J2C25 is switched ON, "1" is written to bit 1 of address BH of the AJ71UC24 in the condition (a), or to bit 9 of address BH in the condition (b).)

POINT

The number of I/O points of I/O modules (A0J2-E56[ ][ ], E28[ ][ ], E32[ ], E24[ ]) connected to the A0J2C25 is fixed to 32 input points and 24 output points per module regardless of the module type.

If a 28-point module is connected to the A0J2C25, the data received by the AJ71UC24 which corresponds to 16 input points of the second half is set to OFF ("0"). If an output module is connected to the A0J2C25, the data received by the AJ71UC24 which corresponds to 32 input points is set to OFF ("0") because there is no corresponding input signals.

Example: When the number of receive data points is set at 48 points in the system shown below:

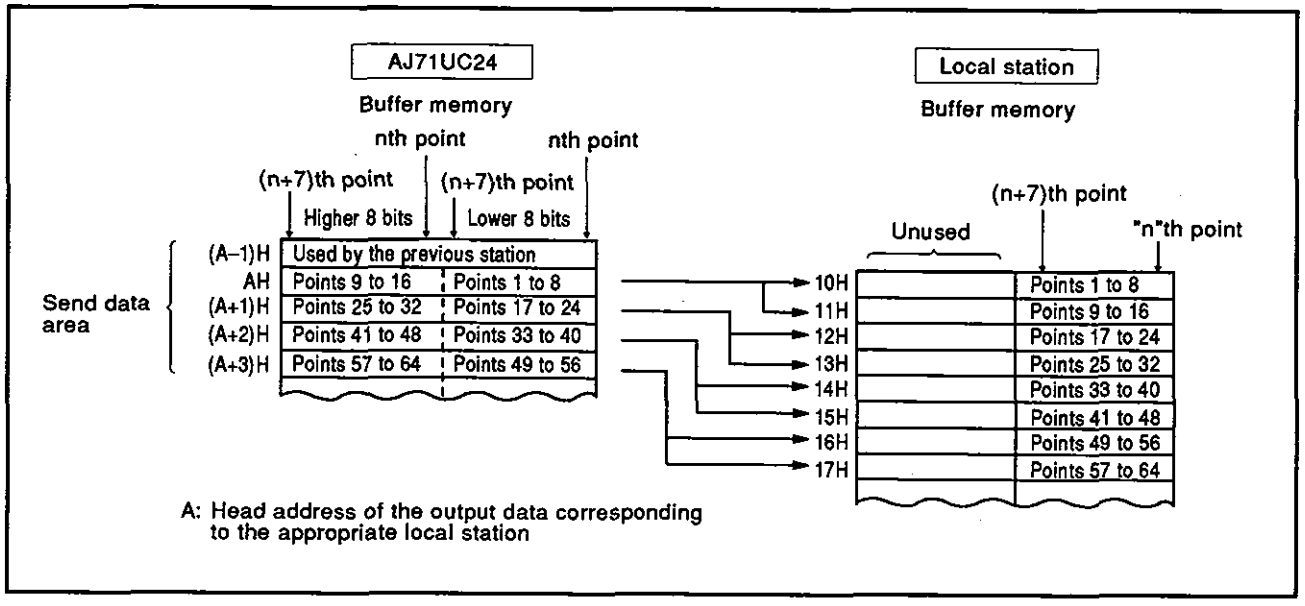


14.5.2 Communication with local station (AJ71UC24)

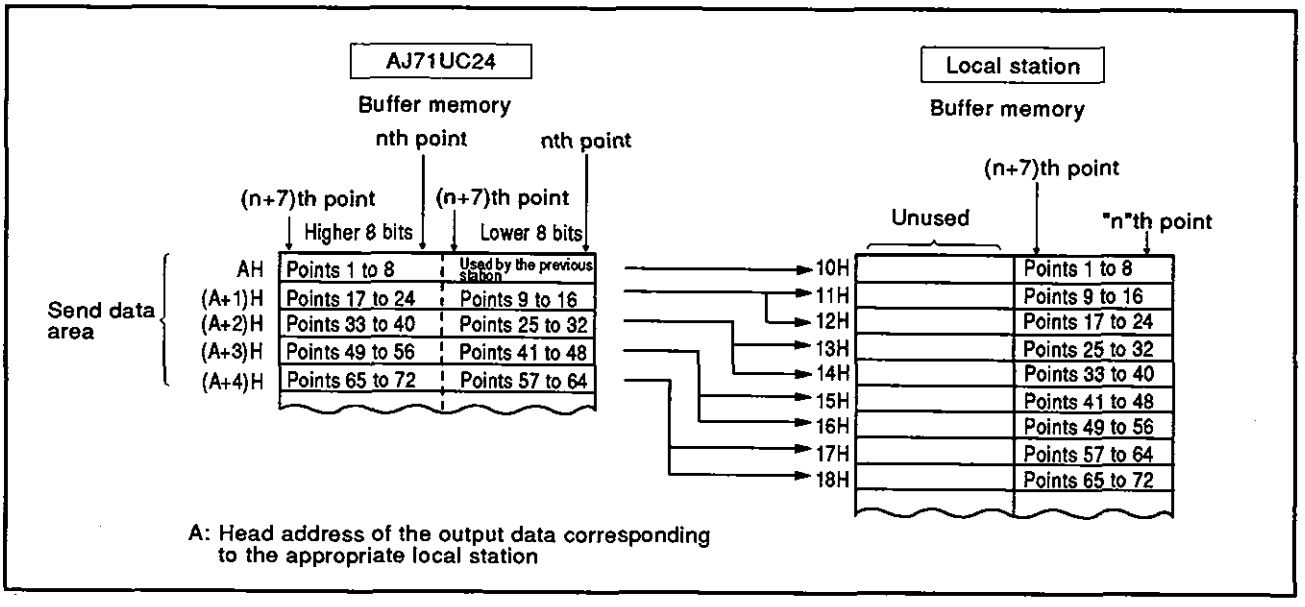
(1) Data output from master to local station

For data transmission from the master to the local station, master buffer bits correspond to local buffer bits as illustrated below.

(a) When the previous station uses higher 8 bits



(b) When the previous station uses only the lower 8 bits



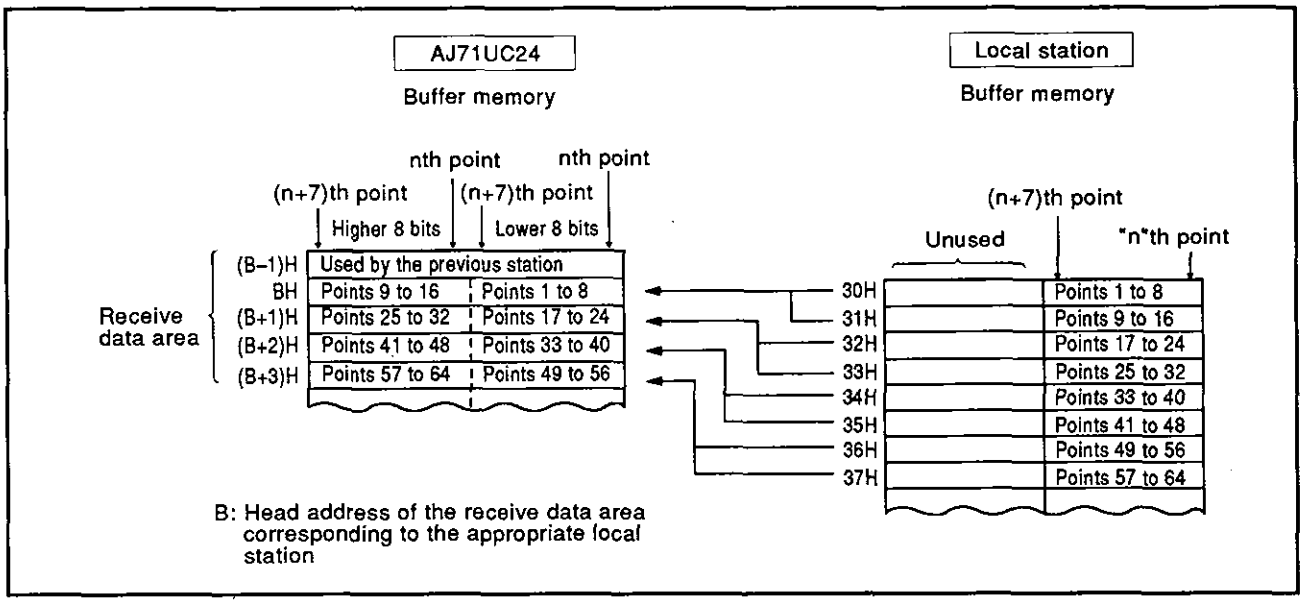
(c) Writing ON/OFF data to master buffer bits switches the corresponding local buffer bits on/off.

(e.g. "1" is written to bit 0 of address AH in the condition (a), or if "1" is written to bit 8 of address AH in the condition (b), bit 0 (point 1) of address 10H at the local station is set to "1".)

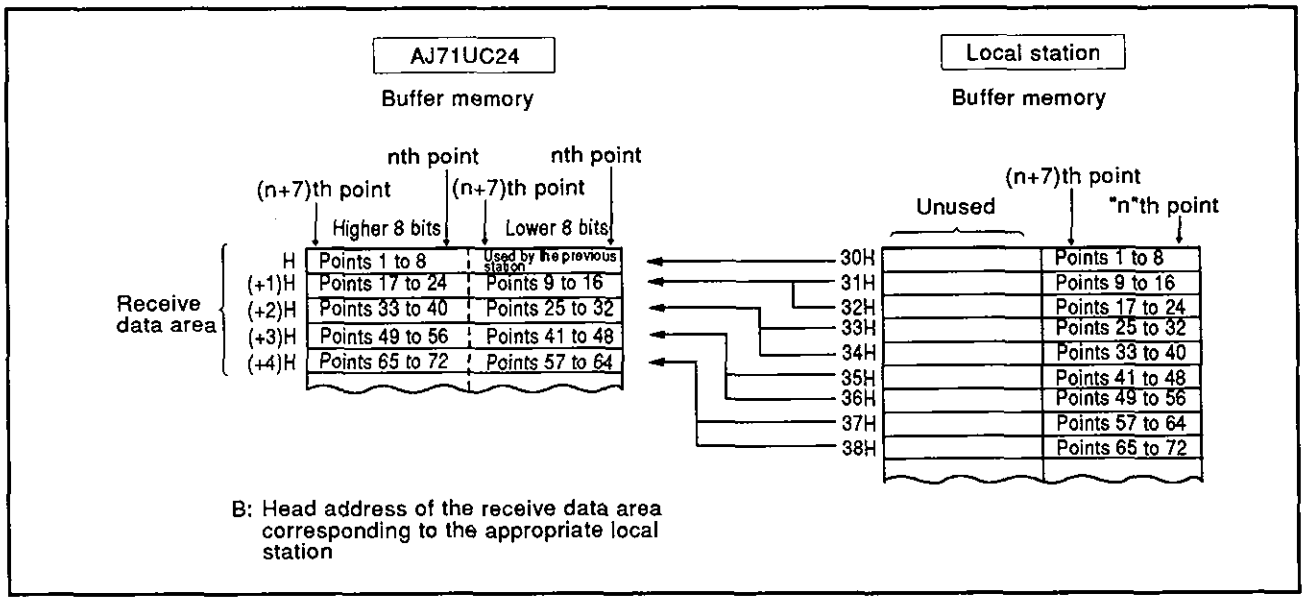
(2) Data input from the local to the master station

When receiving data from the local station, the master buffer bits correspond to the local buffer bits as shown below.

(a) When the previous station uses higher 8 bits



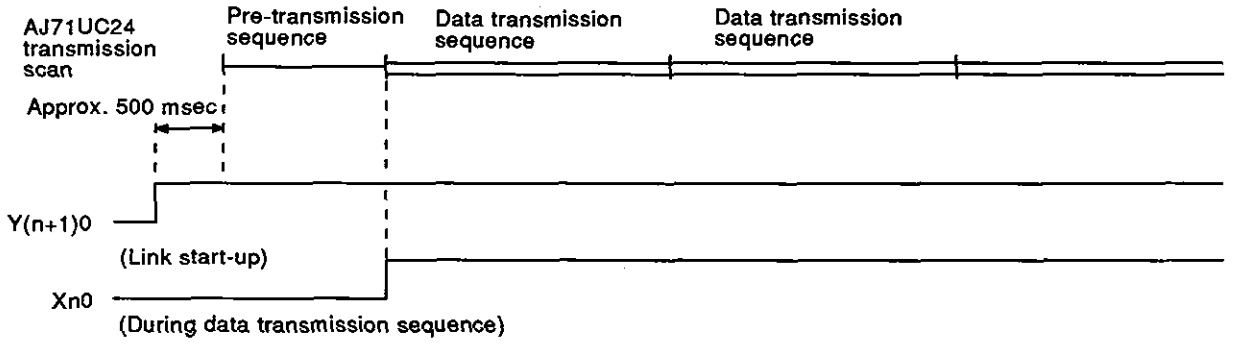
(b) When the previous station uses only the lower 8 bits



(c) Writing ON/OFF data to local buffer bits switches the corresponding master buffer bits on/off.

(e.g. if "1" is written to bit 1 (point 2) of address 30H at the local station, bit 1 (point 2) of address BH at the master station in the condition (a), or bit 9 of address BH at the master station in the condition (b) is set to "1".)

14.6 AJ71UC24 Control



(1) Approximately 500 msec after Y(n+1)0 is switched on, the pre-transmission sequence checks the link status and I/O points.

(2) The pre-transmission sequence is for the processing which confirms connection with slave stations, number of I/O points, etc.

(3) When the pre-transmission checks are complete, the data transmission sequence is started automatically and Xn0 is switched on. I/O data communication cycles are repeated between the master and slave stations in the order specified for the transmission priority.

Xn0 should be used as an interlock in the sequence program to prevent buffer memory transactions from being processed during the data transmission sequence.

(4) The data transmission sequence is for the I/O data send/receive processing with slave stations. Data communication is executed with slave stations in the order specified for transmission priority. After completing data transmission with all the set slave stations, data communication is executed with the first slave station. Data communication is repeated cyclically in this manner.

14.7 Error Control

14.7.1 Pre-transmission error processing

(1) Any error which occurs during the pre-transmission sequence, will cause communication with all slave stations to be stopped and:

(a) AJ71UC24 Xn1 turns on;

(b) "L2" LED on the AJ71UC24 front is lit;

(c) The error code is written to buffer address 60H.

(For error codes, see Sections 6.1 and 6.2)

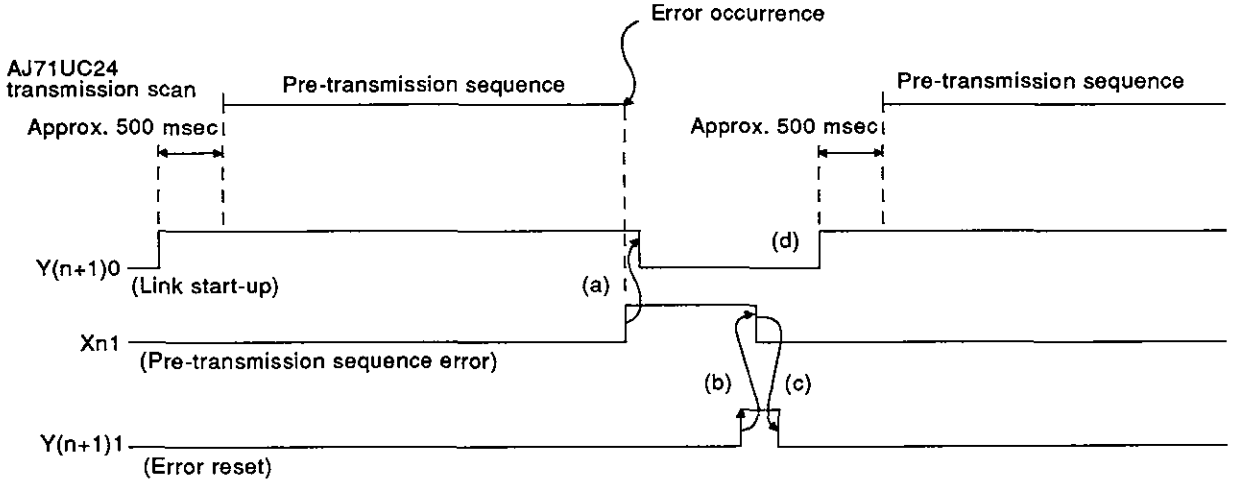
(2) Restart the pre-transmission sequence:

(a) Switch on Y(n+1)1 in the sequence program to reset the error.

(Xn1 turns off automatically.)

(b) Switch on Y(n+1)0 in the sequence program.

(3) Sequence error and restart control timing chart



(a) Switch on Xn1 to reset Y(n+1)0 (in the sequence program).

(b) Switch on Y(n+1)1 in the sequence program, Xn1 automatically switches off.

(c) When Xn1 turns off, Y(n+1)1 is switched off in the sequence program.

(d) Switch on Y(n+1)0 in the sequence program, to restart the pre-transmission sequence.

14.7.2 Data transmission error processing

Any error which occurs during the data transmission sequence, will have one of the following effects: the faulty station may be disconnected from the network for continued link operation or communication between all stations may be stopped (depends on SW22 setting) and:

(1) 1 (master): 1 (slave) ratio and SW22 off

(a) Xn2 switches on and Xn0 off.

(b) The "L1" LED on the AJ71UC24 front turns off and the "L3" LED is lit.

(c) The error code is written to buffer address 60H.

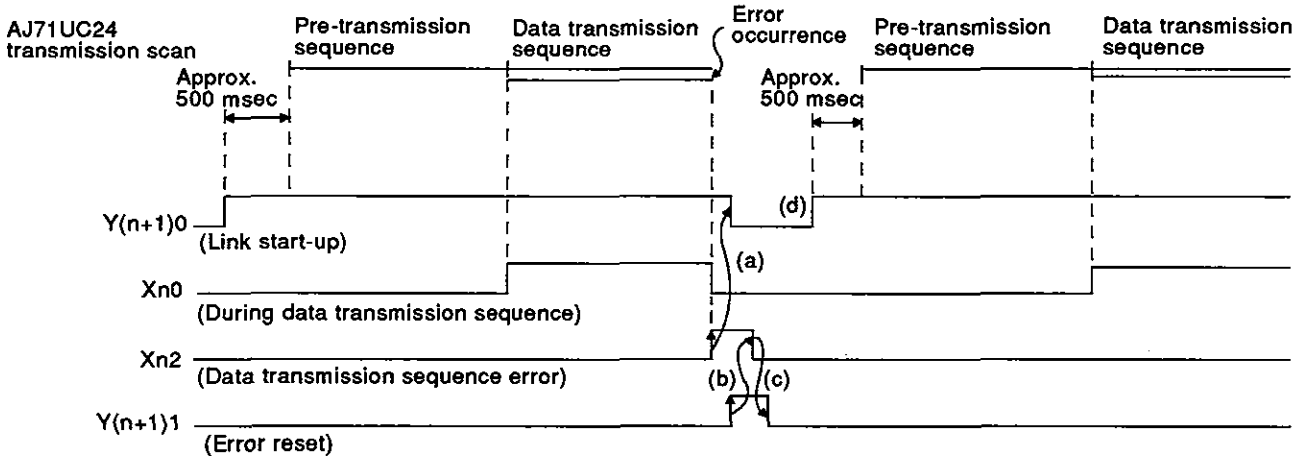
(2) Restart the data transmission sequence:

(a) Switch on Y(n+1)1 in the sequence program to reset the error.

(Xn2 turns off automatically.)

(b) Switch on Y(n+1)0 in the sequence program to execute the pre-transmission sequence.

(3) Sequence error and restart control timing chart



(a) Switch Xn2 on, to switch off Y(n+1)0 (in the sequence program).

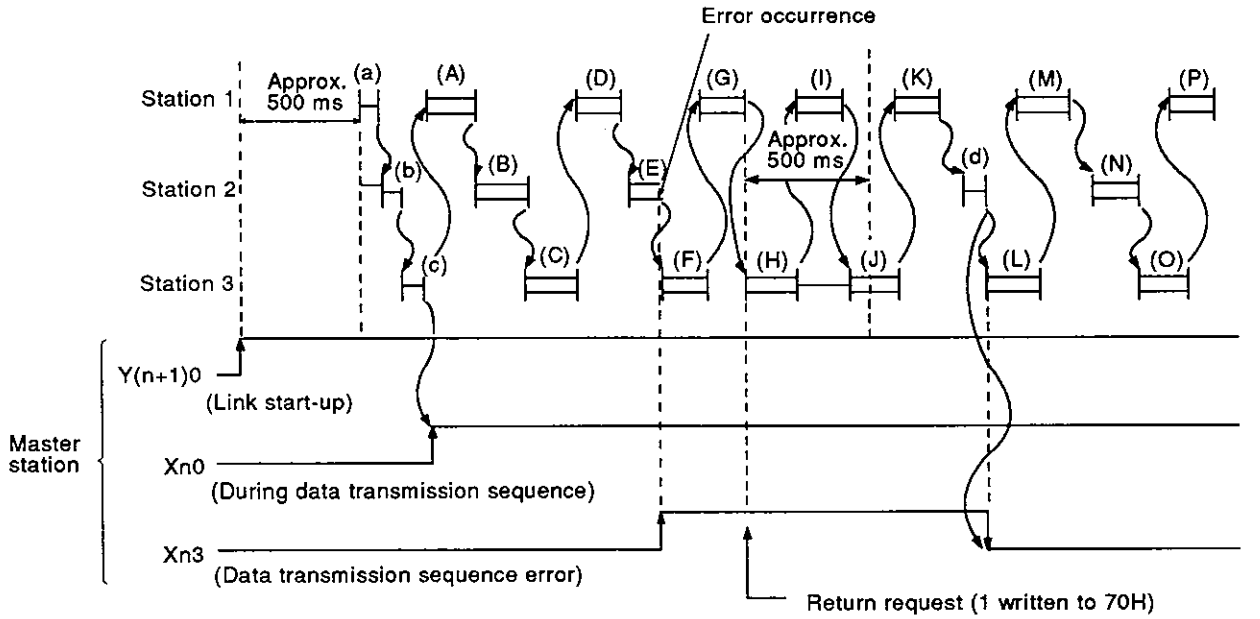
(b) Switch on Y(n+1)1 in the sequence program, Xn2 switches off automatically.

(c) When Xn2 turns off, Y(n+1)1 is turned off in the sequence program.

(d) Switch on Y(n+1)0 in the sequence program, to restart the pre-transmission sequence.

(4) 1 (master): n (slave) ratio and SW22 on

(3 slave stations in the following chart)



- About 500 ms after Y(n+1)0 switches on, the pre-transmission sequence is started at station 1 ((a)). ((a) → (b) → (c))
- After completion of the pre-transmission at the final station, the data transmission sequence is commenced at station 1 ((A)).
- For an error occurring at station 2 ((E)) during the data transmission sequence, the handshake signals between the AJ71UC24 (master) and PC CPU and the data between the master and slave stations are transferred as follows:

  1) When the error occurs, Xn3 turns on and the "L6" LED is lit.

  2) The data transmission sequence is stopped at station 2 and initiated at station 3.

     This sequence is executed at stations 1 and 3 until station 2 returns to the link system.

  3) To return station 2 to the link system after the error is removed, "1" must be written to the appropriate bit of buffer address 70H in the sequence program.

     The pre-transmission sequence is executed during the first communication with Station 2 at about 500 msec after a return request was issued.

     When the pre-transmission sequence is complete at station 2, Xn3 and the "L6" LED automatically switch off.

14.8 Off-communication Control

The following describes the control processings when a slave station (A0J2C25, AJ71UC24 (local station), manifold serial transfer device) is set to off-communication state by the master station.

(1) Control processings in off-communication state

(a) Setting and cancel of off-communication

Off-communication state is set by writing "1" or canceled by writing "0" to a bit which corresponds to a target slave station at address 1FH of buffer memory.

(Refer to Section 14.3 for detail of buffer memory.)

(b) Transmission data in off-communication state

1) Send data

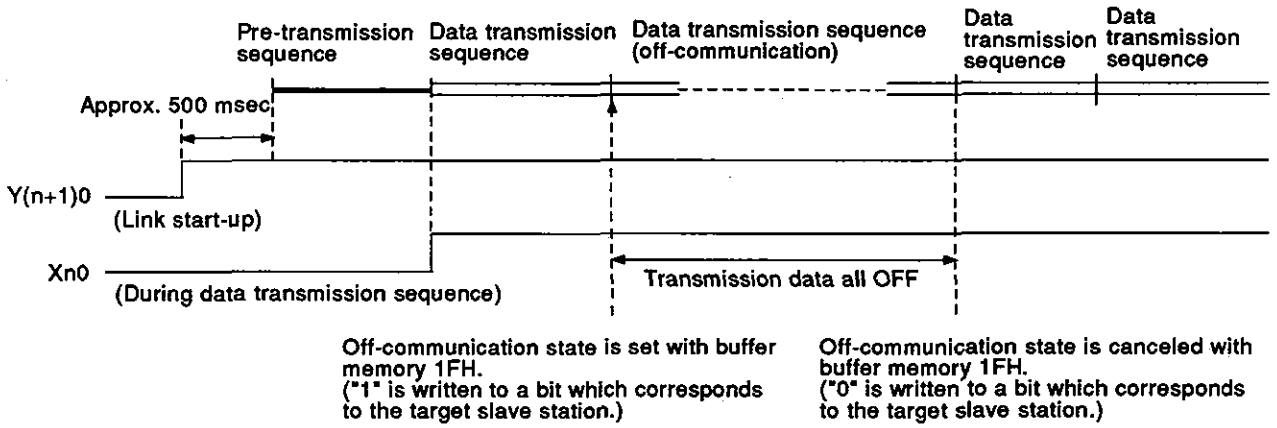
OFF data is sent to an off-communication station regardless of data in the send data area which corresponds to the off-communication station.

2) Receive data

OFF data ("0") is written to the receive data area which corresponds to the off-communication station regardless of data received from the slave (off-communication) station.

(c) Timing chart

The following is the timing chart of control processings in off-communication state.



(2) Control processings when an error occurs in off-communication state

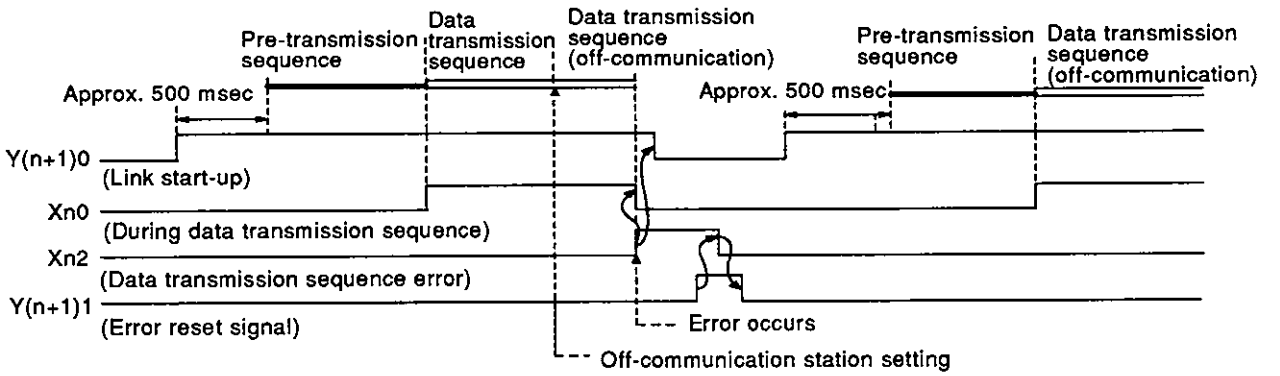
Control processings when an error occurs in off-communication state differ according to link process setting ("STOP" (SW22 OFF) or "CONTINUE" (SW22 ON)) when an error occurs at a slave station, as described below:

(a) When link process setting when an error occurs at a slave station is "STOP"

When an error occurs at a slave station or an off-communication station, the master station suspends the data transmission sequence.

When the link start-up signal is given after the error reset, the pre-transmission sequence starts after 500 msec, and then, the data transmission sequence starts restoring off-communication state.

The following is the timing chart of the control processings.



REMARK

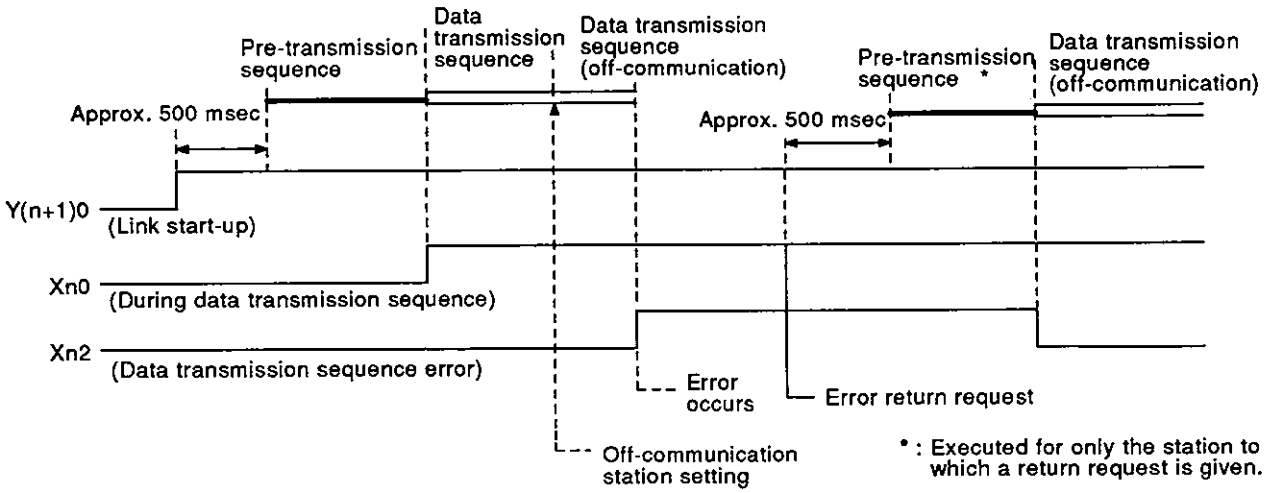
The off-communication setting is not cleared by error occurrence (Xn2 ON) or error reset (Y(n+1)1 ON).

(b) When link process setting when an error occurs at a slave station is "CONTINUE"

When an error occurs at an off-communication station, the master station suspends communication with the station.

When an error return request signal is given, the pre-transmission sequence starts, and then, off-communication state is restored.

The following is the timing chart of the control processings:



14.9 Transmission Delay Time

During transmission between the AJ71UC24 and a slave station, there is a delay until one receives data from the other.

The delay time per station may be found from the following expression.

When there are more than one slave station, add the delay times for each station.

$$\text{Delay time} = \left(\frac{X}{8}\right) \times 0.74 + \left(\frac{Y}{8}\right) \times 0.86 + 6.1 \text{ [msec]}$$

where X = number of points input from a corresponding station

Y = number of points output to a corresponding station

14.10 Transmission Stop Detection Time

(1) Slave stations detect a AJ71UC24 transmission stop in the order set as the transmission priority, starting at the slave station next to the one that made the final communication with the AJ71UC24.

For example, if the AJ71UC24 stops transmission during communication with station 3 and the transmission priority is set as 5, 2, 3, 1, 7, the order in which the slave stations detect the stopped transmission is 1, 7, 5, 2, 3.

(2) Times required to detect stopped transmission:

(a) For the first detecting station

Max. 500 msec after the AJ71UC24 stops transmission

(b) For other slave stations

$$\frac{10}{\text{Transmission speed (19.2/38.4)}} \times \left(6 + \frac{X+Y}{4}\right) + 2 \text{ [msec]}$$

where X = number of input points at the preceding station

Y = number of output points at the preceding station

POINTS

(1) The A0J2C25 switches all outputs off when a stop in transmission is detected.

(2) The AJ71UC24 buffer memory retains data after the transmission stop.

(3) The A0J2CPU can detect a AJ71UC24 transmission stop from the ON/OFF status of Xn0, Xn1 and Xn2. (For I/O unit number 0)

14.11 Programming

14.11.1 Notes on programming

(1) The AJ71UC24 buffer memory data is initialized by:

(a) Resetting the PC CPU; or

(b) Switching the PC power off then on

(2) The initial data in the buffer memory is written to the AJ71UC24 operating system (OS) when Y(n+1)0 switches on.

Hence data at buffer addresses 0H to 18H cannot be rewritten during the pre-transmission or data transmission sequence.

(3) For transmission delays between the PC CPU and slave stations, see Section 14.9.

(4) For details on the use of the FROM and TO instructions for data communication with the PC CPU, see the Programming Manual.

14.11.2 Initial data write

See Section 14.3 for buffer memory addresses.

PROGRAM CONDITIONS

(1) AJ71UC24 I/O unit number = 0 ..... X00 to X1F, Y00 to Y1F

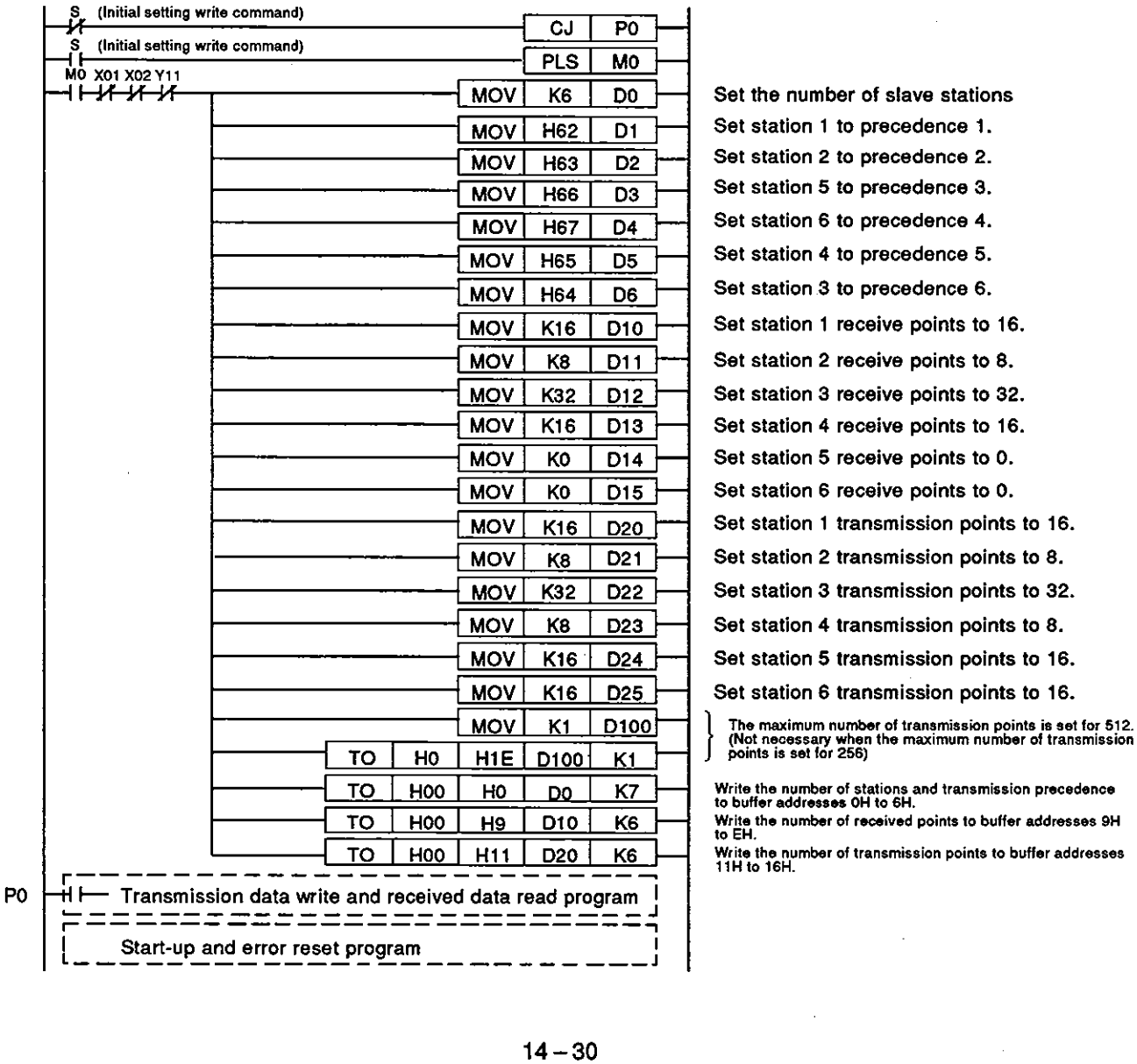
(2) Number of slave stations 6

(3) Transmission precedence ..... Stations 1, 2, 5, 6, 4, 3

(4) Transferred points .....

	Station 1	Station 2	Station 3	Station 4	Station 5	Station 6
Received points	16	8	32	16	0	0
Transmission points	16	8	32	8	16	16

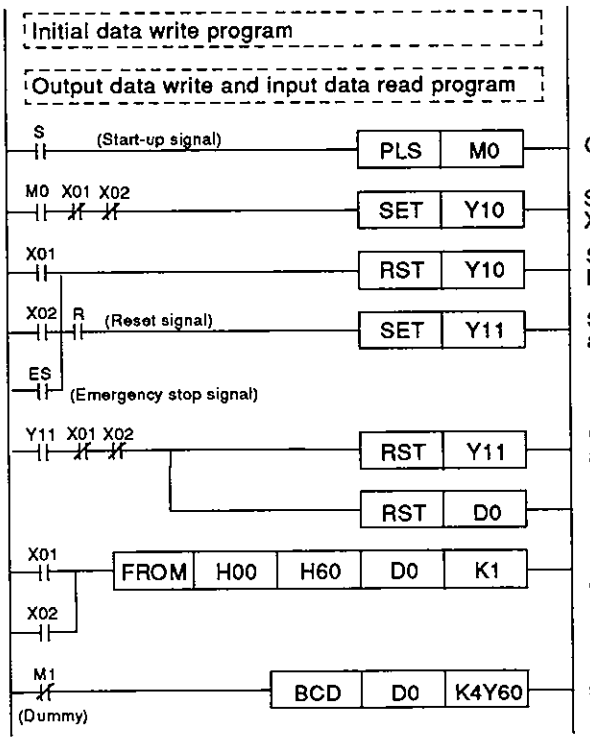
PROGRAM EXAMPLE



14.11.3 Start-up and error reset

Assume the AJ71UC24 I/O numbers to be X00 to X1F, Y00 to Y1F.

(1) When link process setting when an error occurs at a slave station is "STOP"



Convert start-up signal into pulse.

Switch Y10 on to start up providing error flags X01 and X02 are off.

Switch Y10 off to stop start-up if an error has occurred or emergency stop signal turned on.

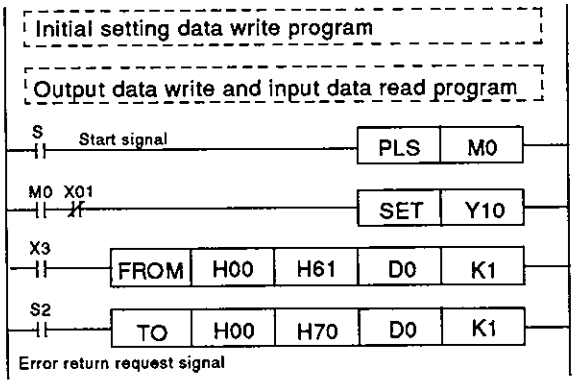
Switch R on after error removal to turn Y11 on and reset the error.

Check that X01 or X02 has switched off and turn off Y11.

Read the error code to buffer address 60H at error occurrence.

Indicate the error code.

(2) When link process setting when an error occurs at a slave station is "CONTINUE"



The start signal is changed into a pulse.

If either of error signals X01 and X02 is not ON, Y10 is turned ON to start.

When X3 is turned on indicating the occurrence of a faulty slave station, the faulty station number is read to D0.

After the faulty station is recovered, the error return request is issued.

14.11.4 Transmission data write

PROGRAM CONDITIONS

(1) AJ71UC24 I/O addresses ..... X00 to X1F, Y00 to Y1F

(2) Number of slave stations 3

(3) Number of outputs.....

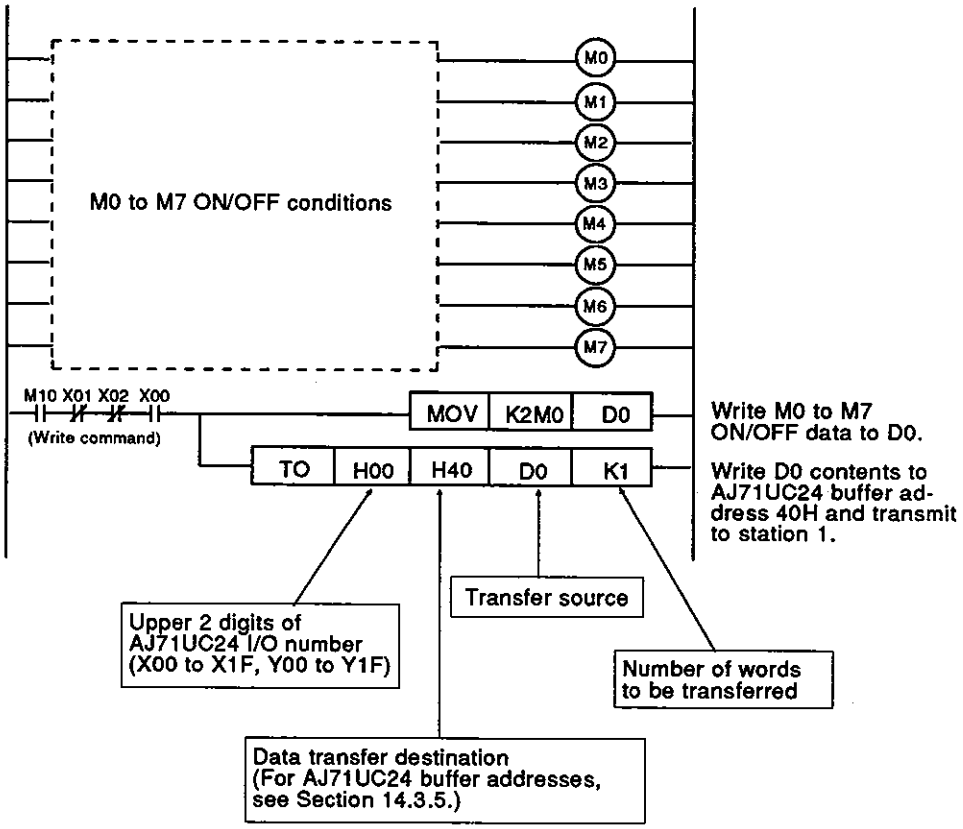
	Station 1	Station 2	Station 3
Points	8	16	8

(4) Max. number of transmission points 256

(5) M0 to M7 ON/OFF data is echoed at the 1st to 8th output devices in station 1.

PROGRAM EXAMPLE

To control the ON/OFF statuses of outputs at station 1



EXPLANATION

(1) Data is written to the specified buffer memory addresses in the AJ71UC24 by the TO instruction and is then automatically transmitted from the AJ71UC24 to slave stations.

(2) Data transmitted to stations 1 to 3 is written to the following AJ71UC24 buffer addresses:

	Maximum Number of Transmission Points: 256	Maximum Number of Transmission Points: 512
Send data of points 1 to 8 of station 1	Lower 8 bits of address 40H	Lower 8 bits of address 40H
Send data of points 1 to 8 of station 2	Lower 8 bits of address 41H	Higher 8 bits of address 40H
Send data of points 9 to 16 of station 2	Lower 8 bits of address 42H	Lower 8 bits of address 41H
Send data of points 1 to 8 of station 3	Lower 8 bits of address 43H	Higher 8 bits of address 41H

IMPORTANT

The data store procedure of the send data area differs according to the setting of the maximum number of transmission points (256 or 512).

When the maximum number of transmission points is set at 512, and, if the TO instruction is executed every 8 bits as shown by M0 to M7 in the example, "0" (OFF) is written to all of higher 8 bits.

When the maximum number of transmission points is set at 512, data transmission should be executed in units of 16 bits (1 word).

14.11.5 Received data read

PROGRAM CONDITIONS

(1) AJ71UC24 I/O addresses .....X00 to X10, Y00 to Y10

(2) Number of slave stations 3

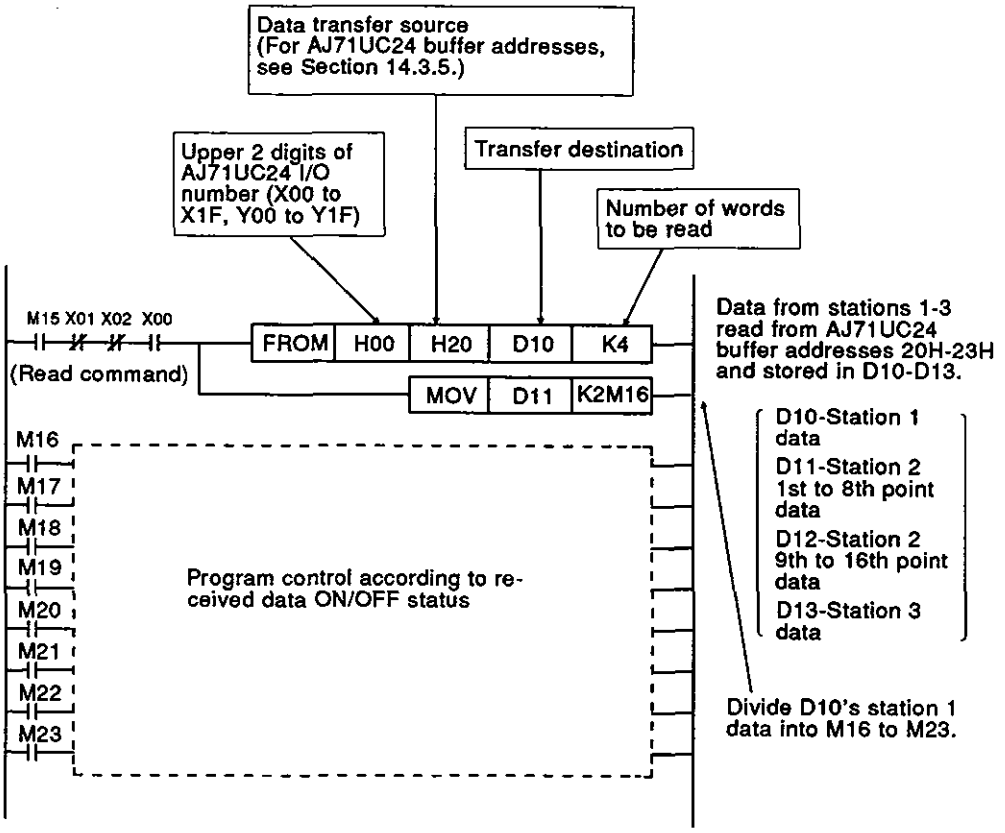
(3) Number of outputs.....

	Station 1	Station 2	Station 3
Points	8	16	8

(4) The ON/OFF statuses of 8 bits are read from station 2 to M16 to M23 in the CPU.

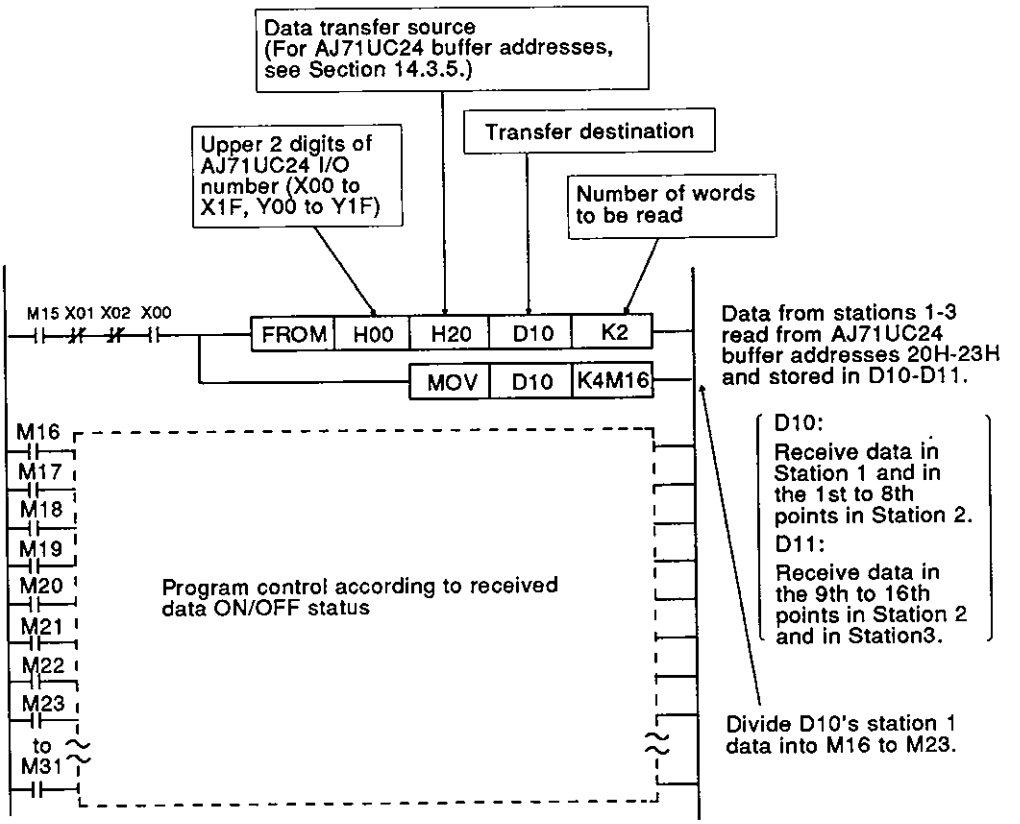
Program example:When the maximum number of transmission points is set at 256

To detect and control each point of received ON/OFF data.



Program example:When the maximum number of transmission points is set at 512

To detect and control each point of received ON/OFF data.



EXPLANATION

(1) Data is automatically received from slave stations and written to the specified buffer memory address in the AJ71UC24.

Reading received data from the AJ71UC24 buffer memory using the FROM instruction allows the received data ON/OFF status to be used in the sequence program.

(2) Data received from stations 1 to 3 is written to the following AJ71UC24 buffer addresses:

	Maximum Number of Transmission Points: 256	Maximum Number of Transmission Points: 512
Receive data of points 1 to 8 of station 1	Lower 8 bits of address 20H	Lower 8 bits of address 20H
Receive data of points 1 to 8 of station 2	Lower 8 bits of address 21H	Higher 8 bits of address 20H
Receive data of points 9 to 16 of station 2	Lower 8 bits of address 22H	Lower 8 bits of address 21H
Receive data of points 1 to 8 of station 3	Lower 8 bits of address 23H	Higher 8 bits of address 21H

IMPORTANT

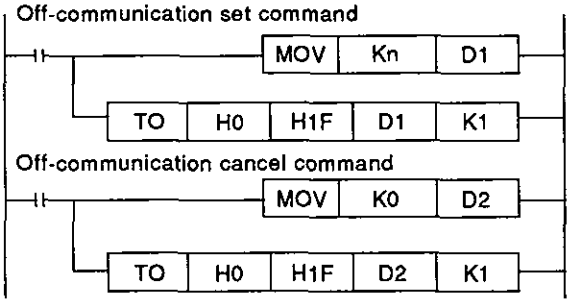
The data store procedure of the receive data area differs according to the setting of the maximum number of transmission points (256 or 512).

When the maximum number of transmission points is set at 512, read of higher 8 bits only of each address is disabled. It is necessary to prepare a program that executes the FROM instruction every word and then processes higher 8 bits only by use of the sequence program.

14.11.6 Off-communication station set/cancel program

The following is the example of a program used to set and cancel off-communication stations.

(The I/O numbers of the AJ71UC24 are X00 to X1F and Y00 Y1F.)



When the off-communication set command is turned ON, a bit which corresponds to the off-communication station is set to D1.

When data of D1 is written to buffer memory address 1FH, the station which corresponds to the bit of the address is set to off-communication state.

By writing "0", off-communication setting is canceled.

15. MULTIDROP LOCAL STATION

15.1 Functions

Item	Function	Ref. Section
Pre-transmission sequence	The AJ71UC24 receives initial data from the master and responds.	15.4
Data transmission sequence	After the pre-transmission sequence, the AJ71UC24 communicates with the master.	
Loopback self-check	RS422/485 port can be checked.	13.5

15.2 Input Signals List for PC CPU

Input device numbers depend on the AJ71UC24 I/O unit number.

The following device numbers assume that the I/O unit number has been set to 0.

Device Number	Signal Name	Description
Xn0	During data transmission sequence	• On indicates normal data transmission sequence. • Off indicates pre-transmission sequence or an error
Xn1	Pre-transmission sequence error	• On indicates an error during pre-transmission sequence. • Switched off when the pre-transmission sequence with the master is normalized.
Xn2	Data transmission sequence error	• On indicates an error during data transmission sequence. • Switched off when the pre-transmission sequence with the master is restored.
Xn3 to XnC	—	• Reserved
XnD	Watch dog timer (WDT) error	• Switched on when the AJ71UC24 WDT times out.
XnE XnF	—	• Reserved

IMPORTANT

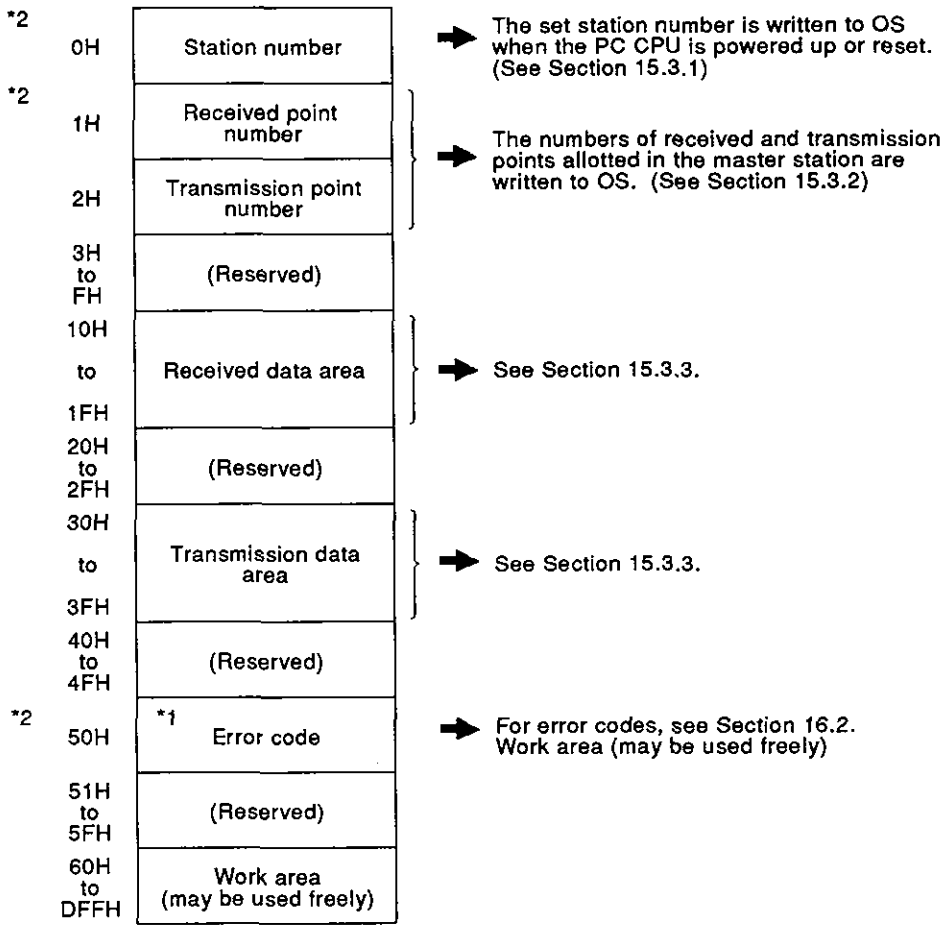
(1) Yn0 to YnF, which are unused by the AJ71UC24, may be used as internal relays.

(2) Y(n+1)0 to Y(n+1)F are reserved for the use by the system and cannot be used by sequence programs.
If any of these devices in used (ON/OFF) by a sequence program, correct operation of the AJ71UC24 are not guaranteed.

15.3 Buffer Memory

The AJ71UC24 has a buffer memory for data communication with the PC CPU. For data transfer between the PC CPU and buffer memory, use the FROM and TO instructions.

Buffer addresses are 16 bit locations.



POINTS

*1: Error codes (address 50H) must be removed from the buffer memory by resetting the PC.

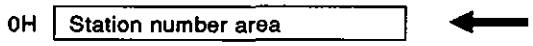
Codes are not cleared when the cause of the error is removed.

The error code in address 50H is always the most recent one.

*2: Do not write data to the OS control areas.

15.3.1 Station number

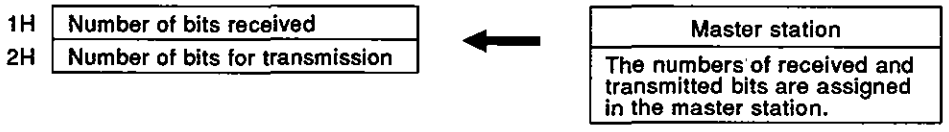
The station numbers are converted into fixed codes and are written to this area when the PC CPU is powered up or reset.



	Fixed Code
Station 1	62H
Station 2	63H
Station 3	64H
Station 4	65H
Station 5	66H
Station 6	67H
Station 7	68H
Station 8	69H

15.3.2 Number of bits received/transmitted

The numbers of received and transmitted bits assigned by the master station are written to their respective areas on completion of the pre-transmission sequence.



POINT

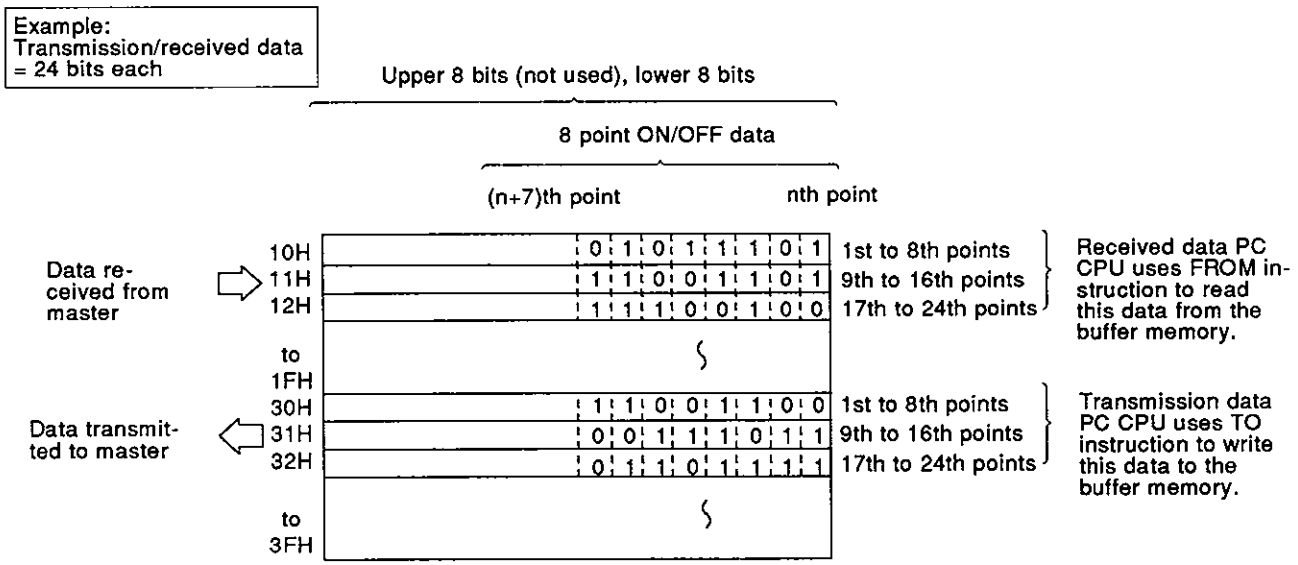
This data is written automatically from the master station.

Do not write data to the station number and received/transmitted point number areas.

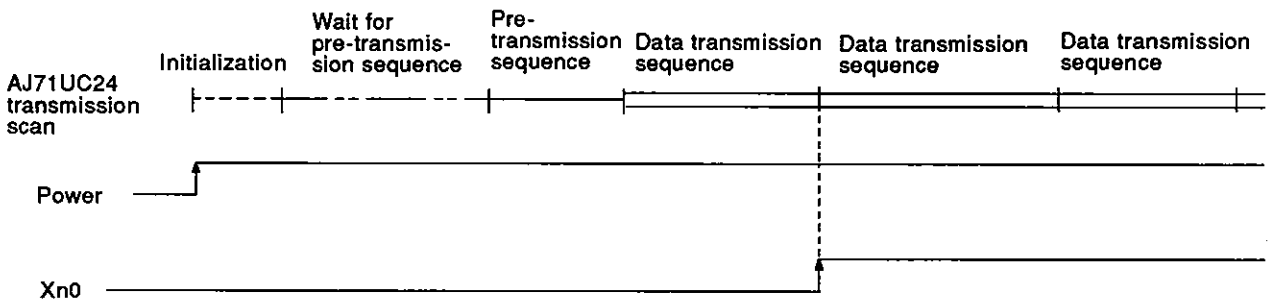
15.3.3 Communication data

Communication data between the master and slave stations is written to the lower 8 bits of buffer address 10H to 3FH.

The received data is written to the received data area and data for transmission must be written to the transmission data area from the sequence program as illustrated below.



15.4 AJ71UC24 Control



(1) Pre-transmission sequence

When the power is switched on, the AJ71UC24 is initialized and waits for the pre-transmission sequence from the master station.

(2) During the pre-transmission sequence, the local AJ71UC24 confirms the link status and I/O points.

(3) Data transmission sequence

When the pre-transmission checks are complete, the data transmission sequence is started automatically.

After the first transmission sequence is finished, Xn0 is switched on (Assuming that the I/O unit number is 0).

The transfer of data between the PC CPU and AJ71UC24 buffer must be started in the sequence program after Xn0 switches on.

(4) When the master AJ71UC24 is connected to several slaves, Xn0 is switched on after completion of the first data transmission sequence.

15.5 Error Control

15.5.1 Pre-transmission error processing

(1) Any error which occurs during the pre-transmission sequence, will cause transmission to the master station to be stopped and:

(a) AJ71UC24 Xn1 switches on;

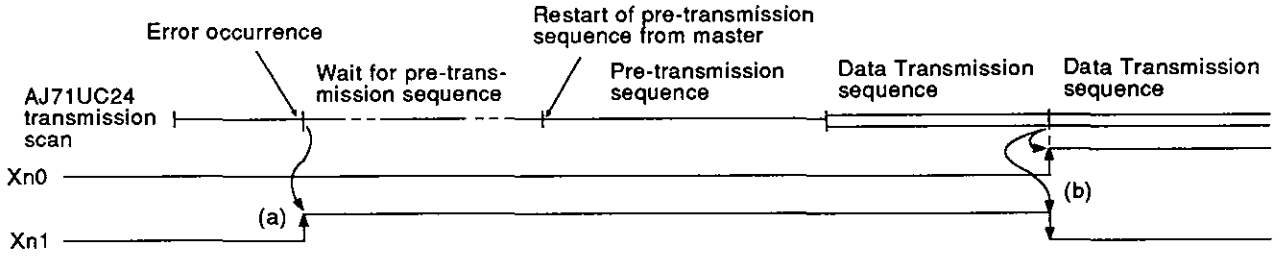
(b) "L2" LED on the AJ71UC24 front is lit;

(c) The error code is written to buffer address 50H.

(For error codes, see Section 16.2)

(2) Sequence restart is controlled by the master after the error is removed.

(3) Sequence error control timing chart



(a) The error switches Xn1 on.

(b) After the pre-transmission sequence is completed without fault. Xn1 switches off automatically.

15.5.2 Data transmission error processing

(1) Any error which occurs during the data transmission sequence, will cause communication with the master station to be stopped, and:

(a) Xn2 switches on.

(b) The "L2" LED on the AJ71UC24 front is lit.

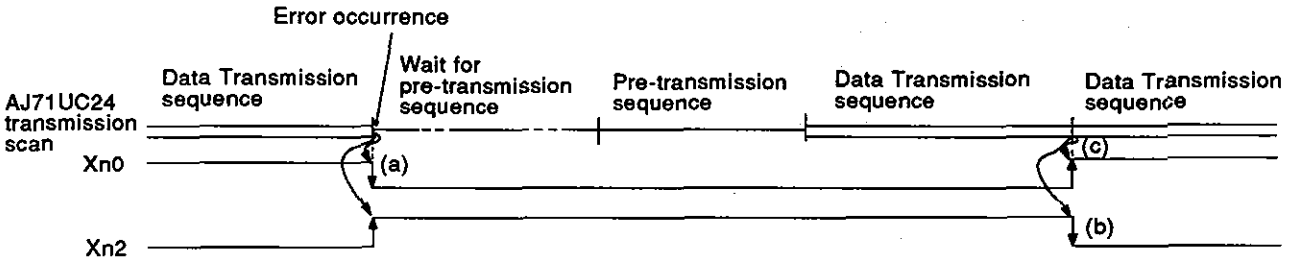
(c) The error code is written to buffer address 50H.

(For error codes, see Section 16.2)

(2) Sequence restart is controlled by the master after the error is removed.

(3) Sequence error control timing chart.

(a) 1 (master): 1 (slave) ratio and SW22 off



1) The error switches Xn0 off and Xn2 on.

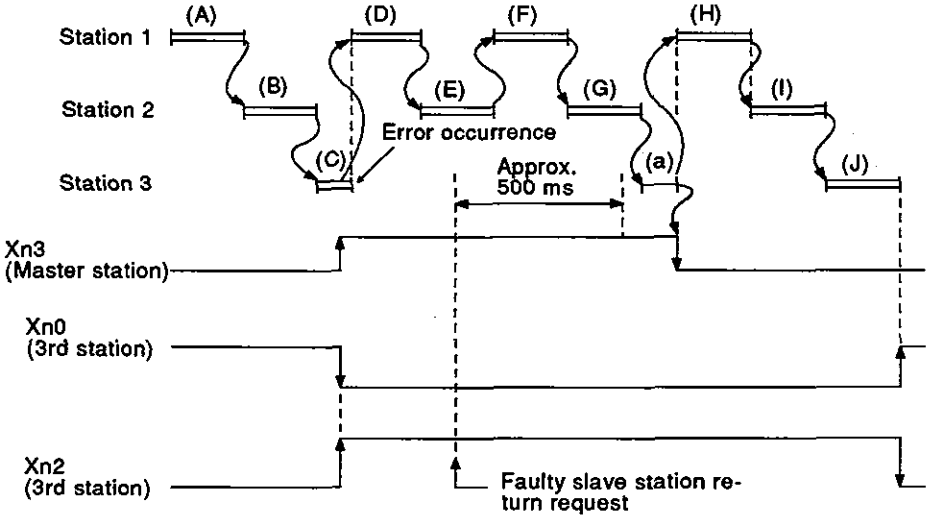
2) Xn2 automatically switches off on normal completion of the re-started pre-transmission sequence.

3) Xn0 switches on after completion of the first restarted data transmission sequence.

POINT

When an error occurs during the data transmission sequence, the received data area is not cleared.

(b) AJ71UC24 as local station n and master station SW22 on (n = 3)



- If an error occurs during the data transmission sequence ((C)) with station 3, the master station stops communication with station 3 and initiates the data transmission sequence with station 1 ((D)). Approx. 500 ms after the return request is given from the master station, the pre-transmission sequence is initiated at station 3. If this is completed without fault, then the data transmission sequence ((J)) is restarted.

1) The error switches Xn0 off and Xn2 on.

2) Xn0 switches on, Xn2 switches off when the data transmission sequence is completed ((J)) after the pre-transmission sequence at station 3.

15.6 Programming

15.6.1 Notes on programming

(1) The AJ71UC24 buffer memory data is initialized by:

(a) Resetting the PC CPU; or

(b) Switching the PC power off then on.

(2) The initial data (0H to 2H) in the buffer memory is written to the AJ71UC24 OS during the pre-transmission sequence.

(3) Hence data at buffer addresses 0H to 3H should not be rewritten during the pre-transmission or data transmission sequence.

(4) The PC CPU for transmission delays between the PC CPU and master station, see Section 14.9.

(5) The PC CPU for details on the use of the FROM and TO instructions for data communication with the PC CPU, see the Programming Manual.

(6) When the maximum number of transmission pints of the master station is set at either 256 or 512, a program used with local stations does not change.

15.6.2 Transmission data write

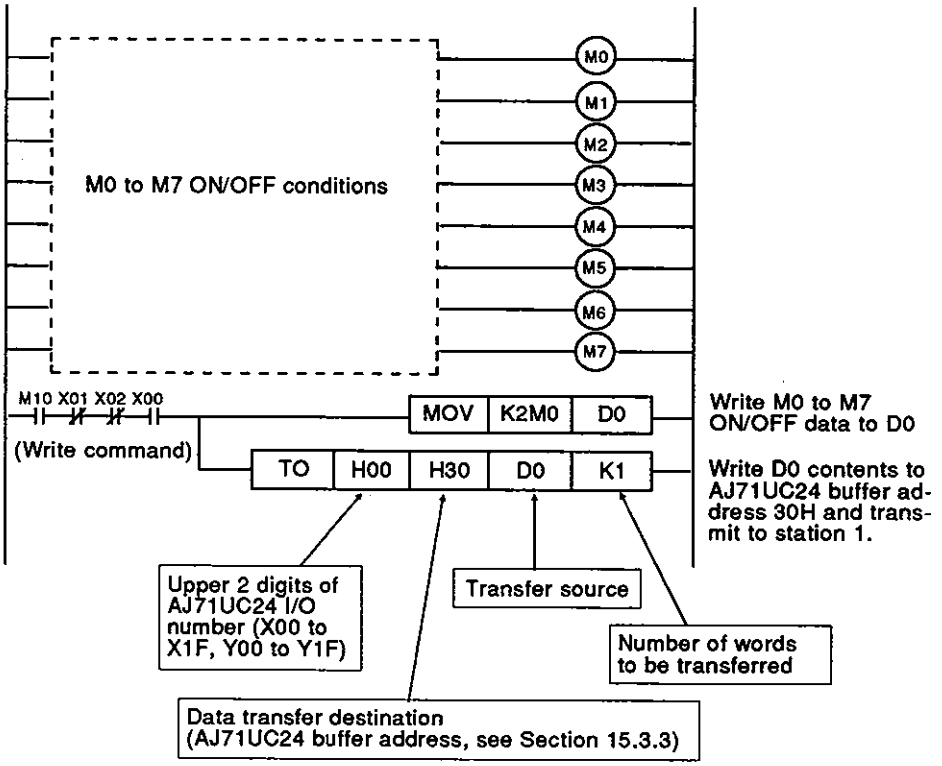
PROGRAM CONDITIONS

(1) AJ71UC24 I/O addresses .....X00 to X1F, Y00 to Y1F

(2) M0 to M7 ON/OFF data is echoed at the 1st to 8th output devices at the master station.

PROGRAM EXAMPLE

To control the ON/OFF statuses of outputs at the master station



EXPLANATION

(1) Data is written to the specified buffer memory addresses in the AJ71UC24 by the TO instruction and is then automatically transmitted from the AJ71UC24 to the master station.

1st to 8th device data .....Address 30H

For further details, see Section 15.3.3.

15.6.3 Received data read

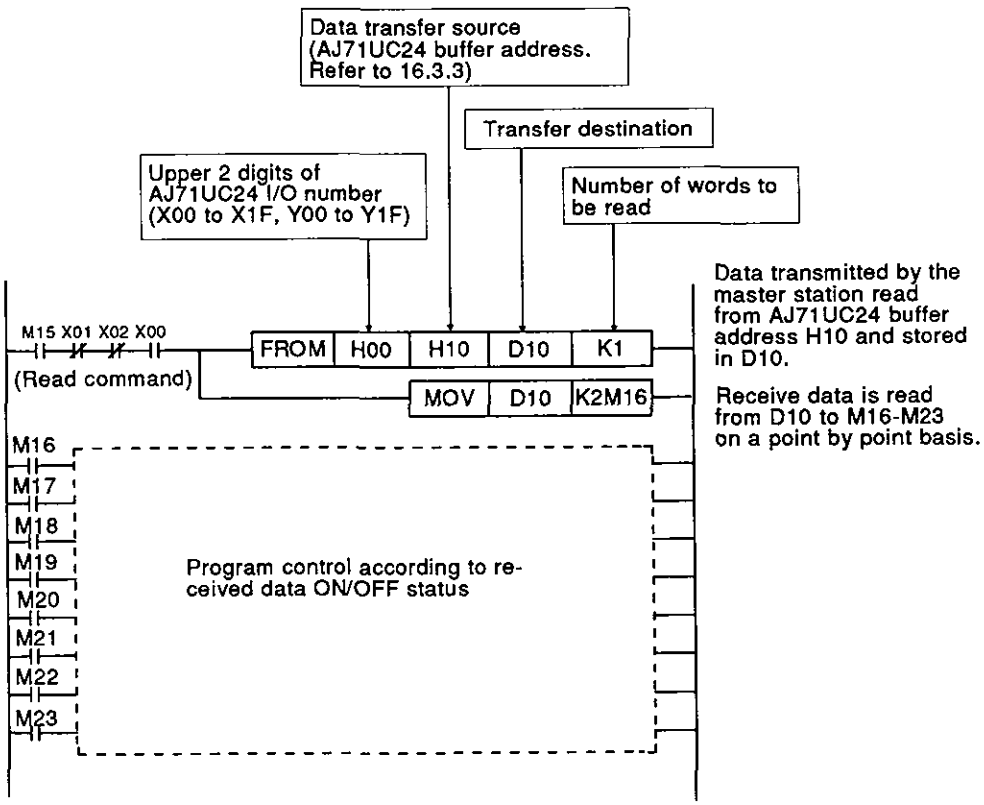
PROGRAM CONDITIONS

(1) AJ71UC24 I/O addresses ..... X00 to X10, Y00 to Y10

(2) The ON/OFF statuses of 8 bits in the master station are echoed at M16 to M23 in the PC CPU.

PROGRAM EXAMPLE

To detect and control each point of received ON/OFF data.



EXPLANATION

(1) Data written from the master station is automatically stored in the specified buffer memory addresses in the AJ71UC24.

Reading received data from the AJ71UC24 buffer memory using the FROM instruction allows the received data ON/OFF status to be used in the sequence program.

1st to 8th device data ..... Address 10H

For further details, see Section 15.3.3.

16. TROUBLESHOOTING (MULTIDROP LINK FUNCTIONS)

This chapter describes errors which can occur with the multidrop functions.

16.1 Error Codes (Master Station)

During data transmission between the AJ71UC24 and slave stations appropriate error codes are written to buffer address 60H to define the error as follows:

Error Code (Hexadecimal)	Description			LED Signal	Remedy
01H (1)	Pretransmission sequence	Any of the following errors has occurred during pretransmission sequence. • Initial data setting error • DIP switch setting error • Cable connection error • Data communication error	During communication with station 1	*1 L2 ON Xn1 ON	1) Check initial data. 2) Check DIP switches. 3) Check slave station power. 4) Check cable. 5) Check terminal resistor.
02H (2)			During communication with station 2		
03H (3)			During communication with station 3		
04H (4)			During communication with station 4		
05H (5)			During communication with station 5		
06H (6)			During communication with station 6		
07H (7)			During communication with station 7		
08H (8)			During communication with station 8		
09H (9)		Initial data has not been transferred from the buffer memory to the RS-422/485 interface transmission buffer.			1) Check the number of FROM/TO instructions. 2) Hardware fault
11H (17)	Data transmission sequence	Any of the following errors has occurred during data transmission sequence. • Cable error • Data communication error	During communication with station 1	*1 L3 ON Xn2 ON	1) Check slave station power. 2) Check cable
12H (18)			During communication with station 2		
13H (19)			During communication with station 3		
14H (20)			During communication with station 4		
15H (21)			During communication with station 5		
16H (22)			During communication with station 6		
17H (23)			During communication with station 7		
18H (24)			During communication with station 8		
19H (25)		Data cannot be transferred between the buffer memory and the RS-422/485 interface communication buffer.			1) Check the number of FROM/TO instructions. 2) Hardware fault
21H (33)	Pretransmission sequence	Initial data is wrong.		L2 ON Xn1 ON	Check initial data. (See Section 13.3)

*1: When SW22 (setting of link processing(slave station is faulty)) turns ON (continuation), "L6" LED turns ON, and Xn3 turns ON.

16.2 Error Codes (Local Station)

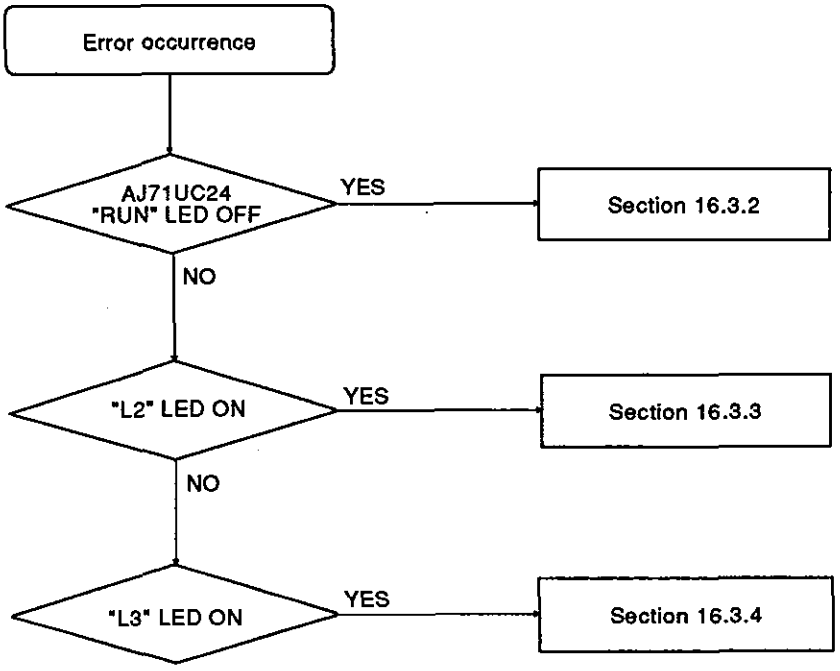
During transmission between the master and slave stations appropriate error codes are written to buffer address 50H to define the error as follows:

Error Code (Hexa-decimal)	Description			LED Signal	Remedy
01H (1)	Pretrans-mission sequence	Any of the following errors has occurred during pretransmission sequence. • Initial data setting error • DIP switch setting error • Cable connection error • Data communication error	During communication with station 1	L2 ON Xn1 ON	1) Check initial data. 2) Check DIP switches. 3) Check slave station power. 4) Check cable. 5) Check terminal resistor.
02H (2)			During communication with station 2		
03H (3)			During communication with station 3		
04H (4)			During communication with station 4		
05H (5)			During communication with station 5		
06H (6)			During communication with station 6		
07H (7)			During communication with station 7		
08H (8)			During communication with station 8		
09H (9)		Initial data has not been transferred from the buffer memory to the RS-422/485 interface transmission buffer.			1) Check the number of FROM/TO instructions. 2) Hardware fault
11H (17)	Data transmis-sion sequence	Any of the following errors has occurred during data transmission sequence. • Cabl error • Data communication error	During communication with station 1	L3 ON Xn2 ON	1) Check slave station power. 2) Check cable
12H (18)			During communication with station 2		
13H (19)			During communication with station 3		
14H (20)			During communication with station 4		
15H (21)			During communication with station 5		
16H (22)			During communication with station 6		
17H (23)			During communication with station 7		
18H (24)			During communication with station 8		
19H (25)		Data cannot be transferred between the buffer memory and the RS-422/485 interface communication buffer.			1) Check the number of FROM/TO instructions. 2) Hardware fault

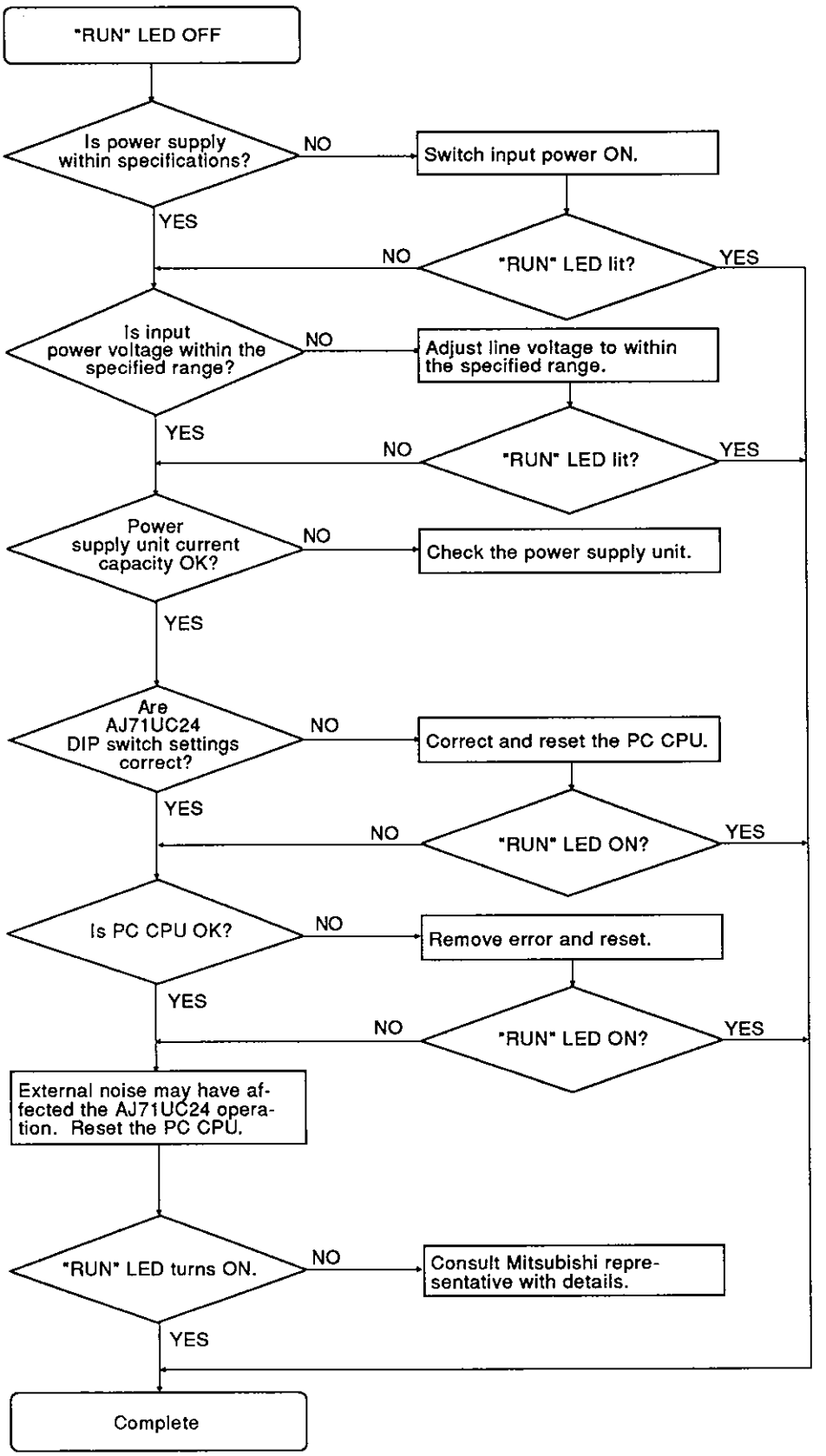
16.3 Troubleshooting OFF

This section describes basic troubleshooting procedures for the multidrop link functions. The User's Manuals give information on PC CPU module troubleshooting.

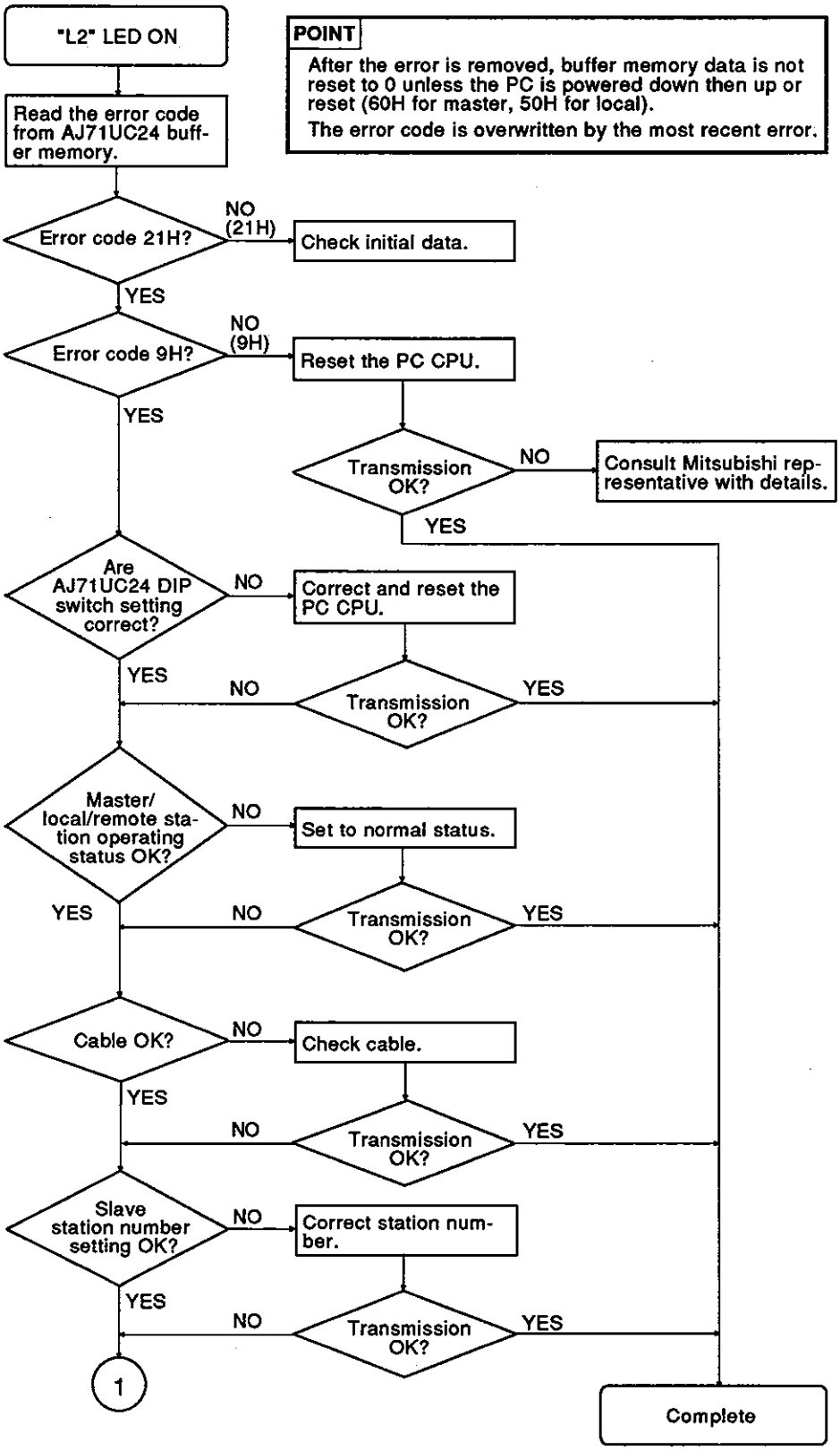
16.3.1 Troubleshooting flow chart

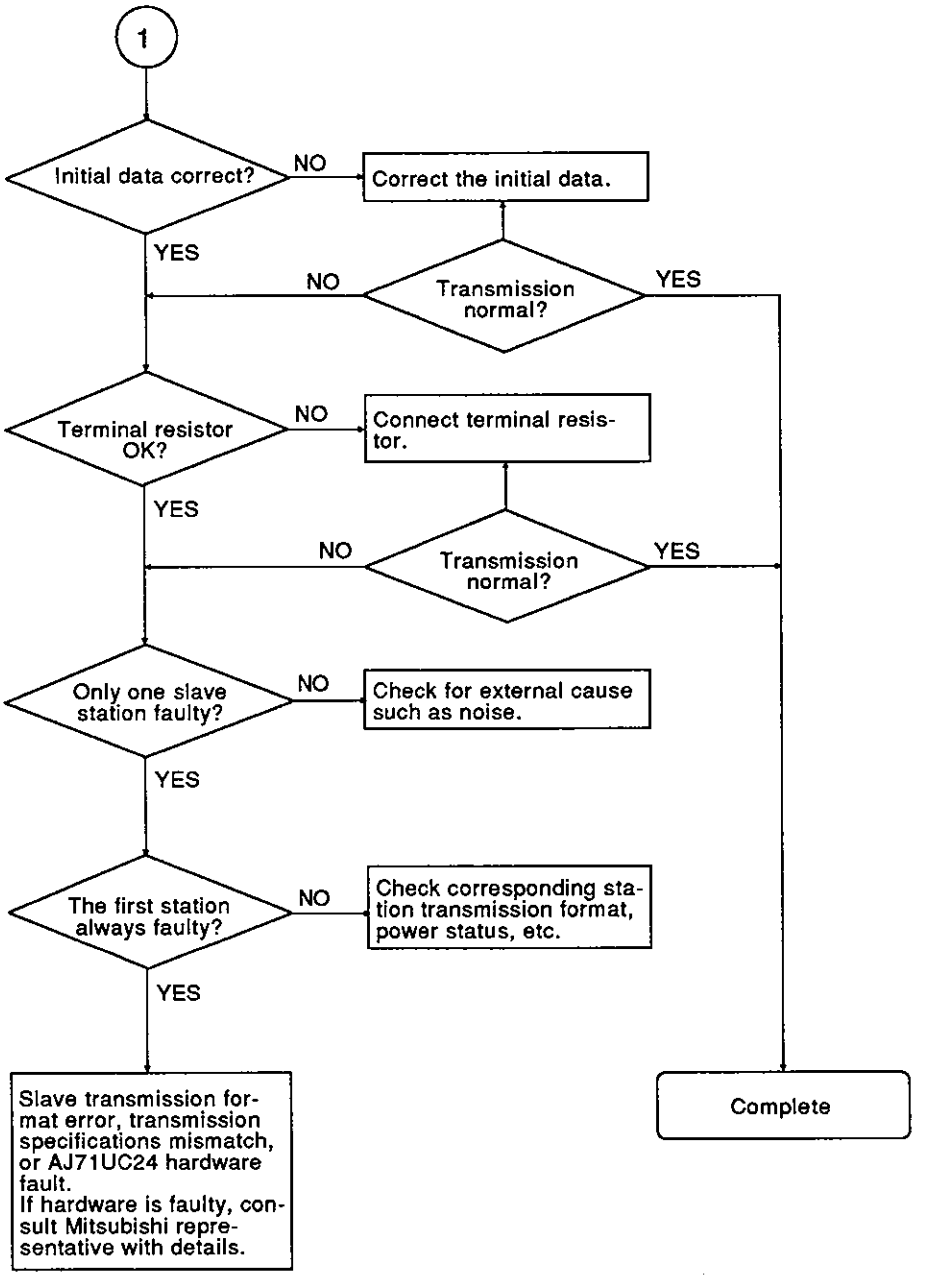


16.3.2 RUN LED turns OFF

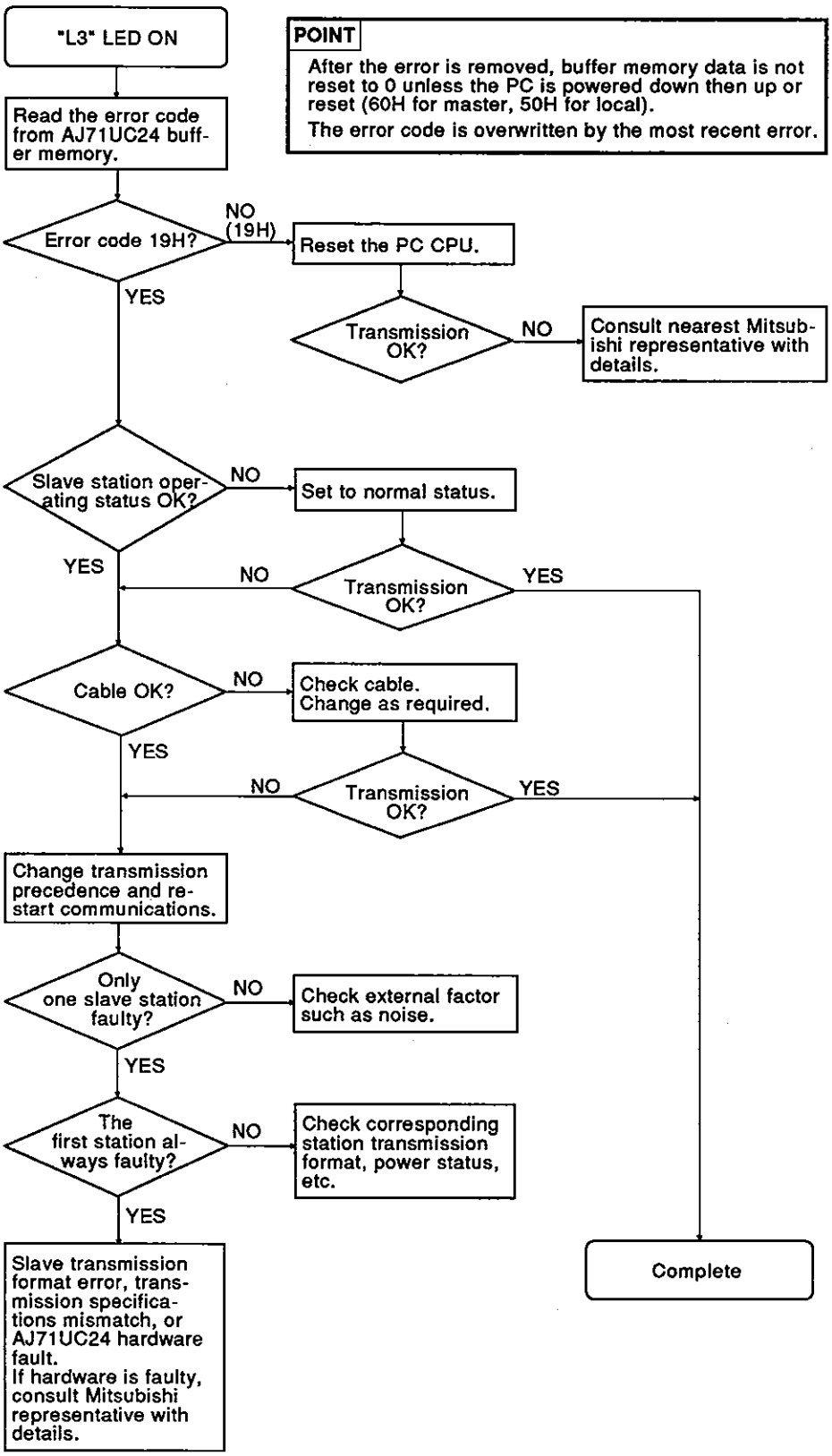


16.3.3 L2 LED turns ON



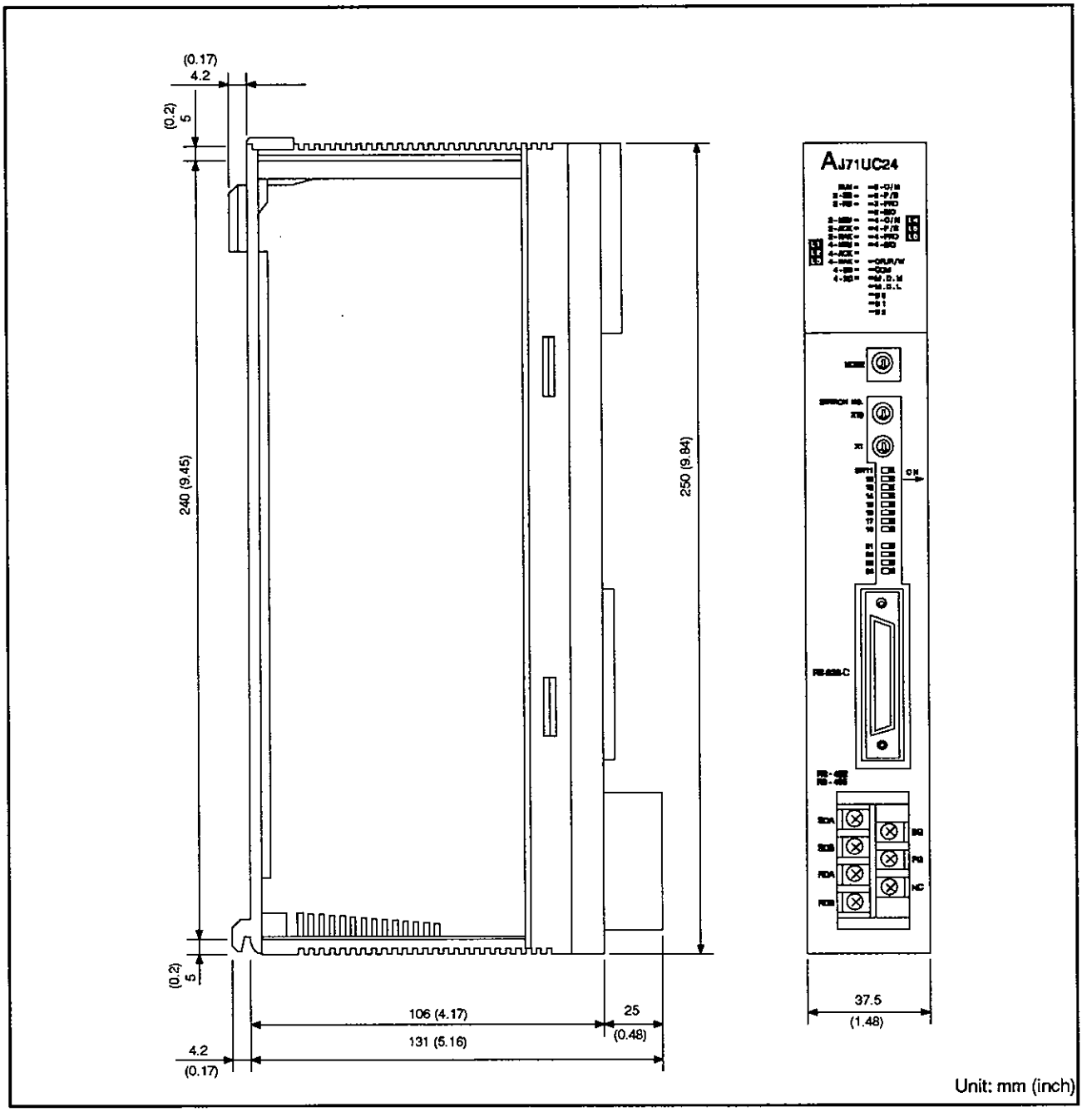


16.3.4 L3 LED turns ON



APPENDICES

APPENDIX 1 EXTERNAL VIEW



APPENDIX 2 PRECAUTIONS CONCERNING COMPATIBILITY AND THE USE OF EXISTING PROGRAMS PREPARED FOR THE AJ71C24-S8 COMPUTER LINK MODULE

The following sections describe the precautions which should be taken when using the AJ71UC24 link/multidrop link module (hereinafter called the AJ71UC24). These precautions cover its compatibility with the AJ71C24-S8 computer link module (hereinafter called the AJ71C24-S8), the use of the existing programs prepared for the AJ71C24-S8, and the procedures for changing, adding and installing modules to the existing network.

2.1 Compatibility

The AJ71UC24 and the AJ71C24-S8 have the same dimensions, and can be installed in the same way. They also use the same basic programs (PC CPU programs and computer programs).
Compatibility is maintained within the functions supported by the AJ71C24-S8.

2.2 Precautions When Using Existing Programs

The following are the precautions for replacing the AJ71C24-S8 with the AJ71UC24:

(1) Terminal resistance connection

While the routine setting of terminal resistance for the AJ71C24-S8 via the RS-422 is made by switch, the AJ71UC24 must be connected with a terminal resistance proper for RS-422 or RS-485 communications.

(2) I/O signals to PC CPU

The request-to-switch-mode signal (Y(n+1)9) and the switch-completed signal (Xn9) are provided with the AJ71UC24. Normal mode switching from a PC CPU is executed by this request-to-switch-mode signal.

2.3 Function Comparison

The following table shows the functions upgraded from the AJ71C24-S8 and newly equipped with the AJ71UC24.

Function \ Module	AJ71C24-S8	AJ71UC24	Reference Section
Interface specification	• RS-232C, RS-422	• RS-232C, RS-422/485	Section 3.2.4
New buffer memory	—	• Stores RS-232C signal data and the statuses of the setting switches (for mode setting, station number setting, transmission specification setting) on the face of the AJ71UC24.	Section 3.7 Section 7.8 Section 7.9 Section 7.10
Mode switching function	• Normal mode switching	• Both normal and forced mode switching patterns are available.	Section 3.4
Multidrop link function	Unavailable	• A link system (multidrop link system) can be built up between a master station and local or remote stations using an inexpensive RS-422/485 interfaces.	Chapters 13 to 16

APPENDIX 3 ASCII CODE TABLE

The codes are as shown in APPENDIX 4 in the AJ71C24-S8 User's Manual.

APPENDIX 4 COMMUNICATIONS TIME BETWEEN A PC CPU AND AN AJ71UC24

While running, the PC CPU, in response to a request from the AJ71UC24, processes data by the number of processable points per communications, as shown in Section 3.3.1, after executing an END instruction.

The intervening times (i.e. by how much the scan time increases) for each processing operation and its corresponding processing times (indicated in number of scans) are shown below.

(1) ACPU common commands

Item				Command	Intervening Times (Scan Time Increases)				Scan Count Required for Processing
					A0J2H, A1S, A1N, A2N, A3N	A3H	AnA	Access Data Unit	
Device data	Device memory	Batch read	Bit units	BR	0.76 ms	0.57 ms	1.38 ms	256 points	1 scan (2 scans for device "R" only)
			Word units	WR	1.13 ms	0.81 ms	2.42 ms	64 points	
		Batch write	Bit units	BW	1.13 ms	0.94 ms	1.06 ms	160 points	2 scans (1 scan when "enable during RUN" is set, excluding R)
			Word units	WW	1.13 ms	0.84 ms	2.60 ms	64 points	
		Test (random write)	Bit units	BT	1.13 ms	0.90 ms	1.06 ms	20 points	2 scans (1 scan when "enable during RUN" is set, excluding R)
			Word units	WT	1.13 ms	0.90 ms	1.06 ms	10 points	
		Monitor data registration	Bit units	BM	—	—	—	—	—
			Word units	WM					1 scan for device "R" only
		Monitor	Bit units	MB	2.02 ms	0.93 ms	1.46 ms	40 points	1 scan
			Word units	MN	2.08 ms	0.96 ms	1.47 ms	20 points	
	Extension file register	Batch read		ER	1.27 ms	0.76 ms	2.42 ms	64 points	2 scans (3 scans for ET (only AnACPU))
		Batch write		EW	1.27 ms	0.76 ms	2.60 ms	64 points	
		Test (random write)		ET	1.31 ms	0.87 ms	0.97 ms	10 points	
		Monitor data registration		EM	—	—	—	—	—
		Monitor		ME	1.75 ms	0.98 ms	1.42 ms	20 points	1 scan
	Buffer memory	Batch read		CR	—	—	—	—	—
		Batch write		CW					
Special function module buffer memory		Batch read		TR	FROM instruction processing time + 1.13 msec.	FROM instruction processing time + 0.81 msec.	FROM instruction processing time + 0.75 msec.	128 bytes	1 scan
		Batch write		TW					2 scans (1 scan when "enable during RUN" is set)
Program	Sequence program	Batch read	Main	MR	1.20 ms	0.78 ms	0.70 ms	64 steps	1 scan
			Sub	SR	1.20 ms	0.84 ms	0.70 ms		
		Batch write	Main	MW	1.35 ms	0.75 ms	0.70 ms		2 scans
			Sub	SW	1.70 ms	0.76 ms	0.70 ms		

Item				Com-mand	Intervening Times (Scan Time Increases)				Scan Count Required for Processing
					A0J2H, A1S, A1N, A2N, A3N	A3H	AnA	Access Data Unit	
Program	Microcomputer program	Batch read	Main	UR	1.35 ms	0.76 ms	—	128 bytes	2 scans
			Sub	VR	1.35 ms	0.76 ms			
		Batch write	Main	UW	1.35 ms	0.73 ms			
			Sub	VW	1.53 ms	0.73 ms			
	Comment	Batch read		KR	1.35 ms	0.76 ms	2.42 ms	128 bytes	2 scans
		Batch write		KW	1.53 ms	0.73 ms	2.60 ms		
	Parameter	Batch read		PR	0.68 ms	0.50 ms	2.42 ms	128 bytes	2 scans
		Batch write		PW	—	—	—	—	—
		Analysis request		PS					
PC CPU		Remote RUN		RR	—	—	—	—	—
		Remote STOP		RS					
		PC model read		PC	—	—	—	—	—
Global				GW	—	—	—	—	—

(2) AnACPU dedicated commands

Item				Com-mand	Intervening Times (Scan Time Increases)		Scan Count Required for Processing
					AnA	Access Data Unit	
Device data	Device memory	Batch read	Bit units	JR	1.19 ms	256 points	1 scan (2 scans for device "R" only)
			Word units	QR	2.07 ms	64 points	
		Batch write	Bit units	JW	0.99 ms	160 points	2 scans (1 scan when "enable during RUN" is set, excluding R)
			Word units	QW	2.32 ms	64 points	
		Test (random write)	Bit units	JT	0.91 ms	20 points	2 scans (1 scan when "enable during RUN" is set, excluding R)
			Word units	QT	0.93 ms	10 points	
		Monitor data registration	Bit units	JM	—	—	—
			Word units	QM			1 scan for device "R" only
		Monitor	Bit units	MJ	1.34 ms	40 points	1 scan
			Word units	MQ	1.35 ms	20 points	
	Extension file register	Direct read		NR	2.30 ms	64 points	3 scans (4 scans when a set range covers several blocks)
		Direct write		NW	2.57 ms	64 points	
Program	Extension comment	Batch read		DR	2.31 ms	128 bytes	2 scans
		Batch write		DW	2.59 ms		

POINTS

(1) The PC CPU can perform only one of these operations with each END processing. If the A6GPP and the AJ71UC24 access a given PC CPU at the same time, one processing must wait until the other processing is completed. The scan count required for processing, therefore, further increases.

(2) Even though communications using the AJ71UC24 is not performed, the scan time increases by approximately 0.2 msec. (or 0.1 msec. with the A3HCPU and the AnACPU).

APPENDIX 5 SPECIAL FUNCTION MODULE BUFFER MEMORY ADDRESSES

The details are as described in APPENDIX 7 in the AJ71C24-S8 User's Manual.

APPENDIX 6 PRECAUTIONS DURING COMMUNICATIONS WHEN USING RS-422/485 INTERFACE

The details are as described in APPENDIX 6 in the AJ71C24-S8 User's Manual.

APPENDIX 7 SEQUENCE PROGRAM EXAMPLES SHOWING HOW TO OUTPUT WORD DEVICE DATA TO THE PRINTER IN THE NO-PROTOCOL MODE

The details are as described in APPENDIX 8 in the AJ71C24-S8 User's Manual.

APPENDIX 8 EXAMPLE OF A SEQUENCE PROGRAM FOR DATA COMMUNICATIONS IN THE BIDIRECTIONAL MODE

The details are as described in APPENDIX 9 in the AJ71C24-S8 User's Manual.

APPENDIX 9 AJ71UC24 SETTING RECORD FORM

The record form described here is designed to record the settings of the AJ71UC24 for computer linking. Use this form to keep the record of the settings of the AJ71UC24 or to prepare computer link programs for PC CPUs and computers.
Make and use duplications of this form.

Method of entry

(1) Number and date

Enter the number of the record form and the date at the top right corner of the form.

(2) Settings of the buffer memory special applications area

Enter the set values, which change the default settings when the AJ71UC24 READY signal (Xn7) is turned ON, in the set value column. The settings required for the dedicated protocol and the no-protocol/bidirectional mode at the start-up of the AJ71UC24 are indicated with a o mark in the columns next to the address column.

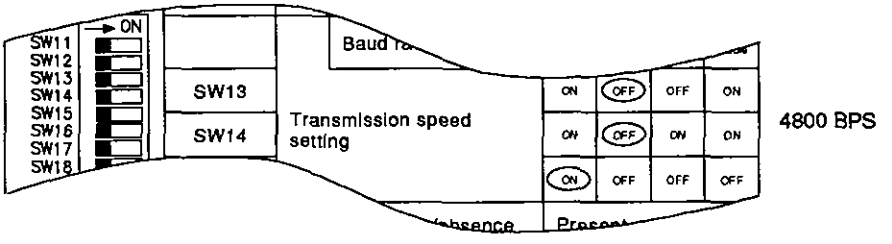
(3) Switch settings

(a) Station number setting switch

Enter the set values (value indicated by the arrow) in the columns of the tens digit and the ones digit of each station number.

(b) Transmission specification setting switch

Circle ON or OFF in the ON/OFF column according to the switch settings of the SW11 to the SW24.



(c) Mode setting switch

Enter the set value (value indicated by the arrow) in the mode setting switch column.

REMARK

The set value of each switch can be checked at buffer memory addresses 11EH to 11FH.

Record form No. Date : :

Record of AJ71UC24 settings

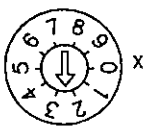
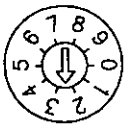
Settings of the buffer memory special applications area | **See Section 3.5 and Chapter 7.**

Buffer memory

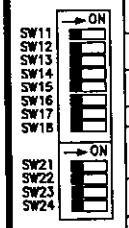
Address	Dedicated Protocol	No-protocol	Bidirectional	Name	Set Value	Default Setting
100H	—	o	—	No-protocol receive-completed code setting area		0D0AH(CR, LF)
101H	—	—	—	Error LED ON status storage area	—	0
102H	—	—	—	Error LED turn OFF request area	—	0
103H	o	o	o	No-protocol word/byte setting area		0 (words)
104H	—	o	o	No-protocol send buffer memory head address setting area		0
105H	—	o	o	No-protocol send buffer memory length setting area		80H
106H	—	o	o	No-protocol receive buffer memory head address setting area		80H
107H	—	o	o	No-protocol receive buffer memory length setting area		80H
108H	—	o	—	No-protocol receive-completion data length setting area		127 (words)
109H	—	—	—	On-demand buffer memory head address setting area	—	0
10AH	—	—	—	On-demand data length setting area	—	0
10BH	o	o	o	RS-232C CD terminal check setting area		0 (Check CD enabled)
10CH	—	—	—	On-demand error storage area	—	0
10DH	—	—	—	No-protocol received data clear request area	—	0
10EH	—	—	—	System area (unavailable)	—	—
10FH	o	o	o	RS-232C communications mode setting area		0 (Full-duplex)
110H	o	o	o	Simultaneous transmission priority/non-priority setting area		0 (Priority)
111H	o	o	o	Transmission method at transmission resume		0 (Not retransmitted)
112H	—	—	o	Bidirectional mode setting area		0 (No-protocol mode)
113H	o	o	o	Time-out check time setting area		0 (Infinite)
114H	—	—	o	Simultaneous transmission data valid/invalid setting area		0 (Data valid)
115H	—	—	o	Check sum enable/disable setting area		0 (Check sum enabled)
116H	—	—	—	Data send error storage area	—	0
117H	—	—	—	Data receive error storage area	—	0
118H	—	—	—	Mode setting status storage area		1H to DH
119H	—	—	—	Mode switching setting area		0
11AH	o	o	o	Transmission time setting area		0 (DTR control)
11BH	o	o	o	DC1/DC3 control code setting area		1311H
11CH	o	o	o	DC2/DC4 control code setting area		1412H
11DH	—	—	—	RS-232C signal data storage area	—	Depending on data communications status
11EH	—	—	—	Mode setting switch/station number setting switch status storage area	—	Depending on switch status
11FH	—	—	—	Transmission specification setting switch status storage area	—	

Set value of switch

(1) Station number setting switch (See Section 4.3.3.)

	Setting Contents	Set Value
 X 10	Tens digit of station number	
 X1	Ones digit of station number	

(2) Transmission specification setting switch (See Section 4.3.2.)



Setting Switch	Setting Item	Setting Value
SE11	Main channel	ON OFF
SW12	Data bit	ON OFF
	Baud rate	—
SW13	Transmission speed	ON OFF
SW14		ON OFF
SW15		ON OFF
SW16	Parity bit presence/absense	ON OFF
SW17	Even/odd parity	ON OFF
SW18	Stop bit	ON OFF
SW21	Sum check enable/disable	ON OFF
SW22	Write during RUN enable/disable	ON OFF
SW23	Computer link/multidrop link	ON OFF
SW24	Unused	—

(3) Mode setting switch (See Section 4.3.1.)

Mode Setting Switch No.	Setting		Set Value
	RS-232C	RS-422/485	
0	Unavailable		
1	Protocol 1 mode	No-protocol mode	
2	Protocol 2 mode	No-protocol mode	
3	Protocol 3 mode	No-protocol mode	
4	Protocol 4 mode	No-protocol mode	
5	No-protocol mode	Protocol 1 mode	
6	No-protocol mode	Protocol 2 mode	
7	No-protocol mode	Protocol 3 mode	
8	No-protocol mode	Protocol 4 mode	
9	No-protocol mode ↔	No-protocol mode	
A	Protocol 1 mode ↔	Protocol 1 mode	
B	Protocol 2 mode ↔	Protocol 2 mode	
C	Protocol 3 mode ↔	Protocol 3 mode	
D	Protocol 4 mode ↔	Protocol 4 mode	
E	Unavailable		
F	Reserved for module test		

IMPORTANT

(1) Design the configuration of a system to provide an external protective or safety inter locking circuit for the PCs.

(2) The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(a) Ground human body and work bench.

(b) Do not touch the conductive areas of the printed circuit board and its electrical parts with and non-grounded tools etc.

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisfy yourself as to its suitability for your specific application.

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