Datel DVME-624C2

12-Bit, 4-Channel VMEbus D/A Board

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DATEL®

Manual Number: UM-DVME-624

User Manual
for
DVME-624

September, 1993

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UNPACKING

This package should contain a DVME-624 board, a user's manual and a diagnostic program on a 5 1/4" diskette. Upon receipt of this package, visually inspect the board for missing or damaged material. In the event of damage, save all packing materials and immediately notify your carrier to validate shipping claims.

ALWAYS STORE THE BOARD IN THE ANTISTATIC COVER

This board contains components that are susceptable to static discharge, and should be handled with appopriate caution. The plastic, antistatic cover protects CMOS components from being damaged by static discharge. It also protects against dust and moisture condensation.

RETAIN THE ORIGINAL PACKING MATERIALS

Should the board need repair at a later date, it can safely be returned if packed in the original materials.

WARRANTY

DATEL warrants that the articles delivered are free from defects in material and workmanship under normal use and service as described in the literature for this product. Obligations under this warranty are limited to replacing or repairing, at DATEL's option, any of said articles returned to DATEL's factory within one year of shipment, with transportation charges prepaid.

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SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides the necessary information needed to configure, install, program, and fully operate DATEL's DVME-624 VMEbus D/A board. All specifications, connector pin-outs, and engineering drawings are included to assist the user in the use and implementation of the DVME-624 into its intended application.

Section one gives a general description of the DVME-624 and presents a list of the boards specifications. All information needed to set up and configure the DVME-624 for installation into VMEbus system is found in section two. Section three provides pin assignment information of all the DVME-624 connectors. Section four presents all the necessary information needed to program the DVME-624. The last section gives a more detailed description of the DVME-624's operation.

1.2 GENERAL DESCRIPTION

The DVME-624 is a double height (6U) VMEbus analog output module. It provides four channels of isolated digital-to-analog (D/A) conversion with 12 bits of resolution. Overall accuracy is within +/- 0.05 % of full scale range. To ensure the board's compatibility with popular process control and test instrumentation, five voltage ranges and a 4-20 mA current loop output option are jumper selectable for the D/A channels.

The DVME-624 is available in four different versions; DVME-624V1, DVME-624V2, DVME-624C1 and DVME-624C2. Each version is differentiated by output settling time and availability of 4-20mA current loop drivers. The -C suffix designates that the board provides 4-20 mA voltage-to-current converters at each output in addition to voltage outputs while the -V suffix designates that the board provides voltage outputs only. The -1 suffix specifies outputs that settle to the rated accuracy within 30 microseconds while the 2 suffix specifies a 6 microsecond settling time. The use of the term DVME-624 in this manual applies to all versions unless specifically differentiated with the V1, V2, C1, or C2 suffix.

The most important and unique feature of the DVME-624 board is its 300 Volt channel-to-channel and channel-to-bus isolation. The DVME-624 is suited for applications where high common mode voltages or actuator failure could cause high voltages to be applied to the outputs of a controlling analog output board.

Without isolation these voltages could migrate through the analog output board and interfere with the VMEbus. These type of applications often have a low level analog signal superimposed on a high voltage such as in the testing of power supplies, isolation amplifiers, etc. Isolation is accomplished through a combination of optoisolators for digital signals and transformer isolation for power distribution. Discrete on-board dc-to-dc converters provide four individually isolated supplies for each D/A converter.

The DVME-624 features a D/A converter power-on reset circuit which forces the D/A outputs to zero volts at power-on time regardless of output voltage range or input coding selection. This feature is useful where external actuators must initialize to an off state at power-on. All the analog outputs of the DVME-624 are brought out to a single DB-25 style connector on the front panel. DATEL offers a convenient screw termination panel, model DVME-691D, with cables that plug directly into the output connectors of up to two DVME-624 boards. The DVME-624 installs into the VMEbus through the P1 connector and does not utilize the P2 connector.

The DVME-624 is fully bus and card cage compatible with the VMEbus. It supports non-privileged user or supervisory short I/O addressing capabilities and is shipped as a memory mapped peripheral occupying 256 bytes in the CPU address space. The board is 9.2"W x 6.3"D x 0.6"H (233.3 x 160 x 15.2 mm). Multiple DVME-624 boards may be mounted in adjacent card slots when used with a standard .80" spacing card cage.

The DVME-624 draws all of its power from the VMEbus +5V and +12V lines. On-board DC to DC Converters provide the isolated +/-15V to drive the board's analog circuitry. Total typical current drawn from the VMEbus +5V and +12V is 1.2 A and 0.4 A, respectively.

Figure 1-1. illustrates the block diagram of the DVME-624 D/A board. The board consists basically of the VMEbus interface logic, D/A converter section, isolation circuitry, data register hardware, optional 4-20 mA current loop drivers, and DC-to-DC converter circuitry.

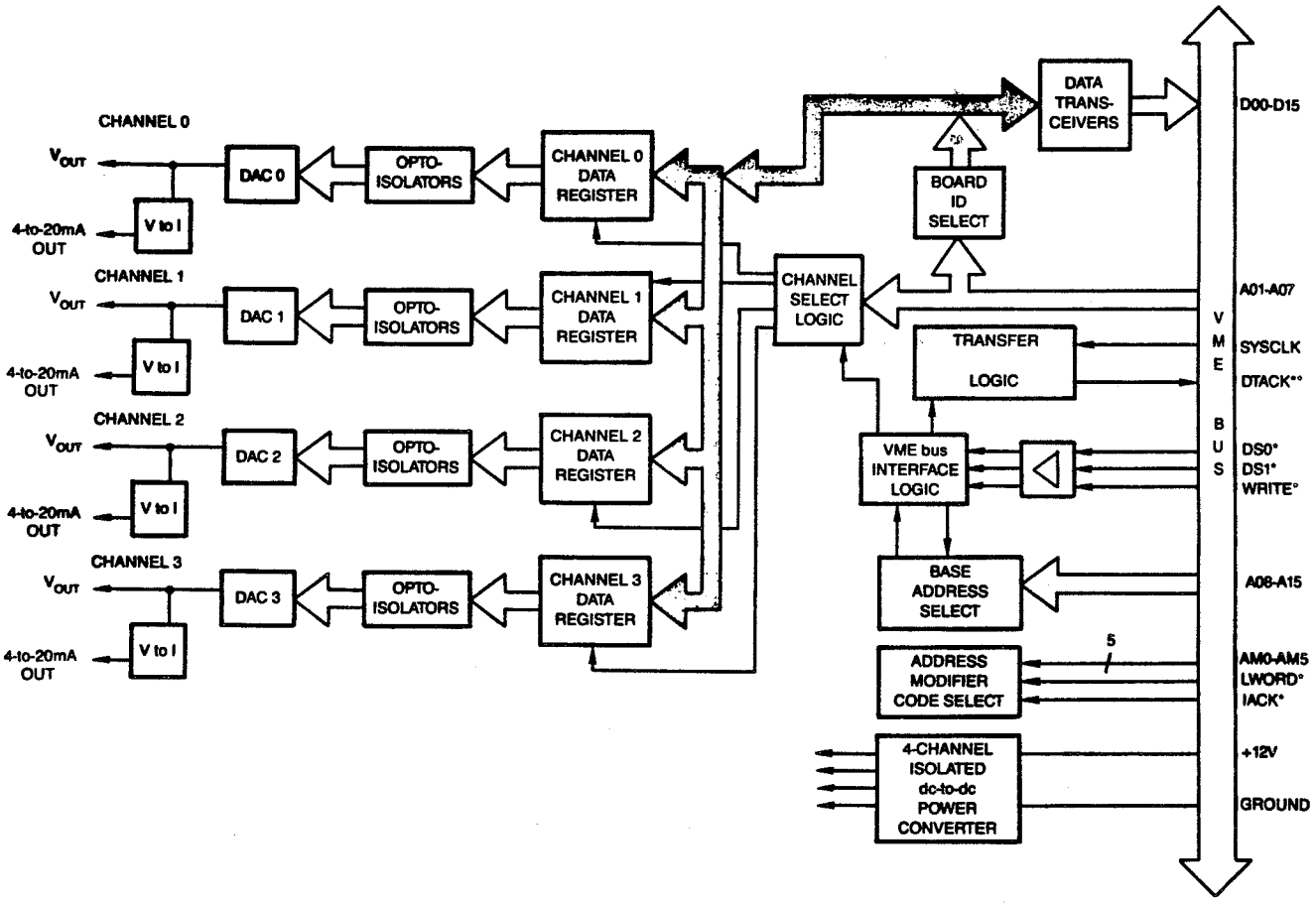

Figure 1-1. Block Diagram of the DVME-624

1.3 SPECIFICATIONS

All specifications typical at 25 degrees C, Vexc = +24VDC, RLoop = 250 ohms unless otherwise noted.

INTERFACE SPECIFICATIONS		[comments]
Interface	VMEbus A16, D16 slave	[IEEE P1014/D1.0]
Data Bus	16 bits	
Address Bus	Short I/O Space 16 address lines 6 address modifiers	[Board selected by address modifiers 29h, 2Dh, 39h and 3Dh]
Interrupts	none	
Memory Mapping	Short I/O User or Supervisor	[256 bytes allocated per board]
Data Transfer Acknowledge Line	DTACK*	[Acknowledge to the VME BUS host that data has been placed or accepted from the VMEbus data lines.]

Note: DTACK* is derived from the 16 MHZ bus SYSCLK which must be supplied.

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CONNECTOR SPECIFICATIONS

VME BUS - P1	96 Pin Male DIN Connector		
Analog Output - J1	One - 25 Pin "D" Type Female Connector	[	Amp P/N 745783-1 or equivalent]

ANALOG SPECIFICATONS		[comments]
GENERAL - ANALOG OUTPUT		
Number of Channels	4	
Isolation	300 VRMS	[sustained, max.]
Output Range	0 to 5 V 0 to 10 V +/- 2.5 V +/- 5 V +/- 10 V (std) 4-20 mA	[jumperable] [Current loop]
Digital Input Coding	Bipolar 2's Complement	[Jumperable to Bipolar Offset Binary or Unipolar Straight Binary]
Resolution	12 Bits	[Left Justified, Bits D0 through D3 not used]
Reset	Minus Full Scale	[Output will reset to 0.000 VDC at power up]
Current Loop Excitation Voltage	15-36Vdc	[Supplied by user]

PERFORMANCE - ANALOG OUTPUT

Typical at +25 deg C, Vexc = +24VDC Rloop = 250 ohms unless otherwise specified.

SPECIFICATION	MINIMUM	TYPICAL	MAXIMUM
Accuracy	.05% of FSR		
Differential nonlinearity			+/-0.5 LSB
Zero temp drift		3 ppm/degC	5 ppm/degC
Offset temp drift		5 ppm/degC	10 ppm/degC
Gain temp drift		15 ppm/degC	30 ppm/degC
Settling time			
DVME624-x2 DVME624-x1			6 u sec 30 u sec
Output current			+/- 5 mA
Output impedance		50 mohm	
Isolation (channel to channel)	300 VRMS		
Isolation, output to bus	300 VRMS		
CURRENT LOOP DVME-624Cx only			
Accuracy	0.1% of FSR		
Excitation	15 Vdc	24 VDC	36 Vdc
Load Resistance	100 Ohm		1000 Ohm

POWER SUPPLY AND PHYSICAL CHARACTERISTICS

POWER SUPPLY REQUIREMENTS

+ 5VDC +/- 0.5% @ 1.0A (1.2A max)

+12VDC +/- 2.0% @ 0.4A (0.7A max)

PHYSICAL CHARACTERISTICS

Outline Dimensions (minus connectors)	9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)
Weight	11 oz.
Operating Temperature Range	0 to 60 Degree C
Storage Temperature Range	-20 to +80 Degree C
Relative Humidity	0 to 90% Non-Condensing

SECTION 2

BOARD INSTALLATION AND JUMPERING

2.1 INTRODUCTION

The DVME-624 has a base address selection DIP switch and five basic jumper blocks. The jumpers select DAC voltage output ranges, data input coding, address modifier code, DTACK* delay, and current output option. This section describes the selection and configuration of the DVME-624 for installation into the targeted application. This section also describes how to calibrate the DVME-624 using the DVME-IOTEST menu driven test software provided.

Figure 2-1 illustrates the DVME-624 board layout specifically showing switch S1, jumper, and component positioning.

2.2 Base Address Selection

The DVME-624 is configured to appear as 256 bytes of memory locations in the CPU's Address space. The board is shipped with a standard base address of C900 hex and is a short I/O device. It utilizes the 16 bit addressing mode of the VMEbus and responds to either Address Modifier codes 29H, 2DH, 39H or 3DH through user jumper selection. The base address of the DVME-624 is selected using DIP switch S1 which decodes VMEbus Address lines A15 through A08. The high 8 Address lines A23 - A16 are not decoded due to short I/O addressing. Figure 2-2 shows the DVME-624's base address switch factory setting and selection convention. Note that an ON switch corresponds to a logic 0 and an OFF corresponds to a logic 1. Refer to Figure 2-1 for the location of the Base address switch S1 on the DVME-624. When selecting the base address of the DVME-624 be sure that you do not allocate any address space that overlaps with any other devices already configured in your system. In the event that more than one (1) DVME-624 D/A board is used in a system be sure to set each board to a different base address.

The base address of DATEL's DVME-624 is selectable within the range of $0000 to $FF00 in the short I/O address space of the targeted VMEbus system. The short I/O address space is typically mapped to addresses $FF0000 - $FFFFFF in the VMEbus systems memory map.

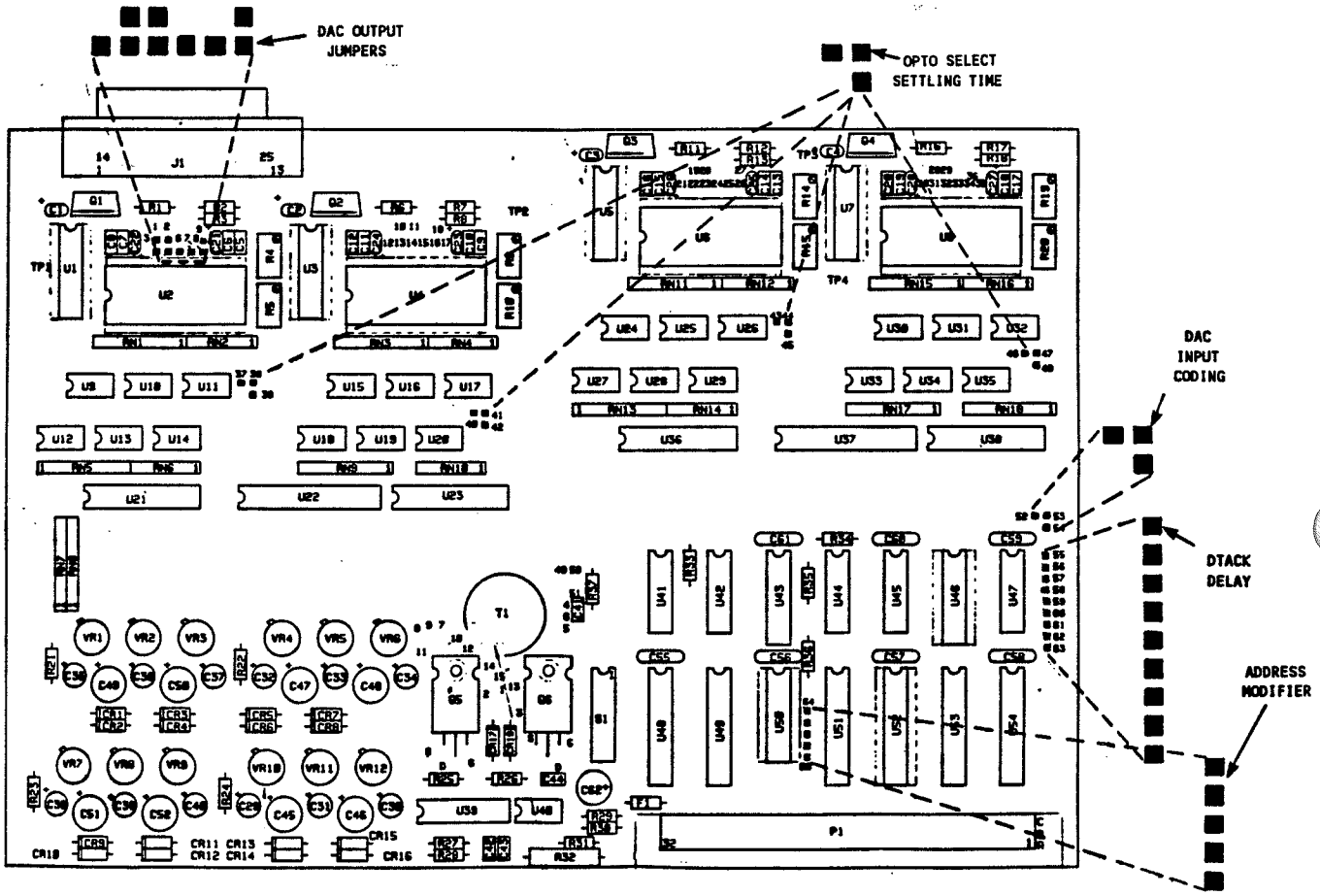


Figure 2-1. Board Layout of the DVME-624

DVME-624 Base Address Switch S1

When setting the base address, remember that the DVME-624 board functions in "blocks" of 256 decimal locations (100 HEX).

S1-8	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1
X	X			X			X
		X	X		X	X	
A15	A14	A13	A12	A11	A10	A09	A08
1	1	0	0	1	0	0	1
BINARY							
C				9			
HEX							

NOTE: Lower 8 bits select the DVME-624 on-board registers. (256 locations). The upper 8 bits (A15 - A08) are not decoded by the DVME-624 and are not used for short I/O devices.

Figure 2-2. DVME-624 Base Address Switch Factory Setting

2.3 Address Modifier Selection

The DVME-624 Board may be jumpered to respond to one of four Address Modifier Codes on the VMEbus AM5 - AM0 lines. Normally only modifier codes 29H and 2DH should be used. These are Short I/O (16 bit address) access codes and the DVME-624 is designed as a Short I/O device. Address modifier Codes 39H and 3DH are reserved for standard (24-bit address) data access and are available for future expansion. The board is shipped standard for Short Non-Privileged and supervisory I/O Access (29 hex). Address Modifier Selection is summarized in Table 2-2. Refer to Figure 2-1 for Address Modifier Code jumper locations.

TABLE 2-2 Address Modifier Code Jumpers

Address Modifier Code(hex)	Function	Connect Jumper 64 to
29 or 2D	Short Non-Privileged or short supervisory I/O Access	67
2D	Short Supervisory I/O Access only	68
39 or 3D *	Standard Non-Privileged or standard supervisory Data Access	65
3D *	Standard Supervisory Data Access only	66

* Codes 39h and 3Dh are not intended for use on this board. They are used for 24-bit addressing.

2.4 DTACK* Delay Selection

The DVME-624 generates a Transfer Acknowledge (DTACK) signal in response to read or write commands from the host computer.

A jumper selectable delay ranging from 125 to 1000 nanoseconds is available on the DVME-624. The DTACK* delay is generated from the VMEbus SYSCLK signal which is assumed to have a period of 62 nsec. Note that the VMEbus SYSCLK is REQUIRED for the DVME-624 to operate. The selectable DTACK delays are mainly for use by DATEL to handle different data set up times for various present and future models. The DVME-624 comes from the factory configured with a delay of 250nS selected and should not be changed for most applications. Table 2-3 lists the selectable delay times available to the corresponding jumpers. Refer to Figure 2-1 for the location of the DTACK* Delay jumpers.

TABLE 2-3 DTACK* DELAY JUMPER

DELAY (nsec)	JUMPER
125	57 to 63
250	60 to 63 (standard)
375	61 to 63
500	62 to 63
625	59 to 63
750	58 to 63
875	56 to 63
1000	55 to 63

2.5 D/A Output Range Selection

The output voltage range of the four on-board D/A converters may be jumpered as described in TABLE 2-4. The DVME-624 can be jumpered to set its outputs to zero volts on reset. If the power-on reset feature of the board is used, all four channels must be configured for either unipolar or bipolar outputs. If the reset to zero feature is not required, the output range may be individually selected. In either case, the DAC input coding is selected for the entire board. Refer to Figure 2-1 for the output voltage range jumper locations.

TABLE 2-4 DAC OUTPUT RANGE JUMPERS (CHAN 0 to 3)

VOLTAGE RANGE	DAC 3	DAC 2	DAC 1	DAC 0
0 to 5V	35 to 36 30 to 31 33 to 34	26 to 27 21 to 22 24 to 25	17 to 18 12 to 13 15 to 16	8 to 9 3 to 4 6 to 7
0 to 10V	35 to 36 30 to 31	26 to 27 21 to 22	17 to 18 12 to 13	8 to 9 3 to 4
+/-2.5V	35 to 36 31 to 32 33 to 34	26 to 27 22 to 23 24 to 25	17 to 18 13 to 14 15 to 16	8 to 9 4 to 5 6 to 7
+/-5V	35 to 36 31 to 32	26 to 27 22 to 23	17 to 18 13 to 14	8 to 9 4 to 5
+/-10V standard	34 to 35 31 to 32	25 to 26 22 to 23	16 to 17 13 to 14	7 to 8 4 to 5
4-20 mA	35 to 36 30 to 31 28 to 29	26 to 27 21 to 22 19 to 20	17 to 18 12 to 13 10 to 11	8 to 9 3 to 4 1 to 2

2.6 Current Loop Output Option

The DVME-624Cx offers 4-20mA current outputs in addition to the five selectable voltage output ranges. Each channel has its own voltage to current converter output circuitry. A user-supplied external 15 - 36V dc excitation voltage is required for each current output. Table 2-5 lists the necessary jumper selection to configure each channel for current output. Note that the digital-to-analog converter must be jumpered for 0 - 10V dc range when using current outputs. If the jumpers are not configured as listed in Table 2-5 the voltage to current converters may be damaged.

The voltage to current converter chips are socketed on the DVME-624Cx. Unpopulated sockets are on the DVME-624Vx versions. Refer to Figure 2-1 for output current component and jumper positioning.

Table 2-5: DAC Current Output Jumpers

	DAC 3	DAC 2	DAC 1	DAC 0
4-20 mA	35 to 36 30 to 31 28 to 29	26 to 27 21 to 22 19 to 20	17 to 18 12 to 13 10 to 11	8 to 9 3 to 4 1 to 2

Warning: Jumpers 28 to 29, 19 to 20, 10 to 11, and 1 to 2 must be removed for any D/A converter with an output voltage range other than 0-10V dc. Other ranges could damage the voltage to current converters.

2.7 High-speed Output Settling Time Option

The DVME-624 is offered with a choice of one of two output settling times depending on the version selected. The lower-cost DVME-624V1 and DVME-624C1 provide outputs that settle within 30 microseconds. For more demanding high-performance applications the outputs of the DVME-624V2 and DVME-624C2 settle within 6 microseconds. Jumpers are provided on the DVME-624 board to select whether the normal or high-speed optoisolators are installed on the PC Board. Normally these jumpers are installed at the factory relative to the DVME-624 version and shouldn't be changed by the user. Table 2-6 lists the correct jumpering for each version.

TABLE 2-6 OptoIsolator/ Settling Time Jumper Settings

Model Number	Output Settling Time	Jumpers
DVME-624 x 1	30 uS	37-38, 40-41, 43-44, 46-47
DVME-624 x 2	6 uS	38-39, 41-42, 44-45, 47-48

(The "x" refers to the "V" or "C" version)

Refer to Figure 2-1 for the location of the Opto-isolator jumpers.

2.8 DAC Input Coding Jumpers

The input coding for all four D/A channels is selected by jumpers on the DVME-624 board. These jumpers also cause the DAC outputs to output 0.000V at power-on regardless of whether unipolar or bipolar output is selected. Table 2-7 lists the correct jumpering corresponding to the choices of D/A input coding. Refer to Figure 2-1 for the positioning of the input coding jumpers.

TABLE 2-7 DAC INPUT CODING JUMPERS

INPUT CODING	JUMPER
Unipolar Binary	52 to 53 49 to 51
Bipolar, Offset Binary	49 to 50 52 to 53
Bipolar, 2's Comp (Std)	49 to 50 53 to 54

Refer to the Calibration Table in APPENDIX C for corresponding voltage output values for a sample of input codes in hex. Note that the column labled BIN CODE represents "offset binary" for bipolar ranges and straight binary for unipolar ranges.

2.9 Installing The DVME-624 Into A System

Following the instructions in the previous section should properly configure all board jumpers. The DVME-624 is very easy to install into a VMEbus system. The following "check list" provides you with a step-by-step procedure to successfully install the DVME-624.

1) Remove power from the VMEbus card cage.

2) Rearrange the existing cards in the card cage to accommodate the new board addition(s). Study your host manuals to position the IACK and bus grant jumpers the card cage backplane. If you want interrupts from boards further away from the CPU board than the 624, they will be daisy chained by the 624. Board slots between the 624 and the CPU board must either contain boards which daisy-chains these signals or must have the backplane jumpers installed.

3) OBSERVE THE RULES GOVERNING ESD (ELECTROSTATIC DISCHARGE) IN THE HANDLING OF THE VMEbus BOARDS. Make yourself the same voltage potential as the grounded card cage by placing your hand on the card cage BEFORE handling the VME boards.

4) Carefully insert the DVME-624 board(s) into a normal 6U height slot in the VMEbus rack, making sure that the component side of the board is to the right. Make sure the P1 connector seats properly to avoid damaging it.

5) DO NOT CONNECT any analog output signals to the DVME-624 boards until you have read this entire manual. Figure 2-3 shows the typical installation of a DVME-624 into a VMEbus system. Note that the DVME-624 only uses the VMEbus P1 connector.

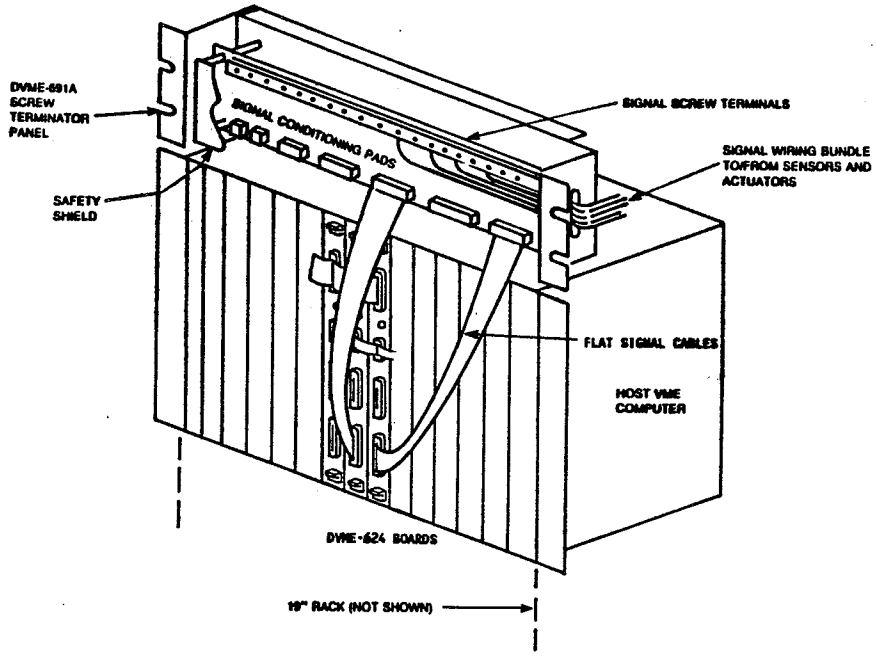


Figure 2-3. DVME-624 Board Installation

2.10 Typical Output Wiring

Analog outputs can be taken directly from the output connector on the DVME-624's front panel. Since its possible to have voltage or currents outputs on connector J1, it is extremely important to observe the correct channel pinouts listed in the Tables in Section 3. Figure 2-4 shows typical voltage and current output channel configurations. As an aid to connection of field wiring for each channel, DATEL offers the DVME-691D termination panel.

The following are examples of how to connect the output of the DVME-624 to your application.

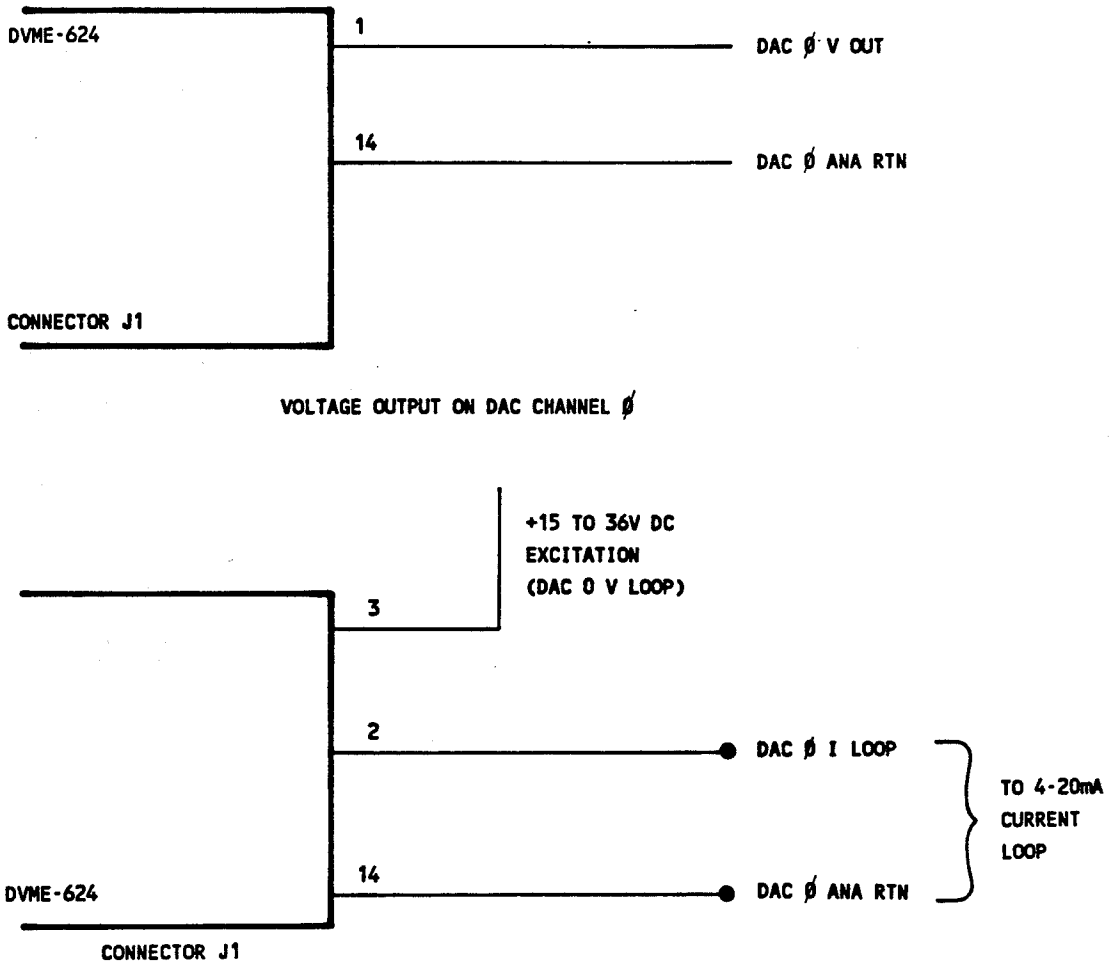


Figure 2-4. Typical Circuits for Voltage and Current Outputs.

2.11 DVME-691D Screw Termination Panel

Datel offers a rack-mountable screw termination panel for easy connection to your application's field wiring. Located on these screw termination panels are power rails that run adjacent to each channel for an optional user-supplied excitation voltage for current outputs. Contact Datel for a data sheet on Model DVME-691A/691D.

SECTION 3

CONNECTOR PIN ASSIGNMENTS

3.1 Introduction

The DVME-624 has one connector on its front panel and the VMEbus P1 connector at the rear. This section shows the pin-outs of each of the DVME-624's connectors. The mating connector used to interface to the external user application circuitry is not supplied with the DVME-624. It is a common DB-25P style connector. A description and AMP part number is provided in Table 3-1 below for easy ordering information.

Table 3-1 Analog Output Connector Part Number

Description	Ordering Part Number
25-Pin D	AMP P/N 745783 or equivalent

3.2 Analog Output Connector J1

The pin assignments of the DAC Analog Output connector J1 is described in Table 3-2. There is a screw termination panel available, DATEL Model DVME-691 permitting easy connection to your application field wiring. The screw termination panel eliminates the requirement for the construction of custom cable assemblies to connect the DVME-624 to the field wiring. Each DVME-624 connector has four voltage output channels. The DVME-624Cx version also supports four current outputs per connector. Two DVME-624 can be directly connected to a single DVME-691D. Note that V LOOP represents the extenal, user supplied, excitation voltage needed if current outputs are desired.

TABLE 3-2 ANALOG OUTPUT CONNECTOR J1

PIN NUMBER	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	
14	DAC 0 ANA RTN
15	DAC 0 ANA RTN
16	
17	DAC 1 ANA RTN
18	DAC 1 ANA RTN
19	
20	DAC 2 ANA RTN
21	DAC 2 ANA RTN
22	
23	DAC 3 ANA RTN
24	DAC 3 ANA RTN
25	

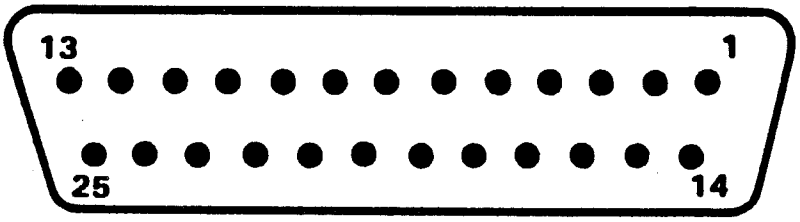


Figure 3-1. 25-Pin "D" Connector Pinout of J1
(Refer to Figure 2-1 for the location of connector J1).

3.3 - This section lists the pin assignments of the VMEbus (IEEE-P1014/D1.0) P1 connector The DVME-624 is a slave output device and consequently does not utilize the bus arbitration or interrupt signals. All bus grant and interrupt acknowledge signals are jumpered by the DVME-624 so that these daisy chains are not broken. The DVME-624 does not use VMEbus connector P2.

TABLE 3-3 VMEbus P1 PIN ASSIGNMENTS

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

SECTION 4

DVME-624 PROGRAMMING INFORMATION

4.1 Introduction

The DVME-624 appears as a block of 256 consecutive bytes in the CPU's address space. Within the DVME-624's 256 byte block are the boards identification code and DAC data registers. The DVME-624 register assignments are straight forward and the board is easy to program. This section describes each of the DVME-624's register assignments and explains in detail how to successfully program this board.

4.2 Internal Hardware Register Assignments.

The DVME-624's 256 byte block of register locations are mapped into the VMEbus systems address space through the boards base address. Table 4-1 lists the DVME-624's register assignments relative to the base address setting.

TABLE 4-1 DVME-624 REGISTER ASSIGNMENTS
(All offsets are in decimal)

BYTE ADDRESS	FUNCTION	READ/WRITE
Base + 0	Board Identification Code	Read Only
|	|	|
Base + 63	Board Identification Code	Read Only
Base + 64		
|	See Note 1	Read Only
Base + 127		
Base + 128		
|	See Note 2	Write Only
Base + 159		
Base + 160	D/A Channel 0	Write Only
Base + 162	D/A Channel 1	
Base + 164	D/A Channel 2	
Base + 166	D/A Channel 3	
Base + 168		
|	See Note 2	Write Only
Base + 255		

Note 1: These addresess are redundant with the ID PROM addresses (Base + 0 to Base + 63).

Note 2: These addresses are redundant in 8 byte blocks with the D/A output registers (BASE + 160 to BASE + 166)

4.3 Board ID PROM

DATEL DVME board products reserve the first 64 bytes of their allocated block of address space for the boards identification code. This code identifies the board model number and the number of 256 byte blocks mapped to the device. It allows the VMEbus host to easily identify the systems I/O configuration and allows the implementation of self configuring and menu driven software.

The DVME-IOTEST software provided with each of DATEL's DVME board products demonstrates one of the benefits of the ID code. It is a menu driven software package that tests any of DATEL's DVME boards given its base address. Because of the board ID code, one program can test all models by jumping into the specific test menus for each board independent of its location in the system. Without the ID code the software would have to map specific models to particular address locations.

Table 4-2 list the contents of the DVME-624's ID PROM relative to the boards base address.

Table 4-2 Board Identification Code

BYTE ADDR	PROM CONTENTS	ASCII EQUIV	FUNCTION
Base + 1	56H	V	Prom Module Identifier. This Ascii Code is always present here.
+ 3	4DH	M	
+ 5	45H	E	
+ 7	49H	I	
+ 9	44H	D	
Base + 0B	44H	D	Manufacturer ID "DAT" = Datel
+ 0D	41H	A	
+ 0F	54H	T	
Base + 11	64H	d	Board Model No.
+ 13	56H	V	
+ 15	4DH	M	
+ 17	45H	E	
+ 19	2DH	-	
+ 1B	36H	6	
+ 1D	32H	2	
+ 1F	34H	4	
Base + 2F			Board Model No.
Base + 31	31H	1	Number of 256 Byte Blocks Memory Mapped to this Board.

4.4 D/A Data Registers

The DVME-624 has four data registers corresponding to the four D/A output channels. Refer to Table 4-1 for the address locations of these registers. The D/A Data Registers are loaded by the host computer with the digital data to be converted and output by the D/A Converters. The D/A conversion begins on the write operation to the data registers. The register format is illustrated in Figure 4-1. Observe that the data is left justified and may be either binary or 2's complement depending on the board jumpers.

D/A DATA REGISTER HIGH BYTE (BASE+160,162,164,166)

15	14	13	12	11	10	09	08
BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4

MSB

D/A DATA REGISTER LOW BYTE (BASE+161,163,165,167)

7	6	5	4	3	2	1	0
BIT 3	BIT 2	BIT 1	BIT 0	X	X	X	X

LSB

"X" bits are don't care.

Note that some A/D - D/A converter literature refers to the MSB as bit 1. This convention for converters is because the first decision bit for successive approximation A/D's is the MSB.

Figure 4-1. D/A Register High and Low Bytes

4.5 General Programming Considerations

The DVME-624 responds only to word data transfers on write operations; it does not recognize byte operations on write or longword transfers on either read or write. Thus, when writing data to the board registers, word instructions (e.g. MOVE.W) must be used. Normally, the effective address will be the high (even) byte of the register. If this rule is not followed and a byte write instruction is used, the other byte of the register will be loaded with false data. If longword transfers are attempted, a bus error will result. Byte read operations will operate in the expected fashion.

4.6 Example Program

The following 68000 assembly language program is provided as an example to aid the user in writing application software to drive the DVME-624. In this example the factory base address setting of C900H and the standard bipolar 2's complement DAC output configuration are assumed. At the beginning of the program, the data register addresses of the DAC channels 0 through 3 are "equated" to mnemonic labels DAC0 - DAC3. The actual program performs three main functions. It clears DAC channel 0, sets DAC channel 1 to -10V dc (- FSR), and sets DAC channel 2 to +9.9951V dc (+ FSR).

```
1  00001000     ORG.L  $1000
2
3  00FFC9A0 DAC0 EQU $FFC9A0   ; DAC 0 ADDRESS
4  00FFC9A2 DAC1 EQU $FFC9A2   ; DAC 1 ADDRESS
5  00FFC9A4 DAC2 EQU $FFC9A4   ; DAC 2 ADDRESS
6  00FFC9A6 DAC3 EQU $FFC9A6   ; DAC 3 ADDRESS
7   ;
8   ;
9   ;
10  ;
11
12            START:
13  00001000  CLR.W  DAC0          ;DAC 0 -> +1/2 FSR
14  00001006  MOVE.W #$8000,DAC1   ;DAC 1 -> -FSR
15  0000100E  MOVE.W #$7FF0,DAC2   ;DAC 2 -> +FSR
16
17                              END
```

4.7 DVME-IOTEST Test And Calibration Software

The DVME-624 comes complete with a DVME-IOTEST test and calibration software package. The use of this software is described in the self-explanatory IOTEST menus. More information can be derived by examining the source listing. For hosts other than Motorola VERSAdos, IOTEST will need modification (specifically in the TRAP system calls). After editing, the program should be assembled on the new host system. Datel also offers the IOTEST ASCII source files on 360K IBM-PC/XT/AT 5.25" disks as a universal interchange media.

4.8 Board Calibration

Calibration should be performed by a qualified user and he/she must have operational understanding of the DVME-624. For best performance of the DVME-624, calibration is recommended every 3 months under normal conditions. The following is the procedure to calibrate the DVME-624.

[1.0] Equipment

[1.1] Connect a digital voltmeter between the Analog Hi Output and the Analog Low output for the D/A channel to be calibrated. Refer to Section 4 for J1 connector pinouts. If the 4-20 mA current loop is to be calibrated, connect a 250 ohm, 0.1% resistor from the LOOP Iout pin to Analog Low. Connect the DVM across this resistor. Also, Connect a +15V to +30VDC source from the Loop V+ pin to Analog Low.

[1.2] Load the DAC Data Register with 0000 hex for Straight Binary or 8000 hex for 2's Complement configuration. The Calibration Test software may be used to load the data value.

[1.3] Adjust the zero or offset pot to observe a reading of minus full scale on the DVM. The offset pots for each channel are as follows:

TABLE 4-3 ZERO/OFFSET POTENTIOMETERS

DAC	ZERO/OFFSET POT
0	R5
1	R10
2	R15
3	R20

Refer to Figure 2-1 for the location of the Zero/Offset potentiometers.

Minus full scale readings are as follows:

TABLE 4-4 MINUS FULL SCALE READINGS

RANGE	-FULL SCALE READING
0 to +5V	0.0000 V
0 to +10V	0.0000 V
+/-2.5V	-2.5000 V
+/-5V	-5.0000 V
+/-10V	-10.0000 V
4-20 mA	1.0000V

[1.4] Load the DAC Data Register with FFF0 hex for Straight Binary or 7FF0 for 2's Complement configuration. Adjust the Gain potentiometer for the channel under calibration to produce the + Full Scale Reading on the DVM. The gain pot number and + Full Scale reading is given in Tables 4-5 and 4-6. Refer to Figure 2-1 for the location of the Gain Potentiometers.

Table 4-5 GAIN POTENTIOMETERS

DAC	GAIN POT
0	R4
1	R9
2	R14
3	R19

Table 4-6 + FULL SCALE READINGS

RANGE	+FULL SCALE READING
0 to +5V	4.9988 V
0 to +10V	9.9976 V
+/-2.5V	2.4988 V
+/-5V	4.9976 V
+/-10V	9.9951 V
4-20 mA	4.9990 V

[1.5] Check the DAC Calibration by applying the input codes in the Calibration Table in Appendix A of this document. Check that the DAC output agrees with the correct output value.

4.9 DVME-UTIL

DATEL offers a data acquisition software utility package called DVME-UTIL. This package contains routines to drive all of DATEL's VMEbus boards. The software is divided into three main modules. One module contains routines that perform physical-to-logical channel mapping and typical analog I/O funtions. Another module performs all the console I/O funtions. The last module passes parameters from higher level languages to the other module's 68000 assembly language routines. Contact Datel for a DVME-UTIL data sheet.

SECTION 5

DVME-624 THEORY OF OPERATION

5.1 Introduction

This section describes the operation of the DVME-624 in detail. Each circuit is described refering to the appropriate schematics. This section is provided for the user that wants to have a complete understanding of how the board operates. This manual is not designed to be used as a repair manual. All boards needing repair should be sent to DATEL. This section, however, may be used as a reference for simple trouble shooting purposes.

5.2 VMEbus Interface Logic
(Refer to Datel Dwg. No. D-14046 Sht 1)

VMEbus data lines D15 - D00 are buffered and inverted by octal bus tranceiver IC's U53 and U54 (74ALS640-1). The base address of the DVME-624 is decoded by octal comparator U48 (74ALS518) which compares the VMEbus Address lines A15 - A8 with the switch settings of DIP switch S1. The VMEbus Address Modifier lines AM5 - AM0 are decoded by 256 X 4 Bipolar PROM IC U50 (TBP24S10) and determines the address modifier code that the board responds to. Also, U50 decodes the VME Bus LWORD* and IACK* to prevent board response to either long word operations or during bus interrupt acknowledge. The VMEbus SYSCLK 16 MHz clock signal is divided by D F/F U45 pin 9 (74LS74) to produce a 8 MHz square wave which is used to clock Shift Register U47 (74LS164). This Shift Register is used to create the VMEbus Data Transfer Acknowledge signal (DTACK*) which may be delayed by jumper selection to accomodate slower CPU's. The VMEbus Control lines WRITE*, DS1*, DS0*, and SYSRESET* are buffered by Bus Receiver U51 (74LS244) and are decoded by U52 (PAL16L8) to produce several on-board control signals. These control signals are control the Board Select F/F U45-5, control the U53, U54 bus transceiver direction pins, latch the low eight VMEbus Address lines in U49 (74LS374), and to produce a negative Write Strobe Pulse at decoder U43 pin 4 (74LS138). This IC decodes the lower address lines to produce write strobes to the four D/A Channels. Bipolar PROM U46 (TBP18S030) is used as the Board ID PROM.

5.3 D/A Data Registers, Isolators, and D/A Converter Section (Refer to Datel Dwg. No. D-14046 Shts 2 and 3)

Since the four DAC sections are identical, all reference designations that follow pertain to DAC 0 (U2). The DAC Data Register for DAC 0 is composed of octal register U21 (74LS374) and half of dual 4-bit register U22 (74ALS874). The outputs of the DAC Data Register are used to drive the LED's of optoisolators U9 - U14. The output transistors of the optoisolators are used to provide the 12 DAC input data lines. The HI-5680V DAC, U2, is a 12-bit monolithic D/A Converter. U1, (XTR110) along with PNP darlington transistor Q1 (MPS-U95), converts a 0 to +10 Volt input from the DAC to a 4 to 20 mA Current Loop output. The circuit composed of U41 (74LS00) resets the DAC to 0 Volt output on power-up regardless of whether unipolar or bipolar output range is selected.

5.4 Isolated DC to DC Converter Section (Refer to Datel Dwg. No. D-14046 Sht 4)

The DC to DC Converter section converts +12 Volts from the VMEbus to the isolated +5 Volt and +/-15 Volt supplies required the the D/A Sections. Four isolated sets of outputs are provided. Channel to Channel and Channel to Bus isolation is provided by transformer T1. The center-tapped T1 primary is driven in a push-pull manner by power Mosfets Q5 and Q6 which are driven by Pulse Width Modulator IC U39 (UC3525A). The PWM is used as a free running 25 kHz oscillator and provides dead time between the push-pull outputs to prevent transistor destruction. Pulse by pulse current Limiting is provides by sensing primary current with op amp U40 which is used as a comparator. The voltage across current sensing resistor R32 is sensed by the comparator and activates the Shutdown input of the PWM if primary current reaches too high a level. Each secondary winding of T1 is rectified, filtered, and regulated using linear voltage regulators VR1 - VR12.

APPENDIX

Appendix A: Schematic
Appendix B: Assembly Drawing
Appendix C: D/A Calibration Table
Appendix D: Ordering Guide
Appendix E: DVME-624 Data Sheet
Sample Program

D/A CALIBRATION TABLE

UNIPOLAR			BIPOLAR		BIN CODE (hex)	2'S C CODE (hex)
0 - 5V	0 - 10V	4-20mA	+/-5V	+/-10V		
0.0000	0.0000	1.0000	-5.0000	-10.0000	0000	8000
0.0012	0.0024	1.0010	-4.9976	-9.9951	0010	8010
0.0024	0.0049	1.0020	-4.9951	-9.9902	0020	8020
0.0049	0.0098	1.0039	-4.9902	-9.9805	0040	8040
0.0098	0.0196	1.0078	-4.9805	-9.9609	0080	8080
0.0196	0.0391	1.0156	-4.9609	-9.9219	0100	8100
0.0391	0.0781	1.0312	-4.9219	-9.8437	0200	8200
0.0781	0.1563	1.0625	-4.8437	-9.6875	0400	8400
0.1563	0.3125	1.1250	-4.6875	-9.3750	0800	8800
0.3125	0.6250	1.2500	-4.3750	-8.7500	1000	9000
0.6250	1.2500	1.5000	-3.7500	-7.5000	2000	A000
1.2500	2.5000	2.0000	-2.5000	-5.0000	4000	C000
2.5000	5.0000	3.0000	0.0000	0.0000	8000	0000
3.7500	7.5000	4.0000	2.5000	5.0000	C000	4000
4.3750	8.7500	4.5000	3.7500	7.5000	E000	6000
4.6875	9.3750	4.7500	4.3750	8.7500	F000	7000
4.8437	9.6875	4.8750	4.6875	9.3750	F800	7800
4.9219	9.8437	4.9375	4.8437	9.6875	FC00	7C00
4.9609	9.9219	4.9688	4.9219	9.8437	FE00	7E00
4.9805	9.9609	4.9844	4.9609	9.9219	FF00	7F00
4.9902	9.9805	4.9922	4.9805	9.9609	FF80	7F80
4.9951	9.9902	4.9961	4.9902	9.9805	FFC0	7FC0
4.9976	9.9951	4.9980	4.9951	9.9902	FFE0	7FE0
4.9988	9.9976	4.9990	4.9976	9.9951	FFF0	7FF0

APPENDIX D

ORDERING INFORMATION

I. Isolated 4 Channel Digital-to-Analog Board

Model DVME-624 ___ ___

- 1 = 30 microsecond output settling time
- 2 = 6 microsecond output settling time
- V = Voltage output only (no current loop outputs)
- C = Both current and voltage outputs.

SAMPLE PROGRAM

```
   include wsmacs.lib      ;enable lower case

*************************************************************************
*
*  This simple program illustrates the use of the DVME-624,
*  DVME-626, and DVME-628 D/A boards.  The program runs on
*  VERSADOS systems.  It allocates the VME Bus Short I/O Space
*  using the GTSEG directive.  The program then writes a 12-bit
*  count sequence to DAC 2 producing a ramp on the DAC output.
*  The program loops endlessly.
*
*  This program must be modified for other operating systems or
*  other hosts. This program is offered "as is" and should be
*  fully tested by the user before committing it to an application.
*  The user may incorporate all or part of this program in his/her
*  application when used with Datel boards.
*
*************************************************************************

dacbase    equ     $ffffc900       ;standard base address of DAC
                                   ;boards
dac0       equ     $ffffc9a0       ;dac 0
dac1       equ     $ffffc9a2       ;dac 1
dac2       equ     $ffffc9a4       ;dac 2
dac3       equ     $ffffc9a6       ;dac 3
dac4       equ     $ffffc9a8       ;dac 4
dac5       equ     $ffffc9aa       ;dac 5
dac6       equ     $ffffc9ac       ;dac 6
dac7       equ     $ffffc9ae       ;dac 7

   section 0

start:
   lea.l   stack,sp          ; init stack

   move.l  #1,d0             ; load GTSEG directive
   lea.l   io_blk,a0         ; load parameter block adrs
   trap    #1                ; attach short io space to prog
   bne     rmserr            ; if ne - directive error

   clr.w   d0                ; data counter for dac

loop:
   move.w  d0,(dac2).l       ; store data
   addi.w  #$10,d0           ; dac data is left justified.
*                            ; use #$10 for DVME-624/628
*                            ; use #$04 for DVME-626

   bra     loop              ;loop forever
```

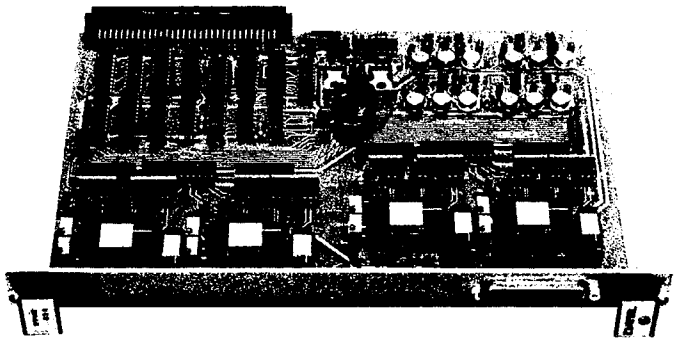
```
rmserr:
   move.l   #2,d0            ;deallocate short io segment

   lea.l    io_blk,a0
   trap     #1

   moveq    #15,d0           ;back to VERSADOS
   trap     #1

   section 10

*
*  RMS68K Segment Parameter Block to access short io space
*
   dc.w     0                ; ensure word boundary

io_blk:     dc.l     0       ; Task_id of 0 means seg is
   dc.l     0                ; for calling task
   dc.w     0                ; options
   dc.w     $0800            ; attributes - Seg is mem mapped i/o
   dc.l     'SHIO'           ; Segment Name
   dc.l     $ffff0000        ; logical = physical address
   dc.l     $00010000        ; length = 65K - all of shrt io space

*
*  STACK STARTS HERE
*
   ds.l     256

stack:      equ      *

   end
```

DVME-624
ISOLATED 4-CHANNEL, 12-BIT, VMEbus D/A BOARD

PRODUCT DATA SHEET

FEATURES

- **4-channel memory mapped D/A board**
- **300 VRMS channel-to-channel and channel-to-bus isolation**
- **Hardware compatible with VMEbus specifications**
- **On-board isolated dc-to-dc power converter**
- **Optional 6 μS or 30 μS settling time models**
- **12-bit resolution**
- **Choice of output voltages:**
  - **a. 0 to 5V dc**
  - **b. 0 to 10V dc**
  - **c. ±2.5V dc**
  - **d. ±5V dc**
  - **e. ±10V dc**
- **Optional 4-to-20mA current loop capability conforming to ISA standards**
- **±1/2 LSB differential non-linearity**
- **±0.05% full-scale range accuracy**



DATEL's DVME-624 IS A HIGH PERFORMANCE ANALOG OUTPUT PERIPHERAL TO A VMEbus-BASED HOST SYSTEM. THE BOARD PROVIDES ISOLATED ANALOG OUTPUTS IN DIFFERENT FULL-SCALE RANGES TO PERFORM IN A VARIETY OF APPLICATION ENVIRONMENTS. SUBJECTED TO RIGOROUS TESTING, THE BOARD IS AN IDEAL CHOICE FOR MOST REAL-TIME APPLICATIONS.

GENERAL DESCRIPTION

The DVME-624 is DATEL's 12-bit, 4-channel D/A board, totally compatible with VMEbus specifications. In a typical application the board provides analog outputs in real-time to the host system at a high speed. The different full-scale output voltage ranges the board offers conform to process control and test and measurement industrial requirements.

Each channel is configurable to different output voltage ranges. The salient feature of the DVME-624 board is the 300 VRMS channel-to-channel and channel-to-bus isolation. The board uses high performance optoisolators to provide the isolation. An on-board dc-to-dc power converter provides isolated power to each D/A converter section.

The isolation makes the DVME-624 an ideal choice for applications where a low-level signal superimposes a high voltage such as in testing of power supplies. The channel-to-bus isolation protects the host system against any catastrophic damages due to an external malfunction such as an actuator failure.

The DVME-624 offers ±1/2 LSB differential non-linearity and operates at ±0.05% full-scale range accuracy. The DVME-624 models are available at two different settling times. The DVME-624C1 and DVME-624V1 models offer 30 μS settling time and the DVME-624C2 and DVME-624V2 models offer 6 μS settling time. The DVME-624 may be obtained with an optional 4-to-20mA industrial current loop output in addition to the voltage outputs. Refer to the ordering information for models with current loop option.

Functionally, the digital data from the VME host system is transferred through a 12-bit data register to one-of-four D/A sections. The DVME-624 converts the 12 most significant bits from the VME data bus to an analog output. Data from the host system may be in straight binary, offset binary, or 2's complement coding. The D/A converter sections are optically isolated from the VME interface logic. The DVME-624 uses monolithic D/A converters to increase the product's reliability and endurance.

The DVME-624 D/A boards will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the DVME-624. The DVME-624 is shipped with an 68010 assembly language diagnostic program example on a 5 1/4" VERSAdos formatted diskette. The diagnostic program's source code is available in hardcopy from DATEL. Consult factory regarding the availability of the diagnostic program's source code in other disk formats.

ORDERING INFORMATION

DVME-624

- 1 — 30 μS Settling time
- 2 — 6 μS Settling time
- V — Voltage output only
- C — Voltage and 4-to-20 mA current loop output

VME Interface

The DVME-624 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to the address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-624 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems. Figure 1 shows the functional block diagram of the DVME-624 D/A board.

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, V_{exc} = +24V dc, R_{loop} = 250 ohms, unless otherwise specified.)

INTERFACE SPECIFICATIONS

Data Bus	16 bits
Address Bus	Short I/O Space, 16 address lines
Address modifiers codes	Codes used 29H, 2DH, 39H, and 3DH
Memory Mapping	Short I/O space, user or supervisor 256 bytes allocated per board

INTERNAL HARDWARE REGISTER/SOFTWARE ASSIGNMENTS

Register Memory Mapping

Relative Address	Function	READ/WRITE
0 through 63	Board Identification Code	Read Only
64 through 127	See Note 1	Read Only
128 through 159	See Note 2	Write Only
160	D/A Channel 0	Write Only
162	D/A Channel 1	Write Only
164	D/A Channel 2	Write Only
166	D/A Channel 3	Write Only
168 through 255	See Note 2	Write Only

Note 1: These addresses are redundant with ID PROM addresses, base + 0 through base + 63.

Note 2: These addresses are redundant in 8-byte blocks with the DAC data registers, base + 160 through base + 166.

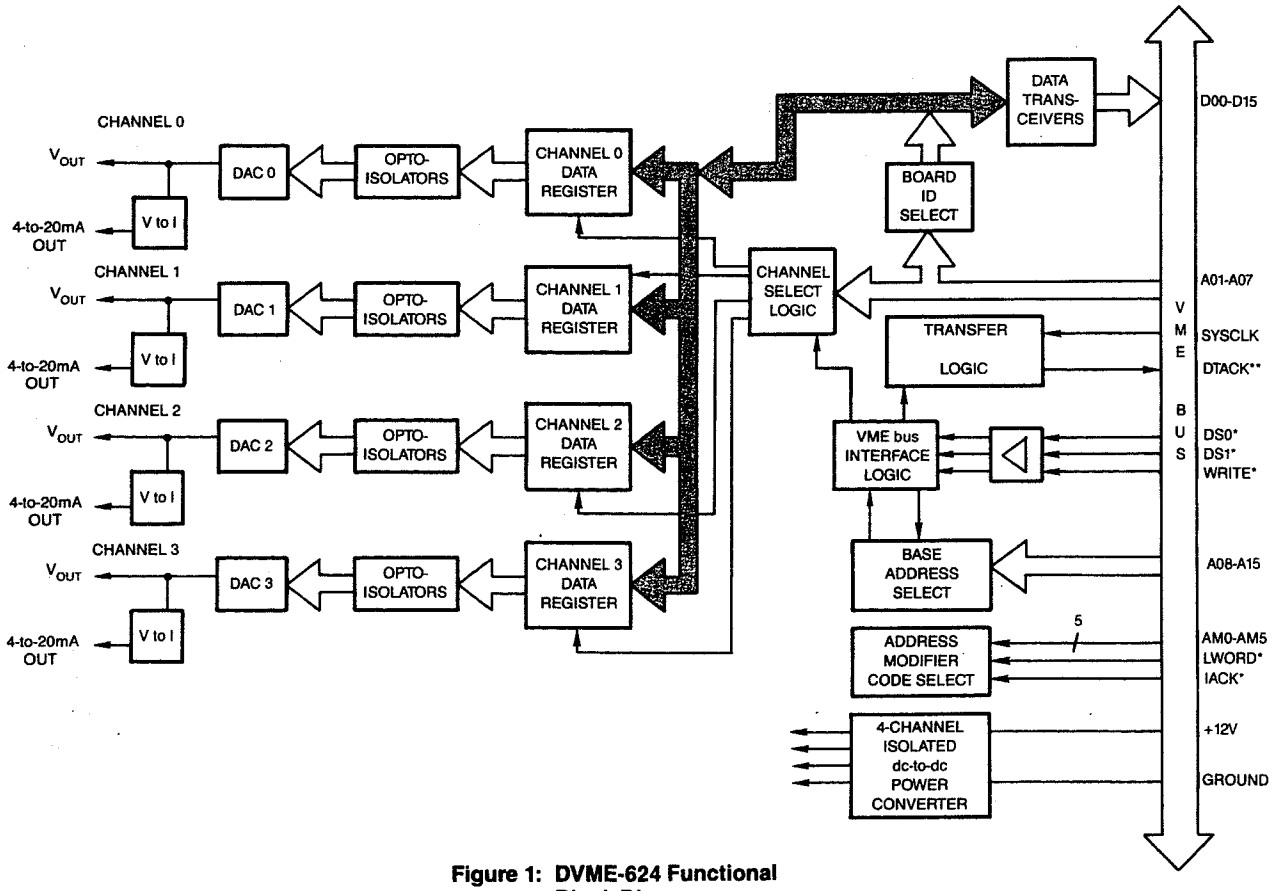


Figure 1: DVME-624 Functional Block Diagram

CONNECTOR SPECIFICATIONS

VME bus — P1 . . . . . 96-pin male DIN connector

Analog Output — J1 . . . . . 25-pin D Type female connector, Amp P/N 745783-1 or equivalent

ANALOG OUTPUT SPECIFICATONS

Number of Channels 4

Channel-to-channel Isolation . . . . . 300 VRMS, sustained maximum

Output full-scale voltage ranges . . . . . 0 to 5V dc
0 to 10V dc
±2.5V dc
±5V dc
±10V dc (standard)

Input data coding . . . . . Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary

Resolution . . . . . 12 Bits. Uses 12 most significant data bits from the data bus. Ignores bits D0 through D3.

Reset . . . . . Minus full-scale, output resets to 0.000V dc

Current Loop . . . . . 4-to-20 mA. Meets ISA standard 550.1 Type 4 Class U

Excitation Voltage (User-supplied) . . . . . 15 to 36V dc

PERFORMANCE

Specification	Minimum	Typical	Maximum
Accuracy	0.05% of FSR	—	—
Differential non-linearity	—	—	0.5 LSB
Zero temperature drift	—	3 ppm/°C	5 ppm/°C
Offset temperature	—	5 ppm/°C	10 ppm/°C
Gain temp drift	—	15 ppm/°C	30 ppm/°C
Settling time:			
DVME-624V1 DVME-624C1	—	—	30 µseconds
DVME-624V2 DVME-624C2	—	—	6 µseconds
Output current	—	±5 mA	—
Output impedance	—	50 milliohms	—

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1.0A typical, 1.2A maximum

+12V dc ±2.0% at 0.4A typical, .7A maximum

CURRENT LOOP

Specification	Minimum	Maximum
Accuracy	0.1% of FSR	—
Excitation (user-supplied)	15V dc	36V dc
Load resistance	100 Ohms	1000 Ohms
Isolation channel-to-channel	300 VRMS	—
Isolation output-to-bus	300 VRMS	—

PHYSICAL CHARACTERISTICS

Outline Dimensions . . . . . 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight . . . . . 9.6 oz (272.3 grams)

Operating temperature range . . . . . 0 to 60°C

Storage temperature range . . . . . −20 to +80°C

Relative humidity . . . . . 0 to 90%, non-condensing

DVME-624 ANALOG OUTPUT CONNECTOR J1

The DVME-624 provides analog outputs using the J1 connector. Depending on the model, the J1 connector contains voltage and current loop outputs. Figure 2 shows the output signals on the J1 connector.

PIN NUMBER	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	

Figure 2: Analog output pinout details

DVME-624 DATA FORMAT

The DVME-624 uses a 12-bit D/A converter for converting the digital data to analog signal. The board uses the 12 most significant bits of the VME data lines as input signals. Figure 3 shows the data format the DVME-624 is designed for.

15		4	3	2	1	0
MSB	DATA BITS	LSB	X	X	X	X
			Not Used by DVME-624			

Figure 3: DVME-624 data format

DVME-624 Board Identification Code

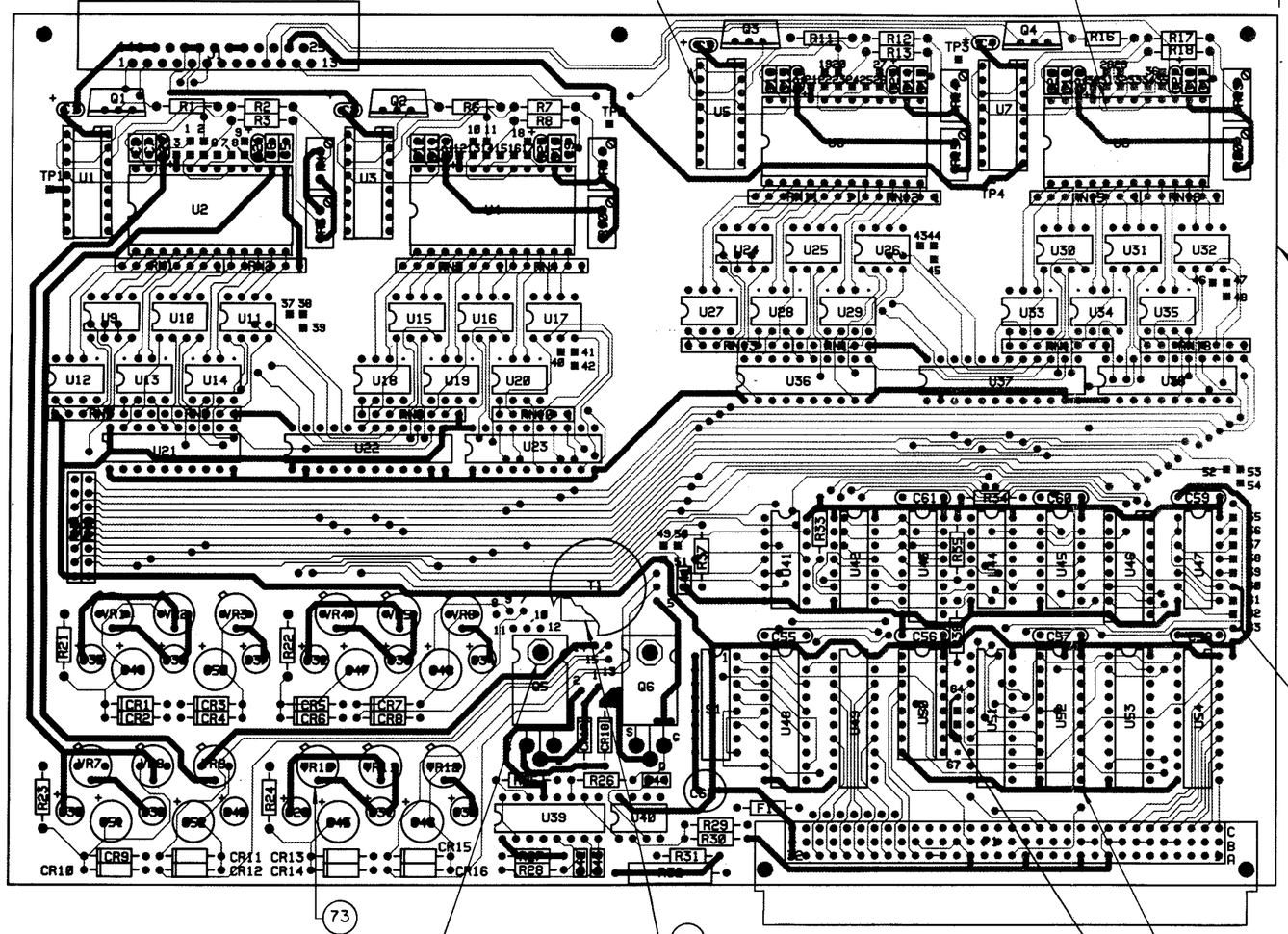
Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	2	
+ 1F	4	

DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DATEL, Inc. 11 CABOT BOULEVARD, MANSFIELD, MA 02048-1194 TEL. (508) 339-3000 / TELEX 174388/ FAX (508) 339-6356
OVERSEAS: DATEL (UNITED KINGDOM) Basingstoke Tel. (256) 469-085 • DATEL (FRANCE) Tel. (1) 3460.0101
DATEL (GERMANY) Tel. (89) 53-0741 • DATEL (JAPAN) Tokyo Tel. (3) 779-1031 • Osaka Tel. (6) 354-2025
For Applications Assistance, dial 1-800-233-2765

REV.	DESCRIPTION	DATE	APPD.
A	DWG. UNDER CHANGE CONT	2-7-85	
B	REV PER ECO 6599 SW	5/13/86	
C	REV PER ECO 6984R	6-1-88	
D	REV PER ECO 8815	10/25/90	

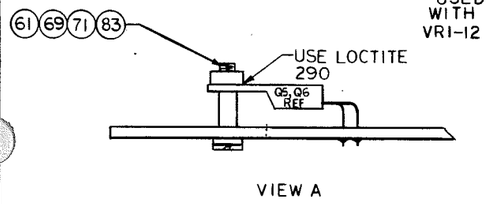


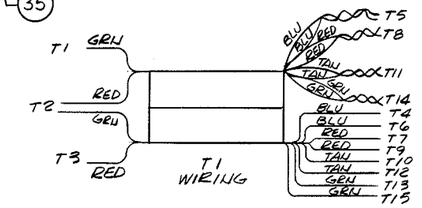
ANALOG OUTPUT JUMPERS (ITEM 65)				
DAC OUTPUT VOLTAGE RANGE	DAC 3	DAC 2	DAC 1	DAC 0
0 to +5V	35 to 36 30 to 31 33 to 34	26 to 27 21 to 22 24 to 25	17 to 18 12 to 13 15 to 16	8 to 9 3 to 4 6 to 7
0 to +10V	35 to 36 30 to 31	26 to 27 21 to 22	17 to 18 12 to 13	8 to 9 3 to 4
±2.5V	35 to 36 31 to 32 33 to 34	26 to 27 22 to 23 24 to 25	17 to 18 13 to 14 15 to 16	8 to 9 4 to 5 6 to 7
±5V	35 to 36 31 to 32	26 to 27 22 to 23	17 to 18 13 to 14	8 to 9 4 to 5
±10V (STANDARD)	34 to 35 31 to 32	25 to 26 22 to 23	16 to 17 13 to 14	7 to 8 4 to 5
4-20mA CURRENT LOOP	35 to 36 30 to 31 28 to 29	26 to 27 21 to 22 19 to 20	17 to 18 12 to 13 10 to 11	8 to 9 3 to 4 1 to 2

INPUT CODING	(ITEM 65) JUMPERS
UNIPOLAR BINARY	52 to 53 49 to 51
BIPOLAR OFFSET BINARY	49 to 50 52 to 53
BIPOLAR 2's COMP (STANDARD)	49 to 50 53 to 54

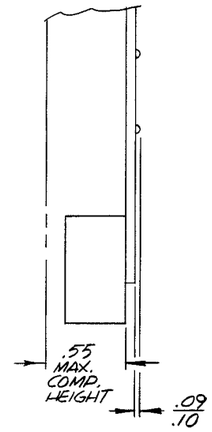
BOARD ACCESS MODE	ADDRESS MODIFIER CODE	(ITEM 84) JUMPER
SHORT NON-PRIV ACCESS STD	29_{16}	64 to 67
SHORT SUPERVISORY ACCESS	$2D_{16}$	64 to 68
STANDARD NON-PRIV ACCESS	39_{16}	64 to 65
STANDARD SUPERVISORY ACCESS	$3D_{16}$	64 to 66

SPEED MODEL	
MODEL	JUMPERS (ITEM 65)
DVME-624X1 30MS SETTING	37-38, 40-41 43-44, 46-47
DVME-624X2 6MS SETTING	38-39, 41-42 44-45, 47-48





NOTE: 1. ALL BLUE WIRES HAVE KNOTS
2. PRIMARY WIRES ARE #28 AWG. (HEAVY)



NOTE: SEE A-16905 FOR REF. DES CHART

FINAL	DVME 624	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS .XX ± .02 .XXX ± .005 FRACTIONS ± 1/64	DRAWN A.LEE	DATE 1/6/85	DATEL DVME 624
NEXT ASSY	USED ON		CHECKED	DATE 11-26-85	
APPLICATION			PROJ. ENG. ASW	DATE 12/4/85	SIZE D · CODE IDENT. NO. 50721 · DWG. NO. 14045 · REV. D
		MATERIAL LM14045	APPD.	DATE 12-4-85	SCALE 2/1 · SHEET 1 OF 1

REV.	DESCRIPTION	DATE	APPD.
A	DWG. UNDER ENG'R CONTROL	1-14-84	
B	REV PER ECO 6599	5/13/85	
C	U3,4,6 & 8 ADD /DAC-80 PER ECO 7234	8-13-87	

RESET

SYSRST* 1C-12
AS* 1A-18
DS1* 1A-12
DSØ* 1A-13
WRITE* 1A-14
IACKIN* 1A-21
IACKOUT* 1A-22
BGO IN 1B-4
BGO OUT 1B-5
SYSCLK 1A-10
BG1 IN 1B-6
BG1 OUT 1B-7
BG2 IN 1B-8
BG2 OUT 1B-9
BG3 IN 1B-10
BG3 OUT 1B-11

74LS244 U51

U52 PALCEUS SCH C-14659 PHS-13124

U45 74LS74

U42 74LS10Ø

U47 74LS138

U44 74S30

R36 1K

C55-C61 .01µF

C62 10pF

1A-16 DTACK*
1C-32
1B-32 + 5V
1A-32
1A-9,11,15,19
1B-20,23 GND
1C-9

SHT 2+3

D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04

RN8 4.7K RN7 4.7K

U46 TBP18S030

R34 1K

S1

U50 TBP14S10 74LS244

U48 74ALS518

U49 74LS374

U54 74ALS640-1

U53 74ALS640-1

P1

IACK* LWORD* AM5 AM4 AM3 AM2 AM1 AMØ

1A-2Ø 1C-13 1C-14 1A-23 1B-19 1B-18 1B-17 1B-16

1C-23 1C-24 1C-25 1C-26 1C-27 1C-28 1C-29 1C-3Ø

A15 A14 A13 A12 A11 A10 AØ9 AØ8

1A-24 1A-25 1A-26 1A-27 1A-28 1A-29 1A-3Ø

AØ7 AØ6 AØ5 AØ4 AØ3 AØ2 AØ1

1C-8 1C-7 1C-6 1C-5 1C-4 1C-3 1C-2 1C-1

D15 D14 D13 D12 D11 D1Ø D09 D08

1A-8 1A-7 1A-6 1A-5 1A-4 1A-3 1A-2 1A-1

DØ7 DØ6 DØ5 DØ4 DØ3 DØ2 DØ1 DØØ

NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE IN OHMS 1/4W ±5%.
2. CAPACITORS ARE IN MICROFARADS.

LAST REF DES USED	REF DES NOT USED
C62 F1 R37 Q6 RN18 T1 U54 CR18 VR12 J1 S1 P1 PTS 68	C53 54

D-14045
NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS .XX ± .....
.XXX ± .....
FRACTIONS ± .....
MATERIAL

DRAWN A.S.W 1/14/85
CHECKED 11-26-84
PROJ. ENG. ASW 12-19-84
APPR. 12-19-84

DATEL
SCHEMATIC
DVME - 624
SIZE D | CODE IDENT. NO. 50721 | DWG. NO. 14046 | REV. B
SCALE — | SHEET 1 OF 4

REV.	DESCRIPTION	DATE	APPD.
	SEE SHT 1		

DAC Ø V LOOP
DAC Ø I LOOP
DAC Ø V OUT
DAC Ø RTN
DAC 1 V LOOP
DAC 1 I LOOP
DAC 1 V OUT
DAC 1 RTN
J1
Q1 MPS-U95
Q2 MPS-U95
R1 100Ω
R6 100Ω
NC NC
U1 XTR110
U3 XTR110
TP1
TP2
+15V(A)
-15V(A)
+5V(A)
+15V(B)
-15V(B)
+5V(B)
R2 4.3M
R3 1.5M
R4 100K
R5 100K
R7 4.3M
R8 1.5M
R9 100K
R10 100K
C2 1µF 50V
C8 .01µF
U2 HI5680V/DAC-80
U4 HI5680V/DAC-80
RN1 10K
RN2 10K
RN3 10K
RN4 10K
U12
U9
U13
U10
U14
U11
U18
U15
U19
U16
U20
U17
RN5 330
RN6 330
RN9 330
RN10 330
+5V
U22 (B) 74ALS874
U21 74LS374
U22 (A) 74ALS874
U23 74LS374
U41 74LS08
R57 100Ω
C41 100pF
51 UNI
49 BIP
50
2'S. COMP
58 BIN
54
52
LDAC Ø (SHT 1)
RESET (SHT 3)
D15 (SHT 1)
D15 (SHT 1)
D14
D13
D12
D11
D10
D09
D08
D07
D06
D05
D04
(SHT 1,3)
LDAC 1 (SHT 1)
MSB (SHT 3)

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS .XX ± .__
.XXX ± .__
FRACTIONS ± __
MATERIAL

DRAWN A.S.W 6/4/85
CHECKED
PROJ. ENG.
APPD.
DATE

DATEL
SCHEMATIC
DVME-624
SIZE D
CAGE CODE
DWG. NO. 1402
SCALE
SHEET NO. 1

REV.	DESCRIPTION	DATE	APPD.
	SEE SHT 1		

DAC 2 V LOOP
DAC 2 I LOOP
DAC 2 V OUT
DAC 2 RTN
DAC 3 V LOOP
DAC 3 I LOOP
DAC 3 V OUT
DAC 3 RTN

J1
Q3 MPS-U95
Q4 MPS-U95
R11 100Ω
R16 100Ω
C3 1µF 50V
C4 1µF 50V
NC NC
U5 XTR110
U7 XTR110
TP3
TP4
R15 100K
R20 100K
R13 1.5M
R18 1.5M
C13 .01
C25 1µF
C14 .01
C26 1µF
C15 .01
C27 1µF
C28 1µF
C17 .01
C18 .01
C19 .01
+15V(C)
-15V(C)
+15V(D)
-15V(D)
R14 100K
R12 4.3M
C16 .01µF
R17 4.3M
C29 .01µF
GAIN
U6 HI5050/DAC-80
U8 HI5050/DAC-80
REF OUT
REF IN
+5V(C)
+5V(D)
RN11 10K
RN12 10K
RN15 10K
RN16 10K
U27
U24
U28
U25
U29
U26
U33
U30
U34
U31
U35
U32
RN13 330
RN14 330
RN17 330
RN18 330
+5V
U37 (B) 74ALS874
U36 74LS374
U37 (A) 74ALS874
U38 74LS374
U41 74LS08
U44 74S38
U42 74LS10
R33 1K
4Q 3Q 2Q 1Q
4D 3D 2D 1D
8Q 7Q 6Q 5Q 4Q 3Q 2Q 1Q
8D 7D 6D 5D 4D 3D 2D 1D
CLR GND OC Vcc

LDAC (SHT 1)
RESET (SHT 2)
MSB (SHT 2)
D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04
(SHT 1,2)
LADC 3 (SHT 1)

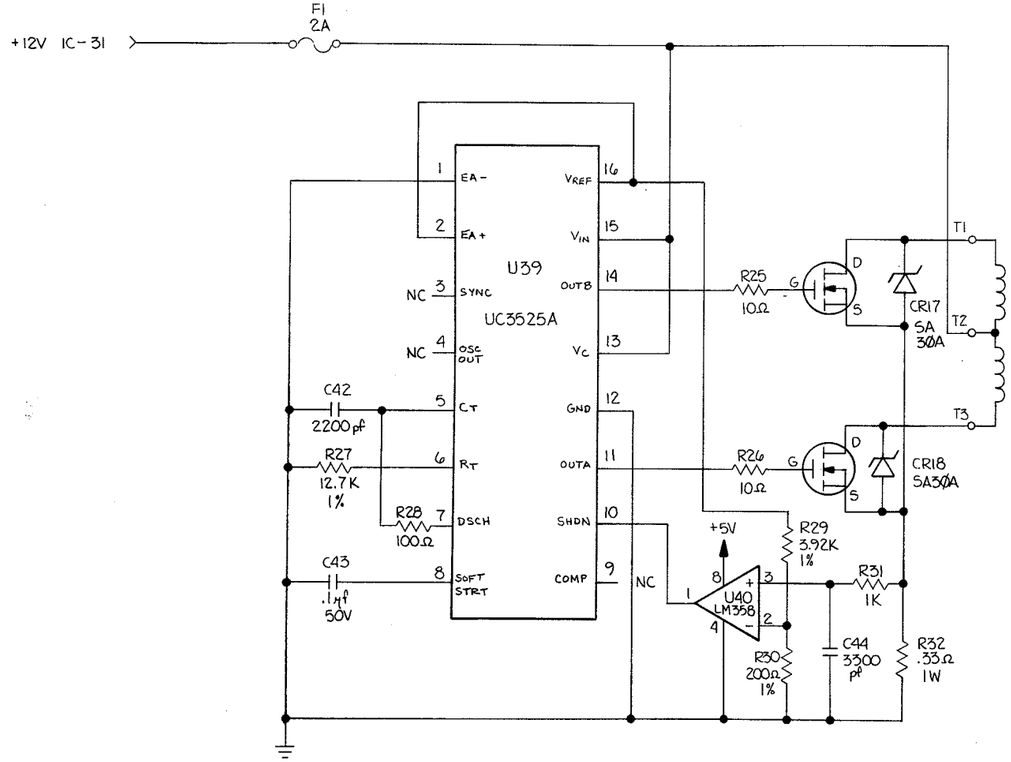
NEXT ASSY	USED ON		
APPLICATION			

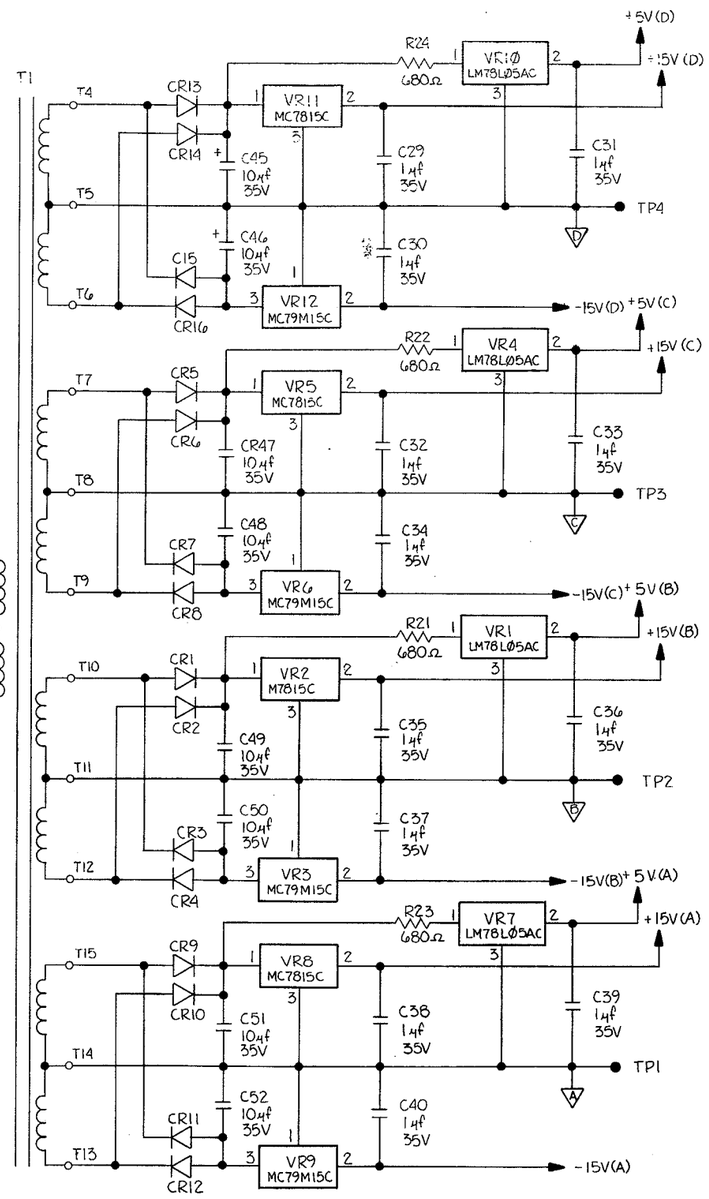
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
TOLERANCES: DECIMALS .XX ± .XXX ± FRACTIONS ±
MATERIAL

DRAWN A.S.W DATE 6/4/85
CHECKED DATE
PROJ. ENG. DATE
APPD. DATE

DATEL
SCHEMATIC
DVME - 624
SIZE D | CODE IDENT. NO. 50721 | DWG. NO. 14046 | REV. E
SCALE | SHEET 3 OF 4

REV.	DESCRIPTION	DATE	APPD.
	SEE SHT 1.		





NOTES:

1. DIODES ARE IN4148.
2. REGULATORS ARE T-39 CASE.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS .XX ± ___
.XXX ± ___
FRACTIONS ± ___
MATERIAL

DRAWN — DATE
CHECKED — DATE
PROJ. ENG. — DATE
APPD. — DATE

DATEL

SCHEMATIC
DVME - 624

SIZE	CODE IDENT. NO.	DWG. NO.	REV.
D	50721	14046	C

SCALE — SHEET 4 OF 4