NI PXI-5404

100 MHz Frequency Generator

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100 MHz Frequency Generator

NI PXI-5404

- 1 channel updated at 300 MS/s
- 9 kHz to 105 MHz sine wave
- DC to 100 MHz clock
- 1.07 µHz frequency resolution
- 1 to 4 V_{pp} sine amplitude
- 12-bit vertical resolution
- ±0.2 dB flatness of sine wave passband (9 kHz to 100 MHz)
- Ideal for coherent sampling applications
- Phase-lock loop for synchronization to other devices and PXI backplane

Operating Systems
- Windows 2000/NT/XP/Me/9x

Recommended Software
- LabVIEW
- LabWindows/CVI

Other Compatible Software
- Visual Basic
- C/C++

Driver Software (included)
- NI-FGEN

Calibration Certificate Included

New

Overview

The National Instruments PXI-5404 is a 100 MHz frequency generator packaged in 1-slot PXI module. It generates sine and clock outputs simultaneously at up to 100 MHz with 1.07 µHz resolution. By using direct digital synthesis (DDS) and precise phase-lock loop circuitry, the PXI-5404 generates stable, accurate sine and clock outputs of which you can programmatically adjust the amplitude, frequency, and phase of the sine and clock outputs as well as the duty cycle of the clock output.

The PXI-5404 is a versatile, cost-effective, sine wave generator with output levels ranging from 1 to 2 V_{pp} into a 50 Ω load with 12-bit resolution, excellent frequency resolution, and passband flatness. Stimulus-response instruments such as network analyzers and ATE test systems will benefit from using the PXI-5404 as the sine stimulus because of its passband flatness, and its frequency accuracy and resolution.

The PXI-5404 can also serve as a programmable clock generator for ATE systems because of its 1.07 µHz frequency resolution, duty-cycle adjustability from 25 to 75 percent, and programmable voltage levels of 5, 3.3, or 1.8 V into high-impedance loads.

Ideal for Coherent Clocking Applications

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pxi5404

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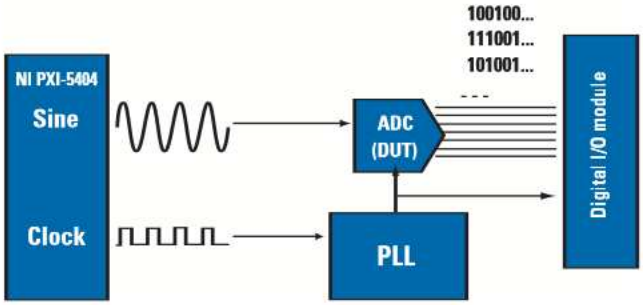
With the simultaneous sine and clock outputs, you can employ coherent clocking to reduce the test time of your device under test (DUT) and eliminate the need for antialias filtering. Because you have a precise phase and frequency relationship between the analog stimulus and the sample clock, there is no need for window-weighting functions in your FFTs for spectral analysis, thus reducing the need to sample the DUT over several cycles of the sine stimulus. With a coherent clocking system, you know both the analog stimulus and the sampling clock frequencies, thus eliminating the need for antialias filters or time-domain window functions. In a coherent sampling system, all the power from the signal and its accompanying harmonics fall into predictable frequency bins.



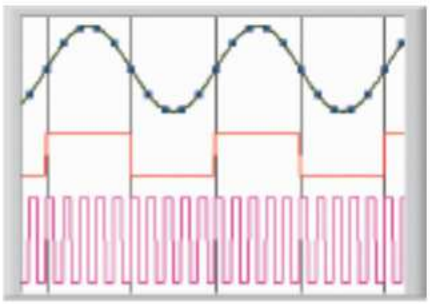


Figure 1. A typical coherent sampling application is the testing of analog-to-digital converters (ADCs). Here the sine stimulus is fed to the ADC and the clock output is phase locked and multiplied to yield a sampling clock to the ADC and to a digital pattern generator/analyzer.

NATIONAL INSTRUMENTS

100 MHz Frequency Generator

Programmable Clock Output Levels for TTL/CMOS

The PXI-5404 has programmable voltage output levels of 5, 3.3, and 1.8 V into high impedance loads and 2.5, 1.65, and 0.9 V into a 50 Ω load. With the flexible clock output levels, the PXI-5404 can address both TTL and CMOS technologies thereby making it an attractive clock source for ATE systems. Additionally an external DC blocking capacitor can be used to shift the outputs to other popular logic levels such as LVPECL and PECL.

Superior Leveled Sine Output Accuracy

The PXI-5404 employs an onboard amplitude-leveling compensation scheme whereby the specified output level enjoys excellent accuracy of ±0.2 dB within the passband of 9 kHz to 100 MHz. In Figures 2 and 3 the effects of the output leveling technique can be seen clearly. This level accuracy makes the PXI-5404 an ideal source for many applications such as communications and ATE, where amplitude accuracy is a key requirement.

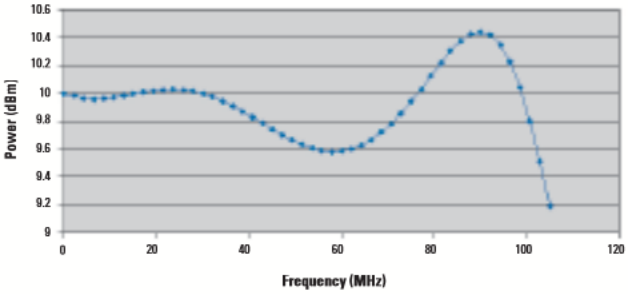


Figure 2. NI PXI-5404 Passband Flatness without Onboard Compensation

Phase-Lock Loop for Synchronization

The phase-lock loop on the PXI-5404 synchronizes sine and clock generation to an external clock. The reference clock source may come from the front panel connector CLK IN, the PXI 10 MHz reference clock on the PXI backplane, or the PXI trigger bus. The PXI-5404 phase-locks to frequencies from 3 to 20 MHz in 1 MHz increments. The PXI-5404 can also operate without an external reference frequency by using its onboard frequency source.

Using phase-lock loops, you can synchronize two or more PXI-5404 sources to within 0.022 deg in phase for outputs up to 100 MHz. Consequently, you can build a high-performance multichannel source on the PXI platform. Thus, with the PXI-5404 you can address applications such as in automotive and video test that require multiple clock frequencies that are phase locked in precise phase relationships.

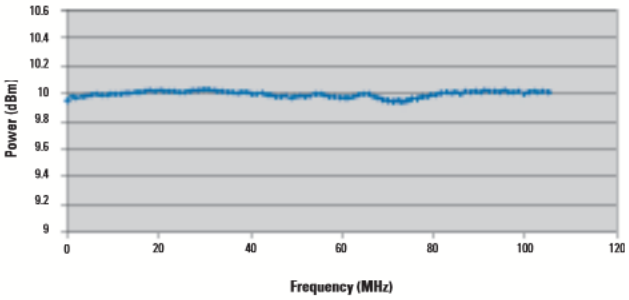


Figure 3. NI PXI-5404 Passband Flatness with Onboard Compensation

Triggering

The sine and clock outputs can run continuously or you can use triggering controls to start sine and clock generation. Trigger sources can be either external or internal (software trigger). External triggers can be received from the front panel connector PFI0, the PXI trigger bus, or the PXI star trigger bus. You can also change the operating frequency, amplitude, and phase of the PXI-5404 output from one of these sources.

Calibration

Every PXI-5404 is factory calibrated and shipped with a calibration certificate verifying that it meets NIST-traceable standards. Periodically, you can externally calibrate the PXI-5404 (provided you have the expertise and equipment), or you can ship it to National Instruments or a qualified metrology lab. External calibration is usually performed on an annual basis. Visit ***ni.com/calibration*** for more information about calibration services.

I/O Connector

The PXI-5404 has five SMB connectors labeled SINE, CLOCK, REF IN, REF OUT, and PFI0. The sine and clock outputs are accessed on SINE and CLOCK, respectively, and an external reference frequency for the phase-lock loop is fed to the REF IN connector. The REF OUT connector is a truly versatile output connector that can route out a signal from multiple sources, including the onboard VCXO reference (divided by 1 to 255), the star trigger bus, the PXI trigger bus, PFI0 connector, and the PXI 10 MHz reference clock. The PFI0 connector is a bidirectional connector. As an input, the PFI0 connector can accept a trigger that initiates sine and clock generation from an external source. As an output, the PFI0 connector can route out the same set of signals as the REF OUT connector.

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Software

If you want to build an automated test application or integrate the PXI-5404 in your test software, use the IVI-compliant NI-FGEN instrument driver with:

- NI LabVIEW
- NI LabWindows/CVI
- Microsoft Visual Basic
- Microsoft Visual C/C++

NI-FGEN comes with a comprehensive set of examples that illustrate the programming and features of the PXI-5404 in all four programming environments. Because NI-FGEN offers simulation mode, you can run your application on a laptop PC, for example. Thanks to this feature, you can develop your application with the PXI-5404 remotely or a team of developers can work on an application without the need for hardware in their systems.

Interactive Control

The PXI-5404 comes with the versatile Sources Soft Front Panel with which you can interactively control the PXI-5404. You can generate sine and clock outputs with control of frequency, phase, amplitude, and duty cycle with the Sources Soft Front Panel. Furthermore, you can run the PXI-5404 in simulation mode from the Sources Soft Front Panel.

Ordering Information

NI PXI-5404 778577-01

Includes the module, NI-FGEN, Sources Soft Front Panel, and calibration certificate.

Specifications

Specifications are valid for the Operating Temperature Range, unless otherwise noted.

Output Characteristics

Number of outputs ..... 1 sine and 1 clock, Both generate same frequency simultaneously.

CH0 SINE (Channel 0 Sine Wave Output, I/O Panel Connector)

Connector ..... SMB
Frequency Range ..... 9 kHz to 105 MHz
Frequency Resolution ..... 1.07 µHz
Phase Range ..... 0 to 359.978 deg
Phase Resolution ..... 16384 steps including endpoints (approximately 0.022 deg)
Output Impedance ..... 50 Ω ±4% (9 kHz to 105 MHz)
Output Protection ..... 10 V_{rms}
Sampling Rate ..... 300 MS/s
Amplitude Range
  Open load ..... 4.00 V_{pp} to 2.00 V_{pp}
  50 Ω load ..... 2.00 V_{pp} to 1.00 V_{pp}
Amplitude Resolution ..... 2048 steps including endpoints (Open Load: Approximately 977 µV. 50 Ω Load: Approximately 489 µV)
Amplitude Accuracy ..... ±1% @ 50 kHz
Amplitude Passband Flatness ..... ±0.2 dB relative to the amplitude @ 50 kHz, 9 kHz < f <105 MHz
Amplitude Temperature Coefficient ..... ±0.013% / °C
Vertical Resolution ..... 12 bits @ 4 V_{pp} (open load)
11 bits @ 2 V_{pp} (open load)
Bandwidth ..... 105 MHz (0.2 dB)
Filter ..... Analog 7-pole elliptical

SINAD	1 MHz	+ 51 dB	Amplitude set to 1.8 V_{pp} (~ –1 dBFS). Measured from 9 kHz to 150 MHz.
	10 MHz	+ 48 dB	
	20 MHz	+ 45 dB	
	50 MHz	+ 42 dB	
	100 MHz	+ 42 dB	
SFDR	1 MHz	- 55 dBc	Amplitude 1.8 V_{pp} (~ –1 dBFS). Measured from 9 kHz to 150 MHz Includes harmonics.
	10 MHz	- 54 dBc	
	20 MHz	- 49 dBc	
	50 MHz	- 45 dBc	
	100 MHz	- 53 dBc	
THD	1 MHz	- 56 dB	Amplitude 1.8 V_{pp} (~ –1 dBFS). Includes 2nd through the 6th harmonic.
	10 MHz	- 52 dB	
	20 MHz	- 48 dB	
	50 MHz	- 41 dB	
	100 MHz	- 36 dB	
Average Noise Density	0.126 µVrms / √Hz - 125 dBm / Hz		Integrated from 9 kHz to 150 MHz

CH0 CLOCK (Channel 0 Clock Output, I/O Panel Connector)

Connector ..... SMB
Frequency Range ..... DC to 105 MHz
Frequency Resolution ..... 1.07 µHz
Phase Range ..... 0 to 359.978 deg
Phase Resolution ..... 16384 steps including endpoints
Output Impedance ..... 50 Ω ±12%, (DC to 105 MHz)
Output Protection ..... +8 to -4 V

Output	5.0 V Level		3.3 V Level		1.8 V Level		Typical
Current	120 mA		72 mA		48 mA		Source or Sink
Amplitude	5.0 V Level		3.3 V Level		1.8 V Level		
(Open Load)	Min	Max	Min	Max	Min	Max	
V_{OL}	-0.10 V	0.40 V	-0.10 V	0.40 V	-0.10 V	0.40 V	
V_{OH}	4.00 V	5.30 V	2.60 V	3.70 V	1.40 V	2.20 V	
Amplitude	5.0 V Level		3.3 V Level		1.8 V Level		If the CH0 CLOCK out signal
(50 Load)	Min	Max	Min	Max	Min	Max	is terminated into a 50 Ω load
V_{OL}	-0.10 V	0.20 V	-0.10 V	0.20 V	-0.10 V	0.20 V	the voltage levels will be
V_{OH}	2.00 V	2.65 V	1.30 V	1.85 V	0.70 V	1.10 V	divided by two.

Rise/Fall Time ..... 4 ns
Duty Cycle Range ..... 25 to 75%
Duty Cycle Accuracy ..... (Typical 1.07 µHz to 60 MHz)
  30 to 70% ..... ±2%
  25 and 75% ..... ±3%

PFI 0 (Programmable Function Interface, I/O Panel Connector)

Connector ..... SMB
Direction ..... Bidirectional
Frequency Range ..... DC to 20 MHz

As an Input

Destination for Input Signal ..... 1. PXI_Trig <0:7> (Backplane Connector)
2. REF OUT (I/O Panel SMB Connector)
3. Start Trigger
Input Resistance ..... 1 kΩ ±1%
Input Protection ..... +8 to -4
V_{IH} ..... 2.0 V
V_{IL} ..... 0.8 V
Output Protection ..... +8 to -4V

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Specifications (continued)

As an Output

Sources for Output Signal	1. PXI_CLK10 (backplane connector) 2. Sample timebase clock (60 MHz) divided by N ($3 \le N \le 255$) 3. REF IN (I/O panel SMB connector) 4. PXI_TRIG <0:7> (backplane connector) 5. PXI star trigger (backplane connector) 6. CLOCK output on CH 0 (I/O panel SMB connector) 7. Software trigger 8. Start trigger
Output Impedance	50 Ω ± 5%
Output Protection	+6 to -1 V
V_{OH} (Minimum)	
Open load	4.0 V
50 Ω load	2.0 V
V_{OL} (Maximum)	
Open load	0.4 V
50 Ω load	0.2 V
Rise/Fall Time	4 ns

REF IN (Reference Input, I/O Panel Connector)

Connector	SMB
Frequency Range	200 kHz to 30 MHz
Destinations	1. PLL reference (refer to "Phase-Lock Loop (PLL)") 2. REF OUT (I/O panel SMB connector) 3. PFI 0 (I/O panel SMB connector) 4. PXI_TRIG <0:7> (backplane connector)
Input Impedance	1 kΩ ±1%
Input Protection	12 V_{pp} (sine or square wave) ±5 VDC
Amplitude	300 mV_{pp} to 5 V_{pp} Sine or square wave
Input Coupling	AC

REF OUT (Reference Output, I/O Panel Connector)

Connector	SMB
Frequency Range	DC to 20 MHz
Sources	1. PXI_CLK10 (backplane connector) 2. Sample timebase (60 MHz) divided by N ($3 \le N \le 255$). 3. REF IN (I/O panel SMB connector) 4. PXI_TRIG <0:7> (backplane connector) 5. PXI star trigger (backplane connector) 6. CH 0 CLOCK output (I/O panel SMB connector) 7. PFI 0 (I/O panel SMB connector) 8. Software trigger 9. Start trigger
Output Impedance	50 Ω ±5 %, DC to 20 MHz
Output Protection	+6 to -1 V
V_{OH}	
Open load	4.0 V
50 Ω load	2.0 V
V_{OL}	
Open load	0.4 V
50 Ω load	0.2 V
Rise/Fall Time	4 ns

Triggers

Type	Start trigger
Sources	1. PFI 0 (I/O Panel SMB Connector) 2. PXI_TRIG<0:7> (backplane connector) 3. PXI star trigger (backplane connector) 4. Software (use function call) 5. Immediate (do not wait for a trigger). Default.
Mode	Continuous
Trigger Detection	Edge (rising)
Pulse Width (Minimum)	10 ns
Trigger to SINE Output Delay	250 µs, typical

Sample Clock

Frequency	300 MS/s
Average Phase Noise Density (PLL Reference set to REF IN)	-112 dBc/Hz 10 MHz SINE output Offset 10 kHz ±500 Hz

Phase-Lock Loop (PLL)

PLL Reference Sources	1. PXI_CLK10 (backplane connector) 2. REF IN (I/O panel SMB connector) 3. PXI_TRIG <0:7> (backplane connector) 4. None (The PLL is not used. See Internal Clock section). Default.
Frequency Accuracy	When using the PLL, the frequency accuracy of the NI PXI-5404 is solely dependent on the frequency accuracy of the PLL Reference Source.
Lock Time	200 ms, typical
PLL Reference Frequencies	3 to 20 MHz in 1 MHz increments
Frequency Locking Range	±50 ppm
PLL Reference Duty Cycles	30 to 70%

Internal Clock

Clock Source	Clock circuitry can either be locked to a reference signal using the PLL, or use an onboard frequency reference
Frequency Accuracy	±2 ppm, typical for 15 to 35 °C Calibrated at room temperature.
Frequency Temperature Coefficent	±0.3 ppm/°C

Multimodule Synchronization

Output skew of multiple NI 5404s	±1 ns Note: Two or more PXI-5404s can be programmatically phase-aligned after generation has started.
PLL Reference Frequencies for Multimodule Synchronization	3, 4, 5, 6, 10, 12, 15, or 20 MHz.

External Calibration (Factory Calibration)

Recommended Calibration Interval	1 year
Warm-up time	15 minutes

Power Requirements

(SINE output, CLOCK output, and REF OUT generating maximum amplitude waveforms into 50 loads).

+3.3 V	1000 mA
+5 V	550 mA
+12 V	180 mA
-12 V	50 mA

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Specifications (continued)

Physical

Dimensions	16.0 by 10.0 cm
(1 3U PXI Slot)	(6.3 by 3.9 in.)
I/O Panel Connectors	
CH0 SINE	SMB male
CH0 CLOCK	SMB male
PFI 0	SMB male
REF IN	SMB male
REF OUT	SMB male
I/O Panel Indicators	
Access LED	Off: Not ready Green: Ready to be accessed by software Amber: Accessed by computer or controller
Active LED	Off: Disabled or in a stopped state Red: Error (PLL unlocked or software detected an error) Green: Generating a waveform Amber: Waiting for a trigger

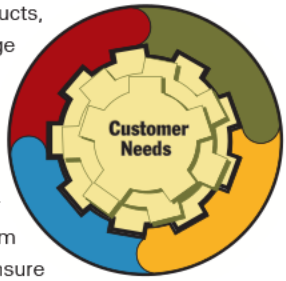
Environment

Operating Temperature	0 to 50 °C
Storage Temperature	-20 to 70 °C

Notes

1. Output voltage amplitudes assume a 50 Ω load, unless otherwise noted.
2. SINE output voltage amplitude set to 2 V_{pp}, unless otherwise noted. Load of 50 Ω unless otherwise noted.
3. CLOCK level set to 5 V, unless otherwise noted.
4. Typical specifications are determined on a small sampling of PXI-5404 modules.
5. Guaranteed by Design specifications are not tested in production.
6. 100% tested specifications are measured on every unit.

NI Services and Support



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