NI PXIe-6545

200MHz Digital Waveform Generator/Analyzer

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SPECIFICATIONS
NI PXIe-6544/6545/6547/6548

100/200 MHz Digital Waveform Generator/Analyzer

このドキュメントには、日本語ページも含まれています。

This document provides the specifications for the NI PXIe-6544 (NI 6544), NI PXIe-6545 (NI 6545), NI PXIe-6547 (NI 6547), and NI PXIe-6548 (NI 6548).

Maximum and *minimum* specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Typical specifications are unwarranted values that are representative of a majority (3σ) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature.

Nominal specifications are unwarranted values that are relevant to the use of the product and convey the expected performance of the product.

All specifications are *Typical* unless otherwise noted. These specifications are valid within the operating temperature range. Specifications are subject to change without notice. For the most recent NI 6544/6545/6547/6548 specifications, visit `ni.com/manuals`. To access the NI 6544/6545/6547/6548 documentation, including the *NI Digital Waveform Generator/Analyzer Getting Started Guide*, which contains functional descriptions of the NI 6544/6545/6547/6548 signals and the connector pinouts, navigate to **Start»Programs»National Instruments»NI-HSDIO»Documentation**.

Hot Surface If the NI 6544/6545/6547/6548 has been in use, it may exceed safe handling temperatures and cause burns. Allow time to cool before removing the NI 6544/6545/6547/6548 from the chassis.

Note All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

Contents

Channel Specifications

Specification	Value		Comments
Number of data channels	**NI 6544/6545**	**NI 6547/6548**	Data rate multiplier is software selectable to be SDR or DDR. Using SDR, data is clocked using the rising or falling edge of the Sample clock. Using DDR, data is clocked using both edges of the Sample clock.
	32 single data rate (SDR) channels	32 single data rate (SDR) channels *or* 16 double data rate (DDR) channels per direction *or* 24 channels when configured for extended data mode. This mode is used for hardware comparison and cycle-to-cycle tristate operations. **Note**: Generation and acquisition sessions may be independently configured for DDR operation on either the lower data channels (<0..15>) or the upper data channels (<16..31>).	
Direction control of data channels	Per channel, per operation	Per channel, per cycle	Per cycle direction control is supported when in extended data mode.
Time to tristate (t_{PZ})	6.2 ns		Nominal into a 2 kΩ and 15 pF load.
Number of programmable function interface (PFI) channels	4		Refer to the *Waveform Specifications* section for more details.

Specification	Value	Comments
Direction control of PFI channels	Per channel	—
Number of clock terminals	2 input 2 output	Refer to the *Timing Specifications* section for more details.

Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)

Specification	Value		Comments
Generation signal type	Single-ended		—
Number of programmable generation voltage levels	1 Voltage high level (V_{OH}) Generation Voltage Low Level (V_{OL}) is always set to 0 V. **Note**: Generation and acquisition sessions share a common programmable voltage resource. For simultaneous operations, acquisition thresholds must be set to half of the Generation Voltage High Level setting.		NI 6547/ 6548 only; for all data, PFI, and clock channels.
Generation voltage range	1.2 V to 3.3 V		
Generation voltage resolution	100 mV		
DC generation voltage accuracy	**Typical** ±35 mV	**Maximum** ±200 mV	Into 1 MΩ; does not include system crosstalk.

<table>
<tr><th>Specification</th><th colspan="5">Value</th><th>Comments</th></tr>
<tr><td>Generation logic families</td><td colspan="5">1.2V, 1.5V, 1.8V, 2.5V, 3.3V Logic Families
Generation and acquisition sessions share a common voltage resource. Simultaneous operations must be set to the same logic family.</td><td rowspan="7">All devices; for all data, PFI, and clock channels.
Nominal values have ±35 mV typical accuracy with a 1 MΩ load.
Does not include system crosstalk.</td></tr>
<tr><td rowspan="6">Generation voltage levels</td><td rowspan="2">Logic Family</td><td colspan="2">Voltage Low Levels</td><td colspan="2">Voltage High Levels</td></tr>
<tr><td>Nominal</td><td>Max</td><td>Min</td><td>Nominal</td></tr>
<tr><td>1.2V (V_{OH} = 1.2 V)</td><td>0.0 V</td><td>0.2 V</td><td>1 V</td><td>1.2 V</td></tr>
<tr><td>1.5V (V_{OH} = 1.5 V)</td><td>0.0 V</td><td>0.2 V</td><td>1.3 V</td><td>1.5 V</td></tr>
<tr><td>1.8V (V_{OH} = 1.8 V)</td><td>0.0 V</td><td>0.2 V</td><td>1.6 V</td><td>1.8 V</td></tr>
<tr><td>2.5V (V_{OH} = 2.5 V)</td><td>0.0 V</td><td>0.2 V</td><td>2.3 V</td><td>2.5 V</td></tr>
<tr><td>3.3V (V_{OH} = 3.3 V)</td><td>0.0 V</td><td>0.2 V</td><td>3.1 V</td><td>3.3 V</td></tr>
<tr><td>Output impedance</td><td colspan="5">50 Ω</td><td>Nominal.</td></tr>
<tr><td rowspan="6">Maximum allowed DC drive strength per channel</td><td colspan="3">Logic Family</td><td colspan="2">Maximum Allowed DC Drive Strength</td><td rowspan="6">Nominal.</td></tr>
<tr><td colspan="3">1.2V</td><td colspan="2">±12 mA</td></tr>
<tr><td colspan="3">1.5V</td><td colspan="2">±15 mA</td></tr>
<tr><td colspan="3">1.8V</td><td colspan="2">±18 mA</td></tr>
<tr><td colspan="3">2.5V</td><td colspan="2">±25 mA</td></tr>
<tr><td colspan="3">3.3V</td><td colspan="2">±33 mA</td></tr>
<tr><td>Data channel driver enable/ disable control</td><td colspan="5">Per channel</td><td>Software-selectable.</td></tr>
<tr><td>Channel power-on state</td><td colspan="5">Drivers disabled, 50 kΩ nominal input impedance</td><td>—</td></tr>
<tr><td>Output protection</td><td colspan="5">The device can indefinitely sustain a short to any voltage between 0 V and 5 V.</td><td>—</td></tr>
</table>

Acquisition Channels (Data, STROBE, and PFI <0..3>)

<table>
<tr><th>Specification</th><th colspan="5">Value</th><th>Comments</th></tr>
<tr><td>Acquisition signal type</td><td colspan="5">Single-ended</td><td>—</td></tr>
<tr><td>Number of programmable acquisition thresholds</td><td colspan="5">1 voltage threshold ($V_{IH} = V_{IL}$)
Note: Generation and acquisition sessions share a common programmable voltage resource. For simultaneous operations, Generation Voltage High Level must be set to twice the Acquisition Voltage Threshold.</td><td rowspan="3">NI 6547/6548 only; for all data, PFI, and clock channels.</td></tr>
<tr><td>Acquisition Voltage Threshold range</td><td colspan="5">0.6 V to 1.65 V</td></tr>
<tr><td>Acquisition Voltage Threshold resolution</td><td colspan="5">50 mV</td></tr>
<tr><td rowspan="2">DC Acquisition Voltage Threshold accuracy</td><td colspan="2">Typical</td><td colspan="3">Maximum</td><td rowspan="2">Does not include system crosstalk.</td></tr>
<tr><td colspan="2">±150 mV</td><td colspan="3">±30%</td></tr>
<tr><td>Acquisition logic families</td><td colspan="5">1.2V, 1.5V, 1.8V, 2.5V, 3.3V Logic Families
Note: Generation and acquisition sessions share a common voltage resource. Simultaneous operations must be set to the same logic family.</td><td rowspan="7">All devices; for all data, PFI, and clock channels.
Does not include system crosstalk.</td></tr>
<tr><td rowspan="7">Acquisition Voltage Thresholds</td><td rowspan="2">Logic Family</td><td colspan="2">Voltage Thresholds Low</td><td colspan="2">Voltage Thresholds High</td></tr>
<tr><td>Min</td><td>Typical</td><td>Typical</td><td>Max</td></tr>
<tr><td>1.2V (V_{IH}, V_{IL}= 0.60 V)</td><td>420 mV</td><td>450 mV</td><td>750 mV</td><td>780 mV</td></tr>
<tr><td>1.5V (V_{IH}, V_{IL}= 0.75 V)</td><td>525 mV</td><td>600 mV</td><td>900 mV</td><td>975 mV</td></tr>
<tr><td>1.8V (V_{IH}, V_{IL}= 0.90 V)</td><td>630 mV</td><td>750 mV</td><td>1.05 V</td><td>1.17 V</td></tr>
<tr><td>2.5V (V_{IH}, V_{IL}= 1.25 V)</td><td>875 mV</td><td>1.10 V</td><td>1.40 V</td><td>1.625 V</td></tr>
<tr><td>3.3V (V_{IH}, V_{IL}= 1.65 V)</td><td>1.155 V</td><td>1.50 V</td><td>1.80 V</td><td>2.145 V</td></tr>
</table>

Specification	Value	Comments
Input impedance	High-impedance (50 kΩ)	Nominal.
Input protection	-1 V to 5 V	Internal diode clamps may begin conduction outside the -0.5 V to 3.5 V range.

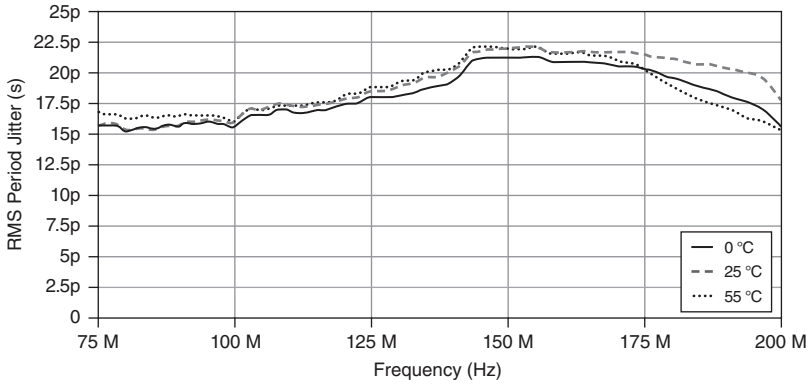
Timing Specifications

Sample Clock

Specification	Value	Comments
Sample clock sources	1. On Board Clock (internal 800 MHz VCO with 32-bit DDS) 2. CLK IN (SMA jack connector) 3. STROBE (Digital Data & Control (DDC) connector; acquisition only)	—
On Board Clock frequency range	**NI 6544, NI 6547**: 100 Hz to 100 MHz **NI 6545, NI 6548**: 100 Hz to 200 MHz	—
On Board Clock frequency resolution	0.2 Hz maximum **Note**: Varies with Sample clock frequency.	NI-HSDIO may be queried for the programmed frequency value.
On Board Clock frequency accuracy	±150 ppm + 5 ppm per year	Accuracy may be increased by using a higher performance external Reference clock.

Specification	Value		Comments
CLK IN frequency range	**NI 6544, NI 6547**: 20 kHz to 100 MHz **NI 6545, NI 6548**: 20 kHz to 200 MHz		Refer to the *CLK IN (SMA Jack Connector)* section for restrictions based on waveform type.
STROBE frequency range	**NI 6544, NI 6547**: 100 Hz to 100 MHz **NI 6545, NI 6548**: 100 Hz to 200 MHz		Refer to the *STROBE (DDC Connector)* section.
Sample clock relative delay adjustment range	0.0 to 1.0 Sample clock period (acquisition sessions) 0.0 ns to 5.0 ns (generation sessions)		You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.
Sample clock relative delay adjustment resolution	0.5 ps		
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMA jack connector)		Internal Sample clocks with sources other than STROBE can be exported.
Exported Sample clock delay range	0.0 to 1.0 Sample clock periods		Resolution is nonlinearly dependent on clock frequency and may be queried for by using NI-HSDIO.
Exported Sample clock delay resolution (δ_C)	117 ps to 143 ps, nominal		
Exported Sample Clock delay frequency	**On Board Clock**	**External Clock**	
	All supported frequencies	Frequencies ≥ 20 MHz	
Exported Sample clock jitter	**Period Jitter**	**Cycle-to-Cycle Jitter**	Characteristic; using On Board Clock.
	24 ps_{rms}	43 ps_{rms}	

Figure 1. Characteristic Period Jitter (RMS) vs. Frequency



Specification	Value			Comments
Exported Sample clock duty cycle		DDC Clock Out		NI 6545/6548 at maximum clock rate (200 MHz). Not including the effects of system crosstalk.
	Logic Family	Min	Max	
	1.2V	37%	50%	
	1.5V	41%	53%	
	1.8V	42%	55%	
	2.5V	45%	57%	
	3.3V	48%	58%	

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

Specification	Value	Comments
Data channel-to-channel skew	±300 ps	Maximum skew across all data channels, PFI channels, and voltage levels when using the same data position or data delay bank.

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td rowspan="11">Maximum data rate per channel</td><td>NI 6544</td><td colspan="3">SDR: 100 Mbps
Supported for all logic families.</td><td rowspan="11">Includes maximum data channel-to-channel skew and typical crosstalk.
NI 6547/6548 devices generate two samples per clock cycle in DDR mode.</td></tr>
<tr><td>NI 6545</td><td colspan="3">SDR: 200 Mbps
Supported for all logic families.</td></tr>
<tr><td>NI 6547</td><td colspan="3">SDR: 100 Mbps
DDR: 200 Mbps
Supported for all logic families and selectable voltage levels.</td></tr>
<tr><td rowspan="9">NI 6548</td><td>Logic Family</td><td>SDR</td><td>DDR</td></tr>
<tr><td>3.3V</td><td rowspan="5">200 Mbps</td><td>400 Mbps</td></tr>
<tr><td>2.5V</td><td>400 Mbps</td></tr>
<tr><td>1.8V</td><td>375 Mbps</td></tr>
<tr><td>1.5V</td><td>350 Mbps</td></tr>
<tr><td>1.2V</td><td>300 Mbps</td></tr>
<tr><td>Voltage Levels</td><td>SDR</td><td>DDR</td></tr>
<tr><td>2.5 V to 3.3 V</td><td rowspan="4">200 Mbps</td><td>400 Mbps</td></tr>
<tr><td>1.8 V to 2.4 V</td><td>375 Mbps</td></tr>
<tr><td>1.5 V to 1.7 V</td><td>350 Mbps</td></tr>
<tr><td>1.2 V to 1.4 V</td><td>300 Mbps</td></tr>
</table>

Figure 2 shows an eye diagram of a 400 Mbps pseudorandom bit sequence (PRBS) waveform in DDR mode at 3.3 V. This waveform was captured on DIO 0 at room temperature into high impedance.

Figure 2. Characteristic Eye Diagram (high impedance)

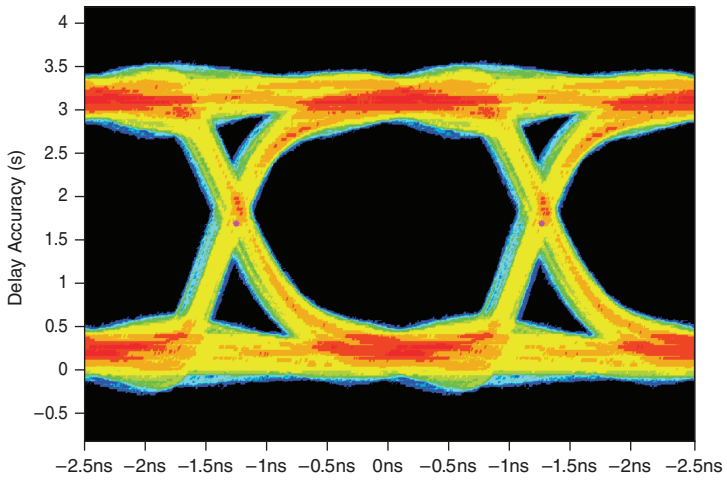
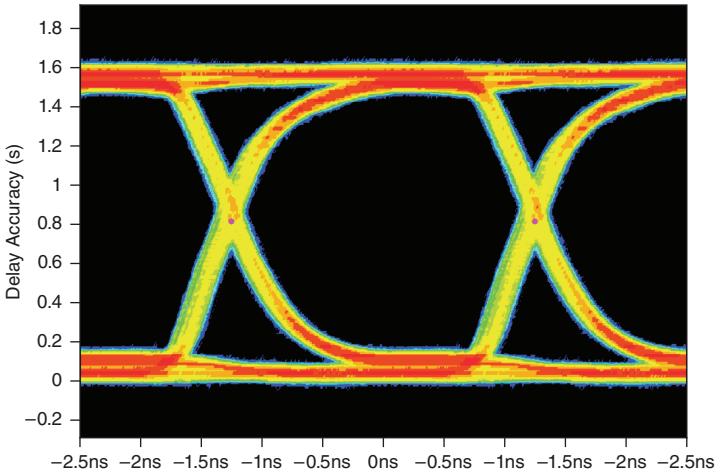


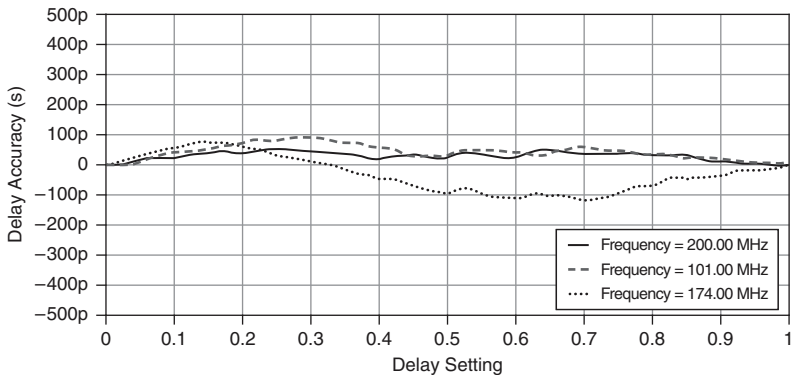
Figure 3 shows an eye diagram of a 400 Mbps PRBS waveform in DDR mode at 3.3 V. This waveform was captured on DIO 0 at room temperature into 50 Ω termination.

Figure 3. Characteristic Eye Diagram (50 Ω Termination)



Specification	Value		Comments
Data position modes	Sample clock rising edge, Sample clock falling edge, or Delay from Sample clock rising edge		—
Data delay banks	**NI 6544/6545**: 1 bank for all channels and PFI lines **NI 6547/6548**: 3 banks Bank 0: DIO<0..3>, DIO<16..19>, DIO<28..31>, PFI <0..3> Bank 1: DIO<4..7>, DIO<20..23> Bank 2: DIO<8..15>, DIO<24..27>		Multibank data delay is supported only in NI-HSDIO 1.7 and later.
Generation data delay range (δ_G)	0.0 to 1.0 Sample clock periods		Resolution is nonlinearly dependent on clock frequency and may be queried for using NI-HSDIO.
Generation data delay resolution (δ_G)	117 ps to 143 ps, nominal		
Generation data delay frequency	**On Board Clock**	**External Clock**	
	All supported frequencies	Frequencies ≥ 20 MHz	

Figure 4. Characteristic Data Delay Accuracy



Specification	Value	Comments
Exported Sample clock offset (t_{CO})	0.0 ns or 1.65 ns (default)	Nominal; Software-selectable for DDC_CLK_OUT.
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	8.1 ns	Characteristic; Exported Sample clock offset = 0 ns

Generation Provided Setup and Hold Times

Exported Sample Clock Offset (t_{PCO})	Minimum Provided Setup Time (t_{PSU})	Minimum Provided Hold Time (t_{PH})
1.65 ns	tp - 2.15 ns	1.15 ns
0.0 ns	tp - 500 ps	-500 ps

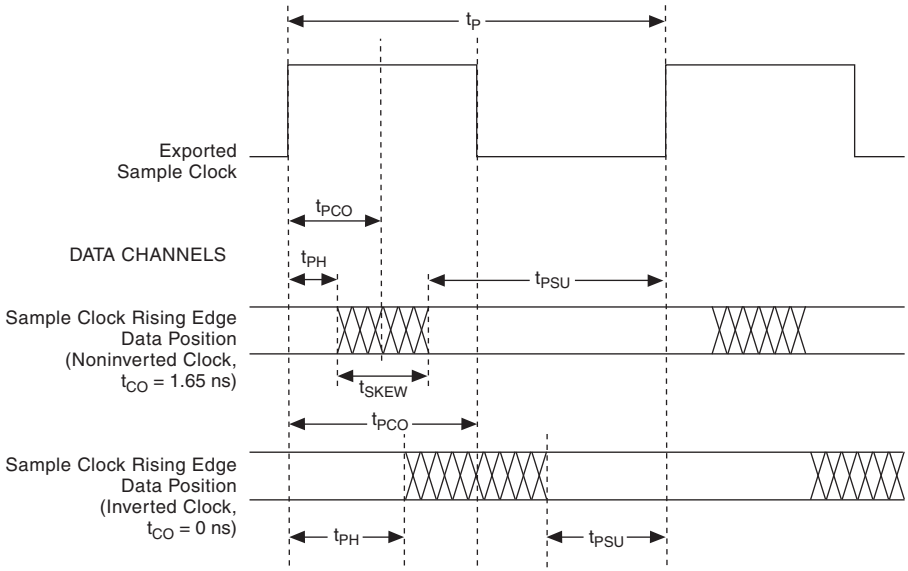
Compare the setup and hold times from the datasheet of your device under test (DUT) to the values in the table above. The provided setup and hold times must be greater than the setup and hold times required for the DUT. If you require more setup time, configure your exported Sample clock mode to Inverted and/or delay your clock or data relative to the Sample clock.

Refer to Figure 5 for a diagram illustrating the relationship between the exported Sample clock mode and the provided setup and hold times.

Notes: This table assumes the data position is set to Sample clock rising edge and the noninverted Sample clock is exported to the DDC connector.

This table includes worst-case effects of channel-to-channel skew and intersymbol interference.

Figure 5. Generation Provided Setup and Hold Times Timing Diagram



$t_P = \frac{1}{f}$ = Sample Clock Period

t_{PH} = Minimum Provided Hold Time

t_{PSU} = Minimum Provided Set-Up Time

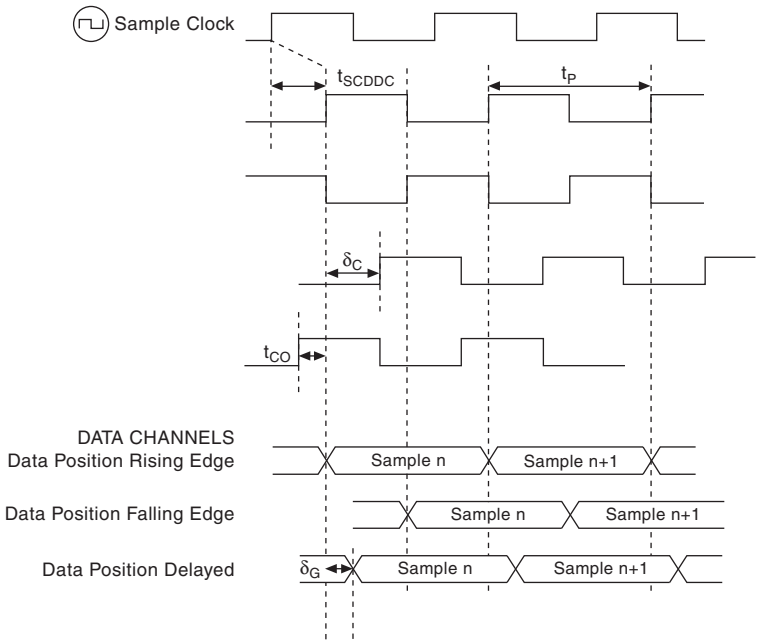
t_{PCO} =Time from Rising Clock Edge to Data Transition (Provided Clock to Out Time)

t_{CO} = Exported Sample Clock Offset

t_{SKEW} = Maximum Channel-to-Channel Skew and Clock Uncertainty

Note Provided setup and hold times account for maximum channel-to-channel skew and jitter.

Figure 6. Generation Timing Diagram



t_{SCDDC} : Time Delay from Sample Clock (Internal) to DDC Connector

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (Fraction of t_P)

$0 \le \delta_G \le 1$: Pattern Generation Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset; 1.65 ns, Software-Selectable

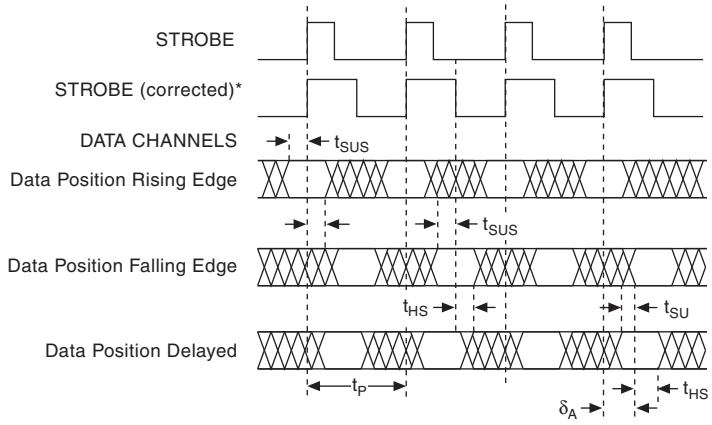
Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

<table>
<tr><th>Specification</th><th colspan="5">Value</th><th>Comments</th></tr>
<tr><td>Channel-to-channel skew</td><td colspan="5">±350 ps</td><td>Maximum skew across all data channels, PFI channels, and voltage levels when using the same data position or data delay bank.</td></tr>
<tr><td rowspan="8">Maximum data rate per channel</td><td>NI 6544</td><td colspan="3">SDR: 100 Mbps
Supported for all logic families.</td><td rowspan="8">Includes maximum data channel-to-channel skew and typical crosstalk.
NI 6547/6548 devices acquires two samples per clock cycle in DDR mode.</td></tr>
<tr><td>NI 6545</td><td colspan="3">SDR: 200 Mbps
Supported for all logic families.</td></tr>
<tr><td>NI 6547</td><td colspan="3">SDR: 100 Mbps
DDR: 200 Mbps
Supported for all logic families and selectable voltage levels.</td></tr>
<tr><td rowspan="6">NI 6548</td><td>Logic Family</td><td>SDR</td><td>DDR</td></tr>
<tr><td>3.3V</td><td rowspan="5">200 Mbps</td><td>300 Mbps</td></tr>
<tr><td>2.5V</td><td>300 Mbps</td></tr>
<tr><td>1.8V</td><td>250 Mbps</td></tr>
<tr><td>1.5V</td><td>225 Mbps</td></tr>
<tr><td>1.2V</td><td>200 Mbps</td></tr>
<tr><td></td><td>Voltage Threshold</td><td>SDR</td><td>DDR</td></tr>
<tr><td></td><td>1.25 V to 1.65 V</td><td rowspan="4">200 Mbps</td><td>300 Mbps</td></tr>
<tr><td></td><td>0.90 V to 1.20 V</td><td>250 Mbps</td></tr>
<tr><td></td><td>0.75 V to 0.85 V</td><td>225 Mbps</td></tr>
<tr><td></td><td>0.60 V to 0.70 V</td><td>200 Mbps</td></tr>
</table>

<table>
<tr><th>Specification</th><th colspan="5">Value</th><th>Comments</th></tr>
<tr><td rowspan="6">Setup and Hold Times to STROBE</td><td rowspan="2">Voltage Threshold</td><td colspan="2">Hold Time (ths)</td><td colspan="2">Setup Times (tsus)</td><td rowspan="6">Characteristic includes maximum data channel-to-channel skew and uncertainty, but does not include system crosstalk. Performance may vary with system crosstalk performance.</td></tr>
<tr><td><20 MHz</td><td>≥20 MHz</td><td><20 MHz</td><td>≥20 MHz</td></tr>
<tr><td>1.25 V to 1.65 V</td><td>2.4 ns</td><td>900 ps</td><td>2.8 ns</td><td>1.15 ns</td></tr>
<tr><td>0.90 V to 1.20 V</td><td></td><td>1.00 ns</td><td></td><td>1.20 ns</td></tr>
<tr><td>0.75 V to 0.85 V</td><td></td><td>1.10 ns</td><td></td><td>1.40 ns</td></tr>
<tr><td>0.60 V to 0.70 V</td><td></td><td>1.25 ns</td><td></td><td>1.75 ns</td></tr>
<tr><td>Data position modes</td><td colspan="5">Sample clock rising edge, Sample clock falling edge, or Delay from Sample clock rising edge.</td><td>—</td></tr>
<tr><td>Data delay banks</td><td colspan="5">NI 6544/6545: 1 bank for all channels and PFI lines
NI 6547/6548: 3 banks
Bank 0: DIO<0..3>, DIO<16..19>, DIO<28..31>, PFI <0..3>
Bank 1: DIO<4..7>, DIO<20..23>
Bank 2: DIO<8..15>, DIO<24..27></td><td>Multibank data delay is supported only in NI-HSDIO 1.7 and later.</td></tr>
<tr><td>Acquisition data delay range</td><td colspan="5">0.0 to 1.0 Sample clock periods</td><td rowspan="3">Resolution is nonlinearly dependent on clock frequency and may be queried for by using NI-HSDIO.</td></tr>
<tr><td>Acquisition data delay resolution</td><td colspan="5">117 ps to 143 ps, nominal</td></tr>
<tr><td rowspan="2">Acquisition data delay frequency</td><td colspan="2">On Board Clock</td><td colspan="3">External Clock and STROBE</td></tr>
<tr><td colspan="2">All supported frequencies</td><td colspan="3">Frequencies ≥ 20 MHz</td></tr>
</table>

Specification	Value	Comments
Setup time to sample clock (t_{susc})	900 ps	Nominal; does not include channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}.
Hold time to sample clock (t_{HSC})	425 ps	
Time delay from DDC connector to internal sample clock	6.8 ns	Nominal.

Figure 7. Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{SUS} = Set-Up Time to STROBE

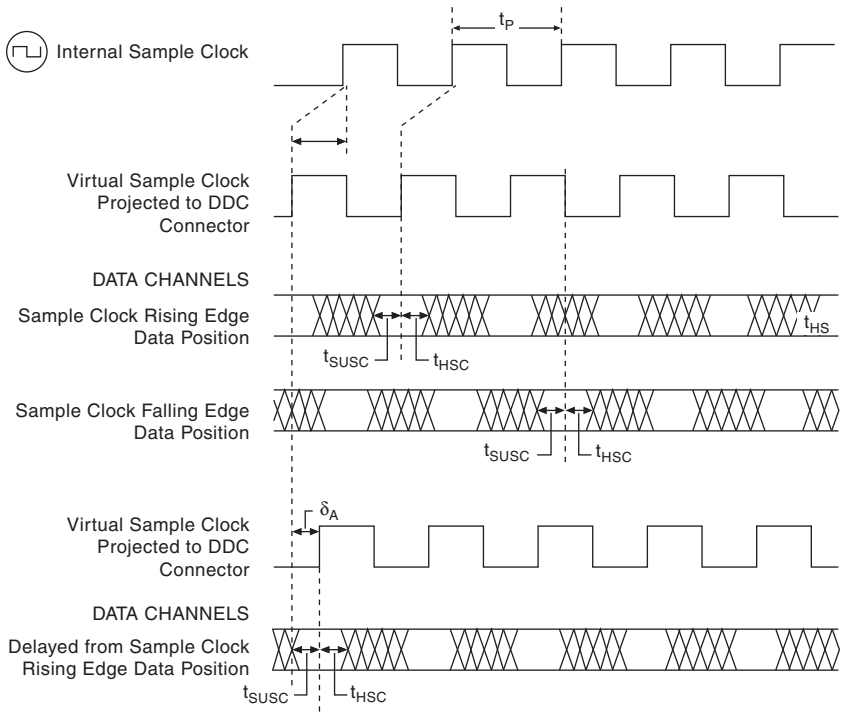
t_{HS} = Hold Time from STROBE

$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

*Note: When using an external Sample clock greater than 20 MHz, the duty cycle is corrected to 50%.

Figure 8. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \leq \delta_A \leq 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

CLK IN (SMA Jack Connector)

Specification	Value	Comments
Direction	Input to device	—
Destinations	1. Reference clock—for the phase lock loop (PLL) 2. Sample clock	—
Input coupling	AC	—
Input protection	±10 VDC	Nominal.

Specification	Value					Comments
Input impedance	50 Ω (default) or 1 kΩ					Software-selectable; Nominal.
Minimum detectable pulse width	2 ns					Nominal.
Clock requirements	Clock must be continuous and free-running.					—
Voltage ranges	**Square Waves**					—
	$0.65\ V_{pp}$ to $5.0\ V_{pp}$					
	Sine Waves					—
	Voltage range	$0.65\ V_{pp}$ to $5.0\ V_{pp}$	$1.0\ V_{pp}$ to $5.0\ V_{pp}$	$1.3\ V_{pp}$ to $5.0\ V_{pp}$	$2.6\ V_{pp}$ to $5.0\ V_{pp}$	
	Frequency range	20 MHz to 100 MHz	13 MHz to 100 MHz	10 MHz to 100 MHz	5 MHz to 100 MHz	Supported by NI 6544 and 6547 only.
		20 MHz to 200 MHz	13 MHz to 200 MHz	10 MHz to 200 MHz	5 MHz to 200 MHz	Supported by NI 6545 and 6548 only.

Specification	Value	Comments
As Sample Clock		
Frequency range	**NI 6544 and NI 6547**: 20 kHz to 100 MHz **NI 6545 and NI 6548**: 20 kHz to 200 MHz	Nominal 3 dB cutoff point at 100 MHz when using 1 kΩ input impedance.
Duty cycle range	f < 20 MHz: 25% to 75% f ≥ 20 MHz: 40% to 60%	—
As Reference Clock		
Reference clock frequency range	5 MHz to 100 MHz (Integer multiples of 1 MHz)	—
Reference clock frequency accuracy	± 0.1%	Required accuracy of the external Reference clock source.
Reference clock duty cycle	25% to 75%	—

STROBE (DDC Connector)

Specification	Value	Comments
Direction	Input to device	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	**NI 6544, NI 6547**: 100 Hz to 100 MHz **NI 6545, NI 6548**: 100 Hz to 200 MHz	—
STROBE duty cycle range	40% to 60% for clock frequencies ≥ 20 MHz 25% to 75% for clock frequencies < 20 MHz **Note**: STROBE duty cycle is corrected to 50% at frequencies ≥ 20 MHz.	Duty cycle at the programmed threshold.

Specification	Value	Comments
Minimum detectable pulse width	2 ns	Nominal; required at acquisition voltage thresholds.
Voltage thresholds	Refer to the *Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—
Clock requirements	Clock must be continuous and free-running.	—
Input impedance	50 kΩ	Nominal.

CLK OUT (SMA Jack Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω	Nominal.
Electrical characteristics	Refer to the *Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)* specifications in the *Channel Specifications* section.	—
Logic type	Matched with generation and acquisition sessions.	—

DDC CLK OUT (DDC Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	Sample clock (generation only)	STROBE and acquisition Sample clock cannot be routed to DDC CLK OUT.
Electrical characteristics	Refer to the *Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)* specifications in the *Channel Specifications* section.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK100 (PXI Express backplane) 2. CLK IN (SMA jack connector) 3. None (internal oscillator locked to an internal reference)	Provides the reference frequency for the PLL.
Lock time	150 ms	Maximum, not including software latency.
Reference clock frequencies	5 MHz to 100 MHz (integer multiple of 1 MHz)	0.1% required accuracy.
Reference clock duty cycle range	25% to 75%	—
Reference clock destinations	CLK OUT (SMA jack connector)	—

Waveform Specifications

Memory and Scripting

Specification	Value			Comments
Memory architecture	The NI 6544/6545/6547/6548 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.			Refer to the *Onboard Memory* section in the *NI Digital Waveform Generator/ Analyzer Help* for more information.
Onboard memory size (generation and acquisition)	1 Mbit/channel	8 Mbit/channel	64 Mbit/channel	Maximum limit for generation sessions assumes no scripting instructions.
Generation modes	**Single-waveform mode** Generate a single waveform once, *n* times, or continuously.			—
	Scripted mode Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.			

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="5">Generation minimum waveform size in samples (S)</td><td rowspan="2">Configuration</td><td colspan="2">Sample Rate</td><td rowspan="5">Sample rate dependent. Increasing sample rate increases minimum waveform size requirement. For information on these configurations, refer to Common Scripting Use Cases in the NI Digital Waveform Generator/ Analyzer Help.</td></tr>
<tr><td>200 MHz (NI 6545/6548 Only)</td><td>100 MHz</td></tr>
<tr><td>Single waveform</td><td>1 S</td><td>1 S</td></tr>
<tr><td>Continuous waveform</td><td>128 S</td><td>64 S</td></tr>
<tr><td>Stepped sequence</td><td>128 S</td><td>64 S</td></tr>
<tr><td>Burst sequence</td><td>1056 S</td><td>512 S</td></tr>
<tr><td>Generation finite repeat count</td><td colspan="3">1 to 16,777,216</td><td>—</td></tr>
<tr><td rowspan="2">Generation waveform quantum</td><td>Data Width = 4</td><td colspan="2">Data Width = 2</td><td rowspan="2">DDR mode sets data width to 2.</td></tr>
<tr><td>1 sample</td><td colspan="2">2 samples</td></tr>
</table>

Specification	Value		Comments
Generation waveform block size (in physical memory)	**Data width = 4**	**Data width = 2**	—
	32 samples	64 samples	
Acquisition minimum record size	1 S		Regardless of waveform size, NI-HSDIO allocates at least 640 bytes for a record.
Acquisition record quantum	1 S		—
Acquisition maximum number of records	2,147,483,647		Session should fetch fast enough so that unfetched data is not overwritten.
Acquisition number of pre-Reference trigger samples	0 up to full record		—
Acquisition number of post-Reference trigger samples	0 up to full record		—

Triggers (Inputs to the NI 6544/6545/6547/6548)

<table>
<tr><th>Specification</th><th>Value</th><th>Comments</th></tr>
<tr><td>Trigger types</td><td>1. Start trigger
2. Pause trigger
3. Script trigger <0..3> (generation sessions only)
4. Reference trigger (acquisition sessions only)
5. Advance trigger (acquisition sessions only)
6. Stop Trigger (generation sessions only)</td><td>—</td></tr>
<tr><td>Sources</td><td>1. PFI 0 (SMA jack connector)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG<0..7> (PXI Express backplane)
4. Pattern match (acquisition sessions only)
5. Software (user function call)
6. Disabled (do not wait for a trigger)</td><td>—</td></tr>
<tr><td>Trigger detection</td><td>1. Start trigger (edge detection: rising or falling)
2. Pause trigger (level detection: high or low)
3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low)
4. Reference trigger (edge detection: rising or falling)
5. Advance trigger (edge detection: rising or falling)
6. Stop Trigger (edge detection: rising or falling)</td><td>—</td></tr>
<tr><td>Minimum required trigger pulse width</td><td>15 ns</td><td>—</td></tr>
<tr><td>Destinations</td><td>1. PFI 0 (SMA jack connectors)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG<0..6> (PXI Express backplane)</td><td>Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported.</td></tr>
<tr><td>Trigger rearm time</td><td>
<table>
<tr><th>Start to Reference Trigger</th><th>Start to Advance Trigger</th><th>Advance to Advance Trigger</th><th>Reference to Reference Trigger</th></tr>
<tr><td>150 s</td><td>220 s</td><td>220 s</td><td>220 s</td></tr>
</table>
</td><td>Maximum number of samples.</td></tr>
</table>

Specification	Value		Comments
Delay from Pause trigger to Pause state and Stop trigger to Done state	**Generation Sessions**	**Acquisition Sessions**	Maximum; Use the Data Active event during generation to determine on a sample by sample basis when the device enters the Pause or Done states.
	50 Sample clock periods + 300 ns	Synchronous with the data	
Delay from trigger to digital data output	3 Sample clock periods + 600 ns		Maximum; Start trigger and Script triggers.

Events (Generated from the NI 6544/6545/6547/6548)

Specification	Value	Comments
Event type	1. Marker <0..2> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event 4. Ready for Advance event (acquisition sessions only) 5. End of Record event (acquisition sessions only)	—
Destinations	1. PFI 0 (SMA jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..6> (PXI Express backplane)	Each event can be routed to any destination, except the Data Active event. The Data Active event can only be routed to the PFI channels.
Marker time resolution (placement)	Markers can be placed at any sample when using SDR mode. Markers must be placed at an integer multiple of two samples when using DDR mode.	—

Miscellaneous

Specification	Value	Comments
Warm-up time	15 minutes	—
On Board Clock characteristics (valid when PLL reference source is set to None)		
Frequency accuracy	±150 ppm	Typical, including temperature effects.
Aging	±5 ppm first year	Nominal.

Power

Specification	Value		Comments
	Characteristic	Maximum	
+3.3 VDC	1.75 A	1.77 A	Characteristic results are commensurate with an average user application using all data channels into high impedance load. Maximum results include worst case data pattern.
+12 VDC	2.2 A	2.3 A	
Total power	32.2 W	33.5 W	

Physical

Specification	Value	Comments
Dimensions	21.6 × 2.0 × 13.0 cm Single 3U CompactPCI Express slot; PXI Express compatible	—
Weight	18.3 oz (519 g)	—

I/O Panel Connectors

Label	Function(s)	Connector Type
CLK IN	External Sample clock, external Reference clock.	SMA jack
PFI 0	Events, triggers.	SMA jack
CLK OUT	External Sample clock, exported Reference clock.	SMA jack
Digital Data & Control (DDC)	Digital data channels, exported Sample clock, STROBE, events, triggers.	68pin VHDCI

Software

Specification	Value	Comments
Driver software	NI-HSDIO driver software 1.6 or later. NI-HSDIO allows you to configure and control the NI 6544/6545/6547/6548. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI application programming interface (API) guidelines. Hardware compare, per cycle tristate, and multibank data delay are supported only in NI-HSDIO 1.7 or later.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments (ADEs): • National Instruments LabVIEW • National Instruments LabWindows™/CVI™ • Microsoft Visual C/C++	Refer to the *NI-HSDIO Instrument Driver Readme* for more information about supported ADE versions.
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 6544/6545/6547/6548. MAX is included on the NI-HSDIO driver CD.	—

Environment

Note To ensure that the NI 6544/6545/6547/6548 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the NI 6544/6545/6547/6548. The NI 6544/6545/6547/6548 is intended for indoor use only.

Specification	Value	Comments
Operating temperature	0 to 55 ºC in all NI PXI Express and hybrid NI PXI Express chassis.	—
Storage temperature	-20 to 70 ºC	—
Operating relative humidity	10% to 90% relative humidity, noncondensing (Meets IEC 60068-2-56.)	—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC 60068-2-56.)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Storage shock	50 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC 60068-2-64.)	—
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.)	—
Altitude	0 m to 2,000 m above sea level (at 25º C ambient temperature)	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Specification	Value	Comments
Safety	The NI 6544/6545/6547/6548 meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1, CSA 61010-1	For UL and other safety certifications, refer to the product label or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.
Electromagnetic Compatibility	The NI 6544/6545/6547/6548 meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use: EN 61326-1 (IEC 61326-1): Class A emissions, Basic immunity EN 55011 (CISPR 11): Group 1, Class A emissions AS/NZS CISPR 11: Group 1, Class A emissions FCC 47 CFR Part 15B: Class A emissions ICES-001: Class A emissions For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section below.	To meet EMC compliance the following cautions apply.
Note: SHC68-C68-D4 or SHC68-C68-D2 shielded cable and provided cable ferrites must be used when operating the NI 6544/6545/6547/6548. **Note**: EMI filler panels (NI P/N 778700-01) must be installed in all empty slots of the NI 6544/6545/6547/6548.		
CE Compliance CE	This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows: 2006/95/EC; Low-Voltage Directive (safety) 2004/108/EC; Electromagnetic Compatibility Directive (EMC)	—
Online Product Certification	Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.	—

Environmental Management	NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers. For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.	—
Waste Electrical and Electronic Equipment (WEEE)	**EU Customers**: At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.	

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。 (For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

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