Delta Tau PMAC ACC-11C

96-Point I/O Board

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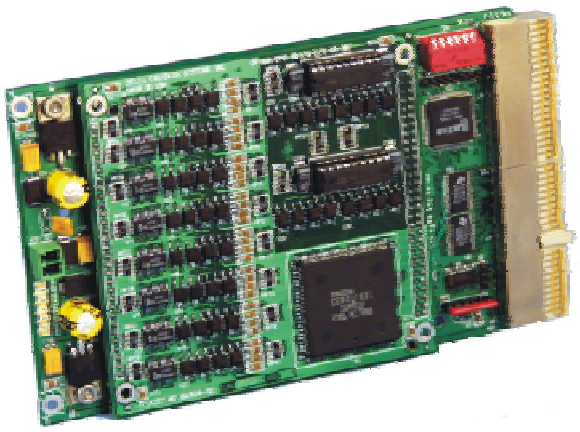
USER MANUAL

Accessory 11C



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INTRODUCTION

The PMAC Accessory 11C is a general-purpose input/output board to the COMPACT UBUS - Turbo system. Both the inputs and outputs of this board are to be configuring as sinking signals ONLY. ACC-11C provides 64 lines of self protected optically isolated inputs and 32 lines of optically isolated outputs when ordered with Option 1. If the board is ordered without Option 1 the I/O board will provide 32 lines of self protected optically isolated inputs and 16 lines of optically isolated outputs. The actual I/O Reads are carried out using M-variables, which will be described later.

The inputs to the ACC-11C board have an activation range from 12V to 24V. Due to the self-protecting circuitry, the inputs can be configured only as sinking inputs. Although self-protecting, there are still limits to the power supplied to the inputs of the ACC-11C. The limiting voltages are V_f = 57 volts input to the I/O and the V_r = 33 volts input to the I/O. These limitations are due to the protective circuitry, including the MMBZ33VALT1 Zener diodes.

The output drivers are organized in a set of 12 4-bit groups. The default configuration of this accessory board uses Seimens BTS 711 L1 four-channel FET chip. With this configuration, the current drawn from each output line should be limited to 225mA at voltage levels between 12 and 24 volts. The specifications for this output chip can be found at the Siemens website.

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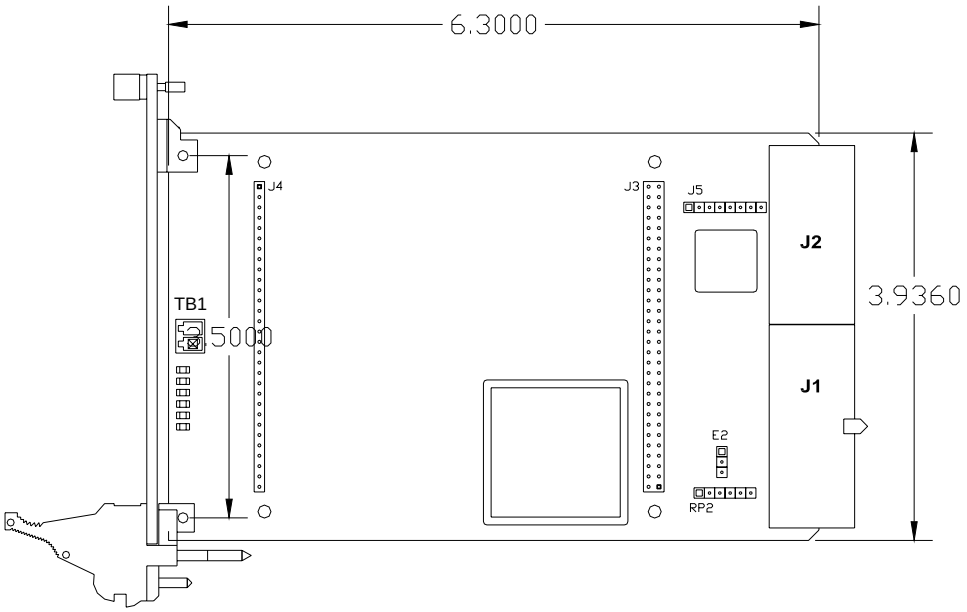
HARDWARE SETUP

The ACC-11C uses expansion port memory locations defined by the type of PMAC (COMPACT UBUS Turbo) it is directly communicating to.

Compact UBUS Turbo PMAC Memory Locations
$078C00, $079C00 $07AC00, $07BC00
$078D00, $079D00 $07AD00, $07BD00
$078E00, $079E00 $07AE00, $07EC00
$078F00, $079F00 $07AF00, $07BF00

The ACC-11C has a set of dipswitches telling it where to process its data. Proper setting of the dipswitches ensures that the COMPACT UBUS IO boards used in the application do not interfere with each other.

Layout Diagram



Address Select Dip Switch S1

The switch one (S1) settings will allow the user to select the starting address location for the first IO gate on the ACC-11C. The following two tables show the dip switch settings for the Turbo PMAC Compact UBUS .

Turbo PMAC Compact UBUS Switch Settings

Chip Select	Compact UBUS Turbo PMAC Address	Dip Switch SW1 Position					
		6	5	4	3	2	1
CS10	Y:$78C00-07	ON	ON	ON	ON	ON	ON
	Y:$79C00-07	ON	ON	ON	OFF	ON	ON
	Y:$7AC00-07	ON	ON	OFF	ON	ON	ON
	Y:$7BC00-07	ON	ON	OFF	OFF	ON	ON
CS12	Y:$78D00-07	ON	ON	ON	ON	ON	OFF
	Y:$79D00-07	ON	ON	ON	OFF	ON	OFF
	Y:$7AD00-07	ON	ON	OFF	ON	ON	OFF
	Y:$7BD00-07	ON	ON	OFF	OFF	ON	OFF
CS14	Y:$78E00-07	ON	ON	ON	ON	OFF	ON
	Y:$79E00-07	ON	ON	ON	OFF	OFF	ON
	Y:$7AE00-07	ON	ON	OFF	ON	OFF	ON
	Y:$7BE00-07	ON	ON	OFF	OFF	OFF	ON
CS16	Y:$78F00-07	ON	ON	ON	ON	OFF	OFF
	Y:$79F00-07	ON	ON	ON	OFF	OFF	OFF
	Y:$7AF00-07	ON	ON	OFF	ON	OFF	OFF
	Y:$7BF00-07	ON	ON	OFF	OFF	OFF	OFF

The default setting is ***ALL CLOSED*** position.

Jumpers

Please refer to the layout diagram of ACC-11C for the location of the jumpers on the board.

E-Point Jumpers

Jumper	Config	Description	Settings	Default
E2	1-2	Sample Clock Select	1-2 servo clock 2-3 phase clock	1-2

USING ACC-11C WITH COMPACT UBUS TURBO

For the UMAC-Turbo, the ACC-11C can be used for either general purpose I/O or as latched inputs. The ACC-11C 48-bits of IO are placed into six 8-bit registers. For example if the base address set by the SW1 setting were set to Y:$78C00, then the IO for the ACC-11C would be found at the following locations:

```
Y:$78000,0,8        ;bits 0-7
Y:$78001,0,8        ;bits 8-15
Y:$78002,0,8        ;bits 16-23
Y:$78003,0,8        ;bits 24-31
Y:$78004,0,8        ;bits 32-39
Y:$78005,0,8        ;bits 40-47
```

Compact UBUS - Turbo Memory Mapping for ACC-11C

The Delta Tau I/O Gate used on the ACC-11C is an 8-bit processor, and therefore the memory mapping to the I/O bits is processed as 8-bit words at the Turbo COMPACT UBUS. Using this simple scheme, you could process up to 768 (48×16) bits of data for general purpose I/O.

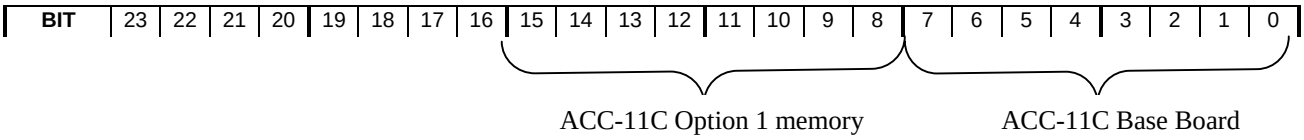
	CS10 **SW1-1 ON** **SW1-2 ON**	**CS12** **SW1-1 OFF** **SW1-2 ON**	**CS14** **SW1-1 ON** **SW1-2 OFF**	**CS16** **SW1-1 OFF** **SW1-2 OFF**	**Description**
SW1-3 ON SW1-4 ON	Y:$078C00,0,8	Y:$078D00,0,8	Y:$078E00,0,8	Y:$078F00,0,8	I/O bits 0-7
	Y:$078C01,0,8	Y:$078D01,0,8	Y:$078E01,0,8	Y:$078F01,0,8	I/O bits 8-15
	Y:$078C02,0,8	Y:$078D02,0,8	Y:$078E02,0,8	Y:$078F02,0,8	I/O bits 16-23
	Y:$078C03,0,8	Y:$078D03,0,8	Y:$078E03,0,8	Y:$078F03,0,8	I/O bits 24-31
	Y:$078C04,0,8	Y:$078D04,0,8	Y:$078E04,0,8	Y:$078F04,0,8	I/O bits 32-39
	Y:$078C05,0,8	Y:$078D05,0,8	Y:$078E05,0,8	Y:$078F05,0,8	I/O bits 40-47
	Y:$078C07,0,8	Y:$078D07,0,8	Y:$078E07,0,8	Y:$078F07,0,8	Control Word
SW1-3 OFF SW1-4 ON	Y:$079C00,0,8	Y:$079D00,0,8	Y:$079E00,0,8	Y:$079F00,0,8	I/O bits 0-7
	Y:$079C01,0,8	Y:$079D01,0,8	Y:$079E01,0,8	Y:$079F01,0,8	I/O bits 8-15
	Y:$079C02,0,8	Y:$079D02,0,8	Y:$079E02,0,8	Y:$079F02,0,8	I/O bits 16-23
	Y:$079C03,0,8	Y:$079D03,0,8	Y:$079E03,0,8	Y:$079F03,0,8	I/O bits 24-31
	Y:$079C04,0,8	Y:$079D04,0,8	Y:$079E04,0,8	Y:$079F04,0,8	I/O bits 32-39
	Y:$079C05,0,8	Y:$079D05,0,8	Y:$079E05,0,8	Y:$079F05,0,8	I/O bits 40-47
	Y:$079C07,0,8	Y:$079D07,0,8	Y:$079E07,0,8	Y:$079F07,0,8	Control Word
SW1-3 ON SW1-4 OFF	Y:$07AC00,0,8	Y:$07AD00,0,8	Y:$07AE00,0,8	Y:$07AF00,0,8	I/O bits 0-7
	Y:$07AC01,0,8	Y:$07AD01,0,8	Y:$07AE01,0,8	Y:$07AF01,0,8	I/O bits 8-15
	Y:$07AC02,0,8	Y:$07AD02,0,8	Y:$07AE02,0,8	Y:$07AF02,0,8	I/O bits 16-23
	Y:$07AC03,0,8	Y:$07AD03,0,8	Y:$07AE03,0,8	Y:$07AF03,0,8	I/O bits 24-31
	Y:$07AC04,0,8	Y:$07AD04,0,8	Y:$07AE04,0,8	Y:$07AF04,0,8	I/O bits 32-39
	Y:$07AC05,0,8	Y:$07AD05,0,8	Y:$07AE05,0,8	Y:$07AF05,0,8	I/O bits 40-47
	Y:$07AC07,0,8	Y:$07AD07,0,8	Y:$07AE07,0,8	Y:$07AF07,0,8	Control Word
SW1-3 OFF SW1-4 OFF	Y:$07BC00,0,8	Y:$07BD00,0,8	Y:$07BE00,0,8	Y:$07BF00,0,8	I/O bits 0-7
	Y:$07BC01,0,8	Y:$07BD01,0,8	Y:$07BE01,0,8	Y:$07BF01,0,8	I/O bits 8-15
	Y:$07BC02,0,8	Y:$07BD02,0,8	Y:$07BE02,0,8	Y:$07BF02,0,8	I/O bits 16-23
	Y:$07BC03,0,8	Y:$07BD03,0,8	Y:$07BE03,0,8	Y:$07BF03,0,8	I/O bits 24-31
	Y:$07BC04,0,8	Y:$07BD04,0,8	Y:$07BE04,0,8	Y:$07BF04,0,8	I/O bits 32-39
	Y:$07BC05,0,8	Y:$07BD05,0,8	Y:$07BE05,0,8	Y:$07BF05,0,8	I/O bits 40-47
	Y:$078C07,0,8	Y:$078D07,0,8	Y:$078E07,0,8	Y:$078F07,0,8	Control Word
Note: SW1-5 and SW1-6 must be set to ON					

Using ACC-11C Option 1 Inputs/Outputs

The ACC-11C option 1 card (part number 603604-10x) is a mezzanine card that plugs into the ACC-11C and allows the user to add an additional 32 inputs and 16 outputs to the system.

The ACC-11C option1 inputs and outputs can be read and written to like the IO points on the ACC-11C base Card. The memory addresses of the ACC-11C option 1 IO points are located at the same base address but the data is shifted 8 bits. For example, if the starting address of the main card was at Y:$78C00,0,8, then the starting address of the option 1 memory would be at Y:$78C00,8,8.

Base Address of ACC-11C and Option 1 (Y:$78C00 for example)



Compact UBUS - Turbo Memory Mapping for ACC-11C Option 1

The Delta Tau I/O Gate used on the ACC-11C is an 8-bit processor, and therefore the memory mapping to the I/O bits is processed as 8-bit words at the Turbo Compact UBUS . Using this simple scheme, you could process an additional 768 (48×16) bits of data for general purpose I/O.

	CS10 **SW1-1 ON** **SW1-2 ON**	**CS12** **SW1-1 OFF** **SW1-2 ON**	**CS14** **SW1-1 ON** **SW1-2 OFF**	**CS16** **SW1-1 OFF** **SW1-2 OFF**	**Description**
SW1-3 ON SW1-4 ON	Y:$078C00,8,8	Y:$078D00,8,8	Y:$078E00,8,8	Y:$078F00,8,8	I/O bits 0-7
	Y:$078C01,8,8	Y:$078D01,8,8	Y:$078E01,8,8	Y:$078F01,8,8	I/O bits 8-15
	Y:$078C02,8,8	Y:$078D02,8,8	Y:$078E02,8,8	Y:$078F02,8,8	I/O bits 16-23
	Y:$078C03,8,8	Y:$078D03,8,8	Y:$078E03,8,8	Y:$078F03,8,8	I/O bits 24-31
	Y:$078C04,8,8	Y:$078D04,8,8	Y:$078E04,8,8	Y:$078F04,8,8	I/O bits 32-39
	Y:$078C05,8,8	Y:$078D05,8,8	Y:$078E05,8,8	Y:$078F05,8,8	I/O bits 40-47
	Y:$078C07,8,8	Y:$078D07,8,8	Y:$078E07,8,8	Y:$078F07,8,8	Control Word
SW1-3 OFF SW1-4 ON	Y:$079C00,8,8	Y:$079D00,8,8	Y:$079E00,8,8	Y:$079F00,8,8	I/O bits 0-7
	Y:$079C01,8,8	Y:$079D01,8,8	Y:$079E01,8,8	Y:$079F01,8,8	I/O bits 8-15
	Y:$079C02,8,8	Y:$079D02,8,8	Y:$079E02,8,8	Y:$079F02,8,8	I/O bits 16-23
	Y:$079C03,8,8	Y:$079D03,8,8	Y:$079E03,8,8	Y:$079F03,8,8	I/O bits 24-31
	Y:$079C04,8,8	Y:$079D04,8,8	Y:$079E04,8,8	Y:$079F04,8,8	I/O bits 32-39
	Y:$079C05,8,8	Y:$079D05,8,8	Y:$079E05,8,8	Y:$079F05,8,8	I/O bits 40-47
	Y:$079C07,8,8	Y:$079D07,8,8	Y:$079E07,8,8	Y:$079F07,8,8	Control Word
SW1-3 ON SW1-4 OFF	Y:$07AC00,8,8	Y:$07AD00,8,8	Y:$07AE00,8,8	Y:$07AF00,8,8	I/O bits 0-7
	Y:$07AC01,8,8	Y:$07AD01,8,8	Y:$07AE01,8,8	Y:$07AF01,8,8	I/O bits 8-15
	Y:$07AC02,8,8	Y:$07AD02,8,8	Y:$07AE02,8,8	Y:$07AF02,8,8	I/O bits 16-23
	Y:$07AC03,8,8	Y:$07AD03,8,8	Y:$07AE03,8,8	Y:$07AF03,8,8	I/O bits 24-31
	Y:$07AC04,8,8	Y:$07AD04,8,8	Y:$07AE04,8,8	Y:$07AF04,8,8	I/O bits 32-39
	Y:$07AC05,8,8	Y:$07AD05,8,8	Y:$07AE05,8,8	Y:$07AF05,8,8	I/O bits 40-47
	Y:$07AC07,8,8	Y:$07AD07,8,8	Y:$07AE07,8,8	Y:$07AF07,8,8	Control Word
SW1-3 OFF SW1-4 OFF	Y:$07BC00,8,8	Y:$07BD00,8,8	Y:$07BE00,8,8	Y:$07BF00,8,8	I/O bits 0-7
	Y:$07BC01,8,8	Y:$07BD01,8,8	Y:$07BE01,8,8	Y:$07BF01,8,8	I/O bits 8-15
	Y:$07BC02,8,8	Y:$07BD02,8,8	Y:$07BE02,8,8	Y:$07BF02,8,8	I/O bits 16-23
	Y:$07BC03,8,8	Y:$07BD03,8,8	Y:$07BE03,8,8	Y:$07BF03,8,8	I/O bits 24-31
	Y:$07BC04,8,8	Y:$07BD04,8,8	Y:$07BE04,8,8	Y:$07BF04,8,8	I/O bits 32-39
	Y:$07BC05,8,8	Y:$07BD05,8,8	Y:$07BE05,8,8	Y:$07BF05,8,8	I/O bits 40-47
	Y:$078C07,8,8	Y:$078D07,8,8	Y:$078E07,8,8	Y:$078F07,8,8	Control Word
Note: SW1-5 and SW1-6 must be set to ON					

Control Register

The control register at address {Base + 7} permits the configuration of the IOGATE IC to a variety of applications. The control register consists of 8 write/read-back bits – Bits 0 - 7. The control register consists of two sections; Direction Control and Register Select.

The direction control allows setting input bytes to be read only. One of the advantages of the IOGATE IC is the ability to define the bits as inputs or outputs. This "control" mechanism allows you to ensure the inputs will always be read properly. Our traditional I/O accessories always define the inputs and outputs by hardware.

The ACC-11C is different from Delta Tau's other I/O boards in that the hardware layout of the board designates the direction of the signal. It is still necessary to set up the soft logic to accommodate the hardware. This will be done in a power up PLC that will be described later.

Direction Control Bits

Bits 0 to 5 of the control register control the direction of the I/O for the matching numbered data register. That is, Bit *n* controls the direction of the I/O at {Base + *n*}. A value of 0 in the control bit (the default) permits a write operation to the data register, enabling the output function for each line in the register. Enabling the output function does not prevent the use of any or all of the lines as inputs, as long as the outputs are off (non-conducting). A value of 1 in the control bit prohibits a write operation to the data register, disabling the output, reserving the register for inputs.

Example: A value of 1 in Bit 3 disables the write function into the data register at address {Base + 3}, ensuring that lines IO24 - IO31 can always be used as inputs.

Register Select Control Bits

Bits 6 and 7 of the control register together select which of 4 possible registers can be accessed at each of the addresses {Base + 0} through {Base + 5}. They also select which of 2 possible registers can be selected at {Base + 6}.

The following table explains how these bits select registers:

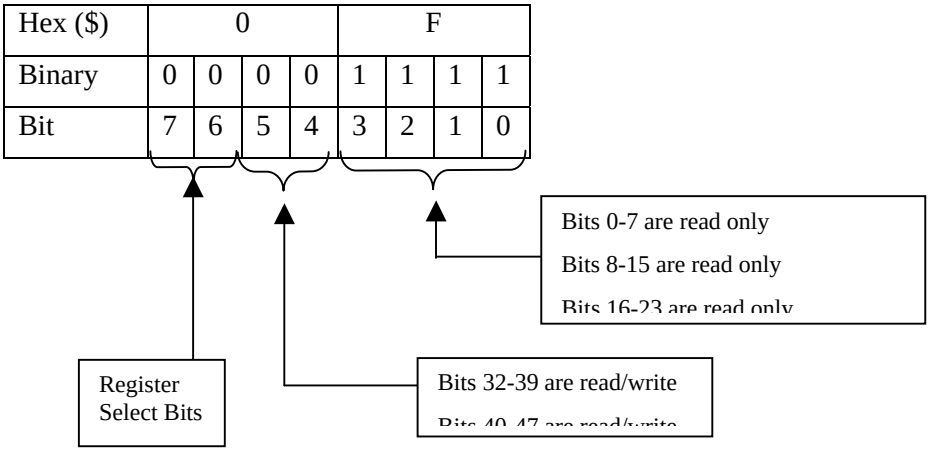
Bit 7	Bit 6	Combined Value	{Base + 0} to {Base + 5} Register Selected	{Base + 6} Register Selected
0	0	0	Data Register	Data Register
0	1	1	Setup Register 1	Setup Register
1	0	2	Setup Register 2	n. a.
1	1	3	Setup Register 3	n. a.

In a typical application, non-zero combined values of Bits 6 and 7 are used only for initial configuration of the IC. These values are used to access the setup registers at the other addresses After the configuration is finished, zeros are written to both Bits 6 and 7, so the data registers at the other regions can be accessed.

Control Word Setup Example

You need to set up the control words for the IO card at power up. To accomplish this task, a simple PLC could be written to set up the control word properly. For this example, we will be setting up an ACC-11C with Option 1.

Control Word for ACC-11C (`M2007->Y:$078C07,0,8`)




```
;**** ACC-11C Base Card Definitions ****

M2000->Y:$078C00,0,8          ;I/O bits 0-7 acc-11C base card
M2001->Y:$078C01,0,8          ;I/O bits 8-15 acc-11C base card
M2002->Y:$078C02,0,8          ;I/O bits 16-23 acc-11C base card
M2003->Y:$078C03,0,8          ;I/O bits 24-31 acc-11C base card
M2004->Y:$078C04,0,8          ;I/O bits 32-39 acc-11C base card
M2005->Y:$078C05,0,8          ;I/O bits 40-47 acc-11C base card
M2006->Y:$078C06,0,8          ;register selected
M2007->Y:$078C07,0,8          ;control register

;**** ACC-11C option 1 Definitions ****

M2008->Y:$078C00,8,8          ;I/O bits 0-7 acc-11c option1
M2009->Y:$078C01,8,8          ;I/O bits 8-15 acc-11c option1
M2010->Y:$078C02,8,8          ;I/O bits 16-23 acc-11c option1
M2011->Y:$078C03,8,8          ;I/O bits 24-31 acc-11c option1
M2012->Y:$078C04,8,8          ;I/O bits 32-39 acc-11c option1
M2013->Y:$078C05,8,8          ;I/O bits 40-47 acc-11c option1
M2014->Y:$078C06,8,8          ;register selected
M2015->Y:$078C07,8,8          ;control register

**IMPORTANT**  The ACC11C must be setup as specified.

;**** PLC to initialize read/write I/O bits ****
OPEN PLC 1 CLEAR
M2007=$0F                     ;define bits 0-31 as inputs and bits 32-47 as outputs (ACC-11C)
M2015=$0F                     ;define bits 0-31 as inputs and bits 32-47 as outputs (ACC-11C Opt1)
DIS PLC1
CLOSE
```

Accessory 11C I/O M-Variables for Compact UBUS Turbo

The following is a list of suggested M-variables for the default switch setting is provided. You may assign any M-variables to these addresses. You may make these M-variable definitions and use them as general purpose I/O for their PLCs or motion programs.

```
M7000->Y:$078C00,0,1   Input 0       M7024->Y:$078C03,0,1   Input 24
M7001->Y:$078C00,1,1   Input 1       M7025->Y:$078C03,1,1   Input 25
M7002->Y:$078C00,2,1   Input 2       M7026->Y:$078C03,2,1   Input 26
M7003->Y:$078C00,3,1   Input 3       M7027->Y:$078C03,3,1   Input 27
M7004->Y:$078C00,4,1   Input 4       M7028->Y:$078C03,4,1   Input 28
M7005->Y:$078C00,5,1   Input 5       M7029->Y:$078C03,5,1   Input 29
M7006->Y:$078C00,6,1   Input 6       M7030->Y:$078C03,6,1   Input 30
M7007->Y:$078C00,7,1   Input 7       M7031->Y:$078C03,7,1   Input 31
M7008->Y:$078C01,0,1   Input 8       M7032->Y:$078C04,0,1   Input 32
M7009->Y:$078C01,1,1   Input 9       M7033->Y:$078C04,1,1   Input 33
M7010->Y:$078C01,2,1   Input 10      M7034->Y:$078C04,2,1   Input 34
M7011->Y:$078C01,3,1   Input 11      M7035->Y:$078C04,3,1   Input 35
M7012->Y:$078C01,4,1   Input 12      M7036->Y:$078C04,4,1   Input 36
M7013->Y:$078C01,5,1   Input 13      M7037->Y:$078C04,5,1   Input 37
M7014->Y:$078C01,6,1   Input 14      M7038->Y:$078C04,6,1   Input 38
M7015->Y:$078C01,7,1   Input 15      M7039->Y:$078C04,7,1   Input 39
M7016->Y:$078C02,0,1   Input 16      M7040->Y:$078C05,0,1   Input 40
M7017->Y:$078C02,1,1   Input 17      M7041->Y:$078C05,1,1   Input 41
M7018->Y:$078C02,2,1   Input 18      M7042->Y:$078C05,2,1   Input 42
M7019->Y:$078C02,3,1   Input 19      M7043->Y:$078C05,3,1   Input 43
M7020->Y:$078C02,4,1   Input 20      M7044->Y:$078C05,4,1   Input 44
M7021->Y:$078C02,5,1   Input 21      M7045->Y:$078C05,5,1   Input 45
M7022->Y:$078C02,6,1   Input 22      M7046->Y:$078C05,6,1   Input 46
M7023->Y:$078C02,7,1   Input 23      M7047->Y:$078C05,7,1   Input 47
```

```
;****** Sample E-Stop PLC *****
; This PLC will abort all motion programs and kill the bus voltage to
; the motors when E-stop is depressed.  When E-Stop button in pulled out
; the motors will servo to actual position (<ctrl> A command) after
; allowing 5 seconds for proper bus voltage.
;     P7000 used as a Latch variable
;     M7000 used Emergency Stop Input
;     M8000 used as Main Contact for main AC for Bus Voltage
;     I5111 used as count down timer

OPEN PLC 5 CLEAR
IF (M7000=1 and P7000=0)      ;emergency stop condition
    CMD^A                     ;global motion program abort
    I5111=500*8388608/I10     ;500 msec delay for deceleration
    WHILE (I5111>0) ENDWHILE
    CMD^K                     ;kill all axes
    M8000=0                   ;turn off BUS voltage
    P7000=1                   ;latch input
Endif
```

```
IF (M7000=0 and P7000=1)
    M8000=1                    ;enable BUS voltage
    I5111=5000*8388608/I10     ;5000 msec delay for bus voltage
    WHILE (I5111>0) ENDWHILE
    CMD^A                      ;close loop for all servos
    P7000=0                    ;latch input
Endif
```

J1 CONNECTOR - COMPACT UBUS PIN-OUTS

Row	Z	A	B	C	D	E	F
25	GND	5V			3.3V	5V	GND
24	GND	BD02	5V	V(I/O)	BD01	BD00	GND
23	GND	3.3V	BD05	BD04	5V	BD03	GND
22	GND	BD09	BD08	3.3V	BD07	BD06	GND
21	GND	3.3V	BD13	BD12	BD11	BD10	GND
20	GND	BD17	GND	BD16	BD15	BD14	GND
19	GND	3.3V	BD20	BD19	GND	BD18	GND
18	GND	BD23	GND	3.3V	BD22	BD21	GND
17	GND	3.3V	{BD26}	{BD25}	GND	{BD24}	GND
16	GND	{BD30}	GND	{BD29}	{BD28}	{BD27}	GND
15	GND	3.3V	BWR-	BRD-	GND	{BD31}	GND
14	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*
13	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*
12	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*	*(KEY)*
11	GND	CS10-	CS4-	CS3-	GND	CS2-	GND
10	GND	CS16-	GND	3.3V	CS14-	CS12-	GND
9	GND	IREQ2-	IREQ1-	MEMCS1-	GND	MEMCS0-	GND
8	GND	PHASE+	GND	SERVO+	WAIT-	IREQ3-	GND
7	GND	PHASE-	WDO	SERVO-	GND		GND
6	GND	BA02	GND	3.3V	BA01	BA00	GND
5	GND	BA04	BA03	RESET-	GND	BX/Y	GND
4	GND	BA07	GND	V(I/O)	BA06	BA05	GND
3	GND	BA11	BA10	BA09	5V	BA08	GND
2	GND	{BA15}	5V	{BA14}	BA13	BA12	GND
1	GND	5V	-12V	PWRGUD	+12V	5V	GND

Notes:

1. Row 25 is physically at the top of the connector in its “normal” orientation; Row 1 is at the bottom. Looking from the front of the rack, Column Z is on the left; Column F is on the right.
2. Supply (Vxx & xxV) and ground pins are in the same locations as the Compact PCI bus.
3. Spaces marked *(KEY)* are for the mechanical key; these are not pins.
4. Pins marked with {} brackets are reserved for future use; the signals inside the brackets are proposed for future expansion to a 32-bit data bus and 16-bit address bus.
5. The BSxx slot select lines of the original UBUS are not present here.
6. The names in the table are taken from the UBUS specification sheet. Alternate names for these signals that match existing schematics are:
    a. BDxx = BDxx_B
    b. BAxx = BAxx_B
    c. Bxx- = Bxx_B-
    d. SERVO+/- = SERVO_B+/-
    e. PHASE+/- = PHASE_B+/-
    f. PWRGUD = PWMENA
    g. MEMCS0- = DPRCS1-
    h. MEMCS1- = VMECS1-
    i. IREQ1- = IRQB-
    j. IREQ2- = EQU_1-
    k. IREQ3- = EQU_2-
    l. WAIT = WAIT2-

J2 CONNECTOR - ACC-11C DIGITAL I/O PIN-OUTS

Row	A	B	C	D	E
22	OUT0	OUT1	ORET	OUT2	OUT3
21	OUT4	OUT5	ORET	OUT6	OUT7
20	OUT8	OUT9	ORET	OUT10	OUT11
19	OUT12	OUT13	ORET	OUT14	OUT15
18	OUT16	OUT17	ORET	OUT18	OUT19
17	OUT20	OUT21	ORET	OUT22	OUT23
16	OUT24	OUT25	ORET	OUT26	OUT27
15	OUT28	OUT29	ORET	OUT30	OUT31
14	IN0	IN1	O+V	IN2	IN3
13	IN4	IN5	ORET	IN6	IN7
12	IN8	IN9	INRET0-15	IN10	IN11
11	IN12	IN13	IN14	IN15	IN16
10	IN17	IN18	IN19	IN20	IN21
9	IN22	IN23	INRET16-31	IN24	IN25
8	IN26	IN27	IN28	IN29	IN30
7	IN31	IN32	IN33	IN34	IN35
6	IN36	IN37	IN38	IN39	IN40
5	IN41	IN42	INRET32-47	IN43	IN44
4	IN45	IN46	IN47	IN48	IN49
3	IN50	IN51	IN52	IN53	IN54
2	IN55	IN56	INRET48-63	IN57	IN58
1	IN59	IN60	IN61	IN62	IN63

ADDE E1 AT U25, E3 AT U29

REV			
REV 1	CHANGED CIRCUITRY AT IN00 THRU IN31 TO PROTECT INPUTS FROM REV VOLTAGE DAMAGE	PJ	2/6/01
REV 2	CHANGED CIRCUTRY AT OUT00 THRU OUT31 FROM "TLE-6228-GP" TO "ULN2803A"	GP	02/23/01
REV 3	ADDED BA12 TO J1-E2 ADDED BA13 TO J1-D2 CHANGED U1-1 FROM BA15 A TO BRD A- CHANGED U1-23 FROM BRD A- TO BD15 CHANGED U1-24 FROM 5V TO BRD A- ADDED E1 AT U25, E3 AT U29	PJ	5/7/01

J1

J1-1 CONN175-CPCI

+5V	A1	A1	+5V
{BA15}	A2	A2	
BA11	A3	A3	BA11
BA07	A4	A4	BA07
BA04	A5	A5	BA04
BA02	A6	A6	BA02
PHASE-	A7	A7	PHASE_B-
PHASE+	A8	A8	PHASE_B+
IREQ2-	A9	A9	
CS16-	A10	A10	CS16-
CS10-	A11	A11	CS10-
(KEY)	A12	A12	
(KEY)	A13	A13	
(KEY)	A14	A14	
+3.3V	A15	A15	
{BD30}	A16	A16	
+3.3V	A17	A17	
BD23	A18	A18	BD23
+3.3V	A19	A19	
BD17	A20	A20	BD17
+3.3V	A21	A21	
BD09	A22	A22	BD09
+3.3V	A23	A23	
BD02	A24	A24	BD02
+5V	A25	A25	+5V

J1-2 CONN175-CPCI

-12V	B1	B1	
+5V	B2	B2	+5V
BA10	B3	B3	
GND	B4	B4	GND
BA03	B5	B5	BA03
GND	B6	B6	GND
WDO	B7	B7	WDO
GND	B8	B8	GND
IREQ2-	B9	B9	
GND	B10	B10	GND
CS4-	B11	B11	CS4-
(KEY)	B12	B12	
(KEY)	B13	B13	
(KEY)	B14	B14	
BWR-	B15	B15	BWR-
GND	B16	B16	GND
{BD26}	B17	B17	
GND	B18	B18	GND
{BD20}	B19	B19	BD20
GND	B20	B20	GND
BD13	B21	B21	BD13
BD08	B22	B22	BD08
BD05	B23	B23	BD05
+5V	B24	B24	+5V
N.C.	B25	B25	

J1-3 CONN175-CPCI

PWRGUD	C1	C1	
{BA14}	C2	C2	
BA09	C3	C3	
V(I/O	C4	C4	V(I/O)
RESET-	C5	C5	RESET
+3.3V	C6	C6	
SERVO-	C7	C7	SERVO_B-
SERVO+	C8	C8	SERVO_B+
MSMCS1-	C9	C9	
+3.3V	C10	C10	
CS3-	C11	C11	CS3-
(KEY)	C12	C12	
(KEY)	C13	C13	
(KEY)	C14	C14	
BRD-	C15	C15	BRD-
{BA29}	C16	C16	
BA25}	C17	C17	
+3.3V	C18	C18	
BD19	C19	C19	BD19
BD16	C20	C20	BD16
BD12	C21	C21	BD12
+3.3V	C22	C22	
BD04	C23	C23	BD04
V(I/O)	C24	C24	V(I/O)
N.C.	C25	C25	

J1-4 CONN175-CPCI

+12V	D1	D1	
BA13	D2	D2	BA13
+5V	D3	D3	
BA06	D4	D4	BA06
GND	D5	D5	+5V
BA01	D6	D6	BA01
GND	D7	D7	GND
WAIT-	D8	D8	
GND	D9	D9	GND
CS14-	D10	D10	CS14-
GND	D11	D11	GND
(KEY)	D12	D12	
(KEY)	D13	D13	
(KEY)	D14	D14	
GND	D15	D15	GND
{BA24}	D16	D16	
GND	D17	D17	GND
DB22	D18	D18	BD22
GND	D19	D19	GND
BD15	D20	D20	BD15
BD11	D21	D21	BD11
BD07	D22	D22	BD07
+5V	D23	D23	
BD01	D24	D24	BD01
+3.3V	D25	D25	+5V

J1-5 CONN175-CPCI

+5V	E1	E1	
BA12	E2	E2	BA12
BA08	E3	E3	
BA05	E4	E4	BA05
RX/Y	E5	E5	
BA00	E6	E6	BA00
N.C.	E7	E7	
IREQ2-	E8	E8	
MSMCS0-	E9	E9	
CS12-	E10	E10	CS12-
CS2-	E11	E11	CS2-
(KEY)	E12	E12	
(KEY)	E13	E13	
(KEY)	E14	E14	
{BD31}	E15	E15	
{BD27}	E16	E16	
{BD24}	E17	E17	
BD21	E18	E18	BD21
BD18	E19	E19	BD18
BD14	E20	E20	BD14
BD10	E21	E21	BD10
BD06	E22	E22	BD06
BD03	E23	E23	BD03
BD00	E24	E24	BD00
+5V	E25	E25	+5V

J1-6 CONN175-CPCI

GND	F1	F1	
n.c.	F2	F2	
GND	F3	F3	
n.c.	F4	F4	
GND	F5	F5	
n.c.	F6	F6	
GND	F7	F7	
n.c.	F8	F8	
GND	F9	F9	
n.c.	F10	F10	
GND	F11	F11	
n.c.	F12	F12	
GND	F13	F13	
n.c.	F14	F14	
GND	F15	F15	
n.c.	F16	F16	
GND	F17	F17	
n.c.	F18	F18	
GND	F19	F19	
n.c.	F20	F20	
GND	F21	F21	
n.c.	F22	F22	
GND	F23	F23	
n.c.	F24	F24	
GND	F25	F25	GND
n.c.	F26	F26	

U1 — P174FCT16245ATA (TSSOP)

BCS-	48	1	
BD00	47	2	BD00_A
BD01	46	3	BD01_A
GND	45	4	GND
BD02	44	5	BD02_A
BD03	43	6	BD03_A
A3	42	7	
VCC	41	8	
BD04	40	9	BD04_A
BD05	39	10	BD05_A
GND	38	11	GND
BD06	37	12	BD06_A
BD07	36	13	BD07_A
BD08	35	14	BD08_A
BD09	34	15	BD09_A
GND	33	16	GND
BD10	32	17	BD10_A
BD11	31	18	BD11_A
VCC	30	19	VCC
BD12	29	20	BD12_A
BD13	28	21	BD13_A
GND	27	22	GND
BD14	26	23	BD14_A
BD15	25	24	BD15_A
OE2			T/R2

U2 — P174FCT16245ATA (TSSOP)

BCS-	48	1	
BD16	47	2	BD16_A
BD17	46	3	BD17_A
A1	45	4	
GND	44	5	GND
BD18	43	6	BD18_A
BD19	42	7	BD19_A
VCC	41	8	VCC
A4	40	9	
A5	39	10	
GND	38	11	GND
A6	37	12	
A7	36	13	
A8	35	14	
A9	34	15	
GND	33	16	GND
A10	32	17	
A11	31	18	
VCC	30	19	VCC
A12	29	20	
A13	28	21	
GND	27	22	GND
A14	26	23	
A15	25	24	
OE2			T/R2

C1–C8 .1UF; C9 .1UF; C10 .1UF; C11 .1UF; C12 .1UF

U5 — ST34C86CF16 (SO16)

SERVO_B-	1	16	VCC
SERVO_B+	2	3	OUT-A
	4		ENA-A,C
	6	5	OUT-C
	7		IN-C
	15		IN-B
	14	13	OUT-B
	12		ENA-B,D
	10	11	OUT-D
	9	8	GND

RP2 220SIP8 SIP SOCKET; C14 .1UF; IOGCLK; OUT0-; OUT0

TO RECIVE "SERVO" OR TO LET "PMAC" CONTROL JUMP "E2" 1-TO-2
TO RECIVE "PHASE" (JUMPER CONTROL ONLY) JUMP "E2" 2-TO-3
JUMP "E2" 1-TO-2 FOR IOGCLK = SERVO
JUMP "E2" 2-TO-3 FOR IOGCLK = PHASE

LM2930S-5.0 VR2; O+5V-2; C115 .1UF; C116 22UF 25V; C117 100UF 35V; D60 15SMC33AT3; O+V; ORET

(jisp) J5 HSIP8NO5: TDO, TDI, BSCAN-, TMS, TCK; C13 .01UF

OPEN "SW1,5,6" FOR "DELTA TAU MACRO_IU CPU (602804)", OR ANY NON-TURBO CPU.

U3 — ISPLSI2064E_UNIV_DECODE (TQFP 100)

VCCIO	1	100	N.C.
GND	2	99	N.C.
BA12	3	98	BA05_A
BA13	4	97	BA04_A
CS16-	5	96	BA03_A
CS14_4-	6	95	BA02_A
CS12_3-_A9	7	94	BA01_A
CS10_2-_A8	8	93	BA00_A
BRD-	9	92	IOGCS-
N.C.	10	91	BCSXX-
BWR-	11	90	BCS16L-
VCC	12	89	BCS16H-
GND	13	88	N.C.
RSCAN-	14	87	GND
RESET-	15	86	GOE_1
TDI	16	85	BCS-
CO0-	17	84	OUT0
CO1-	18	83	BD05
CO2-	19	82	BD04
CO3-	20	81	BD03
CO4-	21	80	BD02
CO5-	22	79	BD01
CO6-	23	78	BDO0
VCCIO	24	77	S13
GND	25	76	N.C.
N.C.	26	75	N.C.
CO7-	27	74	VCCIO
CO8-	28	73	GND
CO9-	29	72	S12
CR0-	30	71	S5
CR1-	31	70	S4
CR2-	32	69	S3
CR3-	33	68	S2
CT0-	34	67	CLKEN
CT1-	35	66	CLK
TMS	36	65	GOE_0
GND	37	64	Y1
TDO	38	63	VCC
CT2-	39	62	GND
CT3-	40	61	Y2
CT4-	41	60	N.C.
CT5-	42	59	TCK
CT6-	43	58	IN3
CT7-	44	57	IN2
CT8-	45	56	IN1
CT9-	46	55	IN0
CT10-	47	54	CT13-
N.C.	48	53	CT12-
N.C.	49	52	CT11-
	50	51	VCCIO
			GND

BSCAN-; RESET-; TDI; OPTION #1; OPTION #2; OPTION #3; SOLDER JUMPER; C10 .1UF; OUT0; OPT#; REV=0; TMS; TDO; P/N= 3603 $E13; C9 .1UF; C12 .1UF; C11 .1UF; TCK; PB_INT-

RP1 47KDIP10C; SW1 SW DIP-6: BS0, BS1, BS2, BS3, BA12, BA13

R2 4.7K; R3 1K; R4 1K; R5 4.7K; R6 1K; R7 1K

D61–D66 LED-GRN; ORET

J2

J2-1 CONN154-CPCI

IN59	A1	A1	IN00
IN55	A2	A2	IN01
IN50	A3	A3	IN02
IN45	A4	A4	IN03
IN41	A5	A5	IN04
IN36	A6	A6	IN05
IN31	A7	A7	IN06
IN26	A8	A8	IN07
IN22	A9	A9	IN08
IN17	A10	A10	IN09
IN12	A11	A11	IN10
IN08	A12	A12	IN11
IN04	A13	A13	IN12
IN00	A14	A14	IN13
OUT26	A15	A15	IN14
OUT24	A16	A16	IN15
OUT20	A17	A17	IN16
OUT16	A18	A18	IN17
OUT12	A19	A19	IN18
OUT08	A20	A20	IN19
OUT04	A21	A21	IN20
OUT00	A22	A22	IN21

J2-2 CONN154-CPCI

IN60	B1	B1	IN22
IN56	B2	B2	IN23
IN51	B3	B3	IN24
IN46	B4	B4	IN25
IN42	B5	B5	IN26
IN37	B6	B6	IN27
IN32	B7	B7	IN28
IN27	B8	B8	IN29
IN23	B9	B9	IN30
IN18	B10	B10	IN31
IN13	B11	B11	IN32
IN09	B12	B12	IN33
IN05	B13	B13	IN34
IN01	B14	B14	IN35
OUT29	B15	B15	IN36
OUT25	B16	B16	IN37
OUT21	B17	B17	IN38
OUT17	B18	B18	IN39
OUT13	B19	B19	IN40
OUT09	B20	B20	IN41
OUT05	B21	B21	IN42
OUT01	B22	B22	IN43

J2-3 CONN154-CPCI

IN61	C1	C1	IN44
INRET48-64	C2	C2	IN45
IN52	C3	C3	IN46
IN47	C4	C4	IN47
INRET32-47	C5	C5	IN48
IN38	C6	C6	IN49
IN33	C7	C7	IN50
IN28	C8	C8	IN51
INRET16-31	C9	C9	IN52
IN19	C10	C10	IN53
IN14	C11	C11	IN54
INRET0-15	C12	C12	IN55
ORET	C13	C13	IN56
O+V	C14	C14	IN57
OUTRET28-32	C15	C15	IN58
OUTRET24-27	C16	C16	IN59
OUTRET20-23	C17	C17	IN60
OUTRET16-19	C18	C18	IN61
OUTRET12-15	C19	C19	IN62
OUTRET8-11	C20	C20	IN63
OUTRET4-7	C21	C21	
OUTRET0-3	C22	C22	

J2-4 CONN154-CPCI

IN62	D1	D1	OUT00
IN57	D2	D2	OUT01
IN53	D3	D3	OUT02
IN48	D4	D4	OUT03
IN43	D5	D5	OUT04
IN39	D6	D6	OUT05
IN34	D7	D7	OUT06
IN29	D8	D8	OUT07
IN24	D9	D9	OUT08
IN20	D10	D10	OUT09
IN15	D11	D11	OUT10
IN10	D12	D12	OUT11
IN06	D13	D13	OUT12
IN02	D14	D14	OUT13
OUT30	D15	D15	OUT14
OUT26	D16	D16	OUT15
OUT22	D17	D17	OUT16
OUT18	D18	D18	OUT17
OUT14	D19	D19	OUT18
OUT10	D20	D20	OUT19
OUT06	D21	D21	OUT20
OUT02	D22	D22	OUT21

J2-5 CONN154-CPCI

IN63	E1	E1	OUT22
IN58	E2	E2	OUT23
IN54	E3	E3	OUT24
IN49	E4	E4	OUT25
IN44	E5	E5	OUT26
IN40	E6	E6	OUT27
IN35	E7	E7	OUT28
IN30	E8	E8	OUT29
IN25	E9	E9	OUT30
IN21	E10	E10	OUT31
IN16	E11	E11	
IN11	E12	E12	
IN07	E13	E13	
IN03	E14	E14	
OUT31	E15	E15	
OUT27	E16	E16	
OUT23	E17	E17	
OUT19	E18	E18	
OUT15	E19	E19	
OUT11	E20	E20	
OUT07	E21	E21	
OUT03	E22	E22	

J2-6 CONN154-CPCI

F1	F1	F1	
F2	F2	F2	
F3	F3	F3	
F4	F4	F4	
F5	F5	F5	
F6	F6	F6	
F7	F7	F7	
F8	F8	F8	
F9	F9	F9	
F10	F10	F10	
F11	F11	F11	
F12	F12	F12	
F13	F13	F13	
F14	F14	F14	
F15	F15	F15	
F16	F16	F16	
F17	F17	F17	
F18	F18	F18	
F19	F19	F19	
F20	F20	F20	
F21	F21	F21	
F22	F22	F22	
GND	GND	F22	

INRET0-15 ↔ INRET16-31; INRET32-47 ↔ INRET48-63

J4 CON30

	1	1	+5V
	2	2	GND
BD08_A	3	3	BD08_A
BD09_A	4	4	BD09_A
BD10_A	5	5	BD10_A
BD11_A	6	6	BD11_A
BD12_A	7	7	BD12_A
BD13_A	8	8	BD13_A
BD14_A	9	9	BD14_A
BD15_A	10	10	BD15_A
BRD_A-	11	11	BRD-_A
BWR_A-	12	12	BWR-_A
BA00_A	13	13	BA00_A
BA01_A	14	14	BA01_A
BA02_A	15	15	BA02_A
IOGCS-	16	16	IOGCS-
PB_INT-	17	17	PB_INT-
IOGCLK	18	18	IOGCLK
RESET-	19	19	RESET-
O+5V-2	20	20	O+5V-2
O+5V-2	21	21	O+5V-2
O+V	22	22	O+V
O+V	23	23	O+V_
O+V_2LED	24	24	O+V_2LED
O+5V-2LED	25	25	O+5V-2LED
+5V-2LED	26	26	+5V-2LED
	27		
	28		
	29	29	GND
	30	30	+5V

DELTA TAU DATA SYSTEMS, Inc.

Title: MAIN CPCI 96I/O (I/O00-47)

Size: D | Document Number: 603603-323 | Rev: -

Date: Monday, May 07, 2001 | Sheet 1 of 2

SEE SHT 1

SEE SHT 1

J3

CON60

INRET0-15
INRET16-31

+5V
GND

O+V_

ORET

O+V

TERMBLK 2

ULN2803A (IN SOCKET)

IOGATE (PLCC84) (IN SOCKET)

E1 JUMPER

E3 JUMPER

CUT TO DISCONNECT PROTECTIVE DIODES

LM2930S-5.0

RUE-090, 0.9 amp

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