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OPERATING MANUAL

PENTEK MODEL 6215

8-Channel 16-bit A/D Converter
VIM-2 Module for Pentek VIM Motherboards

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Pentek Model 6215 Operating Manual – Revision History

Date	Rev	Applicable Serial #'s	Comments
05/17/99	Preliminary	9919001 – Forward	Initial release.
05/27/99	Preliminary	9919001 – Forward	Sections 3.4, 3.5 & 3.6 clarified descriptions of the Overload Interrupt Enable, Interrupt Source Register & Overload Interrupt Source Register
06/03/99	Preliminary	9919001 – Forward	Added Figure 2–2, shows the pinout numbers for the Analog In and the Dist/Sync connectors.
06/30/99	Preliminary	9919001 – Forward	Sect 1.1, Sect 1.4 & Figure 1–1, changed reference from A/D converters to A/D channels also changed names of input channels from A1, A2, A3, A4, B1, B2, B3 and B4 to CH 1, CH 2, CH 3, CH 4, CH 5, CH 6, CH 7 and CH 8.
08/31/99	Preliminary	9919001 – Forward	Figure 2–2, change pinouts on 8 pin Dist/Sync connector
11/30/99	Preliminary	9919001 – Forward	Sect 3.9, corrected Freq equation. Table 3–13, corrected Clock Divider and Sample Frequency Values.
12/01/99	Preliminary	9919001 – Forward	Sect 1.6; added DC offset specification
12/10/99	A	9919001 – Forward	Removed former Appendix B – Sample Code (superseded by 801.62150). Changed former Appendix C (AD7722 manual) to Appendix B.
06/05/00	B	9919001 – Forward	This revision is a near–complete re–write. Too many changes were made to possibly include them all here, but the highlights follow. Chapter 1: General grammatical clean–up & clarification; Where applica–ble, the phrase "VIM Motherboard" replaces "4290/1" and "Motherboard processor" replaces "C6x"; In Section 1.6 (Specs), identify PGA, correct sample rate range and equation for divider, add cross references to device data sheets, add board dimensions. Chapter 2: Redraw Figs 2–1 & 2–2; Add component & sol–der side assembly drawings; Rearrange the content of Table 2–1 such that the pins it defines appear in the same orientation as on the panel; Add Sec. 2.4.1 discussing Analog Input ckt., & Fig. 2–5 illustrating same; Add more in–depth discussion of signals on **DIST/SYNC** connector; Re–arrange Table 2–2 to match pinout; Add section describing **EXT CLK** input, w/ figure; Add section describing F/P LEDs. Chapter 3: Replace the 2nd table in each section, which described the register bits, with more in–depth discussion in subsections; Some registers and MANY bits re–named to give a clearer idea of their function. Add mne–monic column to memory map (Table 3–1); Add Sec. 3.3 & Table 3–2, on A/D channel ID based on which MB processor conducts the access; Enhance Sample Rate Table (formerly 3–13, now 3–9) to include all 3 available internal oscillators; Add Fig. 3–1, illustrating the functions of the various Sync control bits; Add Sec. 3.16 & Tables 3–16 & 3–17, discussing & illustrating output data formats. Appendices: Move AD7722 to A; Include PGA207 as B; move EEPROM to C.
01/03/01	B.1	9919001 – Forward	Sect. 1.6, Specifications; corrected maximum sample rate for Option 010, incorrectly stated 120 MHz, changed to 120 kHz. Also for Sect. 1.6, Specifications; corrected reference frequency for Option 011, incorrectly stated 25 kHz, changed to 25 MHz.
02/01/01	B.2	9919001 – Forward	Sect. 3.11.6 and 3.11.7, Termination Enable and Master Enable must be set to one in stand alone mode.

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Chapter 1: Overview

1.1 General Description

Model 6215 is an 8−channel, 16 bit A/D converter VIM−2 module which attaches directly to a VIM motherboard.

The eight A/D converters are arranged as four pairs of converters, Channels 1 & 2, Channels 3 & 4, Channels 5 & 6 and Channels 7 & 8. The module is assigned to a pair of processors on a VIM motherboard. Each of these two processors normally controls two pairs of A/D converters with one group of two A/D pairs assigned as primary pairs, and the other group assigned as secondary pairs).

Within each group, one pair of A/D channels is connected to one of the motherboard processor's serial ports and the other pair to the second serial port. One processor has primary access to channels 1 – 4 and secondary access to channels 5 – 8, while the other processor has primary access to channels 5 – 8 and secondary access to channels 1 – 4. Referring to the Simplified Block Diagram of the Model 6215, presented in Figure 1−1, on the next page, we see that a given processor's primary A/D channels are those that are connected to that processor's serial ports.

Two Model 6215s may be attached to a VIM motherboard, to form a 16−channel A/D converter utilizing all four processors while occupying only one VMEbus slot. Alternately, the Model 6215 may be combined with another VIM−2 module to provide additional I/O functions.

1.2 A/D Converters

Analog inputs to the eight A/D converters are accepted from a 36−pin front panel connector with provisions for either single−ended or differential signals. The analog input for each A/D converter is fed through a Programmable Gain Amplifier (PGA) which covers a 0 to 20 dB range with a ±10 V differential input signal.

The amplifier's gain is programmable in steps of one, two, five and ten. In order to utilize the A/D converter's full−scale input range, the gain must be set to one for a differential input voltage of ±10 V or a gain of ten for a differential input voltage of ±1 V.

The A/D converters utilize sigma−delta technology and include anti−aliasing filters with a cutoff frequency that tracks at 46% of the sample rate.

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1.3 Model 6215 Block Diagram

Figure 1–1, below, shows a simplified block diagram of the Model 6215.

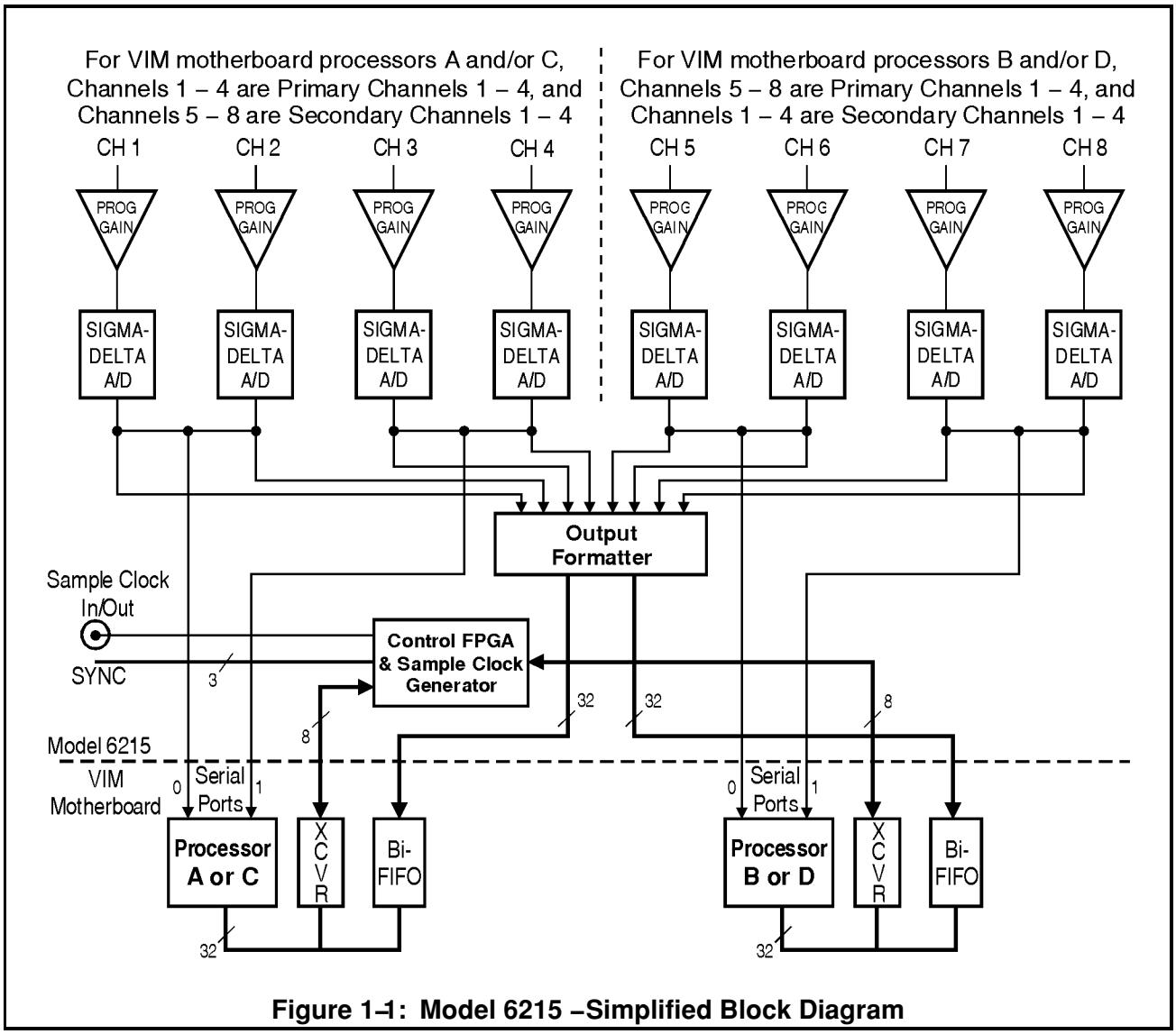


Figure 1–1: Model 6215 –Simplified Block Diagram

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1.4 Formatting the Output of the 6215 A/D Converter

The 6215 A/D converter's output samples can be read by the Motherboard processor in one of two ways, serial or parallel.

In serial mode, sample data from each pair of A/D converters is sent to one VIM serial port, through a Field Programmable Gate Array (FPGA), as a formatted thirty−two bit word. Data from channels 1 and 2 are sent to serial port 0 of one processor, and data from channels 3 and 4 are sent to that processor's serial port 1. Output samples from channels 5 and 6 are sent to serial port 0 of the other processor, and the outputs of channels 7 and 8 are sent to that processor's serial port 1.

In parallel mode sample data from all the A/D converters is available for output to either processor, via the FPGA to the Bi−FIFOs on the VIM motherboard. Individual A/D channels may be enabled to, or masked from, delivering data to the VIM Bi−FIFO.

All A/D channels must be programmed for the same output format. If either processor sets parallel mode, then all channels are in parallel mode. In either serial or parallel output mode, either processor can control (i. e., master) the other processor's group of A/D converters, but both VIM processors should not be programmed for master mode at the same time.

1.5 Communication and Synchronization with the VIM Motherboard

Each processor communicates with an FPGA, in asynchronous VIM memory space. The FPGA contains registers to calibrate, synchronize, set the clock divider and front−end gains of the A/D channels. A supervisory chip generates resets to the A/D converter and FPGA. A power−up or a reset signal from either VIM interface triggers the supervisory chip's reset. The reset is then distributed to the A/D converters and the FPGAs.

An additional supervisory chip is used to control the program loading of the FPGAs. After a power−on reset one FPGA (this is the **Output Formatter** shown in Figure 1−1) loads program data from an EEPROM. The Output Formatter then programs the two other FPGAs (the **Control FPGA and Sample Clock Generator** in Figure 1−1) through its DATAOUT pin. After reset, the **Output Formatter** and **Control FPGA** registers are cleared, all state machines are in an idle state and the data interface is set for serial mode.

In serial mode, the **Output Formatter** assembles data from each pair of A/D converters and sends a framed 32−bit data stream to the VIM serial ports. The clock signal for this data stream is the reference clock. The frame−sync and serial data are shifted out on the rising edge of the serial clock and sampled by the VIM processor on the falling edge. The VIM interface can also source the serial clock, with the same timing scheme as for the reference clock. The serial ports must be held in reset while changing the clock divider or clock source, or until the data−valid bits in the DATA_VALID register are set. The channels are reset in the Serial Control register. Resetting an A/D channel also holds its associated serial port in reset. Selection of the serial clock source is also provided by bits in the Serial Control Register.

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1.5 Communication and Synchronization with VIM Motherboard (continued)

The A/D converter sets the data−valid bit high after the first conversion cycle. The data−valid bit will remain high as long as an overload, reset, calibration or Sync condition does not exist. The data−valid bit is also used to drive the overload interrupt state machine. After data−valid goes high the overload interrupt state machine enters the Armed state. If the data−valid bit goes low (except in response to a reset, calibration or Sync event) the state machine will enter the Interrupt State. If the Interrupt Enable bit is set for that A/D converter and another interrupt in not pending, an Overload Interrupt will be generated. To clear the Overload Interrupt, write a '1' to the Overload Status register bit in question, then clear that same bit to the logic'0' state. This action also puts the Overload Interrupt state machine back in its Idle state. The data−valid signal must then go high to cause a transition from the Idle state to the Armed state. This will happen when the overload condition is removed.

A synchronizing event, either internal or external, will reset the serial/parallel port controllers. Each A/D converter pair can be synchronized either independently or as part of a group. The A/D Synchronization and Calibration (Sync_Cal) Register sets the enables for internal Sync control. Bit D5 in this register drives the Sync state machine. After the Sync enable bits are set in the Sync/cal control register, writing a '1' to D5 of the register will "kick off" the Sync state machine. The Sync state machine sets the enabled Sync bits and waits for D5 to be reset. After bit D5 in the register is reset, the state machine resets all the enabled Sync signals and returns to the idle state. If the external Sync select bits are set, the external Sync signal sets the enabled Sync signals. The external Sync signal is clocked in on the high−going edge of the distributed clock. An external Sync event can generate a VIM interrupt. Bit D2 in the Interrupt Source register is used for the interrupt enable. If this bit is set, an external Sync event will generate an interrupt. The interrupt is cleared by setting bit D1 to the logic '1' state, then clearing that bit to the logic '0' state. The external Sync event is latched. After a power−up or a reset, the user should calibrate and, if desired, synchronize the A/D converters.

In parallel mode the FIFO Channel Select register sets the enables for all eight (8) A/D converters. Each bit in the register is an enable for the FIFO state machine. The state machine cycles through all eight channels, and if the bit for that channel is set, a FIFO enable pulse is generated and data is written into that FIFO. The FIFO write and chip select for the VIM interfaces are enabled all the time. The FIFO full flag is synchronized to the FIFO state machine. If the FIFO is full the FIFO enable is masked off. Of course this action will result in loss of real time data. After a reset the first sample of every channel is marked with a '1' in bit D3 of the FIFO. Also a "MARK" bit is available from the front panel. This bit can be driven by a CMOS/TTL compatible signal applied at pin 18 of the Analog Input connector. This bit is directly connected to bit D4 of the FIFO. When not connected, this signal defaults to the logic '1' state.

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1.6 Specifications

Input Amplifiers

Number:	8 instrumentation amplifiers (Burr/Brown PGA702††)
Inputs:	Differential, ±1 V (2 V_{P-P}) to ±10 V full scale (20 V_{P-P}), 10 kΩ input impedance, ±40 V over−voltage protection
Input Gain:	Independently programmable in steps of x1, x2, x5 & x10

†† – Data Sheet included in this manual as Appendix B

A/D Converters

Number:	8
Type:	Analog Devices AD7722†
Sample Rate (f_s)	4.6875 kHz to 234.375 kHz (with standard 30 MHz internal reference oscillator)
Resolution:	16 bits*
Full Scale Input Range:	±10 V (20 V_{P-P})
Crosstalk:	< −75 dB*
THD:	< −85 dB below full scale*
SFDR:	> 85 dB*
DC_{offset}:	≤ 50 mV**

† – Data Sheet included in this manual as Appendix A
* – For f_{in} = 10 kHz and $f_s \leq$ 195 kHz
** - Reflected from A/D converter to front panel input

Sampling Clocks

Internal Reference:

Standard:	30 MHz (±100 ppm)
Option 010:	30.72 MHz (±100 ppm) – allows 8 kHz sampling
Option 011:	25 MHz (±100 ppm) – allows sampling @ > 195 kHz

External Reference:	600 kHz min., 30 MHz max., TTL compatible front panel SMA input (EXT CLK)
Frequency dividers:	four, one for each A/D pair; each divides internal or external reference clock by 128 x (N + 1), where 0 ≤ N ≤ 49

Sample Rate (f_s), as a function of Reference Frequency:

Standard (30 MHz):	4.6875 kHz min., 234.375 kHz max.
Option 010 (30.72 MHz):	4.8 kHz min., 120 kHz max. (Note: 1 ≤ N ≤ 50)
Option 011 (25 MHz):	4.7637 kHz min., 195.3125 kHz max. (Note: 0 ≤ N ≤ 40)

Control Registers:	sample clock dividers, A/D channel enables, gain control, and clock divider input reference select.
Power:	2.0 A @ + 5 V_{DC} 0.5 A @ +12 V_{DC} 0.5 A @ −12 V_{DC}

Dimensions:	VIM−2 Module
Height:	114 mm (4.50 in.)
Depth:	82 mm (3.25 in.)
Width:	20 mm (0.80 in.)

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the original shipping container and packing material in case reshipment is required.

2.2 Jumper Blocks and Assembly Drawings

There are no jumper blocks, user–configurable or otherwise, on the Model 6215. All functions on the Model 6215 are programmable via software, rather than by jumper selection.

Component– and solder–side assembly drawings of the Model 6215 are presented for your reference in Figure 2–3, on the next page. Note that most component–side parts are normally hidden under the heat sink/shielding can, shown in Figure 2–4, on the page after next.

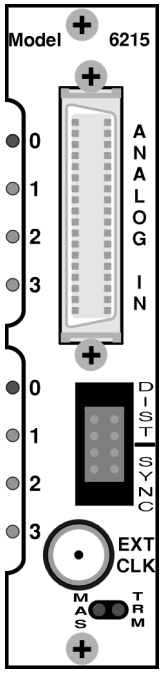


Figure 2–1: Model 6215 – Front Panel

2.3 Front Panel

The Model 6215 front panel, shown in Figure 2–1, top right, includes a 36–pin Analog Input connector, an eight pin Distribution Clock and Sync connector and an SMA connector for an external clock signal. The pin numbers for both multi–pin connectors are illustrated in Figure 2–2, at the right. Characteristics of the signals that may be applied at these inputs are discussed in Sections 2.4, 2.5, and 2.6.

A total of ten LEDs are visible through each Model 6215's front panel. Eight of these (two groups of four, one red and three green, each labeled 0 – 3) are actually mounted on the VIM motherboard, and can be seen through the cutouts at the left side of the panel. Consult the VIM motherboard's manual for details about these indicators.

Two more red LEDs near the bottom of the 6215's panel indicate the modules status on the Sync bus. These indicators will be discussed in Section 2.7, on page 21.

If only one VIM module is installed on the motherboard, the other module position can be covered with a blank panel.

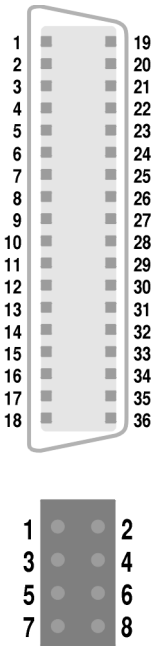
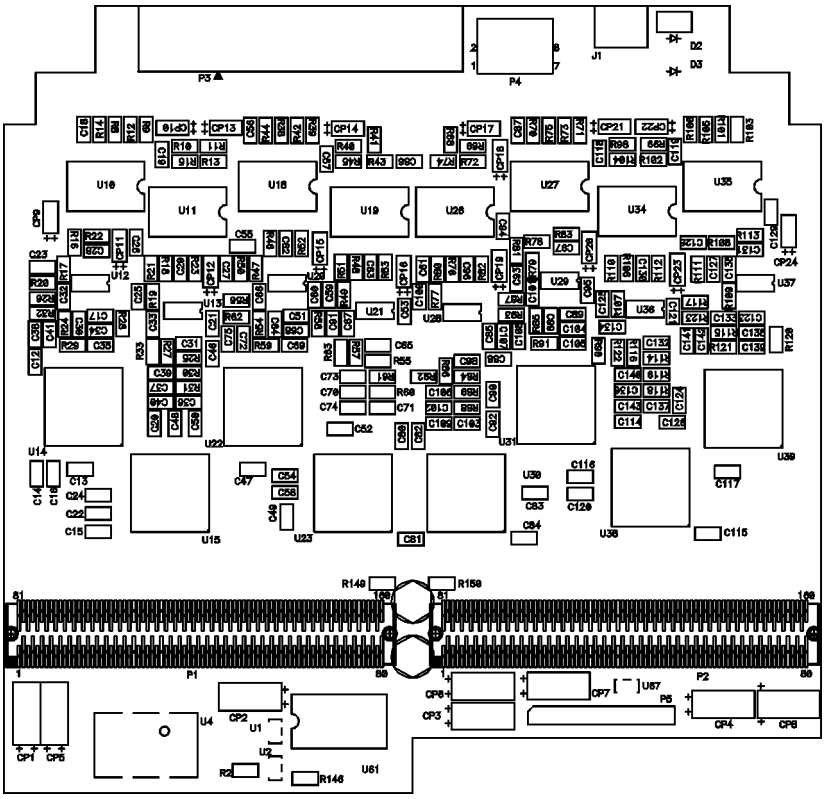
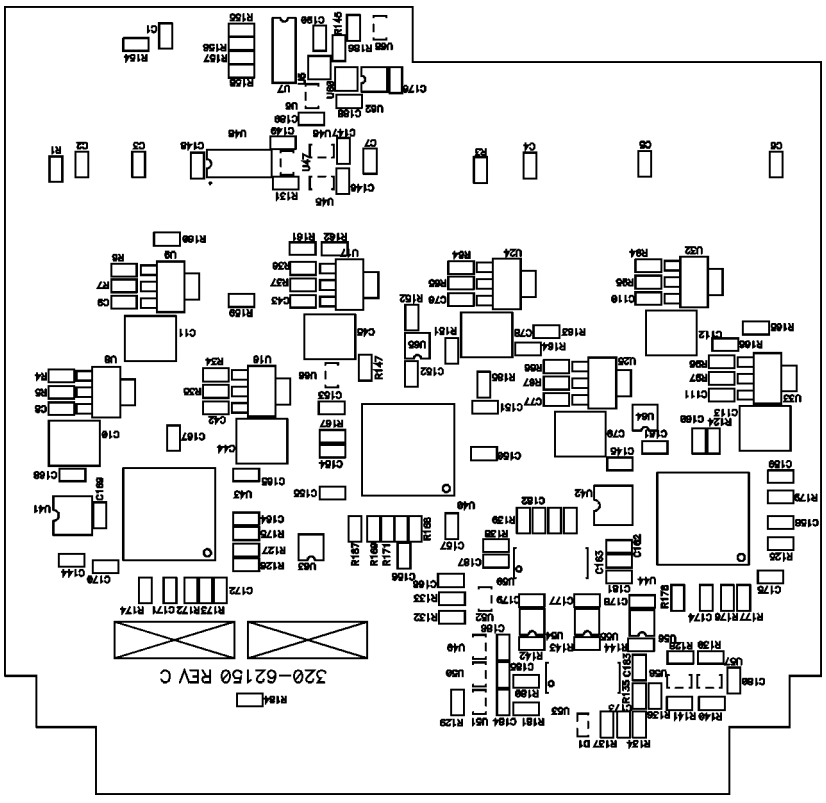


Figure 2–2: Model 6215 – Pin Numbering

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(a) –Component Side



(b) –Solder Side

Figure 2-3: Model 6215 - PC Board Assembly Drawings, Showing VIM Connectors and Mounting Hole Locations

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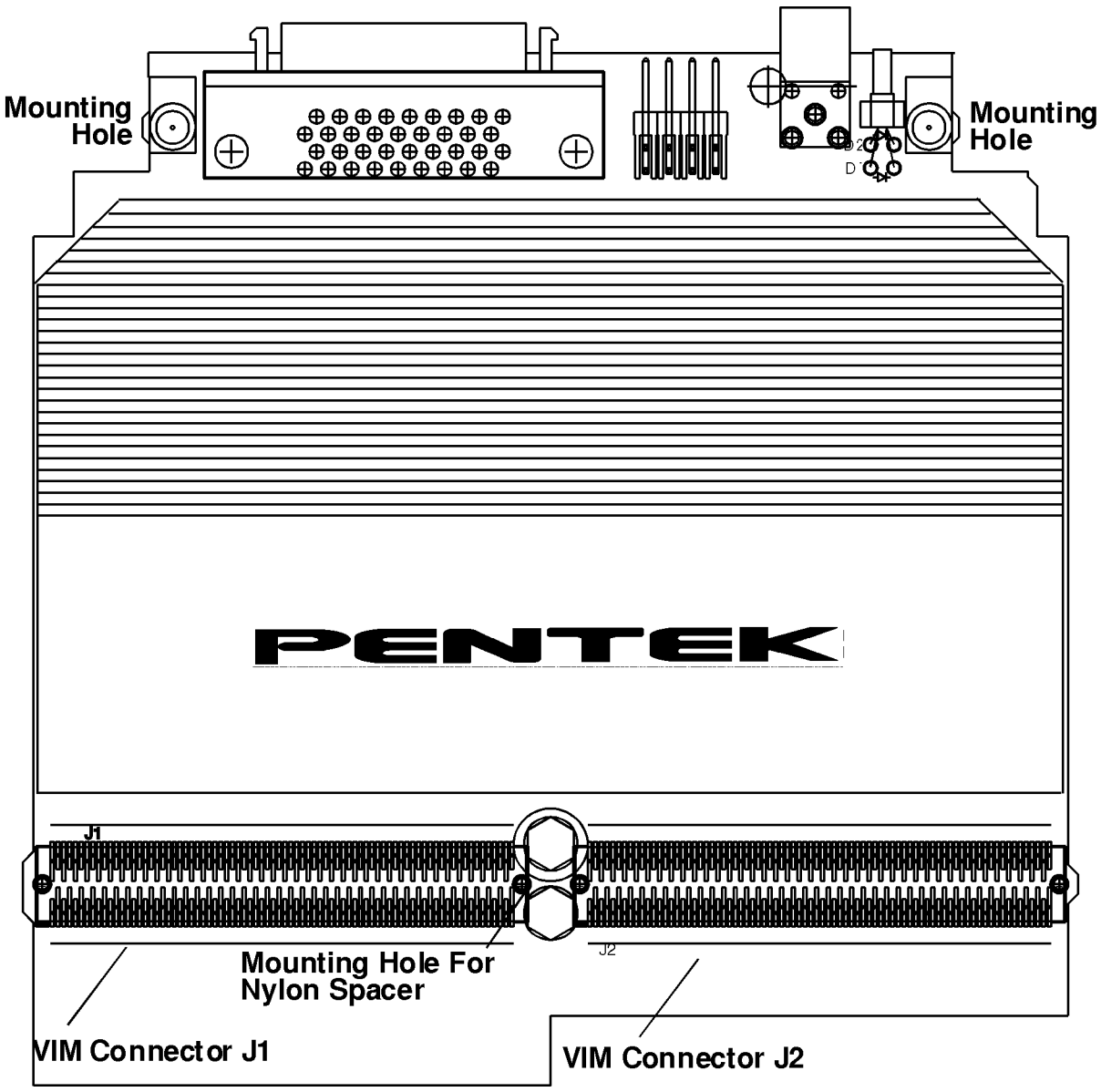


Figure 2-4: Model 6215 –Fully Assembled with Heat Sink / Shielding Can

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2.4 Analog Input Connector

The **ANALOG IN** connector on Pentek's Model 6215 is a 36–pin connector (3M part number N10236–5212VC Pentek part number 351.03601). Cable connectors that mate with the 6215's analog input connector include 3M part numbers 10136–3000VE (a shielded, solder–plug connector) and 10136–6000EC (a shielded, insulation–displacement, Ribbon cable connector). Table 2–1, below, gives the pinout of this connector.

Table 2–1: Model 6215 – Analog Input Connector Pinout

Pin	Description	Pin	Description
1	Analog GND	19	Analog GND
2	CH 1 IN +	20	CH 1 IN –
3	Analog GND	21	Analog GND
4	CH 2 IN +	22	CH 2 IN –
5	Analog GND	23	Analog GND
6	CH 3 IN +	24	CH 3 IN –
7	Analog GND	25	Analog GND
8	CH 4 IN +	26	CH 4 IN –
9	Analog GND	27	Analog GND
10	CH 5 IN +	28	CH 5 IN –
11	Analog GND	29	Analog GND
12	CH 6 IN +	30	CH 6 IN –
13	Analog GND	31	Analog GND
14	CH 7 IN +	32	CH 7 IN –
15	Analog GND	33	Analog GND
16	CH 8 IN +	34	CH 8 IN –
17	Analog GND	35	Analog GND
18	"Mark" Bit	36	Digital GND

2.4.1 Analog Input Circuit Description

Each analog input signal pin on the Model 6215's front panel drives a resistive voltage divider of approximately 10 kΩ impedance. This divider attenuates the amplitude of the signal applied to the pin by a factor of about 8. The attenuated signals are fed to the input of a differential, programmable gain instrumentation amplifier, whose gain can be set for 1, 2, 5 or 10. An input equivalent circuit is shown schematically in Figure 2–5, at the top of the next page.

The Model 6215 can accommodate bipolar input signals in the range of + 10 V_{DC} to – 10 V_{DC} (i. e., 20 $V_{P–P}$). The AD7722's input voltage range is ± 1.25 V_{DC} (2.5 $V_{P–P}$). The input amplifier is protected from signal excursions of ± 40 V.

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2.4 Analog Input Connector (continued)

2.4.1 Analog Input Circuit Description (continued)

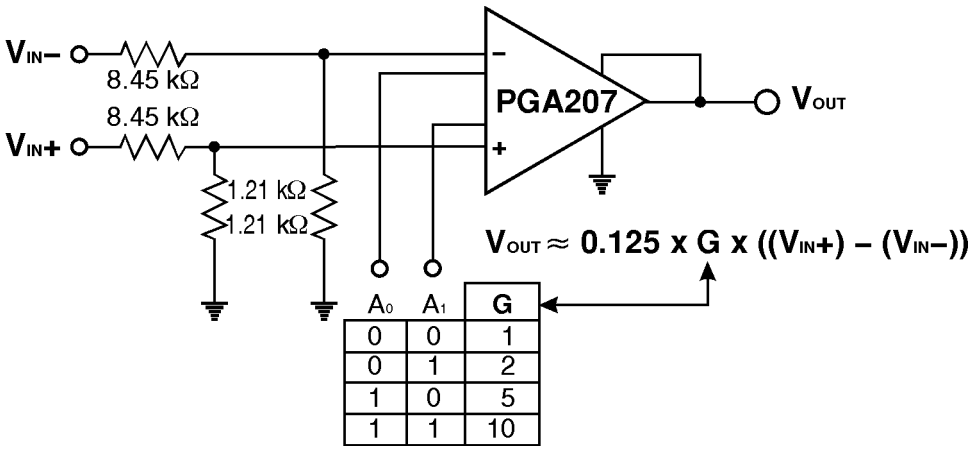


Figure 2-5: Model 6215 –Analog Input Circuit

2.4.2 Mark Signal

The MARK input (pin 18 on the analog input connector) is really a digital input signal, as opposed to all other signal lines on this connector, which accept analog voltages. The device that receives this signal recognizes voltages in excess of + 2.8 V as a logic high, and voltages below + 1.2 V as a logic low. The signal applied here is available as an LVDS output on the DIST / SYNC connector (see Section 2.5), and also as a TTL–level output to the VIM motherboard as VIM_FD4 on the Bi–FIFO interface.

Note that this signal has **NO EFFECT** on the operation of the Model 6215's A/D converters.

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2.5 Dist/Sync Connector (DIST/SYNC)

The 8–pin Distribution/Sync Connector on the Model 6215's front panel provides I/O for 3 low–voltage differential signal (LVDS) pairs. LVDS logic is based on differential voltage swings of approximately 350 mV, allowing for very fast switching times. The differential nature of these signals also provides inherent immunity to noise pickup, as such noise is seen as common mode and the receiving devices react only to the difference between the two signal lines.

This connector implements a system by which multiple 6215 boards can be made to operate synchronously. The two critical signals involved in synchronizing multiple boards are the Clock signal and the Reset (or Sync) signal. By simultaneously releasing the reset on a given group of channels, all of which are clocked from the same source, we can guarantee that these channels are all synchronized to, and phase coherent with, one another. A/D channels on a given 6215 module can be enabled to respond to an internally generated Sync signals on a paired–channel basis. To synchronize channels across multiple 6215 boards, one module (designated as the master) can drive his reference clock and internal Sync signal onto this connector (see Section 3.11.7), and other units (slaves) can accept these signals over a ribbon cable interface (see Section 3.13.3).

Table 2–2, below, shows the pinout for the connector. The signals that can be output to, or accepted on, these pins will be discussed in the subsections beginning at the top of the next page.

Table 2-2: Model 6215 –DIST/SYNC Connector Pinouts

Pin	Description	Pin	Description
1	SYNC	2	$\overline{\text{SYNC}}$
3	GND	4	$\overline{\text{MARK}}$
5	MARK	6	GND
7	DCLK	8	$\overline{\text{DCLK}}$

The recommended mating connector for use here is Adam Tech model number FCS–08–SG–N, a standard, crimp–on 8–pin insulation–displacement type of connector for 0.050" pitch ribbon cable. One mating connector is supplied with each Model 6215 (Pentek's part # for this connector is 353.00802). The assembled cable should be at least 8" in length. An assembled cable for connecting the sync connectors on two Model 6215's is available from Pentek as Model #2127. If your application requires that channels on more than two 6215s be synchronized, please contact our Technical Support Group at (201) 818–5900.

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2.5 Dist/Sync Connector (continued)

2.5.1 SYNC, $\overline{\text{SYNC}}$

The Sync signal serves as a synchronous reset for all of the A/D converters that are appropriately enabled. The Sync signal may either be generated internally or accepted from another 6215 via this interface. A 6215 designated as the Dist/Sync master can drive the Sync signal he generates onto this interface (see Sections 3.11.7) as a differential LVDS pair. A/D Channels on Dist/Sync Slave units can be enabled to respond to, or disabled from responding to, the distributed Sync signal on a channel−pair basis (Section 3.13.3).

2.5.2 MARK, $\overline{\text{MARK}}$

This signal is not related to, or involved in, the channel Synchronization process. This is an LVDS I/O pair, which will follow the TTL−level MARK input (pin 18 on the Analog Input Connector) on the unit configured as master of the Dist/Sync bus (see Section 3.11.7). Also, if you are reading data out of the 6215 in parallel mode via the VIM motherboard's Bi−FIFO interface, while the MARK input on the master is high, the D4 bit in the output data streams of the master and all connected slaves will be set to the logic '1' state. Once again, this signal has no effect on the operation of the A/D converters or synchronization. Its application is completely user defined.

2.5.3 DCLK, $\overline{\text{DCLK}}$

This Distributed Clock is an LVDS representation of the signal selected as the clock reference source (i. e., either the on−board crystal oscillator or the front−panel **EXT CLK** connector) on the unit configured as master of the Dist/Sync bus (see Section 3.11.7). On all units set up as slaves, this signal will replace the on−board crystal oscillator or the front−panel **EXT CLK** connector as the reference signal, which is divided by the Sample Clock divider to produce each unit's sample clock signal. This is an LVDS output on the master, and an LVDS input on all slaves.

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2.6 External Clock Input (EXT CLK)

The threaded, coaxial SMA connector nearest the bottom of the Model 6215's front panel is provided for the application of an external clock signal. This signal can be used as the reference signal used to derive the sample clock signal for the 6215's A/D converters.

The External Clock Input circuit used on Pentek's Model 6215 is designed to accept a wide range of input voltages, from ± 100 mV to ± 5 V AC/DC. The impedance presented by the external clock input is 50 Ω. The applied signal is AC coupled via 0.1 µF to the + input of an LVDS line receiver. This input is diode–protected to ground and +5 V, and biased at +2.5 V (the – input of the receiver is also biased at +2.5 V). Figure 2–6, below, shows the equivalent circuit for the Model 6215's **EXT CLK** input.

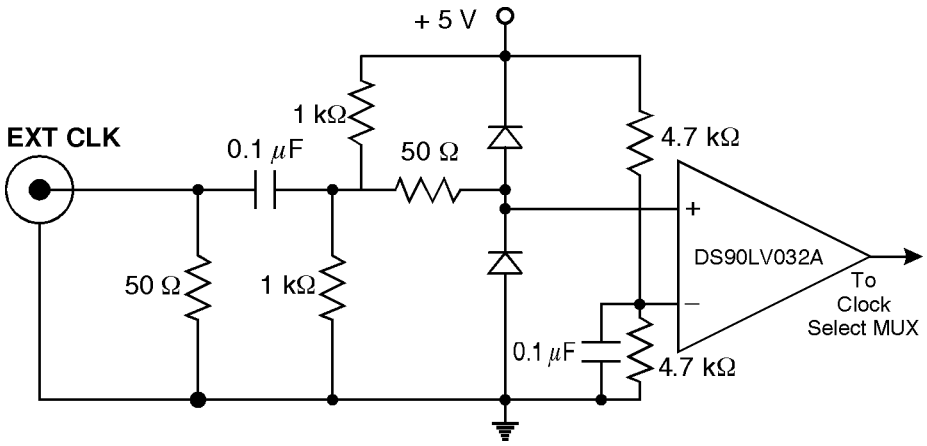


Figure 2-6: Model 6215 –External Clock Input Circuit

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2.7 LED Indicators

A total of ten LED's are visible through the front panel of the Model 6215. Two of these are associated with the 6215's Distribution / Sync Bus interface. These are located at the lower right side of the panel. The other eight are general purpose indicators controlled by the processors on the VIM motherboard, and are visible through the cutouts at the left side of the 6215's front panel. These will all be discussed in the subsections that begin below.

2.7.1 Distribution / Sync Bus Master LED – MAS

The red **MAS** LED, the left–most at the bottom right of the panel, indicates that the Distribution / Sync Bus master function has been enabled for the 6215 in question. This means that the 6215 on whose panel this LED is lit will be the one that provides the distributed Sync and reference clock signals to all other VIM modules connected to the Distribution / Sync Bus. Any Distribution / Sync Bus MUST have **one and only one** master, and it should physically be located at the opposite end of the Distribution / Sync Cable from the Distribution / Sync Bus Terminator (see Section 2.7.2, below). This LED will be illuminated whenever the D0 bit in the 6215's Board Control Register (see Section 3.11.7) is set to the logic '1' state. It will be turned off when that bit is cleared to the logic '0' state.

2.7.2 Distribution / Sync Bus Terminator LED – TRM

The red **TRM** LED, the right–most one at the bottom right of the panel, indicates that the Distribution / Sync Bus Termination function has been enabled for the 6215 in question. This means that the 6215 on whose panel this LED is lit will be the one that provides the terminating resistors for the distributed Sync and reference clock signals generated by the Distribution / Sync Bus master. Any Distribution / Sync Bus MUST have **one and only one** terminator, and it should physically be located at the opposite end of the Distribution / Sync Cable from the Distribution / Sync master (see Section 2.7.1, above). This LED will be illuminated whenever the D1 bit in the 6215's Board Control Register (see Section 3.11.6) is set to the logic '1' state. It will be turned off when that bit is cleared to the logic '0' state.

2.7.3 Motherboard LEDs – 0, 1, 2 & 3

Visible through cutouts at the left side of the Model 6215's front panel are two groups of four LEDs controlled by the processors on the VIM motherboard. Each group of four LEDs contains one red LED (labeled **0**) and 3 green LEDs (labeled **1**, **2** & **3**), and they are under the control of one of the motherboard's processors. Depending upon the position in which the VIM module is installed on the motherboard, the four LEDs nearest the top of the panel are controlled by either Processor A or Processor C, and the four at the bottom are controlled by either Processor B or Processor D. For further details about these indicators, please refer to your VIM motherboard's Operating Manual.

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2.8 Removing a VIM Module from a VIM Motherboard

Use these steps if a VIM module is already installed on your VIM motherboard in the position where you want to install the Model 6215. If that VIM position is already vacant, go to Section 2.9, page 25.

Tools required for all procedures:

1) #1 Phillips screwdriver

2) flat–blade screwdriver (blade width 5/16–in. or less)

CAUTION!!

Perform all assembly steps at an anti–static workstation.

---

1) Place the VIM motherboard on an anti–static workstation, solder side up – The VIM modules should now be facing down.



Figure 2–7: VIM Module –Front Panel Screws

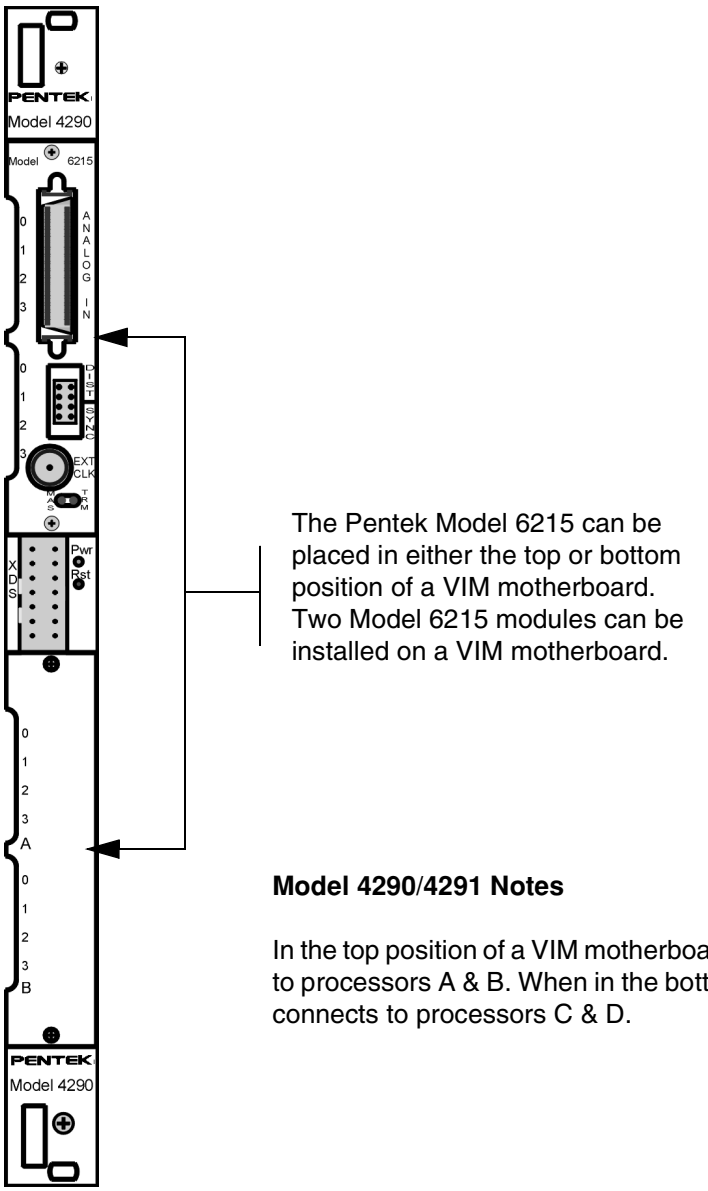
2) Remove the nylon screw at the rear of the VIM module.
The rear of the module is secured to the motherboard by a slotted nylon screw (two screws, if the module is a VIM–4) passed through the mounting hole(s) ((f) and/or (e) in Figure 2–9, on page 24) between the mezzanine connectors and threaded into a nylon spacer(s) on the mezzanine. Remove this (these) screw(s) with the flat–blade screwdriver, and set one aside to use when installing the 6215. If the module you are removing is a VIM–4, store the remaining screw with the module for use when reinstalling that module.

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2.8 Removing a VIM Module from a VIM Motherboard (continued)

3) Remove the VIM module carefully.
Turn the motherboard over, so the VIM module is on top. Gently and carefully, disengage the module's connectors from those on the motherboard. This is most easily accomplished by lifting the board at its edges, near the connector, one side at a time. This may need to be done a little bit at a time (e. g., lift first from the right, then from the left, then repeat the process until all pins are disengaged). At all times, be careful not to bend or break any of the connector pins on the mezzanine module or the motherboard.

4) Store the removed module in an anti–static bag.



The Pentek Model 6215 can be placed in either the top or bottom position of a VIM motherboard. Two Model 6215 modules can be installed on a VIM motherboard.

Model 4290/4291 Notes

In the top position of a VIM motherboard, the Model 6215 connects to processors A & B. When in the bottom position, the Model 6215 connects to processors C & D.

Figure 2-8: Model 6215 Front Panel and Mounting Configurations

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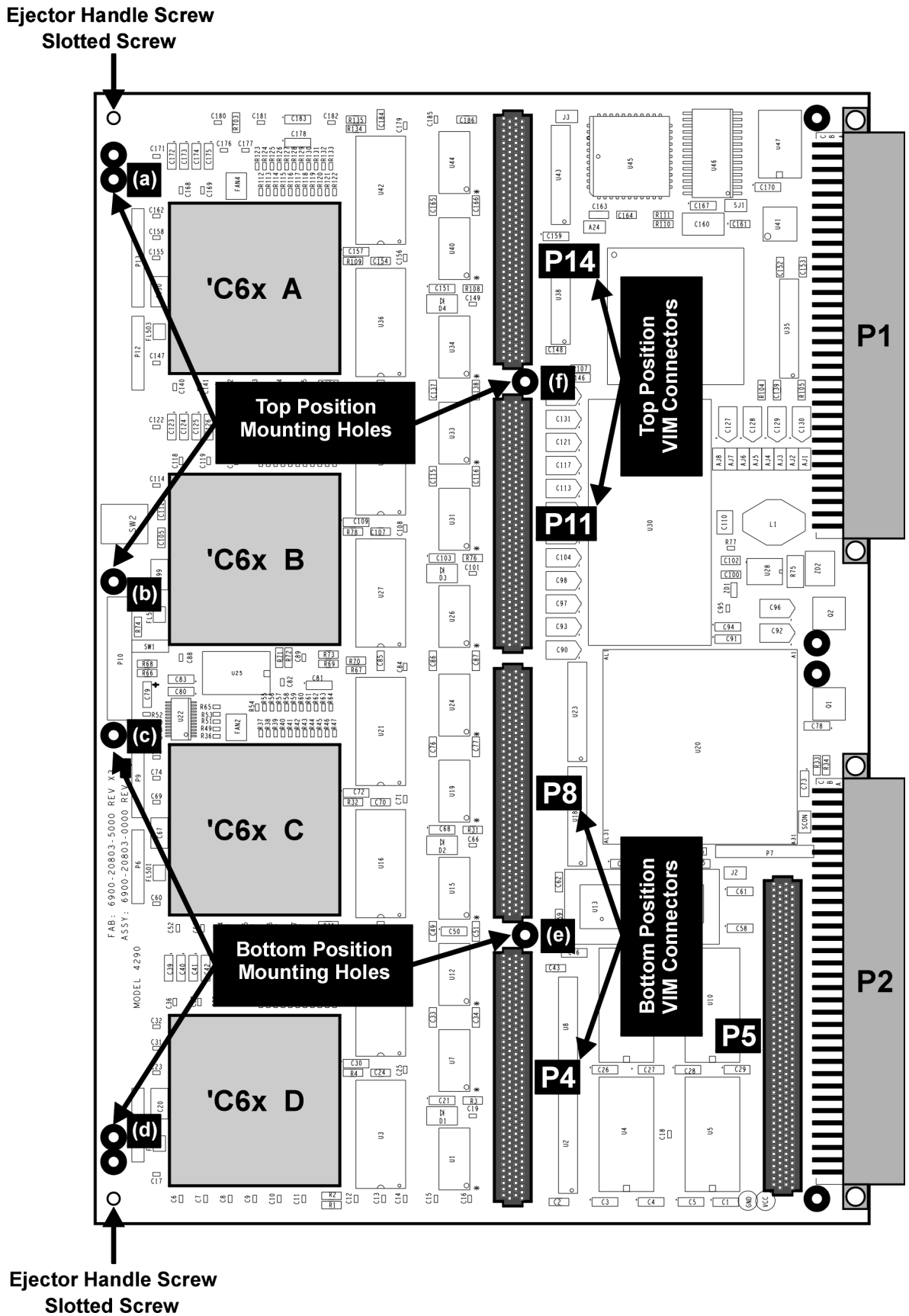


Figure 2-9: Model 4290 VIM Motherboard –Connectors & Mounting Holes

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2.9 Model 6215 Installation

The Model 6215 is a VIM–2 module which mounts on either of two adjacent mezzanine con–nectors on a VIM motherboard, such as the Model 4290 or Model 4291.

Tools required for all procedures:

1) #1 Phillips screwdriver

2) Flat–blade screwdriver (blade width 5/16–in. or less)

CAUTION!!

Perform all assembly steps at an anti–static workstation.

---

1) Remove the shipping brackets from the Model 6215. When the Model 6215 is shipped, two red shipping brackets are placed on the VIM module to hold the front panel in place, see Figure 2–10, below. The shipping brackets need to be removed. This requires the removal of four Phillips screws, two from the front panel (see Figure 2–7, page 22), and two from the bottom (non–component side) of the Model 6215.

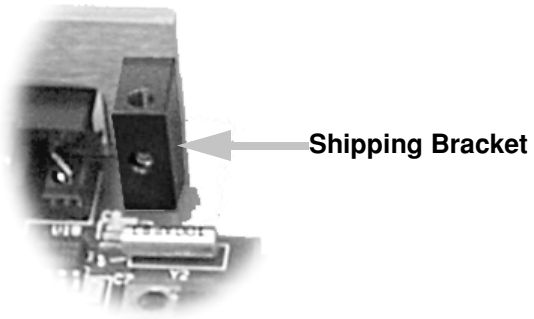


Figure 2–10: Model 6215–Shipping Brackets

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2.9 Model 6215 Installation (continued)

2) Install the nylon standoff on the Model 4290. The nylon standoff goes in the mounting hole closest to the P1 or P2 connector, see Figure 2–11, below. On the Model 4290 /4291 Motherboard diagram, Figure 2–9 on page 24, the mounting hole is labeled as **f** for the top VIM connectors, and **e** for the bottom VIM connectors. The figure below shows the nylon screw inserted into the standoff. In this case, the screw needs to be removed so the Model 6215 can be properly installed. There are two nylon screws. One screw secures the nylon standoff to the VIM motherboard, the other secures the VIM module to the standoff. At this time, only secure the standoff to the VIM motherboard.

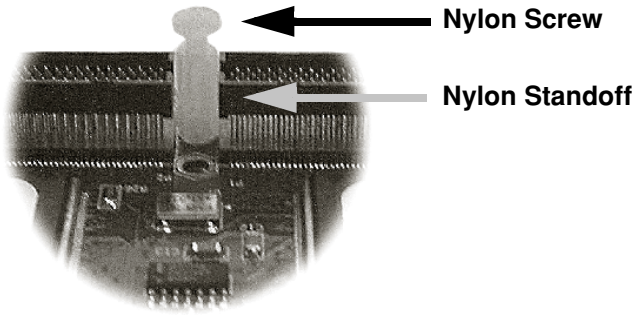


Figure 2–11: Model 6215 –Nylon Standoff Location

3) Place the Model 6215 on the VIM motherboard. Align the Model 6215 VIM connectors (P1 and P2) with the VIM connectors on the VIM motherboard. Gently press on both sides of the Model 6215 until the VIM connectors on both the VIM module and motherboard are fully seated.

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2.9 Model 6215 Installation (continued)

4) Securely fasten the Model 6215 to the VIM motherboard. There are three screws that need to be tightened. A nylon screw attaches the Model 6215 to the nylon standoff, and two 2.5mm oval Phillips–head screws attach the Model 6215 to the front brackets. Place these screws on the Model 6215 and tighten them.



Figure 2–12: Model 6215 –VIM Screw Locations (top view)

5) Install the Model 6215 front panel. The front panel uses two Phillips head screws to secure the front panel to the VIM module. Place the screws on the Model 6215 and tighten them.

This completes the module installation. The Motherboard is installed into a VME card cage to complete the installation process. Refer to the Motherboard's Operating man–ual for details.

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Chapter 3: Memory Map and Register Descriptions

3.1 Overview

This section covers access to the Model 6215 from VIM motherboards such as Pentek's Models 4290, 4291 or 4292. Memory maps to the VIM module's resources are given from the viewpoint of the VIM motherboard's processor, and details are provided describing the use of each resource.

3.2 Model 6215 Memory Map Overview

Table 3–1, below, provides a complete memory map for Pentek's Model 6215. The subsections that follow the table provide detailed information about each register. Note that each Model 6215 has **TWO** of each of the registers listed below, one for each of the potential controlling processors on the VIM Motherboard.

Table 3–1: Model 6215 Memory Map

'C6x Address	Register Name	Mnemonic	Access	Add'l Info
0x0032 zz00	ID EEPROM Readout Register	EEPROM_CTRL	R/W	Appendix C
0x0032 zz04	Overload Interrupt Enable Register	INTR_ENA	R/W	Section 3.5
0x0032 zz08	Interrupt Source Register	INTR_SRC	R/W	Section 3.6
0x0032 zz0C	Overload Status Register	OVL_STAT	R/Clr	Section 3.7
0x0032 zz10	Data Valid Register	DATA_VALID	R. O.	Section 3.8
0x0032 zz14	FIFO Channel Select Register	FIFO_CH_SEL	R/W	Section 3.9
0x0032 zz18	Sample Clock Divider, Secondary Pair #1	SEC_CH1_CLK_DIV	R/W	Section 3.10
0x0032 zz1C	Sample Clock Divider, Secondary Pair #2	SEC_CH2_CLK_DIV	R/W	Section 3.10
0x0032 zz20	Board Control Register	BOARD_CTRL	R/W	Section 3.11
0x0032 zz24	Sample Clock Divider, Primary Pair #1	PRI_CH1_CLK_DIV	R/W	Section 3.10
0x0032 zz28	Sample Clock Divider, Primary Pair #2	PRI_CH2_CLK_DIV	R/W	Section 3.10
0x0032 zz2C	Input Amp Gain Control, Primary Pairs #1 & #2	PRI_GAIN_CTRL	R/W	Section 3.12
0x0032 zz30	Input Amp Gain Control, Secondary Pairs #1 & #2	SEC_GAIN_CTRL	R/W	Section 3.12
0x0032 zz34	A/D Synchronization & Calibration Register	SYNC_CAL	R/W	Section 3.13
0x0032 zz38	Distributed Clock & External Sync Enable Register	DIST_CLK_EXT_SYNC_ENA	R/W	Section 3.14
0x0032 zz3C	Serial Port Control Register	SER_CTRL	R/W	Section 3.15

NOTE: The zz values in the 'C6x address are treated as rollover values and are not used in decoding resource addresses. (e. g., addresses 0x0032 0000 and 0x0032 FF00 point to the identical location on any given Model 6215).

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3.3 A/D Converter Channel Identification

Each of the eight A/D converters on the Model 6215 can be controlled by either of the two processors on the VIM motherboard that have access to the board. Each VIM processor's view of the Model 6215 includes four "primary" A/D converters, and four "secondary" A/D converters. Also, certain programmable functions on the Model 6215 are applied to two channels simultaneously (i. e., to a channel pair), and for these functions, we will refer to primary and secondary pairs. Which A/Ds are primary and which are secondary depends upon which processor happens to be conducting the access.

For VIM Processor A and/or VIM Processor C, A/D converter #1 (i. e., U14 on the 6215 Board) is Primary ADC 1, and A/D Converter #2 (U15) is Primary ADC 2. For paired functions, ADCs 1 and 2 are Primary Pair 1 for Processors A & C. To these processors, A/D #3 (U22) is Primary ADC 3 and A/D converter #4 (U23) is Primary ADC 4. For paired functions, ADCs 3 and 4 are recognized by Processors A & C as Primary Pair 2. For Processors A & C, A/D converter #5 (U30) is Secondary ADC 1, A/D Converter #6 (U31) is Secondary ADC 2, and those processors see these 2 A/Ds as Secondary Pair 1. Finally, to VIM Processors A & C, A/D Converter #7 (U38) is Secondary ADC 3, A/D Converter #8 (U39) is Secondary ADC4 and for paired functions, ADCs 7 & 8 are Secondary Pair 2.

For VIM Processor B and/or VIM Processor D, A/D converter #5 (i. e., U30 on the 6215 Board) is Primary ADC 1, and A/D Converter #6 (U31) is Primary ADC 2. For paired functions, ADCs 5 and 6 are Primary Pair 1 for Processors B & D. To these processors, A/D #7 (U38) is Primary ADC 3 and A/D converter #8 (U39) is Primary ADC 4. For paired functions, ADCs 7 and 8 are recognized by Processors B & D as Primary Pair 2. For Processors B & D, A/D converter #1 (U14) is Secondary ADC 1, A/D Converter #2 (U15) is Secondary ADC 2, and those processors see these 2 A/Ds as Secondary Pair 1. Finally, to VIM Processors B & D, A/D Converter #3 (U22) is Secondary ADC 3, A/D Converter #4 (U23) is Secondary ADC4 and for paired functions, ADCs 3 & 4 are Secondary Pair 2.

The above information is summarized in Table 3–2, below.

Table 3–2: Model 6215 –A/D Identification by VIM Processors

A/D Chan	PCB U #	as seen by Processor A or C		as seen by Processor B or D	
		Separately	Paired	Separately	Paired
1	14	Primary 1 (P1)	Primary Pair 1 (PP1)	Secondary 1 (S1)	Secondary Pair 1 (SP1)
2	15	Primary 2 (P2)		Secondary 2 (S2)	
3	22	Primary 3 (P3)	Primary Pair 2 (PP2)	Secondary 3 (S3)	Secondary Pair 2 (SP2)
4	23	Primary 4 (P4)		Secondary 4 (S4)	
5	30	Secondary 1 (S1)	Secondary Pair 1 (SP1)	Primary 1 (P1)	Primary Pair 1 (PP1)
6	31	Secondary 2 (S2)		Primary 2 (P2)	
7	38	Secondary 3 (S3)	Secondary Pair 2 (SP2)	Primary 3 (P3)	Primary Pair 2 (PP2)
8	39	Secondary 4 (S4)		Primary 4 (P4)	

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3.4 Configuration EEPROM Readout Register – R/W @ 'C6x Address 0x0032 zz00

The format for the code stored by Pentek in this EEPROM is listed in Appendix C of this manual. The format is provided for VIM module designers. Neither the format nor this register are intended for general use.

3.5 Overload Interrupt Enable Register– R/W @ 'C6x Address 0x0032 zz04

The Model 6215's Overload Interrupt Enable Register contains one bit per A/D channel that is used to enable or disable the generation of an interrupt for that channel when the A/D Converter detects that an overload condition at its output. This condition is indicated by a the AD7722's DVALID output transitioning to the logic '0' state in the absence of a reset, Sync or calibration condition. Setting the bit associated with a given A/D channel to the logic '1' state enables the generation of an interrupt to the controlling processor on the VIM motherboard. When a bit in this register is cleared to the logic '0' state, the VIM processor will not be interrupted by overload conditions in the associated channel. Table 3–3, below, tells which bit is associated with which A/D channel.

Table 3-3: Model 6215 – Overload Interrupt Enable Register – R/W @ 'C6x Address 0x0032 zz04

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	S4_OVL_INT_EN	S3_OVL_INT_EN	S2_OVL_INT_EN	S1_OVL_INT_EN	P4_OVL_INT_EN	P3_OVL_INT_EN	P2_OVL_INT_EN	P1_OVL_INT_EN
Function	1 = Overload Interrupt Enabled 0 = Overload Interrupt Disabled							

NOTE: Please refer to Table 3-2 for channel identification as a function of Processor ID. All bits default to the logic '0' state at power-up and resets.

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3.6 Interrupt Source Register – RW @ 'C6x Address 0x0032 zz08

The Interrupt Source Register contains both an interrupt enable bit and a status bit for the occurrence of an External Sync signal. It also has an Overload status bit. When a processor on the VIM motherboard has been interrupted by the 6215, this is the first place it should look to find out why. If the interrupt was caused by an overload (i. e., if the D0 bit in this register reads back in the logic '1' state), the Overload Status Register (see Section 3.7) should then be read to determine which channel was overloaded. Table 3–4, below, shows the bitwise structure of this register. The subsections that begin below the table describe how these bits are used.

Table 3-4: Model 6215 - Interrupt Source Register - R/W @ 'C6x Address 0x0032 zz08

Bit #	D31 – D3		
Bit Name	Reserved – Not Used		
Function	Write with '0's - Mask when Reading		
Bit #	D2	D1*	D0†
Bit Name	EXT_SYNC_INT_EN	EXT_SYNC_STAT	OVL_STATUS
Bit Function	1 = Enable Interrupt on Ext. Sync 0 = Disable Interrupt on Ext. Sync	1 = An External Sync has occurred 0 = No External Syncs have occurred	1 =An Overload has occurred 0 = No Overloads have occurred

All bits default to the logic '0' state at power-up and resets.
* - This bit is Read / Clear † –This bit is Read-Only

3.6.1 External Sync Interrupt Enable – Bit D2

When this bit is set to the logic '1' state, the controlling processor on the VIM motherboard will receive an interrupt when an external Sync event occurs. The term "external Sync" is used here to refer to any synchronizing pulse delivered to the device in question via the Distribution / Sync bus. If you do not want an external Sync to cause an interrupt to the VIM motherboard's processor, clear this bit to the logic '0' state.

3.6.2 External Sync Status – Bit D1

This bit indicates the status of external Sync events. The term "external Sync" is used here, as above, to refer to any synchronizing pulse delivered to the device in question via the Distribution / Sync bus. When an external Sync pulse is applied to the Model 6215, this bit latches the event by transitioning to the logic '1' state. If the D2 bit in this register is set to the logic '1' state, this event will also cause an interrupt to the processor on the VIM motherboard (see Section 3.6.1, above). If an interrupt is not desired, this bit may be polled to determine whether a Sync has happened.

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3.6 Interrupt Source Register (continued)

3.6.2 External Sync Status (continued)

After this bit has been set to the logic '1' state, by latching a Sync event, it must be cleared back to logic '0' before it can detect subsequent Syncs. That function requires two write operations to this bit. To clear this bit, first write a '1' to it, and then write a '0'.

NOTES:

1) If the external Sync inputs are not driven, the output of the LVDS receiver that these lines are connected to is forced to a high logic state. Prior to an actual synchrinizing event, this bit simply follows the logic level present at that output. Thus, if the Sync inputs are not driven, this bit will ALWAYS read back in the logic '1' state.

2) When this bit reads back in the logic '0' state, writing a '1' to it has no effect.

3.6.3 Overload Status – Bit D0

This normally–low, read–only bit will be set to the logic '1' state whenever the voltage level at the input of any enabled A/D converter on the Model 6215 would cause an overflow at the A/D's output. If the bit in the Overload Interrupt Enable Register (see Section 3.5) corresponding to the overloaded channel has been set to the logic '1' state, then this event will generate an interrupt to the processor on the VIM motherboard. If you do not want an interrupt in response to an overload, this bit may be polled to determine if such an event has occurred.

Whether or not an interrupt was generated, the occurrence of an overload will be latched by this bit. In order to detect subsequent overloads, this bit must be cleared to the logic '0' state. You accomplish this by performing two write operations (first with a '1', then with a '0') to the bit in the Overload Status Register (see Section 3.7, at the top of the next page) that corresponds to the channel in which the overload occurred. That action will clear both this bit and the bit you manipulated in the Overload Status Register.

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3.7 Overload Status Register – R/C @ 'C6x Address 0x0032 zz0C

This 8–bit register has one bit associated with each A/D converter on the Model 6215, used to latch an overload condition on that channel. A '1' in any bit in this register indicates that an overload occurred in the associated channel. Note that when any bit in this register is set, the Overload Status bit (D0, see Section 3.6.3, on the previous page) in the Interrupt Source Register (see Section 3.6) will also be set to the logic '1' state. An interrupt to the processor on the VIM motherboard can be generated in response to an overload in a given channel by setting the associated bit in the Overload Interrupt Enable Register (see Section 3.5) to the logic '1' state. Table 3–5, below, tells which bit in this register is associated with which A/D channel.

Since these bits latch in response to an overload, in order to detect subsequent overloads in a given channel, the associated bit in this register must be cleared. To clear any bit in this register that is set to the logic '1' state, you must write to that bit twice, first with a '1', then with a '0'. This action will clear both the bit you manipulated in this register and (assuming that no other bits in this register have been set in the interim) the Overload Status bit in the Interrupt Source Register.

Table 3-5: Model 6215 – Overload Status Register – Read/Clear @ 'C6x Address 0x0032 zz0C

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	S4_OVL	S3_OVL	S2_OVL	S1_OVL	P4_OVL	P3_OVL	P2_OVL	P1_OVL
Function	1 = An Overload Occurred in this Channel 0 = An Overload Did Not Occur in this Channel							

NOTE: Please refer to Table 3-2 for channel identification as a function of Processor ID. All bits default to the logic '0' state at power-up and resets.

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3.8 Data Valid Register – R. O. @ 'C6x Address 0x0032 zz10

This register contains one Read–Only bit associated with each of the eight A/D converters on the Model 6215, used to reflect the state of the associated A/D's DVAL output. The A/D converter sets its data–valid bit high after the first conversion cycle. The data–valid bit will remain high as long as an overload, reset, calibration or Sync condition does not exist. The data–valid bit is also used to drive the Overload Interrupt state machine. When the data–valid goes high, the Overload Interrupt state machine is placed in its Armed State. If the data–valid bit goes low, except in response to a reset, calibration or Sync event, the Overload Interrupt state machine will enter its Interrupt State. Table 3–6, below, tells which bit in this register is associated with which A/D channel.

Table 3–6: Model 6215 - Data Valid Register - R. O. @ 'C6x Address 0x0032 zz10

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DV_S4	DV_S3	DV_S2	DV_S1	DV_P4	DV_P3	DV_P2	DV_P1
Function	1 = A/D Output Data is Valid 0 = A/D Output Data is Not Valid							

NOTE: Please refer to Table 3-2 for channel identification as a function of Processor ID.
All bits default to the logic '0' state at power-up and resets.

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3.9 FIFO Channel Select Register – R/W @ 'C6x Address 0x0032 zz14

This register contains one bit associated with each of the eight A/D converters on the Model 6215, used to allow that channel to send its output data to the VIM Bi–FIFO for parallel–mode readout by the motherboard's processor. Parallel readout mode is enabled when the D4 bit (Readout_Mode, see Section 3.11.3) in the Board Control Register (see Section 3.11) is set to the logic '1' state. To enable any particular A/D channel for parallel output mode, set the associated bit in this register to the logic '1' state. Each bit in this register is an enable for the FIFO control state machine. The state machine cycles through all eight channels, and if the bit for that channel is set, a FIFO write enable pulse is generated and that A/D's data is written to the FIFO. Before attempting to read any data in parallel mode, the BIFO_Reset bit (D3 in the Board Control Register, see Section 3.11.4) should be toggled, to initialize the Bi–FIFO controller state machine. Table 3–7, below, tells which bit in this register is associated with which A/D channel.

Table 3–7: Model 6215 - FIFO Channel Select Register - R/W @ 'C6x Address 0x0032 zz14

Bit #	**D31 – D8**							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	S4_FIFO _Enable	S3_FIFO _Enable	S2_FIFO _Enable	S1_FIFO _Enable	P4_FIFO _Enable	P3_FIFO _Enable	P2_FIFO _Enable	P1_FIFO _Enable
Function	1 = Channel is Enabled to send Output Data to VIM Bi-FIFO 0 = Channel will NOT send Output Data to VIM Bi-FIFO							
NOTE: Please refer to Table 3-2 for channel identification as a function of Processor ID. All bits default to the logic '0' state at power-up and resets.								

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3.10 Sample Clock Divider Registers

The A/D converters on the Model 6215 are arranged in pairs. The two A/D converters in a given pair share a common clock signal. Thus, there are four different A/D sample clock signals. These sample clock signals are derived by division of a common reference clock signal. Each of the four A/D clocks can be set for a different divisor. The desired frequency is calculated by the equation:

$$f_S = \frac{f_{REF}}{128\ (N+1)}$$

where: f_S is the desired Sample Frequency for the channel pair;
f_{REF} is the Reference Frequency;
and N is the value written to that channel pair's Clock Divider Register

The reference clock source can be either the on−board Crystal Oscillator, or an external signal applied to either the SMA or **DIST/SYNC** connectors on the unit's front panel. Bits are provided in the Distribution Clock & Sync Enable Register (see Section 3.14) to select the LVDS clock signal on the **DIST/SYNC** connector on a per−channel−pair basis, and a single bit is provided in the Board Control Register (see Section 3.11) to globally select the signal applied to the SMA connector.

Note that the Output Sample Rate of the AD7722 ADC is specified as 4.6875 kHz minimum to 234.375 kHz maximum (these figures were arrived at by dividing the minimum and maximum Sample Clock input rates (300 kHz and 15 MHz, respectively) by the device's oversampling factor of 64). This places some restrictions on the value if N, over and above the factor of 256 limit imposed by the 8−bits that the divider register contains. To remain within these limits with the standard, 30 MHz internal crystal oscillator, the allowable range of values for N is from 0 to 49, inclusive (i. e., $0 \leq N \leq 49$). These limit values cover the full range of sampling frequencies available from this A/D. For units equipped with Option 010, the internal crystal oscillator's frequency is 30.72 MHz. For this option, the limits on the value of N are from 1 to 50, inclusive (i. e., $1 \leq N \leq 50$). This allows for sample rates from 4.706 kHz to 120 kHz, and also allows the device to be precisely programmed for an 8 kHz sample rate (N = 29). Units equipped with Option 011 have a 25 MHz internal crystal oscillator. With that crystal, frequencies from 4.7637 kHz to 195.3125 kHz can be obtained, and the range of allowable values for N is $0 \leq N \leq 40$. When using an external clock signal, limit the values of N so as not to exceed the minimum and maximum sample rates of the A/D converters.

Table 3−8, at the top of the next page, illustrates the contents of the four Sample Clock Divider Registers, and Table 3−9, also on next page, gives the sample rates that will be obtained with various values of N for all 3 internal oscillator options, rounded to 3 decimal places.

The addresses for the four Sample Clock Divider Registers are:

Primary Pair #1 – R/W @ 'C6x Address 0x0032 zz24
Primary Pair #2– R/W @ 'C6x Address 0x0032 zz28
Secondary Pair #1 – R/W @ 'C6x Address 0x0032 zz18
Secondary Pair #2 – R/W @ 'C6x Address 0x0032 zz1C

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3.10 Sample Clock Divider Registers (continued)

Table 3-8: Model 6215 –Sample Clock Divider Registers								
Bit #	**D31 – D8**							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DIV7 (MSB)	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0 (LSB)
Function	This 8-bit field stores the value 'N', used in calculating the Sample Rate for an A/D pair (see the equation at the top of page 37).							
All bits default to the logic '0' state at power-up and resets.								

Table 3-9: Model 6215 –Sample Clock Dividers –Sample Frequencies with Internal Oscillators												
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**N**	**Divider**	**Standard (30 MHz)**	**Option 010 (30.72 MHz)**	**Option 011 (25 MHz)**
0	0	0	0	0	0	0	0	0	128	234.375 kHz	N/A	195.313 kHz
0	0	0	0	0	0	0	1	1	256	117.188 kHz	120 kHz	97.656 kHz
0	0	0	0	0	0	1	0	2	384	78.125 kHz	80 kHz	65.104 kHz
0	0	0	0	0	0	1	1	3	512	58.594 kHz	60 kHz	48.828 kHz
0	0	0	0	0	1	0	0	4	640	46.875 kHz	48 kHz	39.063 kHz
0	0	0	0	0	1	0	1	5	768	39.063 kHz	40 kHz	32.552 kHz
0	0	0	0	0	1	1	0	6	896	33.482 kHz	34.286 kHz	27.902 kHz
0	0	0	0	0	1	1	1	7	1,024	29.297 kHz	30 kHz	24.414 kHz
0	0	0	0	1	0	0	0	8	1,152	26.042 kHz	26.667 kHz	21.701 kHz
0	0	0	0	1	0	0	1	9	1280	23.438 kHz	24 kHz	19.531 kHz
0	0	0	0	1	0	1	0	10	1408	21.307 kHz	21.818 kHz	17.756 kHz
0	0	0	0	1	1	0	0	12	1664	18.209 kHz	18.462 kHz	15.024 kHz
0	0	0	0	1	1	1	0	14	1920	15.625 kHz	16 kHz	13.021 kHz
0	0	0	1	0	0	0	0	16	2176	13.787 kHz	14.118 kHz	11.489 kHz
0	0	0	1	0	0	1	0	18	2342	12.336 kHz	12.632 kHz	10.279 kHz
0	0	0	1	0	1	0	0	20	2688	11.161 kHz	11.429 kHz	9.301 kHz
0	0	0	1	0	1	1	0	22	2944	10.190 kHz	10.435 kHz	8.492 kHz
0	0	0	1	1	0	0	0	24	3200	9.375 kHz	9.6 kHz	7.813 kHz
0	0	0	1	1	0	1	0	26	3456	8.681 kHz	8.889 kHz	7.234 kHz
0	0	0	1	1	1	0	0	28	3584	8.082 kHz	8.276 kHz	6.735 kHz
0	0	0	1	1	1	0	1	29	3840	7.813 kHz	8 kHz	6.510 kHz
0	0	0	1	1	1	1	0	30	3968	7.560 kHz	7.642 kHz	6.300 kHz
0	0	1	0	0	0	0	0	32	4224	7.102 kHz	7.273 kHz	5.919 kHz
0	0	1	0	0	0	1	0	34	4480	6.696 kHz	6.857 kHz	5.580 kHz
0	0	1	0	0	1	0	0	36	4736	6.334 kHz	6.486 kHz	5.279 kHz
0	0	1	0	0	1	1	0	38	4992	6.010 kHz	6.154 kHz	5.008 kHz
0	0	1	0	1	0	0	0	40	5284	5.716 kHz	5.854 kHz	4.764 kHz
0	0	1	0	1	0	1	0	42	5504	5.451 kHz	5.581 kHz	N/A
0	0	1	0	1	1	0	0	44	5760	5.208 kHz	5.333 kHz	N/A
0	0	1	0	1	1	1	0	46	6016	4.987 kHz	5.106 kHz	N/A
0	0	1	1	0	0	0	1	49	6400	4.688 kHz	4.8 kHz	N/A
0	0	1	1	0	0	1	0	50	6528	N/A	4.706 kHz	N/A

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3.11 Board Control Register – RW @ 'C6x Address 0x0032 zz20

The Model 6215's Board Control Register has 7 active bits, which provide control over the features listed here. The device can be configured as a Master or Slave on the Distribution / Sync bus, and terminating resistors can be activated on that bus for the board that will be the last slave in the chain. If the device is a Master, either the **EXT CLK** SMA connector or the on–board crystal oscillator can be selected as the distributed clock signal and the frequency reference for the Sample Clock Dividers (see Section 3.10). Serial or Parallel output mode may be selected, and a reset bit for the FIFO state machine used in parallel mode is also provided. A bit is provided that a VIM processor can set to claim control of all 8 A/D channels, and a read–only bit is provided to notify a VIM processor that the other VIM processor has claimed control of all 8 A/D channels. Table 3–10, below, summarizes the contents of the Model 6215's Board Control Register. The subsections that begin below the table give detailed descriptions of how these bits are used.

Table 3–10: Model 6215 - Board Control Register - R/W @ 'C6x Address 0x0032 zz20

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6***	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved-Not Used	Other_Proc_is_Master	Master_All_Chans	Readout_Mode	BIFO_Reset	Ext_Clk_Enable	S/D_Term_Enable	S/D_Master_Enable
Bit Function	Write '0' Mask on Reads	1 = True 0 = False	1 = Master 0 = Not Master	1 = Parallel 0 = Serial	1 = Reset 0 = Release	1 = Enable 0 = Disable	1 = Term 0 = No Term	1 = Master 0 = Slave

* - This bit is Read-Only. All bits default to '0' on power-up and reset.

3.11.1 Other Processor is Master of All A/D Channels – D6

When this bit reads back in the logic '1' state, it indicates to the VIM processor reading the register that the **OTHER** VIM processor with access to this module has claimed mastership of all 8 A/D channels. While this bit is set, the processor that reads it has full access to all of its resources, but **none of the configuration changes the processor may make will take effect until the OTHER processor releases its control of the board** (see Section 3.11.2, on the next page). The processor that is not the master can also still read data from the module, via the Bi–FIFO.

If this bit reads back as a '0', then the other VIM processor has not claimed total board control, and the processor conducting the access can claim such mastership, change individual channel settings, etc. This bit is Read Only (the only such bit in this register), and will follow the state of the D5 bit (Master_All_Chans, see Section 3.11.2) in the other VIM processor's version of this register.

Specifically, when a processor reads this bit back in the logic '1' state, the outputs of the following eight registers in that processor's memory map are, in effect, tri–stated: all four Sample Clock Divider registers, both Input Amplifier Gain Control registers, the A/D Sync and Cal register and the Distribution Clock and Sync Enable register.

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3.11 Board Control Register (continued)

3.11.2 Master All A/D Channels – D5

A processor on the VIM motherboard sets this bit to the logic '1' state to claim mastership of all 8 A/D channels on the Model 6215 VIM Module. When a processor sets this bit, the D6 bit in the other processor's Board Control Register (Other_Master, see Section 3.11.1, on the previous page) is also set, to tell the other processor that this one has taken control of the board. This bit is intended for use in parallel readout mode (see Section 3.11.3). The usefulness of this feature in Serial readout mode is somewhat dubious, as it makes little sense for a processor to claim control over eight channels when he can only read data from four of them.

A processor that sets this bit does not prevent the other processor from making accesses to the board. The other processor can access every resource in its memory map in the usual manner, but none of the configuration changes it may make will take effect until this processor releases its mastership by clearing this bit to the logic '0' state.

Specifically, when one processor sets this bit, the outputs of the following eight registers in the OTHER processor's memory map are, in effect, tri-stated: all four Sample Clock Divider registers, both Input Amplifier Gain Control registers, the A/D Sync and Cal register and the Distribution Clock and Sync Enable register.

When this bit is cleared to the logic '0' state, the processor in whose register it resides does not have exclusive master access to the board, and each processor can access all its usual resources.

NOTE: An interesting situation will occur if BOTH processors set this bit at the same time. This is **VERY BAD FORM**, since when one processor sets this bit, the other has a status bit that tells him so, and (if he's polite) the other should not set his own until the first clears his. There is, however, no mechanism in the hardware to prevent a processor from setting his Master_All_Channels bit while the status bit is high. If a processor should be so rude as to set his Master_All_Channels bit while the other processor already has his set, each processor will retain exclusive master access to those resources that he CAN access. However, both of the processors in this contentious situation will ONLY be able to access their SECONDARY channels. We will leave it as an exercise to the user to figure out what impact this will have upon his application, and conclude this section with a recommendation that you take steps in your software to **AVOID THIS CONFLICT**.

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3.11 Board Control Register (continued)

3.11.3 Readout Mode Select – D4

This bit determines the path by which a processor on the VIM motherboard will read the data collected by the Model 6215 module. When this bit is cleared to its default logic '0' state, the processor can read output data from its primary A/D channels ONLY, via the Serial Port interface. We call this con–figuration serial readout mode.

In order to read data from the Model 6215 via the Bi–FIFO interface, the VIM motherboard processor must set this bit to the logic '1' state. In this configuration, which we refer to as parallel readout mode, any processor can read data from any A/D channel, by setting the bits corresponding to the desired channels in the FIFO Channel Select Register (see Section 3.9) to the logic '1' state.

For information about how the data that is output by the Model 6215 is for–matted, over either of these interfaces, please refer to Section 3.16.

3.11.4 VIM Bi–FIFO State Machine Reset – D3

When this bit is set to the logic '1' state, the Bi–FIFO controller state machine for the VIM processor in question will be placed and held in its reset, or initial, state. Before making any attempt to read data from the 6215 in parallel mode, you MUST reset the FIFO state machine.

This bit must be cleared to the logic '0' state to release the state machine and allow it to advance from its initial state and actually deliver data to the moth–erboard's FIFOs. Thus, the FIFO reset function should be written as a toggle, i. e., this bit should first be set to the logic '1' state (to reset the state machine), then cleared back to '0' (to release the reset).

3.11.5 External Clock Enable – D2

This bit selects the reference clock source for the Model 6215 A/D module. The reference clock is the signal that drives the Sample Clock Dividers and (if the unit is in question is the master of the Distribution / Sync Bus (see Section 3.11.7), serves as the distributed clock signal. Set this bit to the logic '1' state to select the **EXT CLK** SMA connector on the module's front panel as the reference clock signal. Clear this bit to the logic '0' state to select the on–board crystal oscillator as the reference clock signal.

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3.11 Board Control Register (continued)

3.11.6 Distribution / Sync Bus Termination Enable – D1

This bit is set to the logic '1' state to connect terminating resistors to the Model 6215's Distribution / Sync bus. If used, the Distribution / Sync bus should be arranged such that the module selected as the master (see Section 3.11.7, below) drives one end of the ribbon cable. The terminations should be enabled (i.e., this bit should be set) **ONLY** in the module at the opposite end of the ribbon cable from the master. Setting this bit will also light the TRM LED on the module's front panel. In the master module, and all other slaves, as well as for any module that does not use the Distribution / Sync bus, this bit should be cleared to the logic '0' state. In a stand alone unit, no master or slave being used, the Termination Enable bit must be set to the logic '1' state.

3.11.7 Distribution / Sync Bus Master Enable – D0

This bit should be set to the logic '1' state **ONLY** in that module that will be the master of the Distribution / Sync bus. The Distribution/ Sync master is the module that will supply the Reference Clock and Sync signals to all other units on the bus (the slaves). The master should be selected such that it drives one end of the ribbon cable that implements the bus. The module at the opposite end of the cable from the master should have the termination feature enabled (see Section 3.11.6, above). Setting this bit will also light the MAS LED on the module's front panel. This bit should be cleared to the logic '0' state on all Distribution / Sync bus slaves, as well as on any unit that does not use that bus. In a stand alone unit, no master or slave being used, the Sync Bus Master Enable bit must be set to the logic '1' state.

3.12 Operational Amplifier Control Registers – R/W @ 'C6x Addresses 0x0032 zz2C (Primary Channels) and 0x0032 zz30 (Secondary Channels)

The full scale input voltage range of the AD7722 A/D converters used on the Model 6215 is ± 1.25 V_{DC} (2.5 V_{P-P}). A resistive voltage divider on each of the 6215's Analog Inputs (see Figure 2–5, on page 17) attenuates the applied input signal by a factor of 8. Thus, to obtain maximum resolution from the A/D converter by utilizing its entire full scale input voltage range, the amplitude of the signals applied to the Model 6215's Analog Inputs should ideally be ± 10 V_{DC} (20 V_{P-P}).

Since it is not always practical to tailor the input signal's amplitude, a programmable amplifier stage is provided at the Model 6215's input, to allow lower–amplitude signals to be analyzed with maximum resolution. Two bits per channel in the Operational Amplifier Control Registers allow the input gain to be set to x1, x2, x5,or x10, to meet with the requirements of your application. Two of these registers are provided for each processor, one for the primary channels and one for the secondary channels. Tables 3–11 and 3–12, on the next page, show which bits in which register control the gain for which A/D channel, and how to set those bits for the desired gain.

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3.12 Board Control Register (continued)

Table 3–11: Model 6215 –Primary Channel Operational Amplifier Control Register – R/W @ 'C6x Address 0x0032 zz2C

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	P4_A1	P4_A0	P3_A1	P3_A0	P2_A1	P2_A0	P1_A1	P1_A0
Function	A1 = 1, A0 = 1 - Gain = 10 A1 = 1, A0 = 0 - Gain = 5				A1 = 0, A0 = 1 - Gain = 2 A1 = 0, A0 = 0 - Gain = 1			

NOTE: Please refer to Table 3-2 for channel identification as a function of Processor ID.
All bits default to the logic '0' state (i. e., all channels are programmed for a gain of 1) at power-up and resets.

Table 3–12: Model 6215 –Secondary Channel Operational Amplifier Control Register – R/W @ 'C6x Address 0x0032 zz30C

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	S4_A1	S4_A0	S3_A1	S3_A0	S2_A1	S2_A0	S1_A1	S1_A0
Function	A1 = 1, A0 = 1 : Gain = 10 A1 = 1, A0 = 0 : Gain = 5				A1 = 0, A0 = 1 : Gain = 2 A1 = 0, A0 = 0 : Gain = 1			

NOTE: Please refer to Table 3-2 for channel identification as a function of Processor ID.
All bits default to the logic '0' state at power-up and resets.

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3.13 A/D Synchronization and Calibration – R/W @ 'C6x Address 0x0032zz34

This register is used to calibrate and synchronize each of the A/D converters. Bits are provided in this register to enable channels to respond to an internally–generated Sync signal on a channel–pair basis, to generate an internal Sync pulse, to enable external Sync for all channels, and to calibrate the primary and secondary A/D channel groups. Table 3–13, below, illustrates the contents of the Model 6215's A/D Synchronization and Calibration Register. The subsections that begin below the table give detailed descriptions of how these bits function.

Table 3–13: A/D Synchronization and Calibration Register - RW @ 'C6x Address 0x0032zz34

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	SEC_ CAL	PRI_ CAL	INTERNAL _SYNC	EXT_ SYNC_EN	SP2_INT_ SYNC_EN	SP1_INT_ SYNC_EN	PP2_INT_ SYNC_EN	PP1_INT_ SYNC_EN
Function	1 = Calibrate Channels 0 = No Action		1 = Gen. Sync 0 = Release/Run	1 = Enable 0 = Disable	1 = Enable Internal Sync for Channel Pair 0 = Disable Internal Sync for Channel Pair			

NOTE: Please refer to Table 3-2 for channel pair identification as a function of Processor ID. All bits default to the logic '0' state at power-up and resets.

3.13.1 Calibrate A/D Channels – Bits D6 (Primary) and D7 (Secondary)

Setting one of these bits to the logic '1' state will initiate a calibration cycle in the associated 4–channel group. In general, a processor can always initiate a calibration cycle in its primary A/D channels by setting D6 to the logic '1' state The exception to this rule occurs when the **other** VIM processor has set its Master_All Chans bit (D5 in the Board Control Register, see Section 3.11.2). If a given processor has set its own Master_All Chans bit, then setting D7 will start a calibration cycle for that processor's secondary A/D channels.

At the start of the calibration cycle, the Data Valid bits (see Section 3.8) associ–ated with the channels being calibrated are cleared to the logic '0' state. The calibration cycle is controlled completely by logic internal to the AD7722 A/D chips, so once the user initiates the cycle, no further intervention is necessary. For complete details about the internal workings of the calibration cycle, please refer to the **Offset and Gain Calibration** section of the Analog Devices AD7722 Data Sheet, in Appendix A of this manual.

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3.13 A/D Synchronization and Calibration (continued)

3.13.1 Calibrate A/D Channels (continued)

When calibration for a given channel has reached completion, the associated Data Valid bit (again, see Section 3.8) will be set to the logic '1' state. The Calibrate function should therefore be written such that the appropriate calibrate bit is toggled (i. e., first set to the logic '1' state, then cleared to the logic '0' state) and then the Data Valid register (at 'C6x address 0x0032 zz10) is polled to determine when the cycle has completed (this should take 64 sample clock cycles). Note that calibration should be performed **BEFORE** synchronization or data taking on the Model 6215.

3.13.2 Generate an Internal Sync Signal – Bit D5

Bit D5 in the 6215's Board Control register is used to start the device's Sync state machine. After the desired Sync Enable bits in this register are set (see Sections 3.13.3, below, and 3.13.4, on the next page), set D5 to the logic '1' state to "kick off" the Sync state machine. The Sync state machine will then initialize all channels for which the enable bit was set, and wait for D5 to be reset. The internal Sync function should therefore be written as a toggle (i. e., first set bit D5 in this register to the logic '1' state, then clear it to the logic '0' state). After D5 is cleared, the state machine returns to its idle state, and the serial/parallel port controllers in the selected channels are reset, thus the channels are synchronized.

On units configured as Distribution / Sync bus masters, the signal created by toggling this bit is converted into LVDS and output as the SYNC signal on the **DIST/SYNC** connector. It then becomes an External Sync signal on the slave units to which it is delivered.

3.13.3 External Sync Enable – Bit D4

This bit must be set to the logic '1' state if ANY A/D channel on a given 6215 is t be synchronized externally. Selection of which channel pairs on the board actually respond to the External Sync is accomplished by means of the four bits in the Distributed Clock and External Sync Enable Register. For more information about those bits, please refer to Section 3.14. If all A/D channels on a given 6215 will be synchronized internally, or if synchronized operation is not necessary in your application, this bit may be left in its default logic '0' state.

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3.13 A/D Synchronization and Calibration (continued)

3.13.4 Internal Sync Enables – Bits D3 (Secondary Pair 2), D2 (Secondary Pair 1), D1 (Primary Pair 2) & D0 (Primary Pair 1)

These bits enable A/D channel pairs to respond to an internally generated Sync signal. To enable a given channel pair for internal synchronization, set the corresponding bit in this register to the logic '1' state. When one of these bits is cleared to the logic '0' state, the corresponding channel pair will not respond to an internally generated Sync signal.

Figure 3–1, below, shows how the 6 LSBs in this register and the four bits in the Distributed Clock and External Sync Enable Register (see Section 3.14, which starts on the next page) control the synchronization function on the Model 6215.

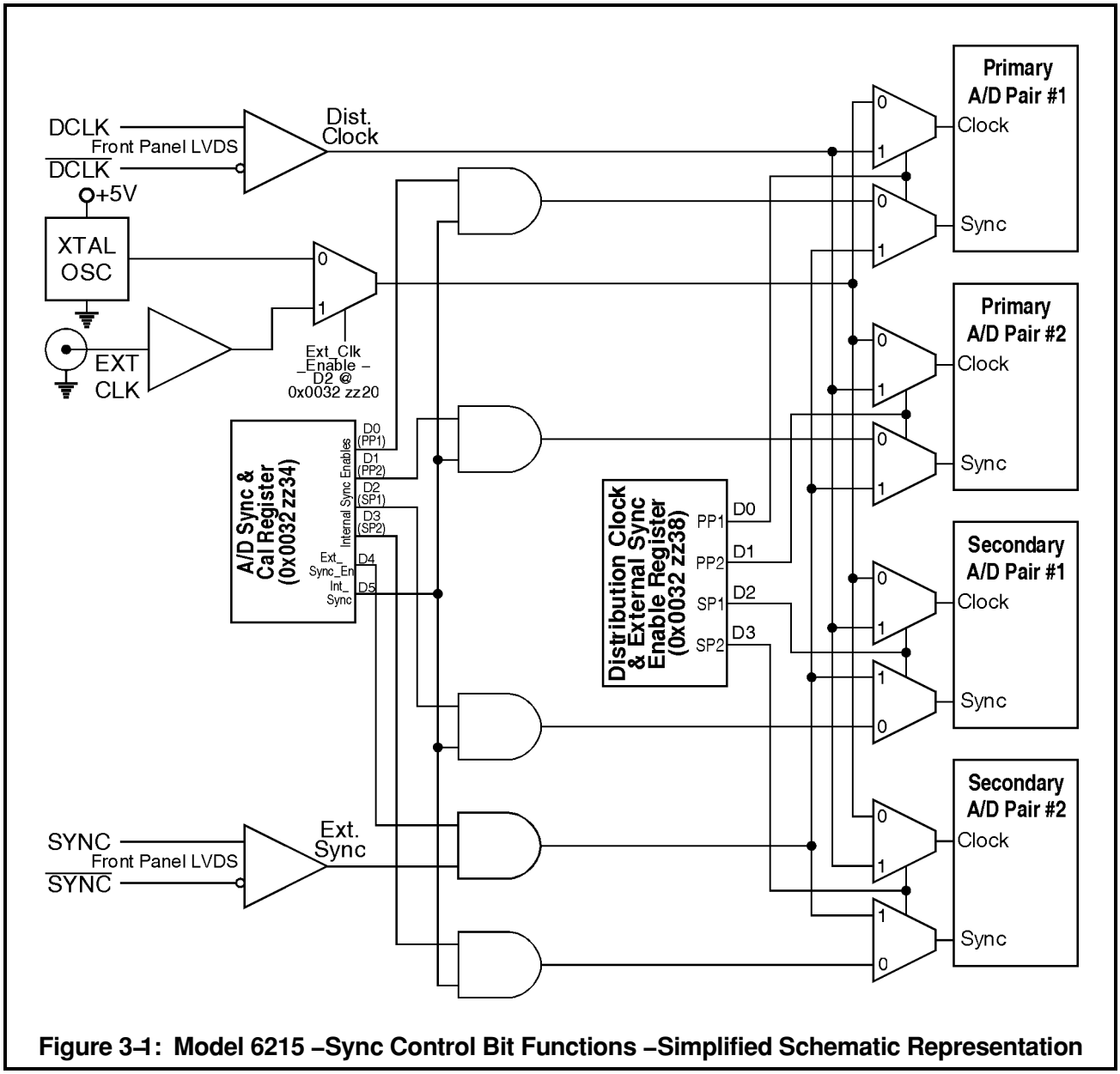


Figure 3–1: Model 6215 –Sync Control Bit Functions –Simplified Schematic Representation

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3.14 Distributed Clock and External Synchronization Enable Register – RW @ 'C6x Address 0x0032zz38

As shown in Figure 3–1, on the previous page, the Clock and Sync inputs on all four A/D pairs on the Model 6215 are each driven from the output of a multiplexer.The four active bits in this register are each connected to the select inputs on one pair of multiplexers. Each of these two muxes selects a signal delivered to the front panel's LVDS **DIST/SYNC** connector when the bit associated with that channel pair is set to the logic '1' state, or a local signal when the bit is cleared to the logic '0' state. Table 3–14, below, shows which bit is associated with which channel pair.

Table 3–14: Distributed Clock and External Sync Enable Register – R/W @ 'C6x Address 0x0032zz38

Bit #	D31 – D4			
Bit Name	Reserved – Not Used			
Function	Write with '0's - Mask when Reading			
Bit #	**D3**	**D2**	**D1**	**D0**
Bit Name	SP2_DIST_ SYNC_ENABLE	SP1_DIST_ SYNC_ENABLE	PP2_DIST_ SYNC_ENABLE	PP1_DIST_ SYNC_ENABLE
Function	1 = Enable Dist. Clk. & Ext. Sync for Channel Pair 0 = Disable Dist. Clk. & Ext. Sync for Channel Pair			

NOTE: Please refer to Table 3-2 for channel pair identification as a function of Processor ID. All bits default to the logic '0' state at power-up and resets.

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3.15 Serial Port Control Register – RW @ 'C6x Address 0x0032zz3C

The eight active bits in this register provide two control functions for the Serial Port Output features of the Model 6215. The four high–order bits (D7 – D4) are used to reset the serial interface, on a channel–pair basis. The four low–order bits (D3 – D0) are used to select either the on–board reference source (i. e., the crystal oscillator or the signal applied to the front panel **EXT CLK** SMA connector) or a clock signal provided by the VIM motherboard as the bit–rate clock for serial port readout. Table 3–15, below, shows the register's bitwise layout. The subsections that begin below the table describe how these bits are used.

Table 3–15: Serial Port Control Register- R/W @ 'C6x Address 0x0032zz3C

Bit #	D31 – D8							
Bit Name	Reserved – Not Used							
Function	Write with '0's - Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	SP2_Ser_ Port_Reset	SP1_Ser_ Port_Reset	PP2_Ser_ Port_Reset	PP1_Ser_ Port_Reset	SP2_'C6x_Ser _Clk_Enable	SP1_'C6x_Ser _Clk_Enable	PP2_'C6x_Ser _Clk_Enable	PP1_'C6x_Ser _Clk_Enable
Function	1 = Hold Serial Port in Reset 0 = Release Serial Port for Data Taking				1 = VIM MB Processor provides Serial Port Clock. 0 = 6215 provides its own Serial Port Clock			
NOTE: Please refer to Table 3-2 for channel pair identification as a function of Processor ID. All bits default to the logic '0' state at power-up and resets.								

NOTE: Although the two bit fields in this register provide controls for the serial ports associated with both the primary and secondary A/D channels, any given processor can only read data from its own primary A/D channels via the serial interface. This feature was provided for those brave individuals who wish to attempt to use the "Single Master" feature (see Section 3.11.2) in serial mode, although that readout method is **NOT RECOMMENDED**.

3.15.1 Serial Port Reset – Bits D7 (Sec. Pr. 2), D6 (Sec. Pr. 1), D5 (Pri. Pr. 2) & D4 (Pri. Pr. 1)

While any of these bits is held in the logic '1' state, the serial port interface for the associated channel pair will be held in its reset state. To release the reset and allow data transfer over a given serial port, clear the associated bit to the logic '0' state. The serial port reset function should be written as a toggle, i. e., the bit in question should first be set to the logic '1' state, to assert the reset, then cleared to the logic '0' state, to release that channel pair's port for data transfer.

3.15.2 Serial Port Clock Selection – Bits D3 (Sec. Pr. 2), D2 (Sec. Pr. 1), D1 (Pri. Pr. 2) & D0 (Pri. Pr. 1)

These four bits determine the source of the serial port clock for A/D channel pair readout on the Model 6215. When a given bit is cleared to the logic '0' state, the serial port clock for the associated channel pair is provided locally, by the module's refer–ence clock source (i. e., the on–board crystal oscillator or the front panel **EXT CLK** connector). When one of these bits is set to the logic '1' state, the serial port clock for the associated channel pair will be provided by the VIM Motherboard processor.

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3.16 Model 6215 Output Data Formats

There are two ways in which a VIM Motherboard processor can read output data from a Model 6215. The data can be read over the Serial Port interface, or it can be read over the Bi–FIFO interface. The readout mode is selected by the Readout_Mode bit (D4, see Section 3.11.3) in the Board Control Register (at 'C6x address 0x0032 zz20). This section shows how the data is formatted when read over either interface.

Table 3–16, below, illustrates the format used when the processor reads data from the Model 6215 in Serial mode. Each processor has two serial ports, and each port carries data from two A/D channels. Port 0 of Processor A (or C, depending upon which position on the motherboard the module is mounted in) reads data from A/D channels 1 and 2. Data from A/D channels 3 and 4 is sent to Port 1 of Processor A (or C). Channels 5 and 6 send their data to Port 0 of Processor B (or D, again depending upon where the module is mounted), and Port 1 of Processor B (or D) gets the data from A/D channels 6 & 7. The lower–numbered channel's data will appear in the upper 16–bits of the longword, as the table shows.

Table 3–16: Model 6215 –Serial Readout Mode –Data Read from Serial Port Output Buffer

SP Word #	D31 ----------D16	D15 ----------D0
Processor A or C, Serial Port 0		
1	MSB –––––Ch. 1, Sample 1 –––––LSB	MSB –––––Ch. 2, Sample 1 –––––LSB
2	MSB –––––Ch. 1, Sample 2 –––––LSB	MSB –––––Ch. 2, Sample 2 –––––LSB
⋮	⋮	⋮
N	MSB –––––Ch. 1, Sample N –––––LSB	MSB –––––Ch. 2, Sample N –––––LSB
Processor A or C, Serial Port 1		
1	MSB –––––Ch. 3, Sample 1 –––––LSB	MSB –––––Ch. 4, Sample 1 –––––LSB
2	MSB –––––Ch. 3, Sample 2 –––––LSB	MSB –––––Ch. 4, Sample 2 –––––LSB
⋮	⋮	⋮
N	MSB –––––Ch. 3, Sample N –––––LSB	MSB –––––Ch. 4, Sample N –––––LSB
Processor B or D, Serial Port 0		
1	MSB –––––Ch. 5, Sample 1 –––––LSB	MSB –––––Ch. 6, Sample 1 –––––LSB
2	MSB –––––Ch. 5, Sample 2 –––––LSB	MSB –––––Ch. 6, Sample 2 –––––LSB
⋮	⋮	⋮
N	MSB –––––Ch. 5, Sample N –––––LSB	MSB –––––Ch. 6, Sample N –––––LSB
Processor B or D, Serial Port 1		
1	MSB –––––Ch. 7, Sample 1 –––––LSB	MSB –––––Ch. 8, Sample 1 –––––LSB
2	MSB –––––Ch. 7, Sample 2 –––––LSB	MSB –––––Ch. 8, Sample 2 –––––LSB
⋮	⋮	⋮
N	MSB –––––Ch. 7, Sample N –––––LSB	MSB –––––Ch. 8, Sample N –––––LSB

NOTE: This table represents the format of the data as presented to the VIM processor AFTER it has been transferred into the serial port's output buffer on the VIM motherboard, NOT the actual serial bitstream

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3.16 Model 6215 Output Data Formats (continued)

When reading data from the Model 6215 in Parallel mode, via the VIM Bi–FIFO interface, data from each channel selected for readout in the FIFO Channel Select Register is sent to the FIFO in numerical order (lowest–numbered channel first). For example, if Channels 1, 3, 5 and 7 are selected for parallel readout, the first word in the FIFO will contain the first sample from Channel 1, the second FIFO word will have Channel 3's first sample, the third word holds Channel 5's first sample, and the fourth word has Channel 7's first sample. This pattern will repeat beginning in the fifth word with the second samples from Channel 1 (in word 5), Channel 3 (word 6), Channel 5 (word 7) and Channel 7 (word 8), and so on. The A/D output data is left–justified in the 16 most significant bits of each FIFO longword. Bits D15 – D5 are unused, and may be masked when read. D4 is the Mark bit, and will follow the MARK input on the front panel **DIST/SYNC** connector. D3 is the "first sample" bit, and will be a '1' in the word containing the first sample output by each channel, and a '0' thereafter. Bits D2 – D0 comprise the Channel ID field. The Channel ID is equal to the channel number minus 1, and the ID will be encoded in binary in the 3 LSBs of each word in the Bi–FIFO. Table 3–17, below, illustrates the contents of the first 16 words in the Bi–FIFO, assuming that all eight A/D channels on the Model 6215 are enabled for parallel readout.

Table 3–17: Model 6215 –Parallel Readout Mode –VIM Motherboard FIFO Contents

FIFO Word #	D31 ––––––––––––––––––D16	D15 –D5	D4	D3	D2 –D0
1	MSB –––––Ch. 1, Sample 1 –––––LSB	Not Used – Mask When Reading	"Mark" Bit	1	0 0 0
2	MSB –––––Ch. 2, Sample 1 –––––LSB			1	0 0 1
3	MSB –––––Ch. 3, Sample 1 –––––LSB			1	0 1 0
4	MSB –––––Ch. 4, Sample 1 –––––LSB			1	0 1 1
5	MSB –––––Ch. 5, Sample 1 –––––LSB			1	1 0 0
6	MSB –––––Ch. 6, Sample 1 –––––LSB			1	1 0 1
7	MSB –––––Ch. 7, Sample 1 –––––LSB			1	1 1 0
8	MSB –––––Ch. 8, Sample 1 –––––LSB			1	1 1 1
9	MSB –––––Ch. 1, Sample 2 –––––LSB			0	0 0 0
10	MSB –––––Ch. 2, Sample 2 –––––LSB			0	0 0 1
11	MSB –––––Ch. 3, Sample 2 –––––LSB			0	0 1 0
12	MSB –––––Ch. 4, Sample 2 –––––LSB			0	0 1 1
13	MSB –––––Ch. 5, Sample 2 –––––LSB			0	1 0 0
14	MSB –––––Ch. 6, Sample 2 –––––LSB			0	1 0 1
15	MSB –––––Ch. 7, Sample 2 –––––LSB			0	1 1 0
16	MSB –––––Ch. 8, Sample 2 –––––LSB			0	1 1 1

NOTE: This table assumes that all eight channels are enabled for Parallel Readout in the FIFO Channel Select Register. Any channel that is not enabled for parallel readout will simply be skipped in the sequence presented above, and the next enabled channel's data will appear in the next FIFO word. For example, if only Channels 1 - 6 are enabled, the 7th FIFO word would contain the 2nd sample from Channel 1

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Appendix A: Analog Devices AD7722 16–Bit, 195 kSPS CMOS, Sigma–Delta ADC

A.1 Analog Devices AD7722

The following pages are a reprint of the Analog Devices AD7722 16–Bit, 195 kSPS CMOS, Sigma–Delta ADC manual.

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16-Bit, 195 kSPS CMOS, Sigma-Delta ADC

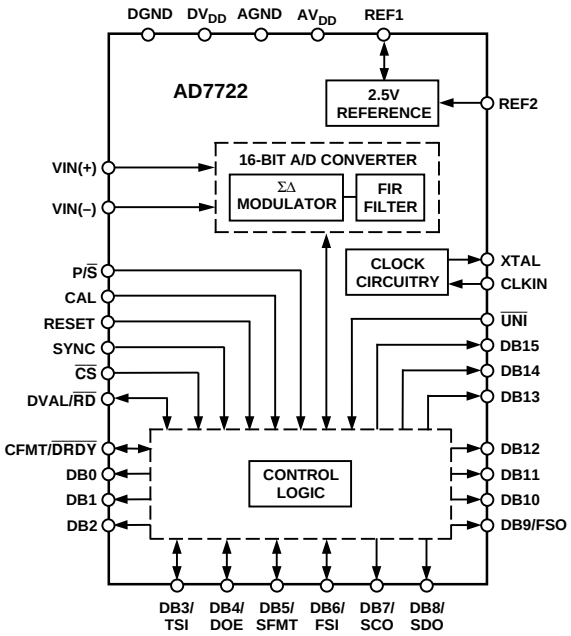
AD7722

FEATURES

16-Bit Sigma-Delta ADC
- **64× Oversampling Ratio**
- **Up to 220 kSPS Output Word Rate**
- **Low-Pass, Linear Phase Digital Filter**

Inherently Monotonic
On-Chip 2.5 V Voltage Reference
Single Supply +5 V
High Speed Parallel or Serial Interface

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7722 is a complete low power, 16-bit, sigma-delta ADC. The part operates from a +5 V supply and accepts a differential input voltage range of 0 V to +2.5 V or ±1.25 V centered around a common-mode bias. The AD7722 provides 16-bit performance for input bandwidths up to 90.625 kHz. The part provides data at an output word rate of 195.3 kHz.

The analog input is continuously sampled by an analog modulator eliminating the need for external sample-and-hold circuitry. The modulator output is processed by two Finite Impulse Response (FIR) digital filters in series. The on-chip filtering reduces the external antialias requirements to first order, in most cases. The group delay for the filter is 215.5 µs, while the settling time for a step input is 431 µs. The sample rate, filter corner frequency, and output word rate are set by an external clock that is nominally 12.5 MHz.

Use of a single bit DAC in the modulator guarantees excellent linearity and dc accuracy. Endpoint accuracy is ensured by on-chip calibration. This calibration procedure minimizes the zero-scale and full-scale errors.

Conversion data is provided at the output register through a flexible serial port or a parallel port. This offers 3-wire, high speed interfacing to digital signal processors. The serial interface operates in an internal clocking (master) mode, whereby an internal serial data clock and framing pulse are device outputs. Additionally, two AD7722s can be configured with the serial data outputs connected together. Each converter alternately transmits its conversion data on a shared serial data line.

The part provides an accurate on-chip 2.5 V reference. A reference input/output function is provided to allow either the internal reference or an external system reference to be used as the reference source for the part.

The AD7722 is available in a 44-pin PQFP package and is specified over the industrial temperature range from –40°C to +85°C.

REV. 0

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AD7722–SPECIFICATIONS[1] (AV_{DD} = AV_{DD1} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND = AGND1 = DGND = 0 V; $\overline{UNI}$ = Logic Low or High; f_{CLKLIN} = 12.5 MHz; F_S = 195.3 kSPS; REF2 = +2.5 V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted)

Parameter	Test Conditions/Comments	A Version Min	Typ	Max	Units
DYNAMIC SPECIFICATIONS[2]					
Bipolar Mode, $\overline{UNI}$ = V_{INH}	V_{CM} = 2.5 V, $V_{IN}(+)$ = $V_{IN}(-)$ =1.25 V pk-pk or, $V_{IN}(-)$ =1.25 V, $V_{IN}(+)$ = 0 to 2.5				
Signal to (Noise + Distortion)[3]	Input Bandwidth 0 kHz–90.625 kHz	86/84.5	90		dB
	Input Bandwidth 0 kHz–100 kHz, f_{CLKIN} = 14 MHz	84.5/83			dB
Total Harmonic Distortion[3]	Input Bandwidth 0 kHz–90.625 kHz			–90/–88	dB
	Input Bandwidth 0 kHz–100 kHz, f_{CLKIN} = 14 MHz			–88/–86	dB
Spurious Free Dynamic Range	Input Bandwidth 0 kHz–90.625 kHz			–90	dB
	Input Bandwidth 0 kHz–100 kHz, f_{CLKIN} = 14 MHz			–88	dB
Unipolar Mode, $\overline{UNI}$ = V_{INL}	$V_{IN}(-)$ = 0 V, $V_{IN}(+)$ = 0 to 2.5				
Signal to (Noise + Distortion)[3]	Input Bandwidth 0 kHz–90.625 kHz	84.5/83	88		dB
Total Harmonic Distortion[3]	Input Bandwidth 0 kHz–97.65 kHz			–89/–87	dB
Spurious Free Dynamic Range	Input Bandwidth 0 kHz–97.65 kHz			–90	dB
Intermodulation Distortion			–93		dB
AC CMRR	$V_{IN}(+)$ = $V_{IN}(-)$ = 2.5 V pk-pk				
	V_{CM} = 1.25 V to 3.75 V, 20 kHz		96		dB
Digital Filter Response					
Pass-Band Ripple	0 kHz–90.625 kHz			±0.005	dB
Cutoff Frequency		96.92			kHz
Stop-Band Attenuation	104.6875 kHz to 12.395 MHz		90		dB
ANALOG INPUTS					
Full-Scale Input Span	$V_{IN}(+)$–$V_{IN}(-)$				
Bipolar Mode	$\overline{UNI}$ = V_{INH}	$-V_{REF2}/2$		$+V_{REF2}/2$	V
Unipolar Mode	$\overline{UNI}$ = V_{INL}	0		V_{REF2}	V
Absolute Input Voltage	$V_{IN}(+)$ and $V_{IN}(-)$	0		AV_{DD}	V
Input Sampling Capacitance			2		pF
Input Sampling Rate	Guaranteed by Design		$2 \times f_{CLKIN}$		Hz
Differential Input Impedance			$1/8E\text{-}09 \times f_{CLKIN}$		kΩ
CLOCK					
CLKIN Mark Space Ratio		45		55	%
REFERENCE					
REF1 Output Voltage		2.32	2.47	2.62	V
REF1 Output Voltage Drift			60		ppm/°C
REF1 Output Impedance			3		kΩ
Reference Buffer					
Offset Voltage	Offset Between REF1 and REF2			±12	mV
Using Internal Reference					
REF2 Output Voltage		2.32	2.47	2.62	V
REF2 Output Voltage Drift			60		ppm/°C
Using External Reference					
REF2 Input Impedance	REF1 = AGND		$1/16E\text{-}09 \times f_{CLKIN}$		kΩ
External Reference Voltage Range	Applied to REF1 or REF2	2.32	2.5	2.62	V
STATIC PERFORMANCE					
Resolution		16			Bits
Differential Nonlinearity	Guaranteed Monotonic		±0.5	±1	LSB
Integral Nonlinearity			±2		LSB
After Calibration					
Offset Error[4]				±3	mV
Gain Error[4, 5]				±0.6	% FSR
Without Calibration					
Offset Error			±6		mV
Gain Error[5]			±0.6		% FSR
Offset Error Drift			±1		LSB/°C
Gain Error Drift	REF2 Is an Ideal Reference, REF1 = AGND				
	Unipolar Mode		±1		LSB/°C
	Bipolar Mode		±0.5		LSB/°C

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Parameter	Test Conditions/Comments	A Version Min	Typ	Max	Units
LOGIC INPUTS (Excluding CLKIN)					
V_{INH}, Input High Voltage		2.0			V
V_{INL}, Input Low Voltage				0.8	V
CLOCK INPUT (CLKIN)					
V_{INH}, Input High Voltage		4.0			V
V_{INL}, Input Low Voltage				0.4	V
ALL LOGIC INPUTS					
I_{IN}, Input Current	V_{IN} = 0 V to DV_{DD}			±10	µA
C_{IN}, Input Capacitance				10	pF
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	$\|I_{OUT}\|$ = 200 µA	4.0			V
V_{OL}, Output Low Voltage	$\|I_{OUT}\|$ = 1.6 mA			0.4	V
POWER SUPPLIES					
AV_{DD}, AV_{DD1}		4.75		5.25	V
DV_{DD}		4.75		5.25	V
I_{DD}	Total from AV_{DD} and DV_{DD}			75	mA
Power Consumption				375	mW

NOTES
[1]Operating temperature range is as follows : A Version ; –40°C to +85°C.
[2]Measurement Bandwidth = 0.5 × F_S; Input Level = –0.05 dB.
[3]T_A = +25°C to +85°C/T_A = T_{MIN} to T_{MAX}.
[4]Applies after calibration at temperature of interest.
[5]Gain Error excludes reference error. The ADC gain is calibrated w.r.t. the voltage on the REF2 pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

DV_{DD} to DGND . . . . . –0.3 V to 7 V
AV_{DD}, AV_{DD1} to AGND . . . . . –0.3 V to 7 V
AV_{DD}, AV_{DD1} to DVDD . . . . . –1 V to +1 V
AGND, AGND1 to DGND . . . . . –0.3 V to +0.3 V
Digital Inputs to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
V_{IN}(+), V_{IN}(–) to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
REF1 to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
REF2 to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
DGND, AGND1, AGND2 . . . . . ±0.3 V
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
θ_{JA} Thermal Impedance . . . . . 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature	Package	Package
AD7722AS	–40°C to +85°C	44-Pin PQFP	S-44

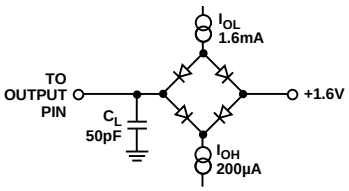


Figure 1. Load Circuit for Timing Specifications

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7722 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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TIMING SPECIFICATIONS (AV_{DD}= +5 V ± 5%, DV_{DD} = +5 V ± 5%, AGND = DGND = 0 V, C_L = 50 pF, T_A = T_{MIN} to T_{MAX}, f_{CLKIN} = 12.5 MHz, SFMT = Logic Low or High, CFMT = Logic Low or High)

	Symbol	Min	Typ	Max	Units
CLKIN Frequency	f_{CLK}	0.3	12.5	15	MHz
CLKIN Period (t_{CLK} = 1/f_{CLK})	t_1	0.067	0.08	3.33	µs
CLKIN Low Pulse Width	t_2	0.45 × t_1		0.55 × t_1	
CLKIN High Pulse Width	t_3	0.45 × t_1		0.55 × t_1	
CLKIN Rise Time	t_4	5			ns
CLKIN Fall Time	t_5	5			ns
FSI Low Time	t_6	2			t_{CLK}
FSI Setup Time	t_7	20			ns
FSI Hold Time	t_8	20			ns
CLKIN to SCO Delay	t_9		40		ns
SCO Period[1]	t_{10}	2			t_{CLK}
SCO Transition to FSO High Delay	t_{11}		4	10	ns
SCO Transition to FSO Low Delay	t_{12}		4	10	ns
SCO Transition to SDO Valid Delay	t_{13}		3	8	ns
SCO Transition from FSI[2]	t_{14}			2.5	t_{CLK}
SDO Enable Delay Time	t_{15}		30	45	ns
SDO Disable Delay Time	t_{16}		10	30	ns
$\overline{DRDY}$ High Time	t_{17}	2			t_{CLK}
Conversion Time[1]	t_{18}	64			t_{CLK}
$\overline{DRDY}$ to $\overline{CS}$ Setup Time	t_{19}	0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{20}	0			ns
$\overline{RD}$ Pulse Width	t_{21}	t_{CLK} + 20			ns
Data Access Time after $\overline{RD}$ Falling Edge[3]	t_{22}			t_{CLK} + 40	ns
Bus Relinquish Time after $\overline{RD}$ Rising Edge	t_{23}			t_{CLK} + 40	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{24}	0			ns
$\overline{RD}$ to $\overline{DRDY}$ High Time	t_{25}		1		t_{CLK}
SYNC/RESET Input Pulse Width	t_{26}	10			ns
DVAL Low Delay from SYNC/RESET	t_{27}			40	ns
SYNC/RESET Low Time Before CLKIN Rising	t_{28}	10			ns
$\overline{DRDY}$ High Delay after SYNC/RESET Low	t_{29}			50	ns
$\overline{DRDY}$ Low Delay after SYNC/RESET Low[1]	t_{30}			(8192 + 64)	t_{CLK}
DVAL High Delay after SYNC/RESET Low[1]	t_{31}			8192	t_{CLK}
CAL Setup Time	t_{34}	10			ns
CAL Pulse Width	t_{35}	1		2	t_{CLK}
Calibration Delay from CAL High	t_{36}			64	t_{CLK}
Unipolar Input Calibration Time, ($\overline{UNI}$ = "0")[1]	t_{37}			(3 × 8192 + 2 × 512)	t_{CLK}
Bipolar Input Calibration Time, ($\overline{UNI}$ = "1")[1]	t_{37}			(4 × 8192 + 3 × 512)	t_{CLK}
Conversion Results Valid, ($\overline{UNI}$ = "0")[1]	t_{38}			(3 × 8192 + 2 × 512 + 64)	t_{CLK}
Conversion Results Valid, ($\overline{UNI}$ = "1")[1]	t_{38}			(4 × 8192 + 3 × 512 + 64)	t_{CLK}

NOTES
[1]Guaranteed by design.
[2]Frame Sync is initiated on falling edge of CLKIN.
[3]With $\overline{RD}$ synchronous to CLKIN t_{22}, can be reduced up to 1 t_{CLK}.

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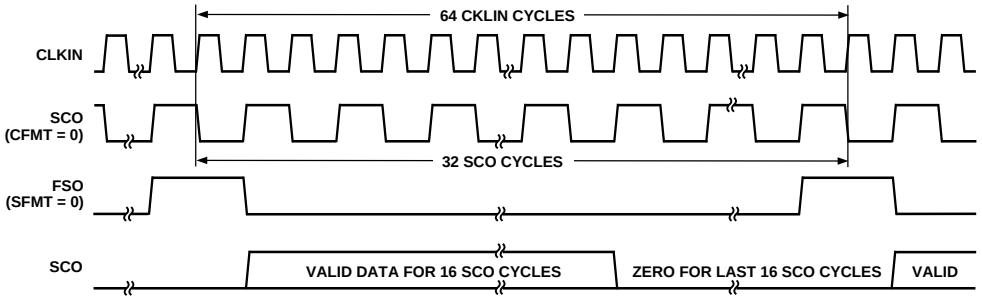


Figure 2a. Generalized Serial Mode Timing (FSI = Logic Low or High, TSI = DOE)

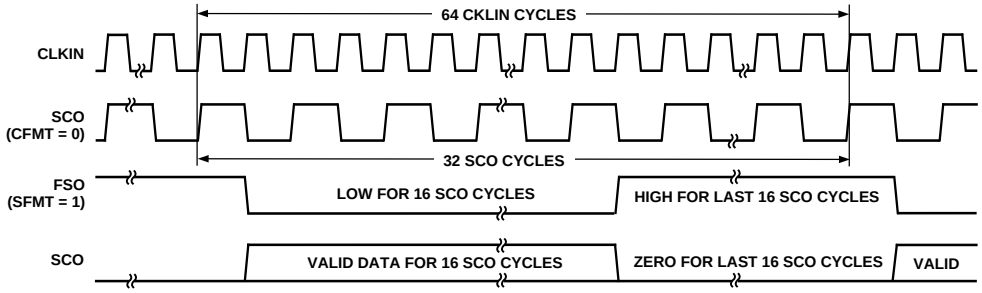


Figure 2b. Generalized Serial Mode Timing (FSI = Logic Low or High, TSI = DOE)

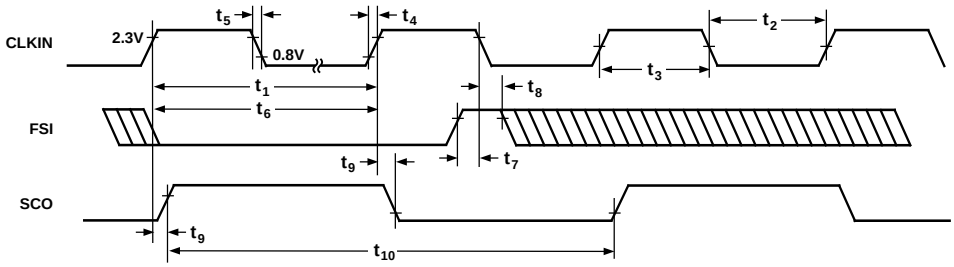


Figure 3. Serial Mode Timing for Clock Input, Frame Sync Input and Serial Clock Output

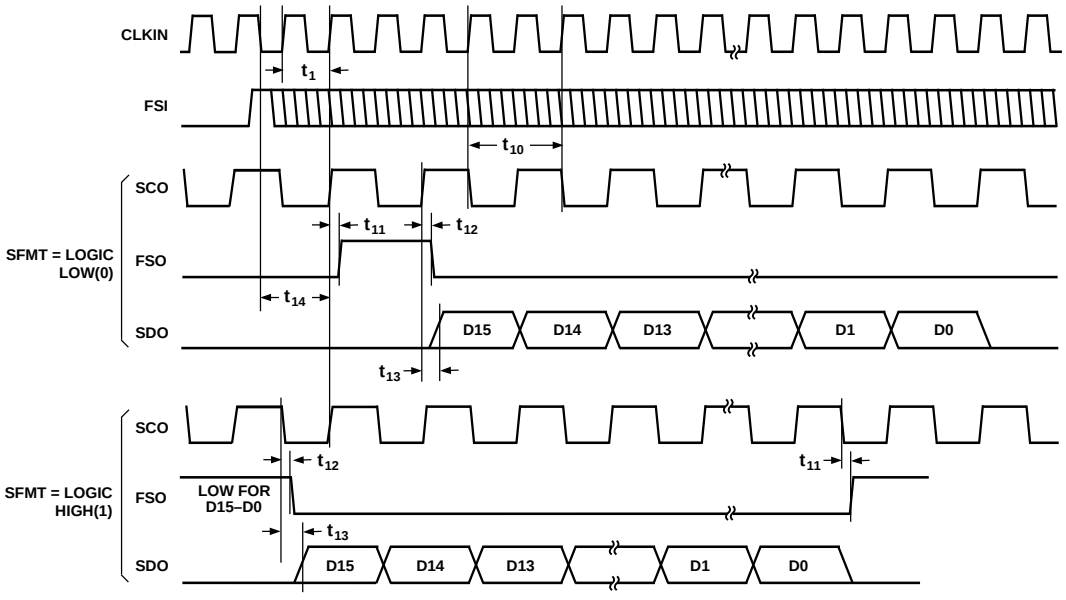


Figure 4. Serial Mode Timing for Frame Sync Input, Frame Sync Output, Serial Clock Output and Serial Data Output (CFMT = Logic Low, TSI = DOE)

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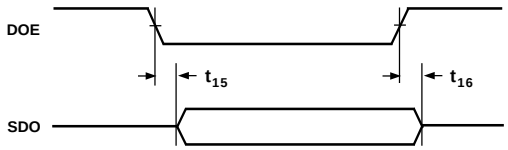


Figure 5. Serial Mode Timing for Data Output Enable and Serial Data Output (TSI = Logic Low)

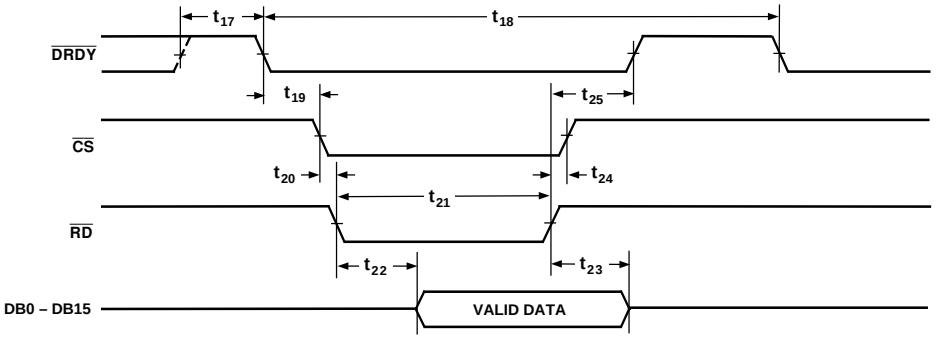


Figure 6. Parallel Mode Read Timing

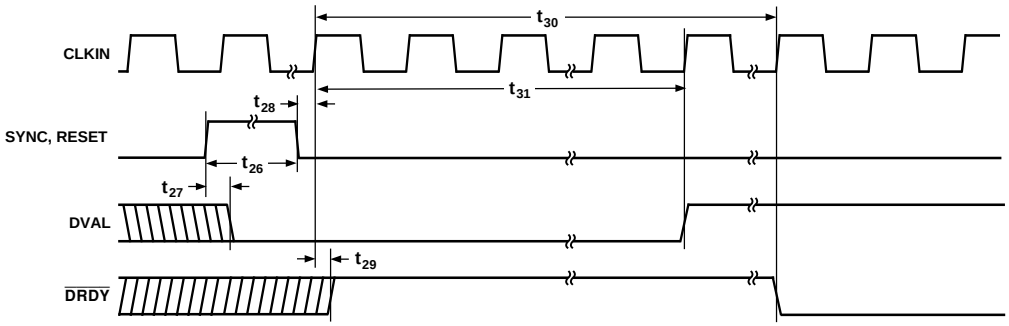


Figure 7. SYNC and RESET Timing, Serial and Parallel Mode

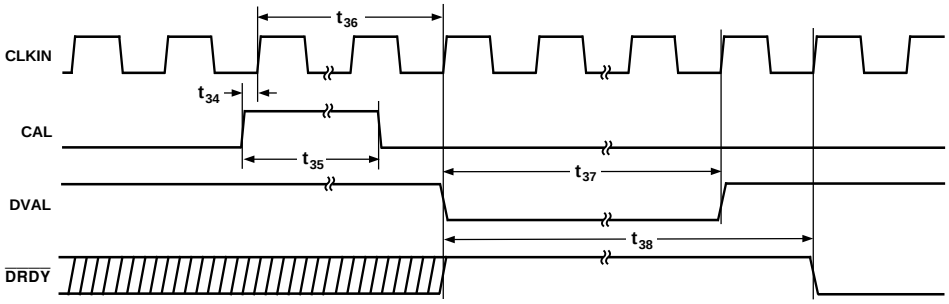


Figure 8. Calibration Timing, Serial and Parallel Mode

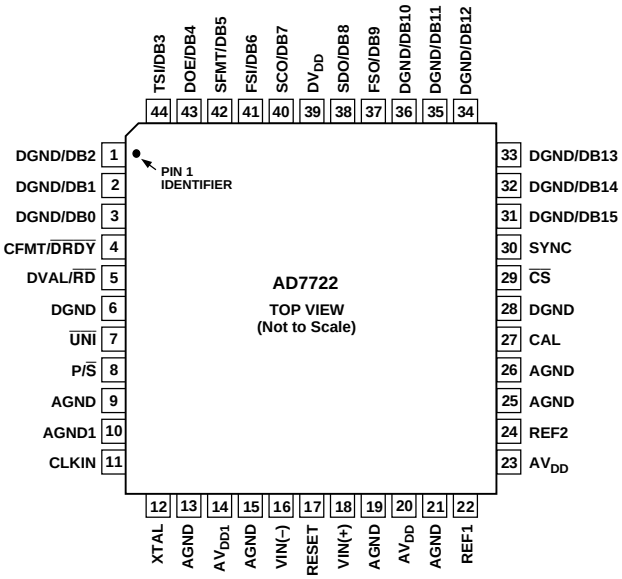
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PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Description
AV_{DD1}	14	Clock logic power supply voltage for the analog modulator, +5 V ± 5%.
AGND1	10	Clock logic ground reference for the analog modulator.
AV_{DD}	20, 23	Analog Power Supply Voltage, +5 V ± 5%.
AGND	9, 13, 15, 19, 21, 25, 26	Ground reference for analog circuitry.
DV_{DD}	39	Digital Power Supply Voltage, +5 V ± 5%.
DGND	6, 28	Ground reference for digital circuitry.
REF1	22	Reference Input/Output. REF1 connects through 3 kΩ to the output of the internal 2.5 V reference and to the input of a buffer amplifier that drives the Σ–Δ modulator. This pin can also be overdriven with an external reference 2.5 V.
REF2	24	Reference Input/Output. REF2 connects to the output of an internal buffer amplifier used to to drive the Σ–Δ modulator. When REF2 is used as an input, REF1 must be connected to AGND.
$V_{IN}(+)$	18	Positive terminal of the differential analog input.
$V_{IN}(-)$	16	Negative terminal of the differential analog input.
$\overline{UNI}$	7	Analog input range select input. $\overline{UNI}$ selects the analog input range for either bipolar or unipolar operation. A logic low input selects unipolar operation. A logic high input selects bipolar operation.
CLKIN	11	Clock Input. Master clock signal for the device. The CLKIN pin interfaces the AD7722 internal oscillator circuit to an external crystal or to an external clock. A parallel resonant, fundamental-frequency, microprocessor-grade crystal and a 1 MΩ resistor should be connected between the CLKIN and XTAL pin with two capacitors connected from each pin to ground. Alternatively, the CLKIN pin can be driven with an external CMOS-compatible clock. The AD7722 is specified with a clock input frequency of 12.5 MHz.
XTAL	12	Oscillator Output. The XTAL pin connects the internal oscillator output to an external crystal. If an external clock is used, XTAL should be left unconnected.
P/$\overline{S}$	8	Parallel/Serial interface select input. A logic high configures output data interface for parallel mode operation. Serial mode operation is selected with the P/S set to a logic low.
CAL	27	Calibration Logic Input. A logic high input for a duration of one CLKIN cycle initiates a calibration sequence for the device Gain and Offset Error.
RESET	17	Reset Logic Input. RESET is used to clear the offset and gain calibration registers. RESET is an asynchronous input. RESET allows the user to set AD7722 to an uncalibrated state if the device had been previously calibrated. A rising edge also resets the AD7722 Σ–Δ modulator by shorting the integrator capacitors in the modulator. In addition RESET functions identically to the SYNC pin described below.
$\overline{CS}$	29	Chip select is a level sensitive logic input. $\overline{CS}$ enables the output data register for parallel mode read operation. The $\overline{CS}$ logic level is sensed on the rising edge of CLKIN. The output data bus is enabled when the rising edge of CLKIN senses a logic low level on $\overline{CS}$ if $\overline{RD}$ is also low. When $\overline{CS}$ is sensed high, the output data bits DB15–DB0 will be high impedance. In serial mode tie $\overline{CS}$ to a logic low.
SYNC	30	Synchronization Logic Input. SYNC is an asynchronous input. When using more than one AD7722 operated from a common master clock, SYNC allows each ADC's Σ–Δ modulator to simultaneously sample its analog input and update its output data register. A rising edge resets the AD7722 digital filter sequencer counter to zero. After a SYNC, conversion data is not valid until after the digital filter settles (reference Figure 7). DVAL goes low in the serial mode. When the rising edge of CLKIN senses a logic low on SYNC (or RESET) the reset state is released; in parallel mode, $\overline{DRDY}$ goes high. After the reset state is released, DVAL returns high after 8192 CLKIN cycles ($128 \times 64/f_{CLKIN}$); in parallel mode, $\overline{DRDY}$ returns low after one additional convolution cycle of the digital filter (64 CLKIN periods), when valid data is ready to be read from the output data register.

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PIN CONFIGURATION
44-Pin PQFP (S-44)



PARALLEL MODE PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Description
DVAL/$\overline{RD}$	5	Read Input is a level sensitive logic input. The $\overline{RD}$ logic level is sensed on the rising edge of CLKIN. This digital input can be used in conjunction with $\overline{CS}$ to read data from the device. The output data bus is enabled when the rising edge of CLKIN senses a logic low level on $\overline{RD}$ if $\overline{CS}$ is also low. When $\overline{RD}$ is sensed high, the output data bits DB15–DB0 will be high impedance.
CFMT/$\overline{DRDY}$	2	Data Ready Logic Output. A falling edge indicates a new output word is available to be read from output data register. DRDY will return high upon completion of a read operation. If a read operation does not occur between output updates, DRDY will pulse high for two CLKIN cycles before the next output update. DRDY also indicates when conversion results are available after a SYNC or RESET sequence and when completing a self-calibration.
DGND/DB15	31	Data Output Bit (MSB)
DGND/DB14	32	Data Output Bit
DGND/DB13	33	Data Output Bit
DGND/DB12	34	Data Output Bit
DGND/DB11	35	Data Output Bit
DGND/DB10	36	Data Output Bit
FSO/DB9	37	Data Output Bit
SDO/DB8	38	Data Output Bit
SCO/DB7	40	Data Output Bit
FSI/DB6	41	Data Output Bit
SFMT/DB5	42	Data Output Bit
DOE/DB4	43	Data Output Bit
TSI/DB3	44	Data Output Bit
DGND/DB2	1	Data Output Bit
DGND/DB1	2	Data Output Bit
DGND/DB0	3	Data Output Bit (LSB)

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SERIAL MODE PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Description
DVAL/$\overline{RD}$	5	Data Valid Logic Output. A logic high on DVAL indicates that the conversion result in the output data register is an accurate digital representation of the analog voltage at the input to the Σ–Δ modulator. The DVAL pin is set low for 8,192 CLKIN cycles if the analog input is overranged and after initiating CAL, SYNC or RESET.
CFMT/$\overline{DRDY}$	4	Serial Clock Format Logic Input. The clock format pin selects whether the serial data, SDO, is valid on the rising or falling edge of the serial clock, SCO. When CFMT is logic low—SDO is valid on the falling edge of SCO if SFMT is Low; SDO is valid on the rising edge of SCO if SFMT is High. When CFMT is logic high—SDO is valid on the rising edge of SCO if SFMT is Low; SDO is valid on the falling edge of SCO if SFMT is High.
TSI/DB3	44	Time Slot Logic Input. The logic level on TSI sets the active state of the DOE pin. With TSI set logic high, DOE will enable the SDO output buffer when it is a logic high, and vice versa. TSI is used when two AD7722s are connected to the same serial data bus.
DOE/DB4	43	Data Output Enable Logic Input. The DOE pin controls the three-state output buffer of the SDO pin. The active state of DOE is determined by the logic level on the TSI pin. When the DOE logic level equals the level on TSI pin, the serial data output, SDO, is active. Otherwise, SDO will be high impedance. SDO can be three-state after a serial data transmission by connecting DOE to FSO.
SFMT/DB5	42	Serial Data Format Logic Input. The logic level on the SFMT pin selects the format of the FSO signal. A logic low makes the FSO output a pulse one SCO cycle wide occurring every 32 SCO cycles. With SFMT set to a logic high, the FSO signal is a frame pulse that is active low for the duration of the 16 data bit transmission.
FSI/DB6	41	Frame Synchronization Logic Input. The FSI input is used to synchronize the AD7722 serial output data register to an external source. When the falling edge of CLKIN detects a low to high transition, the AD7722 interrupts the current data transmission, reloads the output serial shift register, resets SCO, and transmits the conversion result. Synchronization starts immediately, and the next 127 conversions are invalid. In serial mode, DVAL remains high. FSI inputs applied synchronous to the output data rate do not alter the serial data transmission. If FSI is tied to either a logic high or low, the AD7722 will generate FSO outputs controlled by the logic level on SMFT.
SCO/DB7	40	Serial Data Clock Output. The serial clock output is synchronous to the CLKIN signal and has a frequency one-half the CLKIN frequency. A data transmission frame is 32 SCO cycles long.
SDO/DB8	38	Serial Data Output. The serial data is shifted out MSB first, synchronous with the SCO. A serial data transmission lasts 32 SCO cycles. After the LSB is output, trailing zeros are output for the remaining 16 SCO cycles.
FSO/DB9	37	Frame Sync Output. This output indicates the beginning of a word transmission on the SDO pin. Depending on the logic level of the SFMT pin, the FSO signal is either a positive pulse approximately one SCO period wide or a frame pulse, which is active low for the duration of the 16 data bit transmission (reference Figure 4).
DGND/DB0	3	In serial mode these pins should be tied to DGND.
DGND/DB1	2	
DGND/DB2	1	
DGND/DB10	36	
DGND/DB11	35	
DGND/DB12	34	
DGND/DB13	33	
DGND/DB14	32	
DGND/DB15	31	

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TERMINOLOGY

Signal-to-Noise Plus Distortion Ratio (S/(N+D))
S/(N+D) is the measured signal-to-noise plus distortion ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise plus distortion is the rms sum of all of the nonfundamental signals and harmonics to half the sampling rate ($F_{CLKIN}/128$), excluding dc. The ADC is evaluated by applying a low noise, low distortion sine wave signal to the input pins. By generating a Fast Fourier Transform (FFT) plot, the S/(N+D) data can then be obtained from the output spectrum.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the harmonics to the rms value of the fundamental. THD is defined as:

$$THD = 20\log\left(\frac{SQRT\left(V_2^2+V_3^2+V_4^2+V_5^2+V_6^2\right)}{V_1}\right)$$

where $V1$ is the rms amplitude of the fundamental and $V2$, $V3$, $V4$, $V5$ and $V6$ are the rms amplitudes of the second through sixth harmonics. The THD is also derived from the FFT plot of the ADC output spectrum.

Spurious Free Dynamic Range (SFDR)
Defined as the difference, in dB, between the peak spurious or harmonic component in the ADC output spectrum (up to $F_{CLKIN}/128$ and excluding dc) and the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the output spectrum of the FFT. For input signals whose second harmonics occur in the stop band region of the digital filter, a spur in the noise floor limits the SFDR.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Testing is performed using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamental expressed in dB.

Pass-Band Ripple
The frequency response variation of the AD7722 in the defined pass-band frequency range.

Pass-Band Frequency
The frequency up to which the frequency response variation is within the pass-band ripple specification.

Cutoff Frequency
The frequency below which the AD7722's frequency response will not have more than 3 dB of attenuation.

Stop-Band Frequency
The frequency above which the AD7722's frequency response will be within its stop-band attenuation.

Stop-Band Attenuation
The AD7722's frequency response will not have less than 90 dB of attenuation in the stated frequency band.

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are minus full scale, a point 0.5 LSB below the first code transition (100 . . . 00 to 100 . . . 01 in bipolar mode, 000 . . . 00 to 000 . . . 01 in unipolar mode) and plus full scale, a point 0.5 LSB above the last code transition (011 . . . 10 to 011 . . . 11 in bipolar mode, 111 . . . 10 to 111 . . . 11 in unipolar mode). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between two adjacent codes in the ADC.

Common-Mode Rejection Ratio
The ability of a device to reject the effect of a voltage applied to both input terminals simultaneously—often through variation of a ground level—is specified as a common-mode rejection ratio. CMRR is the ratio of gain for the differential signal to the gain for the common-mode signal.

Unipolar Offset Error
Unipolar offset error is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal differential voltage (VIN(+) – VIN(–)+ 0.5 LSB) when operating in the unipolar mode.

Bipolar Offset Error
This is the deviation of the midscale transition code (111 . . . 11 to 000 . . . 00) from the ideal differential voltage (VIN(+) – VIN(–) – 0.5 LSB) when operating in the bipolar mode.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above –full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

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(AV_{DD} = DV_{DD} = 5.0 V, T_A = +25°C; CLKIN = 12.5 MHz, AIN = 20 kHz, Bipolar Mode; V_{IN}(+) = 0 V to 2.5 V, V_{IN}(–) = 1.25 V unless otherwise noted)

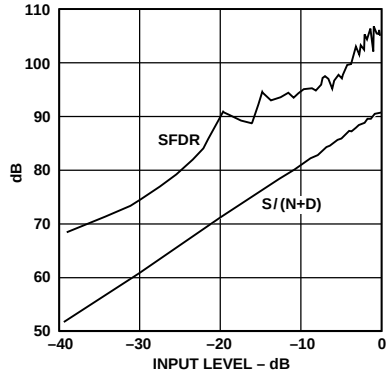


Figure 9. S/(N+D) and SFDR vs. Analog Input Level

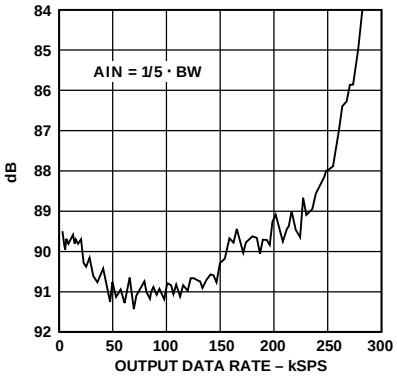


Figure 10. S/(N+D) vs. Output Sample Rate

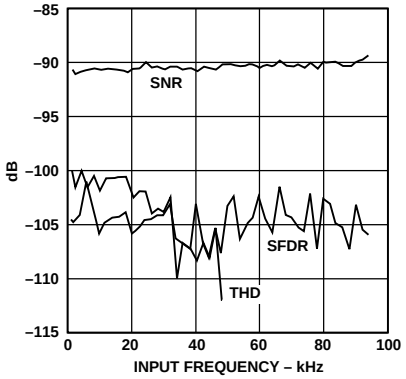


Figure 11. SNR, THD, and SFDR vs. Input Frequency

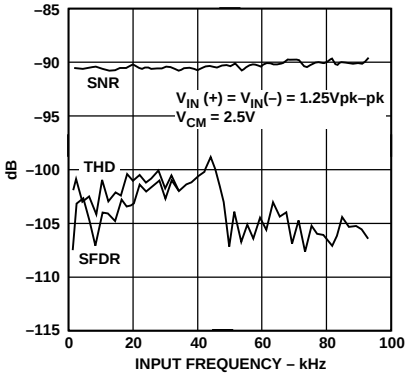


Figure 12. SNR, THD, and SFDR vs. Input Frequency

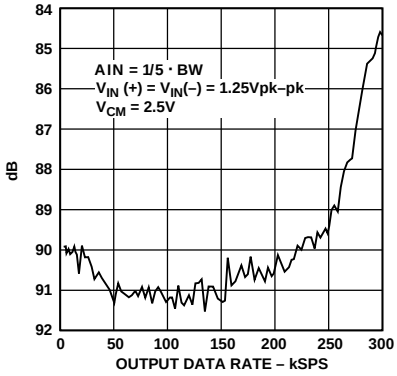


Figure 13. S/(N+D) vs. Output Sample Rate

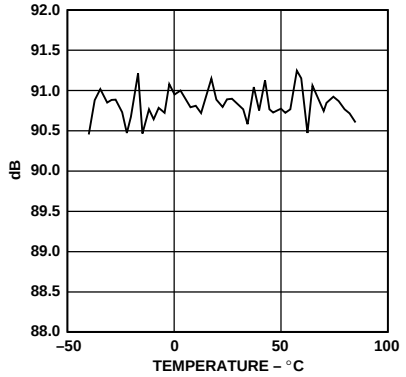


Figure 14. SNR vs. Temperature

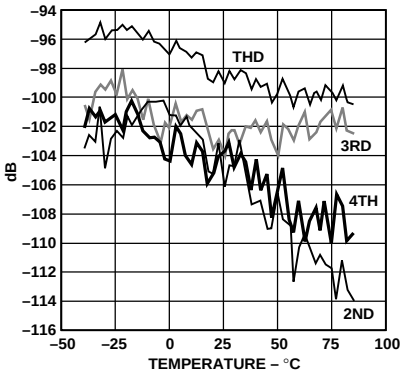


Figure 15. THD vs. Temperature

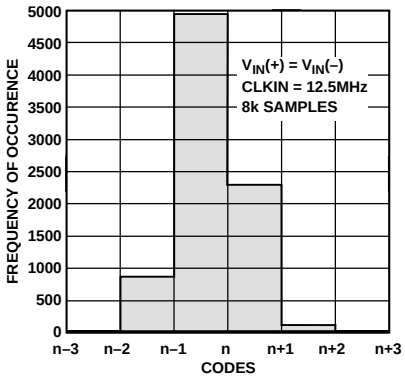


Figure 16. Histogram of Output Codes with DC Input

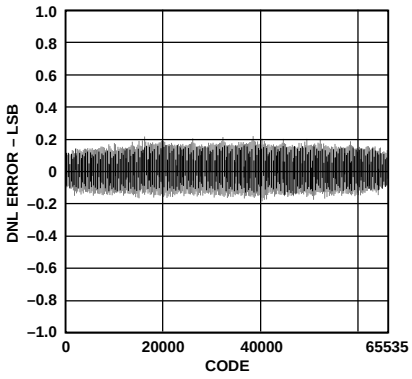


Figure 17. Differential Nonlinearity

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AD7722–Typical Characteristics

(AV_{DD} = DV_{DD} = 5.0 V, T_A = +25°C; CLKIN = 12.5 MHz, AIN = 20 kHz, Bipolar Mode; V_{IN}(+) = 0 V to 2.5 V, V_{IN}(–) = 1.25 V unless otherwise noted)

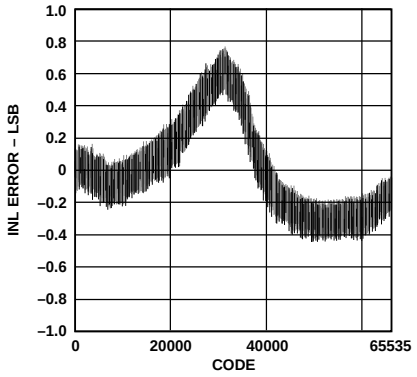


Figure 18. Integral Nonlinearity Error

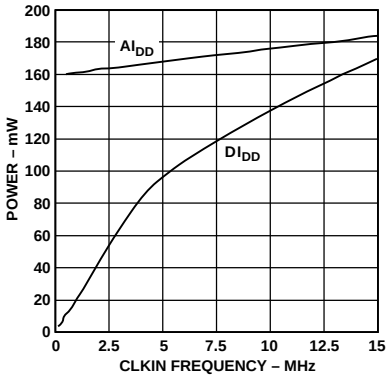


Figure 21. Power Consumption vs. CLKIN Frequency

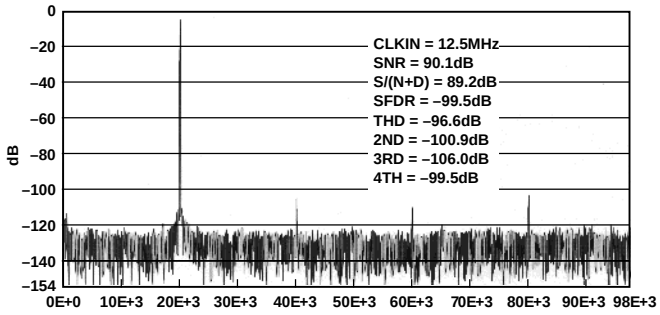


Figure 19. 16K Point FFT

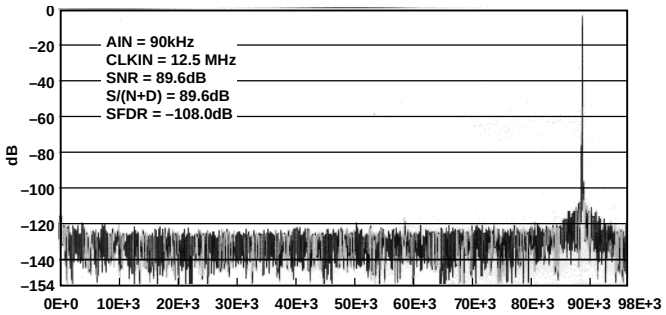


Figure 22. 16K Point FFT

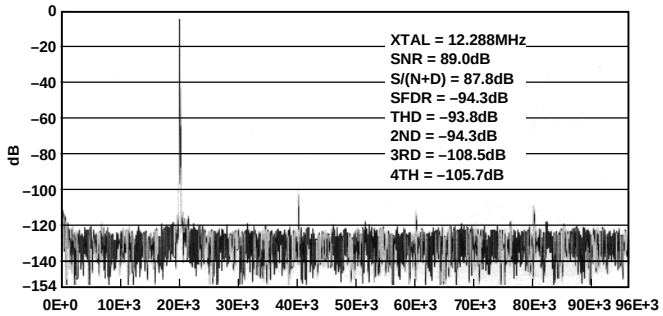


Figure 20. 16K Point FFT

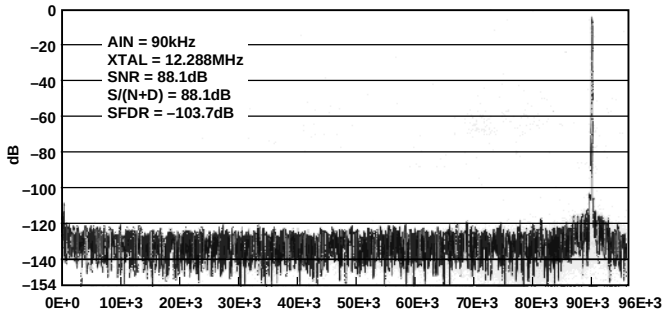


Figure 23. 16K Point FFT

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CIRCUIT DESCRIPTION

The AD7722 ADC employs a sigma-delta conversion technique that converts the analog input into a digital pulse train. The analog input is continuously sampled by a switched capacitor modulator at twice the rate of the clock input frequency, $2 \times f_{CLKIN}$. The digital data that represents the analog input is in the 1's density of the bit stream at the output of the sigma-delta modulator. The modulator outputs a bit stream at a data rate equal to f_{CLKIN}.

Due to the high oversampling rate, which spreads the quantization noise from 0 to $f_{CLKIN}/2$, the noise energy contained in the band of interest is reduced (Figure 24a). To reduce the quantization noise further, a high order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the band of interest (Figure 24b).

The digital filter that follows the modulator provides three main functions. The filter performs sophisticated averaging on the 1 bit samples from the output of the modulator, while removing the large out of band quantization noise (Figure 24c). Lastly the digital filter reduces the data rate from f_{CLKIN} at the input of the filter to $f_{CLKIN}/64$ at the output of the filter. The AD7722 output data rate, F_S, is a little over twice the signal bandwidth, which guarantees that there is no loss of data in the signal band.

Digital filtering has certain advantages over analog filtering. First, since digital filtering occurs after the A/D conversion, it can remove noise injected during the conversion process. Analog filtering cannot remove noise injected during conversion. Second, the digital filter combines low pass-band ripple with a steep roll off, while also maintaining a linear phase response.

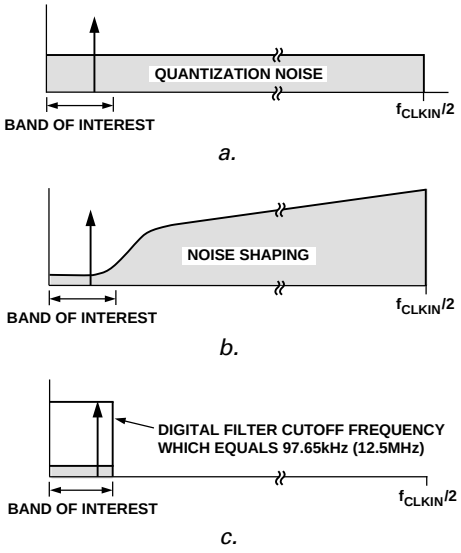


Figure 24. Sigma-Delta ADC

The AD7722 employs two Finite Impulse Response (FIR) filters in series. The first filter is a 384 tap filter that samples the output of the modulator at f_{CLKIN}. The second filter is a 151 tap half-band filter that samples the output of the first filter at $f_{CLKIN}/32$ and decimates by 2. The implementation of this filter architecture results in a filter with a group delay of 42 conversions (84 conversions for settling to a full-scale step).

The digital filter provides 6 dB of attenuation at a frequency ($f_{CLKIN}/128$) one-half its output rate. With a clock frequency of 12.5 MHz, the digital filter has a pass-band frequency of 90.625 kHz, a cutoff frequency is 96.92 kHz and stop-band frequency of 104.6875 kHz.

Due to the sampling nature of the digital filter, the filter does not provide any rejection at integer multiples of its input sampling frequency. The filter response in Figure 25a shows the unattenuated frequency bands occurring at $n \times f_{CLKIN}$ where $n = 1, 2, 3\ldots$. At these frequencies, there are frequency bands $\pm f_{3\,dB}$ wide ($f_{3\,dB}$ is the –3 dB bandwidth of the digital filter) on either side of $n \times f_{CLKIN}$ where noise passes unattenuated to the output. Out of band signals coincident with any of the filter images are aliased into the pass band. However, due to the AD7722's high oversampling ratio, these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered. This means that the antialias filtering requirements in front of the AD7722 are considerably reduced versus a conventional converter with no on-chip filtering. Figure 25b shows the frequency response of an antialias filter. With a –3 dB corner frequency set at $f_{CLKIN}/64$, a single pole filter will provide 36 dB of attenuation at f_{CLKIN}.

Depending on the application, however, it may be necessary to provide additional antialias filtering prior to the AD7722 to eliminate unwanted signals from the frequency bands the digital filter passes. It may also be necessary in some applications to provide analog filtering in front of the AD7722 to ensure that differential noise signals outside the band of interest do not saturate the analog modulator.

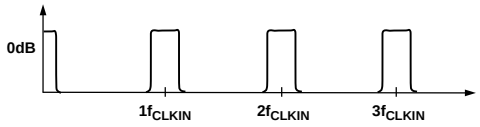


Figure 25a. Digital Filter Frequency Response

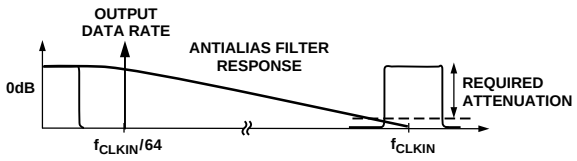


Figure 25b. Frequency Response of Antialias Filter

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APPLYING THE AD7722

Analog Input Range

The AD7722 uses differential inputs to provide common-mode noise rejection (i.e., the converted result will correspond to the differential voltage between the two inputs). The absolute voltage on both inputs must lie between AGND and AV_{DD}.

In the unipolar mode, the full-scale analog input range (VIN(+) – VIN(–)) is 0 V to V_{REF2}. The output code is straight binary in the unipolar mode with 1 LSB = 38 µV. The ideal transfer function is shown in Figure 26.

In bipolar mode, the full-scale input range is $\pm V_{REF2}/2$. The bipolar mode allows complementary input signals. As another example, in bipolar mode, VIN(–) can be connected to a dc bias voltage to allow a single-ended input on VIN(+) equal to V_{BIAS} $\pm V_{REF2}/2$. In bipolar mode the output code is 2s complement with 1 LSB = 38 µV. The ideal transfer function is shown in Figure 27.

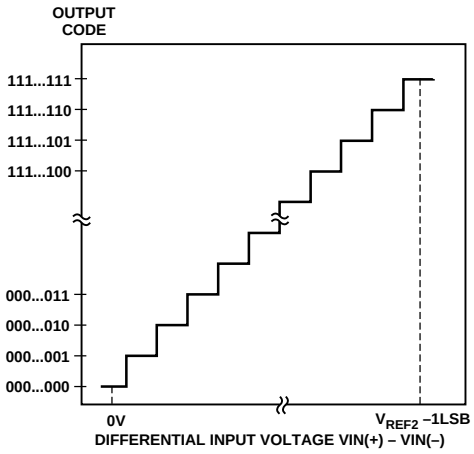


Figure 26. Unipolar Mode Transfer Function

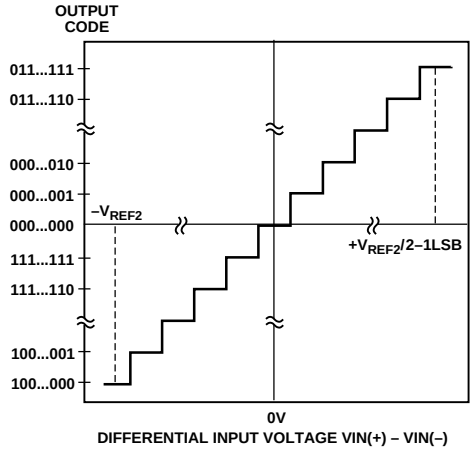


Figure 27. Bipolar Mode Transfer Function

Differential Inputs

The analog input to the modulator is a switched capacitor design. The analog signal is converted into charge by highly linear sampling capacitors. A simplified equivalent circuit diagram of the analog input is shown in Figure 28. A signal source driving the analog input must be able to provide the charge onto the sampling capacitors every half CLKIN cycle and settle to the required accuracy within the next half cycle.

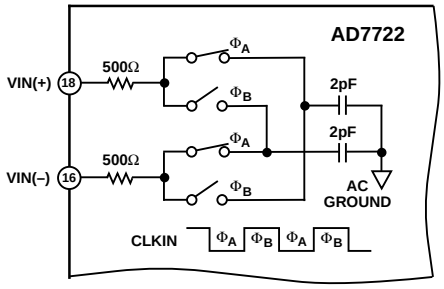


Figure 28. Analog Input Equivalent Circuit

Since the AD7722 samples the differential voltage across its analog inputs, low noise performance is attained with an input circuit that provides low common-mode noise at each input. The amplifiers used to drive the analog inputs play a critical role in attaining the high performance available from the AD7722.

When a capacitive load is switched onto the output of an op amp, the amplitude will momentarily drop. The op amp will try to correct the situation and in the process hits its slew rate limit. This nonlinear response, which can cause excessive ringing, can lead to distortion. To remedy the situation, a low-pass RC filter can be connected between the amplifier and the input to the AD7722 as shown in Figure 29. The external capacitor at each input aids in supplying the current spikes created during the sampling process. The resistor in this diagram, as well as creating the pole for the antialiasing, isolates the op amp from the transient nature of the load.

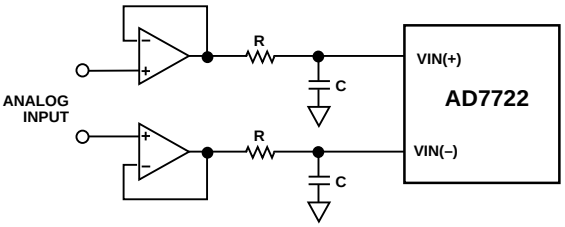


Figure 29. Simple RC Antialiasing Circuit

The differential input impedance of the AD7722 switched capacitor input varies as a function of the CLKIN frequency, given by the equation:

$$Z_{IN} = \frac{10^9}{8 \times f_{CLKIN}} \ k\Omega$$

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Even though the voltage on the input sampling capacitors may not have enough time to settle to the accuracy indicated by the resolution of the AD7722, as long as the sampling capacitor charging follows the exponential curve of RC circuits, only the gain accuracy suffers if the input capacitor is switched away too early.

An alternative circuit configuration for driving the differential inputs to the AD7722 is shown in Figure 30.

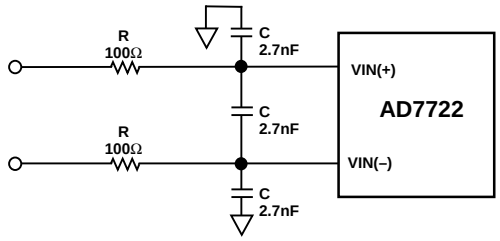


Figure 30. Differential Input with Antialiasing

A capacitor between the two input pins sources or sinks charge to allow most of the charge that is needed by one input to be effectively supplied by the other input. This minimizes undesirable charge transfer from the analog inputs to and from ground. The series resistor isolates the operational amplifier from the current spikes created during the sampling process and provides a pole for antialiasing. The –3 dB cutoff frequency ($f_{3\,dB}$) of the antialias filter is given by Equation 1, and the attenuation of the filter is given by Equation 2.

$$f_{3\,dB} = \frac{1}{6\,\pi\,RC} \quad (1)$$

$$Attenuation = 20\log\left(1/\sqrt{1+\left(\frac{f}{f_{3\,dB}}\right)^2}\right) \quad (2)$$

The choice of the filter cutoff frequency will depend on the amount of roll-off that is acceptable in the pass band of the digital filter and the required attenuation at the first image frequency. For example, when operating the AD7722 with a 12.5 MHz clock; with the typical values of R and C of 100 Ω and 2.7 nF shown in Figure 30, the –3 dB cutoff frequency ($f_{3\,dB}$) creates less than 1 dB of in band (90.625 kHz) roll-off and provides about 36 dB attenuation at the first image frequency.

The capacitors used for the input antialiasing circuit must have low dielectric absorption to avoid distortion. Film capacitors such as Polypropylene, Polystyrene or Polycarbonate are suitable. If ceramic capacitors are used, they must have NP0 dielectric.

Applying the Reference

The reference circuitry used in the AD7722 includes an on-chip 2.5 V band gap reference and a reference buffer circuit. The block diagram of the reference circuit is shown in Figure 31. The internal reference voltage is connected to REF1 through a 3 kΩ resistor and is internally buffered to drive the analog modulator's switched cap DAC (REF2). When using the internal reference, connect 100 nF between REF1 and AGND. If the internal reference is required to bias external circuits, use an external precision op amp to buffer REF1.

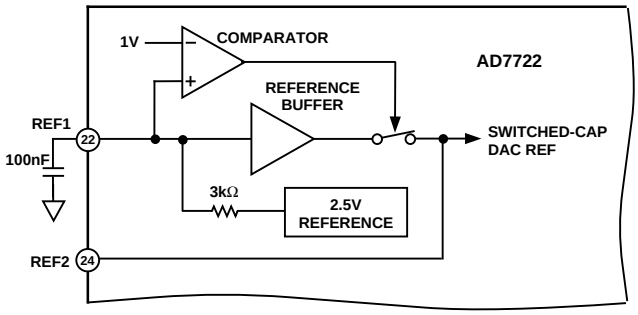


Figure 31. Reference Circuit Block Diagram

The AD7722 can operate with its internal reference or an external reference can be applied in two ways. An external reference can be connected to REF1, overdriving the internal reference. However, there will be an error introduced due to the offset of the internal buffer amplifier. For lowest system gain errors when using an external reference, REF1 is grounded (disabling the internal buffer) and the external reference is connected to REF2.

In all cases, since the REF2 voltage connects to the analog modulator, a 100 nF capacitor must connect directly from REF2 to AGND. The external capacitor provides the charge required for the dynamic load presented at the REF2 pin (Figure 32).

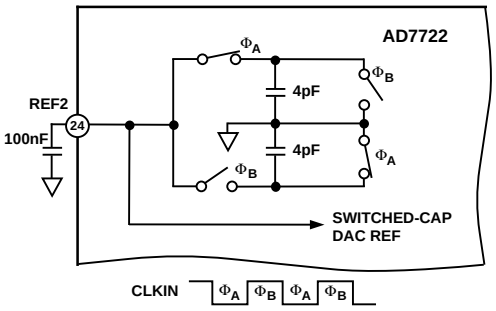


Figure 32. REF2 Equivalent Input Circuit

The AD780 is ideal to use as an external reference with the AD7722. Figure 33 shows a suggested connection diagram.

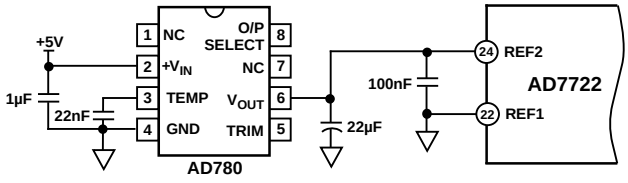


Figure 33. External Reference Circuit Connection

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Input Circuits

Figures 34 and 35 show two simple circuits for bipolar mode operation. Both circuits accept a single-ended bipolar signal source and create the necessary differential signals at the input to the ADC.

The circuit in Figure 34 creates a 0 V to 2.5 V signal at the VIN(+) pin to form a differential signal around an initial bias of 1.25 V. For single-ended applications best THD performance is obtained with VIN(–) set to 1.25 V rather than 2.5 V. The input to the AD7722 can also be driven differentially with a complementary input as shown in Figure 35.

In this case, the input common-mode voltage is set to 2.5 V. The 2.5 V p-p full-scale differential input is obtained with a 1.25 V p-p signal at each input in antiphase. This configuration minimizes the required output swing from the amplifier circuit and is useful for single supply applications.

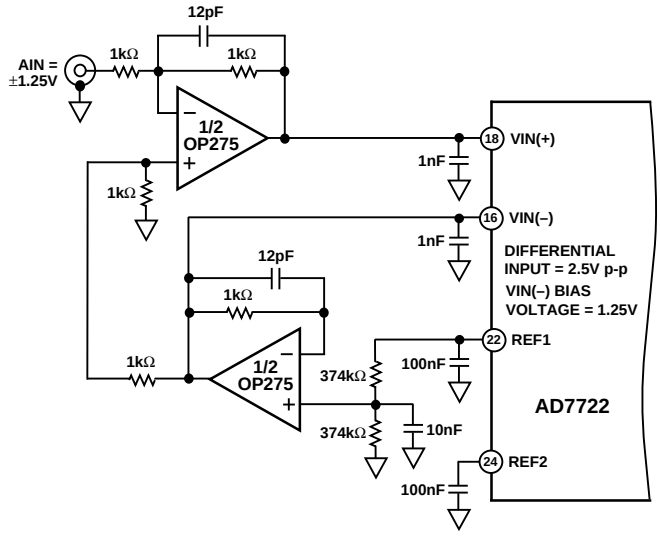


Figure 34. Single-Ended Analog Input Circuit for Bipolar Mode Operation

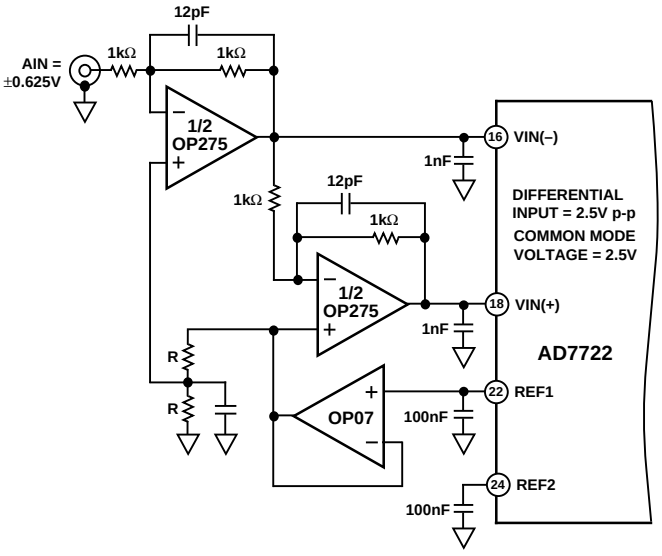


Figure 35. Single-Ended to Differential Analog Input Circuit for Bipolar Mode Operation

The 1 nF capacitors at each ADC input store charge to aid the amplifier settling as the input is continuously sampled. A resistor in series with the drive amplifier output and the 1 nF input capacitor may also be used to create an antialias filter.

Clock Generation

The AD7722 contains an oscillator circuit to allow a crystal or an external clock signal to generate the master clock for the ADC. The connection diagram for use with crystal is shown in Figure 36, below. Consult the crystal manufacturer's recommendation for the load capacitors.

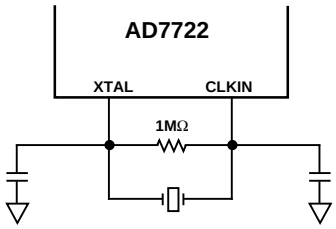


Figure 36. Crystal Oscillator Connection

An external clock must be free of ringing and have a minimum rise time of 5 ns. Degradation in performance can result, as high edge rates increase coupling that can generate noise in the sampling process. The connection diagram for an external clock source (Figure 37) shows a series damping resistor connected between the clock output and the clock input to the AD7722. The optimum resistor will depend on the board layout and the impedance of the trace connecting to the clock input.

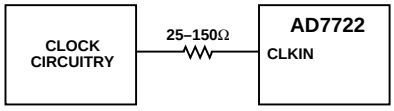


Figure 37. External Clock Oscillator Connection

A low phase-noise clock should be used to generate the ADC sampling clock because sampling clock jitter effectively modulates the input signal and raises the noise floor. The sampling clock generator should be isolated from noisy digital circuits, grounded and heavily decoupled to the analog ground plane.

The sampling clock generator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multipurpose system clock that is generated on the digital ground plane. If the clock signal is passed between its origin on a digital ground plane to the AD7722 on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics.

This can be remedied somewhat by transmitting the sampling clock signal as a differential one, using either a small RF transformer or a high speed differential driver and receiver such as PECL. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

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Varying the Master Clock

Although the AD7722 is specified with a master clock of 12.5 MHz, the AD7722 operates with clock frequencies up to 15 MHz and as low as 300 kHz. The input sample rate, output word rate, and the frequency response of the digital filter are directly proportional to the master clock frequency. For example, reducing the clock frequency to 5 MHz leads to an analog input sample rate of 10 MHz, an output word rate of 78.125 kSPS, a pass-band frequency of 36.25 kHz, a cutoff frequency of 38.77 kHz, and a stop band frequency of 41.875 kHz.

SYSTEM SYNCHRONIZATION AND CONTROL

The AD7722 digital filter contains a sequencer block that controls the digital interface and all the control logic needed to operate the digital filter. A 14-bit cycle counter keeps track of where the filters are in their overall operating cycle and decodes the digital interface signals to the AD7722. The cycle counter has a number of important transition points. In particular, the bottom six bits control the convolution counter that decimates by 64 to the update rate of the output data register. The counter's top bit is used to provide ample time (8192 CLKIN cycles) to allow the modulator and digital filter to settle as the AD7722 sequences through its autocalibration process. The counter increments on the rising edge of the signal at the CLKIN pin and all of the digital I/O signals are synchronous with this clock. The upper bit of this counter also controls when DVAL or DRDY indicates valid data is available in the output data register after a SYNC, RESET, CAL or an initial FSI. During normal operation the delay of 128 conversion (8192 CLKIN cycles) should not be confused with actual settling time (5376 CLKIN cycles) and group delay (2688 CLKIN cycles) of the of the digital filter.

SYNC Input

The SYNC input provides a synchronization function for use in parallel or serial mode. SYNC allows the user to start gathering samples of the analog input from a known point in time. This allows a system using multiple AD7722s, operated from a common master clock, to be synchronized so that each ADC updates its output register simultaneously. The SYNC input resets the digital filter without affecting the contents of the calibration registers.

In a system using multiple AD7722s, a common signal to their sync input will synchronize their operation. On the rising edge of SYNC, the digital filter sequencer counter is reset to zero. The filter is held in a reset state until a rising edge on CLKIN senses SYNC low. A SYNC pulse, one CLKIN cycle long, can be applied synchronous to the falling edge of CLKIN. This way, on the next rising edge of CLKIN, SYNC is sensed low, the filter is taken out of its reset state and multiple parts start to gather input samples.

In serial mode DVAL remains low for 8192 CLKIN cycles to allow the modulator and digital filter to settle. In parallel mode DRDY remains high for an additional 64 CLKIN cycles when valid data is loaded into the output register. After a SYNC, conversion data is not valid until the digital filter settles (reference Figure 7).

DVAL

The DVAL pin, when used in the serial mode, indicates if invalid data may be present at the ADC output. There are four events which can cause DVAL to be deasserted and they have different implications for how long the results should be considered invalid.

DVAL is set low if there is an overflow condition in the first stage of the digital filter. The overflow can result from an analog input signal nearly twice the allowable maximum input span. When an overflow condition is detected, DVAL is set low for 64 CLKIN cycles, (one output period) and the output data is clipped to either positive or negative full scale depending on the sign of the overflow. After the next convolution is completed (64 CLKIN cycles), if the overflow condition does not exist, DVAL goes high to indicate a valid output is available. Otherwise DVAL will remain low until the overflow condition is eliminated.

The second stage digital filter can overflow as a result of overflow from the first stage. The overflow condition is detected when the second stage filter calculates a conversion result that exceeds either plus or minus full scale (i.e., below –32,768 or above 32,767 in bipolar mode). When the overflow is detected, DVAL is set low, and the output register is updated with either positive or negative full scale, depending on the sign of the overload. After the next convolution is completed, DVAL returns high if the next conversion result is within the full-scale range.

As with all high order sigma-delta modulators, large overloads on the analog input can cause the modulator to go unstable. The modulator is designed to be stable with input signals as high as twice full scale within the input bandwidth. Out of band signals as high as the full-scale range will not cause instability. When instability is detected by internal circuits, DVAL is set low, and the output is clipped to either positive or negative full scale depending on the polarity of the overload. The modulator is reset to a stable state, and the digital filter sequencer counter is reset. DVAL is set low for a minimum of 8192 CLKIN cycles while the modulator settles out, and the digital filter accumulates new samples. DVAL returns high to indicate valid data is available from the serial output register 8192 CLKIN cycles after the overload condition is removed.

Lastly, DVAL also indicates when valid data is available at the serial interface after initial power-up or upon completion of a CAL, RESET or SYNC sequence.

Reset Input

The AD7722 RESET input controls the digital filter the same as the SYNC input described above. Additionally, it resets the modulator by shorting its integrator capacitors and clears the on-chip calibration registers so that the conversion results are not corrected for offset or gain error.

Power-On Reset

A power-on reset function is provided to reset the AD7722 internal logic after initial power-up. On power-up the offset and gain calibration registers are cleared.

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Offset and Gain Calibration

A calibration of offset and gain errors can be performed in both serial and parallel modes by initiating a calibration cycle. During this cycle, offset and gain registers in the filter are loaded with values representing the dc offset of the analog modulator and a modulator gain correction factor. The correction factors are determined by an on-chip microcontroller measuring the conversion results for three different input conditions: minus full scale (–FS), plus full scale (+FS), and midscale. In normal operation, the offset register is subtracted from the digital filter output, and this result is then multiplied by the gain correction factor to obtain an offset and gain corrected final result.

The calibration cycle is controlled by internal logic, and the user need only initiate the cycle. A calibration is initiated when the rising edge of CLKIN senses a high level on the CAL input. There is an uncertainty of up to 64 CLKIN cycles before the calibration cycle actually begins because the current conversion must complete before calibration commences. The calibration values loaded into the registers only apply for the particular analog input mode (bipolar/unipolar) selected when initiating the calibration cycle. On changing to a different analog input mode, a new calibration must be performed.

During the calibration cycle, in unipolar mode, the offset of the analog modulator is evaluated; the differential inputs to the modulator are shorted internally to AGND. Once calibration begins, DVAL goes low and $\overline{DRDY}$ goes high indicating there is invalid data in the output register. After 8192 CLKIN cycles, when the modulator and digital filter settle, the average of eight output results (512 CLKIN cycles) is calculated and stored in the offset register. In unipolar mode, this result also represents minus full scale, required to calculate the gain correction factor. The gain correction factor can then be determined by internally switching the inputs to +FS (V_{REF2}). The positive input of the modulator is switched to the reference voltage and the negative input to AGND. Again, when the modulator and digital filter settle, the average of the eight output results is used to calculate the gain correction factor.

In bipolar mode, an additional measurement is required since zero scale is not the same as –FS. Therefore, calibration in bipolar mode requires an additional 8704 CLKIN cycles. Zero scale is similarly determined by shorting both analog inputs to AGND. Then the inputs are internally reconfigured to apply +FS and –FS ($+V_{REF2}/2$ and $-V_{REF2}/2$) to determine the gain correction factor.

After the calibration registers have been loaded with new values, the inputs of the modulator are switched back to the input pins. However, correct data is available at the interface only after the modulator and filter have settled to the new input values.

Should the part see a rising edge on the SYNC or RESET pin during a calibration cycle, the calibration cycle is discontinued, and a synchronization operation or reset will be performed.

The calibration registers are static. They need to be updated only if unacceptable drifts in analog offsets or gain are expected. After power-up, a RESET is not mandatory since power-on reset circuitry clears the offset and gain registers. Care must be taken to ensure the CAL pin is held low during power-up. Before initiating a calibration routine, ensure the supplies and reference input have settled, and that the voltage on the analog input pins is between the supply voltages.

DATA INTERFACING

The AD7722 offers a choice of serial or parallel data interface options to meet the requirements of a variety of system configurations. In parallel mode, multiple AD7722s can be easily configured to share a common data bus. Serial mode is ideal when it is required to minimize the number of data interface lines connected to a host processor. In either case, careful attention to the system configuration is required to realize the high dynamic range available with the AD7722. Consult the recommendations in the "Power Supply Grounding and Layout" section. The following recommendations for parallel interfacing also apply for the system design in serial mode.

Parallel Interface

When using the AD7722, place a buffer/latch adjacent to the converter to isolate the converter's data lines from any noise which may be on the data bus. Even though the AD7722 has three-state outputs, use of an isolation latch represents good design practice. This arrangement will inject a small amount of digital noise on the AD7722 ground plane; these currents should be quite small and can be minimized by ensuring that the converter input/output does not drive a large fanout (they normally can't by design). Minimizing the fanout on the AD7722's digital port will also keep the converter logic transitions relatively free from ringing and thereby minimize any potential coupling into the analog port of the converter.

The simplified diagram (Figure 38) shows how the parallel interface of the AD7722 can be configured to interface with the system data bus of a microprocessor or a modern microcontroller such as the MC68HC16 or 8XC251.

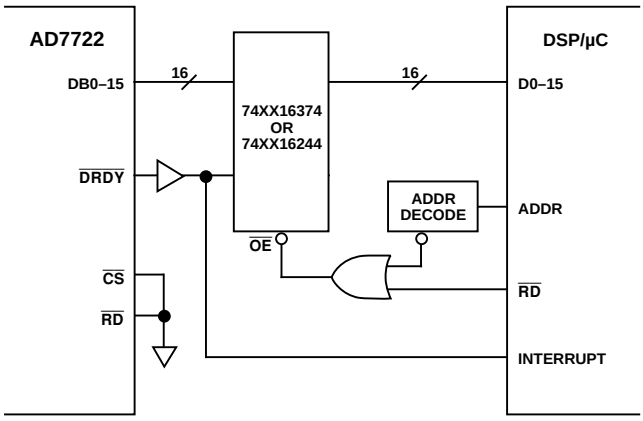


Figure 38. Parallel Interface Connection

With $\overline{CS}$ and $\overline{RD}$ tied permanently low the data output bits are always active. When the $\overline{DRDY}$ output goes high for two CLKIN cycles, the rising edge of $\overline{DRDY}$ is used to latch the conversion data before a new conversion result is loaded into the output data register. The falling edge of $\overline{DRDY}$ then sends an appropriate interrupt signal for interface control. Alternatively if buffers are used instead of latches the falling edge of $\overline{DRDY}$ provides the necessary interrupt when a new output word is available from the AD7722.

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SERIAL INTERFACE

The AD7722's serial data interface port allows easy interfacing to industry standard digital signal processors. The AD7722 operates solely in the master mode providing three serial data output pins for transfer of the conversion results. The serial data clock output (SCO), serial data output (SDO) and frame sync output (FSO) are all synchronous with CLKIN. SCO frequency is always one-half the CLKIN frequency. FSO is continuously output at the conversion rate of the ADC (FCLKIN/64). The generalized timing diagrams in Figure 2 show how the AD7722 may be used to transmit its conversion results.

Serial data shifts out of the SDO pin synchronous with SCO. The FSO is used to frame the output data transmission to an external device. An output data transmission is 32 SCO cycles in duration. The serial data shifts out of the SDO pin MSB first, LSB last for a duration of 16 SCO cycles. For the next 16 SCO cycles SDO outputs zeros.

Two control inputs, SFMT and CFMT, select the format for the serial data transmission. FSO is either a pulse (approximately one SCO cycle in duration) or a square wave with a period of 32 SCO cycles, depending on the state of the SFMT. The logic level applied to SFMT also determines if the serial data is valid on the rising or falling edge of the SCO. The clock format pin, CFMT, simply switches the phase of SCO for the selected FSO format.

With a logic low level on SFMT and CFMT set low (Figure 4), FSO pulses high for one SCO cycle at the beginning of a data transmission frame. When FSO goes low, the MSB is available on the SDO pin after the rising edge of SCO and can be latched on the SCO falling edge.

With a logic high level on SFMT and CFMT set low (Figure 4), the data on the SDO pin is available after the falling edge of SCO and can be latched on the SCO rising edge. FSO goes low at the beginning of a data transmission frame when the MSB is available and returns high after 16 SCO cycles.

The Frame Sync Input (FSI) can be used if the AD7722 conversion process must be synchronized to an external source. FSI is an optional signal; if FSI is grounded or tied high frame, syncs are internally generated. Frame sync allows the conversion data presented to the serial interface to be a filtered and decimated result derived from a known point in time. FSI can be applied once after power-up, or it can be a periodic signal, synchronous to CLKIN, occurring every 64 CLKIN cycles. When FSI is applied for the first time, or if a low to high transition is detected that is not synchronized to the output word rate, the next 127 conversions should be considered invalid while the digital filter accumulates new samples. Figure 4 shows how the frame sync signal resets the serial output interface and how the AD7722 will begin to output its serial data transmission frame. A common frame sync signal can be applied to two or more AD7722s to synchronize them to a common master clock.

Two Channel Multiplexed Operation

Three additional serial interface control pins (DOE, TSI and CFMT) are provided. The connection diagram in Figure 39 shows how they are used to allow the serial data outputs of two AD7722s to easily share one serial data line. Since a serial data transmission frame lasts 32 SCO cycles, two AD7722s can share a single data line by alternating transmission of their 16-bit output data onto one SDO pin.

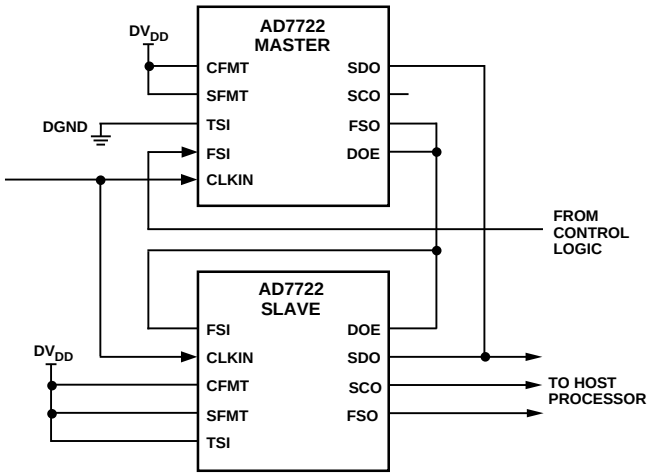


Figure 39. Connection for Two Channel Multiplexed Operation

The Data Output Enable pin (DOE) controls SDO's output buffer. When the logic level on DOE matches the state of the TSI pin, the SDO output buffer drives the serial dataline; otherwise the output of the buffer goes high impedance. The serial format pin (SFMT) is set high to chose the frame sync output format. The clock format pin (CFMT) is set high so that

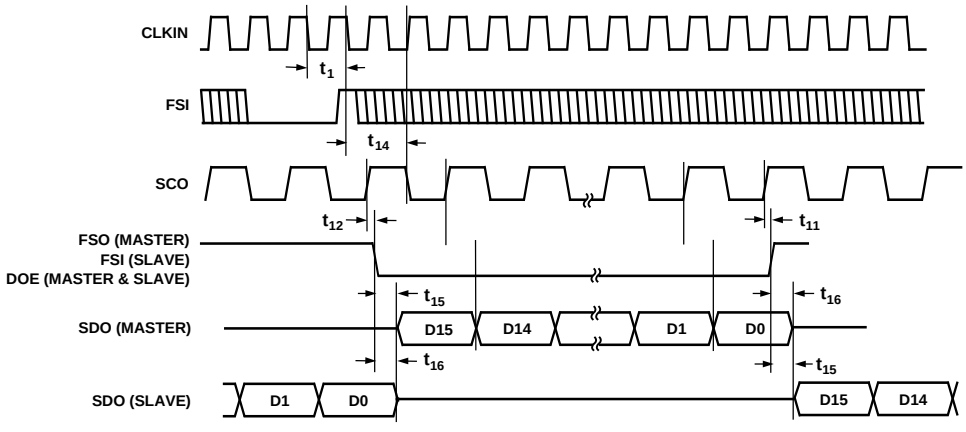


Figure 40. Timing for Two Channel Multiplexed Operation

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serial data is made available on SDO after the rising edge of SCO and can be latched on the SCO falling edge.

The master device is selected by setting TSI to a logic low and connecting its FSO to DOE. The slave device is selected with its TSI pin tied high, and both its FSI and DOE are controlled from the master's FSO. Since the FSO of the master controls the DOE input of both the master and slave, one ADCs SDO is active while the other is high impedance (Figure 40). When the master transmits its conversion result during the first 16 SCO cycles of a data transmission frame, the low level on DOE sets the slave's SDO high impedance. Once the master completes transmitting its conversion data, its FSO goes high and triggers the slave's FSI to begin its data transmission frame.

Serial Interfacing to DSPs

In serial mode, the AD7722 can be interfaced directly to several industry standard DSPs. In all cases, the AD7722 operates as the master with the DSP operating as the slave. The AD7722 outputs its own serial clock (SCO) to transmit the digital word on the SDO pin to a DSP. The DSP's serial interface is synchronized to the data transmission provided by the FSO signal.

Since the serial data clock from the AD7722 is always one-half the CLKIN frequency, DSPs that can accept relatively high serial clock frequencies are required. The ADSP-21xx family of DSPs can operate with a maximum serial clock of 13.824 MHz; the DSP56002 allows a maximum serial clock of 13.3 MHz; while the TMS320C5x-57 accepts a maximum serial clock of 10.989 MHz. To interface the AD7722 to other DSPs, the master clock frequency of the AD7722 can be reduced so that the SCO frequency equals the maximum allowable frequency of the serial clock input to the DSP. When the AD7722 is operated with a lower CLKIN frequency (< 10 MHz), DSPs such as the TMS320C20/C25 and DSP56000/1 can be used.

Figures 41 to 43 show the interfaces between the AD7722 and several DSPs. In all cases, the interface control pins, TSI, DOE, SFMT, CFMT, SYNC, and FSI can be permanently hardwired together to either DGND or DVDD. Alternatively, SFMT or CFMT can be tied either high or low to configure the serial data interface for the particular format required by the DSP. The frame synchronization signal, FSI, can be applied from the user's system control logic.

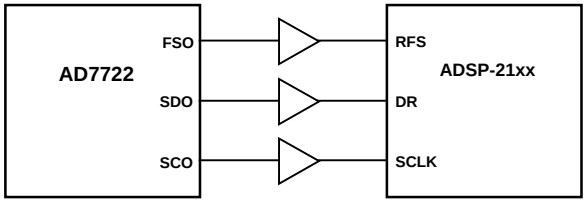


Figure 41. AD7722 to ADSP-21xx Interface

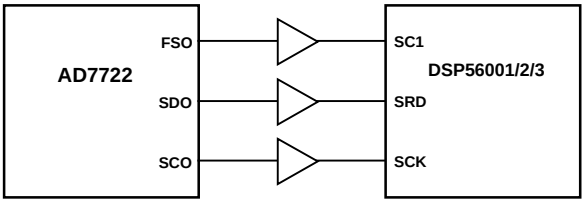


Figure 42. AD7722 to DSP56000 Interface

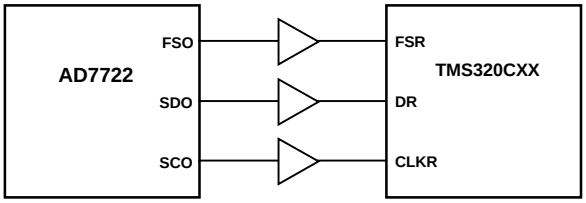


Figure 43. AD7722 to TMS320C20/25/50 Interface

Grounding and Layout

The analog and digital power supplies to the AD7722 are independent and separately pinned out to minimize coupling between analog and digital sections within the device. The AD7722 should be treated as an analog component and grounded and decoupled to the analog ground plane. All the AD7722 ground pins should be soldered directly to a ground plane to minimize series inductance. All converter power pins should be decoupled to the analog ground plane. To achieve the best decoupling, place surface mount capacitors as close as possible to the device, ideally right up against the device pins.

The printed circuit board that houses the AD7722 should use separate ground planes for the analog and the digital interface circuitry. All converter power pins should be decoupled to the analog ground plane, and all interface logic circuit power pins should be decoupled to the digital ground plane. This facilitates the use of ground planes, which can physically separate sensitive analog components from the noisy digital system. Digital and analog ground planes should only be joined in one place and should not overlap to minimize capacitive coupling between them.

Separate power supplies for AVDD and DVDD are also highly desirable. The digital supply pin DVDD should be powered from a separate analog supply, but if necessary DVDD may share its power connection to AVDD. Refer to the connection diagram (Figure 44). The 10 Ω resistor, in series with the DVDD pin, is required to dampen the effects of the fast switching currents into the digital section of the AD7722. The ferrite is also recommended to filter high frequency signals from corrupting the analog power supply.

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A minimum etch technique is generally best for ground planes because it gives the best shielding. Noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. In waveform sampling and reconstruction systems, the sampling clock (CLKIN) is as vulnerable to noise as any analog signal. CLKIN should be isolated from the analog and digital systems. Fast switching signals like clocks should be shielded with their associated ground to avoid radiating noise to other sections of the board, and clock signals should never be routed near the analog inputs.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7722 to shield it from noise coupling. The power supply lines to the AD7722 should use as large a trace as possible (preferably a plane) to provide a low impedance path and reduce the effects of glitches on the power supply line. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board.

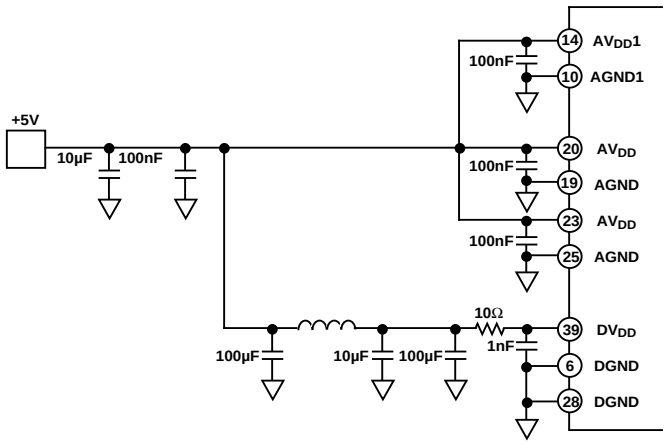
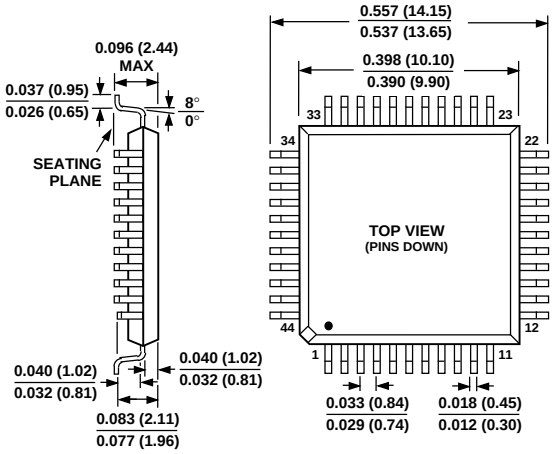


Figure 44. Power Supply Decoupling

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Pin PQFP
(S-44)



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Appendix B: Burr/Brown PGA207 – High–Speed Programmable Gain Instrumentation Amplifier

B.1 Burr/Brown PGA207

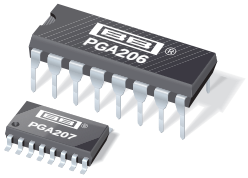
The following pages are a reprint of the Burr/Brown PGA207 High–Speed Programmable Gain Instrumentation Amplifier Data Sheet.

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BURR - BROWN®



PGA206
PGA207

High-Speed Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- DIGITALLY PROGRAMMABLE GAINS:
  PGA206: G=1, 2, 4, 8V/V
  PGA207: G=1, 2, 5, 10V/V
- TRUE INSTRUMENTATION AMP INPUT
- FAST SETTLING: 3.5µs to 0.01%
- FET INPUT: I_B = 100pA max
- INPUT PROTECTION: ±40V
- LOW OFFSET VOLTAGE: 1.5mV max
- 16-PIN DIP, SOL-16 SOIC PACKAGES

APPLICATIONS

- MULTIPLE-CHANNEL DATA ACQUISITION
- MEDICAL, PHYSIOLOGICAL AMPLIFIER
- PC-CONTROLLED ANALOG INPUT BOARDS

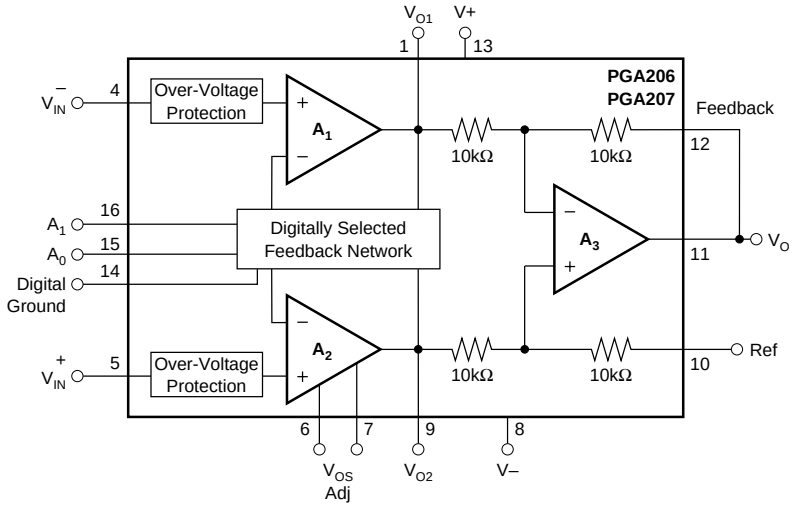
DESCRIPTION

The PGA206 and PGA207 are digitally programmable gain instrumentation amplifiers that are ideally suited for data acquisition systems.

The PGA206 and PGA207's fast settling time allows multiplexed input channels for excellent system efficiency. FET inputs eliminate I_B errors due to analog multiplexer series resistance.

Gains are selected by two CMOS/TTL-compatible address lines. Analog inputs are internally protected for overloads up to ±40V, even with the power supplies off. The PGA206 and PGA207 are laser-trimmed for low offset voltage and low drift.

The PGA206 and PGA207 are available in 16-pin plastic DIP and SOL-16 surface-mount packages. Both are specified for –40°C to +85°C operation.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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PDS-1241B
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SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	PGA206P, U PGA207P, U MIN	PGA206P, U PGA207P, U TYP	PGA206P, U PGA207P, U MAX	PGA206PA, UA PGA207PA, UA MIN	PGA206PA, UA PGA207PA, UA TYP	PGA206PA, UA PGA207PA, UA MAX	UNITS
INPUT								
Offset Voltage, RTI	All Gains							
Initial	T_A = +25°C		±0.5	±1.5		±1	±2.5	mV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}, G = 8, 10		±2			*		µV/°C
vs Power Supply	V_S = ±4.5V to ±18V		±5	±20		±10	±40	µV/V
Long-Term Stability			4.5			*		µV/mo
Impedance, Differential			10^{13} || 1			*		Ω || pF
Common-Mode			10^{12} || 4			*		Ω || pF
Common-Mode Voltage Range[1]	V_O = 0V	±($\|V_S\|$–4)	±($\|V_S\|$ –2.5)		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±11V, ΔR_S = 1kΩ							
	G = 1	80	92		75	86		dB
	G = 2	85	96		80	90		dB
	G = 4 or 5	90	100		84	94		dB
	G = 8 or 10	95	100		84	94		dB
INPUT BIAS CURRENT	V_{IN} = 0		2	100		*	*	pA
vs Temperature			See Typical Curve			*		
Offset Current			1	100		*	*	pA
vs Temperature			See Typical Curve			*		
NOISE VOLTAGE, RTI	G = 8,10; R_S = 0Ω							
f = 10Hz			30			*		nV/√Hz
f = 100Hz			20			*		nV/√Hz
f = 1kHz			18			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*		µVp-p
Noise Current								
f = 1kHz			1.5			*		fA/√Hz
GAIN	All Gains, V_O = ±11V							
Gain Error			±0.01	±0.05		*	±0.1	%
Gain vs Temperature[2]			±1	±10		*	*	ppm/°C
Nonlinearity			±0.0003	±0.002		*	±0.005	% of FSR
OUTPUT								
Voltage, Positive		(V+) –4	(V+) –2.3		*	*		V
Negative		(V–) +4	(V–) +1.5		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			±17			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		5			*		MHz
	G = 2		4			*		MHz
	G = 4, 5		1.3			*		MHz
	G = 8, 10		600			*		kHz
Slew Rate	V_O = ±10V, G = 1 to 10		25			*		V/µs
Settling Time, 0.1%	20V Step, All Gains		2			*		µs
0.01%	20V Step, All Gains		3.5			*		µs
Output Overload Recovery	50% Overdrive		1.5			*		µs
DIGITAL LOGIC INPUTS								
Digital Ground Voltage, V_{DG}		V–		(V+) –4	*		*	V
Digital Low Voltage		V–		V_{DG} + 0.8V	*		*	V
Digital Input Current			1			*		pA
Digital High Voltage		V_{DG}+2		V+	*		*	V
Gain Switching Time			500			*		ns
POWER SUPPLY								
Voltage Range		±4.5	±15	±18	*	*	*	V
Current	V_{IN} = 0V		+12.4/–11.2	±13.5		*		mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
Thermal Resistance, θ_{JA}			80			*		°C/W

* Specification same as PGA206P or PGA207P.

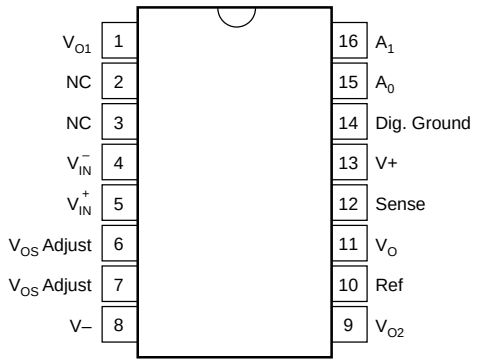
NOTES: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

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PIN CONFIGURATION

Top View **DIP SOL-16**



NC: No Internal Connection

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
PGA206PA	16-Pin Plastic DIP	180
PGA206P	16-Pin Plastic DIP	180
PGA206UA	SOL-16 Surface Mount	211
PGA206U	SOL-16 Surface Mount	211
PGA207PA	16-Pin Plastic DIP	180
PGA207P	16-Pin Plastic DIP	180
PGA207UA	SOL-16 Surface Mount	211
PGA207U	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Logic Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

ORDERING INFORMATION

PRODUCT	GAINS	PACKAGE	TEMPERATURE RANGE
PGA206PA	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206P	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206UA	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA206U	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207PA	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207P	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207UA	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207U	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

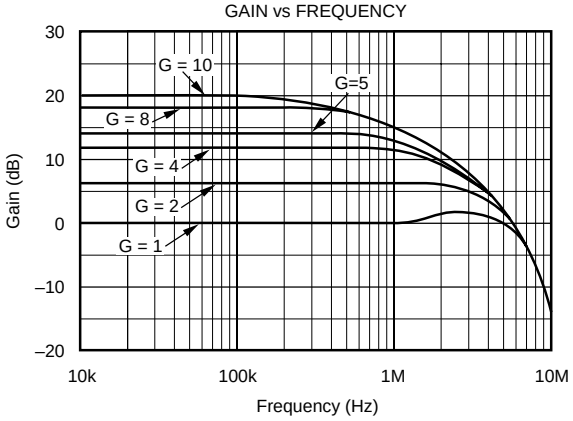
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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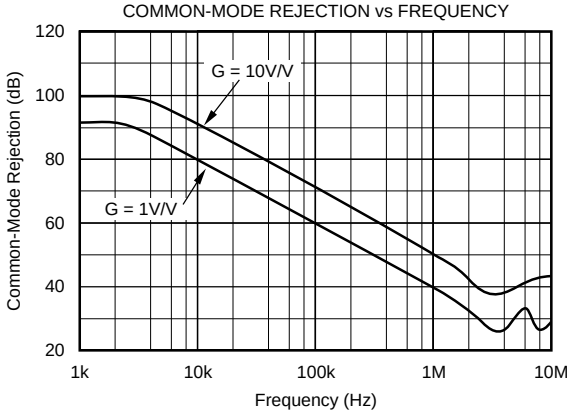
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

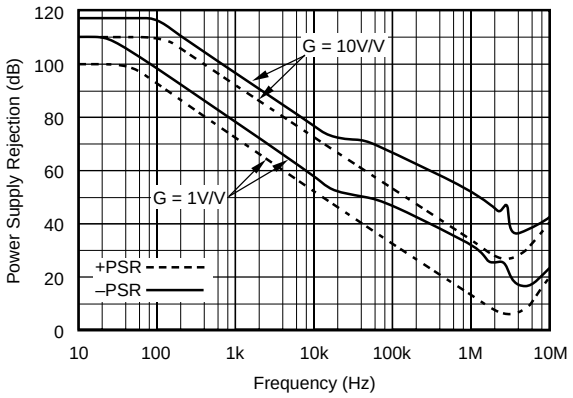
GAIN vs FREQUENCY



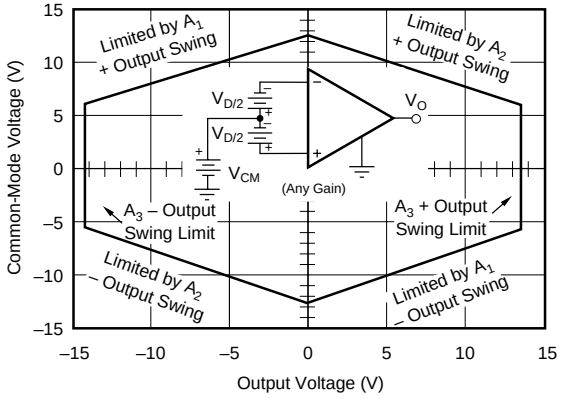
COMMON-MODE REJECTION vs FREQUENCY



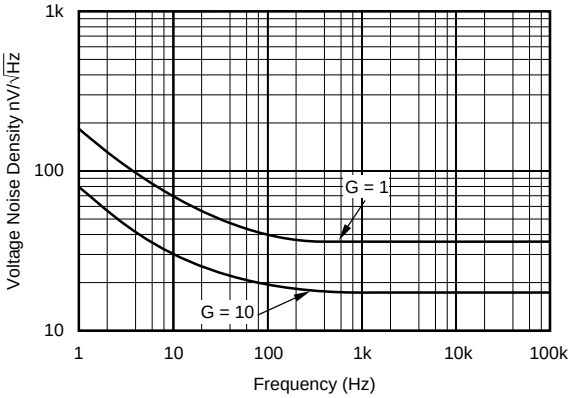
POWER SUPPLY REJECTION vs FREQUENCY



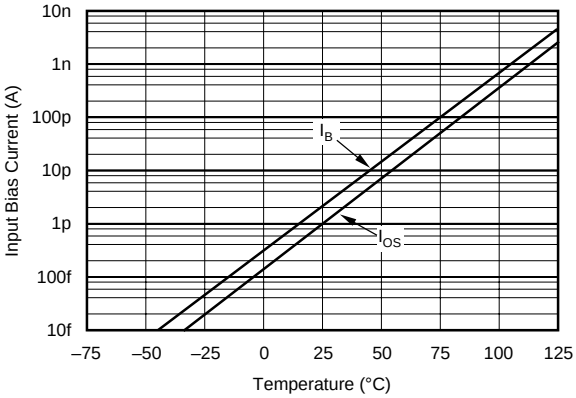
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



INPUT VOLTAGE NOISE vs FREQUENCY



INPUT BIAS CURRENT vs TEMPERATURE

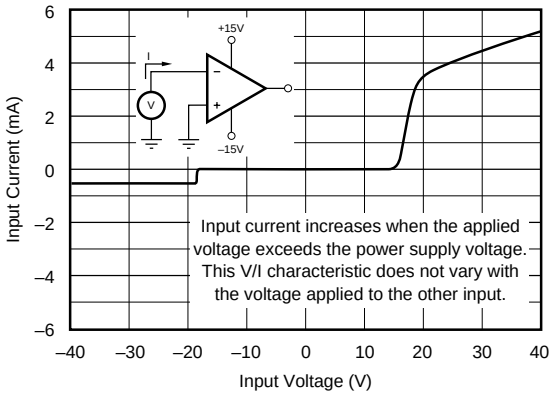


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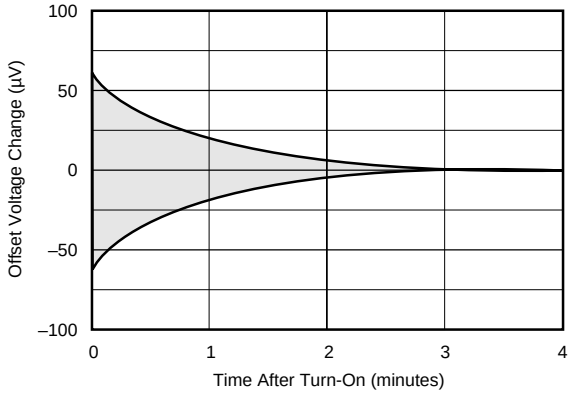
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

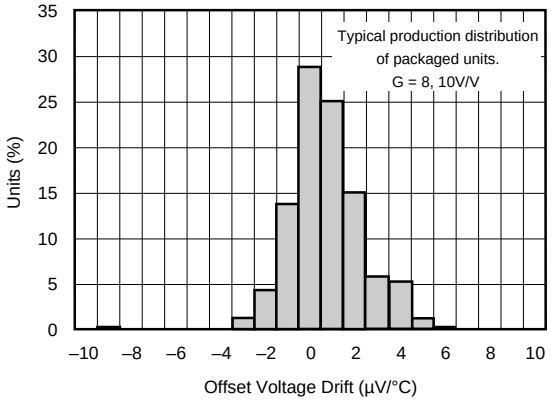
INPUT OVER-VOLTAGE V/I CHARACTERISTIC



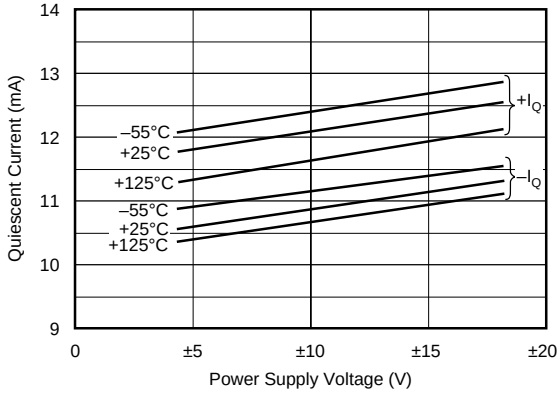
OFFSET VOLTAGE WARM-UP TIME



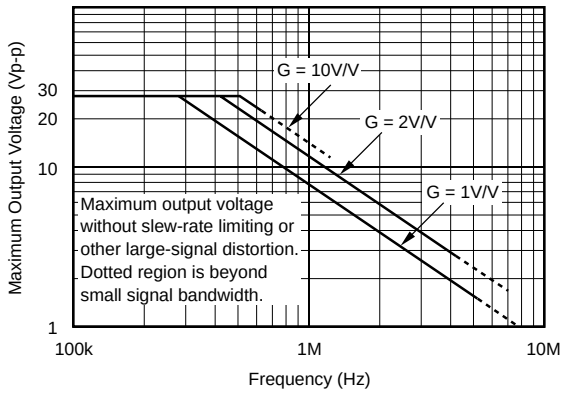
OFFSET VOLTAGE TEMPERATURE DRIFT PRODUCTION DISTRIBUTION



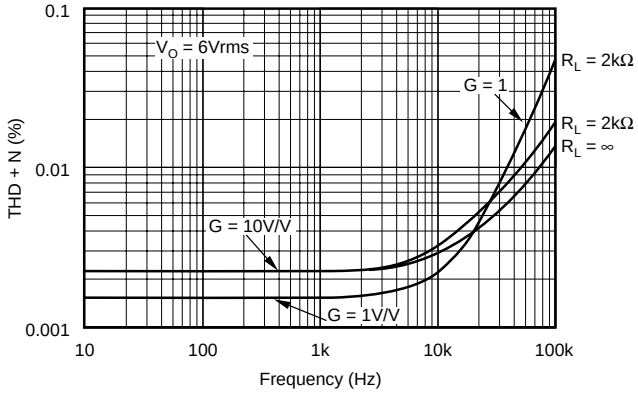
QUIESCENT CURRENT vs POWER SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

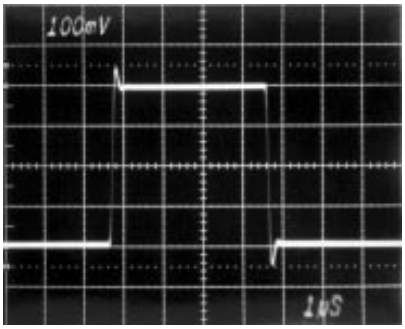


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TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

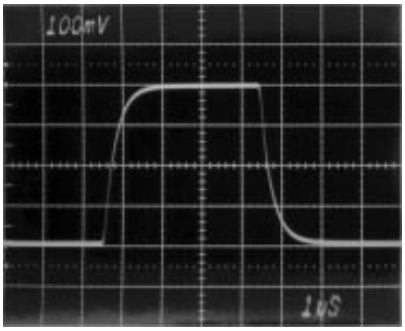
SMALL SIGNAL RESPONSE
G = 1, C_L = 50pF



100mV/div

1µs/div

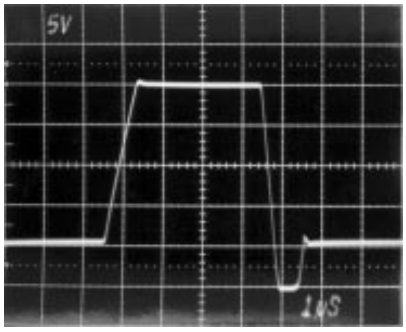
SMALL SIGNAL RESPONSE
G = 10, C_L = 50pF



100mV/div

1µs/div

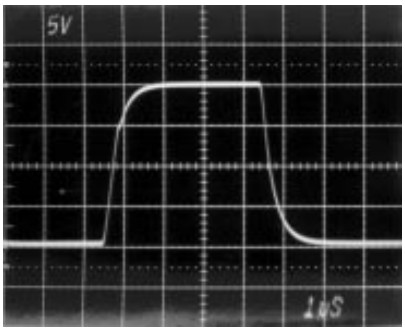
LARGE SIGNAL RESPONSE
G = 1, C_L = 50pF



5V/div

1µs/div

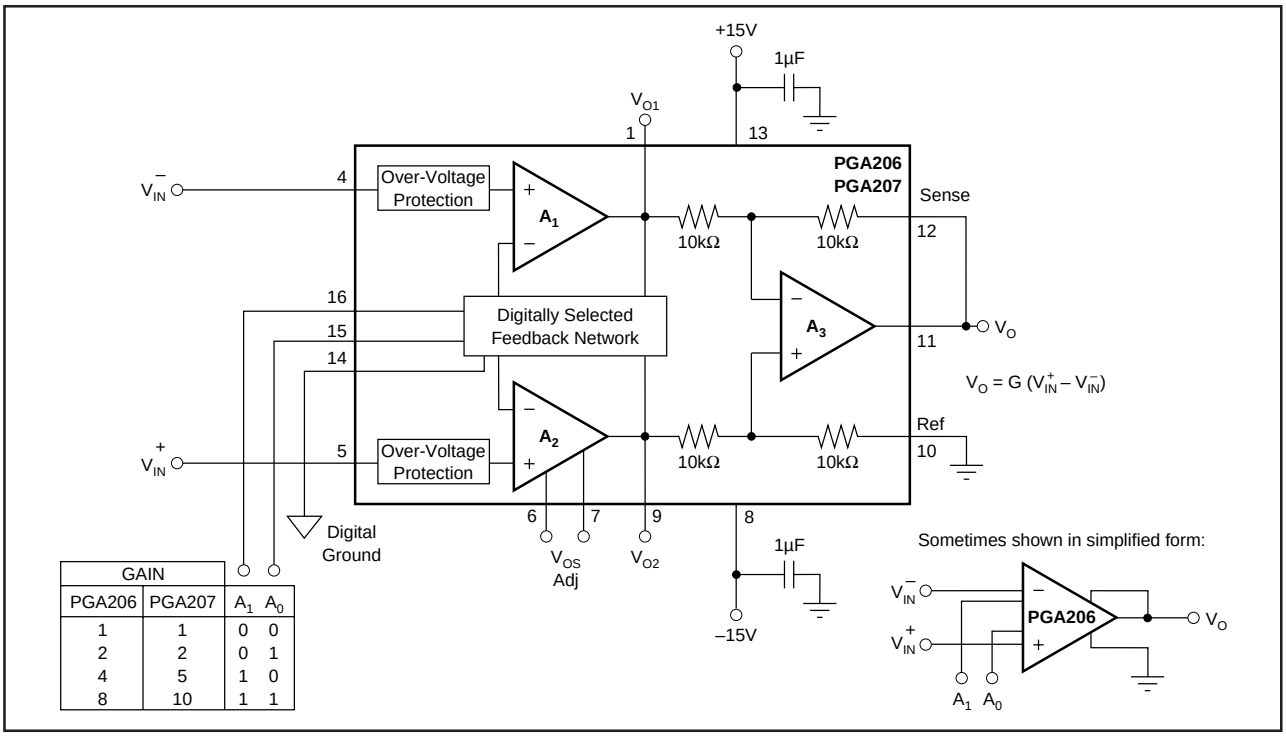
LARGE SIGNAL RESPONSE
G = 10, C_L = 50pF



5V/div

1µs/div

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GAIN			
PGA206	PGA207	A_1	A_0
1	1	0	0
2	2	0	1
4	5	1	0
8	10	1	1

FIGURE 1. Basic Connections.

APPLICATIONS INFORMATION

Figure 1 shows the circuit diagram for basic operation of the PGA206 or PGA207. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 2Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The output sense connection (pin 12) must be connected to the output terminal (pin 11) for proper operation. This connection can be made at the load for best accuracy.

DIGITAL INPUTS

The digital inputs A_0 and A_1 select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential ranging from the V– power supply to 4V less than V+. Digital ground is usually equal to analog ground potential and the two grounds are connected at the power supply. The digital inputs interface directly to CMOS and TTL logic.

A nearly constant current of approximately 1.2mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs, A_0 and A_1, are not latched. A change in logic input immediately selects a new gain. Switching time of the logic is approximately 500ns. The time to respond to gain change is equal to switching time, plus the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to acquire gain control data from a high speed digital bus. Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the digital latch as far as practical from analog circuitry to avoid coupling digital noise into analog input circuitry.

OFFSET VOLTAGE ADJUSTMENT

The PGA206 and PGA207 are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment. Multiplexed data acquisition systems generally correct offset by grounding the inputs of one channel to measure offset voltage. Stored offset values for each gain are then subtracted from subsequent readings of other channels.

Figure 2 shows optional offset voltage trim circuits. Offset voltage changes with the selected gain. To adjust for low offset voltage in all gains, both input and output offsets must be trimmed.

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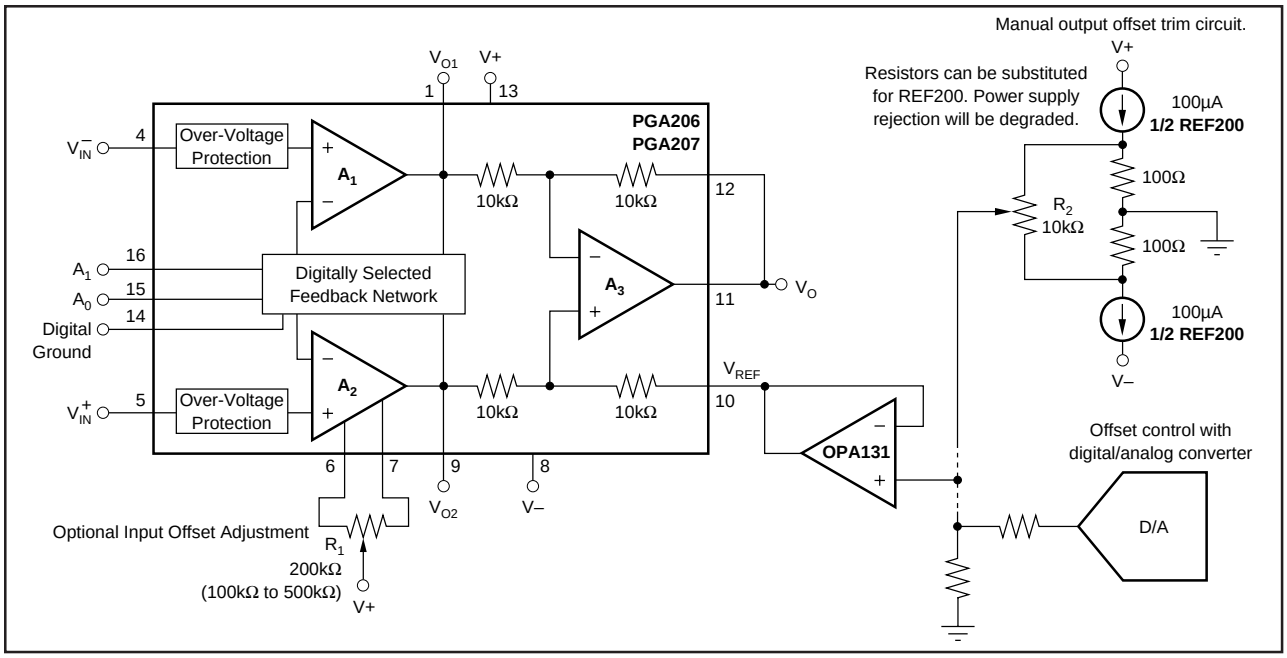


FIGURE 2. Optional Offset Voltage Trim Circuits.

R_1 adjusts the offset of the input amplifiers. Output stage offset is adjusted with R_2. A buffer op amp is required in the output offset adjustment circuit, as shown, to assure that the Ref pin is driven by a low source impedance. To adjust for low offset voltage in all gains, first adjust the input stage offset in the highest gain. Then adjust the output stage offset (R_2) in G = 1. Iterate the adjustments for lowest offset in all gains.

Offset can also be adjusted under processor control with a D/A converter as shown in Figure 2. The D/A's output voltage can be reduced with a resistor divider for better adjustment resolution, but an op amp buffer following the divider is required to provide a low source impedance to the ref terminal. A different offset value is required for each amplifier gain.

INPUT BIAS CURRENT RETURN PATH

The FET inputs of the PGA206 and PGA207 provide extremely high input impedance. Still, a path must be provided for the bias current of each input. Figure 3 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the linear input voltage range and the input amplifiers will saturate.

If the differential source resistance is low, a bias current return path can be connected to only one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 3). These applications do not require additional resistor(s) for proper operation.

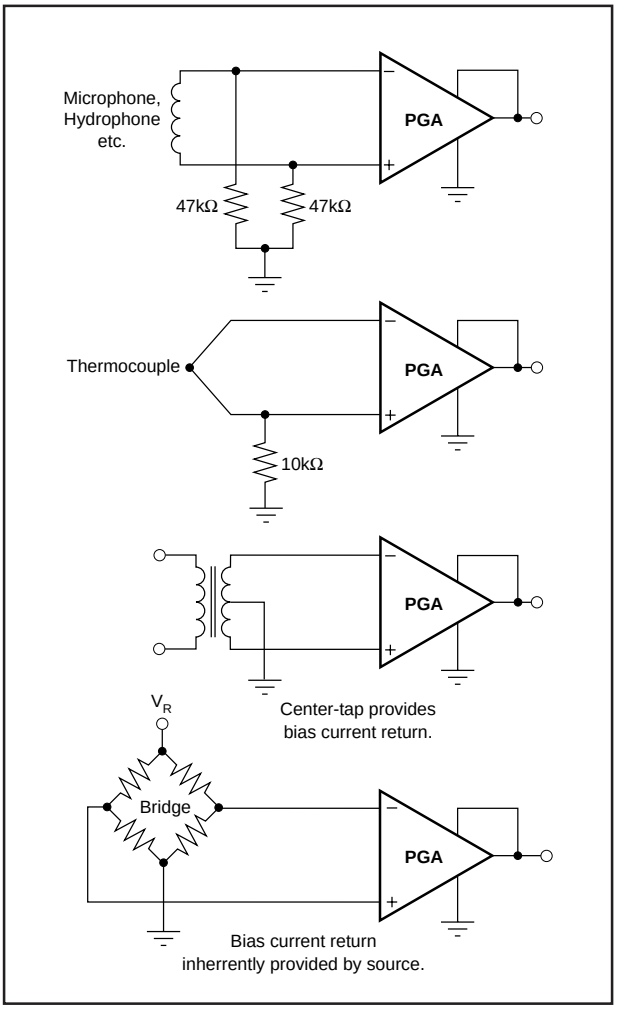


FIGURE 3. Providing an Input Bias Current Path.

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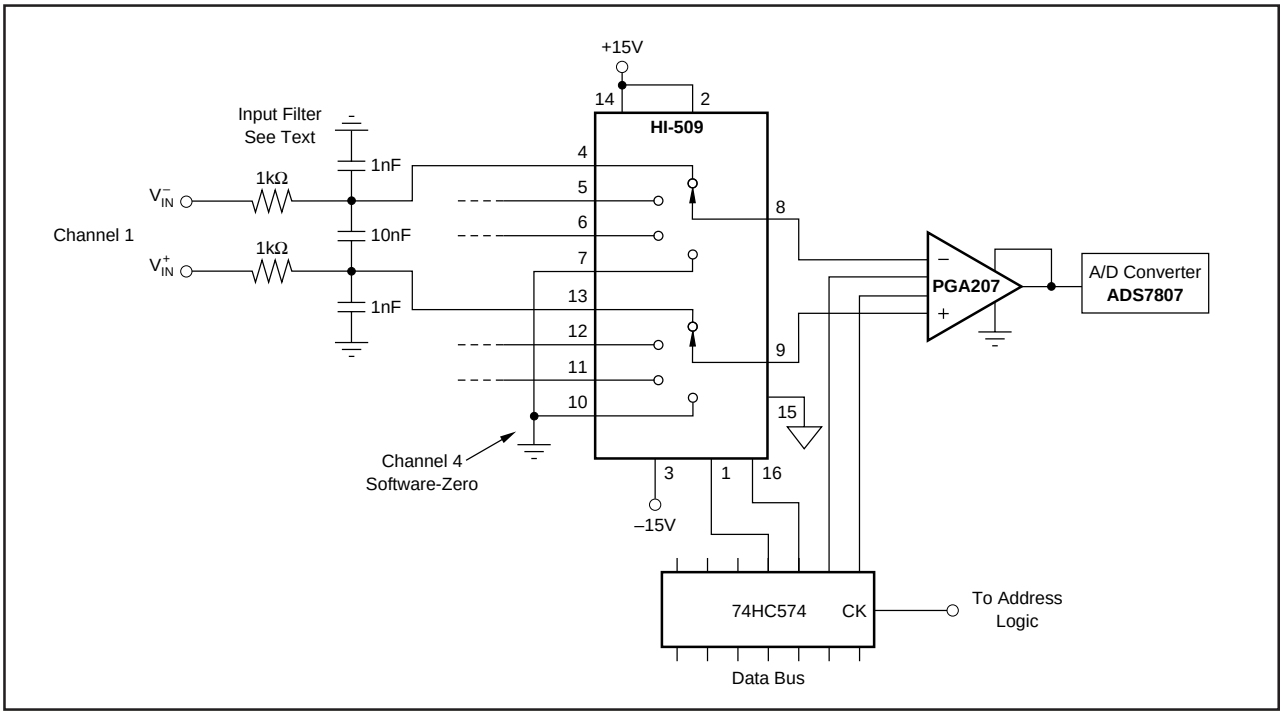


FIGURE 4. Multiplexed-Input Signal Acquisition System.

INPUT COMMON-MODE RANGE

The linear input voltage range of the PGA206 and PGA207 is from approximately 2.3V below the positive supply voltage to 1.5V above the negative supply. As a differential input voltage causes output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA206 or PGA207 will be near 0V even though both inputs are overloaded. This condition can be detected by sensing the voltage on the V_{01} and V_{02} pins to determine whether they are within their linear operating range.

INPUT PROTECTION

The inputs of the PGA206 and PGA207 are individually protected for voltages up to ±40V. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value. The typical performance curve "Input Overload V/I Characteristic" shows this behavior. The inputs are protected even if no power supply voltage is applied.

MULTIPLEXED INPUTS

The PGA206 and PGA207 are ideally suited for multiple channel data acquisition. Figure 4 shows a typical application with an analog multiplexer used to connect one of four differential input signals to a single PGA207.

Careful circuit layout will help preserve accuracy of multiplexed signals. Run the inverting and non-inverting connections of each channel parallel to each other over a ground plane, or directly adjacent on top and bottom of the circuit board. Grounded guard traces between channels help reduce stray signal pick-up.

Multiplexed signals from high impedance sources require special care. As inputs are switched by the multiplexer, charge can be injected into the source, disturbing the input signal. Since many such sources involve slow signals, a simple R/C filter at the input can be used to dramatically reduce this effect. The arrangement shown filters both the differential signal and common-mode noise.

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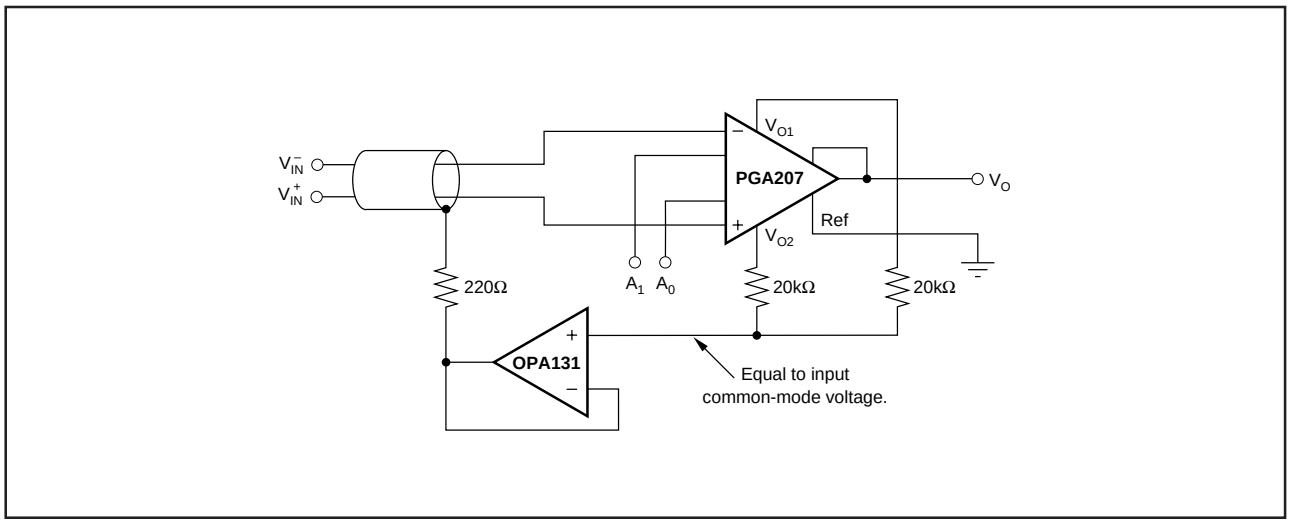
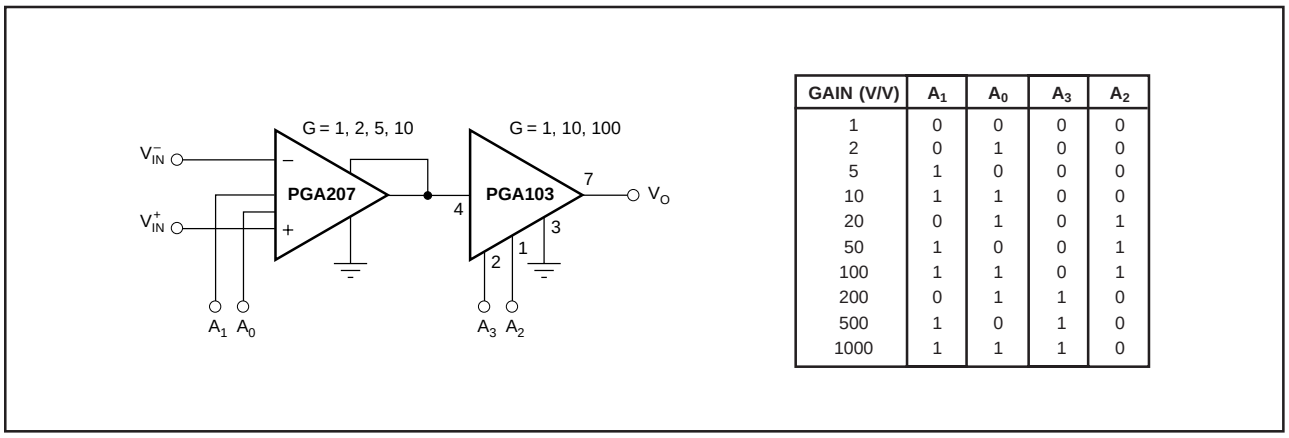


FIGURE 5. Shield Drive Circuit.



GAIN (V/V)	A_1	A_0	A_3	A_2
1	0	0	0	0
2	0	1	0	0
5	1	0	0	0
10	1	1	0	0
20	0	1	0	1
50	1	0	0	1
100	1	1	0	1
200	0	1	1	0
500	1	0	1	0
1000	1	1	1	0

FIGURE 6. Wide Gain Range Programmable IA.

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Appendix C: Configuration EEPROM Format

C.1 Introduction

All VIM Modules are required to contain an Identification (ID) EEPROM with a checksum stored in the last location. When booted, the 'C6x processors check for the presence of VIM modules, through the presence bit on the VIM connector itself. If a module is present, the processor reads the module's ID EEPROM and generates a 16–bit checksum from the results of the readout. There are three conditions for the checksum; valid checksum (**0x00EE C0DE**), bad checksum (**0x00BADC5**), and No VIM module installed (**0xFFFF FFFF**). All checksums are placed in Global SRAM at the following locations:

'C6x Processor	Global SRAM Location
Processor A	**0x0000 0900**
Processor B	**0x0000 1900**
Processor C	**0x0000 2900**
Processor D	**0x0000 3900**

If the generated checksum does not match the stored value, the processor lights its red LED, and places **BADC5** in Global SRAM. Even though the processor illuminates LED 0, the red LED, the processor is fully functional.

VIM designer note: The ID EEPROM must be a serial device with a capacity of at least 64 x 16, e.g., the Microchip 93LC46 or equivalent. It is access by means of a register at address **0x0032 0000** in the VIM module's memory map. The bitwise layout of this register is defined in Table C–1, below.

Table C–1: VIM ID EEPROM Register –R/W @ VIM Address 0x0032 0000

Bit #	D31 –D4	D3	D2	D1	D0
Bit Name	Not Used	Chip Select	Serial Data Out	Reserved	Serial Clock
Access	Read/Write	Read/Write	Read Only	N/A	Read/Write
Function	Not Applicable	1 = Selected 0 = Not Selected	Stored Data	Not Applicable	Toggle to pulse Clock line

C.2 EEPROM Format Example

Shown on the next page is the contents of an EEPROM, the example shows the Pentek Model 6215, and an explanation of what each word is used for.

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C.2 EEPROM Format Example (continued)

Table C–2: EEPROM Example (Model 6215 shown)

Global SRAM Locations	EEPROM Word Location	Contents	Comments
0x0000 z900	00/01	0x00EE C0DE	Valid data flag
0x0000 z904	02/03	0x6215 0000	Model, Model Extension –Extension field is currently unused.
0x0000 z908	04/05	0x0354 2001	PCB number. This is taken from the VIM board.
0x0000 z90C	06/07	0x0001 FFFF	Assembly Rev, Option #1 –Rev A = 1, B=2, etc. space is allocated for up to 9 installed options.
0x0000 z910	08/09	0xFFFF FFFF	Option #2, Option #3 –When there are no options, **F** appears in the entire field.
0x0000 z914	10/11	0xFFFF FFFF	Option #4, Option #5
0x0000 z918	12/13	0xFFFF FFFF	Option #6, Option #7
0x0000 z91C	14/15	0xFFFF FFFF	Option #8, Option #9
0x0000 z920	16/17	0xFFFF FFFF	Module Specific Code goes in locations 16 through 61.
0x0000 z924	18/19	0xFFFF FFFF	
0x0000 z928	20/21	0xFFFF FFFF	
0x0000 z92C	22/23	0xFFFF FFFF	
0x0000 z930	24/25	0xFFFF FFFF	
0x0000 z934	26/27	0xFFFF FFFF	
0x0000 z938	28/29	0xFFFF FFFF	
0x0000 z93C	30/31	0xFFFF FFFF	
0x0000 z940	32/33	0xFFFF FFFF	
0x0000 z944	34/35	0xFFFF FFFF	
0x0000 z948	36/37	0xFFFF FFFF	
0x0000 z94C	38/39	0xFFFF FFFF	
0x0000 z950	40/41	0xFFFF FFFF	
0x0000 z954	42/43	0xFFFF FFFF	
0x0000 z958	44/45	0xFFFF FFFF	
0x0000 z95C	46/47	0xFFFF FFFF	
0x0000 z960	48/49	0xFFFF FFFF	
0x0000 z964	50/51	0xFFFF FFFF	
0x0000 z968	52/53	0xFFFF FFFF	
0x0000 z96C	54/55	0xFFFF FFFF	
0x0000 z970	56/57	0xFFFF FFFF	
0x0000 z974	58/59	0xFFFF FFFF	
0x0000 z978	60/61	0xFFFF FFFF	
0x0000 z97C	62/63	0x0000 xxxx	Word 62 should always be cleared (**0000**). Word 63 contains the byte summation of words 0 –61.
NOTE: **z** = **0** for Processor A, **1** for Processor B, **2** for Processor C, and **3** for Processor D.			

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