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OPERATING MANUAL

PENTEK MODEL 6210

Dual A/D Converter and Digital Receiver
VIM Module for Pentek VIM Motherboards

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Pentek Model 6210 Operating Manual – Revision History

Date	Rev	Applicable Serial #'s	Comments
08/14/98	Preliminary	9841001 – Forward	Initial release.
11/16/98	Preliminary	9841001 – Forward	Added bit D04 to the Control Register. Added Table 2–4 to explain PRCLK source and freq. when the 6210 is a master. Added Figure 2–4 to show Sync and Clock signal sources.
2/18/99	Preliminary	9841001 – Forward	Added table 3–12 on loading DAC. Added Section 3.8.1 explaining Gain Amplifier. Added EEPROM format (Appendix A). Added sample code in Appendix B.
3/24/99	Preliminary	9841001 – Forward	Replaced installation instructions, they now reflect the currently shipping product. Replaced the Front Panel with the currently shipping product. Added Table 3–13 about full scale values.
6/24/99	Preliminary	9841001 – Forward	Corrected Figure 2–4, the sync lines were connected to the wrong place. Added note to Figure 2–4 about which Harris Chip is connected to which DSP on the Model 4290/4291. Corrected figure 2–1, the Front Panel labeling changed slightly. Corrected option 102 (gain), which was called option 101 throughout the manual. Added option 101 to the specs. Replaced Harris addendum with current version.
3/6/00	A	9841001 – Forward	Complete re–format – many tables removed & replaced w/ text. All references to 4290/91 changed to VIM motherboard, and non–address specific references to 'C6x changed to VIM motherboard processor. Updated & corrected Block Diagram. Sec. 1.7. Corrected supply currents. Internal Oscillator is 64 MHz, not 65. Further corrections to Fig. 2–4. Note that Gain values given in Table 3–6 for PGA do not account for filter insertion loss. Add Table 3–9 describing format/packing of output data. Improved description of signal levels/limits for EXT CLK IN. Improved description of control interface to HSP50214. Re–arrange Appendices – Move EEPROM format to Appendix D; Replace Harris's Data Sheet for HSP50214 with Intersil's & make it Appendix A; Add AD603 Data Sheet as Appendix B; LTC1451 Data Sheet is Appendix C; Add bandwidth / sample rate calculation Application Note as Appendix E; Old Appendix B (Programming Example) now covered in ReadyFlow Manual for 6210 (Pentek part # 801.62100)
3/9/00	A.1	9841001 – Forward	Add Options 020, 021, 030 & 101 to Specifications. Add AD6640 Data Sheet as Appendix B. Bump all following Appendix names up 1 letter. Correct DDR part # in Fig. F.1 & TOC listing for the figure. Also corrected another typo in Appendix F.
3/17/00	B	98041001 – Forward	Copy Table 2–4 (PRCLK Divider) into Sec. 3.4.1, where the divider bit is discussed, as Table 3–3. Added Table 3–11 (A/D Output Data Coding) in Sec. 3.8.2. Other Table #'s changed appropriately.
3/21/00	B.1	98041001 – Forward	Logic was reversed for BIFO_Disable bit, D3 in Control Reg. Corrected in Table 3–2 and Sec. 3.4.2.
10/24/00	B.2	98041001 – Forward	Sect 1.2 and 1.7, clarified the descriptions of Options 030 and 102.
4/5/01	C	98041001 – Forward	Sec. 1.3 – Changed Option 101 in NOTE to Option 020. Sec. 2.3.1 – recommend that Ext. Clock In be 2V p–p in amplitude. Add Sec. 2.3.1.1, on Duty Cycle Sensitivity. Sec. 2.4 – add part #'s for Sync Bus – Serial I/O mating connector. Sec 2.4.1 – mention that Sync Bus can support 8 units, & Model 9190 can sync up to 80 units. Also correct NOTE below Fig. 2–5 – DDR2 is controlled by Proc. B or D. Add Sec. 2.4.1.6, on Sync Bus Compatibility. Sec. 2.4.2 – Better description of how Serial Port signals are passed from Motherboard to FP connector, less text in subsections. Sec. 2.4.3 – $\overline{\text{TTL–SYNC}}$ pulse must be at least 2 sample clocks wide.

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Chapter 1: Overview

1.1 General Description

Pentek's Model 6210 is a VIM−2 Digital Drop Receiver (DDR) module (devices of this type are also often referred to as Digital Down Converters, or DDCs), designed to be attached directly to any of Pentek's DSP− or RISC−based VIM motherboards, such as Pentek Models 4290, 4291 and 4292. It forms a complete 2−channel software radio system including tuning, filtering and demodulation.

Two Model 6210s may be attached to any VIM−compatible processor board to form a 4−channel software radio which utilizes all four processors while occupying only one VMEbus slot. Alternately, the Model 6210 may be combined with another VIM−2 module to provide additional I/O functions.

1.2 Input Section

Each channel includes an analog front end which employs a wideband input amplifier followed by a programmable gain amplifier. It accommodates wideband analog inputs between 5 kHz and 80 MHz, at full−scale levels of −20 dBm to +10 dBm. Analog inputs are accepted through front panel SMA connectors.

An anti−aliasing filter removes out−of−band frequency components and can be tailored for specific signal types. The standard factory−supplied lowpass filter has a cutoff frequency of 25 MHz. The programmable−gain amp and filter may be bypassed to support undersampling applications.

Option 030 provides a filter cut−off frequency of 30 MHz. Option 102 provides full scale levels of −30 dBm to 0 dBm. Both option Option 030 and Option 102 may be combined.

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1.3 A/D Converters

Each channel employs an Analog Devices AD6640 12–bit A/D converter capable of sampling rates up to 65 MHz. The A/D sample clock can be derived from an internal 64 MHz crystal oscillator or from an external reference supplied to another front panel SMA connector.



1) Due to packaging constraints the internal oscillator is not user-replaceable. If other clock frequencies are required, contact Pentek for custom oscillators.

(2)The maximum sampling rate can only be achieved using an external reference signal, unless the internal oscillator is replaced (Option 020 provides a 65 MHz oscillator)

Both A/D converters operate synchronously from the same sampling clock to support multi–channel applications (such as direction finding) where phase between channels must be maintained.

1.4 Digital Drop Receivers

The output of each A/D converter feeds the Intersil HSP50214B, which represents a new generation of complex digital down converters and communication signal processors.

Included in the HSP50214B are an input numerically–controlled local oscillator (NCO) and mixer to translate input signals down to baseband. The mixer is followed by multistage digital filters, including a comb filter, half–band filters and an FIR filter with programmable coefficients. Together, they support decimation factors from 4 to 16,384, and a maximum output bandwidth of 929 kHz with an 84 dB SFDR at an output sampling rate of 12.24 MHz.

A second processing section consists of a resampling polyphase filter which operates asynchronously, with a second clock signal. The output section includes direct I and Q complex outputs, a hardware cartesian–to–polar converter, a frequency discriminator with programmable FIR filter, a timing error signal for symbol tracking, and AGC outputs.

A digital multiplexer allows either the digital receiver output or the A/D output to be sent into the 'C6x BI–FIFO, to support direct, wideband input data capture. A front panel ribbon cable bus allows multiple 6210s to share a common sample clock and synchronize the phase of the digital receivers across modules.

1.5 Connection to VIM Motherboard

Both 16–bit parallel output data ports (ports A and B) from the Model 6210 flow into the FIFO structures on the VIM motherboard. A control path from each motherboard processor permits direct programming of the HSP50214B functions including tuning, decimation, output formatting, filter control and filter coefficients.

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1.6 Simplified Block Diagram

Figure 1–1, below, provides a simplified block diagram of the Model 6210.

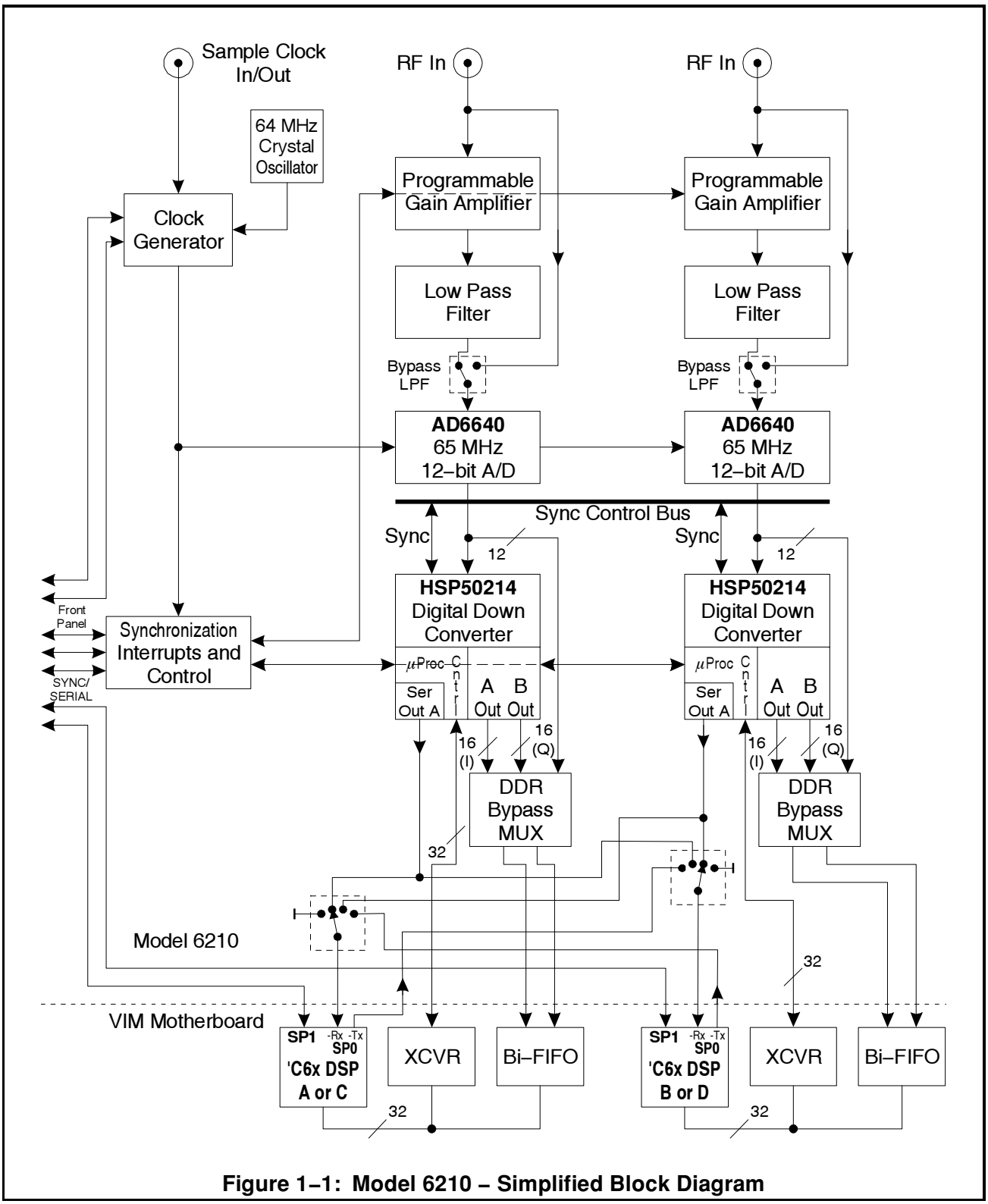


Figure 1–1: Model 6210 – Simplified Block Diagram

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1.7 Specifications

The specifications below are typical, at 25°C ambient temperature, with + 5 V_{DC} and ± 12 V_{DC} power supplies within ± 1 % of nominal, unless otherwise specified.

Input Channels

Quantity:	2
Input Type:	Single−ended, non inverting
Input Impedance:	
Standard:	50 Ω
Option 101:	650 kΩ
Full Scale Voltage:	± 1.0 Volts

Input Amp/Filter

Quantity:	2 (one per A/D Channel)
Amplifier #1	
Type:	Fixed gain Burr Brown OPA642
Bandwidth:	80 MHz
Bypass:	None
Amplifier #2	
Type:	Analog Devices AD603* Programmable Gain Amp controlled by 12−bit D/A (Linear Technology LTC1451†)
Bandwidth:	25 MHz
Bypass:	Programmable (includes filter)
Gain (full scale):	
Standard:	10 dBm to −20 dBm
Option 102:	0 dBm to −30 dBm

* – Data Sheet included as Appendix C, courtesy of Analog Devices Inc., Norwood, MA.
† – Data Sheet included as Appendix D, courtesy of Linear Technology Corp., Milpitas, CA.

Anti−Aliasing Filter	
Type:	Fixed frequency low pass − 5 pole Chebyshev
Passband (−3 dB):	
Standard:	25 MHz
Option 030:	30 MHz
Passband Flatness:	± 1 dB
Stopband:	80 MHz
Stopband Attenuation:	> 60 dB
Bypass:	Programmable (includes P. G. Amp)

A/D Converter:

Device:	Analog Devices AD6640**
Quantity:	2
Sampling Rate:	6.5 MHz min, 65 MHz max.
Coupling:	AC, 5 kHz cut in
Clock Source:	Selectable − Onboard crystal oscillator or front panel external clock.
Resolution:	12 bits

** – Data Sheet included as Appendix B, courtesy of Analog Devices Inc., Norwood, MA.

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1.7 Specifications (continued)

Signal Purity

Front End Performance w/ Programmable Amp

Harmonic Distortion:	–60 dB
Signal/Noise Ratio (30 MHz)	–50 dB
Spur Free Dynamic Range:	–65 dB
Crosstalk:	–60 dB @ 1 MHz

Front End Performance w/o Programmable Amp

Harmonic Distortion:	–70 dB
Signal/Noise Ratio (30 MHz)	–60 dB
Spur Free Dynamic Range:	–70 dB
Crosstalk:	–60 dB @ 1 MHz

Sample Rate Control

Clock Source:

Internal:	Onboard crystal oscillator
Standard:	64 MHz
Option 020:	65 MHz
Oprion 021:	53.125 MHz
External:	Front Panel Low–Voltage Differential Signal (LVDS) 65 MHz max.
Sample Rate Divider:	internal or external source can be divided by 1, 2, 4, 8, or 10 .

Digital Receiver

Device:	Intersil HSP50214*
Quantity:	2
Data Source:	Associated A/D (A/D 1 to DDR 1, A/D 2 to DDR 2)
Clock Source:	Same as associated A/D source.
Bypass:	Under software control, each DDR can be bypassed individually to provide A/D output to the BI–FIFO interface.
Sync:	Provided through VIM motherboard–driven control register or via front panel connector.

* – Data Sheet included as Appendix A, courtesy of Intersil Corp., Palm Bay, FL.

Front Panel

Analog Input:	2 SMA Connectors (1 per channel)
Sample Clock:	Multipin connector (programmable as input or output – differential LVDS compatible only) and 1 SMA connector (also LVDS only)
Sync:	Multipin connector (programmable as input or output – differential LVDS compatible only) and one TTL input
VIM Motherboard Functions	Provides access to VIM Motherboard XDS connec–tor and status LEDs
VIM Motherboard Reset:	Front panel control

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1.7 Specifications (continued)

Power Requirements:

+5 V_{DC}
Min. (idle): 760 mA
Max. (loaded): 2000 mA

+12 V_{DC}
Min. (idle): 750 mA
Max. (loaded): 750 mA

−12 V_{DC}
Min. (idle): 500 mA
Max. (loaded): 500 mA

Dimensions:

VIM−2 Module
Height: 114 mm (4.5−in.)
Depth: 82 mm (3.25−in.)
Width: 20 mm (0.8−in.)

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If any damage is discovered, please contact Pentek immediately at (201) 818−5900. Also, please save the original shipping container and packing material in case reshipment is required.

2.2 Jumper Blocks

The Model 6210 PC board contains several jumper blocks. Figure 2−1, on the next page, shows all jumper block locations. Please be aware that all of the jumpers are configured at the factory for proper operation and, with the exception of JB2 (see Section 2.2.1 and Table 2−2, at the bottom of this page) should not be moved. Table 2−1, below, provides the factory jumper settings for reference, or in case you suspect that they have been tampered with.

Table 2−1: Model 6210 − Factory Jumper Settings

Jumper Block	Factory Setting
JB1	Pins 1−2
JB2	Pins 2−3
JB3	Jumper ON (pins 1−2)
JB4	Pins 2−3

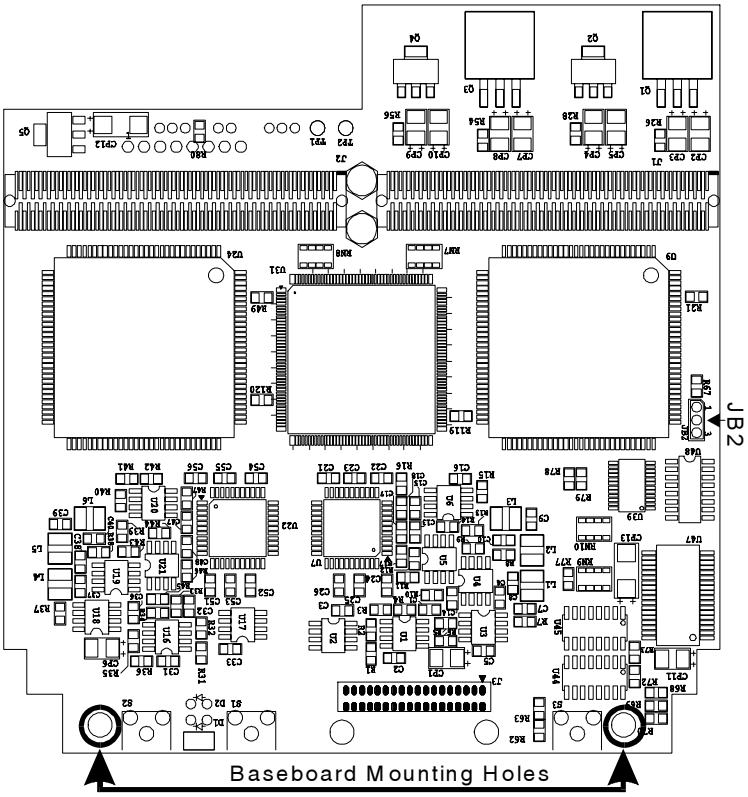
2.2.1 External Clock Function Select Jumper − JB2

Install a jumper between pins 2 and 3 of JB2 to use a signal applied to the front panel EXT CLK input connector as the source of the sample clock signal for the A/D converter. To use the EXT CLK input as the reference clock signal for the DDR, place a jumper between pins 1 & 2 of JB2. For a description of the signals that can be applied to the EXT CLK input connector, please refer to Section 2.3.1.

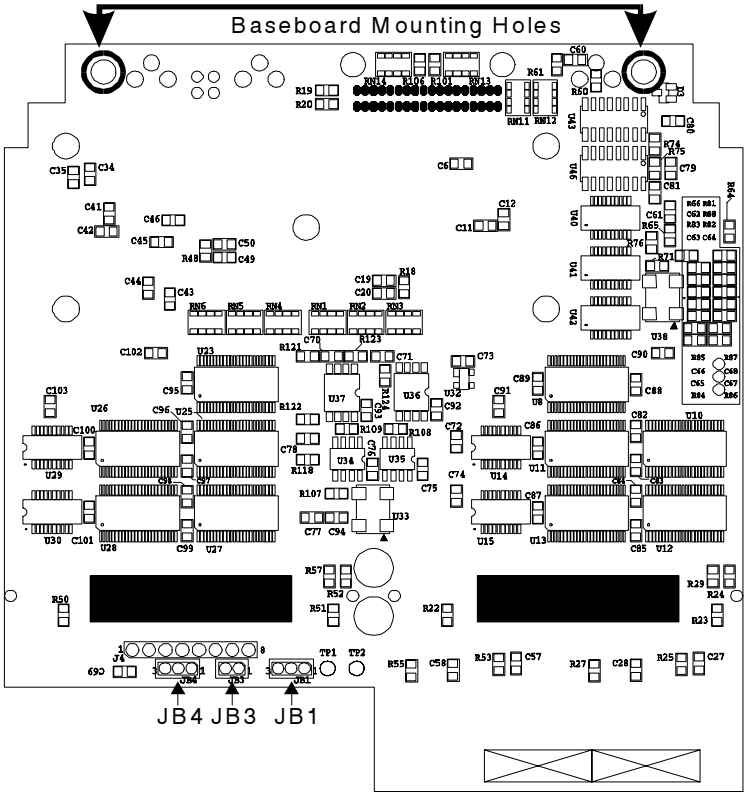
Table 2−2: Model 6210 − External Clock

Jumper Position	External Clock Function
1 − 2	DDR Reference Clock
2 − 3*	A/D Sample Clock*
* − Factory Default Setting	

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(a) Component Side



(b) Solder Side

Figure 2–1: Model 6210 PC Board, Showing Jumper Blocks & Mounting Holes

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2.3 Model 6210 Front Panel Features

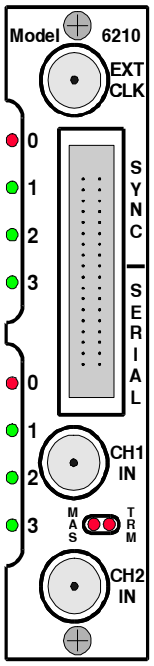


Figure 2–2: Model 6210 – Front Panel

The Model 6210's front panel is shown in Figure 2–2, at the right. This panel occupies one of the VIM module positions available on a VIM motherboard's front panel. If the Model 6210 is the only mezzanine board installed, the other half of the motherboard's panel may be filled with a blank, supplied with the motherboard. Available on the Model 6210's front panel are three SMA connectors, one for each channel's analog input signal and a third for an external clock signal. Two indicator LEDs associated with the 6210's Sync Bus interface are visible between the two analog input connectors, and four LED's associated with each motherboard processor that can access the module can be seen through cutouts on the left side of the panel. The panel's most prominent feature is the 36–pin Sync Bus – Serial I/O connector, which will be covered in Section 2.4. The other panel features discussed will all be discussed in the subsections that begin below.

2.3.1 External Clock Input – EXT CLK

The threaded, coaxial SMA connector nearest the top of the Model 6210's front panel is provided for the application of an external clock signal. This signal can be used either as the sample clock signal for the 6210's A/D converters, or as the reference clock signal for its DDR.

The External Clock Input circuit used on Pentek's Model 6210 is designed to accept Low–Voltage Differential Signals (LVDS). The impedance presented by the external clock input is 50 Ω The applied signal is AC coupled via 0.1 µF to the + input of an LVDS line receiver. This input is diode–protected to ground and +3.3 V, and biased at +1.65 V (the – input of the receiver is also biased at +1.65 V). LVDS devices can typically react to differential input signal swings as low as 250 mV, or, when used in a single–ended manner (as in this case), to signal levels as low as 100 mV above, or 20 mV below, the bias voltage. For most applications, Pentek recommends that the signal applied to this connector be a square or sine wave, with 2 V p–p amplitude, at frequencies up to 65 MHz. Figure 2–3, at the top of the next page, shows the equivalent circuit for the Model 6210's EXT CLK input.

2.3.1.1 Duty Cycle Sensitivity

The A/D converter used on the Model 6210 is the AD6640, from Analog Devices. The graphs presented in the AD6640 Data Sheet (see Appendix B) indicate that the ADC is relatively insensitive to duty cycle variations between 40% and 65%. Figure 17 in the AD6640 Data Sheet shows the SNR and Spurious performance at varying duty cycles for a 2.2 MHz analog input signal sampled at 65 MHz. Under these conditions, the performance seems quite good.

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2.3 Model 6210 Front Panel Features (continued)

2.3.1 External Clock Input (continued)

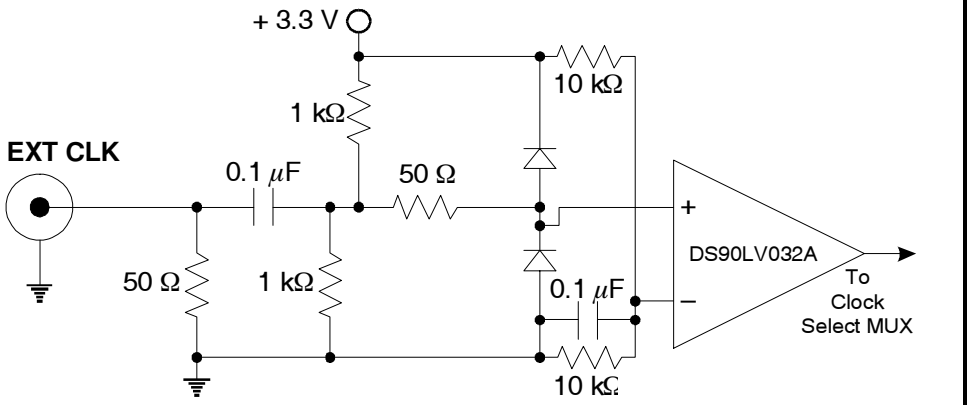


Figure 2–3: Model 6210 – External Clock Input Circuit

2.3.1.1 Duty Cycle Sensitivity (continued)

Our experience with this device under different conditions, however, has not been quite so favorable. We have found that if the device is operated at sample rates of 60 MHz or more, with an input signal that is offset slightly from the sample rate (e. g., sampling a 60.05 MHz signal at a 60 MHz sample rate), significant conversion errors can occur at the ADC's output if the duty cycle varies even marginally from 50%.

Referring to the AD6640's switching specifications for the ENCODE input (this is where the sample clock signal is delivered), we see that the minimum high and low pulse widths at that input are both 6.5 nsec. Bearing that in mind, consider that a perfect square wave at 65 MHz has a half–cycle time slightly less than 7.7 nsec. Now bring that perfect square wave into the real world, where such things as rise and fall time exist, and you can see how it might become difficult NOT to violate the 6.5 nsec pulse width specification at the maximum sample rate.

There is a significant amount of signal conditioning and selection circuitry between the 6210's EXT CLK input and the AD6640's ENCODE input. This tends to cause a small amount of difference between the duty cycle of the signal you deliver to the front panel connector and the duty cycle of the signal we deliver to the ADC. So, even if you know that your EXT CLK input signal has a duty cycle of 50% $\pm$ 0.00001%, that's probably not what the ADC sees.

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2.3 Model 6210 Front Panel Features (continued)

2.3.1 External Clock Input (continued)

2.3.1.1 Duty Cycle Sensitivity (continued)

Now that we've given you what seems to be some bad news, we'll follow with the good news. We have ONLY seen the AD6640's duty cycle sensitivity become a problem in the very specific situation where the sample rate is relatively high (> 60 MHz), AND the analog input signal's frequency is very close to the absolute sample rate or a multiple thereof. In such cases, the apparent output signal from the A/D is an alias of the difference frequency, and contains a relatively high number of samples per cycle. The problem is easily visible in real−time plots of the A/D output, as glitches in the output signal. Should your application require that you operate your 6210 in this manner, we make the following recommendations:

1) DO NOT use the internal oscillator as your clock source, as there is no way to control the internal clock's duty cycle. Instead, apply and select an external clock signal with a variable duty cycle.

2) Before attempting any serious data acquisition, monitor and plot the A/D output in real time, and adjust the duty cycle of the clock input until the glitches disappear.

2.3.2 Analog Inputs – CH1 IN, CH2 IN

The two threaded, coaxial SMA connectors nearest the bottom of the Model 6210's front panel are the Analog Input Connectors. The analog inputs are terminated in 50 Ω, and directly coupled to the non−inverting inputs of OPA642 Operational Amplifiers. The maximum input signal swing for linear operation is ± 1 V (i.e., 2 V_{P-P}). The amplifier's bandwidth is 80 MHz, but because the Model 6210's maximum sample rate is 65 MHz (64 MHz if the internal crystal oscillator is used as the sample clock), the bandwidth of signals applied to these inputs should be limited to 32.5 MHz (32 MHz if the internal crystal oscillator is used as the sample clock), or to one half of the programmed sample rate, unless your application requires undersampling.

2.3.3 Indicator LEDs

A total of ten LED's are visible through the front panel of the Model 6210. Two of these are associated with the 6210's Sync Bus interface. These are located between the Analog Input Connectors, slightly to the right of the center of the panel. The other eight are general purpose indicators controlled by the processors on the VIM motherboard, and are visible through the cutouts at the left side of the 6210's front panel. These will all be discussed in the subsections that begin at the top of the next page.

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2.3 Model 6210 Front Panel Features (continued)

2.3.3 Indicator LEDs (continued)

2.3.3.1 Sync Bus Master LED – MAS

The red MAS LED, the leftmost one near the panel's center, indicates that the Sync Bus master function has been enabled for the 6210 in question. This means that the 6210 on whose panel this LED is lit will be the one that provides the Sync signals to all other VIM modules connected to the Sync Bus. Any Sync Bus MUST have **one and only one** master, and it should physically be located at the opposite end of the Sync Cable from the Sync Terminator (see Section 2.3.3.2, below). This LED will be illuminated whenever the D0 bit in the 6210's Control Register (see Section 3.4) is set to the logic '1' state. It will be turned off when that bit is cleared to the logic '0' state.

2.3.3.2 Sync Bus Terminator LED – TRM

The red TRM LED, the rightmost one near the panel's center, indicates that the Sync Bus Master termination has been enabled for the 6210 in question. This means that the 6210 on whose panel this LED is lit will be the one that provides the terminating resistors for the Sync signals generated by the Sync Bus master. Any Sync Bus MUST have **one and only one** terminator, and it should physically be located at the opposite end of the Sync Cable from the Sync master (see Section 2.3.3.1, above). This LED will be illuminated whenever the D1 bit in the 6210's Control Register (see Section 3.4) is set to the logic '1' state. It will be turned off when that bit is cleared to the logic '0' state.

2.3.3.3 Motherboard LEDs – 0, 1, 2 & 3

Visible through cutouts at the left side of the Model 6210's front panel are two groups of four LEDs controlled by the processors on the VIM motherboard. Each group of four LEDs contains one red LED (labeled 0) and 3 green LEDs (labeled 1, 2 & 3), and they are under the control of one of the motherboard's processors. Depending upon the position in which the VIM module is installed on the motherboard, the four LEDs nearest the top of the panel are controlled by either Processor A or Processor C, and the four at the bottom are controlled by either Processor B or Processor D. For further details about these indicators, please refer to your VIM motherboard's Operating Manual.

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2.4 Sync Bus – Serial I/O Connector

Accessible through each Model 6210's front panel is a 36–pin serial connector (3M part #81036–500203, Pentek part # 354.03610), several pins of which are connected to (and driven by) the VIM motherboard's serial ports. The mating connector is 3M part # 83036–6006 or an equivalent, Pentek part # 353.03605. Also included on this connector are signals used for synchronizing multiple units. Table 2–3, at the bottom of this page, contains the pinouts and description of this connector, whose pin numbering scheme is shown in Figure 2–4, at the right.

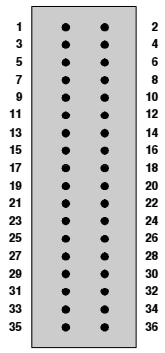


Figure 2–4: Model 6210 – Front Panel Sync Bus – Serial I/O Connector Pin Numbering

2.4.1 Signals for Synchronizing Multiple Boards

The following LVDS (Low–Voltage Differential Signaling) signals make up the sync bus; MCLK, PRCLK, MSYNC, SYNC1, and SYNC2. The sub–sections that begin on the page after next describe each of these signals. Figure 2–5, on the next page, shows a block diagram of the Sync and Clock signal sources.

Table 2–3: Model 6210 – Sync Bus – Serial I/O Pinouts

Pin	Signal	Pin	Signal
1	Ground	2	MCLK
3	$\overline{\text{MCLK}}$	4	Ground
5	MSYNC	6	$\overline{\text{MSYNC}}$
7	SYNC1	8	$\overline{\text{SYNC1}}$
9	SYNC2	10	$\overline{\text{SYNC2}}$
11	Ground	12	PRCLK
13	$\overline{\text{PRCLK}}$	14	Ground
15	$\overline{\text{TTL–SYNC}}$	16	Ground
17	P0–CLKR1	18	Ground
19	P0–FSR1	20	P0–DR1
21	P0–CLKS1	22	Ground
23	P0–CLKX1	24	Ground
25	P0–FSX1	26	P0–DX1
27	P1–CLKR1	28	Ground
29	P1–FSR1	30	P1–DR1
31	P1–CLKS1	32	Ground
33	P1–CLKX1	34	Ground
35	P1–FSX1	36	P1–DX1

Up to eight (8) 6210's can be operated synchronously by cabling these connectors together. Further details about how this is accomplished are provided in the subsections beginning on the page after next, and in Sections 3.4 and 3.9. If your application requires more than 8 units synchronized units, Pentek's Model 9190 can be used to synchronize up to eighty (80) 6210s.

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2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

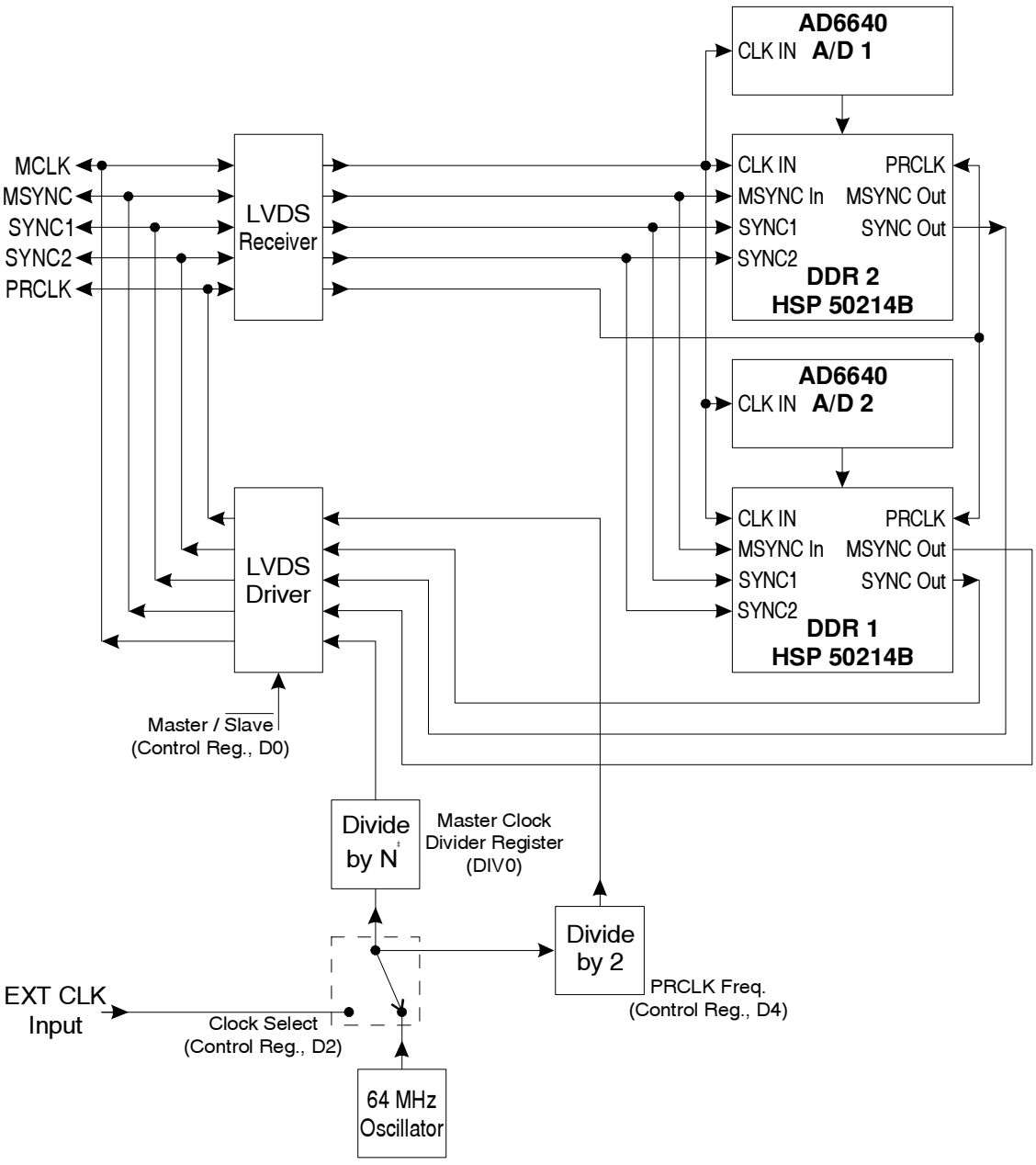


Figure 2–5: Model 6210 – Block Diagram of Clock and Sync Signal Sources



DDR 1 is controlled by VIM Motherboard Processor A or C, and DDR2 is controlled by Processor B or D, depending where the VIM module is installed on the motherboard.

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2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

2.4.1.1 MCLK, $\overline{\text{MCLK}}$

This signal is used as both the sample clock for the A/D converters, and the front–end processing clock for the DDRs. When the Model 6210 is configured as a master, this is an LVDS output at the A/D sample clock rate. If the board is configured for an external clock, then the original source for this signal is the **EXT CLK** SMA input connector. Otherwise, the on–board crystal oscillator is used as the frequency source. The frequency of MCLK is equal to the external or crystal frequency divided by the contents of the Master Clock Divider register (see Section 3.5).

When configured as a slave, this signal is a differential LDVS input and will be used as the A/D sample clock and the front–end processing clock for the DDRs, instead of the board's own external clock input or on–board oscillator. This is how several boards are able to sample synchronously from the same reference clock source.

2.4.1.2 PRCLK, $\overline{\text{PRCLK}}$

This signal is the clock used by the back–end processing of the HSP50214B DDR chips, referred to as PROCCLK in the DDR's Data Sheet in Appendix A of this manual. When the Model 6210 is configured as a Sync master, this is a differential LVDS output. Table 2–4, at the top of the next page, contains a list of possible PRCLK sources and their frequency limits, when the Model 6210 is configured as a Sync master. **PRCLK MUST BE LESS THAN 55 MHz**, regardless of the clock source.

When configured as slave, this is a differential LVDS input used by the HSP50214B DDR in place of the on–board generated PRCLK. In this way, the DDRs of several boards may all be synchronized to the same PRCLK source.

When bypassing the HSP50214B chips, and using the 6210 as an A/D converter only, these signals are ignored.

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2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

2.4.1.2 PRCLK, $\overline{\text{PRCLK}}$ (continued)

Table 2–4: Model 6210 – Master PRCLK Signal Source & Frequency

Mode	A/D Clock Frequency	Clock Source*	PRCLK_Divider Setting (Control Reg., D4)	Description
Master (Control Reg., D0 = 1)	< 55 MHz	EXT. CLK	1	PRCLK = Ext. CLK
		INT. OSC†	1†	PRCLK = INT. OSC.†
	> 55 MHz	EXT. CLK	0	PRCLK = EXT CLK/2
		INT. OSC	0	PRCLK = INT. OSC/2

* – The clock source is selected by the Ext_Clk Enable bit (D2, Control Register).

† – This selection is only valid if the standard, 64 MHz internal oscillator is replaced by one whose frequency is 55 MHz or less (e.g., Option 021).

2.4.1.3 MSYNC, $\overline{\text{MSYNC}}$

This signal is the reset pulse used by the HSP50214B DDRs to synchronize their front– and back–end processing. If the board is configured as a master, then this is a differential LVDS output. If the board is configured as slave, this signal is a differential LVDS input. MSYNC's quiescent state is low, and synchronization occurs on the rising edge of this signal (or the falling edge of the normally–high $\overline{\text{MSYNC}}$).

2.4.1.4 SYNC1, $\overline{\text{SYNC1}}$

This signal is the reset pulse for HSP50214B DDR front–end processing. It resets all DDR processing associated with MCLK, including the VIM motherboard's input Bi–FIFOs and the Bi–FIFO write rate dividers across multiple channels and/or boards. SYNC1's quiescent state is low, and synchronization occurs on the rising edge of this signal (or the falling edge of the normally–high $\overline{\text{SYNC1}}$).

If the Model 6210 is configured as a Sync bus master, this is a differential LVDS output. SYNC OUT of Channel 2's HSP50214B DDR is used as the source for the differential LVDS output. For proper operation, the Syncout CLK Select bit (D3) of DDR2's Control Word 0 should be cleared to the logic '0' state. This configures DDR2 such that its SYNC OUT signal is derived from CLKIN (i.e., the Sync bus MCLK signal – see Figure 2–5, and the Control Word 0 description in the HSP50214 Data Sheet, Appendix A of this manual). If the Model 6210 is configured as a Sync bus slave, this is a differential LVDS input.

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2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

2.4.1.5 SYNC2, $\overline{\text{SYNC2}}$

This signal is the same as SYNC1 except its source is Channel 1's DDR SYNC OUT and is used to synchronize all back–end DDR processing associated with PRCLK. Channel 1's DDR control register should be configured for SYNC OUT to be derived from PRCLK for proper operation. SYNC2's quiescent state is low, and synchronization occurs on the rising edge of this signal (or the falling edge of the normally–high $\overline{\text{SYNC2}}$).

2.4.1.6 Compatibility with Other Products' Sync Buses

At the time of this manual's publication, Pentek manufactures four devices that use the same physical connector to implement a Sync bus and Serial I/O port. These are the Models 6210 and 6216 Digital Reciver/ADCs, the Model 6211 A/D Converter, and the Model 6229 Digital Transmitter/DAC. The serial port implementations are identical across these four products. However, if you simply take a length of 36–wire ribbon cable and crimp a 36–pin insulation–displacement connector at either end, you'll be connecting the serial port transmitters to other transmitters, and the receivers to other reveivers. Such configurations are clearly to be avoided, so any required serial port interconnections will have to be made via some sort of breakout box or board, reminiscent of the RS–232 implementations that we all remember from the good(?) old days.

Cables that are intended to connect only the Sync busses of these devices can b e constructed using two or more 36–pin IDC connectors (3M part # 83036–6006 or an equivalent, Pentek part # 353.03605), and a 16–wire ribbon cable connecting pins 1 – 16 on all connectors. One should be aware, however, that there are some differences in the Sync bus implementations across these devices. The paragraphs that follow will comment on the interoperability of the Sync busses among these four products.

The Models 6211 is essentially identical the Model 6210, except that it lacks a Digital Receiver stage. The 6211 can generate and receive the differentially–paired MCLK and SYNC1 signals. It can neither generate nor receive the differentially–paired MSYNC, SYNC2 and PRCLK signals, but the pins used for these signals are left unconnected on the Model 6211, so it will not interfere with the propagation of these signals. The Model 6210 can generate and receive all five of these differential pairs. Thus, if a synchronized system using both 6210s and 6211s were to be assembled, one of the 6210s should be the SYNC bus master.

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2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

2.4.1.6 Compatibility with Other Products' Sync Buses (continued)

The Model 6216 is a Wideband Digital Receiver and A/D converter. Its ADC stage is also identical to the Model 6210's , but it uses Graychip's GC1012 Down–Converter instead of the Intersil HSP50214 used in this product. There are several differences between the synchronizing features of these two devices, most notably that synchronization occurs on the rising edge of the sync signals on the 6210, and on the falling edge of these signals on the 6216. Thus, 6210s and 6216s CANNOT be synchronized with one another. Finally, the Model 6229's Sync bus is compatible with the 6216's , and therefore not compatible with the 6210's.

2.4.2 Serial Port Signals

The signals listed in the subsections below are associated with the VIM motherboard's Serial Ports. If the Model 6210 is installed above (i. e., controlled by) Processors A & B on the VIM motherboard, then Processor A's serial port 1 is P0, and Processor B's serial port 1 is P1. If the Model 6210 is installed above VIM motherboard Processors C & D, then Processor C's serial port 1 is P0, and Processor D's serial port 1 is P1. All these signals are delivered directly from the 6210's VIM Motherboard connector to the front panel Sync Bus – Serial I/O Connector via a small series resistor (47 Ω), and are pulled up to +5 V via 8.2 kΩ on the I/O connector side of the series resistor.

2.4.2.1 P0–CLKR1, P1–CLKR1

These are the Serial Port Receive Clock Signals from the VIM motherboard.

2.4.2.2 P0–FSR1, P1–FSR1

These are the Serial Port Receive Frame Sync signals from the VIM motherboard.

2.4.2.3 P0–CLKS1, P1–CLKS1

These are the Serial Port External Clock Source signals from the VIM motherboard.

2.4.2.4 P0–DR1, P1–DR1

These are the Serial Port Receive Data signals from the VIM motherboard.

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2.4 Sync Bus – Serial I/O Connector (continued)

2.4.2 Serial Port Signals (continued)

2.4.2.5 P0–CLKX1, P1–CLKX1

These are the Serial Port Transmit Clock signals from the VIM motherboard.

2.4.2.6 P0–FSX1, P1–FSX1

These are the Serial Port Transmit Frame Sync signals from the VIM motherboard.

2.4.2.7 P0–DX1, P1–DX1

These are the Serial Port Transmit Data signals from the VIM motherboard.

2.4.3 $\overline{\text{TTL–SYNC}}$

This signal is a single–ended, TTL compatible sync input. SYNC1 and SYNC2 pulses will be created in slave units on the rising edge of this signal. The signal applied to this input must be a logic high in its quiescent state, and the negative–going sync pulse applied here must be at least two sample clock periods wide. If left unconnected, this pin is pulled to a high logic level.

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2.5 Installing the Model 6210 on a VIM Motherboard

Pentek's VIM motherboard ship with two blank panels where optional VIM modules, such as the Model 6210, can be installed. This section provides directions for removing blank panels, and installing the Model 6210, or other VIM modules.

WARNING

Perform all assembly steps at an antistatic workstation!

Tools required for all procedures:

1) #1 Phillips screwdriver

2) flat–blade screwdriver (blade width 5/16–in. or less)

2.5.1 Preparing the VIM Module for Installation

1) Remove the blank insert from the position in which your VIM module will be installed by removing the two countersunk Phillips screws from the top & bottom of the insert.

2) Remove the front panel from the VIM module by removing the two countersunk Phillips screws from the top & bottom of the panel.

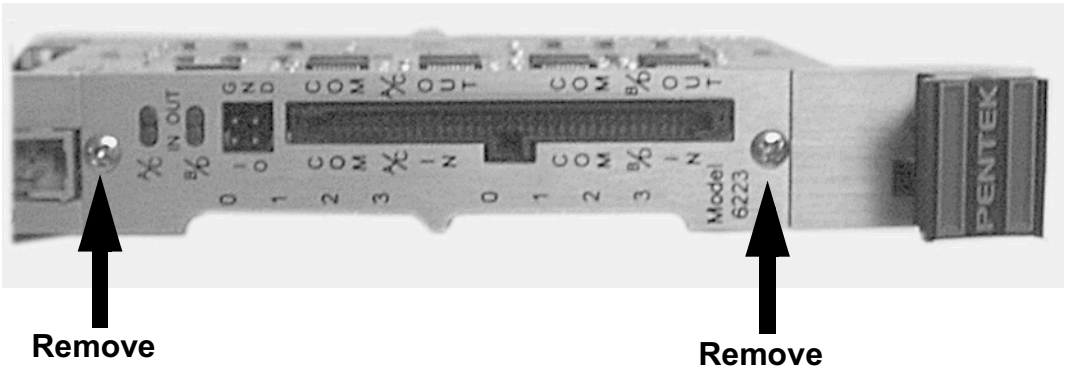


Figure 2–6: VIM Module Countersunk Screws

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2.5 Installing the Model 6210 on a VIM Motherboard (continued)

2.5.1 Preparing the VIM Module for Installation (continued)

3) Remove the two shipping brackets that were used to mount the front panel to the VIM module, by removing the two pan–head Phillips screws from the solder side of the VIM module. These brackets may be discarded or saved to use to store the panel on the VIM module if and when it is removed from the VIM motherboard.

4) At the rear of the VIM module, on the component side, is a nylon spacer with a nylon screw threaded into it.

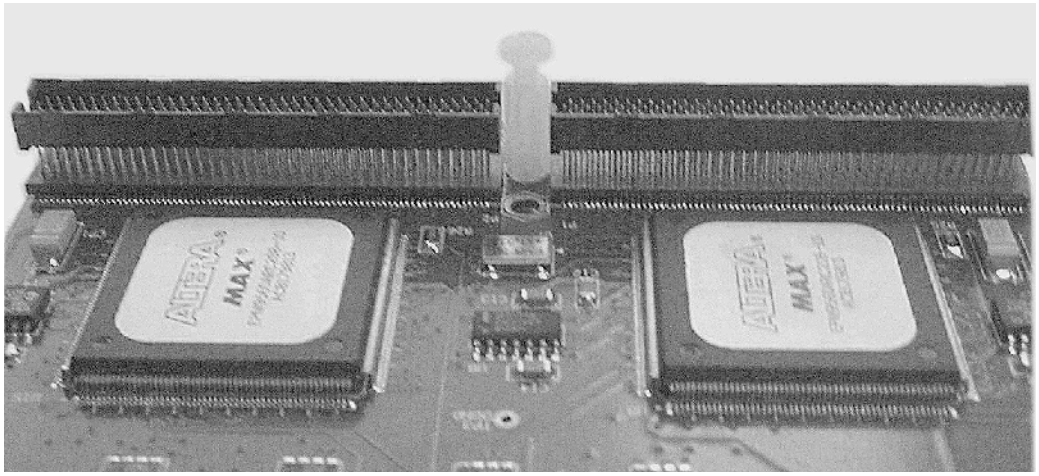


Figure 2–7: VIM Module Nylon Spacer

a) Remove the nylon screw threaded into the spacer from the component side. Set this screw aside, as it will be used when installing the VIM module on the motherboard.

b) The spacer should be installed in the hole BEHIND the VIM connectors (i.e., farthest from the front panel's location). If the spacer is installed in the front hole, reposition it by removing the nylon screw on the SOLDER side of the VIM module, and threading it back into the spacer through the rear–most hole.

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2.5 Installing the Model 6210 on a VIM Motherboard (continued)

2.5.2 Installing the VIM Module on the VIM Motherboard

1) With the VIM motherboard's component side (the one with the mezzanine connectors) up, and the connectors on the VIM module face down, align the P1 and P2 connectors on the VIM module with the pair of connectors corresponding to the desired location on the motherboard (e.g., P11 and P14 at the top of the 4290, or P8 and P4, at the bottom).

2) **GENTLY but firmly**, press down on the areas of the VIM module opposite both connectors, to fully seat the VIM module's connectors in the motherboard's. If you meet with significant resistance, check the connector alignment. Misalignment can cause bent pins or break connector housings, so **NEVER APPLY EXCESSIVE FORCE**.

3) After seating the connectors, secure the front of the VIM module to the motherboard by threading two pan−head Phillips screws through the holes in the front of the solder side of the VIM module into the threaded holes in motherboard's panel brackets.

4) Turn the assembly over, such that the mezzanine board is on the work surface and the solder side of the VIM motherboard is face up.

5) Secure the rear of the VIM module to the motherboard using the nylon screw you removed earlier through the rear mounting hole on the motherboard, threaded into the nylon spacer on the VIM module.

6) Attach the VIM module's front panel to the motherboard using two countersunk Phillips screws, passed through the holes at the top and bottom of the VIM panel and threading them into the threaded holes in the motherboard's panel brackets.

7) If an additional VIM module is to be installed, repeat this procedure in the other module location on the motherboard.

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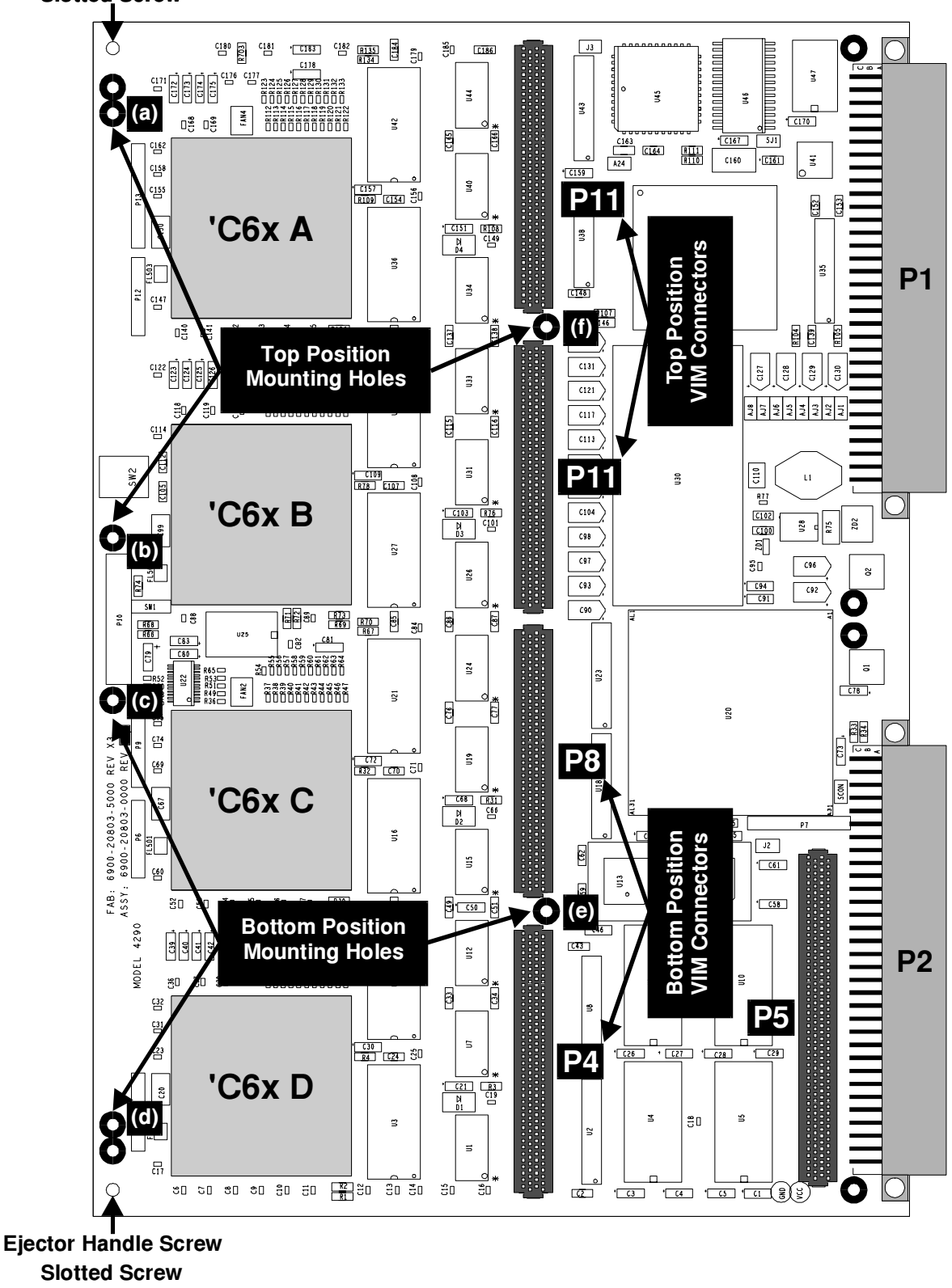


Figure 2–8: Model 4290 VIM Motherboard – Connectors & Mounting Holes

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Chapter 3: Memory Map and Register Descriptions

3.1 Overview

This section covers access to the Model 6210 from the VIM motherboard. Memory maps to VIM module resources are given from the motherboard processor's viewpoint, and details are provided describing the use of each resource.

3.2 Model 6210 Memory Map

Table 3–1, below, provides a complete memory map for the Model 6210 mezzanine board. The subsections that follow the table provide detailed information about each register.

Table 3–1: Model 6210 Memory Map

'C6X Address	Register Description	Mnemonic	Access	Additional Info
0x0032 0000	ID EEPROM Readout	EEPROM	R. O.	Appendix E
0x0032 0004 – 0x0032 001C	Reserved	—	N/A	N/A
0x0032 0020*	Control Register*	CONTROL	R/W	Section 3.4
0x0032 0024*	Master Clock Divider*	MCLKDIV	R/W	Section 3.5
0x0032 0028	BIFO Decimation Register	BIFODIV	R/W	Section 3.6
0x0032 002C	Programmable Gain Amplifier	GAIN	R/W	Section 3.7
0x0032 0030	Data Format / Signal Path Register	DATA_CONTROL	R/W	Section 3.8
0x0032 0034*	SYNC Generate Register*	SYNC	W.O.	Section 3.9
0x0032 0038	Serial Port 0 Connection Register	SPORT_CONTROL	R/W	Section 3.10
0x0032 003C	CIC Gain Adjust Register	CIC_GAIN_ADJ	R/W	Section 3.11
0x0032 0040	DDR Holding Register 0	DDR0	R/W	Section 3.12
0x0032 0044	DDR Holding Register 1	DDR1	R/W	
0x0032 0048	DDR Holding Register 2	DDR2	R/W	
0x0032 004C	DDR Holding Register 3	DDR3	R/W	
0x0032 0050	DDR Write Destination Address Register	DDR4	R/W	
0x0032 0054	DDR Read Source Register	DDR5	R/W	
0x0032 0058	Reserved	—	N/A	N/A
0x0032 005C	DDR Status Read Register	DDR6	R/W	Section 3.12

* – These registers are accessible only to Processor A or Processor C on the VIM motherboard, depending upon the position in which the VIM module is installed.

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3.3 ID EEPROM Readout Register – R. O. @ 'C6x Address 0x0032 0000

The format for the code stored by Pentek in this EEPROM is listed in Appendix E of this manual. The format is provided for VIM module designers. Neither the format nor this register is intended for general use.

3.4 Control Register – R/W @ 'C6x Address 0x0032 0020

The Control Register allows you to configure the Model 6210 as a master or slave on the sync bus and to toggle the on–board sync bus termination. It also provides a bit that selects the source of the clock as internal or external, a bit to divide the frequency of the signal that will be used as the PROCCLK for the DDR by 2 (this is necessary if that signal's frequency exceeds 55 MHz), and a bit to synchronize the operation of the BIFO on the motherboard. All bits in the Control Register default to the logic '0' state. The Control Register is accessible only to Processor A or Processor C on the VIM motherboard, depending upon the position in which the module is installed. Neither Processor B nor Processor D on a VIM motherboard can ever access this register. Table 3–2, below, shows the contents of the Model 6210's Control Register. The subsections that begin below the table give detailed descriptions of the bits in this register.

Table 3–2: Model 6210 – Control Register – R/W @ 'C6x Address 0x0032 0020

Bit #	**D31 – D8**							
BitName	Reserved							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved			PRCLK_ Divider	BIFO_ Disable	Ext_Clk _Enable	Term_ Enable	Master/ $\overline{\text{Slave}}$
Bit Function	Write with 0's Mask when Reading			1 = ÷ 1 0 = ÷ 2	1 = Disable 0 = Enable	1 = Ext Clk 0 = Crystal	1 = Term 0 = No Term	1 = Master 0 = Slave
All bits default to the logic '0' state at power–up and resets.								

3.4.1 PROCCLK Frequency Divider – Bit D4

This bit is allows the user to ensure that the frequency of the signal that drives the PROCCLK input of the HSP50214 never exceeds 55 MHz. This signal is called PRCLK on the 6210's Sync bus. If, for example, the 64 MHz on–card crystal oscillator is the original source of the PRCLK signal, the divider can be enabled by clearing this bit to the logic '0' state (which is the default). If an external clock signal, or the Sync bus's PRCLK, is the source for PROCCLK, and the frequency of that signal is below 55 MHz, the divider can be disabled by setting this bit to the logic '1' state. Table 3–3, at the top of the next page, shows how this bit should be set dependent upon clock source selection and frequency.

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3.4 Control Register (continued)

3.4.1 PROCCLK Frequency Divider (continued)

Table 3–3: Model 6210 – Master PROCCCLK Signal Source & Frequency

Mode	A/D Clock Frequency	Clock Source*	PROCCLK_Divider Setting	Description
Master (Control Reg., D0 = 1)	< 55 MHz	EXT. CLK	1	PRCLK = Ext. CLK
		INT. OSC†	1†	PRCLK = INT. OSC.†
	> 55 MHz	EXT. CLK	0	PRCLK = EXT CLK/2
		INT. OSC	0	PRCLK = INT. OSC/2

* – The clock source is selected by the Ext_Clk Enable bit (D2, Control Register).

† – This selection is only valid if the standard, 64 MHz internal oscillator is replaced by one whose frequency is 55 MHz or less (e.g., Option. 021).

3.4.2 BIFO Disable – Bit D3

This bit is used to synchronize the mezzanine BIFOs on VIM motherboards across multiple channels. This is accomplished by first setting this bit on each channel to be synchronized to the logic '1' state, then resetting the motherboard's BIFO. When this bit is subsequently cleared to the logic '0' state (its default condition), no data is written to the BIFO until the next rising edge of the SYNC1 signal (see Section 2.4.1.4, on page 22). In this manner, data acquisition in all channels connected to the Sync Bus is started simultaneously. This bit **MUST** be cleared to the logic '0' state for normal operation.

3.4.3 External Clock Enable – Bit D2

This bit determines which signal will drive the Model 6210's Master Clock Divider (see Section 3.5). When this bit is set to the logic '1' state, the signal applied to the front panel **EXT CLK** connector is selected. When this bit is cleared to the logic '0' state (its default condition), the on–board, 64 MHz crystal oscillator is selected.

3.4.4 Termination Enable – Bit D1

This bit is set to the logic '1' state to connect termination resistors to the Model 6210's Sync bus. This should be done ONLY on the slave Model 6210 that is at the opposite end of the Sync Bus from the Sync Bus master, or on a stand–alone device that is not connected to the external Sync Bus. On all other devices, clear this bit to the logic '0' state (the default), to disconnect the terminators.

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3.4 Control Register (continued)

3.4.5 Master / $\overline{\text{Slave}}$ – Bit D0

Set this bit to the logic '1' state to configure a Model 6210 as a Sync bus master. This bit must also be set to the logic '1' state on any Model 6210 that will not be connected to a Sync Bus. To configure a Model 6210 as a Sync Bus slave, clear this bit to the logic '0' state (its default condition).

3.5 Master Clock Divider – R/W @ 'C6x Address 0x0032 0024

The Master Clock Divider register divides the master clock signal (provided by the on–card, 64 MHz oscillator or the front panel **EXT CLK** connector, see Section 3.4.3) by the quantity written to the lower byte (D7 – D0) of this register, plus one. This register should **ONLY** be written with all zeros (the register's default condition) or odd numbers, such that the actual number that the master clock frequency is divided by is either 1 or an even number. The output of this divider is applied to the ENCODE inputs of the AD6640 A/D converter, and to the front end of the HSP50214 DDR. For example, when the low byte of this register contains all zeros (their default condition), the master clock signal will be passed to the A/D's ENCODE inputs and the DDR front end unaltered (i.e., divided by 1). However, if the internal oscillator is selected, and the low byte of this register contains the quantity 7, the A/D's ENCODE frequency (and the DDR's front–end processing frequency) will be 8 MHz (64 MHz ÷ (7+1)).

Like the Control Register, the Master Clock Divider is only accessible from Processor A or Processor C on the VIM motherboard, depending upon the position in which the module is installed. Neither Processor B nor Processor D on a VIM motherboard can ever access this register. Table 3–4, below, illustrates the contents of the Model 6210's Master Clock Divider Register.

Table 3–4: Model 6210 – Master Clock Divider – R/W @ 'C6x Address 0x0032 0024

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	MSB ––– LSB							
Function	Main Clock is divided by the quantity in this field +1 to produce the Master clock for the ADC & DDR front end. This field MUST be written with either an odd number, or zero.							
All bits default to the logic '0' state at power–up and resets.								

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3.6 BIFO Decimation Register – R/W @ ‘C6x address 0x0032 0028

The Master Clock, described in Section 3.5, on the previous page, may be further divided to create the Write Enable signal for the VIM motherboard’s mezzanine BIFO. 8 bits are provided for this frequency division, in this register. Each channel (i.e., each processor on the motherboard that can access this module) has its own unique version of this register, to allow the two channels to operate at different rates. This divider works in a manner similar to the Master Clock Divider. The BIFO Write Rate is equal to the Master Clock rate divided by the 8–bit value in this register plus one. Also, the valid data values for this 8–bit field are restricted to odd numbers (which will result in even divisors) and zero (which gives a divisor of one, and is the register’s default condition). Table 3–5, below, shows the contents of this register.

Table 3–5: Model 6210 – Motherboard BIFO Decimation Register – R/W @ ‘C6x Address 0x0032 0028

Bit #	**D31 – D8**							
Name	Not Used							
Function	Write with 0’s, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	MSB– –LSB							
Function	BIFO Write Rate divisor							

All bits default to the logic ‘0’ state at power–up and resets.
The Reference Clock is divided by the quantity in this register +1
to produce the Write Enable for the Motherboard’s BIFO.
This 8–bit field MUST be written with either an odd number, or zero.
All bits default to the logic ‘0’ state at power–up and resets.

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3.7 Programmable Gain Amplifier (GAIN) – R/W @ 'C6x Address 0x0032 002C

This register controls the Model 6210's Pragrammable–Gain Amplifier (PGAmp), shown in Figure 1–1, on page 9. This register is only functional if the PGAmp has not been bypassed (see Section 3.8.3). The amplifier is the Analog Devices Model AD603, and its gain control voltage is provided by a D/A converter, specifically the LTC1451, from Linear Technology. Appendix C of this manual is the data sheet for the amplifier, and Appendix D contains the data sheet for the D/A. Both provide complete block diagrams, specifications and other pertinent information. The DAC is programmed by serially shifting in a 12–bit data word. As shown in Table 3–6, below, the 3 active bits in this register provide a chip select for the DAC, a bit to toggle to create the serial shift clock, and a data bit. When reset, and when powered on, all 3 of these bits default to the logic '0' state.

Table 3–6: Model 6210 – Programmable Gain Amplifier Register – R/W @ 'C6x 0x0032 002C

Bit #	D 3 1 – D 3	D2	D1	D0
Bit Name	Reserved	Chip_ Select	Data_ In	Serial _Clock
Bit Function	Write with Zeros, Mask when Reading	1 = Not Selected 0 = Load Data	Data to be shifted	Toggle for shift clock
All bits default to the logic '0' state at power–up and resets.				

3.7.1 Loading the 12–bit Gain Control Word

The Gain Control Register is used to serially load the 12–bit gain control word (GCW) into the LTC1451 DAC, which provides a gain control voltage for the input amplifier. The gain control word is loaded into the DAC, MSB first, by first clearing the Chip Select bit (D2) to the logic '0' state, then toggling the Serial_Clock bit (D0) for each bit of the gain control word, stored in this regis–ter's Input_Data bit, D1. The bits that comprise the gain control word are latched on the rising edge (i. e., the logic '1' to logic '0' transition) of the Serial_Clock bit. The DAC's output voltage is updated on the rising edge (i.e., the logic '0' to logic '1' transition) of the Chip_Select bit. The complete sequence for writing the 12–bit word to the DAC involves 26 write operations to this register. A complete write sequence is shown in Table 3–8, at the bot–tom of the next page.

A sample program for loading the control word into the DAC is provided in the ReadyFlow Board Support Package for the Model 6210. The Gain Control Word for 0 dB gain is 250 (decimal), or 0xFA (hex). The gain control resolution is approximately 0.04 dB per LSB of the control word. Thus, incrementing or dec–remeting the control word by 25 decimal changes the gain of the amplifier by 1 dB. Table 3–7, at the top of the next page, shows the Gain Control Word value that should be loaded into the LTC1451 for full scale input amplitudes of +10 dBm to –20 dBm (or with option 102, 0 to –30 dBm) in 10 dBm increments.

When calculating the required gain for your application, remember to take into account the input low–pass filter, which may have an insertion loss of up to 5 dB.

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3.7 Programmable Amplifier Gain (continued)

3.7.1 Loading the 12–bit Gain Control Word (continued)

Table 3–7: Model 6210 – Gain Control Word vs. Full Scale Input Amplitude

Gain Control Word		Full Scale Input Amplitude (Standard)	Full Scale Input Amplitude (Option 102)
Decimal	Hex		
250	0x00FA	10 dBm	0 dBm
500	0x01F4	0 dBm	–10 dBm
750	0x02EE	–10 dBm	–20 dBm
1000	0x03E8	–20 dBm	–30 dBm

NOTE: The values given in this table **DO NOT** account for insertion loss of the low–pass input filter, which may be as high as 5 dB.

Table 3–8: Model 6210 – Sequence for Loading Gain Control Word

Write #	Description	D2	D1	D0
–	Initial state. Chip select asserted (default power–up state).	0	0	0
1	De–assert chip select.	1	0	0
2	Assert chip select & setup bit 11, MSB of the GCW.	0	(GCW bit 11)	0
3	Latch bit 11, MSB of the GCW.	0	(GCW bit 11)	1
4	Setup bit 10 of the GCW.	0	(GCW bit 10)	0
5	Latch bit 10 of the GCW.	0	(GCW bit 10)	1
6	Setup bit 09 of the GCW.	0	(GCW bit 9)	0
7	Latch bit 09 of the GCW.	0	(GCW bit 9)	1
8	Setup bit 08 of the GCW.	0	(GCW bit 8)	0
9	Latch bit 08 of the GCW.	0	(GCW bit 8)	1
10	Setup bit 07 of the GCW.	0	(GCW bit 7)	0
11	Latch bit 07 of the GCW.	0	(GCW bit 7)	1
12	Setup bit 06 of the GCW.	0	(GCW bit 6)	0
13	Latch bit 06 of the GCW.	0	(GCW bit 6)	1
14	Setup bit 05 of the GCW.	0	(GCW bit 5)	0
15	Latch bit 05 of the GCW.	0	(GCW bit 5)	1
16	Setup bit 04 of the GCW.	0	(GCW bit 4)	0
17	Latch bit 04 of the GCW.	0	(GCW bit 4)	1
18	Setup bit 03 of the GCW.	0	(GCW bit 3)	0
19	Latch bit 03 of the GCW.	0	(GCW bit 3)	1
20	Setup bit 02 of the GCW.	0	(GCW bit 2)	0
21	Latch bit 02 of the GCW.	0	(GCW bit 2)	1
22	Setup bit 01 of the GCW.	0	(GCW bit 1)	0
23	Latch bit 01 of the GCW.	0	(GCW bit 1)	1
24	Setup bit 00, LSB of the GCW.	0	(GCW bit 0)	0
25	Latch bit 00, LSB of the GCW.	0	(GCW bit 0)	1
26	De–assert chip select.	1	0	0

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3.8 Data Format / Signal Path Register (DATA) – R/W @ 'C6x Address 0x0032 0030

Each Motherboard Processor that can access this module has a separate version of this register, which contains four active bits. There are bits used to determine whether the data delivered to the motherboard is from the A/D or the DDR and whether the programmable gain amplifier and low–pass, anti aliasing filter are in the signal path before the A/D. The other two bits determine whether or not the data applied to the DDR input is pre–decimated by a factor of two, and (if the DDR is bypassed) whether or not the A/D's output data is packed. Table 3–9, below, shows the layout of the Model 6210's Data Format/Signal Path Register, and the subsections that begin below the table describe how the bits are used.

Table 3–9: Model 6210 – Data Format / Signal Path Register – R/W @ 'C6x 0x0032 0030

Bit #	D31 – D4	D3	D2	D1	D0
Bit Name	Reserved	DDR_In_ Dec_x2	Pack_ Mode	LPF/PGAmp Bypass	DDR_ Bypass
Bit Function	Write with Zeros, Mask when Reading	1 = Decimate 0 = No Dec	1 = Pack 0 = No Pack	1 = Bypass 0 = Use	1 = Use DDR 0 = A/D Only
All bits default to the logic '0' state at power–up and resets.					

3.8.1 Decimate DDR Input by 2 – Bit D3

When this bit is set to the logic '1' state, the data delivered to the DDR by the A/D converter is decimated by a factor of 2 (i.e., all even–numbered samples are dropped). This is required if the HSP50214's internal Cascaded Integrator–Comb (CIC) filter is bypassed (i.e., if bit D6 in the Control Word 0 Register in the DDR is set to the logic '1' state). When this bit is cleared to the logic '0' state (its default condition), all data converted by the A/D is delivered to the DDR (i.e., no samples are dropped).

3.8.2 Pack Mode – Bit D2

This bit is functional ONLY if the DDR is bypassed, and the 6210 is delivering raw A/D data to the VIM motherboard (i.e., if the D0 bit in this register is cleared to the logic '0' state). If the preceding statement is true, then when this bit is set to the logic '1' state, each 32–bit longword delivered to the motherboard's BIFO by the 6210's A/D will contain two consecutive 12–bit data samples, left–justified in each 16–bit field. In this case, the low word of each longword contains the earlier sample.

If the DDR is bypassed (D0 in this register contains a '0') and this bit is cleared to the logic '0' state (the default condition), then each 32–bit word delivered to the VIM motherboard by the 6210 will contain a single 12–bit A/D sample, left justified in the lower 16–bit word.

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3.8 Data Format / Signal Path Register (continued)

3.8.2 Pack Mode (continued)

If the DDR is in the 6210's data path between the A/D and the VIM mother–board (i.e., if D0 in this register is set to the logic '1' state), then the state of this bit is ignored, and the operating mode of the HSP50214 determines the output data format (see Appendix A, the HSP50214 data sheet, for details about set–ting the operating mode of the DDR). If the DDR operates in Complex mode, each 32–bit word delivered from the 6210's DDR to the motherboard BIFO contains a 16–bit Q (quadrature or imaginary) sample in the upper word (D31 – D16), and a 16 bit I (in–phase or real) sample in the lower word (D15 – D0). If the DDR operates in Real–Only mode, each 32–bit word delivered from the 6210's DDR to the motherboard BIFO contains only one 16–bit I sample, in the low word. In all unpacked formats, the data in the upper word is indetermi–nate.

All data delivered to the motherboard BIFO by the 6210 is in signed 2's com–plement format, with the MSB of the data sample set to the logic '1' state to indicate negative data values. Table 3–10, below, illustrates the available for–mats for output data from the Model 6210.

Table 3–10: Model 6210 – Output Data to Motherboard BIFO – Packing Formats

Packed A/D Data (D2 = 1, D0 = 0)						
O/P Word #	**D31 – – – – – – – – – – – – – D20**		**D19-D16**	**D15 – – – – – – – – – – – – – D4**		**D3 - D0**
1	(MSB)	A/D Sample #2 (LSB)	? ?	(MSB)	A/D Sample #1 (LSB)	? ?
2	(MSB)	A/D Sample #4 (LSB)	? ?	(MSB)	A/D Sample #3 (LSB)	? ?
Unpacked A/D Data (D2 = 0, D0 = 0)						
O/P Word #	**D31 – – – – – – – – – – – – – – – – – D16**			**D15 – – – – – – – – – – – – – D4**		**D3 - D0**
1	Indeterminate			(MSB)	A/D Sample #1 (LSB)	??
2	Indeterminate			(MSB)	A/D Sample #2 (LSB)	??
Complex DDR Data (D2 = X, D0 = 1)						
O/P Word #	**D31 – – – – – – – – – – – – – – – – – D16**			**D15 – – – – – – – – – – – – – – – – D0**		
1	(MSB)	DDR Q Sample #1 (LSB)		(MSB)	DDR I Sample #1	(LSB)
2	(MSB)	DDR Q Sample #2 (LSB)		(MSB)	DDR I Sample #2	(LSB)
Real DDR Data (D2 = X, D0 = 1)						
O/P Word #	**D31 – – – – – – – – – – – – – – – – – D16**			**D15 – – – – – – – – – – – – – – – – D0**		
1	Indeterminate			(MSB)	DDR I Sample #1	(LSB)
2	Indeterminate			(MSB)	DDR I Sample #2	(LSB)
?? = Indeterminate, X = Don't Care						

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3.8 Data Format / Signal Path Register (continued)

3.8.2 Pack Mode (continued)

When the DDR's are bypassed, output data by the Model 6210's A/D converters is encoded in true 12–bit 2's complement format, with the remaining 4 bits of the 16–bit word in which the sample resides indeterminate. The MSB (D15) is used as a sign bit and indicates a negative input voltage when set to the logic '1' state. The maximum negative input voltage (–1 V_{DC} for the standard input signal range) results in an output data code of 1000 0000 0000 xxxx (0x800x), while an input exactly one step above half–scale (≅ + 490 mV_{DC}) produces an output code of all 12 active bits cleared to the logic '0' state. A full–scale positive input voltage (+1 V_{DC}) produces an output data code of 0111 1111 1111 xxxx (0x7FFx). Table 3–11, below, provides the output data coding scheme used by the Model 6211.

Table 3–11: Model 6210 – A/D Output Data Coding

Step (Decimal)	Input Voltage (DC, Nominal)	Binary Output Code (D15 – D0)	Hexadecimal Output Code
0	–1.00000 V	1000 0000 0000 xxxx	0x800x
1	–0.99951 V	1000 0000 0001 xxxx	0x801x
2	–0.99902 V	1000 0000 0010 xxxx	0x802x
⋮	⋮	⋮	⋮
2046	–0.00049 V	1111 1111 1110 xxxx	0xFFEx
2047	0.00000 V	1111 1111 1111 xxxx	0xFFFx
2048	+0.00049 V	0000 0000 0000 xxxx	0x000x
2049	+0.00098 V	0000 0000 0001 xxxx	0x001x
⋮	⋮	⋮	⋮
4093	+0.99902 V	0111 1111 1101 xxxx	0x7FDx
4094	+0.99951 V	0111 1111 1110 xxxx	0x7FEx
4095	+1.00000 V	0111 1111 1111 xxxx	0x7FFx
x = Indeterminate			

3.8.3 Programmable–Gain Amplifier & Low–Pass Filter Bypass – Bit D1

When this bit is set to the logic '1' state, the analog input signal is routed around the programmable–gain amplifier and the low–pass, anti aliasing filter. This allows the full bandwidth of the input signal to be delivered to the A/D converter, which is necessary in undersampling applications. For applications where undersampling is not required and it is desirable to eliminate frequency components above the Nyquist limit that may be present in the input signal, clear this bit to the logic '0' state to place the low–pass filter and programmable–gain amplifier in the signal path.

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3.8 Data Format / Signal Path Register (continued)

3.8.4 DDR Bypass – Bit D0

This bit allows the Model 6210 to function as a simple A/D converter, by routing the output data directly to the BIFO on the VIM motherboard. A/D data will bypass the Intersil HSP50214 DDR chip when this bit is cleared to the logic '0' state (its default condition). When this bit is set to the logic '1' state, the DDR is placed in the data path between the A/D converter and the motherboard's BIFO, and all of the Model 6210's digital receiver functions are available.

3.9 SYNC Generate Register (SYNC) – W.O. @ 'C6x Address 0x0032 0034

Any write operation to this register will cause the generation of a SYNC1 pulse. The data associated with the write operation is neither used nor stored and is therefore trivial. The ability to generate a SYNC1 pulse via a write operation is provided for applications in which the DDR is bypassed, because the SYNC1 pulse is usually generated by the HSP50214B DDR. This register along with the BIFO Disable bit (D3 in the Control Register, see Section 3.4.2) allow a 6210 in which the DDR is unused to become a Sync bus master.

This register is accessible only to Processor A or Processor C on the VIM motherboard, depending upon the position in which the module is installed. Neither Processor B nor Processor D on a VIM motherboard can ever access this register.

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3.10 Serial Port 0 Connection Register (SPORT) – R/W @ 'C6x Address 0x0032 0038

The Serial Port 0 Connection Register (SPORT) controls which device provides serial input to the receive section of Serial Port 0 for a processor on the VIM motherboard. The two active bits in this register comprise a field that determines the source of the serial connection. Each processor on the VIM motherboard that can access a given 6210 has a separate version of this register, whose power–up default state is both bits cleared to the logic '0' state.

Figure 1–1, on page 9 contains the block diagram of the Model 6210 and shows the various serial connections possible using this register. Table 3–12, below, shows the register's layout & summarizes the function of its lone bit–field. The connections made by the states of the bits are defined in more detail in the subsections beginning below the table.

Table 3–12: Model 6210 – Serial Port 0 Connection Register – R/W @ 'C6x 0x0032 0038

Bit #	D 3 1 – D 2	D1	D0
Bit Name	Reserved	SPort_Source_1	SPort_Source_0
Bit Function	Write with Zeros, Mask when Reading	1, 1 = Other Processor 1, 0 = Other DDR	0, 1 = Own DDR 0, 0 = Not Connected
All bits default to the logic '0' state at power–up and resets.			

3.10.1 The Other Processor's Serial Port 0 Transmit Section (D1 = 1, D0 = 1)

When a processor on the VIM motherboard sets both bits in this register to the logic '1' state, the receiver portion of that processor's Serial Port 0 will be connected to the transmit section other processor's Serial Port 0.

3.10.2 The Other Processor's DDR (D1 = 1, D0 = 0)

When a processor on the VIM motherboard sets D1 in this register to the logic '1' state and clears D0 to the logic '0' state, Serial Output A on the receiver–normally associated with the other processor (i.e., receiver 2 for processor A or C, or receiver 1 for processor B or D) will be connected to the receiver section of that processor's serial port 0.

3.10.3 The Processor's Own DDR (D1 = 0, D0 = 1)

When a processor on the VIM motherboard clears D1 in this register to the logic '0' state and sets D0 to the logic '1' state, Serial Output A on the receiver normally associated with that processor (i.e., receiver 1 for processor A or C, or receiver 2 for processor B or D) will be connected to the receiver section of that processor's serial port 0.

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3.10 Serial Port Connection Register (continued)

3.10.4 Not Connected (D1 = 0, D0 = 0)

When a processor on the VIM motherboard clears both bits in this register to the logic '0' state, the receiver section of that processor's Serial Port 0 is not connected to any other device.

3.11 CIC Gain Adjust Register– R/W @ 'C6x Address 00x0032 003C

The three active bits in this register drive the three GAINADJ pins the HSP50214B DDR chip. The GAINADJ function adds an offset to the gain via a shifter between the mixer and CIC filter (internal to the HSP50214B chip), . GAINADJ value is added to the shift code in the DDR's Control Word 0 Register, bits D16 – D13. The actual gain that can be provided in this section reaches its maximum value when the sum of the 4 CIC shift gain bits (CW0, D16 – D13), and these three Gain Adjust bits is equal to 15 (0xF). The gain adjustment provided by these 3 bits is equal to 6dB/LSB (i.e., a 1–bit change in the value stored in this register will result in a 6 dB change in the gain, thus code 002 would give 12 dB gain, code 111 would result in 42dB of gain). For additional information, please see the section entitled "Using the Input Gain Adjust Control Signals" in the Intersil HSP50214B data sheet, Appendix A of this manual.

Table 3–13: Model 6210 – CIC Gain Adjust Register – R/W @ 'C6x 0x0032 003C

Bit #	D 3 1 – D 4	D2	D1	D0
Bit Name	Reserved	Gain Adj_2	Gain Adj_1	Gain Adj_1
Bit Function	Write with Zeros, Mask when Reading	Gain applied before CIC filter is changed by 6dB/LSB in this field.		
All bits default to the logic '0' state at power–up and resets.				

3.12 Processor Interface the HSP50214 DDR

The remaining registers in the Model 6210's memory map provide the means by which processors on the VIM motherboard can write control information to, and read status data from, the HSP50214 DDR chip. These resources include four holding registers for temporary storage of write/read data, a destination address register for writes, a source address register for reads and a dedicated register for the data returned by sta–tus reads. Table 3–14, at the top of the next page, summarizes the functions & addresses of these registers. The text that follows the table describes how these resources are used to communicate with the DDR.

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3.12 Processor Interface the HSP50214 DDR (continued)

Table 3–14: Model 6210 – DDR Interface Resources

'C6X Address	Register Description	Mnemonic	Access	Function
0x0032 0040	DDR Holding Register 0	DDR0	R/W	Control Word D0:D7
0x0032 0044	DDR Holding Register 1	DDR1	R/W	Control Word D8:D15
0x0032 0048	DDR Holding Register 2	DDR2	R/W	Control Word D16:D23
0x0032 004C	DDR Holding Register 3	DDR3	R/W	Control Word D24:D31
0x0032 0050	DDR Write Destination Address Register	DDR4	R/W	Control Register to Write
0x0032 0054	DDR Read Source Register	DDR5	R/W	Source of Read Data
0x0032 005C	DDR Status Read Register	DDR6	R. O.	Status Register

The 6210's write interface to the HSP50214 uses an indirect addressing scheme wherein a 32–bit data word is first loaded into four 8–bit master registers internal to the DDR chip from the 8 LSB's of the four DDR Holding Registers on the 6210 (DDR0 – DDR3). The address of the desired destination register in the DDR is then written to the 6210's DDR Write Destination Address Register (DDR4). Writing this address triggers a circuit that generates a pulse, synchronous to a clock, that loads the HSP 50214's internal Destination Register. The sync circuits and data words are synchronized to different clocks (CLKIN or PROCCLK) depending on the registers affected by a given write operation. For additional information, you may refer to the "Microprocessor Write" section of the HSP50214 data sheet, in Appendix A of this manual.

The 6210's read interface to the HSP50214 uses both read and write operations to obtain data from the DDR. First, a 3–bit "read code" must be written must to the 6210's DDR Read Source Register to select the source of data to be read. The data sources selected by the various read codes are listed in Table 3–15, at the top of the next page. Writing to the Read Source register will cause the 6210 to initiate a readout cycle, which will transfer the requested data from the selected source to the 8 LSBs of some or all of the 6210's four DDR holding registers (DDR0 – DDR3), depending upon the specific data source. For additional information, please refer to the "Microprocessor Read" section of the HSP50214 data sheet, in Appendix A of this manual.

An additional register has been provided to allow the user to easily obtain status infor–mation from the HSP50214. Reading the DDR Status Read Register (DDR6), will return the status bits shown in Table 3–16, at the bottom of the next page. This topic is also covered in the "Microprocessor Read" section of Appendix A.

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3.12 Processor Interface the HSP50214 DDR (continued)

Table 3–15: Model 6210 – DDR Read Source Definitions			
Read Code (D2 : D0)	**Data Source**	**Data Returned**	
		Type	**Where**
000	I & Q Buffer RAM	I (LSB)	DDR0
		I (MSB)	DDR1
		Q (LSB)	DDR2
		Q (MSB)	DDR3
001	Magnitude & Phase Buffer RAM	Mag (LSB)	DDR0
		Mag (MSB)	DDR1
		Phase (LSB)	DDR2
		Phase (MSB)	DDR3
010	Buffered Frequency	Freq (LSB)	DDR0
		Freq (MSB)	DDR1
011	Not Used	Not Applicable	
100	Input Level Detector	Input AGC (LSB)	DDR0
		Input AGC (NSB)	DDR1
		Input AGC (MSB)	DDR2
101	Not Used	Not Applicable	
110			
111			

Table 3–16: Model 6210 – DDR Status Read Register – R/W @ 'C6x 0x0032 003C								
Bit #	**D31 – D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved	Internal_FIFO_Depth			Internal_ FIFO_Empty	Internal_ FIFO_Full	Buffer_ Ready	Integration_ Complete
Bit Function	Mask on Reads	# of 80–bit (16–bit I, Q, |r|, ϕ& f) samples in Internal FIFO			1 = True 0 = False		1 = Not Ready 0 = Ready	1 = Complete 0 = Incomplete
All bits default to the logic '0' state at power–up and resets.								

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Appendix A: Intersil HSP50214B – Programmable Downconverter

Included for your reference on the following pages is the data sheet for the HSP50214B Programmable Downconverter, provided by the courtesy of Intersil Corp., Palm Bay FL. Please note that this device is referred to as a Digital Drop Receiver (DDR) in the body of this manual, whreras the manufacturer uses the term Programmable Downconverter (PDC). These are application–oriented terms, used to refer to devices that perform essen–tially identical functions.

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Data Sheet May 2000 File Number 4450.3

Programmable Downconverter

The HSP50214B Programmable Downconverter converts digitized IF data into filtered baseband data which can be processed by a standard DSP microprocessor. The Programmable Downconverter (PDC) performs down conversion, decimation, narrowband low pass filtering, gain scaling, resampling, and Cartesian to Polar coordinate conversion.

The 14-bit sampled IF input is down converted to baseband by digital mixers and a quadrature NCO, as shown in the Block Diagram. A decimating (4 to 32) fifth order Cascaded Integrator-Comb (CIC) filter can be applied to the data before it is processed by up to 5 decimate-by-2 halfband filters. The halfband filters are followed by a 255-tap programmable FIR filter. The output data from the programmable FIR filter is scaled by a digital AGC before being re-sampled in a polyphase FIR filter. The output section can provide seven types of data: Cartesian (I, Q), polar (R, θ), filtered frequency ($d\theta/dt$), Timing Error (TE), and AGC level in either parallel or serial format.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP50214BVC	0 to 70	120 Ld MQFP	Q120.28x28
HSP50214BVI	-40 to 85	120 Ld MQFP	Q120.28x28

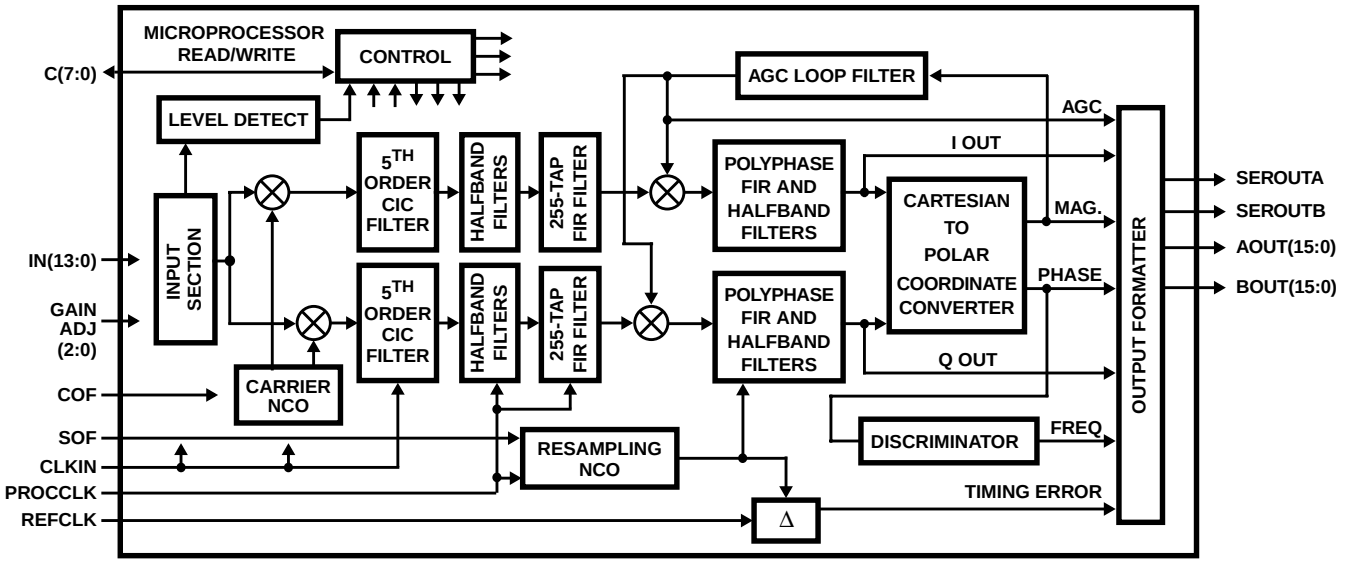
Features

- Up to 65 MSPS Front-End Processing Rates (CLKIN) and 55MHz Back-End Processing Rates (PROCCLK) Clocks May Be Asynchronous
- Processing Capable of >100dB SFDR
- Up to 255-Tap Programmable FIR
- Overall Decimation Factor Ranging from 4 to 16384
- Output Samples Rates to ≅12.94 MSPS with Output Bandwidths to ≅ 982kHz Lowpass
- 32-Bit Programmable NCO for Channel Selection and Carrier Tracking
- Digital Resampling Filter for Symbol Tracking Loops and Incommensurate Sample-to-Output Clock Ratios
- Digital AGC with Programmable Limits and Slew Rate to Optimize Output Signal Resolution; Fixed or Auto Gain Adjust
- Serial, Parallel, and FIFO 16-Bit Output Modes
- Cartesian to Polar Converter and Frequency Discriminator for AFC Loops and Demodulation of AM, FM, FSK, and DPSK
- Input Level Detector for External I.F. AGC Support

Applications

- Single Channel Digital Software Radio Receivers
- Base Station Rx's: AMPS, NA TDMA, GSM, and CDMA
- Compatible with HSP50210 Digital Costas Loop for PSK Reception
- Evaluation Platform Available

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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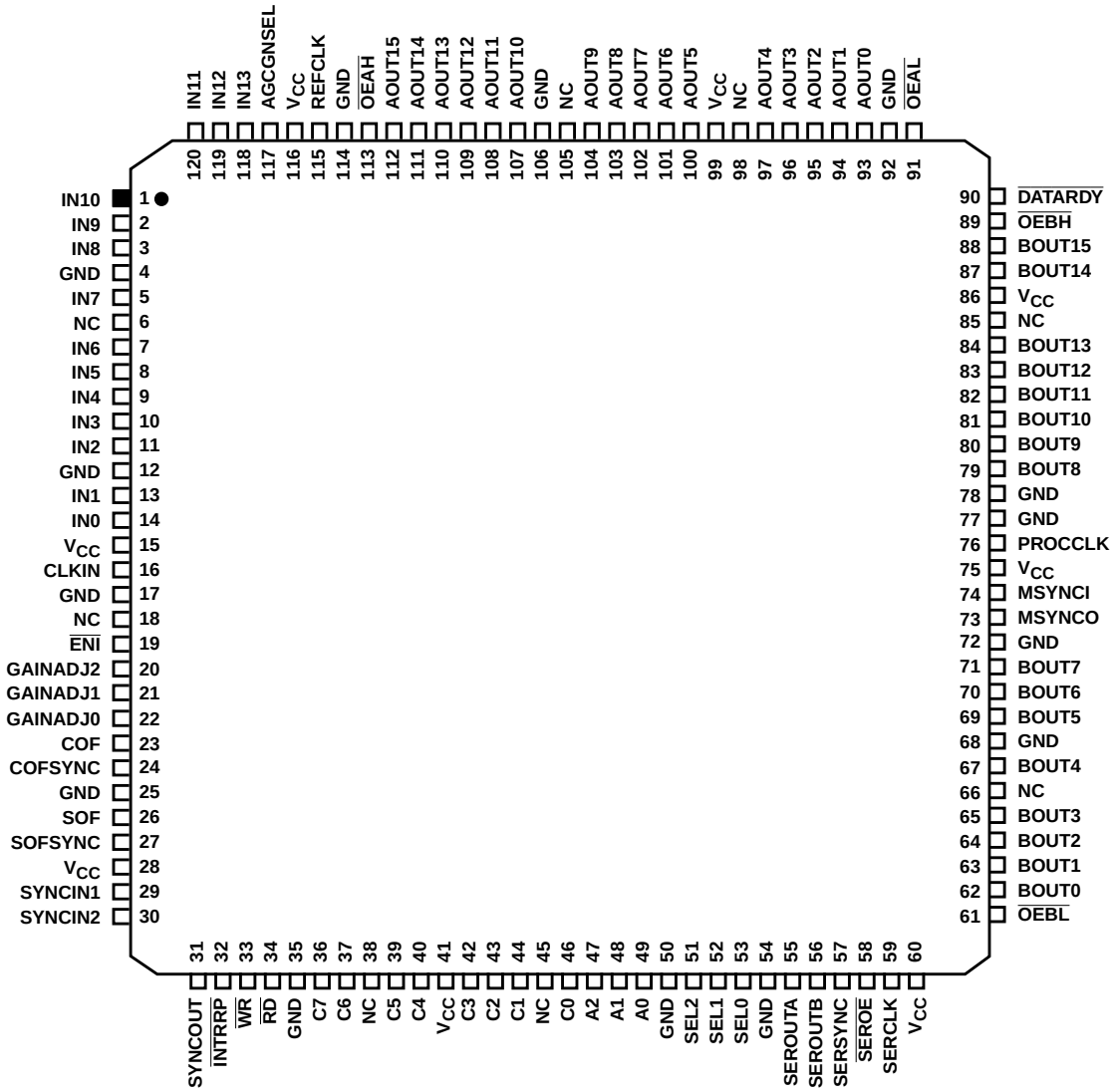
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Pinout

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Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}	-	Positive Power Supply Voltage.
GND	-	Ground.
CLKIN	I	Input Clock. This clock should be a multiple of the input sample rate. All input section processing occurs on the rising edge of CLKIN. The frequency of CLKIN is designated f_{CLKIN}.
IN(13:0)	I	Input Data. The format of the input data may be set to offset binary or 2's complement. IN13 is the MSB (see Control Word 0).
$\overline{ENI}$	I	Input Enable. Active Low. This pin enables the input to the part in one of two modes, gated or interpolated (see Control Word 0). In gated mode, one sample is taken per CLKIN when $\overline{ENI}$ is asserted. The input sample rate is designated f_S, which can be different from f_{CLKIN} when $\overline{ENI}$ is used.
GAINADJ(2:0)	I	GAINADJ Input. Adds an offset to the gain via the shifter following the mixer. GAINADJ value is added to the shift code from the microprocessor (µP) interface. The shift code is saturated to a maximum code of F. The gain is offset by (6dB)(GAINADJ); (000 = 0dB gain adjust; 111 = 42dB gain adjust) GAINADJ2 is the MSB. See "Using the Input Gain Adjust Control Signals" Section.
PROCCLK	I	Processing Clock. PROCCLK is the clock for all processing functions following the CIC Section. Processing is performed on PROCCLK's rising edge. All output timing is derived from this clock. ***NOTE: This clock may be asynchronous to CLKIN.***
AGCGNSEL	I	AGC Gain Select. This pin selects between two AGC loop gains. This input is setup and held relative to PROCCLK. Gain setting 1 is selected when AGCGNSEL = 1.
COF	I	Carrier Offset Frequency Input. This serial input pin is used to load the carrier offset frequency into the Carrier NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32 bits. The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
COFSYNC	I	Carrier Offset Frequency Sync. This signal is asserted one CLK before the most significant bit (MSB) of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
SOF	I	Re-Sampler Offset Frequency Input. This serial input pin is used to load the offset frequency into the Re-Sampler NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32 bits. The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
SOFSYNC	I	Re-Sampler Offset Frequency Sync. This signal is asserted one CLK before the MSB of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
AOUT(15:0)	O	Parallel Output Bus A. Two parallel output modes are available on the HSP50214B. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of AOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. AOUT15 is the MSB. In this mode, the AOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. For this mode, the output choices are: I, |r|, or f. The format is 2's complement, except for magnitude, which is unsigned binary with a zero as the MSB. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a data type is selected using SEL(2:0). Up to 7 data sets are stored in the Buffer RAM Output Port. The LSBytes of the AOUT and BOUT busses form the 16 bits for the buffered output mode and can be used for buffered mode while the MSBytes are outputting data in the direct output mode. For this mode, the output formats are the same as the Direct Output Port mode.
BOUT(15:0)	O	Parallel Output Bus B. Two parallel output modes are available on the HSP50214B. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of BOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. BOUT15 is the MSB. In this mode, the BOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. For this mode, the output choices are: Q, ϕ, or |r|. The format is 2's complement, except for magnitude which is unsigned binary with a zero as the MSB. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a particular information is selected using SEL(2:0). Up to 7 data sets is stored in the Buffer RAM Output Port. The least significant byte of BOUT can be used to either output the least significant byte of the B Parallel Direct Output Port or the least significant byte of the Buffer RAM Output Port. See Output Section. For this mode the output formats are the same as the Direct Output Port mode.

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Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{DATARDY}}$	O	Output Strobe Signal. Active Low. Indicates when new data from the Direct Output Port Section is available. DATARDY is asserted for one PROCCLK cycle during the first clock cycle that data is available on the parallel out busses. See Output Section.
$\overline{\text{OEAH}}$	I	Output enable for the MSByte of the AOUT bus. Active Low. The AOUT MSByte outputs are three-stated when $\overline{\text{OEAH}}$ is high.
$\overline{\text{OEAL}}$	I	Output enable for the LSByte of the AOUT bus. Active Low. The AOUT LSByte outputs are three-stated when $\overline{\text{OEAL}}$ is high.
$\overline{\text{OEBH}}$	I	Output enable for the MSByte of the BOUT bus. Active Low. The BOUT MSByte outputs are three-stated when $\overline{\text{OEBH}}$ is high.
$\overline{\text{OEBL}}$	I	Output enable for the LSByte of the BOUT bus. Active Low. The BOUT LSByte outputs are three-stated when $\overline{\text{OEBL}}$ is high.
SEL(2:0)	I	Select Address is used to choose which information in a data set from the Buffer RAM Output Port is sent to the least significant bytes of AOUT and BOUT. SEL2 is the MSB.
$\overline{\text{INTRRP}}$	O	Interrupt Output. Active Low. This output is asserted for 8 PROCCLK cycles when the Buffer RAM Output Port is ready for reading.
SEROUTA	O	Serial Output Bus A Data. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SEROUTB	O	Serial Output Bus B Data. Contents may be related to SEROUTA. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SERCLK	O	Output Clock for Serial Data Out. Derived from PROCCLK as given by Control Word 20 in the Microprocessor Write Section.
SERSYNC	O	Serial Output Sync Signal. Serves as serial data strobes. See Output Section and Microprocessor Write Section.
$\overline{\text{SEROE}}$	I	Serial Output Enable. When high, the SEROUTA, SEROUTB, SERCLK, and SERSYNC signals are set to a high impedance.
C(7:0)	I/O	Processor Interface Data Bus. See Microprocessor Write Section. C7 is the MSB.
A(2:0)	I	Processor Interface Address Bus. See Microprocessor Write Section. A2 is the MSB.
$\overline{\text{WR}}$	I	Processor Interface Write Strobe. C(7:0) is written to Control Words selected by A(2:0) in the Programmable Down Converter on the rising edge of this signal. See Microprocessor Write Section.
$\overline{\text{RD}}$	I	Processor Interface Read Strobe. C(7:0) is read from output or status locations selected by A(2:0) in the Programmable Down Converter on the falling edge of this signal. See Microprocessor Read Section.
REFCLK	I	Reference Clock. Used as an input clock for the timing error detector. The timing error is computed relative to REFCLK. REFCLK frequency must be less than or equal to PROCCLK/2.
MSYNCO	O	Multiple Chip Sync Output. Provided for synchronizing multiple parts when CLKIN and PROCCLK are asynchronous. MSYNCO is the synchronization signal between the input section operating under CLKIN and the back end processing operating under PROCCLK. This output sync signal from one part is connected to the MSYNCI signal of all the HSP50214Bs.
MSYNCI	I	Multiple Chip Sync Input. The MSYNCI pin of all the parts should be tied to the MSYNCO of one part. ***NOTE: MSYNCI must be connected to an MSYNCO signal for operation.***
SYNCIN1	I	CIC Decimation/Carrier NCO Update Sync. Can be used to synchronize the CIC Section, carrier NCO update, or both. See the Multiple Chip Synchronization Section and Control Word 0 in the Microprocessor Write Section. Active High.
SYNCIN2	I	FIR/Timing NCO Update/AGC Gain Update Sync. Can be used to synchronize the FIR, Timing NCO update, AGC gain update, or any combination of the above. See the Multiple Chip Synchronization Section and Control Words 7, 8, and 10 in the Microprocessor Write Section. Active High.
SYNCOUT	O	Strobe Output. This synchronization signal is generated by the µP interface for synchronizing multiple parts. Can be generated by PROCLK or CLKIN (see Control Word 0 and Control Word 24 in the Microprocessor Write Section). Active High.

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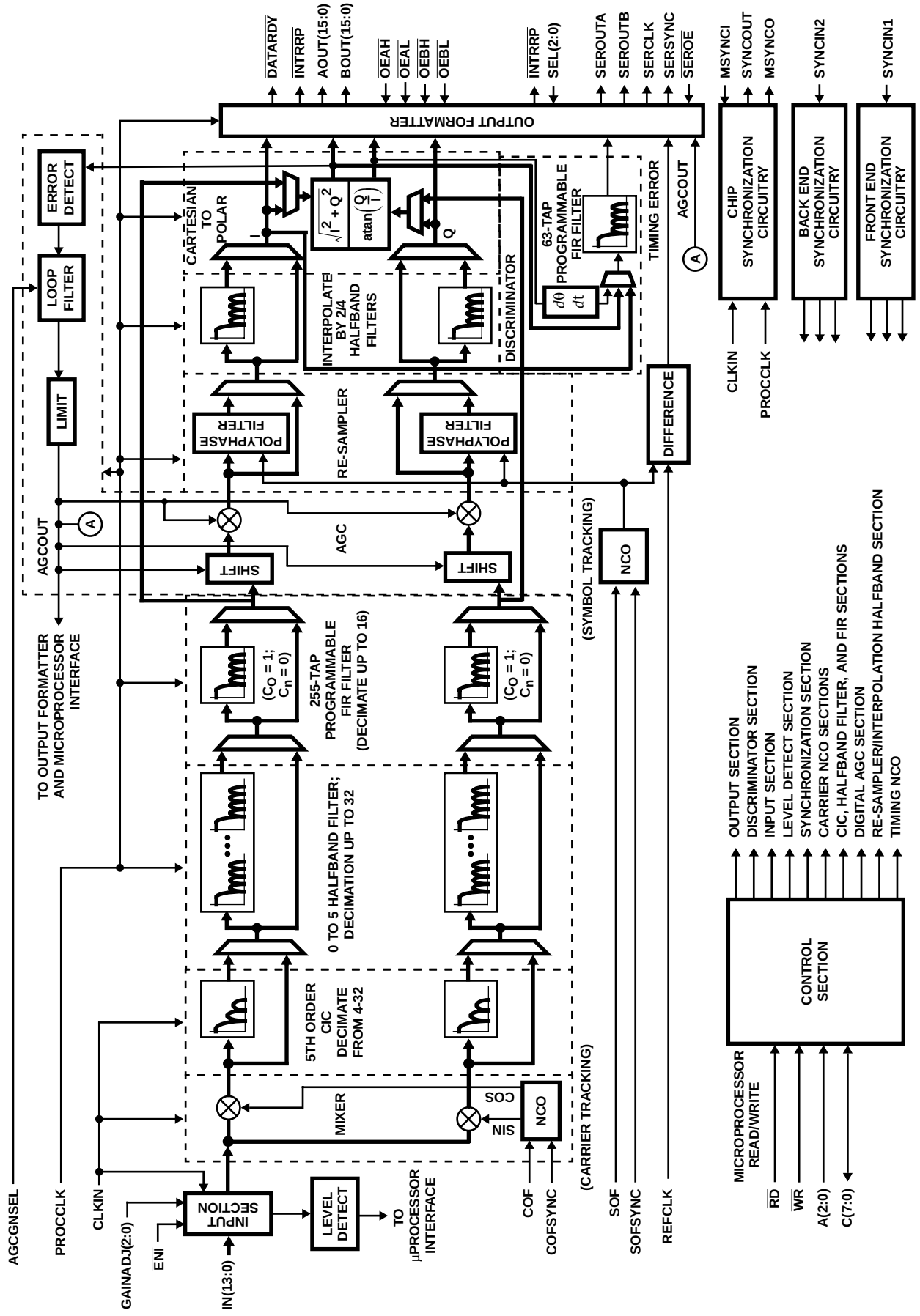


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE HSP50214B PROGRAMMABLE DOWNCONVERTER

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Functional Description

The HSP50214B Programmable Downconverter (PDC) is an agile digital tuner designed to meet the requirements of a wide variety of communications industry standards. The PDC contains the processing functions needed to convert sampled IF signals to baseband digital samples. These functions include LO generation/mixing, decimation filtering, programmable FIR shaping/bandlimiting filtering, resampling, Automatic Gain Control (AGC), frequency discrimination and detection as well as multi-chip synchronization. The HSP50214B interfaces directly with a DSP microprocessor to pass baseband and status data.

A top level functional block diagram of the HSP50214B is shown in Figure 1. The diagram shows the major blocks and multiplexers used to reconfigure the data path for various architectures. The HSP50214B can be broken into 13 sections: Synchronization, Input, Input Level Detector, Carrier Mixer/Numerically Control Oscillator (NCO), CIC Decimating Filter, Halfband Decimating Filter, 255-Tap Programmable FIR Filter, Automatic Gain Control (AGC), Re-sampler/Halfband Filter, Timing NCO, Cartesian to Polar Converter, Discriminator, and Output Sections. All of these sections are configured through a microprocessor interface.

The HSP50214B has three clock inputs; two are required and one is optional. The input level detector, carrier NCO, and CIC decimating filter sections operate on the rising edge of the input clock, CLKIN. The halfband filter, programmable FIR filter, AGC, Re-Sampler/Halfband filters, timing NCO, discriminator, and output sections operate on the rising edge of PROCCLK. The third clock, REFCLK, is used to generate timing error information.

NOTE: All of the clocks may be asynchronous.

PDC Applications Overview

This section highlights the motivation behind the key programmable features from a communications system level perspective. These motivations will be defined in terms of ability to provide DSP processing capability for specific modulation formats and communication applications. The versatility of the Programmable Downconverter can be intimidating because of the many Control Words required for chip configuration. This section provides system level insight to help allay reservations about this versatile DSP product. It should help the designer capitalize on the greatest feature of the PDC - ***VERSATILITY THROUGH PROGRAMMABILITY***. It is this feature, when fully understood, that brings the greatest return on design investment by offering a single receiver design that can process the many waveforms required in the communications marketplace.

FDM Based Standards and Applications

Table 1 provides an overview of some common frequency division multiplex (FDM) base station applications to which the PDC can be applied. The PDC provides excellent selectivity for frequency division multiple access (FDMA) signals. This high selectivity is achieved with 0.012Hz resolution frequency control of the NCO and the sharp filter responses capable with a 255-tap, 22-bit coefficient FIR filter. The 16-bit resolution out of the Cartesian to Polar Coordinate Converter are routed to the frequency detector, which is followed by a 63-tap, 22-bit coefficient FIR filter structure for facilitating FM and FSK detection. The 14-bit input resolution is the smallest bit resolution found throughout the conversion and filtering sections, providing excellent dynamic range in the DSP processing. A unique input gain scaler adds an additional 42dB of range to the input level variation, to compensate for changes in the analog RF front end receive equipment. Synchronization circuitry allows precise timing control of the base station reconfiguration for all receive channels simultaneously. Portions of this table were corroborated with reference [2].

TABLE 1. CELLULAR PHONE BASE STATION APPLICATIONS USING FDMA

STANDARD	AMPS (IS-91)	MCS-L1 MCS-L2	NMT-400 NMT-900	C450	ETACS NTACS
RX BAND (MHz)	824-849	925-940	453-458 890-915	451-456	871-904 915-925
CHANNEL BW (kHz)	30	25.0 12.5	25 12.5	20.0 10.0	25.0 12.5
# TRAFFIC CHANNELS	832	600 1200	200 1999	222 444	1240 800
VOICE MODULATION	FM	FM	FM	FM	FM
PEAK DEVIATION (kHz)	12	5	5	4	9.5
CONTROL MODULATION	FSK	FSK	FSK	FSK	FSK
PEAK DEVIATION (kHz)	8	4.5	3.5	2.5	6.4
CONTROL CHANNEL RATE (Kbps)	10	0.3	1.2	5.3	8

TDM Based Standards and Applications

Table 2 provides an overview of some common Time Division Multiplexed (TDM) base station applications to which the PDC can be applied. For time division multiple access (TDMA) applications, such as North American TDMA (IS136), where 30kHz is the received band of interest for the PCS basestation, the PDC offers 0.012Hz frequency resolution in downconversion in addition to $\alpha = 0.35$ matched (programmable) filtering capability. The $\pi/4$ DPSK modulation can be processed using the PDC Cartesian to Polar coordinate converter and $d\phi/dt$ detector circuitry or by

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processing the I/Q samples in the DSP µP. The PDC provides the ability to change the received signal gain and frequency, synchronous with burst timing. The synchronous gain adjustment allows the user to measure the power of the signal at the A/D at the end of a burst, and synchronously reload that same gain value at the arrival of the next user burst.

For applications other than cellular phones (where the preambles are not changed), the PDC frequency discriminator output can be used to obtain correlation on the preamble pattern to aid in burst acquisition.

TABLE 2. CELLULAR BASESTATION APPLICATIONS USING TDMA

STANDARD	GSM	PCN	IS-54
TYPE	Cellular	Cellular	Cellular
BASESTATION RX BAND (MHz)	935-960	1805-1880	824-849
CHANNEL BW (kHz)	200	200	30
# TRAFFIC CHANNELS	8	16	3
VOICE MODULATION	GMSK	GMSK	π/4 DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6
CONTROL MODULATION	GMSK	GMSK	π/4 DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6

Several applications are combinations of frequency and time domain multiple access schemes. For example, GSM is a TDMA signal that is frequency hopped. The individual channels contain Gaussian MSK modulated signals. The PDC again offers the 0.012Hz tuning resolution for de-hopping the received signal. The combination of halfband and 256-tap programmable, 22-bit coefficient FIR filters readily performs the necessary matched filtering for demodulation and optimum detection of the GMSK signals.

CDMA Based Standards and Applications

For Code Division Multiple Access (CDMA) type signals, the PDC offers the ability to have a single wideband RF front end, from which it can select a single spread channel of interest. The synchronization circuitry provides for easy control of multiple PDC for applications where multiple received signals are required, such as base-stations.

In IS-95 CDMA, the receive signal bandwidth is approximately 1.2288MHz wide with many spread spectrum channel in the band. The PDC supplies the downconversion and filtering required to receive a single RF channel in the presence of strong adjacent interference. Multiple PDC's would be sourced from a single receive RF chain, each processing a different receive frequency channel. The despreader would usually follow the PDC. In some very specific applications, with short, fixed codes, the filtering and despreading may be possible with innovative use of the programmable, 22-bit coefficient FIR filter. The PDC offers 0.012Hz resolution on tuning to the desired receive channel and excellent rejection of the portions of the band not being processed, via the halfband and 255-tap programmable, 22-bit coefficient FIR filter.

Traditional Modulation Formats

AM, ASK, FM AND FSK

The PDC has the capability to fully demodulate AM and FM modulated waveforms. The PDC outputs 15 bits of amplitude or 16 bits of frequency for these modulation formats. The FM discriminator has a 63-tap programmable, 22-bit coefficient FIR filter for additional signal conditioning of the FM signal. Digital versions of these formats, ASK and FSK are also readily processed using the PDC. Just as in the AM modulated case, ASK signals will use 15-bit magnitude output of the Cartesian to Polar Coordinate converter. Multi-tone FSK can be processed several ways. The frequency information out of the discriminator can be used to identify the received tone, or the filter can be used to identify and power detect a specific tone of the received signal. AMPS is an example of an FM application.

PM AND PSK

The PDC provides the downconversion, demodulation, matched filtering and coordinate conversion required for demodulation of PM and PSK modulated waveforms. These modulation formats will require external carrier and symbol timing recovery loop filters to complete the receiver design. The PDC was designed to interface with the HSP50210 Digital Costas Loop to implement the carrier phase and symbol timing recovery loop filters (for continuous PSK signals - not burst).

Digital modulation formats that combine amplitude and phase for symbol mapping, such as m-ary QAM, can also be downconverted, demodulated, and matched filtered. The received symbol information is provided with 16 bits of resolution in either Cartesian or Polar coordinates to facilitate remapping into bits and to recover the carrier phase. External Symbol mapping and Carrier Recovery Loop Filtering is required for this waveform.

Resampling and Interpolation Filters

Two key features of the resampling FIR filter are that the re-sampler filter allows the output sample rate to be programmed with millihertz resolution and that the output sample rate can be phase locked to an independent separate clock. The re-sampler frees the front end sampling clocks from having to be synchronous or integrally related in rate to the baseband output. The asynchronous relationship between front end and back end clocks is critical in applications where ISDN interfaces drive the baseband interfaces, but the channel sample rates are not related in any way. The interpolation halfband filters can increase the rate of the output when narrow frequency bands are being processed. The increase in output rate allows maximum use of the programmable FIR while preserving time resolution in the baseband data.

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14-Bit Input and Processing Resolution

The PDC maintains a minimum of 14 bits of processing resolution through to the output, providing over 84dB of dynamic range. The 18 bits of resolution on the internal references provide a spurious floor that is better than 98dBc. Furthermore, the PDC provides up to 42dB of gain scaling to compensate for any change in gain in the RF front end as well as up to 96dB of gain in the internal PDC AGC. This gain maximizes the output resolution for small signals and compensates for changes in the RF front end gain, to handle changes in the incoming signal.

Summary

The greatest feature of the PDC is its ability to be reconfigured to process many common standards in the communications industry. Thus, a single hardware element can receive and process a wide variety of signals from PCS to traditional cellular, from wireless local loop to SATCOM. The high resolution frequency tuning and narrowband filtering are instrumental in almost all of the applications.

Multiple Chip Synchronization

Multiple PDCs are synchronized using a MASTER/SLAVE configuration. One part is responsible for synchronizing the front end internal circuitry using CLKIN while another part is responsible for synchronizing the backend internal circuitry using PROCCLK.

The PDC is synchronized with other PDCs using five control lines: SYNCOUT, SYNCIN1, SYNCIN2, MSYNCO, and MSYNCI. Figure 2 shows the interconnection of these five signals for multiple chip synchronization where different sources are used for CLKIN and PROCCLK.

PDC A is the Master sync through MSO.

PDC B configures the CLKIN sync through SYNCIN1.

PDC A configures the PROCCLK sync through SYNCIN2.

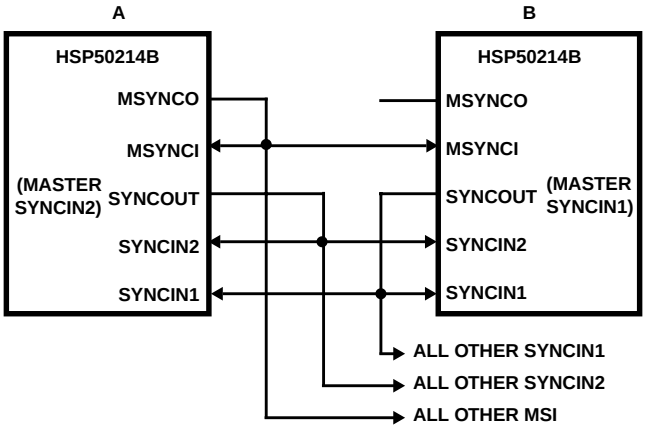


FIGURE 2. SYNCHRONIZATION CIRCUIT

SYNCOUT for PDC B should be set to be synchronous with CLKIN (Control Word 0, Bit 3 = 0. See the Microprocessor Write Section). SYNCOUT for PDC B is tied to the SYNCIN1 of all the PDCs. The SYNCIN1 can be programmed so that the carrier NCO and/or the 5th order CIC filter of all PDCs can be synchronously loaded/updated using SYNCIN1. See Control Word 0, Bits 19 and 20 in the Microprocessor Write Section for details.

SYNCOUT for one of the PDC's other than PDC B, should be set for PROCCLK (bit 3 = 1 in Control Word 0). This output signal is tied to the SYNCIN2 of all PDCs. The SYNCIN2 can be programmed so that the AGC updates its accumulator with the contents in the master registers (Control Word 8, Bit 29 in the Microprocessor Write Section). SYNCIN2 is also used to load or reset the timing NCO using bit 5, Control Word 11. The halfband and FIR filters can be reset on SYNCIN2 using Control Word 7, Bit 21. The MSYNCO of one of the PDCs is then used to drive the MSYNCI of all the PDCs (including its own).

For application configurations where CLKIN and PROCCLK have the same source, SYNCIN1 and SYNCIN2 can be tied together. However, if different enabling is desired for the front end and backend processing of the PDC's, these signals can still be controlled independently.

In the HSP50214B, the Control Word 25 reset signal has been extended so that the front end reset is 10 CLKIN periods wide and the back end reset is 10 PROCCLK periods wide. This guarantees that no enables will be caught in the pipelines. In addition, the SYNCIN1 internal reset signal, which is enabled by setting Control Word 7, Bit 21 = 1, has been extended to 10 cycles.

In summary, SYNCIN1 is used to update carrier phase offset, update carrier center frequency, reset CIC decimation counters and reset the carrier NCO (clear the feedback in the NCO). SYNCIN2 is used to reset the HB filter, FIR filter, re-sampler/HB state machines and the output FIFO, load a new gain into the AGC and load a new re-sampler NCO center frequency and phase offset.

Input Section

The block diagram of the input controller is provided in Figure 3. The input can support offset binary or two's complement data and can be operated in gated or interpolated mode (see Control Word 0 from the Microprocessor Write Section). The gated mode takes one sample per clock when the input enable (ENI) is asserted. The gated mode allows the user to synchronize a low speed sampling clock to a high speed CLKIN.

The interpolated mode allows the user to input data at a low sample rate and to zero-stuff the data prior to filtering. This zero stuffing effectively interpolates the input signal up to the rate of the input clock (CLKIN). This interpolated mode allows the part to be used at rates where the sampling frequency is above the maximum input rate range of the halfband filter section, and where the desired output bandwidth is too wide to use a Cascaded Integrator Comb (CIC) filter without significantly reducing the dynamic range.

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See Figures 4-7 for an interpolated input example, detailing the associated spectral results.

Interpolation Example:

The specifications for the interpolated input example are:

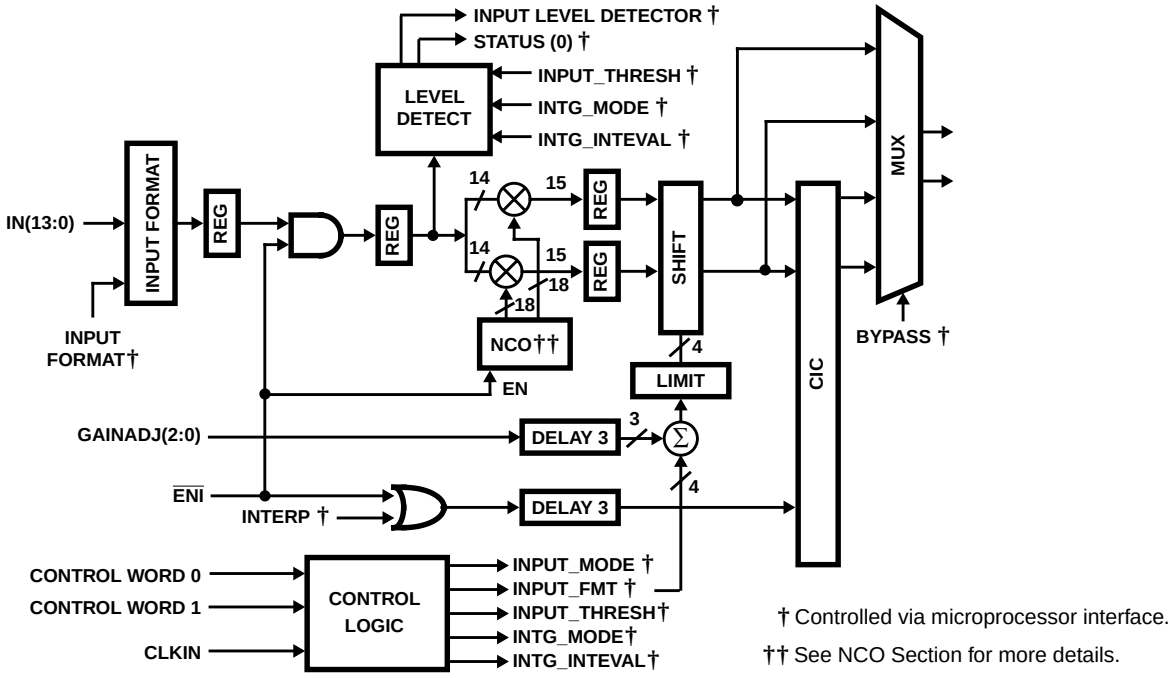
CLKIN = 40MHz
Input Sample Rate = 5 MSPS
PROCCLK = 28MHz
Interpolate by 8, Decimate by 10
Desired 85dB dynamic range output bandwidth = 500kHz

Input Level Detector

The Input Level Detector Section measures the average magnitude error at the PDC input for the microprocessor by comparing the input level against a programmable threshold and then integrating the result. It is intended to provide a gain error for use in an AGC loop with either the RF/IF or A/D converter stages (see Figure 8). The AGC loop includes Input Level Detector, the microprocessor and an external gain control amplifier (or attenuator). The input samples are rectified and added to a threshold programmed via the microprocessor interface, as shown in Figure 9. The bit weighting of the data path through the input threshold detector is shown in Figure 10. The threshold is a signed number, so it should be set to the inverse of the desired input level. The threshold can be set to zero if the average input level is desired instead of the error. The sum of the threshold and the absolute value of the input is accumulated in a 32-bit accumulator. The accumulator can handle up to 2^{18} samples without overflow. The integration time is controlled by an 18-bit counter. The integration counter preload (ICPrel) is programmed via the microprocessor interface through Control Word 1. Only the upper 16 bits are programmable. The 2 LSBs are always zero. Control Word 1, Bits 29-14 are programmed to:

$$ICPrel = (N)/4 + 1 \quad \text{(EQ. 1)}$$

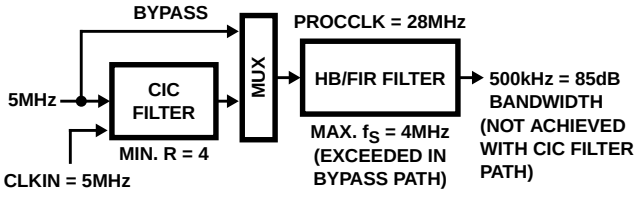
where N is the desired integration period, defined as the number of input samples to be integrated. N must be a multiple of 4: [0, 4, 8, 12, 16 .... , 2^{18}].



† Controlled via microprocessor interface.

†† See NCO Section for more details.

FIGURE 3. BLOCK DIAGRAM OF THE INPUT SECTION



Without Interpolation, the CIC bypass path exceeds the HB/FIR filter input sample rate and the CIC filter path will not yield the desired 85dB dynamic range band width of 500kHz.

FIGURE 4. STATEMENT OF THE PROBLEM

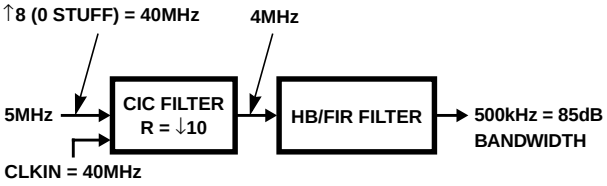


FIGURE 5. BLOCK DIAGRAM OF THE INTERPOLATION APPROACH

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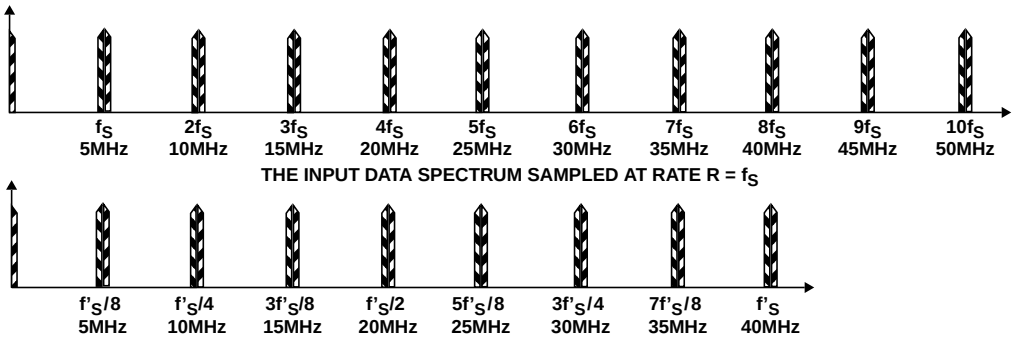


FIGURE 6. INTERPOLATION SPECTRUM: INTERPOLATE BY 8 THE INPUT DATA WITH ZERO STUFFING; SAMPLE AT RATE R = f's

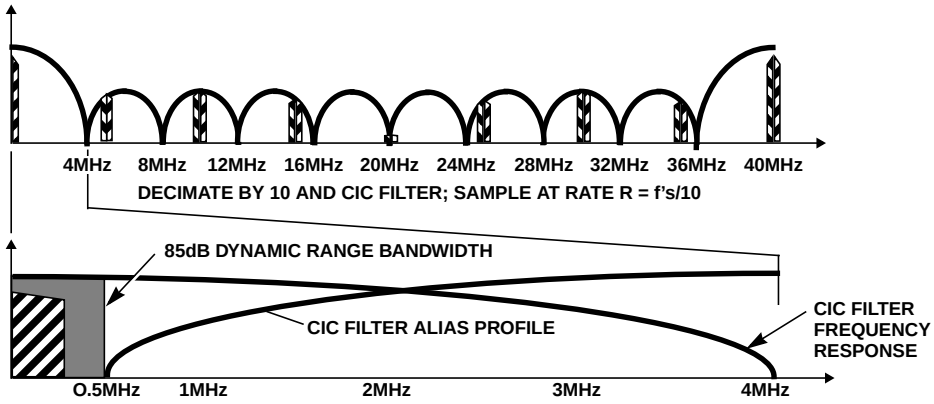


FIGURE 7. ALIAS PROFILE AND THE 85dB DYNAMIC RANGE BANDWIDTH

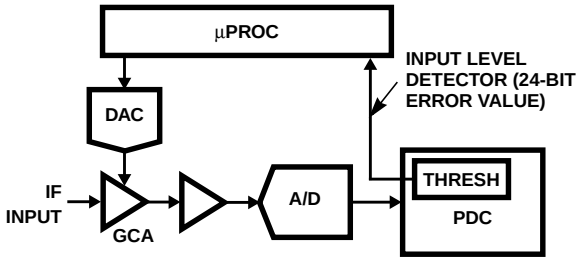


FIGURE 8. PROCESSOR BASED EXTERNAL IF AGC

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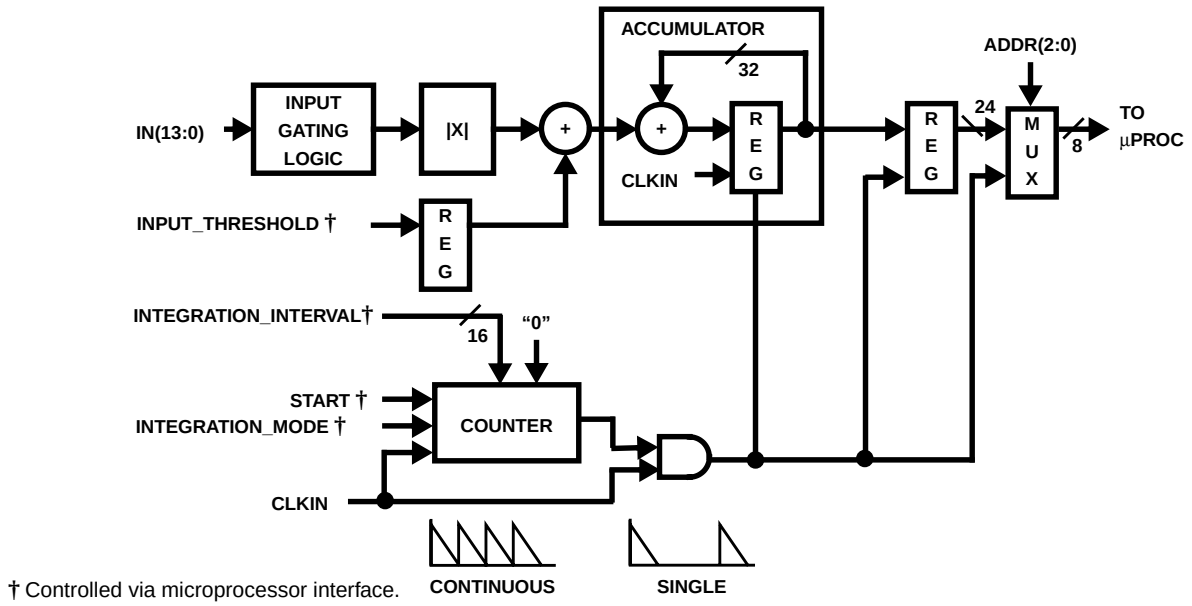


FIGURE 9.

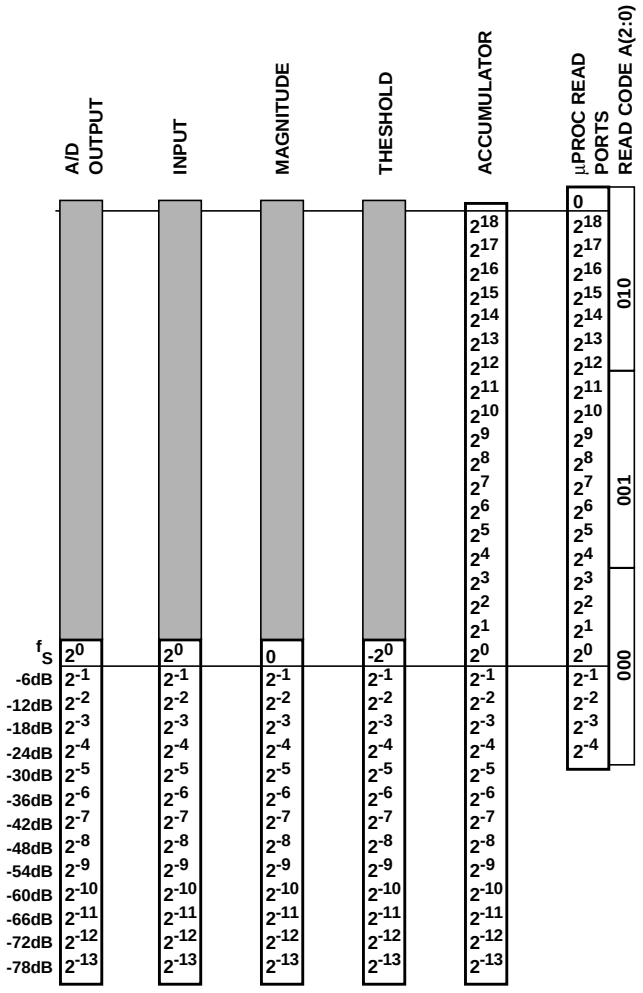


FIGURE 10. INPUT THRESHOLD DETECTOR BIT WEIGHTING

The integration period counter can be set up to run continuously or to count down and stop. Continuous integration counter operation lets the counter run, with sampling occurring every time the counter reaches zero. Because the processor samples the detector read port asynchronous to the CLKIN, data can be missed unless the status bit is monitored by the processor to ensure that a sample is taken for every integration count down sequence.

Additionally, in the HSP50214B, the ability to align the start/restart of the input level detector integration period with an external event is provided. This allows the sync signals, which are synchronized to external events, to be used to align all of the gain adjustments or measurements. If Control Word 27, Bit 17 is set to a logic one, the SYNCIN1 signal will cause the input level detector to start/restart its integration period. If Control Word 27, Bit 17 is set to a logic zero, control of the start/restart of the input level detector integration period does not respond to SYNCIN1.

In the count down and stop mode, the microprocessor read commands can be synchronized to system events, such as the start of a burst for a TDMA application. The integration counter can be started at any time by writing to Control Word 2. At the end of the integration period (counter = 0000), the upper 23 bits of the accumulator are transferred to a holding register for reading by the microprocessor. Note that it is not the restarting of the counter (by writing to Control Word 2) that latches the current value, but the end of the integration count. When the accumulator results are latched, a bit is set in the Status Register to notify the processor. Reading the most significant byte of the 23 bits clears the status bit. See the Microprocessor Read Section. Figure 11 illustrates a typical AGC detection process.

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Typically, the average input error is read from the Input Level Detector port for use in AGC Applications. By setting the threshold to 0, however, the average value of the input signal can be read directly. The calculation is:

$$dBFS_{RMS} = (20)\log[(1.111)(level)/((N)(16))] \quad \text{(EQ. 2)}$$

where "level" is the 24-bit value read from the 3 level Detector Registers and "N" is the number of samples to be integrated. Note that to get the RMS value of a sinusoid, multiply the average value of the rectified sinusoid by 1.111. For a full scale input sinusoid, this yields an RMS value of approximately $3dBf_S$.

NOTE: 1.111 scales the rectified sinusoid average ($2/\pi$) to $1/\sqrt{2}$

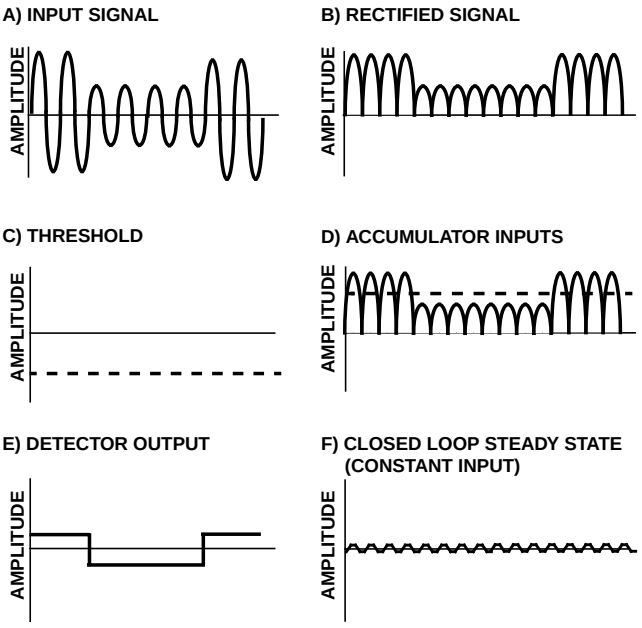


FIGURE 11. SIGNAL PROCESSING WITHIN LEVEL DETECTOR

In the HSP50214B, the polarity of the LSB's of the integration period pre-load is selectable. If Control Word 27, Bit 23 is set to a logic one, the two LSB's of the integration period preload are set to logic ones. This allows a power of two to be set for the integration period, for easy normalization in the processor. If Control Word 27, Bit 23 is set to a logic zero, then the two LSB's of the integration period preload are set to zeros as in the HSP50214.

Carrier Synthesizer/Mixer

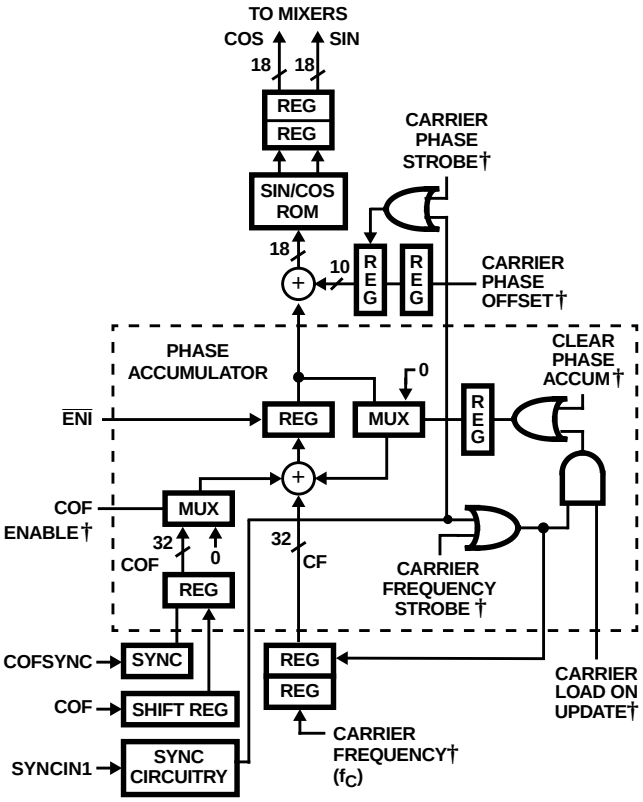
The Carrier Synthesizer/Mixer Section of the HSP50214B is shown in Figure 12. The NCO has a 32-bit phase accumulator, a 10-bit phase offset adder, and a sine/cosine ROM. The frequency of the NCO is the sum of a center frequency Control Word, loaded via the microprocessor interface (Control Word 3, Bits 0 to 31), and an offset frequency, loaded serially via the COF and COFSYNC pins. The offset frequency can be zeroed in Control Word 0, Bit 1. Both frequency control terms are 32 bits and the addition is modulo 2^{32}. The output frequency of the NCO is computed as:

$$f_C = f_S * N/(2^{32}), \quad \text{(EQ. 3)}$$

or in terms of the programmed value:

$$N = INT[f_C \times 2^{32}/f_S]_{HEX}, \quad \text{(EQ. 3A)}$$

where N is the 32-bit sum of the center and offset frequency terms, f_C is the frequency of the carrier NCO sinusoids, f_S is the input sampling frequency, and INT is the integer of the computation. See the Microprocessor Write Section on instructions for writing Control Word 3.



† Controlled via microprocessor interface.

FIGURE 12. BLOCK DIAGRAM OF NCO SECTION

For example, if N is 3267 (decimal), and f_S is 65MHz, then f_C is 49.44Hz. If received data is modulated at a carrier frequency of 10MHz, then the synthesizer/mixer should be programmed for N = 27627627 (hex) or D89D89D8 (hex).

Because the input enable, ENI, controls the operation of the phase accumulator, the NCO output frequency is computed relative to the input sample rate, f_S, not to f_{CLKIN}. The frequency control, N, is interpreted as two's complement because the output of the NCO is quadrature. Negative frequency L.O.s select the upper sideband; positive frequency L.O.s select the lower sideband. The range of the NCO is $-f_S/2$ to $+f_S/2$. The frequency resolution of the NCO is $f_S/(2^{32})$ or approximately 0.015Hz when CLKIN is 65 MSPS and ENI is tied low.

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The phase of the Carrier NCO can be shifted by adding a 10-bit phase offset to the MSB's (modulo 360^{o}) of the output of the phase accumulator. This phase offset control has a resolution of 0.35^{o} and can be interpreted as two's complement from -180^{o} to 180^{o} ($-\pi$ to π) or as binary from 0 to 360^{o} (0 to 2π). The phase offset is given by:

$$\phi_{OFF} = 2\pi \times (PO/2^{10}); (-(2^{9}) \le PO \le (2^{9}-1)) \quad (-512 \text{ to } 511) \qquad \text{(EQ. 4)}$$

or, in terms of the parameter to be programmed:

$$PO = INT[(2^{10}\phi_{OFF})/2\pi]_{HEX}; (-\pi < \phi_{OFF} < \pi) \qquad \text{(EQ. 4A)}$$

where PO is the 10-bit two's complement value loaded into the Phase Offset Register (Control Word 4, Bits 9-0). For example, a value of 32 (decimal) loaded into the Phase Offset Register would produce a phase offset of 11.25^{o} and a value of -512 would produce an offset of 180^{o}. The phase offset is loaded via the microprocessor interface. See the Microprocessor Write Section on instructions for writing Control Word 4.

The most significant 18 bits from the phase adder are used as the address a sin/cos lookup table. This lookup table maps phase into sinusoidal amplitude. The sine and cosine values have 18 bits of amplitude resolution. The spurious components in the sine/cosine generation are at least -102dBc. The sine and cosine samples are routed to the mixer section where they are multiplied with the input samples to translate the signal of interest to baseband.

The mixer multiplies the 14-bit input by the 18-bit quadrature sinusoids. The mixer equations are:

$$I_{OUT} = I_{IN} \times \cos(\omega_c) \qquad \text{(EQ. 5)}$$

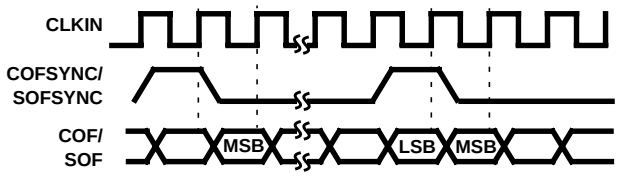
$$Q_{OUT} = I_{IN} \times \sin(\omega_c) \qquad \text{(EQ. 5A)}$$

The mixer output is rounded symmetrically to 15 bits.

To allow the frequency and phase of multiple parts to be updated synchronously, two sets of registers are used for latching the center frequency and phase offset words. The offset phase and center frequency Control Words are first loaded into holding registers. The contents of the holding registers are transferred to active registers in one of two ways. The first technique involves writing to a specific Control Word Address. A processor write to Control Word 5, transfers the center frequency value to the active register while a processor write to Control Word 6 transfers the phase offset value to the active register.

The second technique, designed for synchronizing updates to multiple parts, uses the SYNCIN1 pin to update the active registers. When Control Word 1, Bit 20 is set to 1, the SYNCIN1 pin causes both the center frequency and Phase Offset Holding Registers to be transferred to active registers. Additionally, when Control Word 0, Bit 0 is set to 1, the feedback in the phase accumulator is zeroed when the transfer from the holding to active register occurs. This feature provides synchronization of the phase accumulator starting phase of multiple parts. It can also be used to reset the phase of the NCO synchronous with a specific event.

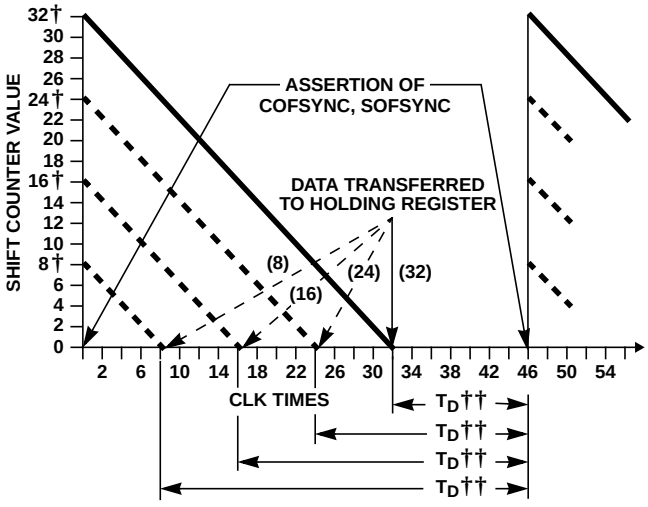
The carrier offset frequency is loaded using the COF and COFSYNC pins. Figure 13 details the timing relationship between COF, COFSYNC and CLKIN. The offset frequency word can be zeroed if it is not needed. Similarly, the Sample Offset Frequency Register controlling the Re-Sampler NCO is loaded via the SOF and SOFSYNC pins. The procedure for loading data through the two pin NCO interfaces is identical except that the timing of SOF and SOFSYNC is relative to PROCCLK.



OTE: Data must be loaded MSB first.

IGURE 13. SERIAL INPUT TIMING FOR COF AND SOF INPUTS

Each serial word has a programmable word width of either 8, 16, 24, or 32 bits (See Control Word 0, Bits 4 and 5, for the Carrier NCO programming and Control Word 11, Bits 3 and 4, for Timing NCO programming). On the rising edge of the clock, data on COF or SOF is clocked into an input shift register. The beginning of a serial word is designated by asserting either COFSYNC or SOFSYNC "high" one CLK period prior to the first data bit.



†Serial word width can be: 8, 16, 24, 32 bits wide.

†T_D is determined by the COFSYNC, COFSYNC rate.

FIGURE 14. HOLDING REGISTERS LOAD SEQUENCE FOR COF AND SOF SERIAL OFFSET FREQUENCY DATA

NOTE: Serial Data must be loaded MSB first, and COFSYNC or SOFSYNC should not be asserted for more than one CLK cycle.

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NOTE: COF loading and timing is relative to CLKIN while SOF loading and timing is relative to PROCCLK.

NOTE: T_D can be 0, and the fastest rate is with 8-bit word width.

The assertion of the COFSYNC (or SOFSYNC) starts a count down from the programmed word width. On following CLKs, data is shifted into the register until the specified number of bits have been input. At this point the contents of the register are transferred from the Shift Register to the respective 32-bit Holding Register. The Shift Register can accept new data on the following CLK. If the serial input word is defined to be less than 32 bits, it will be transferred to the MSBs of the 32-bit Holding Register and the LSBs of the Holding Register will be zeroed. See Figure 14 for details.

CIC Decimation Filter

The mixer output may be filtered with the CIC filter or it may be routed directly to the halfband filters. The CIC filter is used to reduce the sample rate of a wideband signal to a rate that the halfbands and programmable filters can process, given the maximum computation speed of PROCCLK. (See Halfband and FIR Filter Sections for techniques to calculate this value).

Prior to the CIC filter, the output of the mixer goes through a barrel shifter. The shifter is used to adjust the gain in 6dB steps to compensate for the variation in CIC filter gain with decimation. (See Equation 6). Fine gain adjustments must be done in the AGC Section. The shifter is controlled by the sum of a 4-bit CIC Shift Gain word from the microprocessor and a 3-bit gain word from the GAINADJ(2:0) pins. The three bit value is pipelined to match the delay of the input samples. The sum of the 3 and 4-bit shift gain words saturates at a value of 15. Table 1 details the permissible values for the GAINADJ(2:0) barrel shifter control, while Figure 15 shows the permissible CIC Shift Gain values.

The CIC filter structure for the HSP50214B is fifth order; that is it has five integrator/comb pairs. A fifth order CIC has 84dB of alias attenuation for output frequencies below 1/8 the CIC output sample rate.

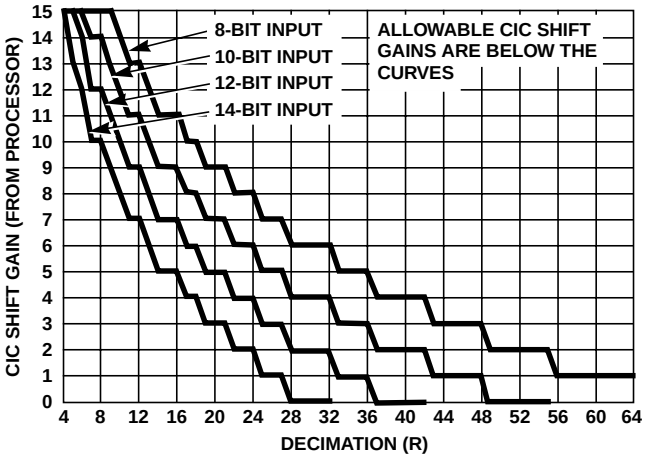


FIGURE 15. CIC SHIFT GAIN VALUES

The decimation factor of the CIC filter is programmed in Control Word 0, Bits 12 - 7. The CIC Shift Gain is programmed in Control Word 0, Bits 16-13. The CIC Bypass is set in Control Word 0, Bit 6. When bypassing the CIC filter, the $\overline{ENI}$ signal must be de-asserted between samples, i.e., the CLKIN rate must be $\geq 2 \bullet f_S$.

TABLE 3. GAIN ADJUST CONTROL AND CIC DECIMATION

ΔGAIN VALUE (dB)	GAIN ADJ(2:0)	MAX. CIC DECIMATION
0	000	32
6	001	27
12	010	24
18	011	21
24	100	18
30	101	16
36	110	12
42	111	10

CIC Gain Calculations

The gain through the CIC filter increases with increased decimation. The programmable barrel shifter that precedes the first integrator in the CIC is used to offset this variation. Gain variations due to decimation should be offset using the 4-bit CIC Shift Gain word. This allows the input signal level to be adjusted in 6dB steps to control the CIC output level.

The gain at each stage of the CIC is:

$$k = R^N, \quad \text{(EQ. 6)}$$

where R is the decimation factor and N is the number of stages. The input to the CIC from the mixer is 15 bits, and the bit widths of the accumulators for the five stages in the HSP50214B are 40, 36, 32, 32, and 32, as shown in Figure 16. This limits the maximum decimation in the CIC to 32 for a full scale input.

If R is 32, the gain through all five integrator stages is $32^5 = 2^{25}$. (The gain through the last four CIC stages is 2^{20}, through the last 3 it is 2^{15}, etc.). The sum of the input bits and the growth bits cannot exceed the accumulator size. This means that for a decimation of 32 and 15 input bits, the first accumulator must be 15 + 25 = 40 bits.

Thus, the value of the CIC Shift Gain word can be calculated:

$$\begin{aligned} SG &= \text{FLOOR}\,[39 - (IIN) - \log_2(R)^5 && \text{for } 4<R<32 \\ &= 15 && \text{for } R = 4 \end{aligned} \quad \text{(EQ. 7)}$$

NOTE: The number of input bits is IIN. (If the number of bits into the CIC filter is used, the value 40 replaces 39).

For 14 bits, Equation 7 becomes:

$$\begin{aligned} SG &= \text{FLOOR}[25 - \log_2(R)^5] && \text{for } 4 < R < 32 \\ &= 15 && \text{for } R = 4 \end{aligned} \quad \text{(EQ. 8A)}$$

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For 12 bits, Equation 7 becomes:

$$SG = FLOOR[27 - \log_2(R)^5] \text{ for } 5 < R < 40$$
$$= 15 \text{ for } 4 \le R \le 5 \quad \text{(EQ. 8B)}$$

For 10 bits, Equation 7 becomes:

$$SG = FLOOR[29 - \log_2(R)^5] \text{ for } 6 < R < 52$$
$$= 15 \text{ for } 4 \le R \le 6 \quad \text{(EQ. 8C)}$$

For 8 bits, Equation 7 becomes:

$$SG = FLOOR[31 - \log_2(R)^5] \text{ for } 9 < R < 64$$
$$= 15 \text{ for } 4 \le R \le 9 \quad \text{(EQ. 8D)}$$

Figure 15 is a plot of Equations 8A through 8D. The 4-bit CIC Shift Gain word has a range from 0 to 15. The 6-bit Decimation Factor counter preload field, (R-1), has a range from 0 to 63, limited by the input resolution as cited above.

Using the Input Gain Adjust Control Signals

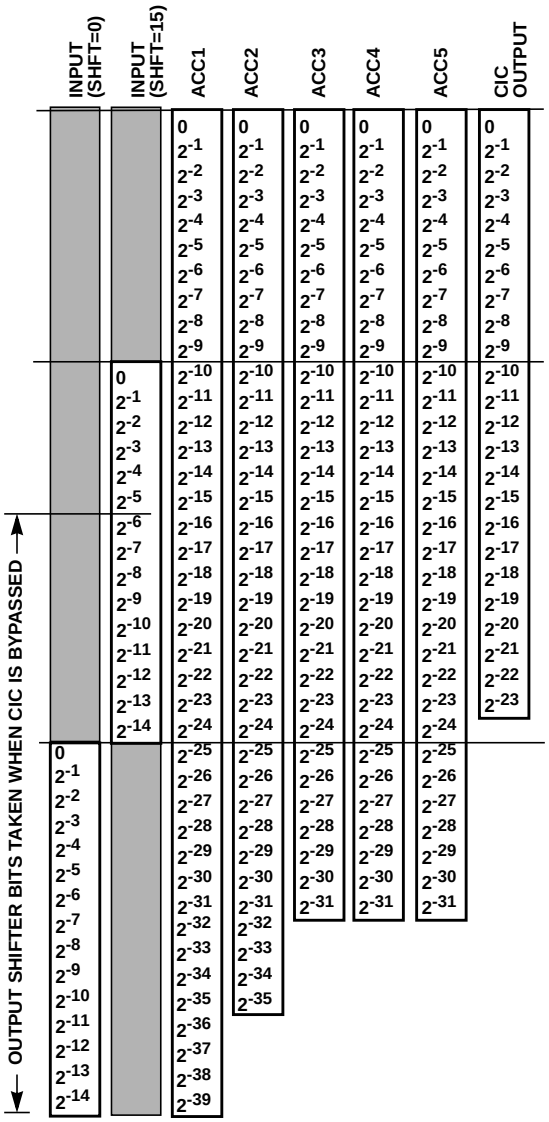
The input gain offset control GAINADJ(2:0)) is provided to offset the signal gain through the part, i.e., to keep the CIC filter output level constant as the analog front end attenuation is changed. The gain adjust offset is 6dB per code, so the gain adjust range is 0 to 42dB. For example, if 12dB of attenuation is switched in at the receiver RF front end, a code of 2 would increase the gain at the input to the CIC filter up 12dB so that the CIC filter output would not drop by 12dB. This fixed gain adjust eliminates the need for the software to continually normalize.

One must exercise care when using this function as it can cause overflow in the CIC filter. Each gain adjust in the shifter from the gain adjust control signals is the equivalent of an extra bit of input. The maximum decimation in the CIC is reduced accordingly. With a decimation of 32, all 40 bits of the CIC are needed, so no input offset gain is allowed. As the decimation is reduced, the allowable offset gain increases. Table 3 shows the decimation range versus desired offset gain range. Table 3 assumes that the CIC Shift Gain has been programmed per Equation 7 or 8A.

The CIC filter decimation counter can be loaded synchronous with other PDC chips, using the SYNCIN1 signal and the CIC External Sync Enable bit. The CIC external Sync Enable is set via Control Word 0, Bit 19.

Halfband Decimating Filters

The Programmable Down Converter has five halfband filter stages, as shown in Figure 17. Each stage decimates by 2 and filters out half of the available bandwidth. The first halfband, or HB1, has 7 taps. The remaining halfbands; HB2, HB3, HB4, and HB5; have 11, 15, 19, and 23 taps respectively. The coefficients for these halfbands are given in Table 4. Figure 18 shows the frequency response of each of the halfband filters with respect to normalized frequency, F_N. Frequency normalization is with respect to the input sampling frequency of each filter section. Each stage is activated by their respective bit location (15-20) in Control Word 7. Any combination of halfband filters may be used, or all may be bypassed.



***NOTE:** If 14 input bits are not needed, the gain adjust can be increased by one for each bit that the input is shifted down at the input. For example, if only 12 bits are needed, an offset range of 24dB is possible for a decimation of 24.*

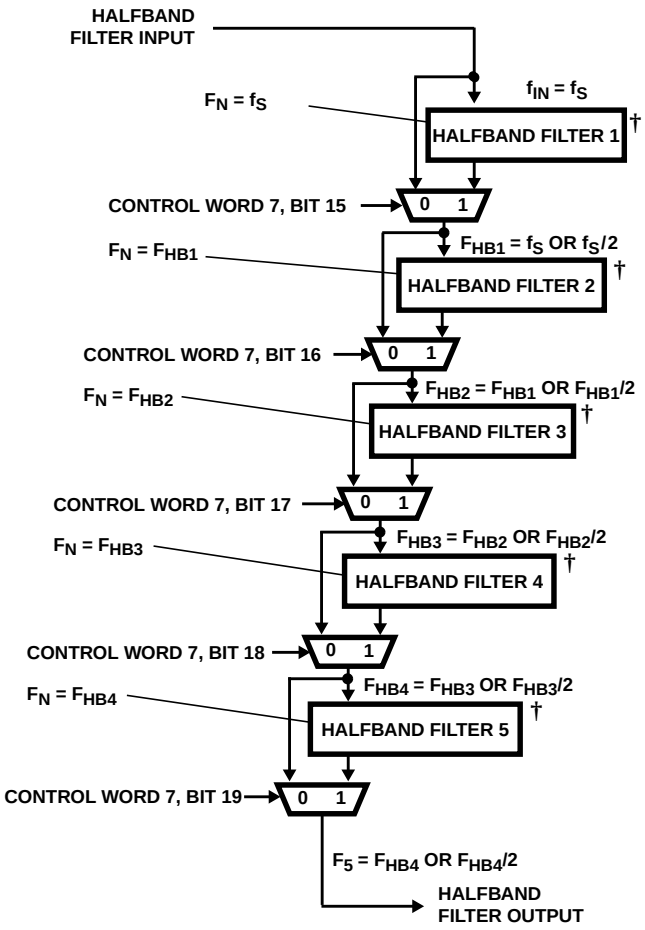
FIGURE 16. CIC FILTER BIT WEIGHTING

Since each halfband filter section decimates by 2, the total decimation through the halfband filter is given by:

$$DEC_{HB} = 2^N \quad \text{(EQ. 9)}$$

where N = Number of Halfband Filters Selected (1 - 5).

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† Each halfband section decimates by 2.

FIGURE 17. BLOCK DIAGRAM OF HALFBAND FILTER SECTION

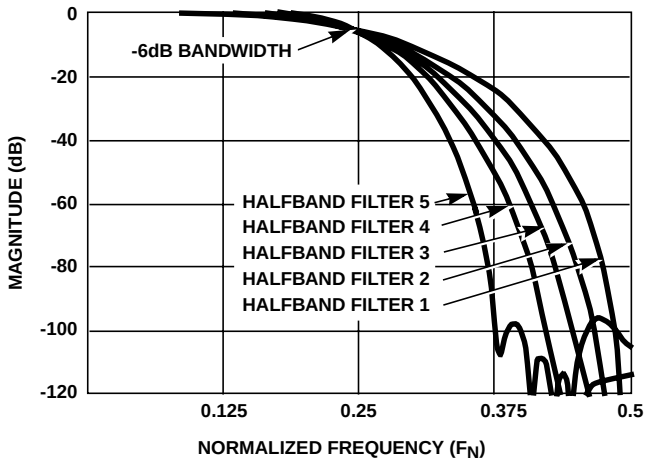


FIGURE 18. HALFBAND FILTER FREQUENCY RESPONSE

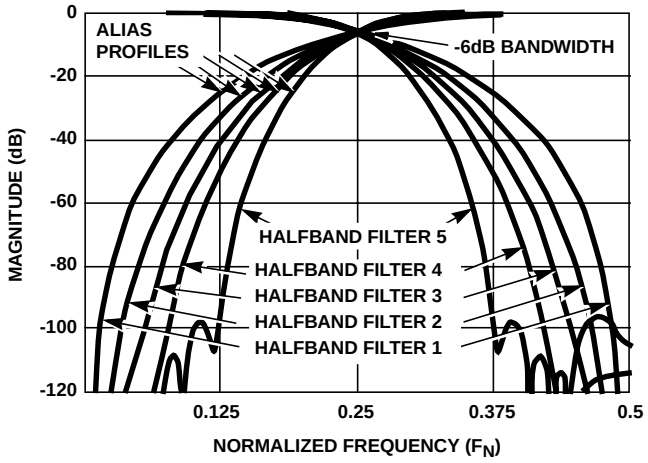


FIGURE 19. HALFBAND FILTER ALIAS CONSIDERATIONS

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TABLE 4. HALFBAND FILTER COEFFICIENTS

COEFFICIENTS	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C0	- 0.031303406	0.005929947	-0.00130558	0.000378609	-0.000347137
C1	0.000000000	0.000000000	0.000000000	0.000000000	0.000000000
C2	0.281280518	-0.049036026	0.012379646	-0.003810883	0.00251317
C3	0.499954224	0.000000000	0.000000000	0.000000000	0.000000000
C4	0.281280518	0.29309082	-0.06055069	0.019245148	-0.010158539
C5	0.000000000	0.499969482	0.000000000	0.000000000	0.000000000
C6	- 0.031303406	0.29309082	0.299453735	-0.069904327	0.03055191
C7		0.000000000	0.499954224	0.000000000	0.000000000
C8		-0.049036026	0.299453735	0.304092407	-0.081981659
C9		0.000000000	0.000000000	0.500000000	0.000000000
C10		0.005929947	-0.06055069	0.304092407	0.309417725
C11			0.000000000	0.000000000	0.500000000
C12			0.012379646	-0.069904327	0.309417725
C13			0.000000000	0.000000000	0.000000000
C14			-0.00130558	0.019245148	-0.081981659
C15				0.000000000	0.000000000
C16				-0.003810883	0.03055191
C17				0.000000000	0.000000000
C18				0.000378609	-0.010158539
C19					0.000000000
C20					0.00251317
C21					0.000000000
C22					-0.000347137

NOTE: While Halfband filters are typically selected starting with the last stage in the filter chain to give the maximum alias free bandwidth, a higher throughput rate may be obtained using other filter combinations. See Application Note 9720, "Calculating Maximum Processing Rates of the PDC".

Depending on the number of halfbands used, PROCCLK must operate at a minimum rate above the input sample rate, f_S, to the halfband. This relationship depends on the number of multiplies for each of the halfband filter stages. The filter calculations take 3, 4, 5, 6, and 7 multiplies per input for HB1, HB2, HB3, HB4, and HB5 respectively. If we keep the assumption that f_S is the input sampling frequency, then Equation 10 shows the minimum ratio needed.

$$f_{PROCCLK}/f_S \geq ([(7)(HB5)(2^{HB5})+ (6)(HB4)(2^{(HB4 + HB5)})+ (5)(HB3)(2^{(HB3+HB4+HB5)})+ (4)(HB2)(2^{(HB2+HB3+ HB4+HB5)})+ (3)(HB1)(2^{(HB1+HB2+HB3+HB4+HB5)})]/2^T \quad \text{(EQ. 10)}$$

where

HB1 = 1 if this section is selected and 0 if it is bypassed;
HB2 = 1 if this section is selected and 0 if it is bypassed;
HB3 = 1 if this section is selected and 0 if it is bypassed;
HB4 = 1 if this section is selected and 0 if it is bypassed;
HB5 = 1 if this section is selected and 0 if it is bypassed;
T = number of Halfband Filters Selected. The range for T is from 0 to 5.

Examples of PROCCLK Rate Calculations

Suppose we enable HB1, HB3, and HB5. Using Figure 16, HB1= 1, HB3 = 1, and HB5 = 1. Since stage 2 and stage 4 are not used, HB2 and HB4 = 0. PROCCLK must operate faster than (7x2+5x4+3x8)/8 = 7.25 times faster than f_S.

If all five halfbands are used, then PROCCLK must operate at (7x2+6x4+5x8+4x16+3x32)/32 = 7.4375 times faster than f_S.

255-Tap Programmable FIR Filter

The Programmable FIR filter can be used to implement real filters with even or odd symmetry, using up to 255 filter taps, or complex filters with up to 64 taps. The FIR filter takes advantage of symmetry in coefficients by summing data samples that share a common coefficient, prior to multiplication. In this manner, two filter taps are calculated per multiply accumulate cycle. Asymmetric filters cannot share common coefficients, so only one tap per multiply accumulate cycle is calculated. The filter can be effectively bypassed by setting the coefficient $C_0 = 1$ and all other coefficients, $C_N = 0$.

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Additionally, the Programmable FIR filter provides for decimation factors, R, from 1 to 16. The processing rate of the Filter Compute Engine is PROCCLK. As a result, the frequency of PROCCLK must exceed a minimum value to ensure that a filter calculation is complete before the result is required for output. In configurations which do not use decimation, one input sample period is available for filter calculation before an output is required. For configurations which employ decimation, up to 16 input sample periods may be available for filter calculation.

For real filter configurations, use Equation 11 to calculate the number of taps available at a given input filter sample rate.

$$TAPS = (floor[PROCCLK/(F_{SAMP}/R) - R])(1 + SYM) - [(SYM)(ODD\#)] \quad \text{(EQ. 11A)}$$

for real filters, and

$$TAPS = floor[(PROCCLK/(F_{SAMP}/R) - R)/2] \quad \text{(EQ. 11B)}$$

for complex filters, where floor is defined as the integer portion of a number; PROCCLK is the compute clock; f_{SAMP} = the FIR input sample rate; R = Decimation Factor; SYM = 1 for symmetrical filter, 0 for asymmetrical filter; ODD# = 1 for an odd number of filter taps, 0 = an even number of taps.

Use Equation 12 to calculate the maximum input rate.

$$F_{SAMP} = (PROCCLK)(R)/[R + [floor[(Taps) + (SYM)(ODD\#)]/(1 + SYM)]] \quad \text{(EQ. 12A)}$$

for real filters, and

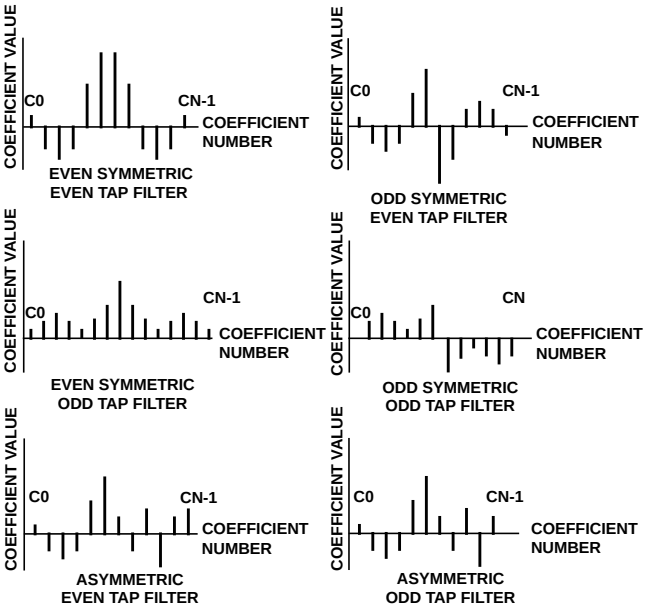
$$F_{SAMP} = [(PROCCLK)(R)]/[R + floor[(Taps)(2)]] \quad \text{(EQ. 12B)}$$

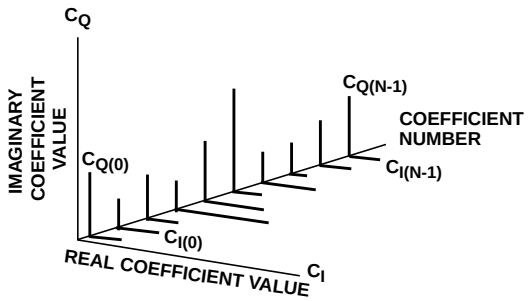
for complex filters, where floor[x], PROCCLK, f_{SAMP}, R = Decimation Factor, SYM, and ODD# are defined as in Equation 11.

Use Equation 13 to calculate the maximum output sample rate for both real and complex filters.

$$F_{FIR\,OUT} = (F_{SAMP})/R \quad \text{(EQ. 13)}$$

The coefficients are 22 bits and are loaded using writes to Control Words 128 through 255 (see Microprocessor Write Section). For real filters, the same coefficients are used by I and Q paths. If the filter is configured as a symmetric filter using Control Word 17, Bit 9, then coefficients are loaded starting with the center coefficient in Control Word 128 and proceeding to last coefficient in Control Word 128+n. The filter symmetry type can be set to even or odd symmetric, and the number of filter coefficients can be even or odd, as illustrated in Figure 20. Note that complex filters can also be realized but are only allowed to be asymmetric. Only the coefficients that are used need to be loaded.





Definitions:

Even Symmetric: h(n) = h(N-n-1) for n = 0 to N-1

Odd Symmetric: h(n) = -h(N-n-1) for n = 0 to N-1

Asymmetric: A filter with no coefficient symmetry.

Even Tap filter: A filter where N is an even number.

Odd Tap filter: A filter where N is an odd number.

Real Filter: A filter implemented with real coefficients.

Complex Filters: A filter with quadrature coefficients.

FIGURE 20. DEMONSTRATION OF DIFFERENT TYPES OF DIGITAL FIR FILTERS CONFIGURED IN THE PROGRAMMABLE DOWNCONVERTER

Automatic Gain Control (AGC)

The AGC Section provides gain to small signals, after the large signals and out-of-band noise have been filtered out, to ensure that small signals have sufficient bit resolution in the Resampling/Interpolating Halfband filters and the Output Formatter. The AGC can also be used to manually set the gain. The AGC optimizes the bit resolution for a variety of input amplitude signal levels. The AGC loop automatically adds gain to bring small signals from the lower bits of the 26-bit programmable FIR filter output into the 16-bit range of the

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output section. Without gain control, a signal at -72dBFS = $20\log_{10}(2^{-12})$ at the input would have only 4 bits of resolution at the output (12 bits less than the full scale 16 bits). The potential increase in the bit resolution due to processing gain of the filters can be lost without the use of the AGC.

Figure 23 shows the Block Diagram for the AGC Section. The FIR filter data output is routed to the Resampling and Halfband filters after passing through the AGC multipliers and Shift Registers. The outputs of the Interpolating Halfband filters are routed to the Cartesian to Polar coordinate converter. The magnitude output of the coordinate converter is routed through the AGC error detector, the AGC error scaler and into the AGC loop filter. This filtered error term is used to drive the AGC multiplier and shifters, completing the AGC control loop.

The AGC Multiplier/Shifter portion of the AGC is identified in Figure 23. The gain control from the AGC loop filter is sampled when new data enters the Multiplier/Shifter. The limit detector detects overflow in the shifter or the multiplier and saturates the output of I and Q data paths independently. The shifter has a gain from 0 to 90.31dB in 6.021dB steps, where 90.31dB = $20\log_{10}(2^N)$, when N = 15. The mantissa provides an additional 6dB of gain in 0.0338dB steps where 6.0204dB = $20\log_{10}[1+(X)2^{-15}]$, where $X = 2^{15}-1$. Thus, the AGC multiplier/shifter transfer function is expressed as:

$$\text{AGC Mult/Shift Gain} = 2^N[1+(X)2^{-15}], \quad \text{(EQ. 14)}$$

where N, the shifter exponent, has a range of $0<N<15$ and X, the mantissa, has a range of $0<X<(2^{15}-1)$.

Equation 14 can be expressed in dB,

$$(\text{AGC Mult/Shift Gain})\text{dB} = 20\log_{10}(2^N[1+(X)2^{-15}]) \quad \text{(EQ. 14A)}$$

The full AGC range of the Multiplier/Shifter is from 0 to 96.331dB ($20\log_{10}[1+(2^{15}-1)2^{-15}] + 20\log_{10}[2^{15}] = 96.331$). Figure 21 illustrates the transfer function of the AGC multiplier versus mantissa control for N = 0. Figure 22 illustrates the complete AGC Multiplier/Shifter Transfer function for all values of exponent and mantissa control.

The resolution of the mantissa was increased to 16 bits in the A Version, to provide a theoretical AM modulation level of -96dBc (depending on loop gain, settling mode and SNR). This effectively eliminates AM spurious caused by the AGC resolution.

For fixed gains, either set the upper and lower AGC limits to the same value, or set the limits to minimum and maximum gains and set the AGC loop gain to zero.

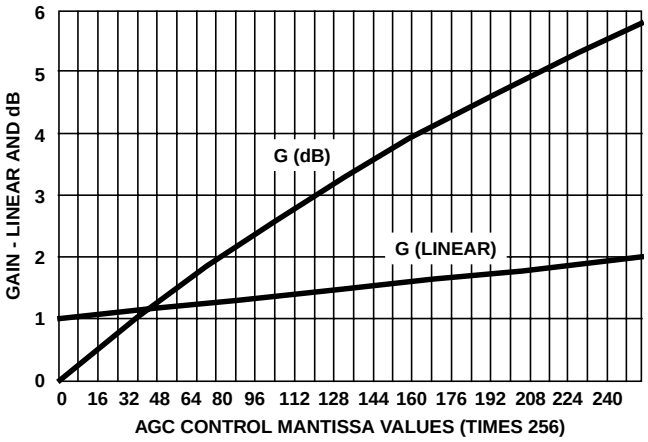


FIGURE 21. AGC MULTIPLIER LINEAR AND dB TRANSFER FUNCTION

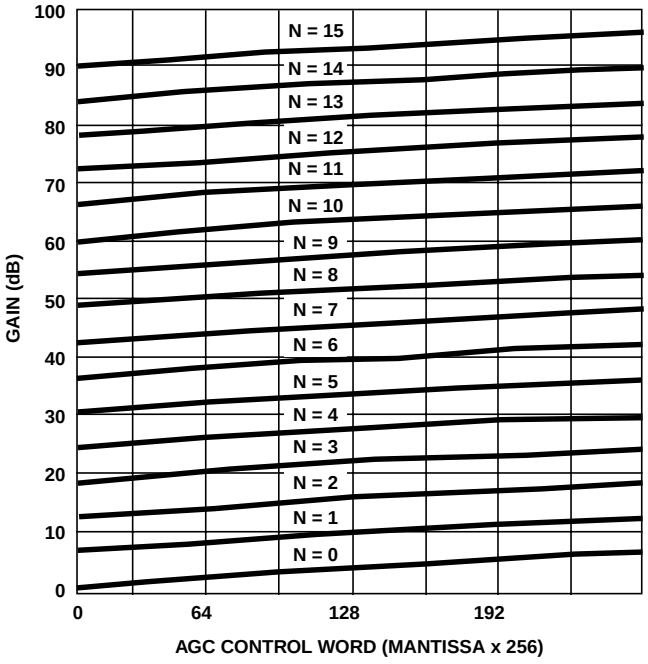


FIGURE 22. AGC GAIN CONTROL TRANSFER FUNCTION

The Cartesian to Polar Coordinate converter accepts I and Q data and generates magnitude and phase data. The magnitude output is determined by the equation:

$$|r| = 1.64676\sqrt{I^2+Q^2}. \quad \text{(EQ. 15)}$$

where the magnitude limits are determined by the maximum I and Q signal levels into the Cartesian to Polar converter. Taking fractional 2's complement representation, magnitude ranges from 0 to 2.329, where the maximum output is

$$|r| = 1.64676\sqrt{(1.0)^2+(1.0)^2} = 1.64676\times 1.414 = 2.329.$$

The AGC loop feedback path consists of an error detector, error scaling, and an AGC loop filter. The error detector subtracts the magnitude output of the coordinate converter from the programmable AGC THRESHOLD value. The bit weighting of

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the AGC THRESHOLD value (Control Word 8, Bits 16-28) is shown in Table 5. Note that the MSB is always zero. The range of the AGC THRESHOLD value is 0 to +3.9995. The AGC Error Detector output has the identical range.

TABLE 5. AGC THRESHOLD (CONTROL WORD 8) BIT WEIGHTING

28	27	26	25	24	23	22	21	20	19	18	17	16
2^2	2^1	2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

The loop gain is set in the AGC Error Scaling circuitry, using the two programmable mantissas and exponents. The mantissa, M, is a 4-bit value which weights the loop filter input from 0.0 to 0.9375. The exponent, E, defines a shift factor that provides additional weighting from 2^0 to 2^{-15}. Together the mantissa and exponent define the loop gain as given by,

$$\text{AGC Loop Gain} = M_{LG}2^{-4}\ 2^{-(15-E_{LG})} \quad \text{(EQ. 16)}$$

where M_{LG} is a 4-bit binary value ranging from 0 to 15, and E_{LG} is a 4-bit binary value ranging from 0 to 15. Table 7 and 8 detail the binary values and the resulting scaling effects of the AGC scaling mantissa and exponent. The composite (shifter and multiplier) AGC scaling Gain range is from 0.0000 to $2.329(0.9375)2^0 = 0.0000$ to 2.18344. The scaled gain error can range (depending on threshold) from 0 to 2.18344, which maps to a “gain change per sample” range of 0 to 3.275dB/sample.

The AGC Gain mantissa and exponent values are programmed into Control Word 8, Bits 0-15. The PDC provides for the storing of two values of AGC Scaling Gain (both exponent and mantissa). This allows for quick adjustment of the loop gain by simply asserting the external control line AGCGNSEL. When AGCGNSEL = 0, then AGC GAIN 0 is selected, and when AGCGNSEL = 1, AGC Loop Gain 1 is selected. Possible applications include acquisition/tracking, no burst present/burst present, strong signal/weak signal, track/hold, or fast/slow AGC values.

The AGC loop filter consists of an accumulator with a built in limiting function. The maximum and minimum AGC gain limits are provided to keep the gain within a specified range and are programed by 12-bit Control Words using the following the equation:

$$\text{AGC Gain Limit} = (1 + m_{AGC}2^{-9})2^e \quad \text{(EQ. 17)}$$

$$(\text{AGC Gain Limit})\text{dB} = (6.02)(\text{eeee}) + 20\log(1.0 + 0.\text{mmmmmmmm}) \quad \text{(EQ. 17A)}$$

where m is an 8-bit mantissa value between 0 and 255, and e is the 4-bit exponent ranging from 0 to 15. Control Word 9, Bits 16-27 are used for programming the upper limit, while bits 0-11 are used to program the lower threshold. The ranges and format for these limit values are shown in Tables 6A - C. The bit weightings for the AGC Loop Feedback elements are detailed in Table 9.

TABLE 6A. AGC LIMIT EXPONENT vs GAIN

GAIN(dB)	EXPONENT	MANTISSA
96.332	15	255
90.309	15	0
84.288	14	0
78.268	13	0
72.247	12	0
66.227	11	0
60.206	10	0
54.185	9	0
48.165	8	0
42.144	7	0
36.124	6	0
30.103	5	0
24.082	4	0
18.062	3	0
12.041	2	0
6.021	1	0
0.000	0	0

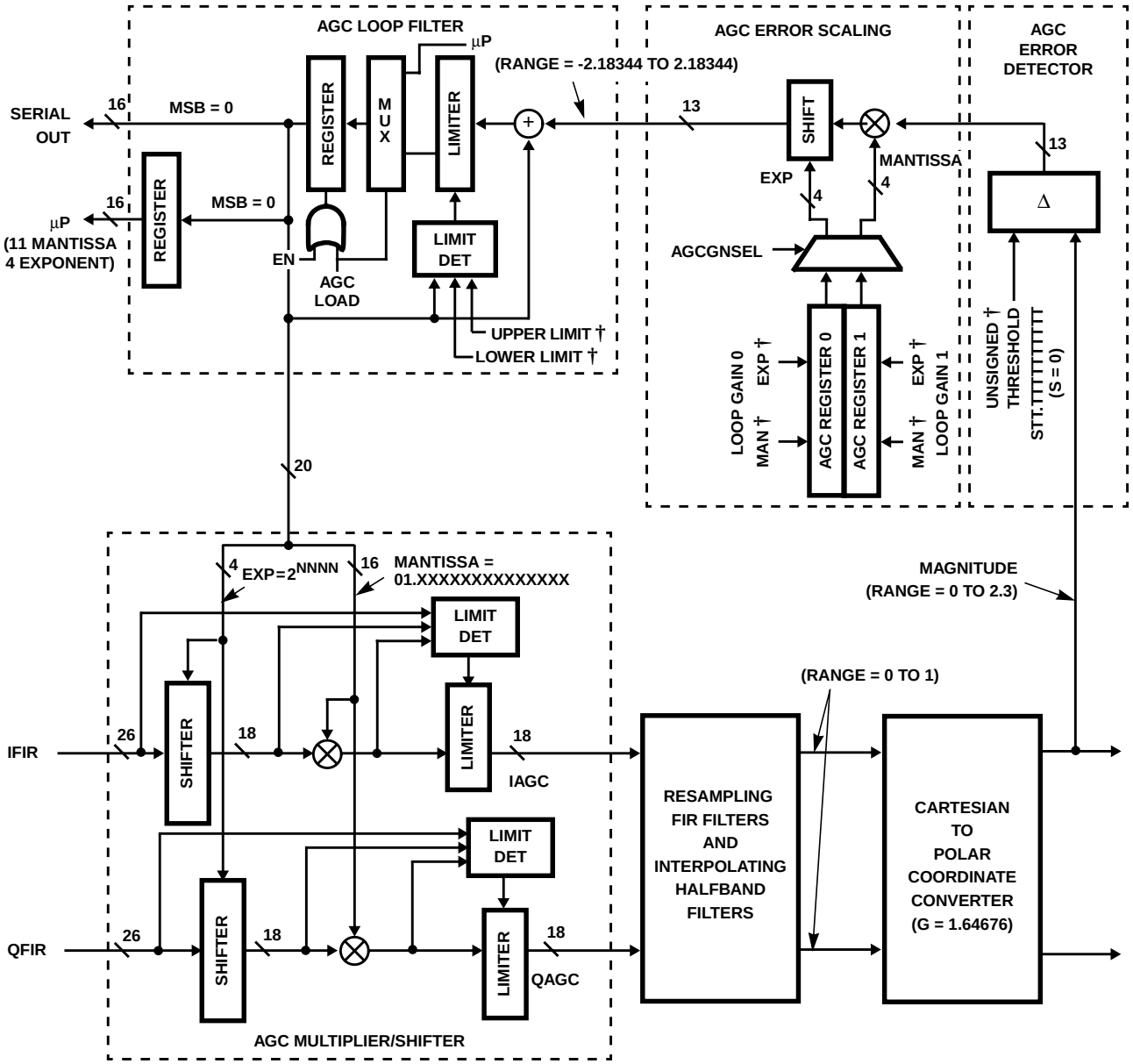
TABLE 6B. AGC LIMIT MANTISSA vs GAIN

GAIN(dB)	EXPONENT	MANTISSA
6.000	0	255
5.750	0	240
5.500	0	226
5.250	0	212
5.000	0	199
4.750	0	185
4.500	0	173
4.250	0	161
4.000	0	149
3.750	0	138
3.500	0	127
3.250	0	116
3.000	0	105
2.750	0	95
2.500	0	85
2.250	0	75
2.000	0	66
1.750	0	57
1.500	0	48
1.250	0	39
1.000	0	31
0.750	0	23
0.500	0	15
0.250	0	7
0.020	0	1

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TABLE 6C. AGC LIMIT DATA FORMAT

CONTROL WORD 9 BIT:	27	26	25	24	23	22	21	20	19	18	17	16
FORMAT	e	e	e	e	m	m	m	m	m	m	m	m



† Controlled via microprocessor interface.

FIGURE 23. AGC BLOCK DIAGRAM

Using AGC loop gain, the AGC range, and expected error detector output, the gain adjustments per output sample for the Loop Filter Section of the Digital AGC can be given by

$$\text{AGC Slew Rate} = 1.5\text{dB}(\text{THRESH} - (\text{MAG}*1.64676)) \times (M_{LG})(2^{-4})\left(2^{-(15-E_{LG})}\right) \quad \text{(EQ. 18)}$$

The loop gain determines the growth rate of the sum in the loop accumulator which, in turn, determines how quickly the AGC gain traces the transfer function given in Figures 21 and 22. Since the log of the gain response is roughly linear, the loop response can be approximated by multiplying the maximum AGC gain error by the loop gain. The expected

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range for the AGC rate is ~ 0.000106 to 3.275dB/output sample time for a threshold of 1/2 scale. See the notes at the bottom of Table 9 for calculation of the AGC response times. The maximum AGC Response is given by:

$$\text{AGC Response}_{Max} = \text{Input(Cart/Polar Gain)(Error Det Gain)(AGC Loop Gain)(AGC Output Weighting)} \quad \text{(EQ. 19)}$$

Since the AGC error is scaled to adjust the gain, the loop settles asymptotically to its final value. The loop settles to the mean of the signal.

TABLE 7. AGC LOOP GAIN BINARY MANTISSA TO GAIN SCALE FACTOR MAPPING

BINARY CODE (MMMM)	SCALE FACTOR	BINARY CODE (MMMM)	SCALE FACTOR
0000	0.0000	1000	0.5000
0001	0.0625	1001	0.5625
0010	0.1250	1010	0.6250
0011	0.1875	1011	0.6875
0100	0.2500	1100	0.7500
0101	0.3125	1101	0.8125
0110	0.3750	1110	0.8750
0111	0.4375	1111	0.9375

TABLE 8. AGC LOOP GAIN BINARY EXPONENT TO GAIN SCALE FACTOR MAPPING

BINARY CODE (EEEE)	SCALE FACTOR	BINARY CODE (EEEE)	SCALE FACTOR
0000	2^{15}	1000	2^{7}
0001	2^{14}	1001	2^{6}
0010	2^{13}	1010	2^{5}
0011	2^{12}	1011	2^{4}
0100	2^{11}	1100	2^{3}
0101	2^{10-}	1101	2^{2}
0110	2^{9}	1110	2^{1}
0111	2^{8}	1111	2^{0}

For example, if M_{LG} = 0101 and E_{LG} = 1100, the AGC Loop Gain = $0.3125*2^{-7}$. The loop gain mantissas and exponents are set in the AGC Loop Parameter Control Register (Control Word 8, Bits 0-15).

Two AGC loop gains are provided in the Programmable Down Converter, for quick adjustment of the AGC loop. The AGC Gain select is a control input to the device, selecting Gain 0 when AGCGNSEL = 0, and selecting Gain 1 when AGCGNSEL = 1.

In the HSP50214, a reset event (caused by SYNCIN2 or CW25) would clear the AGC loop filter accumulator. In the HSP50214B, if Control Word 27, Bit 15 is set to zero, the AGC loop filter accumulator will clear as in the original HSP50214. If Control Word 27, Bit 15 is set to a one, the backend reset (from CW25) will not clear the AGC loop filter accumulator.

In the HSP50214, the settling mode of the AGC forces the mean of the signal magnitude error to zero. The gain error is scaled and used to adjust the gain up or down. This proportional scaling mode causes the AGC to settle to the final gain value asymptotically. This AGC settling mode is preferred in many applications because the loop gain adjustments get smaller and smaller as the loop settles, reducing any AM distortion caused by the AGC.

With this AGC settling mode, the proportional gain error causes the loop to settle more slowly if the threshold is small. This is because the maximum value of the threshold minus the magnitude is smaller. Also, the settling can be asymmetric, where the loop may settle faster for “over range” signals than for “under range” signals (or vice versa).

In some applications, such as burst signals or TDMA signals, a very fast settling time and/or a more predictable settling time is desired. The AGC may be turned off or slowed down after an initial AGC settling period.

To minimize the settling time, a median AGC settling mode has been added to the HSP50214B. This mode uses a fixed gain adjustment with only the direction of the adjustment controlled by the gain error. This makes the settling time independent of the signal level.

For example, if the loop is set to adjust 0.5dB per output sample, the loop gain can slew up or down by 16dB in 16 symbol times, assuming a 2 samples per symbol output sample rate. This is called a median settling mode because the loop settles to where there is an equal number of magnitude samples above and below the threshold. The disadvantage of this mode is that the loop will have a wander (dither) equal to the programmed step size. For this reason, it is advisable to set one loop gain for fast settling at the beginning of the burst and the second loop gain for small adjustments during tracking.

The median settling mode is enabled by setting Control Word 27, Bit 16 to a logic one. If Control Word 27, Bit 16 is zero, the mean loop settling mode is selected and the loop works identically to the HSP50214.

In the median mode, the loop works as follows:

The sign of the true gain error selects a fixed gain error of 0010000000000_b or 1110000000000_b.

These gain error values are scaled by the programmable AGC loop gains to adjust the data path gain.

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The maximum slew rate is ~1.5dB per output sample. See Equation 18.

In order to fully evaluate the dynamic range of the PDC, Table 9B is provided, which details the bit weighting from the input to the AGC Multiplier.

Re-Sampler/Halfband Filter

The re-sampler is an NCO controlled polyphase filter that allows the output sample rate to have a non-integer relationship to the input sample rate. The filter engine can be viewed conceptually as a fixed interpolation filter, followed by an NCO controlled decimator.

The prototype polyphase filter has 192 taps designed at 32 times the input sample rate. Each of the 32 phases has 6 filter taps (6)(32) = 192. The stopband attenuation of the prototype filter is greater than 60dB, as shown in Figure 24. The signal to total image power ratio is approximately 55dB, due to the aliasing of the interpolation images. The filter is capable of decimation factors from 1 to 4. If the output is at least 2x the baud rate, the 32 interpolation phases yield an effective sample rate of 64x the baud rate or approximately 1.5%, (1/64), maximum timing error.

Following the Re-sampler are two interpolation halfband filters. The halfband filters allow the user to up-sample by 2 or 4 to recover time resolution lost by decimating. Interpolating by 2 or 4 gives 1/4 or 1/8 baud time resolution (assuming 2x baud at the re-sampler output). The halfband filters use the same coefficients as HB3 and HB5 from the Halfband Filters Section. If one halfband is used, the 23-tap filter is chosen. If two are used, the 23-tap filter runs first followed by the 15-tap filter operating at twice the first halfband's rate. The 23-tap filter requires 7 multiplies, and the 15-tap filter requires 5 multiplies to complete a filter calculation.

Using the interpolation halfband filters allows for reduction in the FIR filter sample rate. This optimizes the use of the programmable FIR filter by allowing the FIR output sample rate to be closer to the Nyquist rate of the desired bandwidth. Optimizing the FIR filter performance provides better use of the programmable FIR taps. Table 10 details the maximum clocking rates for the possible resampling and interpolation halfband filter configurations of this section of the PDC. Control Word 16, Bits 2-0 identify the filter configuration. Control Word 16, Bit 3 is used to bypass the polyphase re-sampler filter.

For proper data output from the interpolation filters, the data ready signal must account for the interpolation process. Figure 25 illustrates the insertion of additional data ready pulses to provide sufficient pulses for the new output sample rate. The Re-sampler Output Pulse Delay parameter is set in Control Word 16, Bits 4-11. These bits set the delay between the output samples when interpolation is utilized. Program this distance between pulses using

$$N = [(f_{PROCCLK}/f_{OUT}) - 1] \quad \text{(EQ. 20)}$$

A value of at least 5 is required to have sufficient time to update the Output Buffer Register. (Writing 5 samples requires 5 clock cycles) A value of at least 16 is required for proper serial output from the part. (Conversion from 16-bit parallel to serial). The value is programmed in numbers of PROCCLK's.

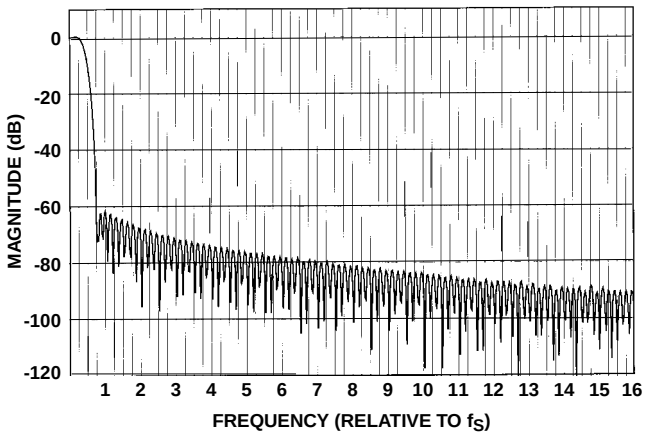


FIGURE 24A. POLYPHASE RESAMPLER FILTER BROADBAND FREQUENCY RESPONSE

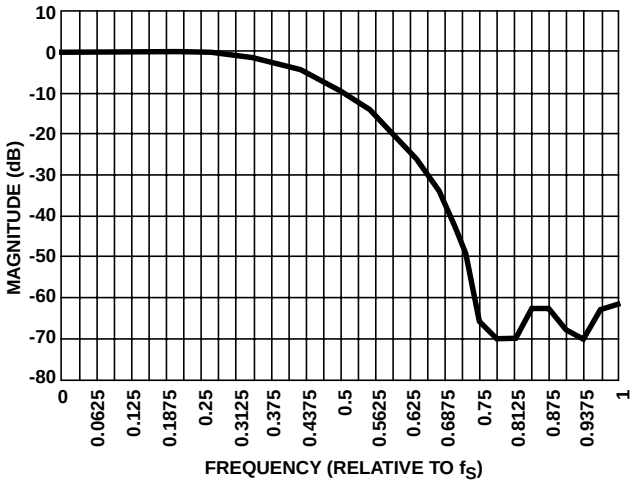


FIGURE 24B. POLYPHASE RESAMPLER FILTER PASS BAND FREQUENCY RESPONSE

There is a 65dB limitation in SNR using the Re-Sampler Filter. When only the Interpolation FIRs are used, the full SNR range is passed.

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TABLE 9A. BIT WEIGHTING FOR AGC LOOP FEEDBACK PATH

AGC ACCUM BIT POSITION	GAIN ERROR INPUT	GAIN ERROR BIT WEIGHT	AGC LOOP FILTER GAIN (MANTISSA)	AGC LOOP FILTER GAIN MULTIPLIER (OUTPUT)	SHIFT = 0	SHIFT = 4	SHIFT = 8	SHIFT = 15	AGC OUTPUT AND AGC LIMITS BIT WEIGHT		AGC GAIN RESOLUTION (dB)
31					2	2	2	2	0		
30					2	2	2	2	E	3	48
29					2	2	2	2	E	2	24
28					2	2	2	2	E	1	12
27	12	= 2		2	2	2	2	2	E	0	6
26	11	= 1		1	2	2	2	1	M	-1	3
25	10	= 0.	0.	0.	2	2	2	0.	M	-2	1.5
24	9	= 1	x	1	2	2	2	1	M	-3	0.75
23	8	= 2	x	2	2	2	2	2	M	-4	0.375
22	7	= 3	x	3	2	2	2	3	M	-5	0.1875
21	6	= 4	x	4	2	2	2	4	M	-6	0.09375
20	5	= 5		5	2	2	2	5	M	-7	0.04688
19	4	= 6		6	2	2	1	6	X	-8	0.02344
18	3	= 7		7	2	2	0.	7		-9	0.01172
17	2	= 8		8	2	2	1	8		-10	0.00586
16	1	= 9		9	2	2	2	9		-11	0.00293
15	0	= 10		10	2	1	3	10		-12	0.00146
14				11	2	0.	4	11		-13	0.000732
13				12	2	1	5	12		-14	0.000366
12				13	2	2	6	13		-15	0.000183
11				14	1	3	7	14		-16	0.0000916
10					0.	4	8	G		-17	0.0000458
9					1	5	9	G		-18	0.0000229
8					2	6	10	G		-19	0.0000114
7					3	7	11	G		-20	0.00000572
6					4	8	12	G		-21	0.00000286
5					5	9	13	G			
4					6	10	14	G			
3					7	11	G	G			
2					8	12	G	G			
1					9	13	G	G			
0					10	14	G	G			

AGC Response_{Max} = Input(Cart/PolarGain)(Error Det Gain)(AGC Loop Gain_{Max})(AGC Output Weighting). G = ground = 0.

$$\text{AGC Response}_{Max} = (\sqrt{2})(1.64676)\left(\frac{15}{16}\right)(1)(1.5\text{dB}) \sim 3.275\text{dB/output sample time}.$$

$$\text{AGC Response}_{Min} = (\sqrt{2})(1.64676)(2^{-15})(1)(1.5\text{dB}) \sim 0.000106\text{dB/output sample time}.$$

Thus, the expected range for the AGC rate is ~ 0.000106 to 3.275dB/output sample time.

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TABLE 9B. PDC BIT WEIGHTING

BIT WEIGHT	INPUT	SIN/COS	MIX OUT	CIC IN SHIFT = 0	CIC IN SHIFT = 15	CIC BIT WEIGHTS IIIIICCCCC	CIC OUT	HB DATA IN	HB DATA OUT/FIR IN	FIR COEF	FIR MULTI/ ACC	FIR OUT
0	0	0	0	S	S	xxxxxxxxxx	0	0	0	0	1	
1	1	1	1	S	S	xxxxxxxxxx	1	1	1	1	0	0
2	2	2	2	S	S	xxxxxxxxxx	2	2	2	2	1	1
3	3	3	3	S	S	xxxxxxxxxx	3	3	3	3	2	2
4	4	4	4	S	S	xxxxxxxxxx	4	4	4	4	3	3
5	5	5	5	S	S	xxxxxxxxxx	5	5	5	5	4	4
6	6	6	6	S	S	xxxxxxxxxx	6	6	6	6	5	5
7	7	7	7	S	S	xxxxxxxxxx	7	7	7	7	6	6
8	8	8	8	S	S	xxxxxxxxxx	8	8	8	8	7	7
9	9	9	9	S	S	xxxxxxxxxx	9	9	9	9	8	8
10	10	10	10	S	10(S)	xxxxxxxxxx	10	10	10	10	9	9
11	11	11	11	S	11	xxxxxxxxxx	11	11	11	11	10	10
12	12	12	12	S	12	xxxxxxxxxx	12	12	12	12	11	11
13	13	13	13	S	13	xxxxxxxxxx	13	13	13	13	12	12
14		14	14	S	14	xxxxxxxxxx	14	14	14	14	13	13
15		15	SRnd	S	15	xxxxxxxxxx	15	15	15	15	14	14
16		16		S	16	xxxxxxxxxx	16	16	16	16	15	15
17		17		S	17	xxxxxxxxxx	17	17	17	17	16	16
18				S	18	xxxxxxxxxx	18	18	18	18	17	17
19				S	19	xxxxxxxxxx	19	19	19	19	18	18
20				S	20	xxxxxxxxxx	20	20	20	20	19	19
21				S	21	xxxxxxxxxx	21	21	21	21	20	20
22				S	22	xxxxxxxxxx	22	22	22		21	21
23				S	23	xxxxxxxxxx	23	23	23		22	22
24				S	24	xxxxx	Rnd	Rnd	Rnd		23	23
25				25(S)	25	xxxxx	SAT	SAT	SAT		24	24
26				26	26	xxxxx					25	Rnd
27				27	27	xxxxx					26	SAT
28				28	28	xxxxx					27	
29				29	29	xxxxx					28	
30				30	30	xxxxx					29	
31				31	31	xxxxx					30	
32				32	32	xx					31	
33				33	33	xx					32	
34				34	34	xx					(Rnd Out of Mult.)	
35				35	35	xx						
36				36	36	x						
37				37	37	x						
38				38	38	x						
39				39	39	x						

NOTES:

1. SRnd = Symmetric Round; Rnd = Round; SAT = Saturation.
2. The NBW out of the CIC filter is 0.5 x f_{SOUT}. If the $NBW_{IN} = f_S/4$ and $NBWOUT = f_{SOUT}/2$, then the processing gain for a decimation x 16 CIC should be ~ 8 (9dB or 1.5 bits) versus A/D noise, the processing gain should be $10\log(BW_{IN}/BW_{OUT})$.

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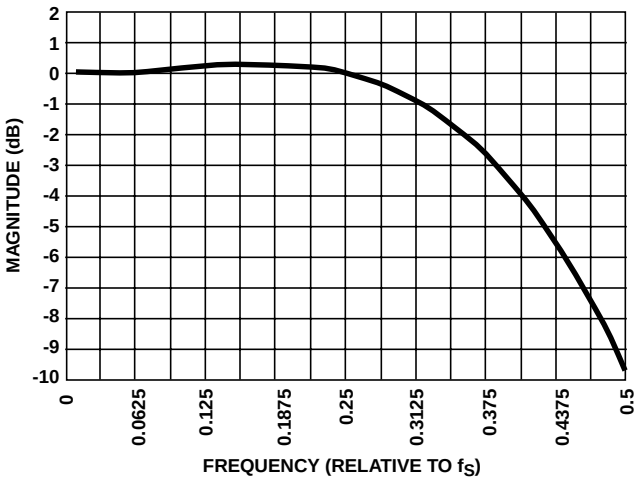


FIGURE 24C. POLYPHASE RESAMPLER FILTER EXPANDED RESOLUTION PASSBAND FREQUENCY RESPONSE

TABLE 10. POLYPHASE AND INTERPOLATING HALFBAND FILTER MAXIMUM CLOCKING RATES

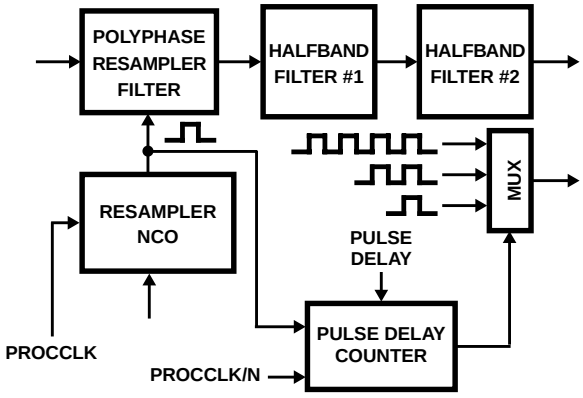
MODE	CLOCK CY-CLES	RE-SAM-PLER INPUT RATE (MHz)	INTER-POLATION RATE	OUTPUT RATE (MHz)
Bypass	0	55.00	-	55.00
Polyphase Filter	6	55/6 = 9.17	-	9.17 (Note 3)
Polyphase and 1 Halfband Filter	13	55/13 = 4.23	2	8.46 (Note 3)
Polyphase and 2 Halfband Filters	23	55/23 = 2.39	4	9.56 (Note 3)
1 Halfband Filter	7	55/7 = 7.86	2	15.72
2 Halfband Filters	17	55/17 = 3.24	4	12.94

NOTE:

3. This frequency is set by the Resampler NCO.

In burst systems (such as TDMA), time resolution is needed for quickly identifying the optimum sample point. The timing is adjusted by shifting the decimation in the DSP µP to the closest sample. Use of timing error in this way may yield a faster acquisition than a phase-locked loop coherent bit synchronization. Finding the optimum sample point minimizes intersymbol interference.

Fine time resolution is needed in CDMA systems to resolve different multipath rays. In CDMA systems, the demands on the programmable FIR can only be relieved by the resampler/interpolation halfband filters. Assume the chip rate for a baseband CDMA system is 1.2288MHz and PROCCLK is limited to 55MHz. Using the symmetric filter pre-sum approach, PROCCLK limits the programmable FIR to 110MIPS (millions of instructions per second) effective due to symmetry. If the CDMA filter (loaded into the programmable FIR Section) requires an impulse response with a span of 12 chips, the filter at 2x the chip-rate would need 24 taps. The 24 taps would translate into 59MIPS = (1.2288MHz)(2)(24). To get the same filtering at 8x the chip rate would require 944MIPS = (1.2288MHz)(8)(96). Direct 8x filtering can not be accomplished with the programmable filter alone because 944MIPS are much greater that the 60MIPs effective limit set by PROCCLK. It is necessary to decimate down to 2x the chip rate to get a realistic number of filter taps. Both interpolation halfband filters are then used to obtain the 8x CDMA output. 944MIPS is a lot of MIPS. The HSP50214B gets the equivalent processing by decimating down and interpolating backup.



THIS BLOCK GENERATES EXTRA DATA READY PULSES FOR THE NEW OUTPUTS FROM THE INTERPOLATION PROCESS.

HB2	HB1	RSMPLR	# EXTRA PULSES
0	0	0	0 BYPASS
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	3 (NV)
1	0	1	3 (NV)
1	1	0	3
1	1	1	3

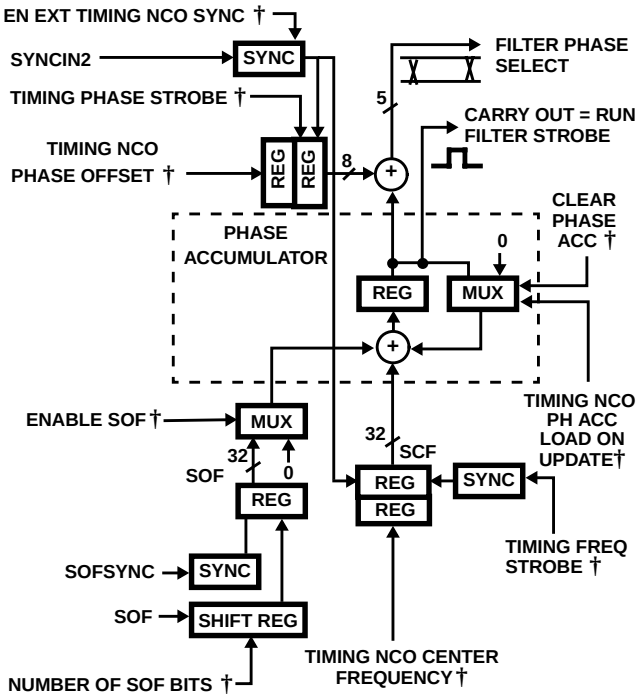
NV = INVALID MODE

FIGURE 25. GENERATING DATA READY PULSES FOR OUTPUT DATA

Timing NCO

The Timing NCO is very similar to the carrier NCO Phase Accumulator Section. It provides the NCO driven sample pulse and associated phase information to the resampling filter process described in the Re-sampler Filter Section. The Timing NCO does not include the SIN/COS Section found in the Carrier NCO. The top level block diagram is shown in Figure 26.

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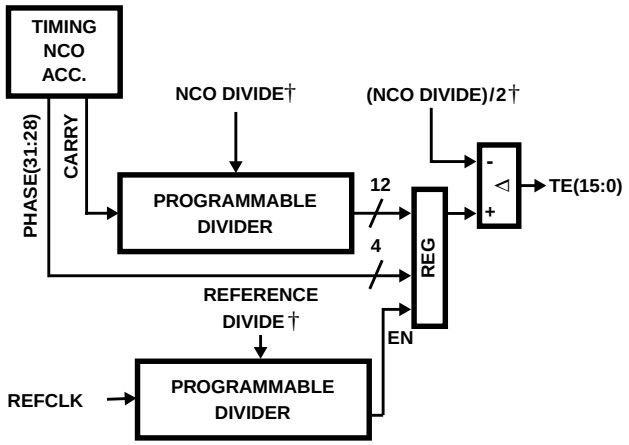


† Controlled via microprocessor interface.

FIGURE 26. TIMING NCO BLOCK DIAGRAM

The programmable parameters for the Timing NCO include an Enable External Timing NCO Sync (Control Word 11, Bit 5), the serial word width, Number of Offset Frequency Bits (Control Word 11, Bits 3-4), an Enable Offset Frequency control (Control Word 11, Bit 2), a Clear NCO Accumulator control (Control Word 11, Bit 1), a Timing NCO Phase Accumulator Load On Update control (Control Word 11, Bit 0), the Timing NCO Center Frequency (Control Word 12), a Timing Phase Offset (Control Word 13, Bits 0-7), a Timing Frequency Strobe (Control Word 14) and a Timing Phase Strobe (Control Word 15). Refer to the Carrier Synthesizer Mixer Section for a detailed discussion of the serial interface for the Timing NCO offset frequency word.

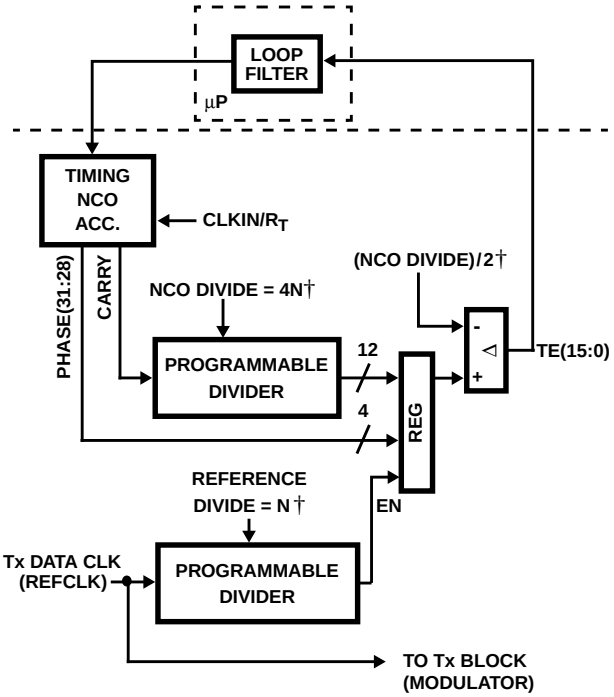
A timing error detector is provided for measuring the phase difference between the timing NCO and a external clock input, REFCLK. Timing Error is generated by comparing the values of two programmable counters. One counter is clocked with the Timing NCO carry out and the other is clocked by the REFCLK. The 12-bit NCO Divide parameter is set in Control Word 18, Bits 16-27. The NCO Divide parameter is the preload to the counter that is clocked by the Timing NCO carry out. The 12-bit Reference Divide parameter is set in Control Word 18, Bits 0-11, and is the preload for the counter that is clocked by the Reference clock. Figure 26 details the block diagram of the timing error generation circuit. The 16 bits of timing error are available both as a PDC serial output and as a processor read parameter. See the Processor Read Section for more details on accessing this value.



† Controlled via microprocessor interface.

FIGURE 27. TIMING ERROR GENERATION

Figure 27A illustrates an application where the Timing Error Generator is used to lock the receiver samples with a transmit data rate. In this example, the receive samples are at four times the transmit data rate. An external loop filter is required, whose frequency error output is fed into the Timing NCO. This allows the loop to track out the long term drift between the receive sample rate and the transmit data clock.



R_T = TOTAL DECIMATION (CIC, HB FILTERS AND FIR)

† Controlled via microprocessor interface.

FIGURE 27A. TIMING ERROR APPLICATION

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Cartesian to Polar Converter

The Cartesian to Polar converter computes the magnitude and phase of the I/Q vector. The I and Q inputs are 18 bits. The converter phase output is 18 bits (truncated) with the 16 MSB's routed to the output formatter and all 18 bits routed to the frequency discriminator. The 16-bit output phase can be interpreted either as two's complement (-0.5 to approximately 0.5) or unsigned (0.0 to approximately 1.0), as shown in Figure 28. The phase conversion gain is $1/2\pi$. The phase resolution is 16 bits. The 16-bit magnitude is unsigned binary format with a range from 0 to 2.32. The magnitude conversion gain is 1.64676. The magnitude resolution is 16 bits. The MSB is always zero.

Table 11 details the phase and magnitude weighting for the 16 bits output from the PDC.

TABLE 11. MAG/PHASE BIT WEIGHTING

BIT	MAGNITUDE	PHASE (^{O})
15 (MSB)	2^2 (Always 0)	180
14	2^1	90
13	2^0	45
12	2^{-1}	22.5
11	2^{-2}	11.25
10	2^{-3}	5.625
9	2^{-4}	2.8125
8	2^{-5}	1.40625
7	2^{-6}	0.703125
6	2^{-7}	0.3515625
5	2^{-8}	0.17578125
4	2^{-9}	0.087890625
3	2^{-10}	0.043945312
2	2^{-11}	0.021972656
1	2^{-12}	0.010986328
0 (LSB)	2^{-13}	0.005483164

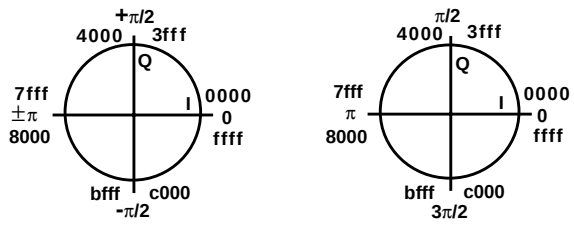


FIGURE 28. PHASE BIT MAPPING OF COORDINATE CONVERTER OUTPUT

The magnitude and phase computation requires 17 clocks for full precision. At the end of the 17 clocks, the magnitude and phase are latched into a register to be held for the next stage, either the output formatter or frequency discriminator. If a new input sample arrives before the end of the 17 cycles, the results of the computations up until that time, are latched. This latching means that an increase in speed causes only a decrease in resolution. Table 12 details the exact resolution that can be obtained with a fixed number of clock cycles up to the required 17. The input magnitude and phase errors induced by normal SNR values will almost always be worse than the Cartesian to Polar conversion.

TABLE 12. MAG/PHASE ACCURACY vs CLOCK CYCLES

CLOCKS	MAGNITUDE ERROR (% f_S)	PHASE ERROR (DEG.)†	PHASE ERROR (% f_S)
6	0.065	3.5	2
7	0.016	1.8	1
8	0.004	0.9	0.5
9	<0.004	0.45	0.25
10	<0.004	0.22	0.12
11	<0.004	0.11	0.062
12	<0.004	0.056	0.03
13	<0.004	0.028	0.016
14	<0.004	0.014	0.008
15	<0.004	0.007	0.004
16	<0.004	0.0035	0.002
17	<0.004	0.00175	0.001

† Assumes $\pm 180^O = f_S$.

In the HSP50214, the input to the coordinate converter I/Q to |r|/θ) block is 18 bits. If the signal range is large and the AGC is not used, the quantization noise can become a contributing factor in the phase and frequency computations. For example, if the signal range is 84dB and the maximum signal is set at full scale, the minimum signal would have only 4 bits each for I and Q.

In the HSP50214B, an additional data path option was added that allows the output of the 255 tap programmable FIR filter to be routed directly to the coordinate converter. Rather than having to select only 18 bits out of the available 26 bit output, all 26 bits of the FIR output are routed to the coordinate converter. This change eliminates quantization effects to give more accuracy in the phase and frequency discriminator outputs. The AGC settling time is not a factor because the AGC is effectively bypassed for the magnitude, phase, and frequency computations.

NOTE: The most significant 18 bits of the computed phase are still routed to the discriminator.

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One caveat to selecting the FIR outputs to be routed directly to the coordinate converter is that because the I/Q samples for the coordinate conversion are chosen from before the resampler, the magnitude and phase samples will not align with the I/Q samples, if the resampler or interpolation halfband filters are used.

This optional signal routing mode was intended for FM or for burst PSK where a fixed decimation can be used. It is also applicable when resampling or timing adjustments on the demodulated samples are done in a processor following PDC.

The magnitude resolution may suffer because there is no gain adjustment before computing the magnitude. If the signal is < - 90dBFS, it will be below the LSB of the magnitude output.

The enable signal for gating data into the coordinate converter is either the AGC data ready signal or the resampler data ready signal. If the resampler is bypassed, the AGC data ready signal is used and there is a delay of 6 clock cycles between the FIR data being ready and the coordinate converter block sampling it. If the resampler is enabled, its data ready signal will be delayed by 6 clocks (for the AGC) plus the compute delay of the resampler block. This may cause the I/Q to $|r|/\theta$ output sample alignment to shift with decimation. For this reason, it is recommended that the resampler/halfband filter block be bypassed when using this new data path.

To select the output of the 255 tap programmable FIR filter to be routed to the coordinate converter, set Control Word 27, Bit 13 to a logic one. For routing as in the HSP50214, set Control Word 27, Bit 13 to a logic zero.

Frequency Discriminator

The discriminator block delays phase from the Cartesian to Polar Section and subtracts it from the latest sample. This delay and subtract can be modeled as a programmable delay comb filter. The output of the filter is $d\theta/dt$, or frequency. The transfer function of the discriminator is set by

$$H(z) = 1 - Z^{-D} \quad \text{(EQ. 21)}$$

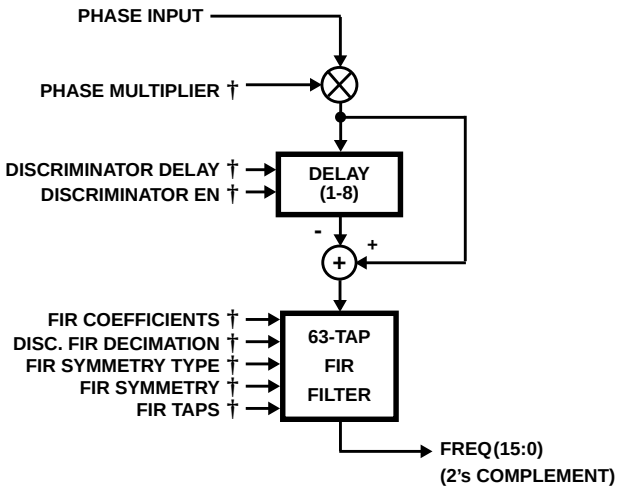
where D is the programmable discriminator delay expressed in number of sample clock delays. The discriminator output frequency is then filtered with a programmable FIR filter. The Block Diagram of the Frequency Discriminator is shown in Figure 29.

The range of delay in the discriminator is from 1 to 8 samples. Modulo 2π subtraction eliminates rollover problems in the subtraction at 2π. The alias free discriminator frequency range is given by:

$$\text{Range}_{FREQDISC} = CW \pm F_{SAMPOUT}/(D+1); \quad \text{(EQ. 22)}$$

where D is the discriminator delay defined in Equation 21 ($1 < D < 8$), $f_{SAMPOUT}$ is the Discriminator FIR filter output sample rate and CW is the desired center frequency. When the phase multiplier is set to a value other than 2^0, the discriminator range is reduced proportionally. The phase multiplier can be 1, 2, 4 or 8 (2^0 to 2^3). Thus, a multiply of 2^1 reduces the range by 2, a multiply of 2^2 reduces the range by 4, and a multiply of 2^3 reduces the range by 8.

The FIR filter can be configured with up to 63 symmetric taps and up to 32 asymmetric taps. In the symmetric mode, the FIR can be configured for even or odd symmetry, as well as with an even or odd number of filter taps. Decimation is provided to allow more processing time for longer (i.e., more taps) filter structures.



† Controlled via microprocessor interface.

FIGURE 29. FREQUENCY DISCRIMINATOR BLOCK DIAGRAM

The HSP50214B offers an expanded choice of signals to be filtered by the discriminator FIR. The choices are:

1) 18 bits of delayed, and subtracted (and optionally shifted) phase. This is the Discriminator FIR filter input found in the HSP50214.

2) 18 bits of magnitude from the coordinate converter block. This was added to provide for post-detection filtering of AM signals.

3) 18 bits from the I output of the resampler/interpolation halfband filter block. This was added to provide for processing of SSB signals.

The shift, delay, and subtract functions are bypassed for items (2) and (3).

In addition to the FIR input selections, the Q input to the coordinate converter block can be zeroed so that the magnitude output is the magnitude of I only. Again this was added to provide for processing SSB signals.

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The Discriminator FIR filter input selections are made in Control Word 27, Bits 18 and 19. The bit definitions are:

00 Item (1) described above.

01 Item (2) described above.

1X Item (3) described above.

Control Word 27, Bit 14 is used to control the Q input to the coordinate converter. The bit definitions is:

0 I and Q enabled to the I/Q to R/Theta block.

1 The Q input to the I/Q to R/Theta block is zeroed.

The enable signals associated with the various input selections to the Discriminator FIR filter are:

1 The data ready strobe from the coordinate converter block.

2 The data ready strobe from the coordinate converter block.

The enable signals associated with the various input selections to the coordinate converter are:

3a The data ready signal to the coordinate converter block when the resampler is bypassed. This is the AGC output data ready signal.

3b The data ready to the coordinate converter block when the resampler/halfband filters are enabled. This is the resampler halfband filter block output data ready signal.

The discriminator input is 18 bits, and the output is rounded asymmetrically to 16 bits. The phase into the discriminator can be multiplied by 2^0, 2^1, 2^2, or 2^3 (modulo 2π) to remove PSK data modulation. All programmable parameters for the Frequency Discriminator are set in Control Word 17. Bits 15 and 16 are the phase multiplier which represents the shift applied to the input phase. For CW, the multiply should equal 2^0, (00). For BPSK, QPSK, and 8PSK, the multiply should equal 2^1, (01); 2^2, (10); or 2^3, (11); respectively. Bit 14 is used to enable or disable the discriminator. Bits 11-13 set the decimation in the programmable FIR filter. Bit 10 sets the filter symmetry type as either odd or even, bit 9 sets whether the filter is asymmetric or symmetric, and bits 3-8 set the number of FIR filter taps. Bits 0-2 set the number of delays in the frequency discriminator.

Output Section

The Output Section routes the 7 types of processed signals to output pins in three basic modes. These basic modes are: Parallel Direct Output, Serial Direct Output, and the Buffer RAM Output. The Serial and Parallel Direct Output modes were designed to output data strobes and “real time” continuous streams of data. The Buffer RAM Output mode outputs data upon receipt of an asynchronous request from an external DSP processor or other baseband processing engine. The use of the interrupt signal from the Programmable Down Converter in conjunction with the request strobes from the controller ensures that data is transferred only when both the controller and the Programmable Down Converter are ready. The Buffer RAM output can be operated in a First In First Out (FIFO) or SNAPSHOT mode with the data output either via the 8-bit processor interface or a 16-bit processor interface.

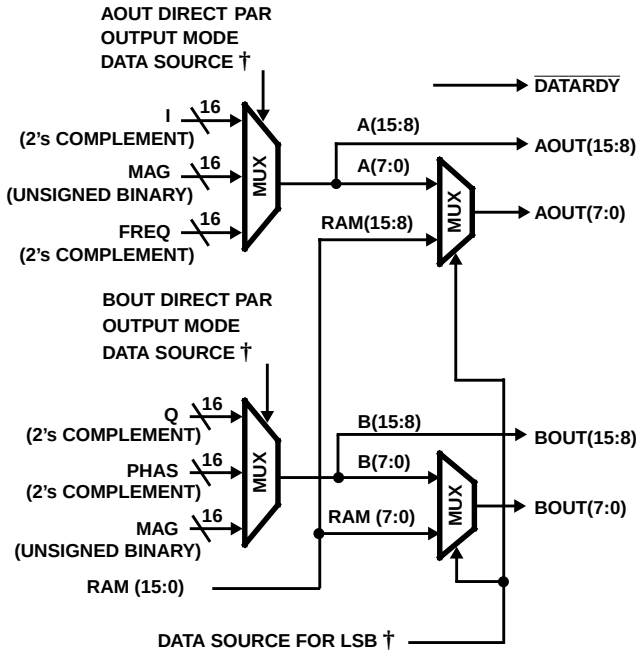
Parallel Direct Output Port Mode

The Parallel Direct Output Port Mode outputs two 16-bit words, AOUT and BOUT, of “real time” data. Figure 30 details the parallel output circuitry. Selection of the data source for the AOUT and BOUT parallel outputs is done via Control Word 20, Bits 22-23, and 20-21, respectively. The AOUT port can output I, Magnitude, or Frequency data. The BOUT port can output Q, Phase or Magnitude data. The upper bytes of AOUT and BOUT are always in the parallel direct mode. The 16-bit parallel direct mode is selected by setting Control Word 20, Bit 25, to zero.

The $\overline{\text{DATARDY}}$ output is asserted during the first clock cycle of the new data on the AOUT bus. The rate at which the data out of the HSP50214 transitions and the rate at which $\overline{\text{DATARDY}}$ is asserted can be different.

Data Transitions:

The transition rate of the parallel output data is dependent on which of the three types of data is selected for the AOUT Output channel: I (real symbols), |r| (magnitude), or f (frequency). Q (quadrature symbols), ø (phase), or |r| (magnitude) are available on the BOUT output. When selected as an output, the I Q, |r|, and ø outputs transition at the symbol rate. The f (frequency) output transitions at the discriminator FIR filter output rate.



† Controlled via microprocessor interface.

FIGURE 30. PARALLEL OUTPUT BLOCK DIAGRAM

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Data Ready Signal Assertion Rate:

The assertion rate of the $\overline{\text{DATARDY}}$ signal Is the data transition rate of the A_{OUT} output data either [I, |r| or f]. The time alignment of parallel data words available for output are as follows:

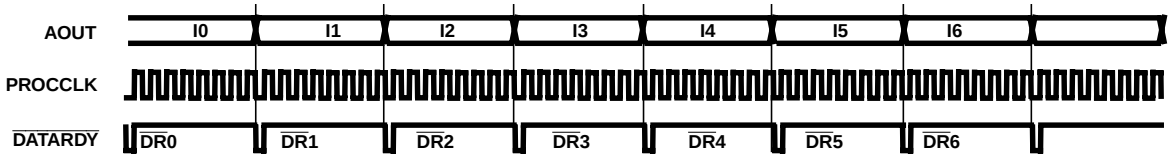
I and Q are aligned in time,

|r| and ø are time aligned, but one sample clock delayed from the associated I and Q samples.

DATARDY Is asserted time aligned with and at the same rate as the data type selected for the AOUT output. Figure 31 details the timing of the AOUT and $\overline{\text{DATARDY}}$ for an AOUT = I data selection.

Note that the BOUT data word may be at a different rate and skewed in time with respect to $\overline{\text{DATARDY}}$, depending on the type of data selected for output. This is because of the timing relationships defined above, and because the DATARDY is driven by the AOUT signal. Figure 32 details such a configuration.

When the f (frequency) word is selected for output on AOUT, the DATARDY signal is asserted at the discriminator FIR filter output rate, which will be a reduced rate when decimation is engaged in the filter. The f (frequency)S output is delayed from the associated I and Q samples one sample time plus, the discriminator FIR filter impulse response time. Figure 33 details the timing of this configuration for a FIR filter that decimates by 4.



NOTE: The number of PROCCLKS per output symbol is not representative, but shown to be small for clarity of establishing timing with respect to the DATARDY signal. For each application, the relationship of the output symbol rate to PROCCLK must be properly illustrated to determine the exact nature of the timing.

FIGURE 31. $\overline{\text{DATARDY}}$ WAVEFORMS WHEN I (READ DATA) IS SELECTED AS AOUT

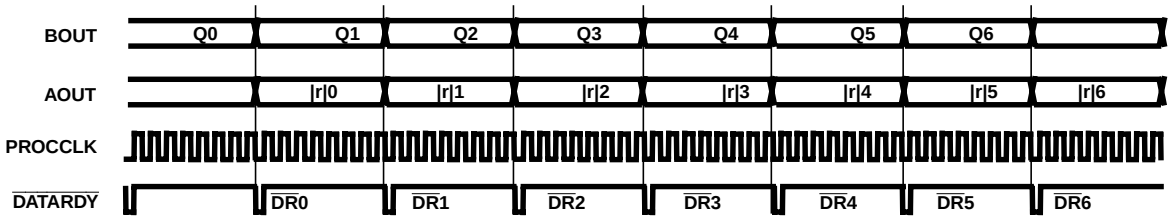
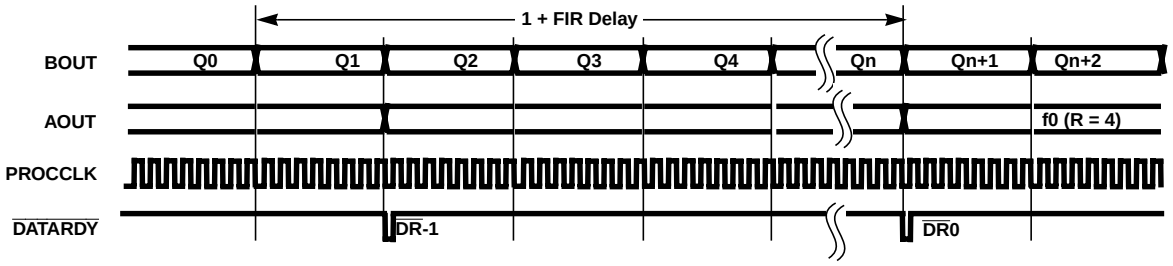


FIGURE 32. DATARDY WAVEFORMS WHEN |r| (MAGNITUDE) IS SELECTED AS AOUT



***NOTE:** I and Q are sample aligned in time. |r| and ϕ are sample aligned in time, but one sample delayed from I or Q. The frequency sample is delayed in time from I or Q by 1 sample time + 63 tap FIR impulse response. If the FIR is set to decimate and frequency is selected for AOUT, the DATARDY signal will be at the discriminator FIR output (decimated) rate.*

FIGURE 33. DATARDY WAVEFORMS WHEN f (FREQUENCY) IS SELECTED AS AOUT

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Serial Direct Output Port Mode

The Serial Direct Output Port Mode offers the ability to construct two serial output data streams, SEROUTA AND SEROUTB, from 16-bit I, Q, magnitude, phase, frequency, timing error, and AGC level data words. The total number of data words (1 to 8) for serial output, and the sequential order of these data word components of the serial output are programmable. Each data word may be used once in either the SEROUTA or SEROUTB data streams. Figure 34 illustrates the conceptual implementation of the Serial Direct Output Port Mode.

In the Serial Direct Mode, the output data is loaded into Serial Shift Registers and routed to two serial output pins, SEROUTA and SEROUTB. The serial output shift clock, SERCLK, is PROCCLK divided by 1, 2, 4, 8, or 16. The divide down ratio is programmed using Control Word 20, Bits 14-16. The data is shifted out on the rising edge of the internal SERCLK. The external clock polarity of SERCLK is programmable via Control Word 20, Bit 18. A sync signal is provided for detection of the start or end of each word in the serial sequence. Control Word 20, Bit 17, sets the SERSYNC signal location as either preceding the MSB (typical for interfacing with microprocessors) or following the LSB (typical for interfacing to D/A converters). Control Word 20, Bit 19, sets the SERSYNC polarity as active low or high. The LSB of each data word can be configured as either the true LSB data, or set at a fixed logic “1” or “0” for use as a tag bit. Control Word 20, Bits 0-13 set the LSB of each of the 7 types of data words that can be configured in the serial output stream. Control Word 19, Bits 21-24 set the number of serial data words that will be linked to form the serial outputs. Up to 7 data words can be linked to form the serial output. SEROUTA and SEROUTB will have an identical number of words in the serial output streams.

The 16-bit I, Q, magnitude, phase, frequency, timing error, AGC level, and “zeros” data words are loaded into their respective shift registers. The Magnitude and AGC Level data word are unsigned binary format with a leading zero, while the remaining signals are 2’s complement format.

Any of the eight data sources can be selected as the first serial word for SEROUTA or SEROUTB. Control Word 19, Bits 25-30 set the data type for the first serial word for SEROUTA and SEROUTB. The three bit data type identifier is shown both in Table 13 and in Figure 34, to the right of the controls for the cross matrix switch. Serial output data word sequences are formed by linking data words by programming the data source for each shift requester’s shift input signal. This programming links the Shift Registers together in one or two serial chains. Thus, the Control Word 19 term “Link follows X data”, where X is one of the seven data types. Once the data source data word is selected (by programming a three bit word representing one of the data types into Control Word 19, Bits 25-27 (SEROUTA), and 28-30 (SEROUTB)), the process for identifying the next word is to select a three bit data type identifier which represents the data type to follow the source data type. Program these bits into the Control Word 19 field representing the “Link following X data”, where X = the source data type, defines the second word in the sequence. Likewise, the third data word is linked by selecting the Control Word 19 bits that identify the “Link following X data”, where X = the data type of the second word in the serial chain. The process continues until all the desired data words have been linked.

NOTE: ***I and Q are sample aligned in time. |r| and ϕ are sample aligned in time, but one sample delayed from I or Q. The frequency sample is delayed in time from I or Q by 1 sample time + 63 tap FIR impulse response. If the FIR is set to decimate, the FIR output will be repeated every sample time until a new value appears at the filter output. (i.e., the frequency samples are clocked out at the I, Q sample rate regardless of decimation.)***

TABLE 13. LINKING CONTROL WORDS FOR SERIAL OUTPUT

DATA TYPE IDENTIFIER	DATA TYPE
000	I Data
001	Q Data
010	Magnitude (MAG) Data
011	Phase (PHAS) Data
100	Frequency (FREQ) Data
101	Timing Error (TIMER) Data
110	AGC Gain
111	Zeros

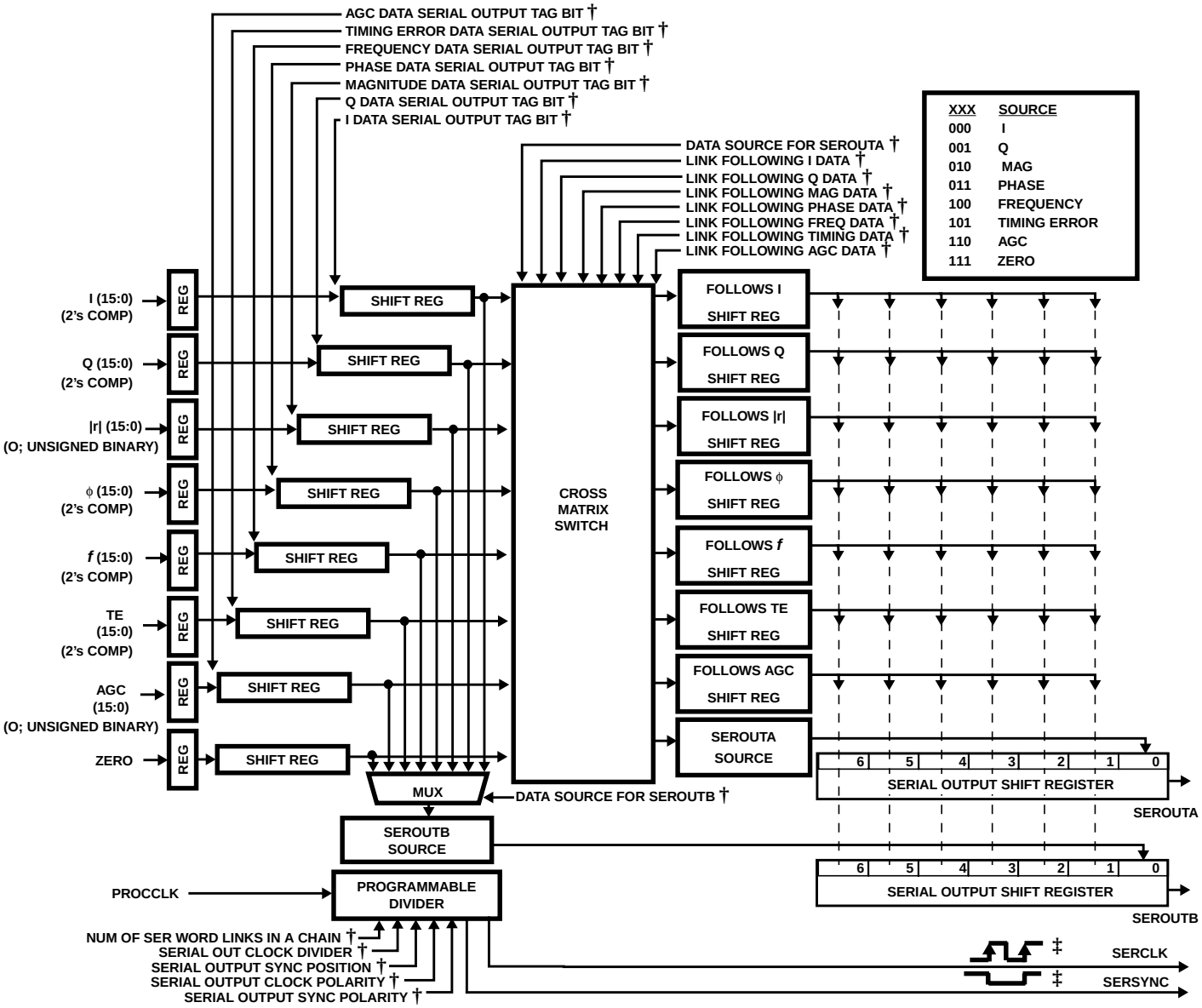
Two examples will illustrate the process of configuring a serial output using the Serial Output mode.

The serial data stream looks like:

SEROUTA:	**CONTROL WORD 19 FIELD**
start	
I data word >	SEROUTA source data = 000
Q data word >	Link following I data = 001
ϕ data word >	Link following Q data = 011
Zero data word >	Link following ϕ data = 111
end >	

SEROUTB:	**CONTROL WORD 19 FIELD**
start	
|r| data word >	SEROUTB source data = 010
f data word >	Link following |r| data = 100
TE data word>	Link following *f* data = 101
AGC data word >	Link following TE data = 110
end >	

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† Controlled via microprocessor interface

‡ Polarity is programmable

FIGURE 34. SERIAL OUTPUT FORMATTER BLOCK DIAGRAM

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Serial Output Configuration Example 1:

It is desired to output the I data word, followed by the Q data word, followed by the Phase data word on the SEROUTA output. Similarly, it is desired to output the Magnitude data word followed by the Frequency data word, followed by the Timing Error data word, followed by the AGC Level data word on the SEROUTB output. Table 14 illustrates how Control Word 19 should be programmed.

TABLE 14. EXAMPLE 1 SERIAL OUTPUT CONTROL SETTINGS

CONTROL WORD 19 BIT POSITION	FUNCTION	BIT VALUE	RESULT
30-28	SEROUTA Data Source	000	(I)
27-25	SEROUTB Data Source	010	(|r|)
24-21	Number of Serial Word Links in a Chain	100	(4)
20-18	Link following I data	001	(Q)
17-15	Link following Q data	011	(ϕ)
14-12	Link following |r| data	100	(*f*)
11-9	Link following ϕ data	111	(Zeros)
8-6	Link following ***f*** data	101	(Timing)
5-3	Link following AGC data	XXX	(N/A)
2-0	Link following Timing Error data	110	(AGC)

NOTE: ***Because all but the first data word in the serial output is identified by the data type that it follows, SEROUTB can only be fully independent of the sequence in SEROUTA if it does not use any of the same data word types. This implies a partition as described in Example 1. Once a data word that is used in SEROUTA is called out in SEROUTB, the remaining sequence in SEROUTB will be identical to that portion of SEROUTA sequence that follows the duplicate data type. This follows from using the "Link follows 'data type' data" for word linkage.***

NOTE: ***Each type of data word should be used only once in each data stream. If the "Link following I data" is programmed with the data type identifier for I, then the part will repeat the I data word until all of the data word locations are filled. In Example 1, if bits 20-18 were erroneously programmed to 000 (I data) then the SEROUTA would be four sequential repeats of the I data word.***

Serial Output Configuration Example 2:

It is desired to output only three data words on each serial output. The I data word, followed by the Q data word, followed by the Magnitude data word is to be output on SEROUTA. The Q data word followed by the Magnitude data word, followed by the one other data word to be output on SEROUTB. The choices for the remaining data word in the SEROUTB signal are: phase, frequency, AGC level and timing error. Table 15 illustrates how Control Word 19 should be programmed.

TABLE 15. EXAMPLE 2 SERIAL OUTPUT CONTROL SETTINGS

CONTROL WORD 19 BIT POSITION	FUNCTION	BIT VALUE	RESULT
30-28	SEROUTA Data Source	000	(I)
27-25	SEROUTB Data Source	001	(Q)
24-21	Number of Serial Word Links in a Chain	011	(3)
20-18	Link following I data	001	(Q)
17-15	Link following Q data	010	(|r|)
14-12	Link following |r| data	TBD	TBD
11-9	Link following ϕ data	XXX	(N/A)
8-6	Link following ***f*** data	XXX	(N/A)
5-3	Link following AGC data	XXX	(N/A)
2-0	Link following Timing Error data	XXX	(N/A)

The serial data stream looks like:

SEROUTA:	**CONTROL WORD 19 FIELD**
start	
I data word >	SEROUTA source data = 000
Q data word >	Link following I data = 001
|r|data word >	Link following Q data = 010
end >	

SEROUTB:	**CONTROL WORD 19 FIELD**
start	
Q data word >	SEROUTB source data = 001
|r|data word >	Link following Q data = 010
TBD data word>	Link following |r| data = TBD
end >	

As shown by this example, once Q was linked to |r| in the SEROUTA chain, the SEROUTB chain must have |r| following Q, if Q is selected. Figure 35 illustrates the construction of the serial output streams. If the serial data stream was changed to be a length of four data words, then, by default, the SEROUTA would be whatever is selected for SEROUTB data word 3. SEROUTB would need to identify the fourth data word. **Thus, SEROUTA and SEROUTB are not fully independent because they share the Q data** word (and by default, the MAGNITUDE follows Q data link and whatever is selected for data word 3 to follow MAGNITUDE data in SEROUTB).

The other signals provided with the SEROUTA and SEROUTB are the SERSYNC and the SERCLK. The SERSYNC signal can be programmed in either early or late sync mode. The sync signal is pulsed active low or active high for each information word link of the chain of data created using Control Word 19. Figure 36 shows the four possible configurations of SERSYNC as programmed using Control Word 20.

As previously discussed, Control Word 20, Bits 17 and 19, set the functionality of the LSB of each data word. These bits may be programmed to be either a logic "0", logic "1" or as normal data. The fixed states are designed to allow the microprocessor to synchronize to the serial data stream.

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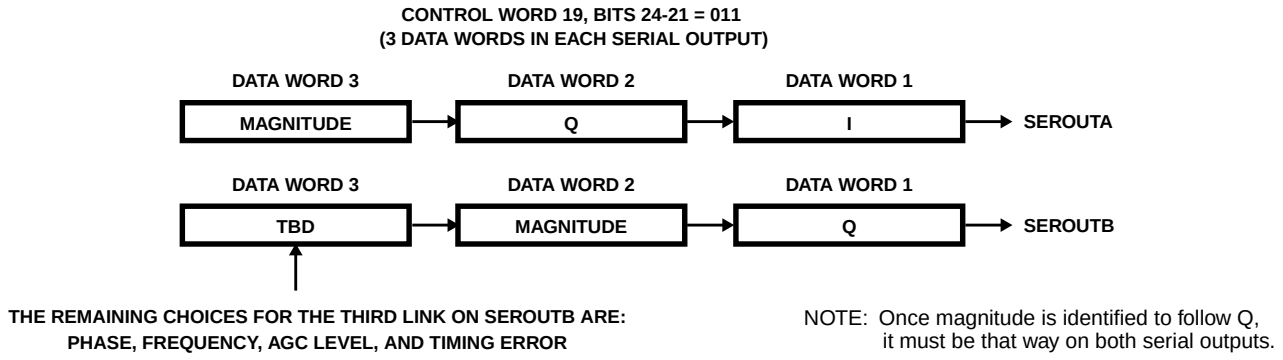


FIGURE 35. EXAMPLE 2 SERIAL OUTPUT DATA STREAM

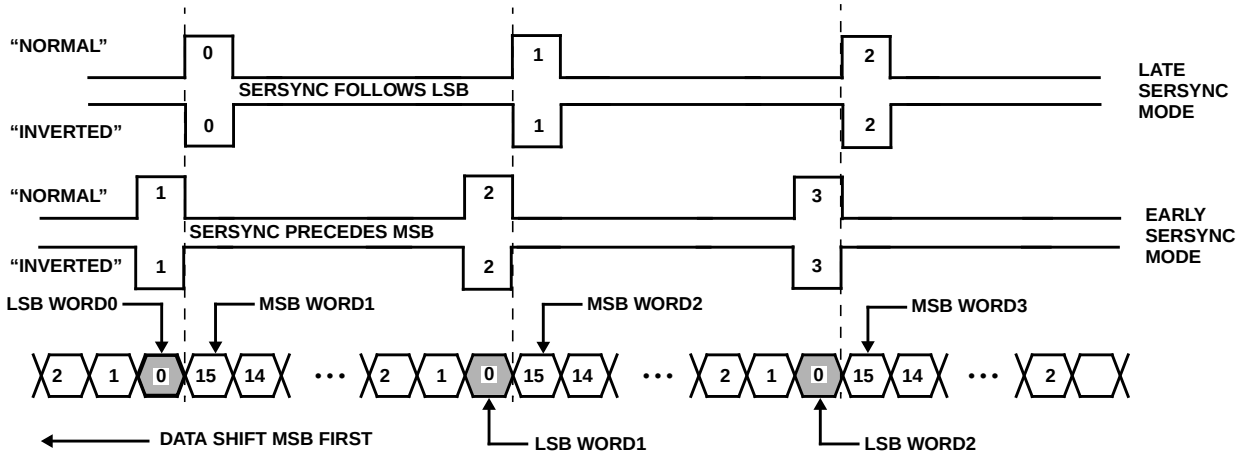


FIGURE 36. VALID SERSYNC CONFIGURATION OPTIONS

The serial direct output can be programmed to output less than 16 bits. New output data preempts old output data, so if SERSYNC is programmed to precede the MSB, then data will shift out until new data comes along. Note that if SERSYNC is programmed to follow the LSB, then a sync will never occur.

Buffer RAM Output Port

The Buffer RAM parallel output mode utilizes a RAM to store output data for future retrieval by either the 8-bit microprocessor that is configuring the PDC or by a 16-bit baseband processing engine (which could also be a microprocessor). Data is output from the RAM only on request and can be obtained from either the 8-bit µP interface or from a 16-bit interface that uses the two LSBytes of AOUT and BOUT. The RAM holds up to eight 80-bit sample sets. Each sample set includes 16 bits of each I, Q, magnitude, phase, and frequency data. The RAM samples are mapped as shown in Table 16. The Buffer RAM controller supports both FIFO and Snapshot modes.

TABLE 16. RAM DATA STORAGE MAP

RAM SAMPLE SET	I DATA (000)	Q DATA (001)	|r| DATA (010)	Φ DATA (011)	*F* DATA (100)
0	$I_0(15:0)$	$Q_0(15:0)$	$\|r\|_0(15:0)$	$\phi_0(15:0)$	$f_0(15:0)$
1	$I_1(15:0)$	$Q_1(15:0)$	$\|r\|_1(15:0)$	$\phi_1(15:0)$	$f_1(15:0)$
2	$I_2(15:0)$	$Q_2(15:0)$	$\|r\|_2(15:0)$	$\phi_2(15:0)$	$f_2(15:0)$
3	$I_3(15:0)$	$Q_3(15:0)$	$\|r\|_3(15:0)$	$\phi_3(15:0)$	$f_3(15:0)$
4	$I_4(15:0)$	$Q_4(15:0)$	$\|r\|_4(15:0)$	$\phi_4(15:0)$	$f_4(15:0)$
5	$I_5(15:0)$	$Q_5(15:0)$	$\|r\|_5(15:0)$	$\phi_5(15:0)$	$f_5(15:0)$
6	$I_6(15:0)$	$Q_6(15:0)$	$\|r\|_6(15:0)$	$\phi_6(15:0)$	$f_6(15:0)$
7	$I_7(15:0)$	$Q_7(15:0)$	$\|r\|_7(15:0)$	$\phi_7(15:0)$	$f_7(15:0)$

***NOTE:** I and Q are sample aligned in time. |r| and ϕ are sample aligned in time, but one sample delayed from I or Q. The frequency sample is delayed in time from I or Q by 1 sample time + 63 tap FIR impulse response. If the FIR is set to decimate, the FIR output will be repeated every sample time until a new value appears at the filter output. (i.e., the frequency samples are clocked out at the I, Q sample rate regardless of decimation.)*

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The FIFO mode allows the processor to service the interface only when enough samples are present in the RAM. This mode is provided so that the µProcessor does not have to service the PDC every output sample. An interrupt, $\overline{\text{INTRRPT}}$, is asserted when the desired number of samples are available. The PDC can be programmed to assert the interrupt when up to 7 samples are available. Control Word 21, Bit 15 is used to set the Buffer RAM controller to the FIFO mode, while Control Word 21, Bits 12-14 set the number of RAM samples to be stored (0 to 7) before the interrupt ($\overline{\text{INTRRPT}}$) is asserted. Control Word 20, Bit 24 determines whether the RAM output interface is the 8-bit microprocessor interface or the 16-bit processor interface. In the 16-bit interface the MSByte is sent to AOUT(7:0) while the LSByte is sent to BOUT(7:0).

The $\overline{\text{INTRRP}}$ output signal goes low for 8 PROCCLK cycles when the number of samples in the Buffer RAM (depth) reaches the programmed depth. The depth of the RAM is calculated using Equation 23. A DSP microprocessor or the data processing engine can use the $\overline{\text{INTRRP}}$ signal to know that the RAM is ready to be read.

$$D_{RAM} = [(ADDR_{WRITE} - ADDR_{READ}) - 1]_{MOD8} \quad \text{(EQ. 23)}$$

FIFO Operation via 16-Bit µProcessor Interface

Figure 37 shows the conceptual configuration of the 16-bit µProcessor interface. This interface looks like a 16-bit µProcessor read-only microprocessor interface. The SEL(2:0) lines are the address bus and the OEAL and OEBL lines are the read lines. The address is decoded as shown in Table 17.

Use of the 16-bit interface for Buffer RAM output requires Control Word 20, Bit 25, to be set to a logic “0” and Control Word 20, Bit 24, to be set to a logic “1”. Once the Control Word 20 has been set to route data to AOUT(7:0) and BOUT(7:0), then the microprocessor must place a value on the PDC input pins SEL(2:0), to choose which data type will be output on AOUT(7:0) and 6BOUT(7:0). Table 17 defines the data types in terms of SEL(2:0). With the control lines set, the selected data is read MSByte on AOUT(7:0) and LSByte on BOUT(7:0) when $\overline{\text{OEAL}}$ and $\overline{\text{OEBL}}$ (are low). New data only read when $\overline{\text{OEBL}}$ goes low, so use µP for 8-bit modes. Programming SEL(2:0) = 110 outputs a 16-bit status signal on AOUT and BOUT. The FIFO status includes FULL, EMPTY, FIFO Depth, and READYB. These status signals are defined in Table 18.

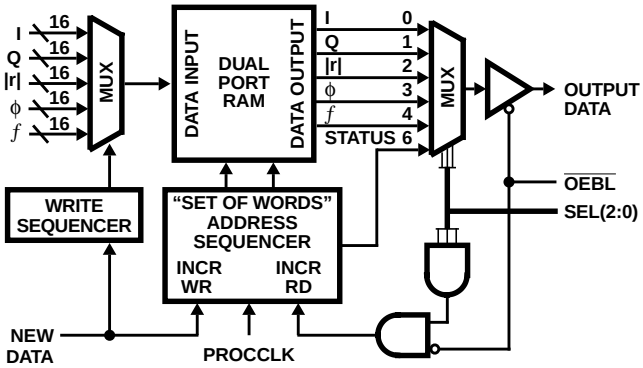


FIGURE 37. 16-BIT MICROPROCESSOR INTERFACE BUFFER RAM MODE BLOCK DIAGRAM

TABLE 17. BUFFER RAM OUTPUT SELECT DEFINITIONS

SEL(2:0)	OUTPUT DATA TYPE
000	I Data
001	Q Data
010	Magnitude
011	Phase
100	Frequency
101	Unused
110	Memory Status
111	Reading this address increments to the next sample set

TABLE 18. STATUS BIT DEFINITIONS

AOUT BIT LOCATION	INFORMATION
(7:5)	FIFO depth - When in FIFO mode, these bits are the current depth of the FIFO.
4	EMPTY - When in FIFO mode, the FIFO is empty, and the read pointer cannot be advanced. Active High.
3	FULL - When in FIFO mode, the FIFO is full, and new samples will not be written. Active High.
2	READYB - When in FIFO mode, the output buffer has reached the programmed threshold. In the snapshot mode, the programmed number of samples have been taken. Active Low.
1-0	GND

NOTE: In the Status output, BOUT(7:0) are all GND.

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Figure 38 shows the interface between a 16-bit microprocessor (or other baseband processing engine) and the Buffer RAM Output Section of the Programmable Down Converter, configured for data output via the parallel outputs AOUT and BOUT. In the 16-bit microprocessor interface configuration, the Buffer RAM pointer is incremented when the µProcessor reads address SEL(2:0) = 7 and $\overline{OEBL}$ = 0.

After reset, the FIFO must be incremented to read the first sample set. This is because the RAM read and write pointers cannot point to the same address. Thus, the FIFO pointer must move to the next address before reading the next set of data (I, Q, |r|, ϕ, and *f*) samples. 4 PROCCLK cycles are required after an increment before reading can resume. The FIFO write pointer is reset to zero (the first data sample) when Control Word 22 is written to via the 8-bit microprocessor interface. See the Microprocessor Read Section for more detail on how to obtain the Buffer RAM output with this technique. Figure 39 shows the timing diagram required for parallel output operations. In this diagram, only the I, Q and Frequency data are taken from each sample before incrementing to the next sample. Figure 39 assumes that the pointer has already been incremented into a sample.

NOTE: For the very first sample read, the pointer must be incremented first and 4 PROCCLKs must pass before this sample can be read.

Figure 39 shows $\overline{INTRRP}$ going low before the FIFO is read. The FIFO can be read before the number of samples reaches the INTRRP pointer. The number of samples in the FIFO must be monitored by the user via a status read.

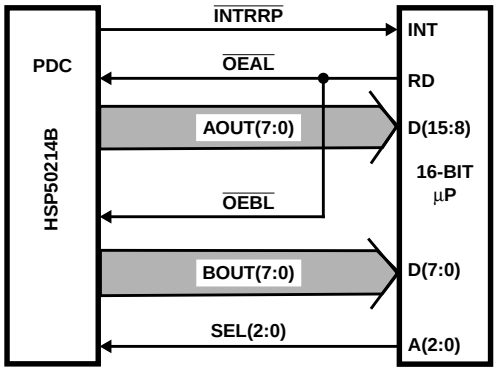


FIGURE 38. INTERFACE BETWEEN A 16-BIT MICROPROCESSOR AND PDC IN FIFO BUFFER RAM MODE

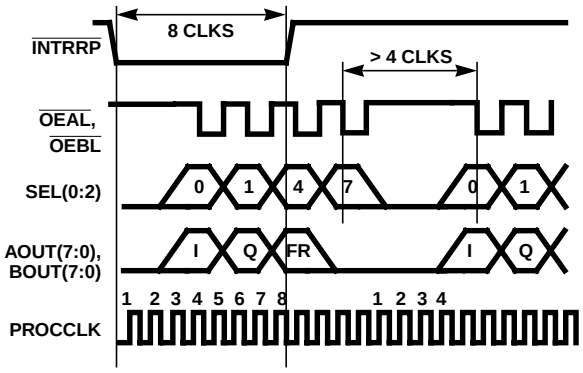


FIGURE 39. TIMING DIAGRAM FOR PDC IN FIFO MODE WITH OUTPUTS I, Q, AND FREQUENCY SENT TO AOUT(7:0) AND BOUT(7:0)

Suppose the depth of the Buffer RAM Output Section is programmed for an $\overline{INTRRP}$ pointer depth of 4. If the output is at 4 times the baud rate, the processing routine for the microprocessor may only need to read the buffer when the Buffer RAM had 4 samples since processing is usually on a baud by baud basis.

Figure 40 illustrates the conceptual view of the FIFO as a circular buffer, with the Write address one step ahead of the Read Address.

Figure 40A deals with clockwise read and write address incrementing. The FIFO depth is the difference between the Write and Read pointers, modulo 8. Figure 40B illustrates a FIFO status of Full, while Figure 40C illustrates a FIFO empty status condition. Figure 40D illustrates a programmed FIFO depth of 3 and the INTRRP signal indicating that the buffer has sufficient data to be read.

Following some simple rules for operating the FIFO will eliminate most operational errors:

Rule #1: The Read and Write Pointers cannot point at the same address (the circuitry will not allow this).

Rule #2: The FIFO is full when the Write Address = Read Address -1 (no more data will be written until some samples are read or the FIFO is reset).

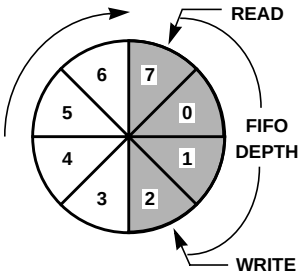
Rule #3: The FIFO is empty when the Read Address = (Write Address -1) (the circuitry will not allow the read pointer to be incremented).

Rule #4: You cannot write over what you have not read.

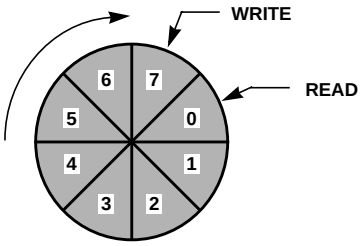
Rule #5: RESET places the Write address pointer = 000 and Read address pointer = 111.

Rule #6: The best addressing scheme is to read the FIFO until it is empty. This avoids erroneous $\overline{INTRRP}$ assertions and provides for simple FIFO depth monitoring. The interrupt is generated when the depth increments past the threshold.

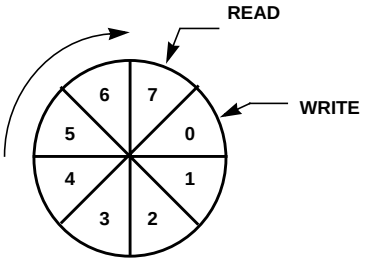
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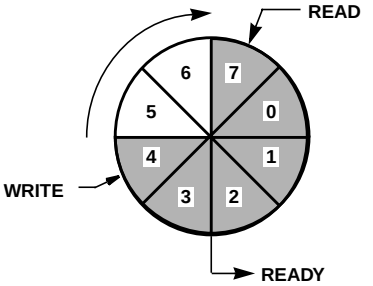
A: FIFO DEPTH IS (WRITE - READ)



B: FIFO FULL IS WHEN (WRITE - READ) = 7



C: FIFO EMPTY IS WHEN (WRITE - READ) = 1



D: FIFO READY IS WHEN (WRITE - READ) > DEPTH

FIGURE 40. FIFO REGISTER OPERATION

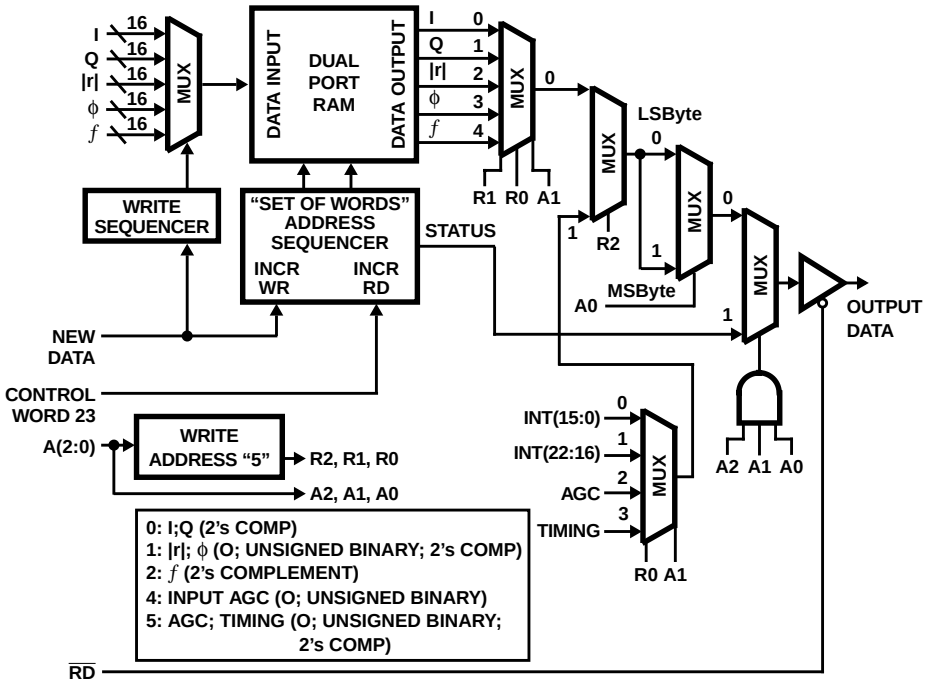
FIFO Operation via 8-Bit µProcessor Interface

The Buffer RAM Output may also be accessed via the 8-bit microprocessor interface C(7:0). Figure 41 shows the conceptual configuration of the 8-bit µprocessor interface. Control Word 20, Bit 24 must be set to 0 in order to obtain Buffer RAM data to this output. The Microprocessor Read Section describes how to read the data from each sample out of the C(7:0) interface.

Recall that $\overline{\text{INTRRP}}$ stays low for 8 PROCCLK cycles. The FIFO can be read before the INTRRP signal goes low; the number of samples in the FIFO must be monitored by the user. The timing relationship of the $\overline{\text{INTRRP}}$ to the snapshot data is shown in Figure 42.

The read pointer of the FIFO is incremented when Control Word 23 is written to. The data cannot be read from the next sample until 4 PROCCLKs after the Buffer RAM pointer has been incremented. Control Word 22 is used to reset the Read and Write pointers of the Buffer RAM output to the first sample to 000 and 007 for write and read respectively.

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R2	R1	R0	A2	A1	A0	SELECTION
0	0	0	0	0	0	RAM I LSB
0	0	0	0	0	1	RAM I MSB
0	0	0	0	1	0	RAM Q LSB
0	0	0	0	1	1	RAM Q MSB
0	0	1	0	0	0	RAM |r| LSB
0	0	1	0	0	1	RAM |r| MSB
0	0	1	0	1	0	RAM ϕ LSB
0	0	1	0	1	1	RAM ϕ MSB
0	1	0	0	0	0	RAM f LSB
0	1	0	0	0	1	RAM f MSB
0	1	1	X	X	X	NOT USED
1	0	0	0	0	0	INPUT INTEG LSB
1	0	0	0	0	1	INPUT INTEG NMSB
1	0	0	0	1	0	INPUT INTEG MSB
1	0	1	0	0	0	AGC LSB
1	0	1	0	0	1	AGC MSB
1	0	1	0	1	0	TIMING LSB
1	0	1	0	1	1	TIMING MSB
1	1	X	X	X	X	NOT USED
X	X	X	1	1	1	STATUS

FIGURE 41. 8-BIT MICROPROCESSOR INTERFACE BUFFER RAM MODE BLOCK DIAGRAM

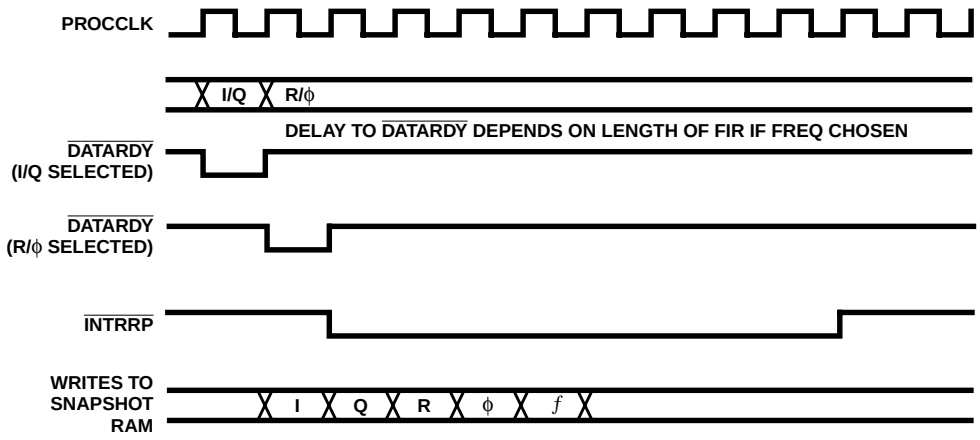


FIGURE 42. RAM LOAD SEQUENCE

Snap Shot Operation

The snapshot mode takes sets of adjacent samples at programmed intervals. It is provided for tracking algorithms that do not require processing of every sample, but do require sets of adjacent samples. For example, bit sync algorithms have narrow loop bandwidths that may not need to be updated every sample. Computing the bit phase may require 4 adjacent samples at 2 times the baud rate. The snapshot mode allows the processor to implement the tracking algorithms for high speed data without having to handle every data sample.

The interval from the start of one snapshot to the start of a second snapshot is programmed into bits 11-4 (where bit 11 is the MSB) of Control Word 21. The actual interval is the value programmed plus 1. If bits 11-4 = 11111111, then the interval is set to 256. If sample sets are to be taken every 4 samples, then bits 11-4 = 00000011.

Figure 43 shows the relationship between the snapshot samples and the snapshot interval.

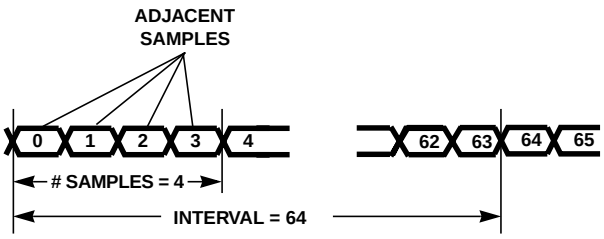


FIGURE 43. SNAP SHOT SAMPLING

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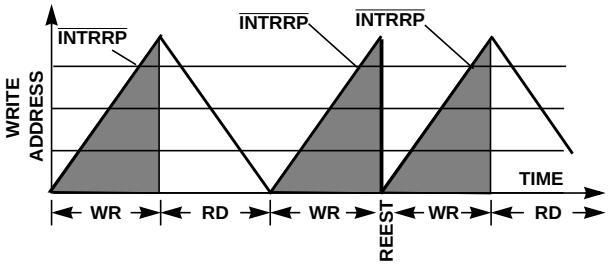
The PDC begins to fill the buffer each time an interval number of samples have passed. The number of sample sets the PDC writes into the buffer and is programmed into bits 3-0 of Control Word 21. The number of samples stored is the programmed value and may be from 1 to 8 sample sets. A sample set consists of I, Q, |r|, ϕ and f.

In snap shot operations, the buffer is read the same as for FIFO operations. Figures 37 and 39 describe the Design Blocks and Timing required to output data on AOUT(7:0) and BOUT(7:0). Table 17 summarizes the selectable output signals. The method for reading data through the Microprocessor Section in snap shot mode is identical to the method described in the FIFO mode subsection and the Microprocessor Read Section.

Avoiding Timing Pitfalls When Using the Buffer RAM Output Port

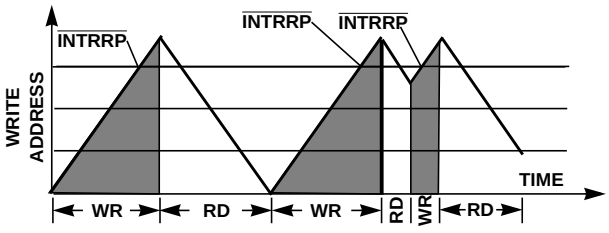
In snapshot mode, the whole buffer is written whenever the interval counter has timed-out. After time-out, old data can be written over. Thus, the data contained within the buffer must be retrieved before time-out to avoid data loss.

It may be desirable to disable the $\overline{\text{INTRRPT}}$ into the controlling microprocessor during read cycles to avoid the generating extra interrupts. Figure 44 details how the WRITE address can trigger extra interrupts. Care must be taken to either read sufficient data out of memory or RESET the addressing to ensure that a complete set of data is the cause of the interrupt.



A COMPLETE SET OF 3 DATA SAMPLES IS IN MEMORY AT $\overline{\text{INTRRP}}$

A: NORMAL READ/WRITE SEQUENCE



THE THIRD INTERRUPT HAS ONLY 1 NEW DATA ENTRY (INSTEAD OF 3) AT $\overline{\text{INTRRP}}$

B: FALSE TRIGGERED INTERRUPT READ/WRITE SEQUENCE

FIGURE 44. AVOIDING FALSE $\overline{\text{INTRRP}}$ ASSERTIONS

Microprocessor Write Section

The Microprocessor Write Section uses an indirect addressing scheme where a 32-bit data word is first loaded in a four 8-bit byte master registers using four writes via C(7:0). The desired destination register address is then written to another address using C(7:0). Writing this address triggers a circuit that generates a pulse, synchronous to clock, that loads the Destination Register. The sync circuits and data words are synchronized to different clocks, CLKIN or PROCCLK, depending on the Destination Registers.

A(2:0) determines the destination for the data on bus, C(7:0). Table 19 shows the address map for microprocessor interface. Figure 45 shows the Control Register loading sequence. The data in C(7:0) and address map in A(2:0) is loaded into the PDC on the rising edge of WR and is latched into the Master Register on the rising edge of WR and A(2:0) = 100. Four clocks must pass before loading the next Control Word to guarantee that the data has been transferred.

Some registers can be loaded (i.e., transferred from the Master Register to a Configuration Register or from a Holding Register to an active register) by initiating a sync. For example, to load the AGC Gain, the value of the AGC gain is first loaded into the Holding Registers, then a transfer is initiated by SYNCIN2 if Control Word 8, Bit 29 = 1. This allows the AGC gain to be loaded by detecting a system event, such as a start of a new burst. Bit 20 of Control Word 0 has the same effect on the Carrier NCO center frequency for assertion of SYNCIN1, except it transfers from a dedicated holding register - not the Master Register.

TABLE 19. DEFINITION OF ADDRESS MAP

A2-0	REGISTER DESCRIPTION
0	Holding Register 0. Transfers to bits 7-0 of the 32-bit Destination Register. Bit 0 is the LSB of the 32-bit register.
1	Holding Register 1. Transfers to bits 15-8 of a 32-bit Destination Register.
2	Holding Register 2. Transfers to bits 23-16 of a 32-bit Destination Register.
3	Holding Register 3. Transfers to bits 31-24 of a 32-bit Destination Register. Bit 31 is the MSB of the 32-bit register.
4	This is the Destination Address Register. On the fourth CLK following a write to this register, the contents of the Holding Registers are transferred to the Destination Register. All 8 bits written to this register are decoded into the Destination Register Address. The configuration destination address map is given in the tables in the Control Word Section.
5	Selects data source for reading. See Microprocessor Read Section.

Suppose a (0018D038)H needs to be loaded into Control Word 0, then Table 20 details the steps to be taken.

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TABLE 20. EXAMPLE PROCESSOR WRITE SEQUENCE

STEP	A(2:0)	C(7:0)	COMMENT
1	000	0011 1000	Loads 38 into Master Register (7:0) on rising edge of $\overline{WR}$.
2	001	1101 0000	Loads D0 into Master Register (15:8) on rising edge of $\overline{WR}$.
3	010	0001 1000	Loads 18 into Master Register (23:16) on rising edge of $\overline{WR}$.
4	011	0000 0000	Loads 00 into Master Register (31:24) on rising edge of $\overline{WR}$.
5	100	0000 0000	Load “0018D038” into Configuration Control Register 0.
6			Wait 4 CLKS.

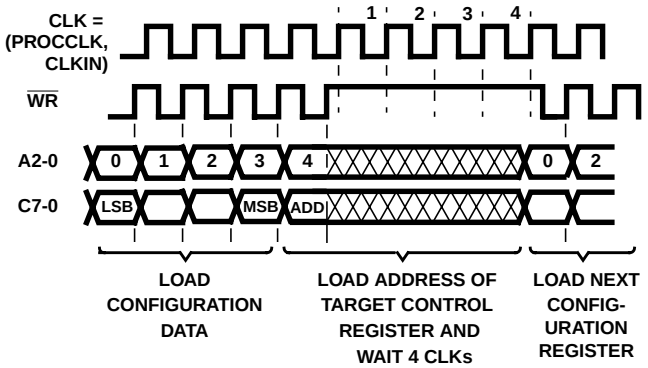


FIGURE 45. LOADING THE CONTROL REGISTERS WITH 32-BIT CONTROL WORDS

Microprocessor Read Section

The microprocessor read uses both read and write procedures to obtain data from the PDC. A write must be done to location 5 to select the source of data to be read. The read source is determined by the value placed on the lower three bits of C(7:0). The output from a particular read code is selected using a read address placed on A(2:0). The output is sent to C(7:0) on the falling edge of $\overline{RD}$.

If the Read Address is equal to 111, the Read Code is ignored, and the status bits shown in Table 22 in the Output Section is sent to C(7:0). This state was provided so that the user could obtain the status bits quickly.

Refer to the Timing Diagram in Figure 46. Suppose the input level detector has a hex value of (321AF5)H, then Table 21 details the steps to be taken.

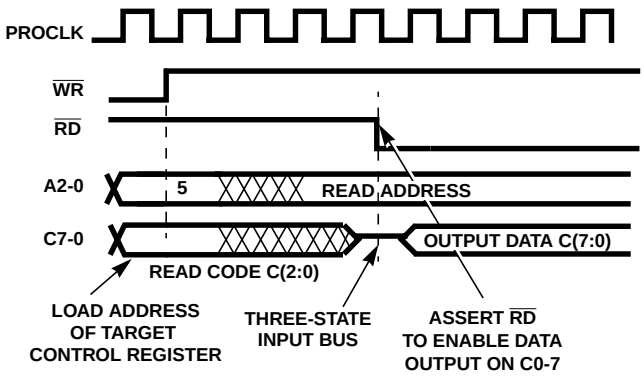


FIGURE 46. READING THE CONTROL REGISTERS USING A LATCH CODE EQUAL TO A 5, A READ ADDRESS AND A READ CODE

TABLE 21. PROCESSOR READ SEQUENCE (INPUT LEVEL SELECTOR)

STEP	A(2:0)	C(7:0)	COMMENT
1	101	100	Write Read Code, 100 to Address 5, $\overline{WR}$ pulled high to generate rising edge.
2	000	1111 1000 (F4)H	Drop $\overline{RD}$ low, Read AGC LSB.
3	001	0001 1010 (1A)H	Pull $\overline{RD}$ high, then drop low, Read AGC NLSB.
4	010	0011 0010 (32)H	Pull $\overline{RD}$ high, then drop low, Read AGC MSB.

TABLE 22. DEFINITION OF ADDRESS MAP

READ CODE C(2:0)	STATUS TYPE	READ ADDRESS A(2:0)
000	Buffer RAM I and Q	000- I LSB. 001- I MSB. 010- Q LSB. 011- Q MSB. See Output Section.
001	Buffer RAM Output (|r| and ϕ)	000- MAG LSB (7-0). 001- MAG MSB (15-8). 010- PHASE LSB (7-0). 011- PHASE MSB (15-8). See Output Section.
010	Buffered Frequency	000- FREQ LSB. 001- FREQ MSB. See Output Section.
011	Not Used	
100	Input Level Detector	Input AGC 000- input AGC LSB (0-7). 001- input AGC NLSB (8-15). 010- input AGC MSB (16-23).

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TABLE 22. DEFINITION OF ADDRESS MAP (Continued)

READ CODE C(2:0)	STATUS TYPE	READ ADDRESS A(2:0)
101	AGC Data and Timing Error	AGC (must write to location 10 to sample) 000- AGC LSB (lower 8 bits of linear Control Word 3 used by multiplier) mmmmmmmm LSB. 001- AGC MSB (4 shift control bits and first three bits of linear) Control Word oeeeemmm MSB. This yields 11 bits of the linear control mantissa. 010- Timing error LSB, not stabilized. 011- Timing error MSB, not stabilized.
110	Not Used	
111	Not Used	
Don't Care	Status	111- Status (6:0) consisting of (6:4)-FIFO depth when output is in FIFO Buffer RAM Output Mode. (3)-EMPTY signalling the FIFO is empty and the read pointer cannot be advanced (Active High). (2)-FULL signalling the FIFO is full and new samples will not be written (Active High). (1)-READYB Output buffer has reached the programmed threshold in FIFO mode or the programmed number of samples have been taken in snapshot mode. (Active Low). (0)-INTEGRATION has been completed in the input level detector and is ready to be read. (Active High).

Applications

Composite Filter Response Example

For this example consider a total receive band roughly 25MHz wide containing 124 200kHz wide FDM channels as shown in Figure 47. The design goal for the PDC is to tune to and filter out a single 200kHz FDM channel from the FDM band, passing only baseband samples onto the baseband processor at a multiple of the 270.8 KBPS bit rate.

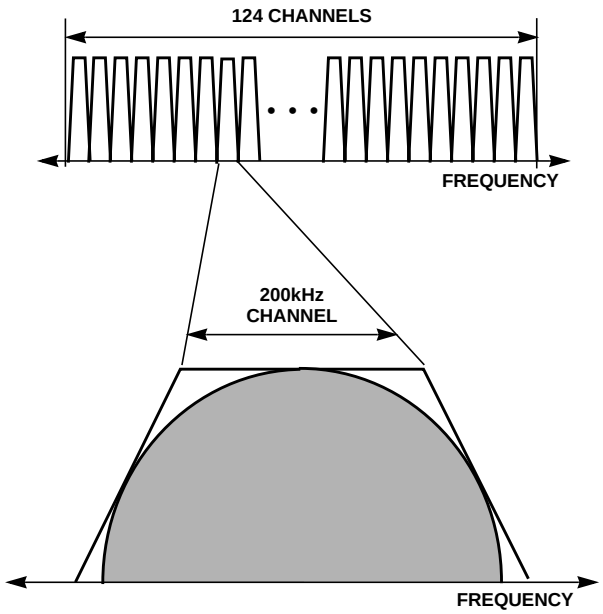


FIGURE 47. RECEIVE SIGNAL FREQUENCY SPECTRUM

RF/IF Considerations

The input frequency to the PDC is dependent on the A/D converter selected, the RF/IF frequency, the bandwidth of interest and the sample rate of the converter. If the A/D converter has sufficient bandwidth, then undersampling techniques can be used to downconvert IF/RF frequencies as part of the digitizing process, using the PDC to process a lower frequency alias of the input signal.

For example, a 70MHz IF can be sampled at 40MHz and the resulting 10MHz signal alias can be processed by the PDC to perform the desired downconversion/tuning and filtering. If the IF signal is less than 1/2 the sample frequency then standard oversampling techniques can be used to process the signal. Of the two techniques, only undersampling allows part of the down conversion function to be brought into the digital domain just through sampling, assuming that a sampling frequency can be found that keeps the alias signals low and that the A/D converter has the bandwidth to accept the unconverted analog signal.

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PDC Configuration

For this example, the PDC is configured as follows:

CLKIN: 39MHz
Mode: . . . . . .Gated
Input Format: . . . . . As required by Digital Source
Carrier NCO Fc: . . . . . .As determined by Channel Freq.
Carrier NCO Phase Offset: 0
Carrier NCO Offset Frequency: . . . . . .Disabled
CIC Filter: . . . . . Enabled
Decimation: 18
PROCCLK:. 28MHz
Half Band Filters: . . . . . HB3 and 5 Enabled
FIR Filter: . . . . . gsmtemp file
. . . . . f_S = 541.667kHz
. . . . . .Decimation = 1
. . . . . .Passband: 90kHz
. . . . . Transition Band: 25kHz
. . . . . .Passband Atten: 3dB
. . . . . Stop Band Atten: 111.25713
. . . . . .FIR Order: 90
. . . . . FIR Symmetry: Even
Resampling Filter: . . . . . HB1 Enabled

The basis for this configuration is:

Sampling Rate: Select a high rate PROCCLK

Output Rate: 1.083MHz (4x Bit Rate; 8x Baud Rate)

CIC Filtering: Primarily Rate Reduction (39/18 = 2.166MHz).

HB Filtering: Flat passband with rate reduction by 4 - low enough (541.66kHz) for sufficient FIR Taps to be used.

FIR Filtering: Primary shaping filter/set final out of band suppression.

Polyphase/HalfBand Filtering: Interpolate by two to output 8x baud rate or 4x bit rate.

The CIC and halfband filter responses are shown in Figures 48A and B.

The composite filter response constrained primarily by halfband filter 5 and the FIR filter, are shown in Figure 49A-C.

For a more detailed discussion of design approaches and trades when designing with the PDC, refer to AN9720 [3], “Calculating the Maximum Processing Rates of the PDC”.

References

For Intersil documents available on the web, see http://www.intersil.com/
Intersil AnswerFAX (321) 724-7800.

[1] *HSP50210 Data Sheet,* Intersil Corporation, AnswerFAX Doc. No. 3652.

[2] *Cellular Radio and Personal Communications: A Book of Selected Readings*, Theodore S. Rappaport, 1995 by IEEE, Inc.

[3] *AN9720 Application Note,* Intersil Corporation, “Calculating Maximum Processing Rates of the PDC (HSP50214B)”, AnswerFAX Doc. No. 99720.

[4] FO-007 Block Diagram of HSP50214.

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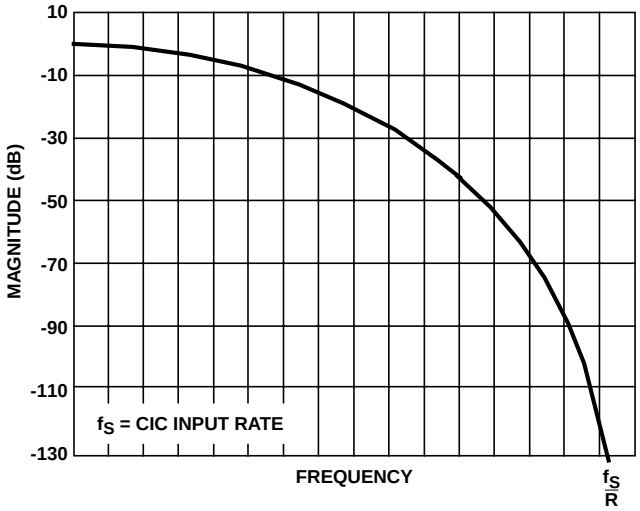


FIGURE 48A. CIC FILTER RESPONSE

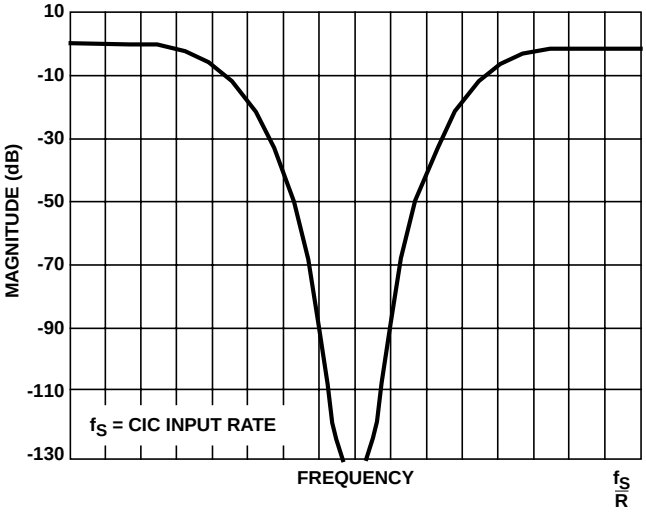


FIGURE 48B. HB3 FILTER RESPONSE

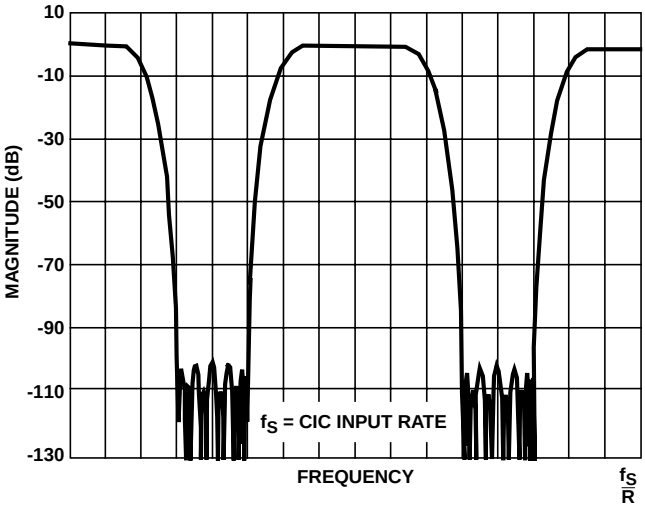


FIGURE 49A. HB5 FILTER RESPONSE

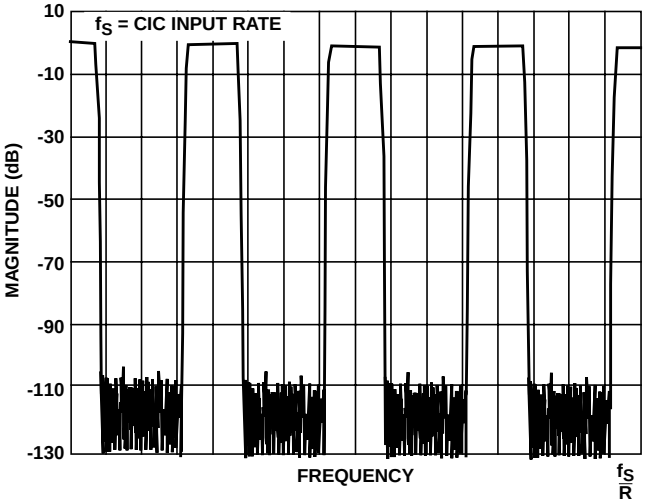


FIGURE 49B. 255 FIR TAP FILTER RESPONSE

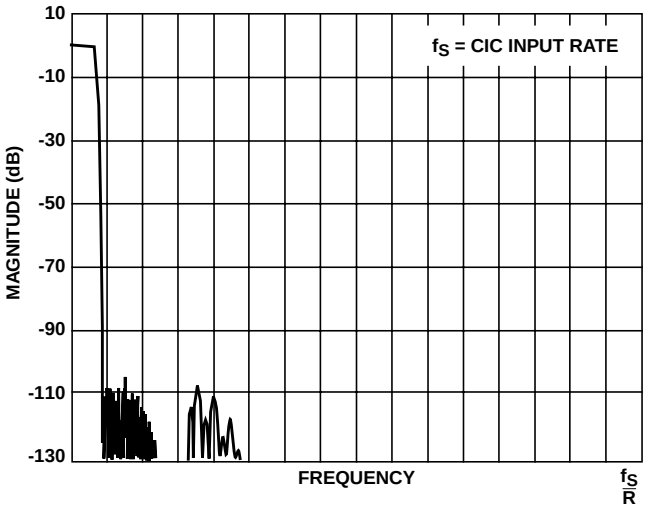


FIGURE 49C. COMPOSITE FILTER RESPONSE

FIGURE 49D. PDC FILTER FREQUENCY SPECTRUMS EXAMPLE (NORMALIZED TO SAME SCALE)

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Configuration Control Word Definitions

Note that in the Configuration Control Register Tables, some of the available 32 bits in a Control Word are not used. Unused bits do not need to be written to the Master Register. If the destination only has 16 bits, then only 2 bytes need to be written to the Master Register. Figure 45 details the timing for proper operation of the Microprocessor Write Section. Bits identified as “Reserved” should be programmed to a zero.

NOTE: CLKIN or PROCCLK must be present to properly load control words. Note in the header which is applicable.

CONTROL WORD 0: CHIP CONFIGURATION, INPUT SECTION, CIC GAIN (SYNCHRONOUS TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-21	Reserved	Reserved.
20	Carrier NCO External Sync Enable	0- The SYNCIN1 pin has no effect on the Carrier NCO. 1- When the SYNCIN1 pin is asserted, the carrier center frequency and phase are updated from the holding registers to the active register. Also, if bit 0 of this word is active, the carrier phase accumulator feedback will be zeroed to set the Carrier NCO to a known phase, allowing the NCOs of multiple parts to be initialized and updated synchronously.
19	CIC External Sync Enable	0- The SYNCIN1 pin has no effect on the CIC filter. 1- When the SYNCIN1 pin is asserted, the decimation counter is loaded, allowing the decimation counters in multiple chips to be synchronized. When CW27 bit-22 is set to a 1, SYNCIN1 will reset both front end and back end circuitry.
18	Input Format	0- Two’s Complement Input Format. 1- Offset Binary Input Format.
17	Input Mode	0- Input operates in Gated Mode. 1- Input operates in Interpolated Mode.
16-13	CIC Shift Gain	These bits control the barrel shifter at the input to the CIC filter. These bits are added to the GAINADJ(2:0) pins to determine the total shift. The sum is saturated at 15. See the CIC Decimation Filter Section for values to be programmed in this field based on CIC filter Decimation. Bit 16 is the MSB. SG = Floor [39 - (number of input bits) - $5\log_2(R)$] for 4 < R < 31 SG = 15 for R = 4. SG = 0 for R = 32.
12-7	CIC Decimation Counter Preload	These bits control the decimation in the CIC filter. Program this field to R-1, where R is the desired decimation factor in the filter. The decimation factor range is 4-32. See CIC Filter Section for effective decimation range relative to the CIC Shift Gain value. Bit 12 is the MSB. While this field allows values from 0 - 63, the valid values are in the range from 4- 32.
6	CIC Bypassed	Active high, this bit routes the output of the input shifter to the output of the CIC with no filtering. When the CIC filter is bypassed, CLKIN must be at least twice the input sample rate (ENI should be toggled to achieve this). When the CIC filter is bypassed, the bottom 24 bits of the barrel shifter output are routed to the halfband filters.
5-4	Number of Offset Frequency Bits	00 - 8 bits. 01 - 16. 10 - 24. 11 - 32.
3	Syncout CLK Select	This bit selects whether the SYNCOUT signal is generated from CLKIN of from PROCCLK 0- CLKIN. 1- PROCLK.
2	Clear Phase Accum	0- Enable accumulator in Carrier NCO. 1- Zero feedback in accumulator.
1	Carrier NCO Offset Frequency Enable	When set to 1, this bit enables the offset frequency word to be added to the center frequency Control Word. The offset is loaded serially via the COF and COFSYNC pins.
0	Carrier NCO Load Phase Accum On Update	When this bit is set to 1, the µP update to the Carrier NCO frequency or an external carrier NCO load using SYNCIN1 will zero the feedback of the phase accumulator, as well as update the phase or frequency. This function can be used to set the NCO to a known phase synchronized to an external event.

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CONTROL WORD 1: INPUT LEVEL DETECTOR (SYNCHRONOUS TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31	Reserved	Reserved.
30	Integration Mode	0- Integration of magnitude error stops when the interval counter times out. 1- Integration runs continuously. When the interval counter times out, the integrator reloads, and the results of the integration is sent to a register for the processor to read.
29-14	Integration Interval	These are the top 16 bits of the 18-bit integration counter, ICPrel. ICPrel = (N)/4+1; where N is the desired integration period in CLKIN cycles, defined as the number of input samples to be integrated. N must be a multiple of 4: [0, 4, 8, 12, 16.... , 2^{18}]. Bit 29 is the MSB. If the input is interpolated, then the zeros must be accounted for, as they will be added to the threshold! If the gated input mode is used, the same input sample will be accumulated multiple times.
13-0	Input Threshold	Input Magnitude Threshold. Bits 12-0 correspond to input bits 12-0. The magnitude of the input is added to this threshold, where the threshold is a signed number. Bit 13 is the MSB.

CONTROL WORD 2: INPUT LEVEL DETECTOR START STROBE (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Start Input Level Detector AGC Integrator	Writing to this location starts/restarts the input AGC error integrator. The integrator will either restart or stop when the integration interval counter times out depending on bit 30 of Control Register 1 (see Microprocessor Write Section).

CONTROL WORD 3: CARRIER NCO CENTER FREQUENCY (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-0	Carrier Center Frequency	These bits control the frequency of the Carrier NCO. The frequency range of the NCO is $\pm f_S/2$ where f_S is the input sample rate. The bits are computed by the equation $N = (F_{NCO} / f_S)*2^{32}$. Bit 31 is the MSB. This location is a holding register. After loading, a transfer to the active register is done by writing to Control Word 5 or by generating a SYNCIN1 with Control Word 0, Bit 20 set to 1. The Carrier NCO only updates $\overline{ENI}$ is active.

NOTE: In the HSP50214B, if the SYNCIN1 occurs when the NCO is not updating, the load signal is held internal to the part until the next NCO update.

CONTROL WORD 4: CARRIER PHASE OFFSET (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-10	Reserved	Reserved.
9-0	Carrier Phase Offset	These bits, PO, are used to offset the phase of the carrier NCO. The bits are computed by the Equation $PO = INT[(2^{10}\phi_{off})/ 2\pi]_{HEX}$; $(-\pi < \phi_{off} < \pi)$ for 10-bit 2's complement representation or from 0 to 2π for 10-bit offset binary representation. Bit 9 is the MSB. This location is a holding register. After loading, a transfer to the active register is done by writing to Control Word 6 or by generating a SYNCIN1 with Control Word 0, Bit 20 set to 1. The carrier NCO only updates when $\overline{ENI}$ is active.

CONTROL WORD 5: CARRIER FREQUENCY STROBE (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Carrier Frequency Strobe	Writing to this address updates the carrier frequency Control Word from the Holding Register.

CONTROL WORD 6: CARRIER PHASE STROBE (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Carrier Phase Strobe	Writing to this address updates the carrier phase offset Control Word with the value written to the phase offset (PO) register.

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CONTROL WORD 7: HB, FIR CONFIGURATION (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-22	Reserved	Reserved.
21	Enable External Filter Sync	0- The SYNCIN2 pin has no effect on the halfband and FIR filters. 1- When the SYNCIN2 pin is asserted, the filter control circuitry in the halfband filters, the FIR, the resampler, and the discriminator are reset. SYNCIN2 can be used to synchronize the computations of the filters in multiple parts for the alignment (see Synchronization Section).
20	Halfband (HB) Bypass	1- Bypass Halfband Filters. 0- Enable HB Filters (at least one HB must be enabled).
19	HB5 Enable	0- Disables HB number 5 (the last in the cascade). 1- Enables HB filter number 5.
18	HB4 Enable	Setting this bit enables HB filter number 4.
17	HB3 Enable	Setting this bit enables HB filter number 3.
16	HB2 Enable	Setting this bit enables HB filter number 2.
15	HB1 Enable	Setting this bit enables HB filter number 1.
14-11	FIR Decimation	Load decimation from 1-16, where 0000 = 16. Bit 14 is the MSB. 0001 - 1 1001 - 9 0010 - 2 1010 - 10 0011 - 3 1011 - 11 0100 - 4 1100 - 12 0101 - 5 1101 - 13 0110 - 6 1110 - 14 0111 - 7 1111 - 15 1000 - 8 0000 - 16
10	FIR Real/Complex	0- Complex Filter. 1- Dual Real Filters.
9	FIR Sym Type	0- Odd Symmetry. 1- Even Symmetry.
8	FIR Symmetry	0- Symmetric Filters. 1- Asymmetric Filters.
7-0	FIR Taps	Number of taps in the FIR filter. Range is 1 to 255, where 0000000 is invalid.

CONTROL WORD 8: AGC CONFIGURATION 1 (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-30	Reserved	Reserved.
29	Sync AGC Updates to SYNCIN2	When this bit is 1, the SYNCIN2 pin loads the contents of the master registers into the AGC accumulator.
28-16	Threshold	The magnitude measurement out of the cartesian to polar converter is subtracted from this value to get the gain error. A gain of 1.647 in the cartesian to polar conversion that must be taken into account when computing this threshold. These bits are weighted -2^{2} down to 2^{-10}. Bit 28 is the MSB.
15-12	Loop Gain 1 Mantissa	Selected when AGCGNSEL = 1. These bits, MMMM, together with the exponent bits, EEEE (11-8), set the loop gain for the AGC loop. The gain adjustment per output sample is: 1.5dB (Threshold -[Magnitude * 1.6]) $0.MMMM * 2^{-(15 - EEEE)}$ where magnitude ranges from 0 to 1.414 and the threshold is programmed in bits 28-16. The decimal value for the mantissa is calculated as DEC(MMMM)/16. Bit 15 is the MSB.
11-8	Loop Gain 1 Exponent	Selected when AGCGNSEL = 1. These bits are EEEE. See description of bits 15-12. Bit 11 is the MSB.
7-4	Loop Gain 0 Mantissa	Selected when AGCGNSEL = 0. These bits are MMMM. See description for bits 15-12. Same equations are used for Loop 0. Bit 7 is the MSB.
3-0	Loop Gain 0 Exponent	Selected when AGCGNSEL = 0. These bits are EEEE. See description for bits 15-12. Same equations are used for Loop 0. Bit 3 is the MSB.

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CONTROL WORD 9: AGC CONFIGURATION 2 (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-28	Reserved	Reserved.
27-16	Upper Limit	Maximum Gain/Minimum Signal. The upper four bits are used for exponent; the remaining bits form the mantissa in the fractional offset binary: [eeeemmmmmmmm]. See the AGC Section for details. Bit 27 is the MSB. The gain is in dB. G = (6.02)(eeee) + $20\log_{10}(1.0 + 0.mmmmmmmm)$ eeee = Floor $[\log_2(10^{GAIN\ dB/20})]$ mmmmmmmm = Floor $[256(10^{GAIN\ dB/20}/2^{eeee} - 1)]$
15-12	Reserved	Reserved.
11-0	Lower Limit	Minimum Gain/Maximum Signal. The upper four bits are used for exponent; the remaining bits form the mantissa in the fractional offset binary: [eeeemmmmmmmm]. See the AGC Section for details. Bit 11 is the MSB. The gain is in dB. G = (6.02)(eeee) + $20\log_{10}(1.0 + 0.mmmmmmmm)$ eeee = Floor $[\log_2(10^{GAIN\ dB/20})]$ mmmmmmmm = Floor $[256(10^{GAIN\ dB/20}/2^{eeee} - 1)]$

CONTROL WORD 10: AGC SAMPLE GAIN CONTROL STROBE (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Sample AGC Gain Level	Writing to this location samples the output of the AGC loop filter to stabilize the value for µP reading.

CONTROL WORD 11: TIMING NCO CONFIGURATION (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-6	Reserved	Reserved.
5	Enable External Timing NCO Sync	0- SYNCIN2 has no effect on the timing NCO. 1- When SYNCIN2 is asserted, the timing NCO center frequency and phase are updated with the value loaded in their holding registers. If bit 0 of this word is set to 1, the phase accumulator feedback is also zeroed.
4-3	Number of Offset Frequency Bits	00 - 8 bits. 01 - 16. 10 - 24. 11 - 32.
2	Enable Offset Frequency	0- Zero Offset Frequency to Adder. 1- Enable Offset Frequency.
1	Clear Phase Accumulator	0- Enable Accumulator. 1- Zero Feedback in Accumulator.
0	Timing NCO Phase Accumulator Load On Update	When this bit is set to 1, the µP update to the timing NCO frequency or an external timing NCO load using SYNCIN2 will zero the feedback of the phase accumulator as well as update the phase and frequency. This function can be used to set the NCO to a known phase synchronized to an external event.

CONTROL WORD 12: TIMING NCO CENTER FREQUENCY (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-0	Timing NCO Center Frequency	These bits control the frequency of the timing NCO. The frequency range of the NCO is from 0 to F_{RESAMP} where F_{RESAMP} is the input sample rate to the resampling filter. The bits are computed by the equation: $N = (f_{OUT}/F_{RESAMP}) * 2^{32}$. Bit 31 is the MSB. This location is a holding register. After loading, a transfer to the Active Register is done by writing to Control Word 14 or by generating a SYNCIN2 with Control Word 11, Bit 5 set to 1.

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CONTROL WORD 13: TIMING PHASE OFFSET (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-8	Reserved	Reserved.
7-0	Timing NCO Phase Offset	These bits are used to offset the phase of the Timing NCO. The range is 0 to 1 times the resampler input period interpreted either as ± T/2 (2's complement) or 0 to T (offset binary). Bit 7 is the MSB. This location is a holding register. After loading, a transfer to the Active Register is done by writing to Control Word 15 or by generating a SYNCIN2 with Control Word 11, Bit 5 set to 1.

CONTROL WORD 14: TIMING FREQUENCY STROBE (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Timing Frequency Strobe	Writing to this address updates the active timing NCO Frequency Register in the timing NCO (see Timing NCO Section).

CONTROL WORD 15: TIMING PHASE STROBE (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Timing Phase Strobe	Writing to this address updates the active timing NCO Phase Offset Register in the timing NCO (see Timing NCO Section).

CONTROL WORD 16: RESAMPLING FILTER CONTROL (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-12	Reserved	Reserved.
11-4	Re-Sampler Output Pulse Delay	NOTE: These bits program the delay between output samples when interpolating. The extra outputs can be delayed from 2 to 255 clocks from the first output. A delay of 2 equals 255 clocks of delay. A delay of 0 or 1 is an invalid mode. When interpolating by 2, one extra output is generated; when interpolating by 4, 3 extra outputs are generated. Program by the equation (PROCCLK/f_{OUT}) - 1. Bit 11 is the MSB. ***NOTE: If less than 5 is programmed, there will not be sufficient time to fully update the output buffer. If less than 16 is programmed, the serial output may be preempted. This means that it won't finish and if the sync is programmed to follow the data, there may never be a sync.***
3	Re-Sampler Bypass	0- Resampling Filter Enabled. A valid combination of bits 2-0 must also be selected. 1- Resampling Filter Section (including Interpolation halfband filters) is bypassed.
2-0	Filter Mode Select; 2- HB2 Enabled 1- HB1 Enabled 0- Re-Sampler Enabled	000- Not Valid. 001- Re-Sampler Enabled. 010- Halfband 1 Enabled. 011- Re-Sampler and Halfband Filter 1 Enabled. 100- Not Valid. 101- Not Valid. 110- Both Halfband Filters Enabled. 111- Re-Sampler and Both Halfband Filters Enabled.

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CONTROL WORD 17: DISCRIMINATOR FILTER CONTROL, DISCRIMINATOR DELAY (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-17	Reserved	Reserved.
16-15	Phase Multiplier	These bits program allow the phase output of the cartesian to polar converter to be multiplied by 1, 2, 4, or 8 (modulo 2π) to remove phase modulation before the frequency is measured. 00- No Shift on Phase Input to frequency discriminator. 01- Shift Phase Input to frequency discriminator up 1 (one bit), discarding the MSB and zero filling the LSB. 10- Shift Phase Input to frequency discriminator up 2 (two) bits, discarding the MSB and zero filling the LSB. 11- Shift Phase Input to frequency discriminator up 3 (three) bits, discarding the MSB and zero filling the LSB.
14	Discriminator Enable	0- Disable Discriminator. 1- Enable Discriminator.
13-11	Discriminator FIR Decimation	The decimation can be programmed from 1 to 8, where 000 = decimate by 8; 001 = decimate by 1; 010 = decimate by 2; 011 = decimate by 3; 100 = decimate by 4; 101 = decimate by 5; 110 = decimate by 6; and 111 - decimate by 7.
10	FIR Symmetry Type	0- Odd Symmetry. 1- Even Symmetry.
9	FIR Symmetry	0- Symmetric. 1- Asymmetric.
8-3	Number of FIR Taps	Number of FIR taps from 1 to 63, where 00000 is not valid (00001 = 1 tap, 00010 = 2 taps, etc. up to 11111 = 63 taps). Bit 8 is the MSB.
2-0	Discriminator Delay	Sets the number of delays from 1 to 8 in the discriminator. Set delay ddd to delay minus 1, where 000 represents 1 delay; 001 represents 2 delays, 010 represents 3 delays, 011 represents 4 delays, 100 represents 5 delays, 101 represents 6 delays, 110 represents 7 delays, and 111 represents 8 delays. If ddd the decimal representation bits 2-0, then the discriminator a transfer function $H(Z) = 1\text{-}Z^{-(ddd + 1)}$.

CONTROL WORD 18: TIMING ERROR PRELOADS (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-28	Reserved	Reserved.
27-16	NCO Divide	The Re-Sampler NCO output is divided down by the value loaded into this register plus 1. Load with a value that is one less than the desired period. Bit 27 is the MSB.
11-0	Reference Divide	The reference clock is divided down by the value loaded into this register plus 1. Load with a value that is one less than the desired period. Bit 27 is the MSB. A minimum preload of “I” is required.

CONTROL WORD 19: SERIAL OUTPUT ORDER (SYNCHRONIZED TO PROCCLK)

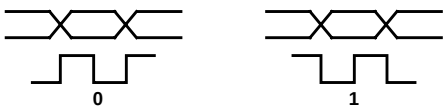
BIT POSITION	FUNCTION	DESCRIPTION
31	Reserved	Reserved.
30-28	Data Source for SEROUTA	Serial Output A Source. The serial data source is selected using Table 12 (see Output Section).
27-25	Data Source for SEROUTB	Serial Output B Source. The serial data source is selected using Table 12 (see Output Section).
24-21	Number of Serial Word Links in a Chain	This parameter determines the number of SERSYNC pulses generated. It can be set from 1 to 7. If this parameter matches the number of serial words that are linked together to form a serial output chain, then there will be a sync pulse for every word in the serial output. In applications where a processor is receiving the serial data, it may be desirable to have a single SERSYNC pulse for the whole serial output chain, instead of a SERSYNC for each word in the data chain. The processor then parses out the various data words. As an example, if the I and Q are chained together and a single SERSYNC pulse is generated for this serial output chain, no ambiguity exists in the processor about which two data samples (one from I and one from Q) are related.
20-18	Link Following I Data	The serial data word, or link, following the I data word is selected using Table 12 (see Output Section).

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CONTROL WORD 19: SERIAL OUTPUT ORDER (SYNCHRONIZED TO PROCCLK) (CONTINUED)

BIT POSITION	FUNCTION	DESCRIPTION
17-15	Link Following Q Data	The serial data word, or link, following the Q data word is selected using Table 12 (see Output Section).
14-12	Link Following Magnitude Data	The serial data word, or link, following the MAG data word is selected using Table 12 (see Output Section).
11-9	Link Following Phase Data	The serial data word, or link, following the PHAS data word is selected using Table 12 (see Output Section).
8-6	Link Following Frequency Data	The serial data word, or link, following the FREQ data word is selected using Table 12 (see Output Section).
5-3	Link Following AGC Level Data	The serial data word, or link, following the AGC data word is selected using Table 12 (see Output Section).
2-0	Link Following Timing Error Data	The serial data word, or link, following the TIMER data word is selected using Table 12 (see Output Section).

CONTROL WORD 20: BUFFER RAM, DIRECT PARALLEL, AND DIRECT SERIAL OUTPUT CONFIGURATION (SYNCHRONIZED WITH PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-26	Reserved	Reserved.
25	Data Source for Least Significant Bytes of AOUT and BOUT	Output LSBytes, bits (7:0), of AOUT and BOUT can provide: 0- Buffer RAM Mode Output or, 1- Parallel Direct Mode Output.
24	Buffered Output Mode Interface	Buffered Mode Output interfaces to either: 0- 8-bit µP (address = µP ASEL(5:#); CLK = µP RAM read). 1- 16-bit µP (address = SEL(2:0); CLK = $\overline{\text{OEBL}}$).
23-22	AOUT Direct Parallel Output Mode Data Source	The data word sent by the Direct Parallel Output Mode to AOUT is: 00- I Data. (2's complement) 01- Magnitude. (O; unsigned binary) 1X- Frequency. (2's complement)
21-20	BOUT Direct Parallel Output Mode Data Source	The data word sent by the Direct Parallel Output Mode to BOUT is: 00- Q Data (2's complement). 01- Phase (2's complement). 1X- Magnitude (O; unsigned binary).
19	Serial Output Sync Polarity	0- Normal Sync Mode (active high). 1- Sync Inverted (active low).
18	Serial Output Clock Polarity	0- Output Clock Inverted rising edge aligns with data transitions. 1- Output Clock Normal falling edge aligns with data transitions.  0 1
17	Serial Output Sync Position	0- Sync is asserted one bit time after the last bit of the serial word (Late Mode). 1- Sync is asserted one bit time prior to the first bit of the serial word (Early Mode).
16-14	Serial Out Clock Divider	000- Serial Output at PROCCLK/16. 001- Serial Output at PROCCLK/8. 010- Serial Output at PROCCLK/4. 011- Serial Output at PROCCLK/2. 1XX- Serial Output at PROCCLK rate.
13-12	I Data Serial Output Tag Bit	00- No Tag Bit. LSB of word is passed. 01- 0 Tag Bit. LSB of word is set to zero. 1X- 1 Tag Bit. LSB of word is set to one.

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CONTROL WORD 20: BUFFER RAM, DIRECT PARALLEL, AND DIRECT SERIAL OUTPUT CONFIGURATION (SYNCHRONIZED WITH PROCCLK) (CONTINUED)

BIT POSITION	FUNCTION	DESCRIPTION
11-10	Q Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
9-8	Magnitude Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
7-6	Phase Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
5-4	Frequency Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
3-2	AGC Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
1-0	Timing Error Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).

CONTROL WORD 21: BUFFER RAM OUTPUT CONTROL REGISTER (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-16	Reserved	Reserved.
15	Output Buffer Mode	0- The output buffer operates in snapshot mode. 1- The output buffer operates in FIFO mode.
14-12	FIFO Mode Depth Threshold	In FIFO mode, when the FIFO depth reaches this threshold, an interrupt is generated and the READY flag is asserted. The threshold may be set from 0 to 7. Bit 14 is the MSB. The interrupt is generated when the FIFO depth reaches the threshold, as the FIFO fills.
11-4	Snapshot Mode Interval	In snapshot mode, the interval between snapshots in the output sample times is determined by this 8-bit binary number, i.e. 256, (2^8), sample time counts between snapshot samples. Program this parameter to 1 less than the desired interval. Bit 11 is the MSB.
3-0	Snapshot Mode Number of Samples	In snapshot mode, the number of samples stored each time the snapshot interval counter times out is equal to the decimal version of this 4-bit number. The range is 1- 8. Bit 3 is the MSB.

CONTROL WORD 22: BUFFER RAM OUTPUT FIFO RESET (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	FIFO reset	A write to this address increments the output FIFO RAM address pointers to READ = 111 and WRITE = 000.

CONTROL WORD 23: INCREMENT OUTPUT FIFO (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	FIFO Strobe	A write to this address increments the output FIFO/buffer to the next sample set.

CONTROL WORD 24: SYNCOUT STROBE OUTPUT PIN (SYNCHRONIZED TO CLKIN OR PROCCLK DEPENDING ON PROGRAMMING IN CONTROL WORD 0)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	SYNCOUT Strobe	A write to this address generates a one clock period wide strobe on the SYNCOUT pin that is synchronized to the clock. This strobe may be synchronized to CLKIN or PROCCLK based on the programming of bit 3 of Control Word 0.

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CONTROL WORD 25: COUNTER AND ACCUMULATOR RESET (SYNCHRONIZED TO BOTH CLKIN AND PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Counter and Accumulator Reset	A write to this address initializes the counters and accumulators for testing. Items that are reset are: Carrier NCO. 1. Loads phase offset <9:0> into register to be used for adding to accumulator. 2. Enables feedback on the accumulator. CIC Filter 1. Resets the decimation counter. 2. Clears enables to CIC. 3. Clears accumulators in CIC. 4. Clears enable leaving CIC. Halfband Filters 1. Resets compute counter in Halfband control. 2. Resets read address for all Halfband Filters. 3. Resets write address for all Halfband Filters. 4. Clears input available strobe. 5. Resets Halfband control logic. 255 Tap FIR 1. Resets FIR read and write address pointers. 2. Zero's coefficient read address. AGC Loop 1. Clears accumulator in loop filter. Re-Sampler and Interpolation Halfband Filters. 1. Resets counters for Halfband addresses for writing. 2. Resets output enable. 3. Reset controller for Re-Sampler. Timing NCO 1. Initializes counters for inserting extra pulses when interpolating halfbands are enabled. In the HSP50214B, a configuration control word bit determines if a Timing NCO reset is executed. If Control Word 27, Bit 20 is set to a logic one, a reset will clear the feedback in the timing NCO phase accumulator. If Control Word 27, Bit 20 is zero, a reset will not clear the timing NCO phase accumulator feedback, which is how the HSP50214 operated. Discriminator 1. Resets read and write address pointers. 2. Zero's coefficient read address. Cartesian to Polar Coordinate Counter 1. Resets Cordic counters (stops current computation). FIFO Control 1. Resets decoder for controlling FIFO. 2. Resets write address for FIFO. 3. Clears $\overline{RD}$ and $\overline{INTRRPT}$. 4. Resets "depth" and "full" flags. 5. Sets the empty flag. 6. Sets the read address to "7", write address to "0". Snapshot Control 1. Zeros the group number. 2. Load interval counter. 3. Resets write address and read address for FIFO. Output Serial Control 1. Reloads shift counter. 2. Reloads "Number of Words" counter. 3. Reloads counter for sync (for early or late). 4. Reloads counter for dividing down SERCLK. 5. In the HSP50214B, the Control Word 25 reset signal is designed such that the front end reset is 10 CLKIN periods wide and the back end reset is 10 PROCCLK periods wide. This guarantees that no enables will be caught in the pipelines.

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CONTROL WORD 26: LOAD AGC GAIN (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
(15:12) (11:5) (5:0)	eeee - AGC Exponent mmmmmmm - AGC Mantissa 000000 - Not Used	AGC LOAD. Writing to this location generates a strobe to load the AGC loop accumulator with bits (15:5) to the master registers. These bits are loaded into the MSBs of the AGC loop filter accumulator. Bits 15:12 are the exponent associated with the AGC gain shifter, while bits 11:5 are the mantissa associated with the AGC multiplier. The weighting of the AGC mantissa is 01.mmmmmmm. When considering Figure 23, the AGC Block Diagram, note the mux between the Register and the Limiter in the AGC Loop filter. The AGC LOAD controls the mux. Normally the mux would select the limiter output. When the AGC LOAD is asserted via the write command, the mux selects the Write Master Registers for data input See Table 20, Figure 45 and the associated text of the data sheet for an explanation of how data is loaded into the Master Registers for use internal to the part. Note that for the AGC LOAD only the lower 16 bits require data be valid to ensure a proper write of an AGC Value that will be loaded on write to CONTROL WORD 26.

CONTROL WORD 27: TEST REGISTER (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-25	Reserved	A fixed value of 0000 000 is loaded here for normal operation.
24	RAM Test Enable	0 = Normal Operation; 1 = RAM Test Enabled. The B Version includes test circuitry for the ROM and RAM blocks that was not present in the original release part. This circuitry must be disabled before loading the coefficient RAM's. This is done by setting bit 24 to zero. ***Because the HSP50214 did not require a "write" to Control Word 27 and the HSP50214B does require that Control Word 27, Bit 24 be set to zero for normal operation, software that was written for the HSP50214 will require modification to work properly with the HSP50214B.***
23	Input Level Detector Counter Preload Select	0 = The two LSB's of the interpolation period preload are set to zero. 1 = The two LSB's of the interpolation period preload are set to one.
22	SYNCIN1 Reset Control	0: SYNCIN1 causes only front end reset. 1: SYNCIN1 causes front end and back end resets.
21	Timing Error Input Select	0 = Operates as HSP50214. 1 = Corrects an error in the 4 LSB's.
20	Timing NCO Reset Control Select	0 = Backend reset will not clear the timing NCO phase accumulator feedback. 1 = Backend reset clears the timing NCO phase accumulator.
19 - 18	Discriminator FIR Input	00 = 18 bits of delayed and subtracted (optionally shifted) phase. 01 = 18 bits of magnitude from coordinate converter. 1X = 18 bits of resampler/halfband filer I output.
17	Input Level Detector Integration Start Select	0 = No external sync control of input end detector start/restart of integration period. 1 = SYNCIN causes the input level detector to start/restart its integration period.
16	AGC Average Control	0: AGC settles to mean. 1: AGC settles to median.
15	AGC Clear Inhibit	When set to zero, this bit will clear the AGC loop filter accumulator on a SYNCIN2 assertion or a WRITE to CW25. When set to a one, a WRITE to CW25 will not clear the AGC loop filter accumulator.
14	Q Input to Coordinate Converter (see bits 19 - 15)	0 = I and Q enabled to coordinate converter. I = Q input to coordinate converter is zeroed.
13	Coordinate Converter Input	0 = The Resampler HB filter output is routed to coordinate converter. 1 = The output of 255 tap FIR is routed to coordinate converter.
12-0	Reserved	A fixed value 0 0010 0111 1000 [0278]hex is loaded here for normal operation. A fixed value 0 0010 0111 1010 [027A]hex is loaded here for setting the Sin/Cos Generator outputs to 7FFF.

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CONTROL WORDS 64-95: DISCRIMINATOR COEFFICIENT REGISTERS (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-10	Discriminator FIR Coefficient	The discriminator FIR coefficients are 22-bit-two's complement. If the filter is symmetric, the coefficients are loaded from the center coefficient at address 64 to the last coefficient. If the filter is asymmetric the coefficients C_0 to C_N are loaded with C_0 in address 64 up to 64+N, where N is number of asymmetric coefficients.

CONTROL WORDS 128-255: 255 PROGRAMMABLE COEFFICIENT REGISTERS

BIT POSITION	FUNCTION	DESCRIPTION
31-10	Programmable FIR Coefficient	The programmable FIR coefficients are 22-bit-two's complement. If the filter is symmetric, the coefficients are loaded from the center coefficient at address 128 to the last coefficient. If the filter is asymmetric the coefficients C_0 to C_N are loaded with C_0 in address 128 up to 128+N, where N is number of asymmetric coefficients. Real Filters are computed as: Xn-k+1 Ck1 + Xn-k+2 Ck-2 + ... XnC0), where C0 is the coefficient in address 128 and Xo is the oldest data sample. Complex filters outputs are computed as follows: Xn is the most recent data sample. k is the number of samples = number of (complex) taps. C0_re is the coefficient loaded into CW128. C0_im is the coefficient loaded into CW129. The convolution starts with the oldest data, times the last complex coefficient, and ends with the newest data, times the first complex coefficient loaded. Iout = (-Xn-k+1_q * Ck-1_im + Xn-k+1_i * Ck-1_re). + (-Xn-k+2_q * Ck-2_im + Xn-1+2_i * Ck-2_re). + ... + (-Xn_q * C0_im + Xn_i * C0_re). Qout = (Xn-k+1_i * Ck-1_im + Xn-k+1_q * Ck-1_re). + (Xn-k+2_i * Ck-2_im + Xn-1+2_q * Ck-2_re). + ... + (Xn_i * C0_im + Xn_q * C0_re).

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Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range
Commercial . . . . . 0^oC to 70^oC
Industrial. . . . . -40^oC to 85^oC
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . .2V to V_{CC}
Input Rise and Fall Time . . . . . 1V/ns Max

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} ($^oC/W$)
MQFP Package 28
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5 ±5%, T_A = 0^oC to 70^oC, Commercial; -40^oC to 85^oC, Industrial

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
Clock Input High	V_{IHC}	V_{CC} = 5.25V	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.75V	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.75V	2.6	-	V
Output Low Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{CC} = 5.25V, Outputs Not Loaded	-	500	µA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	+10	µA
Operating Power Supply Current	I_{CCOP}	CLK = PROCCLK = 52MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Not Loaded	-	420	mA (Note 5)
Input Capacitance	C_{IN}	Freq = 1MHz, V_{CC} open, all measurements are referenced to device ground	-	8	pF (Note 6)
Output Capacitance	C_{OUT}				

NOTES:

5. Power Supply current is proportional to operation frequency. Typical rating for I_{CCOP} is 7mA/MHz.
6. Capacitance T_A = 25^oC, controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.

AC Electrical Specifications

V_{CC} = 5 ±5%, T_A = 0^o to 70^oC, Commercial (Note 7); -40^oC to 85^oC, Industrial (Note 7)

PARAMETER	SYMBOL	65MHz		UNITS
		MIN	MAX	
CLKIN Clock Period	t_{CP}	15	-	ns
CLKIN High	t_{CH}	6	-	ns
CLKIN Low	t_{CL}	6	-	ns
PROCCLK Period	t_{PCP}	18	-	ns
PROCCLK High	t_{PCH}	7	-	ns
PROCCLK Low	t_{PCL}	7	-	ns
REFCLK Clock Frequency	f_{RCP}	-	PROCCLK/2	Hz
REFCLK High	t_{RCH}	7	-	ns
REFCLK Low	t_{RCL}	7	-	ns
Setup Time GAINADJ(2:0), IN(13:0), $\overline{ENI}$, COF, COFSYNC, and SYNCIN1 to CLKIN	t_{DS}	7	-	ns

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AC Electrical Specifications

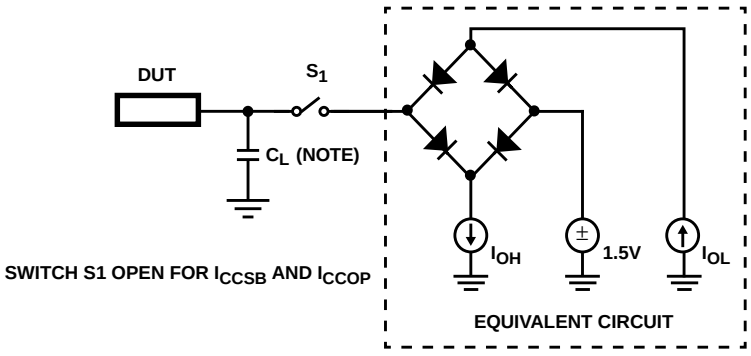
V_{CC} = 5 ±5%, T_A = 0° to 70°C, Commercial (Note 7); -40°C to 85°C, Industrial (Note 7) **(Continued)**

PARAMETER	SYMBOL	65MHz		UNITS
		MIN	MAX	
Hold Time GAINADJ(2:0), IN(13:0), $\overline{ENI}$, COF, COFSYNC, and SYNCIN1 from CLKIN	t_{DH}	0	-	ns
Setup Time AGCGNSEL, SOF, MCSYNCI, SOFSYNC, and SYNCIN2 to PROCCLK	t_{DSS}	7	-	ns
Hold Time AGCGNSEL, SOF, MCSYNCI, SOFSYNC, and SYNCIN2 from PROCCLK	t_{DHS}	0	-	ns
Setup Time, A(2:0) to Rising Edges of $\overline{WR}$	t_{WSA}	8	-	ns
Setup Time, A(2:0) C(7:0) to Rising Edges of $\overline{WR}$	t_{WSC}	10	-	ns
Hold Time, A(2:0) from Rising Edges of $\overline{WR}$	t_{WHA}	2	-	ns
Hold Time, A(2:0) C(7:0) from Rising Edges of $\overline{WR}$	t_{WHC}	0	-	ns
$\overline{WR}$ to CLKIN	t_{WC}	14	-	ns (Note 9)
PROCCLK to AOUT(15:0), BOUT (15:0), $\overline{DATARDY}$, SEROUTA, SEROUTB, $\overline{INTRRP}$	t_{DO_OUT}	-	8	ns
PROCCLK to SYNCOUT	t_{DO_SYNCI}	-	8	ns
PROCCK to MCSYNCO	t_{DO_SYNCO}	-	6	ns
PROCCLK to SERCLK, SERSYNC Valid	t_{DOS}	-	12	ns
$\overline{WR}$ High	t_{WRH}	15	-	ns
$\overline{WR}$ Low	t_{WRL}	8	-	ns
$\overline{RD}$ Low	t_{RL}	20	-	ns
Address Setup to Read Low	t_{AS}	-	3	ns
$\overline{RD}$ LOW to Data Valid	t_{RDO}	-	18	ns
$\overline{RD}$ HIGH to Output Disable	t_{ROD}	-	10	ns (Note 8)
Output Enable Time	t_{OE}	-	6	ns
Output Enable Time - FIFO Read Mode	t_{OEBL}	-	15	ns
Output Disable Time	t_{OD}	-	8	ns (Note 8)
Output Rise, Fall Time	t_{RF}	-	3	ns (Note 8)

NOTES:

7. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400µA. Input reference level for CLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
8. Controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.
9. Setup time required to ensure action initiated by $\overline{WR}$ will be seen by a particular CLKIN.

AC Test Load Circuit



NOTE: Test head capacitance.

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Waveforms

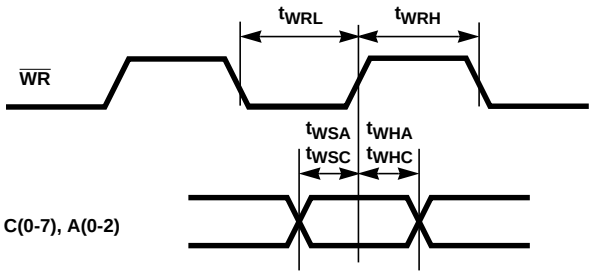


FIGURE 50. TIMING RELATIVE TO $\overline{WR}$

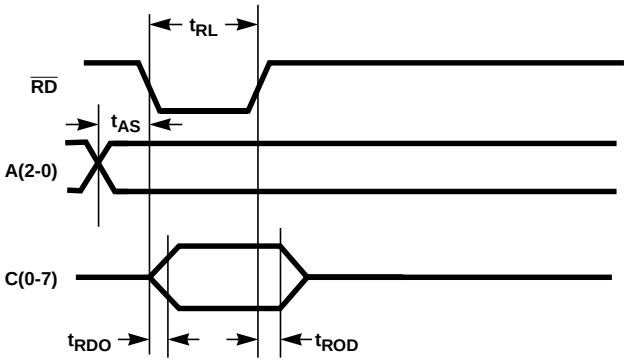


FIGURE 51. TIMING RELATIVE TO $\overline{RD}$

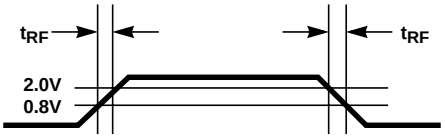


FIGURE 52. OUTPUT RISE AND FALL TIMES

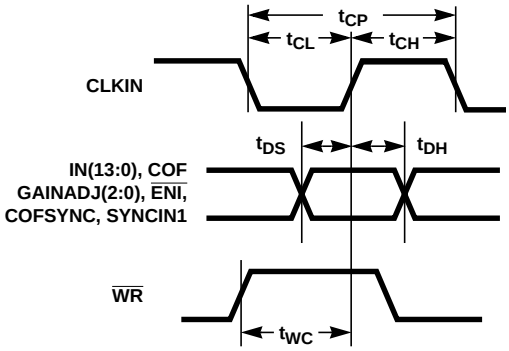


FIGURE 53. TIMING RELATIVE TO CLKIN

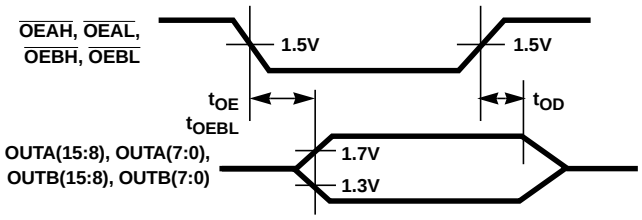


FIGURE 54. OUTPUT ENABLE/DISABLE

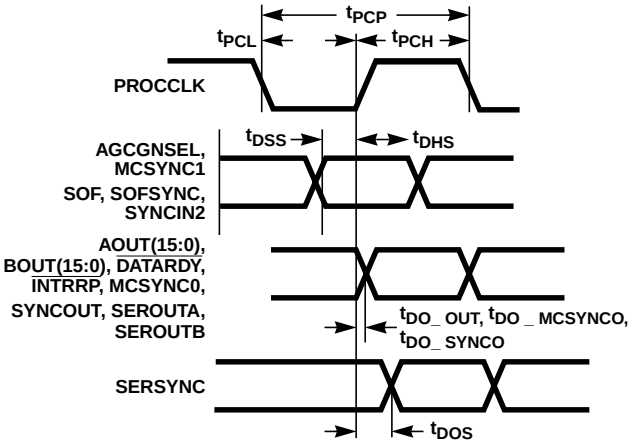


FIGURE 55. TIMING RELATIVE TO PROCCLK

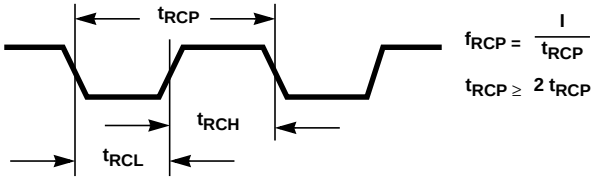


FIGURE 56. REFCLK

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Appendix B: Analog Devices AD6640 – 12–Bit, 65 MSPS IF Sampling A/D Converter

Included for your reference on the following pages is the data sheet for the AD6640 12–bit, 65 Megasample/second IF sampling Analog to Digital Converter, provided by the courtesy of Analog Devices Inc., Norwood, MA.

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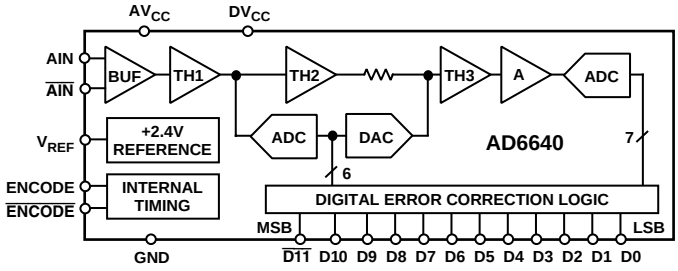
12-Bit, 65 MSPS IF Sampling A/D Converter

AD6640

FEATURES
65 MSPS Minimum Sample Rate
80 dB Spurious-Free Dynamic Range
IF-Sampling to 70 MHz
710 mW Power Dissipation
Single +5 V Supply
On-Chip T/H and Reference
Twos Complement Output Format
3.3 V or 5 V CMOS-Compatible Output Levels

APPLICATIONS
Cellular/PCS Base Stations
Multichannel, Multimode Receivers
GPS Anti-Jamming Receivers
Communications Receivers
Phased Array Receivers

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD6640 is a high speed, high performance, low power, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference are included on-chip to provide a complete conversion solution. The AD6640 runs on a single +5 V supply and provides CMOS-compatible digital outputs at 65 MSPS.

Specifically designed to address the needs of multichannel, multimode receivers, the AD6640 maintains 80 dB spurious-free dynamic range (SFDR) over a bandwidth of 25 MHz. Noise performance is also exceptional; typical signal-to-noise ratio is 68 dB.

The AD6640 is built on Analog Devices' high speed complementary bipolar process (XFCB) and uses an innovative multipass architecture. Units are packaged in a 44-terminal Plastic Thin Quad Flatpack (TQFP) specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate is 65 MSPS.
2. Fully differential analog input stage specified for frequencies up to 70 MHz; enables "IF Sampling."
3. Low power dissipation: 710 mW off a single +5 V supply.
4. Digital outputs may be run on +3.3 V supply for easy interface to digital ASICs.
5. Complete Solution: reference and track-and-hold.
6. Packaged in small, surface mount, plastic 44-terminal TQFP.

REV. 0

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AD6640–SPECIFICATIONS

DC SPECIFICATIONS (AV_{CC} = +5 V, DV_{CC} = +3.3 V; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	AD6640AST Min	Typ	Max	Units
RESOLUTION				12		Bits
ACCURACY						
No Missing Codes	+25°C	I		GUARANTEED		
Offset Error	Full	VI	–10	3.5	+10	mV
Gain Error	Full	VI	–10	4.0	+10	% FS
Differential Nonlinearity (DNL)[1]	+25°C	I	–1.0	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[1]	Full	V		±1.25		LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		50		ppm/°C
Gain Error	Full	V		100		ppm/°C
POWER SUPPLY REJECTION (PSRR)	Full	V		±0.5		mV/V
REFERENCE OUT (V_{REF})[2]	Full	V		2.4		V
ANALOG INPUTS (AIN, $\overline{AIN}$)[3]						
Analog Input Common-Mode Range[4]	Full	V		V_{REF} ± 0.05		V
Differential Input Voltage Range	Full	V		2.0		V p-p
Differential Input Resistance	Full	IV	0.7	0.9	1.1	kΩ
Differential Input Capacitance	+25°C	V		1.5		pF
POWER SUPPLY						
Supply Voltage						
AV_{CC}	Full	VI	4.75	5.0	5.25	V
DV_{CC}	Full	VI	3.0	3.3	5.25	V
Supply Current						
IA_{VCC} (AV_{CC} = 5.0 V)	Full	VI		135	160	mA
ID_{VCC} (DV_{CC} = 3.3 V)	Full	VI		10	20	mA
POWER CONSUMPTION	Full	VI		710	865	mW

NOTES
[1]ENCODE = 20 MSPS
[2]If V_{REF} is used to provide a dc offset to other circuits, it should first be buffered.
[3]The AD6640 is designed to be driven differentially. Both AIN and $\overline{AIN}$ should be driven at levels V_{REF} ± 0.5 volts. The input signals should be 180 degrees out of phase to produce a 2 V p-p differential input signal. See Driving the Analog Inputs section for more details.
[4]Analog input common-mode range specifies the offset range the analog inputs can tolerate in dc-coupled applications (see Figure 35 for more detail).

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AV_{CC} = +5 V, DV_{CC} = +3.3 V; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	AD6640AST Min	Typ	Max	Units
LOGIC INPUTS (ENC, $\overline{ENC}$)[1]						
Encode Input Common-Mode Range[2]	Full	IV	0.2		2.2	V
Differential Input Voltage	Full	IV	0.4			V p-p
Single-Ended Encode					10	V p-p
Logic Compatibility[3]				TTL/CMOS		
Logic "1" Voltage	Full	VI	2.0		5.0	V
Logic "0" Voltage	Full	VI	0		0.8	V
Logic "1" Current (V_{INH} = 5 V)	Full	VI	500	650	800	µA
Logic "0" Current (V_{INL} = 0 V)	Full	VI	–400	–320	–200	µA
Input Capacitance	+25°C	V		2.5		pF
LOGIC OUTPUTS ($\overline{D11}$–D0)[4]						
Logic Compatibility				CMOS		
Logic "1" Voltage (DV_{CC} = +3.3 V)	Full	VI	2.8	DV_{CC} – 0.2		V
Logic "0" Voltage (DV_{CC} = +3.3 V)	Full	VI		0.2	0.5	V
Logic "1" Voltage (DV_{CC} = +5.0 V)	Full	IV	4.5	DV_{CC} – 0.3		V
Logic "0" Voltage (DV_{CC} = +5.0 V)	Full	IV		0.35	0.5	V
Output Coding				Twos Complement		

NOTES
[1]Best dynamic performance is obtained by driving ENC and $\overline{ENC}$ differentially. See Encoding the AD6640 section for more details. Performance versus ENC/$\overline{ENC}$ power is shown in Figure 18 under Typical Performance Characteristics.
[2]For dc-coupled applications, Encode Input Common-Mode Range specifies the common-mode range the encode inputs can tolerate when driven differentially by minimum differential input voltage of 0.4 V p-p. For differential input voltage swings greater than 0.4 V p-p, the common-mode range will change. The minimum value insures that the input voltage on either encode pin does not go below 0 V. The maximum value insures that the input voltage on either encode pin does not go below 2.0 V or above AV_{CC} (e.g., for a differential input swing of 0.8 V, the min and max common-mode specs become 0.4 V and 2.4 V respectively).
[3]ENC or $\overline{ENC}$ may be driven alone if desired, but performance will likely be degraded. Logic Compatibility specifications are provided to show that TTL or CMOS clock sources will work. When driving only one encode input, bypass the complementary input to GND with 0.01 µF.
[4]Digital output load is one LCX gate.

Specifications subject to change without notice.

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SWITCHING SPECIFICATIONS[1] (AV_{CC} = +5 V, DV_{CC} = +3.3 V; ENCODE & $\overline{ENCODE}$ = 65 MSPS; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	AD6640AST Min	Typ	Max	Units
Maximum Conversion Rate	Full	VI	65			MSPS
Minimum Conversion Rate[2]	Full	IV			6.5	MSPS
Aperture Delay (t_A)	+25°C	V		400		ps
Aperture Uncertainty (Jitter)	+25°C	V		0.3		ps rms
ENCODE Pulsewidth High[3]	+25°C	IV	6.5			ns
ENCODE Pulsewidth Low	+25°C	IV	6.5			ns
Output Delay (t_{OD}) DV_{CC} +3.3 V/5.0 V[4]	Full	IV	8.5	10.5	12.5	ns

NOTES
[1]All switching specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]A plot of Performance vs. Encode is shown in Figure 16 under Typical Performance Characteristics.
[3]A plot of Performance vs. Duty Cycle (Encode = 65 MSPS) is shown in Figure 17 under Typical Performance Characteristics.
[4]Outputs driving one LCX gate. Delay is measured from differential crossing of ENC, $\overline{ENC}$ to the time when all output data bits are within valid logic levels.
Specifications subject to change without notice.

AC SPECIFICATIONS[1] (AV_{CC} = +5 V, DV_{CC} = +3.3 V; ENCODE & $\overline{ENCODE}$ = 65 MSPS; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter (Conditions)		Temp	Test Level	AD6640AST Min	Typ	Max	Units
SNR							
Analog Input	2.2 MHz	+25°C	V		68		dB
@ –1 dBFS	15.5 MHz	+25°C	I	64	67.7		dB
	31.0 MHz	+25°C	V		67.5		dB
	69.0 MHz	+25°C	V		66		dB
SINAD							
Analog Input	2.2 MHz	+25°C	V		68		dB
@ –1 dBFS	15.5 MHz	+25°C	I	63.5	67.2		dB
	31.0 MHz	+25°C	V		67.0		dB
	69.0 MHz	+25°C	V		65.5		dB
Worst Harmonic[2] (2nd or 3rd)							
Analog Input	2.2 MHz	+25°C	V		80		dBc
@ –1 dBFS	15.5 MHz	+25°C	I	74	80		dBc
	31.0 MHz	+25°C	V		79.5		dBc
	69.0 MHz	+25°C	V		78.5		dBc
Worst Harmonic[2] (4th or Higher)							
Analog Input	2.2 MHz	+25°C	V		85		dBc
@ –1 dBFS	15.5 MHz	+25°C	I	74	85		dBc
	31.0 MHz	+25°C	V		85		dBc
	69.0 MHz	+25°C	V		84		dBc
Multitone SFDR (w/Dither)[3]							
Eight Tones @ –20 dBFS		Full	V		90		dBFS
Two-Tone IMD Rejection[4]							
F1, F2 @ –7 dBFS		Full	V		80		dBc
Analog Input Bandwidth[5]		+25°C	V		300		MHz

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]For a single test tone at –1 dBFS, the worst case spectral performance is typically limited by the direct or aliased 2nd or 3rd harmonic. If a system is designed such that the 2nd and 3rd harmonics fall out-of-band, overall performance in the band of interest is typically improved by 5 dB. Worst Harmonic (4th or Higher) includes 4th and higher order harmonics and all other spurious components. Reference Figure 12 for more detail.
[3]See Overcoming Static Nonlinearities with Dither section for details on improving SFDR performance. To measure SFDR, eight tones from 14 MHz to 18 MHz (0.5 MHz spacing) are swept from –20 dBFS to –90 dBFS. An open channel at 16 MHz is used to monitor SFDR.
[4]F1 = 14.9 MHz, F2 = 16 MHz.
[5]Specification is small signal bandwidth. Plots of Performance versus Analog Input Frequency are shown in Figures 10, 11 and 12. Sampling wide bandwidths (5 MHz–15 MHz) should be limited to 70 MHz center frequency.
Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Units
ELECTRICAL			
AV_{CC} Voltage	0	7	V
DV_{CC} Voltage	0	7	V
Analog Input Voltage	0	AV_{CC}	V
Analog Input Current		25	mA
Digital Input Voltage (ENCODE)	0	AV_{CC}	V
Digital Output Current	–10	10	mA
ENVIRONMENTAL[2]			
Operating Temperature Range (Ambient)	–40	+85	°C
Maximum Junction Temperature		+150	°C
Lead Temperature (Soldering, 10 sec)		+300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (44-terminal TQFP); θ_{JA} = 55°C/W.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C; sample tested at temperature extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6640AST	–40°C to +85°C (Ambient)	44-Terminal TQFP (Thin Quad Plastic Flatpack)	ST-44
AD6640ST/PCB		Evaluation Board with AD6640AST	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6640 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



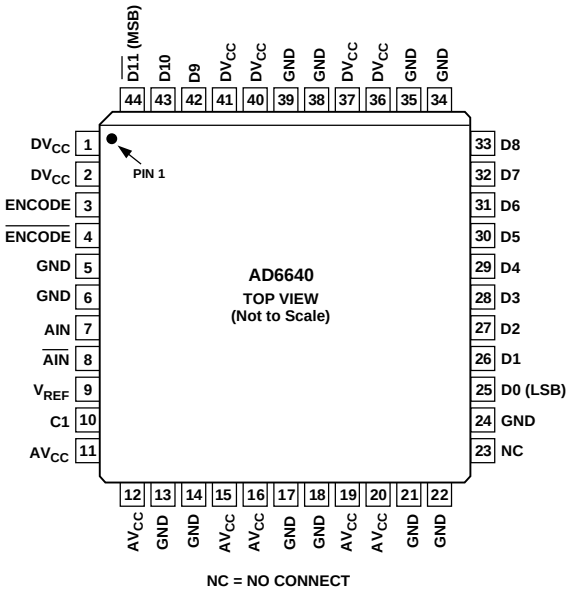
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PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1, 2, 36, 37, 40, 41	DV_{CC}	+3.3 V/+5 V Power Supply (Digital). Powers output stage only.
3	ENCODE	Encode Input. Data conversion initiated on rising edge.
4	$\overline{\text{ENCODE}}$	Complement of ENCODE. Drive differentially with ENCODE or bypass to Ground for single-ended clock mode. See Encoding the AD6640 section.
5, 6, 13, 14, 17, 18, 21, 22, 24, 34, 35, 38, 39	GND	Ground.
7	AIN	Analog Input.
8	$\overline{\text{AIN}}$	Complement of Analog Input.
9	V_{REF}	Internal Voltage Reference. Nominally +2.4 V. Bypass to Ground with 0.1 µF + 0.01 µF microwave chip capacitor.
10	C1	Internal Bias Point. Bypass to ground with 0.01 µF capacitor.
11, 12, 15, 16, 19, 20	AV_{CC}	+5 V Power Supply (Analog).
23	NC	No Connect.
25	D0 (LSB)	Digital Output Bit (Least Significant Bit).
26–33	D1–D8	Digital Output Bits.
42, 43	D9–D10	Digital Output Bits.
44	$\overline{\text{D11}}$ (MSB)[1]	Digital Output Bit (Most Significant Bit).

NOTE
[1]Output coded as twos complement.

PIN CONFIGURATION



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DEFINITION OF SPECIFICATIONS

Analog Bandwidth (Small Signal)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in logic "1" state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

Worst Harmonic
The ratio of the rms signal amplitude to the rms value of the worst harmonic component, reported in dBc.

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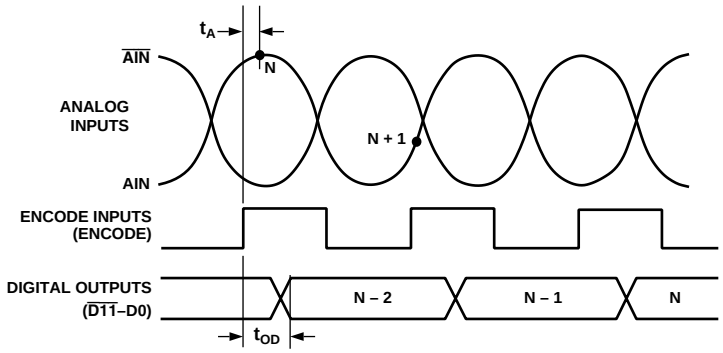


Figure 1. Timing Diagram

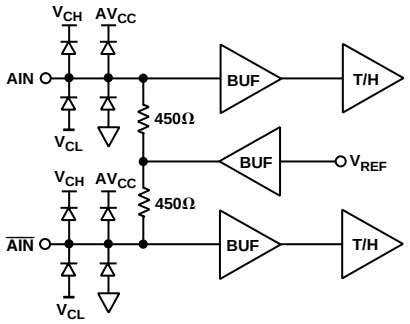


Figure 2. Analog Input Stage

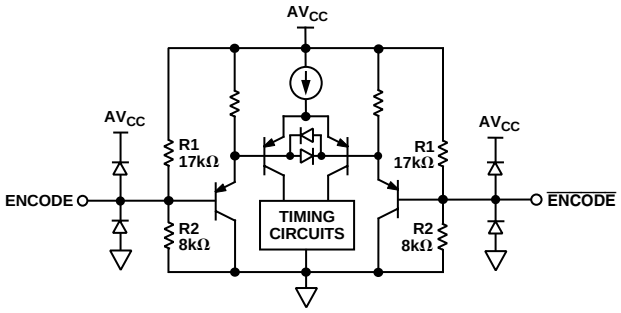


Figure 3. Encode Inputs

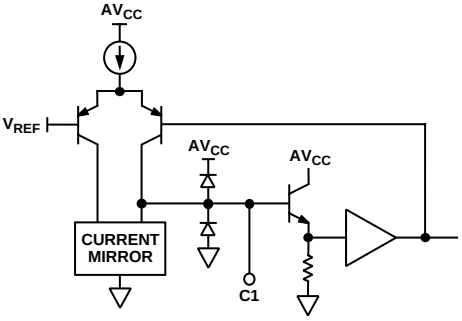


Figure 4. Compensation Pin, C1

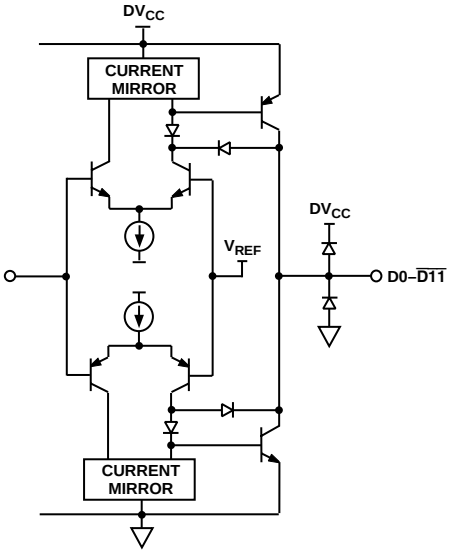


Figure 5. Digital Output Stage

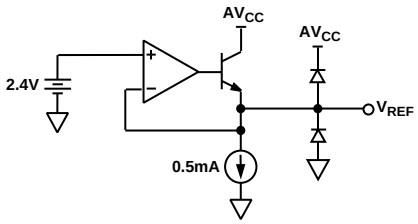


Figure 6. 2.4 V Reference

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AD6640–Typical Performance Characteristics

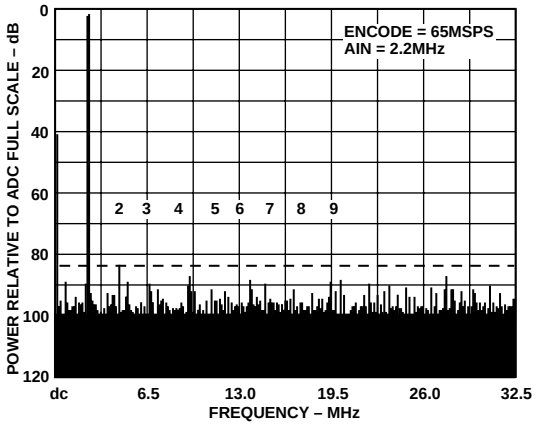


Figure 7. Single Tone at 2.2 MHz

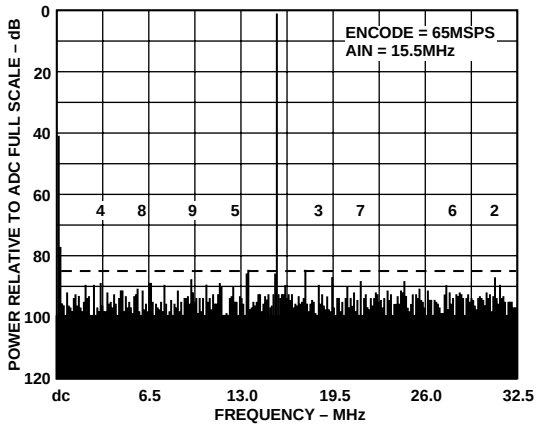


Figure 8. Single Tone at 15.5 MHz

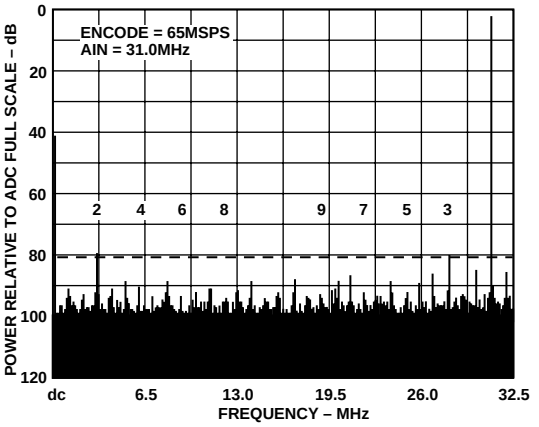


Figure 9. Single Tone at 31.0 MHz

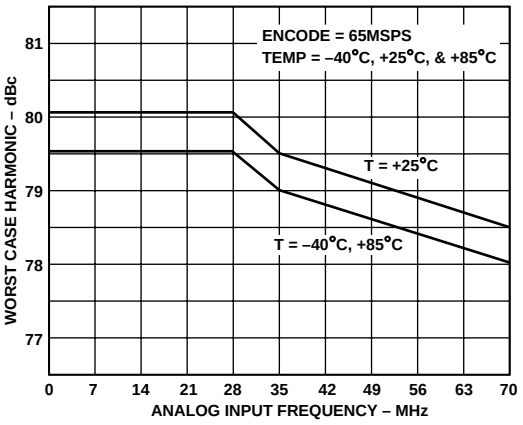


Figure 10. Harmonics vs. AIN

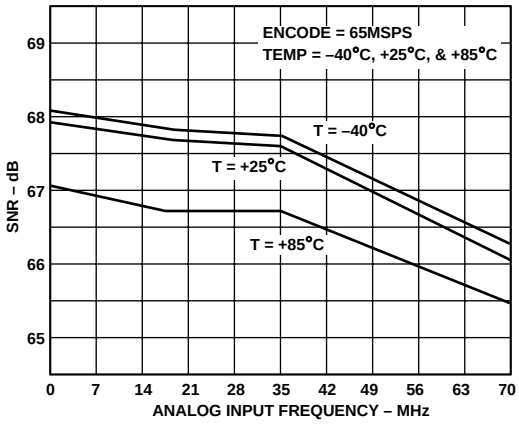


Figure 11. Noise vs. AIN

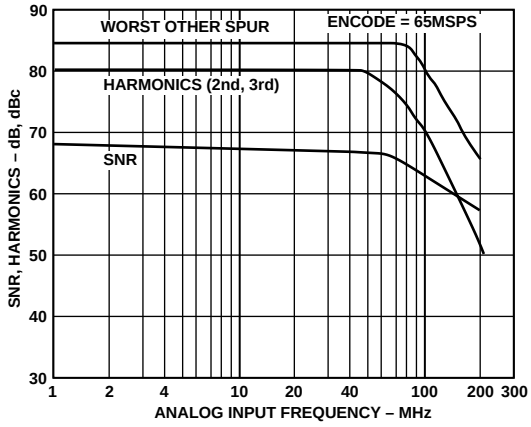


Figure 12. Harmonics, Noise vs. AIN

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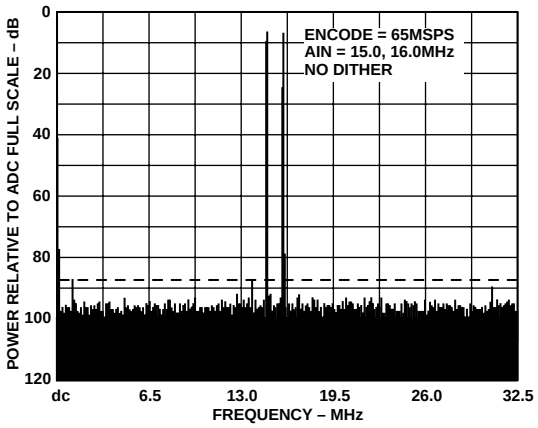


Figure 13. Two Tones at 15.0 MHz & 16.0 MHz

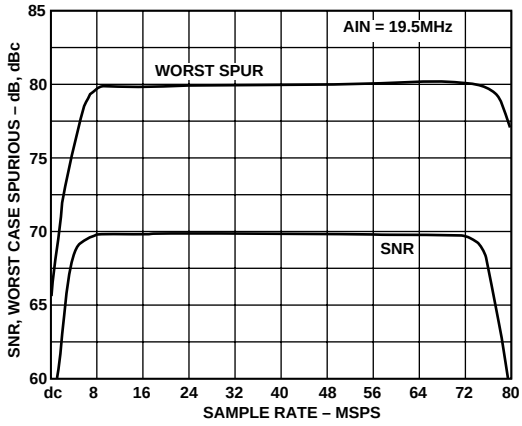


Figure 16. SNR, Worst Spurious vs. Encode

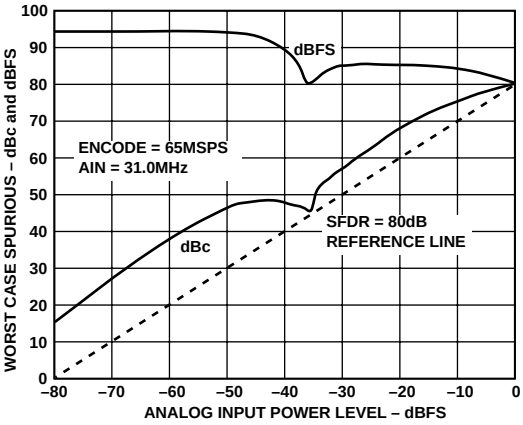


Figure 14. Single Tone SFDR

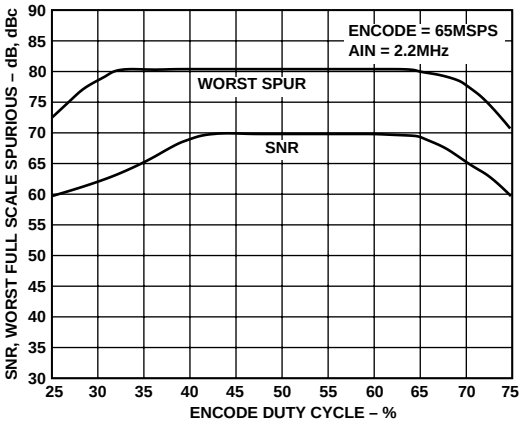


Figure 17. SNR, Worst Spurious vs. Duty Cycle

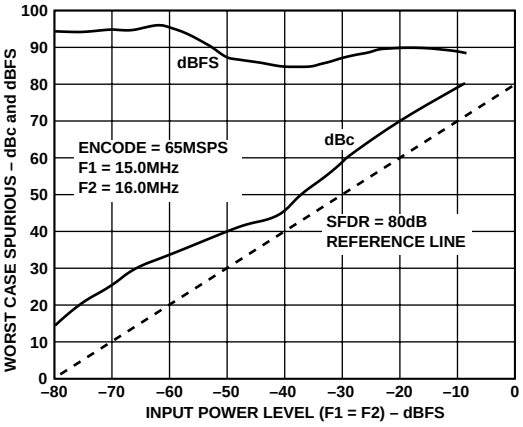


Figure 15. Two Tone SFDR

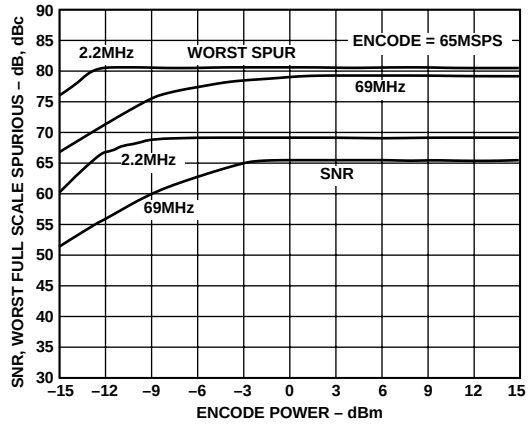


Figure 18. SNR, Worst Spurious vs. Encode Power

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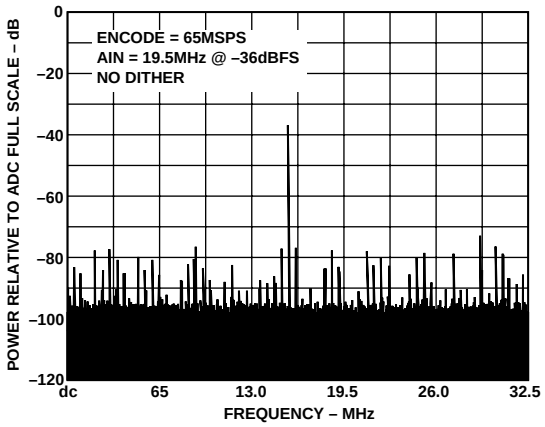


Figure 19. 16K FFT without Dither

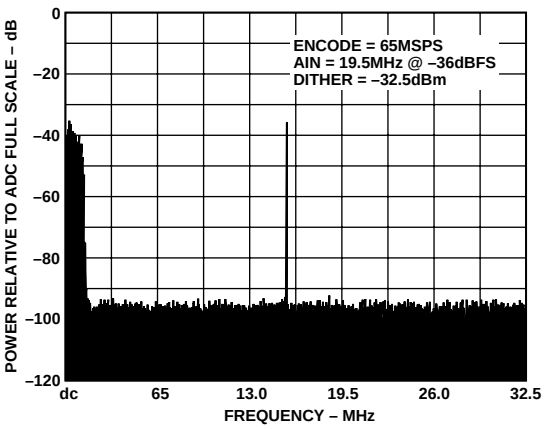


Figure 22. 16K FFT with Dither

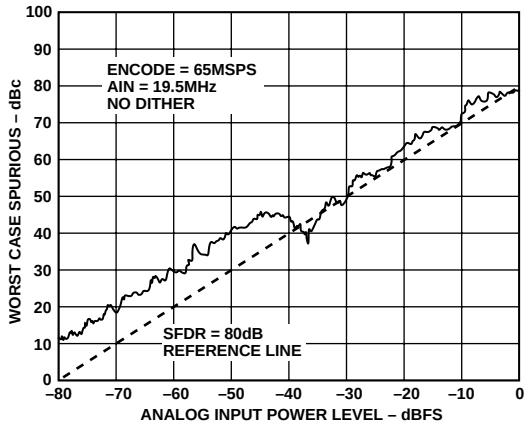


Figure 20. SFDR without Dither

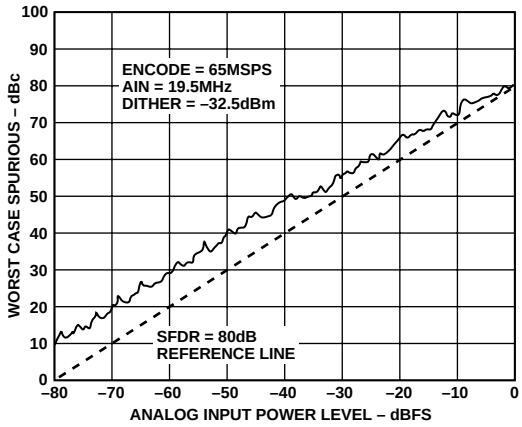


Figure 23. SFDR with Dither

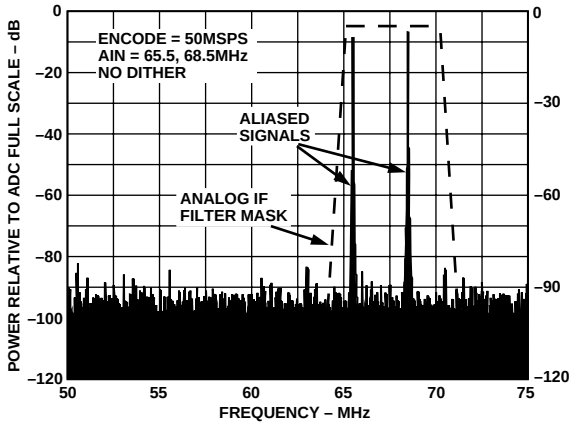


Figure 21. IF-Sampling at 70 MHz without Dither

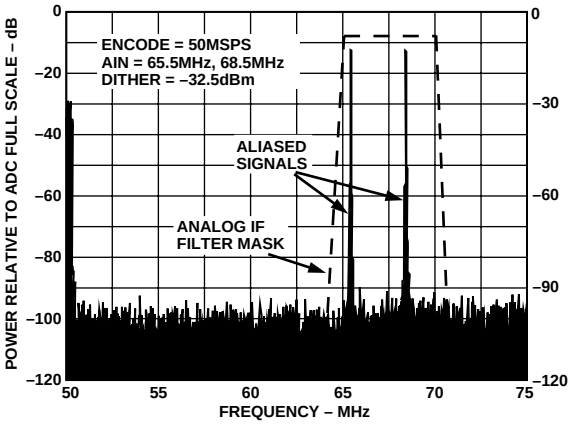


Figure 24. IF-Sampling at 70 MHz with Dither

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THEORY OF OPERATION

The AD6640 analog-to-digital converter (ADC) employs a two-stage subrange architecture. This design approach ensures 12-bit accuracy, without the need for laser trim, at low power.

As shown in the functional block diagram, the AD6640 has complementary analog input pins, AIN and $\overline{\text{AIN}}$. Each analog input is centered at 2.4 volts and should swing ±0.5 volts around this reference (ref. Figure 2). Since AIN and $\overline{\text{AIN}}$ are 180 degrees out of phase, the differential analog input signal is 2 volts peak-to-peak.

Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 6-bit coarse ADC. The digital output of the coarse ADC drives a 6-bit DAC; the DAC is 12 bits accurate. The output of the 6-bit DAC is subtracted from the delayed analog signal at the input of TH3 to generate a residue signal. TH2 is used as an analog pipeline to null out the digital delay of the coarse ADC.

The 6-bit coarse ADC word and 7-bit residue word are added together and corrected in the digital error correction logic to generate the output word. The result is a 12-bit parallel digital CMOS-compatible word, coded as twos complement.

APPLYING THE AD6640

Encoding the AD6640

Best performance is obtained by driving the encode pins differentially. However, the AD6640 is also designed to interface with TTL and CMOS logic families. The source used to drive the ENCODE pin(s) must be clean and free from jitter. Sources with excessive jitter will limit SNR (reference Equation 1 under "Noise Floor and SNR").

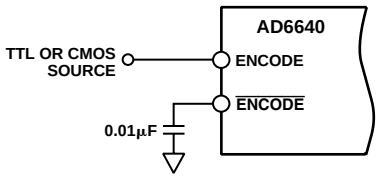


Figure 25. Single-Ended TTL/CMOS Encode

The AD6640 encode inputs are connected to a differential input stage (see Figure 3 under EQUIVALENT CIRCUITS). With no input signal connected to either ENCODE pin, the voltage dividers bias the inputs to 1.6 volts. For TTL or CMOS usage, the encode source should be connected to ENCODE, Pin 3. $\overline{\text{ENCODE}}$ should be decoupled using a low inductance or microwave chip capacitor to ground.

If a logic threshold other than the nominal 1.6 V is required, the following equations show how to use an external resistor, Rx, to raise or lower the trip point (see Figure 3; R1 = 17 kΩ, R2 = 8 kΩ).

$$V_l = \frac{5R2Rx}{R1R2 + R1Rx + R2Rx}$$ to lower logic threshold.

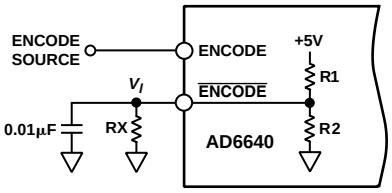


Figure 26. Lower Logic Threshold for Encode

$$V_l = \frac{5R2}{R2 + \frac{R1R_X}{R1 + R_X}}$$ to raise logic threshold.

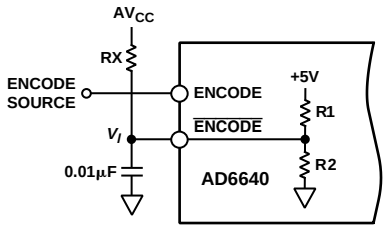


Figure 27. Raise Logic Threshold for Encode

While the single-ended encode will work well for many applications, driving the encode differentially will provide increased performance. Depending on circuit layout and system noise, a 1 dB to 3 dB improvement in SNR can be realized. It is not recommended that differential TTL logic be used however, because most TTL families that support complementary outputs are not delay or slew rate matched. Instead, it is recommended that the encode signal be ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins.

The simplest option is shown below. The low jitter TTL signal is coupled with a limiting resistor, typically 100 ohms, to the primary side of an RF transformer (these transformers are inexpensive and readily available; part number in Figure 28 is from Mini-Circuits). The secondary side is connected to the ENCODE and $\overline{\text{ENCODE}}$ pins of the converter. Since both encode inputs are self-biased, no additional components are required.

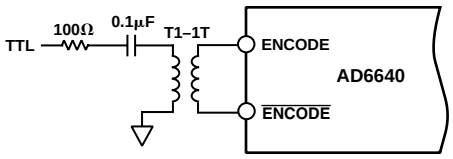


Figure 28. TTL Source – Differential Encode

A clean sine wave may be substituted for a TTL clock. In this case, the matching network is shown below. Select a transformer ratio to match source and load impedances. The input impedance of the AD6640 encode is approximately 11 kΩ differentially. Therefore "R," shown in the Figure 29, may be any value that is convenient for available drive power.

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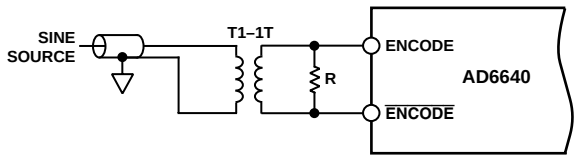


Figure 29. Sine Source – Differential Encode

If a low jitter ECL clock is available, another option is to ac-couple a differential ECL signal to the encode input pins as shown below. The capacitors shown here should be chip capacitors but do not need to be of the low inductance variety.

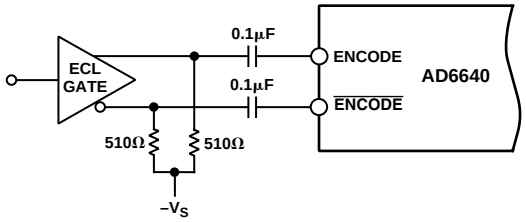


Figure 30. Differential ECL for Encode

As a final alternative, the ECL gate may be replaced by an ECL comparator. The input to the comparator could then be a logic signal or a sine signal.

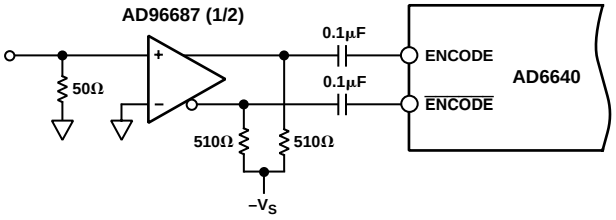


Figure 31. ECL Comparator for Encode

Driving the Analog Input

Because the AD6640 operates from a single +5 volt supply, the analog input voltage range is offset from ground by 2.4 volt. Each analog input connects through a 450 ohm resistor to the 2.4 volt bias voltage and to the input of a differential buffer (Figure 32). This resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6640 should be ac-coupled to the input pins. Since the differential input impedance of the AD6640 is 0.9 kΩ, the analog input power requirement is only –3 dBm, simplifying the drive amplifier in many cases.

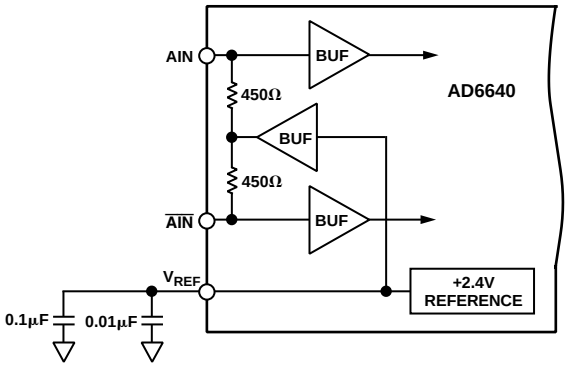


Figure 32. Differential Analog Inputs

To take full advantage of this high input impedance, a 20:1 transformer would be required. This is a large ratio and could result in unsatisfactory performance. In this case, a lower step-up ratio could be used. For example, if R_T were set to 260 ohms, along with a 4:1 transformer, the input would match to a 50 ohm source with a full-scale drive of +4 dBm (Figure 33). Note that the external load resistor, R_T, is in parallel with the AD6640 analog input resistance of 900 ohms. The external resistor value can be calculated from the following equation:

$$R_T = \frac{1}{\frac{1}{Z} - \frac{1}{900}}$$

where Z is the desired impedance (200 Ω for a 4:1 transformer with 50 Ω input source).

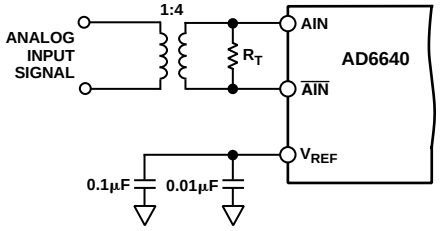


Figure 33. Transformer-Coupled Analog Input Signal

If the lower drive power is attractive, a combination transformer match and LC match could be employed that would use a 4:1 transformer with an LC as shown in Figure 34. This solution is useful when good performance in the third Nyquist zone is required. Such a requirement arises when digitizing high intermediate frequencies in communications receivers.

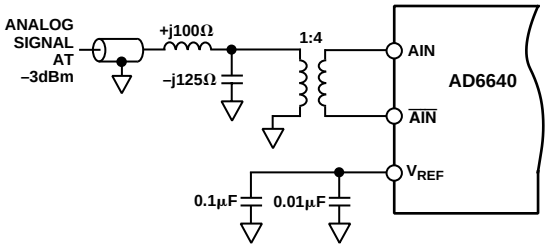


Figure 34. Low Power Drive Circuit

In applications where gain is needed but dc-coupling is not necessary, an extension of Figure 34 is recommended. A 50 ohm gain block may be placed in front of the LC matching network. Such gain blocks are readily available for commercial applications. These low cost modules can have excellent NF and intermodulation performance. This circuit is especially good for the "IF" receiver application previously mentioned.

In applications where dc-coupling is required the following circuit can be used (Figure 35). It should be noted that the addition of circuitry for dc-coupling may compromise performance in terms of noise, offset and dynamic performance. This circuit requires an inverting and noninverting signal path. Additionally, an offset must be generated so that the analog input to each pin is centered near 2.4 volts. Since the input is differential, small differences in the dc voltage at each input can translate into an offset for the circuit. The same holds true for gain mismatch. Therefore, some means of adjusting the gain and offset between

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the sides should be implemented. The addition of small value resistors between the AD9631 and the AD6640 will prevent oscillation due to the capacitive input of the ADC.

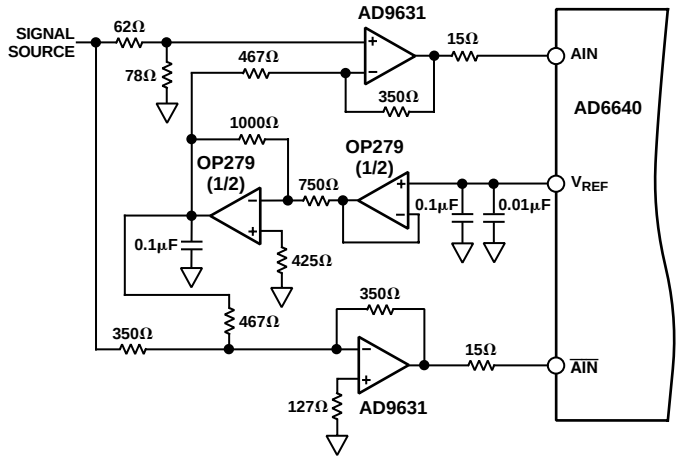


Figure 35. DC-Coupled Analog Input Circuit

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended as switching supplies tend to have radiated components that may be "received" by the AD6640. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD6640 has separate digital and analog +5 V pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC}. Although analog and digital supplies may be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching noise back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 volts; however the DV_{CC} supply may be varied according to output digital logic family (i.e., DV_{CC} should be connected to the same supply as the digital circuitry). The AD6640 is specified for DV_{CC} = 3.3 V as this is a common supply for digital ASICs.

Output Loading

Care must be taken when designing the data receivers for the AD6640. It is recommended that the digital outputs drive a series resistor (e.g. 348 ohms) followed by a gate like the 74LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic shown in Figure 36. The digital outputs of the AD6640 have a constant rise time output stage. The output slew rate is about 1 V/ns when DV_{CC} = +5 V. A typical CMOS gate combined with PCB trace and through hole will have a load of approximately 10 pF. Therefore as each bit switches, 10 mA

$\left(10\,pF \times \frac{1V}{1\,ns}\right)$ of dynamic current per bit will flow in or out of the device. A full-scale transition can cause up to 120 mA (12 bits × 10 mA/bit) of current to flow through the digital output stages. The series resistor will minimize the output currents that can flow in the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD6640.

Layout Information

The schematic of the evaluation board (Figure 36) represents a typical implementation of the AD6640. The pinout of the AD6640 facilitates ease of use and the implementation of high frequency/high resolution design practices. All of the digital outputs are on one side while the other sides contain all of the inputs. It is highly recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. Depending on the configuration used for the encode and analog inputs, one or more capacitors are required on those input pins. The capacitors used on the $\overline{\text{ENCODE}}$ and V_{REF} pins must be a low inductance chip capacitor as referenced previously in the data sheet.

A multilayer board is recommended to achieve best results. Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate (broken only by the insertion of the series resistor). Digital data lines should be kept clear of analog and encode traces.

Evaluation Boards

The evaluation board for the AD6640 is very straightforward, consisting of power, signal inputs and digital outputs. The evaluation board includes the option for an onboard clock oscillator for the encode.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the crystal oscillator and the AV_{CC} pins of the AD6640.

The DV_{CC} power is supplied via J3, the digital interface. This digital supply connection also powers the digital gates on the PCB. By maintaining separate analog and digital power supplies, degradation in SNR and SFDR is kept to a minimum. Total power requirement is approximately 200 mA. This configuration allows for easy evaluation of different logic families (i.e., connection to a 3.3 volt logic board).

The analog input is connected via J2 and is transformer-coupled to the AD6640 (see Driving the Analog Input). The onboard termination resistor is 270 Ω. This resistor, in parallel with the AD6640's input resistance (900 Ω), provides a 50 Ω load to the analog source driving the 1:4 transformer. If a different input impedance is required, replace R16 by using the following equation

$$R16 = \frac{1}{\frac{1}{Z} - \frac{1}{900}}$$

where Z is desired input impedance (200 Ω for a 4:1 transformer with 50 Ω source).

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The analog input range of the PCB is ±0.5 volts (i.e., signal ac-coupled to AD6640).

The encode signal may be generated using an onboard crystal oscillator, U1. The oscillator is socketed and may be replaced by an external encode source via J1. If an external source is used, it should be a high quality TTL source. A transformer converts the single-ended TTL signal to a differential clock (see Encoding the AD6640). Since the encode is coupled with a transformer, a sine wave could have been used; note, however, that U5 requires TTL levels to function properly.

AD6640 output data is latched using 74LCX574 (U3, U4) latches following 348 ohm series resistors. The resistors limit the current that would otherwise flow due to the digital output slew rate. The resistor value was chosen to represent a time constant of ~25% of the data rate at 65 MHz. This reduces slew rate while not appreciably distorting the data waveform. Data is latched in a pipeline configuration; a rising edge generates the new AD6640 data sample, latches the previous data at the converter output, and strobes the external data register over J3.

NOTE: Power and ground must be applied to J3 to power the digital logic section of the evaluation board.

Table I. AD6640ST/PCB Bill of Material

Item	Quantity	Reference	Description
1	2	+5 VA, GND	Banana Jack
2	11	C7–C9, C11–C17, C19	Ceramic Chip Capacitor 0805, 0.1 µF
3	2	C4, C6	Tantalum Chip Capacitor 10 µF
4	1	J3	40-Pin Double Row Male Header
5	3	J1, J2, J4	BNC Coaxial PCB Connector
6	1	R1	Surface Mount Resistor 1206, 348 Ω
7	25	R2–R14, R20–R25, R30–R35	Surface Mount Resistor 1206, 348 Ω
8	1	R15	Surface Mount Resistor 1206, 100 Ω
9	1	R16	Surface Mount Resistor 1206, 270 Ω
10	2	T1, T2	Surface Mount Transformer Mini-Circuits T4–1T, 1:4 Ratio
11	1	U1	Clock Oscillator (Optional)
12	1	DUT	AD6640AST 12-Bit–65 MSPS ADC Converter
13	2	U3, U4	74LCX574 Octal Latch
14	1	U5	74LVQ00 Quad Two Input NAND Gate
15	1	C1, C18	Ceramic Chip Capacitor 0508, 0.01 µF Low Inductance
16	2	C2, C3	Ceramic Chip Capacitor 0508, 0.1 µF Low Inductance
17	2	CR1, CR2	1N2810 Schottky Diode

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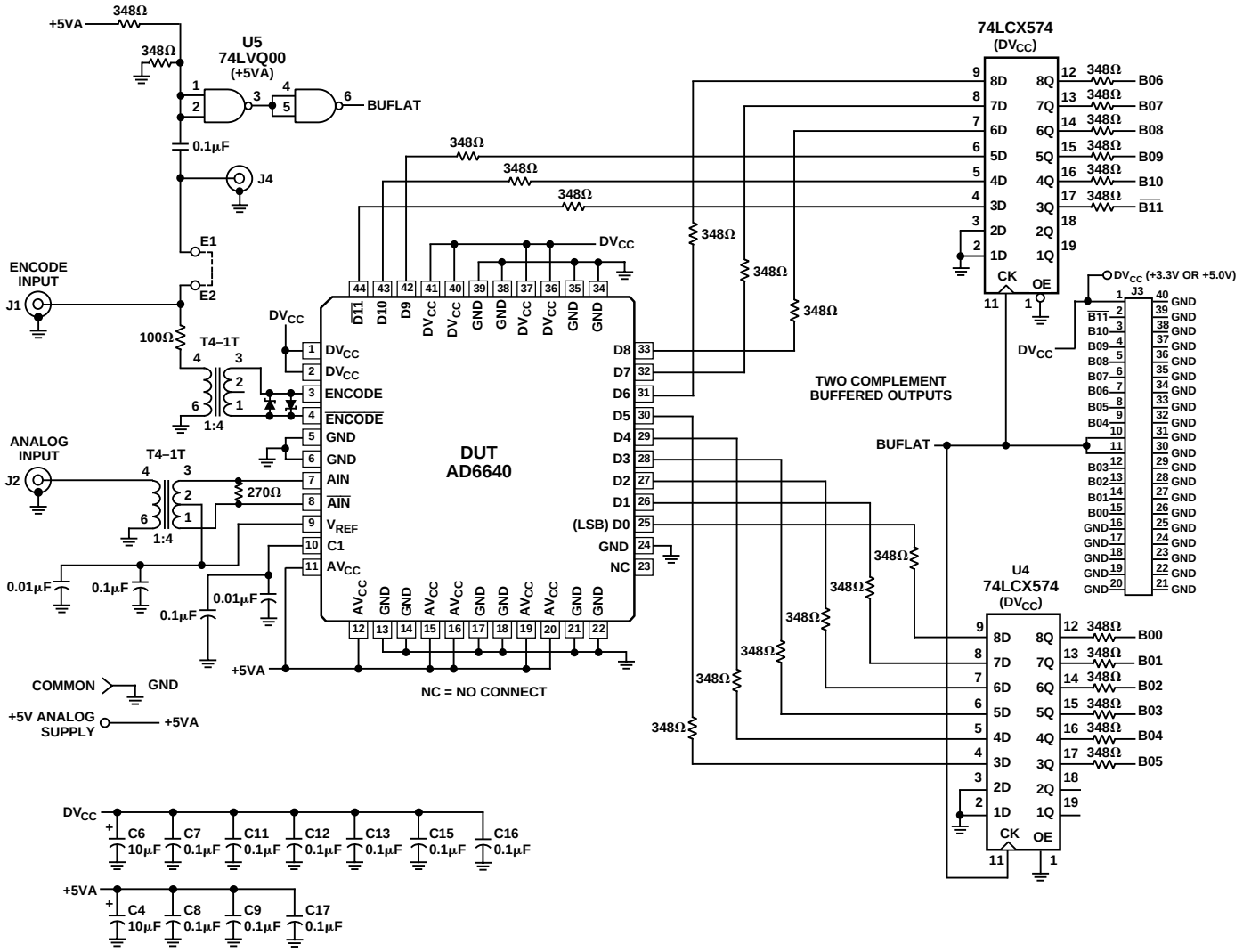


Figure 36. AD6640ST/PCB Schematic

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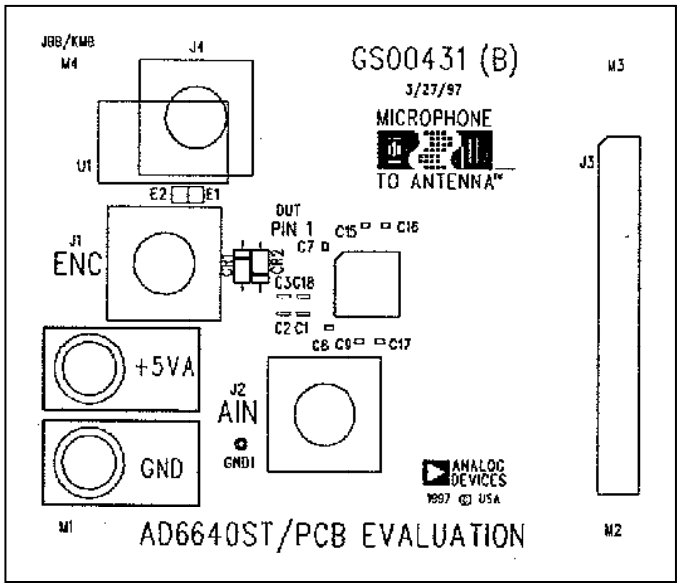


Figure 37. AD6640ST/PCB Top Side Silkscreen

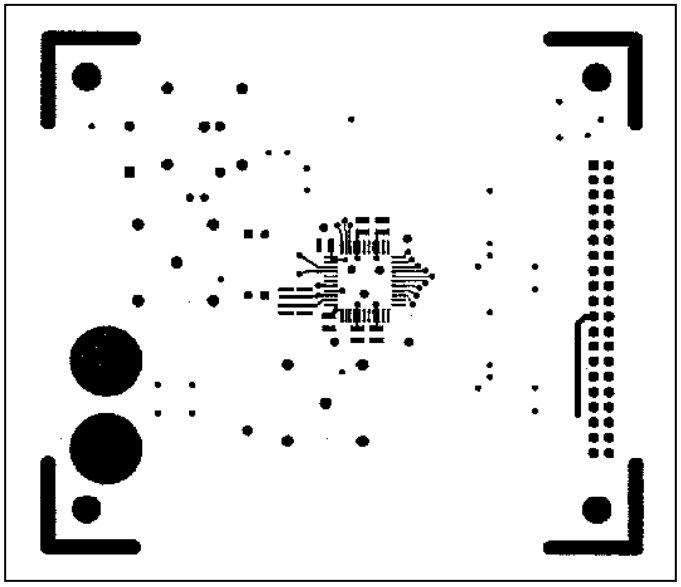


Figure 39. AD6640ST/PCB Top Side Copper

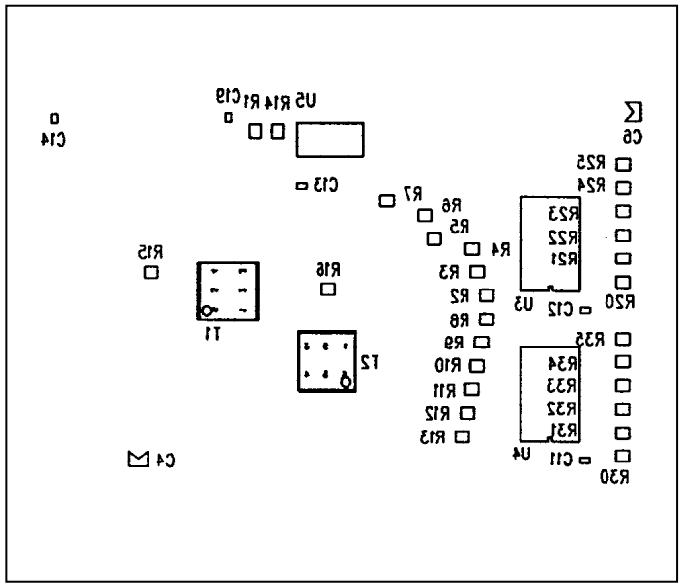


Figure 38. AD6640ST/PCB Bottom Side Silkscreen

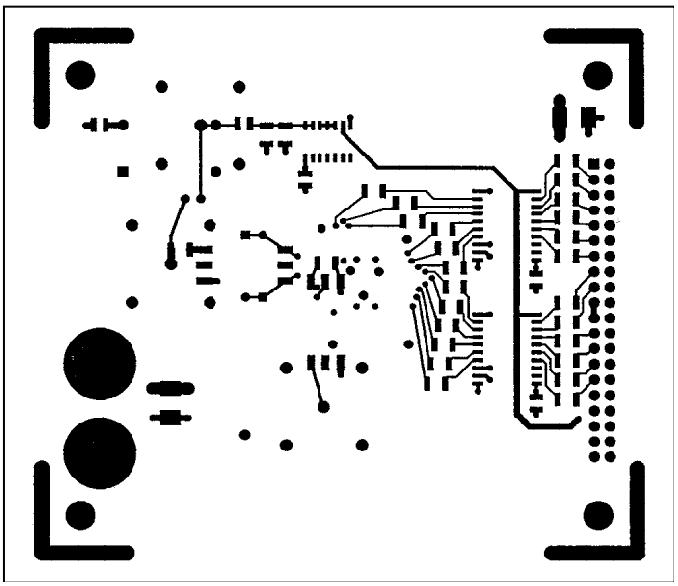


Figure 40. AD6640ST/PCB Bottom Side Copper (Positive)

NOTE: Evaluation boards are often updated, consult factory for latest version.

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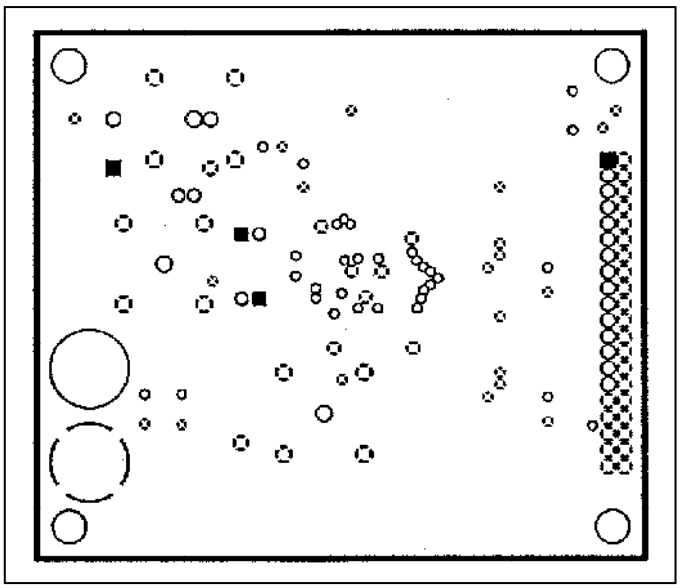


Figure 41. AD6640ST/PCB Ground Layer (Negative)

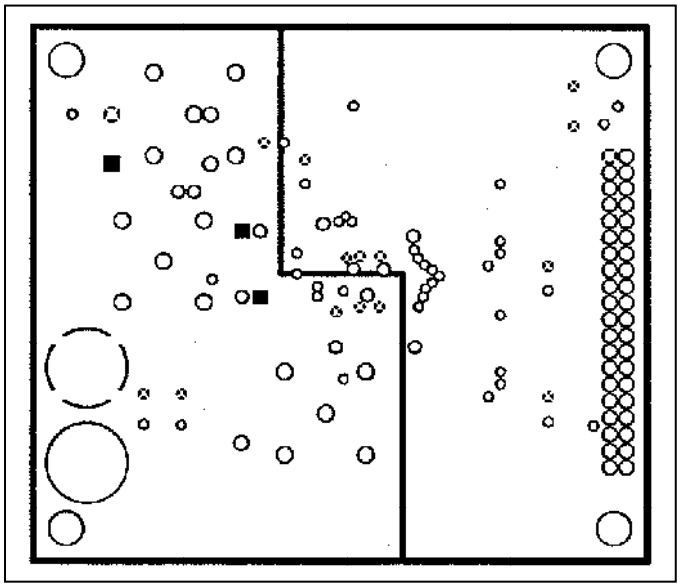


Figure 42. AD6640ST/PCB "Split" Power Layer (Negative)

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DIGITAL WIDEBAND RECEIVERS

Introduction

Several key technologies are now being introduced that may forever alter the vision of radio. Figure 43 shows the typical dual conversion superheterodyne receiver. The signal picked up by the antenna is mixed down to an intermediate frequency (IF) using a mixer with a variable local oscillator (LO); the variable LO is used to "tune-in" the desired signal. This first IF is mixed down to a second IF using another mixer stage and a fixed LO. Demodulation takes place at the second or third IF using either analog or digital techniques.

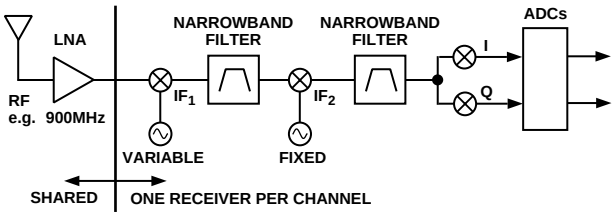


Figure 43. Narrowband Digital Receiver Architecture

If demodulation takes place in the analog domain then traditional discriminators, envelop detectors, phase locked loops or other synchronous detectors are generally employed to strip the modulation from the selected carrier.

However, as general purpose DSP chips such as the ADSP-2181 become more popular, they will be used in many baseband-sampled applications like the one shown in Figure 43. As shown in the figure, prior to ADC conversion, the signal must be mixed down, filtered, and the I and Q components separated. These functions are realizable through DSP techniques, however several key technology breakthroughs are required: high dynamic range ADCs such as the AD6640, new DSPs (highly programmable with onboard memory, fast), digital tuners and filters such as the AD6620, wide band mixers and amplifiers.

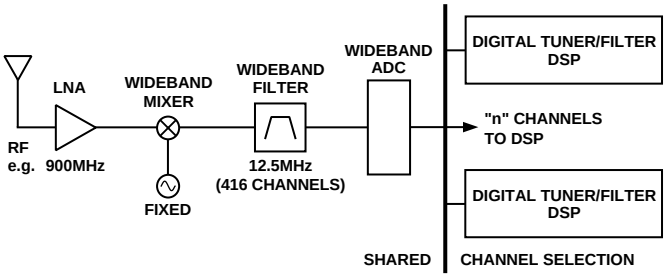


Figure 44. Wideband Digital Receiver Architecture

Figure 44 shows such a wideband system. This design shows that the front end variable local oscillator has been replaced with a fixed oscillator and the back end has been replaced with a wide dynamic range ADC, digital tuner and DSP. This technique offers many benefits.

First, many passive discrete components have been eliminated that formed the tuning and filtering functions. These passive components often require "tweaking" and special handling during assembly and final system alignment. Digital components require no such adjustments; tuner and filter characteristics are always exactly the same. Moreover, the tuning and filtering characteristics can be changed through software. Since software is used for demodulation, different routines may be used to demodulate different standards such as AM, FM, GMSK or any other desired standard. In addition, as new standards arise or new software revisions are generated, they may be field installed with standard software update channels. A radio that performs demodulation in software as opposed to hardware is often referred to as a soft radio because it may be changed or modified simply through code revision.

System Description

In the wideband digital radio (Figure 44), the first down conversion functions in much the same way as a block converter does. An entire band is shifted in frequency to the desired intermediate frequency. In the case of cellular base station receivers, 5 MHz to 30 MHz of bandwidth are down-converted simultaneously to an IF frequency suitable for digitizing with a wideband analog-to-digital converter. Once digitized the broadband digital data stream contains all of the in-band signals. The remainder of the radio is constructed digitally using special purpose and general purpose programmable DSP to perform filtering, demodulation and signal conditioning not unlike the analog counter parts.

In the narrowband receiver (Figure 43), the signal to be received must be tuned. This is accomplished by using a variable local oscillator at the first mix down stage. The first IF then uses a narrow band filter to reject out of band signals and condition the selected carrier for signal demodulation.

In the digital wideband receiver (Figure 44), the variable local oscillator has been replaced with a fixed oscillator, so tuning must be accomplished in another manner. Tuning is performed digitally using a digital down conversion and filter chip frequently called a channelizer. The term channelizer is used because the purpose of these chips is to select one channel out of many within the broadband spectrum present in the digital data stream of the ADC.

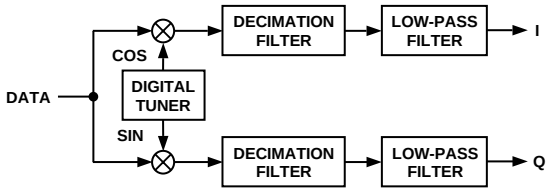


Figure 45. AD6620 Digital Channelizer

Figure 45 shows the block diagram of a typical channelizer, such as the AD6620. Channelizers consist of a complex NCO (Numerically Controlled Oscillator), dual multiplier (mixer), and matched digital filters. These are the same functions that would be required in an analog receiver, however implemented in digital form. The digital output from the channelizer is the desired carrier, frequently in I & Q format; all other signals have been filtered and removed based on the filtering characteristics desired. Since the channelizer output consists of one selected RF channel, one tuner chip is required for each frequency received, although only one wideband RF receiver is needed for the entire band. Data from the channelizer may then be processed using a digital signal processor such as the ADSP-2181 or the SHARC® processor, the ADSP-21062. This data may then be processed through software to demodulate the information from the carrier.

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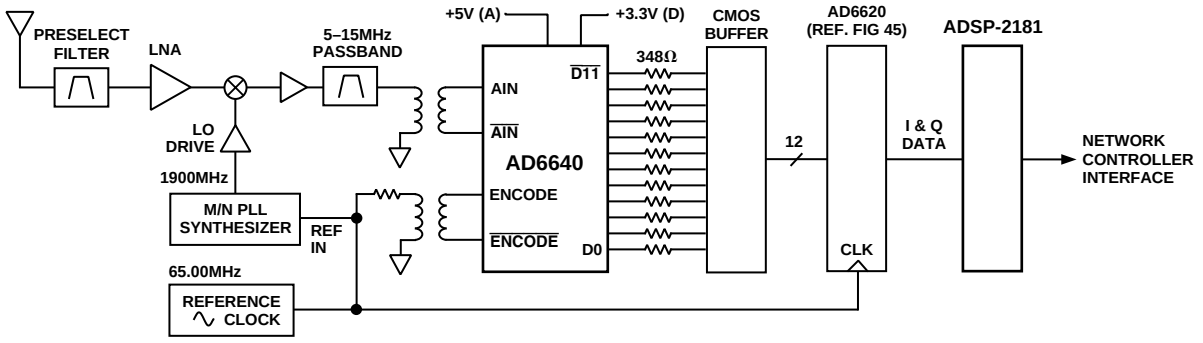


Figure 46. Simplified Wideband PCS Receiver

System Requirements

Figure 46 shows a typical wideband receiver subsystem based around the AD6640. This strip consists of a wideband IF filter, amplifier, ADC, latches, channelizer and interface to a digital signal processor. This design shows a typical clocking scheme used in many receiver designs. All timing within the system is referenced back to a single clock. While this is not necessary, it does facilitate PLL design, ease of manufacturing, system test, and calibration. Keeping in mind that the overall performance goal is to maintain the best possible dynamic range, many considerations must be made.

One of the biggest challenges is selecting the amplifier used to drive the AD6640. Since this is a communications application, it is common to directly sample an intermediate frequency (IF) signal. As such, IF gain blocks can be implemented instead of baseband op amps. For these gain block amplifiers, the critical specifications are third order intercept point and noise figure. A bandpass filter will remove harmonics generated within the amplifier, but intermods should be better than the performance of the A/D converter. In the case of the AD6640, amplifier intermods must be better than –80 dBFS when driving full-scale power. As mentioned earlier, there are several amplifiers to choose from and the specifications depend on the end application. Figure 47 shows a typical multitone test.

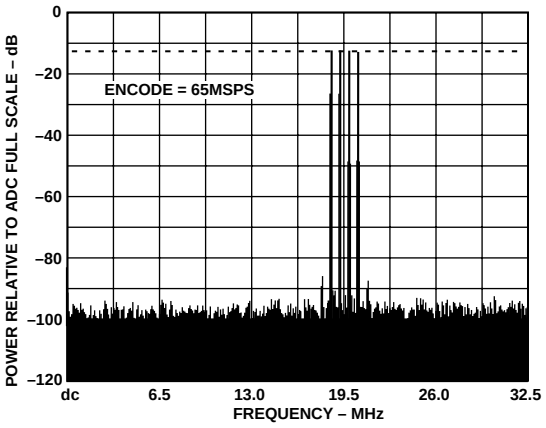


Figure 47. Multitone Performance

Two other key considerations for the digital wideband receiver are converter sample rate and IF frequency range. Since performance of the AD6640 converter is largely independent of both sample rate and analog input frequency (Figures 10, 11 and 16), the designer has greater flexibility in the selection of these parameters. Also, since the AD6640 is a bipolar device, power dissipation is not a function of sample rate. Thus there is no penalty paid in power by operating at faster sample rates. All of this is good because, by carefully selecting input frequency range and sample rate, some of the drive amplifier and ADC harmonics can actually be placed out-of-band.

For example, if the system has second and third harmonics that are unacceptably high, by carefully selecting the encode rate and signal bandwidth, these second and third harmonics can be placed out-of-band. For the case of an encode rate equal to 60 MSPS and a signal bandwidth of 7.5 MHz, placing the fundamental at 7.5 MHz places the second and third harmonics out of band as shown in the table below.

Table II.

Encode Rate	60 MSPS
Fundamental	7.5 MHz–15 MHz
Second Harmonic	15 MHz–30 MHz
Third Harmonic	22.5 MHz–30 MHz, 30 MHz–15 MHz

Another option can be found through bandpass sampling. If the analog input signal range is from dc to FS/2, then the amplifier and filter combination must perform to the specification required. However, if the signal is placed in the third Nyquist zone (FS to 3 FS/2), the amplifier is no longer required to meet the harmonic performance required by the system specifications since all harmonics would fall outside the passband filter. For example, the passband filter would range from FS to 3 FS/2. The second harmonic would span from 2 FS to 3 FS, well outside the passband filter's range. The burden then has been passed off to the filter design provided that the ADC meets the basic specifications at the frequency of interest. In many applications, this is a worthwhile tradeoff since many complex filters can easily be realized using SAW and LCR techniques alike at these relatively high IF frequencies. Although harmonic performance of the drive amplifier is relaxed by this technique, intermodulation performance cannot be sacrificed since intermods must be assumed to fall in-band for both amplifiers and converters.

Noise Floor and SNR

Oversampling is sampling at a rate that is greater than twice the bandwidth of the signal desired. Oversampling does not have anything to do with the actual frequency of the sampled signal, it is the bandwidth of the signal that is key. Bandpass or "IF" sampling refers to sampling a frequency that is higher than Nyquist and often provides additional benefits such as down conversion using the ADC and replacing a mixer with a track-and-hold. Oversampling leads to processing gains because the

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faster the signal is digitized, the wider the distribution of noise. Since the integrated noise must remain constant, the actual noise floor is lowered by 3 dB each time the sample rate is doubled. The effective noise density for an ADC may be calculated by the equation:

$$V_{NOISE\ rms} / \sqrt{Hz} = \frac{10^{-SNR/20}}{\sqrt{4\ FS}}$$

For a typical SNR of 68 dB and a sample rate of 65 MSPS, this is equivalent to 25 nV/$\sqrt{\text{Hz}}$. This equation shows the relationship between SNR of the converter and the sample rate FS. This equation may be used for computational purposes to determine overall receiver noise.

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, the following equation accurately predicts the SNR based on three terms. These are jitter, average DNL error and thermal noise. Each of these terms contributes to the noise within the converter.

Equation 1:

$$SNR = -20 \log\left[\left(2\pi F_{ANALOG}\ \ t_{J\,rms}\right)^2 + \left(\frac{1+\varepsilon}{2^{12}}\right)^2 + \left(\frac{V_{NOISE\ rms}}{2^{12}}\right)^2\right]^{1/2}$$

F_{ANALOG} = analog input frequency

$t_{J\ rms}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry)

ε = average DNL of the ADC (typically 0.51 LSB)

$V_{NOISE\ rms}$ = V rms thermal noise referred to the analog input of the ADC (typically 0.707 LSB)

Processing Gain

Processing gain is the improvement in signal-to-noise ratio (SNR) gained through oversampling and digital filtering. Most of this processing gain is accomplished using the channelizer chips. These special purpose DSP chips not only provide channel selection and filtering but also provide a data rate reduction. The required rate reduction is accomplished through a process called decimation. The term decimation rate is used to indicate the ratio of input data rate to output data rate. For example, if the input data rate is 65 MSPS and the output data rate is 1.25 MSPS, then the decimation rate is 52.

Large processing gains may be achieved in the decimation and filtering process. The purpose of the channelizer, beyond tuning, is to provide the narrowband filtering and selectivity that traditionally has been provided by the ceramic or crystal filters of a narrowband receiver. This narrowband filtering is the source of the processing gain associated with a wideband receiver and is simply the ratio of the passband to whole band expressed in dB. For example, if a 30 kHz AMPS signal is being digitized with an AD6640 sampling at 65 MSPS, the ratio would be 0.015 *MHz*/32.5 *MHz*. Expressed in log form, the processing gain is –10 × log (0.015 *MHz*/32.5 *MHz*) or 33.4 dB.

Additional filtering and noise reduction techniques can be achieved through DSP techniques; many applications do use additional process gains through proprietary noise reduction algorithms.

Overcoming Static Nonlinearities with Dither

Typically, high resolution data converters use multistage techniques to achieve high bit resolution without large comparator arrays that would be required if traditional "flash" ADC techniques were employed. The multistage converter typically provides better wafer yields meaning lower cost and much lower power. However, since it is a multistage device, certain portions of the circuit are used repetitively as the analog input sweeps from one end of the converter range to the other. Although the worst DNL error may be less than an LSB, the repetitive nature of the transfer function can play havoc with low level dynamic signals. Spurious signals for a full-scale input may be –80 dBc. However at 36 dB below full scale, these repetitive DNL errors may cause spurious-free dynamic range (SFDR) to fall below 80 dBFS as shown in Figure 20.

A common technique for randomizing and reducing the effects of repetitive static linearity is through the use of dither. The purpose of dither is to force the repetitive nature of static linearity to appear as if it were random. Then, the average linearity over the range of dither will dominate SFDR performance. In the AD6640, the repetitive cycle is every 15.625 mV p-p.

To ensure adequate randomization, 5.3 mV rms is required; this equates to a total dither power of –32.5 dBm. This will randomize the DNL errors over the complete range of the residue converter. Although lower levels of dither such as that from previous analog stages will reduce some of the linearity errors, the full effect will only be gained with this larger dither. Increasing dither even more may be used to reduce some of the global INL errors. However, signals much larger than the mVs proposed here begin to reduce the usable dynamic range of the converter.

Even with the 5.3 mV rms of noise suggested, SNR would be limited to 36 dB if injected as broadband noise. To avoid this problem, noise may be injected as an out-of-band signal. Typically, this may be around dc but may just as well be at FS/2 or at some other frequency not used by the receiver. The bandwidth of the noise is several hundred kilohertz. By band-limiting and controlling its location in frequency, large levels of dither may be introduced into the receiver without seriously disrupting receiver performance. The result can be a marked improvement in the SFDR of the data converter.

Figure 23 shows the same converter shown earlier but with this injection of dither (reference Figure 20).

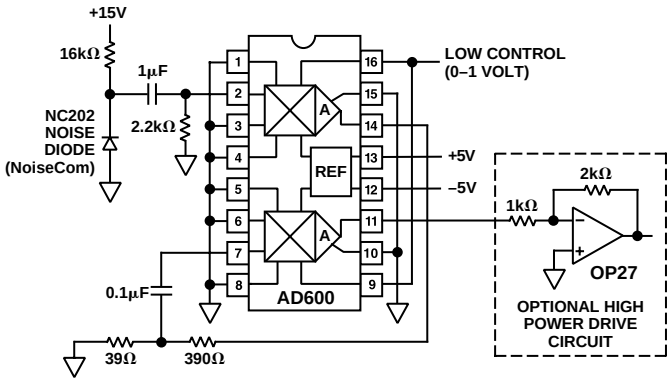


Figure 48. Noise Source (Dither Generator)

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The simplest method for generating dither is through the use of a noise diode (Figure 48). In this circuit, the noise diode NC202 generates the reference noise that is gained up and driven by the AD600 and OP27 amplifier chain. The level of noise may be controlled by either presetting the control voltage when the system is set up, or by using a digital-to-analog converter (DAC) to adjust the noise level based on input signal conditions. Once generated, the signal must be introduced to the receiver strip. The easiest method is to inject the signal into the drive chain after the last down conversion as shown in Figure 49.

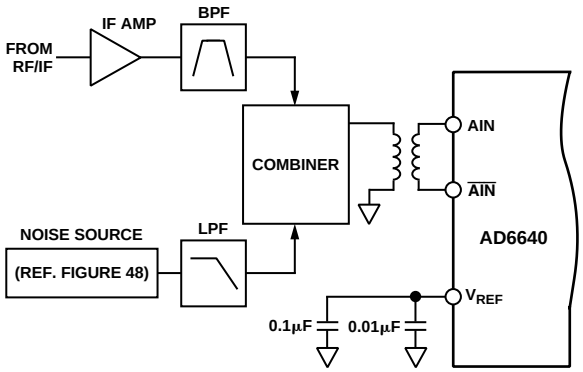


Figure 49. Using the AD6640 with Dither

Receiver Example

To determine how the ADC performance relates to overall receiver sensitivity, the simple receiver in Figure 50 will be examined. This example assumes that the overall down conversion process can be grouped into one set of specifications, instead of individually examining all components within the system and summing them together. Although a more detailed analysis should be employed in a real design, this model will provide a good approximation.

In examining a wideband digital receiver, several considerations must be applied. Although other specifications are important, receiver sensitivity determines the absolute limits of a radio excluding the effects of other outside influences. Assuming that receiver sensitivity is limited by noise and not adjacent signal strength, several sources of noise can be identified and their overall contribution to receiver sensitivity calculated.

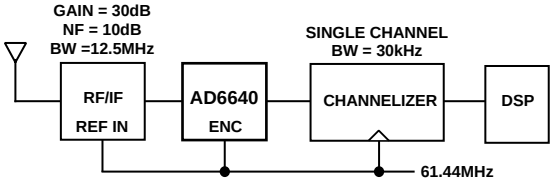


Figure 50. Receiver Analysis

The first noise calculation to make is based on the signal bandwidth at the antenna. In a typical broadband cellular receiver, the IF bandwidth is 12.5 MHz. Given that the power of noise in a given bandwidth is defined by $P_n = kTB$, where B is bandwidth, $k = 1.38 \times 10^{-23}$ is Boltzman's constant and $T = 300k$ is absolute temperature, this gives an input noise power of 5.18×10^{-14} watts or –102.86 dBm. If our receiver front end has a gain of 30 dB and a noise figure of 10 dB, then the total noise presented to the ADC input becomes –62.86 dBm (–102.86 + 30 + 10) or 0.16 mV rms. Comparing receiver noise to dither required for good SFDR, we see that in this example, our receiver supplies about 3% of the dither required for good SFDR.

Based on a typical ADC SNR specification of 68 dB, the equivalent internal converter noise is 0.140 mV rms. Therefore total broadband noise is 0.21 mV rms. Before processing gain, this is an equivalent SNR (with respect to full scale) of 64.5 dB. Assuming a 30 kHz AMPS signal and a sample rate of 61.44 MSPS, the SNR through processing gain is increased by approximately 33 dB to 97.5 dB. However, if eight strong and equal signals are present in the ADC bandwidth, then each must be placed 18 dB below full scale to prevent ADC overdrive. Therefore we give away 18 dB of range and reduce the carrier-to-noise ratio (C/N) to 79.5 dB.

Assuming that the C/N ratio must be 10 dB or better for accurate demodulation, one of the eight signals may be reduced by 66.5 dB before demodulation becomes unreliable. At this point, the input signal power would be –90.5 dBm. Referenced to the antenna, this is –120.5 dBm.

To improve sensitivity, several things can be done. First, the noise figure of the receiver can be reduced. Since front end noise dominates the 0.16 mV rms, each dB reduction in noise figure translates to an additional dB of sensitivity. Second, providing broadband AGC can improve sensitivity by the range of the AGC. However, the AGC would only provide useful improvements if all in-band signals are kept to an absolute minimal power level so that AGC can be kept near the maximum gain.

This noise limited example does not adequately demonstrate the true limitations in a wideband receiver. Other limitations such as SFDR are more restrictive than SNR and noise. Assume that the analog-to-digital converter has an SFDR specification of –80 dBFS or –76 dBm (Full scale = +4 dBm). Also assume that a tolerable carrier-to-interferer (C/I) (different from C/N) ratio is 18 dB. This means that the minimum signal level is –62 dBFS (–80 plus 18) or –58 dBm. At the antenna, this is –88 dBm. Therefore, as can be seen, SFDR (single or multitone) would limit receiver performance in this example. However, as shown previously, SFDR can be greatly improved through the use of dither (Figures 19, 22). In many cases, the addition of the out-of-band dither can improve receiver sensitivity nearly to that limited by thermal noise.

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IF Sampling, Using the AD6640 as a Mix-Down Stage

Since performance of the AD6640 extends beyond the baseband region into the third Nyquist zone, the converter has many uses as a mix-down converter in both narrowband and wideband applications. This application is called bandpass sampling. Doing this has several positive implications in terms of the selection of the IF drive amplifier. Not only is filtering a bit easier, the selection of drive amplifiers is extended to classical IF gain blocks. In the third Nyquist zone and above, the second and third harmonics are easily filtered with a bandpass filter. Now only in-band spurs that result from third order products are important.

In narrowband applications, harmonics of the ADC can be placed out-of-band. One example is the digitization of a 201 MHz IF signal using a 17.333 MHz clock. As shown in Figure 51, the spurious performance has diminished due to internal slew rate limitations of the ADC. However, the SNR of the converter is still quite good. Subsequent digital filtering with a channelizer chip such as the AD6620 will yield even better SNR.

For multicarrier applications, third order intercept of the drive amplifier is important. If the input network is matched to the internal 900 ohm input impedance, the required full-scale drive level is –3 dBm. If spurious products delivered to the ADC are required to be below –90 dBFS, the typical performance of the ADC with dither applied, then the required third order intercept point for the drive amplifier can be calculated.

For multicarrier applications, the AD6640 is useful up to about 80 MHz analog in. For single channel applications, the AD6640 is useful to 200 MHz as shown from the bandwidth charts. In either case, many common IF frequencies exist in this range of frequencies. If the ADC is used to sample these signals, they will be aliased down to baseband during the sampling process in much the same manner that a mixer will down-convert a signal. For signals in various Nyquist zones, the following equations may be used to determine the final frequency after aliasing.

$$f_{1NYQUISTS} = f_{SAMPLE} - f_{SIGNAL}$$
$$f_{2NYQUISTS} = abs\,(f_{SAMPLE} - f_{SIGNAL})$$
$$f_{3NYQUISTS} = 2 \times f_{SAMPLE} - f_{SIGNAL}$$
$$f_{4NYQUISTS} = abs\,(2 \times f_{SAMPLE} - f_{SIGNAL})$$

Using the converter to alias down these narrowband or wideband signals has many potential benefits. First and foremost is the elimination of a complete mixer stage along with amplifiers, filters and other devices, reducing cost and power dissipation. In some cases, the elimination of two IF stages is possible.

Figures 21 and 24 in Typical Performance Characteristics illustrate a multicarrier, IF Sampling System. By using dither, all spurious components are forced below 90 dBFS (Figure 24). The dashed line illustrates how a 5 MHz bandpass filter could be centered at 67.5 MHz. As discussed earlier, this approach greatly reduces the size and complexity of the receiver's RF/IF section.

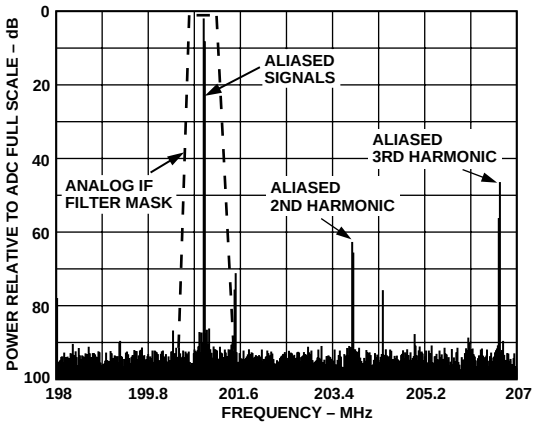


Figure 51. IF-Sampling a 201 MHz Input

RECEIVE CHAIN FOR A PHASED ARRAY CELLULAR BASE STATION

The AD6640 is an excellent digitizer for beam forming in phased array antenna systems. The price performance of the AD6640 followed by AD6620 channelizers allows for a very competitive solution. Phase array base stations allow better coverage by focusing the receivers' sensitivity in the direction needed. Phased array systems allow for the electronic beam to form on the receive antennas.

A typical phased array system may have eight antennas as shown in Figure 52. Since a typical base station will handle 32 calls, each antenna would have to be connected to 32 receivers. If done with analog or traditional radios, the system grows quite rapidly. With a multicarrier receiver, however, the design is quite compact. Each antenna will have a wideband down-converter with one AD6640 per receiver. The output of each AD6640 would drive 32 AD6620 channelizers, which are phase locked in groups of eight—one per antenna. This allows each group of eight AD6620's to tune and lock onto a different user. When the incoming signal direction is determined, the relative phase of each AD6620 in the group can be adjusted such the output signals sum together in a constructive manner, giving high gain and directivity in the direction of the caller. This application would not be possible with traditional receiver designs.

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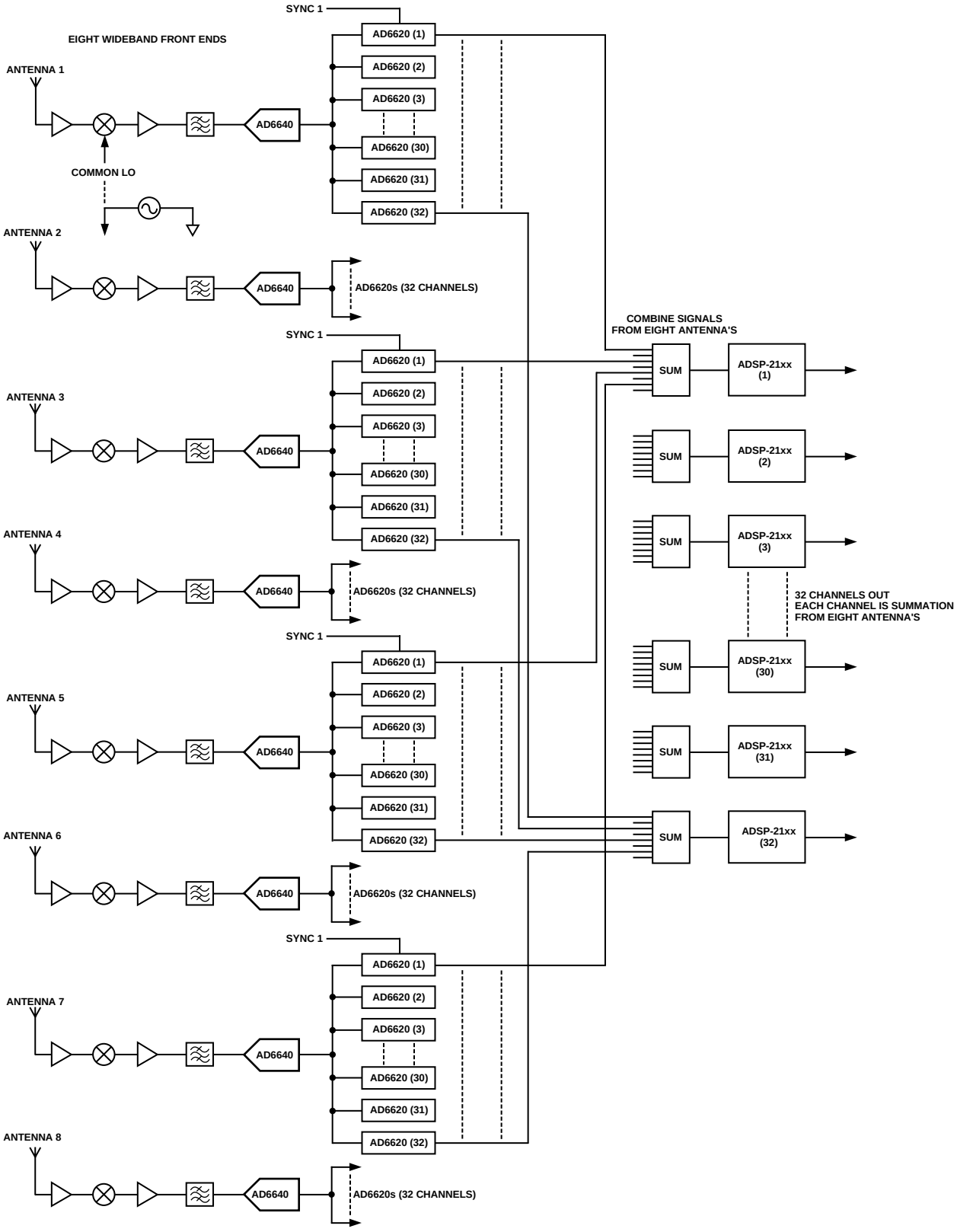


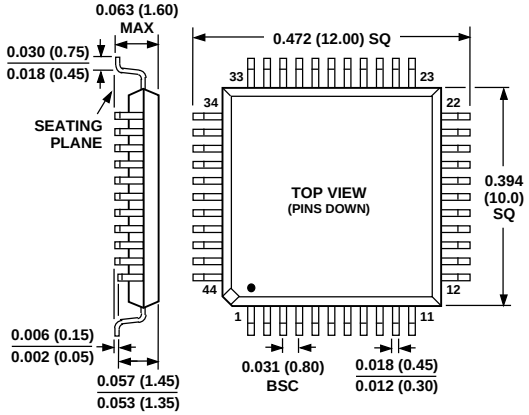
Figure 52. Receive Chain for a Phased Array Cellular Base Station with Eight Antennas and 32 Channels

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AD6640AST OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

44-Terminal Plastic Thin Quad Flatpack (ST-44)



C3141–8–1/98

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Appendix C: Analog Devices AD603 – Variable Gain Amplifier

Included for your reference on the following pages is the data sheet for the AD603 Variable Gain Amplifier, provided by the courtesy of Analog Devices Inc., Norwood, MA.

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Low Noise, 90 MHz Variable-Gain Amplifier

AD603*

FEATURES
"Linear in dB" Gain Control
Pin Programmable Gain Ranges
–11 dB to +31 dB with 90 MHz Bandwidth
9 dB to 51 dB with 9 MHz Bandwidth
Any Intermediate Range, e.g., –1 dB to +41 dB with 30 MHz Bandwidth
Bandwidth Independent of Variable Gain
1.3 nV/√Hz Input Noise Spectral Density
±0.5 dB Typical Gain Accuracy
MIL-STD-883 Compliant and DESC Versions Available

APPLICATIONS
RF/IF AGC Amplifier
Video Gain Control
A/D Range Extension
Signal Measurement

PRODUCT DESCRIPTION

The AD603 is a low noise, voltage-controlled amplifier for use in RF and IF AGC systems. It provides accurate, pin selectable gains of –11 dB to +31 dB with a bandwidth of 90 MHz or 9 dB to 51 dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor. The input referred noise spectral density is only 1.3 nV/√Hz and power consumption is 125 mW at the recommended ±5 V supplies.

The decibel gain is "linear in dB," accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain-control voltage of only 1 V to span the central 40 dB of the gain range. An over- and underrange of 1 dB is provided whatever the selected range. The gain-control response time is less than 1 µs for a 40 dB change.

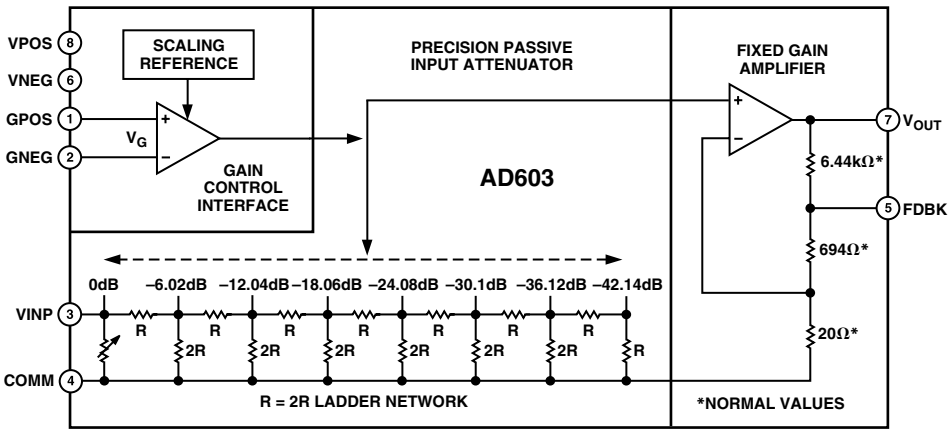
The differential gain-control interface allows the use of either differential or single-ended positive or negative control voltages. Several of these amplifiers may be cascaded and their gain-control gains offset to optimize the system S/N ratio.

The AD603 can drive a load impedance as low as 100 Ω with low distortion. For a 500 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically –60 dBc. The peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load.

The AD603 uses a proprietary circuit topology—the X-AMP™. The X-AMP comprises a variable attenuator of 0 dB to –42.14 dB followed by a fixed-gain amplifier. Because of the attenuator, the amplifier never has to cope with large inputs and can use negative feedback to define its (fixed) gain and dynamic performance. The attenuator has an input resistance of 100 Ω, laser trimmed to ±3%, and comprises a seven-stage R-2R ladder network, resulting in an attenuation between tap points of 6.021 dB. A proprietary interpolation technique provides a continuous gain-control function which is linear in dB.

The AD603A is specified for operation from –40°C to +85°C and is available in both 8-lead SOIC (R) and 8-lead ceramic DIP (Q). The AD603S is specified for operation from –55°C to +125°C and is available in an 8-lead ceramic DIP (Q). The AD603 is also available under DESC SMD 5962-94572.

FUNCTIONAL BLOCK DIAGRAM



*Patented.
X-AMP is a trademark of Analog Devices, Inc.

REV. D

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AD603—SPECIFICATIONS (@ T_A = 25°C, V_S = ±5 V, –500 mV ≤ V_G ≤ +500 mV, GNEG = 0 V, –10 dB to +30 dB Gain Range, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted.)

Model / Parameter	Conditions	AD603 Min	AD603 Typ	AD603 Max	Unit
INPUT CHARACTERISTICS					
Input Resistance	Pins 3 to 4	97	100	**103**	Ω
Input Capacitance			2		pF
Input Noise Spectral Density[1]	Input Short Circuited		1.3		nV/√Hz
Noise Figure	f = 10 MHz, Gain = max, R_S = 10 Ω		8.8		dB
1 dB Compression Point	f = 10 MHz, Gain = max, R_S = 10 Ω		–11		dBm
Peak Input Voltage			±1.4	±2	V
OUTPUT CHARACTERISTICS					
–3 dB Bandwidth	V_{OUT} = 100 mV rms		90		MHz
Slew Rate	R_L ≥ 500 Ω		275		V/µs
Peak Output[2]	R_L ≥ 500 Ω	±2.5	±3.0		V
Output Impedance	f ≤ 10 MHz		2		Ω
Output Short-Circuit Current			50		mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 MHz to 10 MHz		±2		ns
Differential Gain			0.2		%
Differential Phase			0.2		Degree
Total Harmonic Distortion	f = 10 MHz, V_{OUT} = 1 V rms		–60		dBc
3rd Order Intercept	f = 40 MHz, Gain = max, R_S = 50 Ω		15		dBm
ACCURACY					
Gain Accuracy	–500 mV ≤ V_G ≤ +500 mV		±0.5	**±1**	dB
T_{MIN} to T_{MAX}				±1.5	dB
Output Offset Voltage[3]	V_G = 0 V			**20**	mV
T_{MIN} to T_{MAX}				30	mV
Output Offset Variation vs. V_G	–500 mV ≤ V_G ≤ +500 mV			**20**	mV
T_{MIN} to T_{MAX}				30	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor		**39.4**	40	**40.6**	dB/V
T_{MIN} to T_{MAX}		38		42	dB/V
GNEG, GPOS Voltage Range[4]		–1.2		**+2.0**	V
Input Bias Current			200		nA
Input Offset Current			10		nA
Differential Input Resistance	Pins 1 to 2		50		MΩ
Response Rate	Full 40 dB Gain Change		40		dB/µs
POWER SUPPLY					
Specified Operating Range		±4.75		±6.3	V
Quiescent Current			12.5	**17**	mA
T_{MIN} to T_{MAX}				20	mA

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD603 is ×35.7; thus, an input offset of 100 µV becomes a 3.57 mV output offset.

[4]GNEG and GPOS, gain control, voltage range is guaranteed to be within the range of $-V_S$ + 4.2 V to $+V_S$ – 3.4 V over the full temperature range of –40°C to +85°C.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

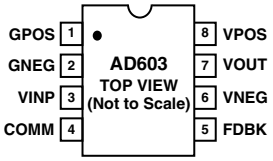
Supply Voltage $\pm V_S$ . . . . . ±7.5 V
Internal Voltage VINP (Pin 3) . . . . . ±2 V Continuous
. . . . . $\pm V_S$ for 10 ms
GPOS, GNEG (Pins 1, 2) . . . . . $\pm V_S$
Internal Power Dissipation[2] . . . . . 400 mW
Operating Temperature Range
AD603A . . . . . −40°C to +85°C
AD603S . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Lead SOIC Package: θ_{JA} = 155°C/W, θ_{JC} = 33°C/W
8-Lead Ceramic Package: θ_{JA} = 140°C/W, θ_{JC} = 15°C/W

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	GPOS	Gain-Control Input "HI" (Positive Voltage Increases Gain)
2	GNEG	Gain-Control Input "LO" (Negative Voltage Increases Gain)
3	VINP	Amplifier Input
4	COMM	Amplifier Ground
5	FDBK	Connection to Feedback Network
6	VNEG	Negative Supply Input
7	VOUT	Amplifier Output
8	VPOS	Positive Supply Input

CONNECTION DIAGRAMS
8-Lead Plastic SOIC (R) Package
8-Lead Ceramic DIP (Q) Package



ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
AD603AR	−40°C to +85°C	8-Lead SOIC	SO-8
AD603AQ	−40°C to +85°C	8-Lead Ceramic DIP	Q-8
AD603SQ/883B*	−55°C to +125°C	8-Lead Ceramic DIP	Q-8
AD603-EB		Evaluation Board	
AD603ACHIPS	−40°C to +85°C	Die	
AD603AR-REEL	−40°C to +85°C	13" Reel	SO-8
AD603AR-REEL7	−40°C to +85°C	7" Reel	SO-8

*Refer to AD603 Military data sheet. Also available as 5962-9457203MPA.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD603 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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THEORY OF OPERATION

The AD603 comprises a fixed-gain amplifier, preceded by a broadband passive attenuator of 0 dB to 42.14 dB, having a gain-control scaling factor of 40 dB per volt. The fixed gain is laser-trimmed in two ranges, to either 31.07 dB (×35.8) or 50 dB (×358), or may be set to any range in between using one external resistor between Pins 5 and 7. Somewhat higher gain can be obtained by connecting the resistor from Pin 5 to common, but the increase in output offset voltage limits the maximum gain to about 60 dB. For any given range, the bandwidth is independent of the voltage-controlled gain. This system provides an under- and overrange of 1.07 dB in all cases; for example, the overall gain is –11.07 dB to 31.07 dB in the maximum-bandwidth mode (Pin 5 and Pin 7 strapped).

This *X-AMP* structure has many advantages over former methods of gain-control based on nonlinear elements. Most importantly, the fixed-gain amplifier can use negative feedback to increase its accuracy. Since large inputs are first attenuated, the amplifier input is always small. For example, to deliver a ±1 V output in the –1 dB/+41 dB mode (that is, using a fixed amplifier gain of 41.07 dB) its input is only 8.84 mV; thus the distortion can be very low. Equally important, the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

Figure 1 is a simplified schematic. The input attenuator is a seven-section R-2R ladder network, using untrimmed resistors of nominally R = 62.5 Ω, which results in a characteristic resistance of 125 Ω ± 20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ± 3%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

The nominal maximum signal at input VINP is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies, although operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. *Pin 4 (SIGNAL COMMON) must be connected directly to the input ground; significant impedance in this connection will reduce the gain accuracy.*

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; thus, the attenuation to each of the taps is progressively 0 dB, 6.02 dB, 12.04 dB, 18.06 dB, 24.08 dB, 30.1 dB, 36.12 dB and 42.14 dB. A unique circuit technique is employed to interpolate between these tap-points, indicated by the "slider" in Figure 1, thus providing continuous attenuation from 0 dB to 42.14 dB. It will help, in understanding the AD603, to think in terms of a mechanical means for moving this slider from left to right; in fact, its "position" is controlled by the voltage between Pins 1 and 2. The details of the gain-control interface are discussed later.

The gain is at all times very exactly determined, and a linear-in-dB relationship is automatically guaranteed by the exponential nature of the attenuation in the ladder network (the X-AMP principle). In practice, the gain deviates slightly from the ideal law, by about ±0.2 dB peak (see, for example, Figure 16).

Noise Performance

An important advantage of the X-AMP is its superior noise performance. The nominal resistance seen at inner tap points is 41.7 Ω (one third of 125 Ω), which exhibits a Johnson noise-spectral density (NSD) of 0.83 nV/√Hz (that is, $\sqrt{4kTR}$) at 27°C, which is a large fraction of the total input noise. The first stage of the amplifier contributes a further 1 nV/√Hz, for a total input noise of 1.3 nV/√Hz. It will be apparent that it is essential to use a low resistance in the ladder network to achieve the very low specified noise level. The signal's source impedance forms a voltage divider with the AD603's 100 Ω input resistance. In some applications, the resulting attenuation may be unacceptable, requiring the use of an external buffer or preamplifier to match a high impedance source to the low impedance AD603.

The noise at maximum gain (that is, at the 0 dB tap) depends on whether the input is short-circuited or open-circuited: when shorted, the minimum NSD of slightly over 1 nV/√Hz is achieved; when open, the resistance of 100 Ω looking into the first tap generates 1.29 nV/√Hz, so the noise increases to a total of 1.63 nV/√Hz. (This last calculation would be important if the AD603 were preceded by, for example, a 900 Ω resistor to allow operation from inputs up to 10 V rms.) As the selected tap moves away from the input, the dependence of the noise on source impedance quickly diminishes.

Apart from the small variations just discussed, the signal-to-noise (S/N) ratio at the output is essentially independent of the attenuator setting. For example, on the –11 dB/+31 dB range the fixed gain of ×35.8 raises the output NSD to 46.5 nV/√Hz. Thus, for the maximum undistorted output of 1 V rms and a 1 MHz bandwidth, the output S/N ratio would be 86.6 dB, that is, 20 log (1 V/46.5 μV).

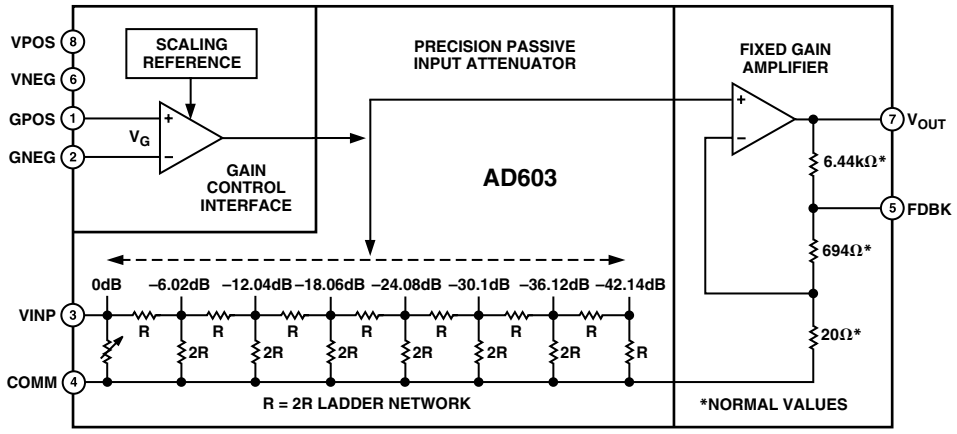


Figure 1. Simplified Block Diagram of the AD603

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The Gain-Control Interface

The attenuation is controlled through a differential, high-impedance (50 MΩ) input, with a scaling factor which is laser-trimmed to 40 dB per volt, that is, 25 mV/dB. An internal bandgap reference ensures stability of the scaling with respect to supply and temperature variations.

When the differential input voltage V_G = 0 V, the attenuator "slider" is centered, providing an attenuation of 21.07 dB. For the maximum bandwidth range, this results in an overall gain of 10 dB (= –21.07 dB + 31.07 dB). When the control input is –500 mV, the gain is lowered by 20 dB (= 0.500 V × 40 dB/V), to –10 dB; when set to +500 mV, the gain is increased by 20 dB, to 30 dB. When this interface is overdriven in either direction, the gain approaches either –11.07 dB (= –42.14 dB + 31.07 dB) or 31.07 dB (= 0 + 31.07 dB), respectively. The only constraint on the gain-control voltage is that it be kept within the common-mode range (–1.2 V to +2.0 V assuming +5 V supplies) of the gain control interface.

The basic gain of the AD603 can thus be calculated using the following simple expression:

$$Gain\ (dB) = 40\ V_G + 10 \quad (1)$$

where V_G is in volts. When Pins 5 and 7 are strapped (see next section) the gain becomes

$$Gain\ (dB) = 40\ V_G + 20\ for\ 0\ to\ +40\ dB$$

and

$$Gain\ (dB) = 40\ V_G + 30\ for\ +10\ to\ +50\ dB \quad (2)$$

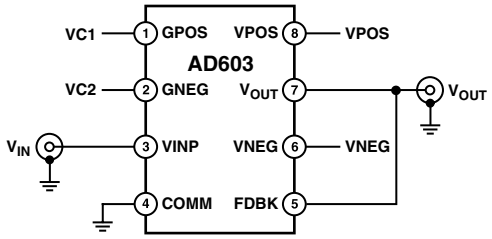
The high impedance gain-control input ensures minimal loading when driving many amplifiers in multiple channel or cascaded applications. The differential capability provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, if the gain is to be controlled by a DAC providing a positive only ground-referenced output, the "Gain Control LO" (GNEG) pin should be biased to a fixed offset of 500 mV, to set the gain to –10 dB when "Gain Control HI" (GPOS) is at zero, and to 30 dB when at 1.00 V.

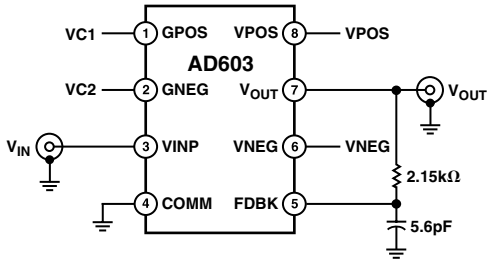
It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC having an FS output of 2.55 V (10 mV/bit), a divider ratio of 2 (generating 5 mV/bit) would result in a gain-setting resolution of 0.2 dB/bit. The use of such offsets is valuable when two AD603s are cascaded, when various options exist for optimizing the S/N profile, as will be shown later.

Programming the Fixed-Gain Amplifier Using Pin Strapping

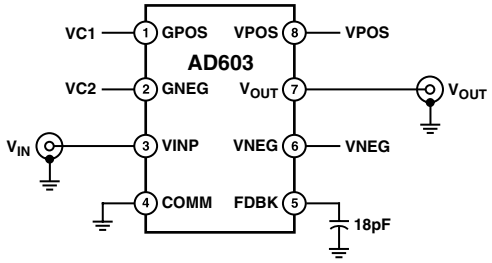
Access to the feedback network is provided at Pin 5 (FDBK). The user may program the gain of the AD603's output amplifier using this pin, as shown in Figure 2. There are three modes: in the default mode, FDBK is unconnected, providing the range +9 dB/+51 dB; when V_{OUT} and FDBK are shorted, the gain is lowered to –11 dB/+31 dB; when an external resistor is placed between V_{OUT} and FDBK any intermediate gain can be achieved, for example, –1 dB/+41 dB. Figure 3 shows the nominal maximum gain versus external resistor for this mode.



a. –10 dB to +30 dB; 90 MHz Bandwidth



b. 0 dB to +40 dB; 30 MHz Bandwidth



c. 10 dB to 50 dB; 9 MHz Bandwidth

Figure 2. Pin Strapping to Set Gain

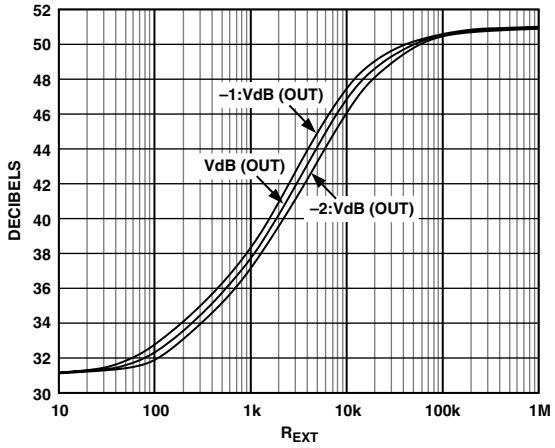


Figure 3. Gain vs. R_{EXT}, Showing Worst-Case Limits Assuming Internal Resistors Have a Maximum Tolerance of 20%

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Optionally, when a resistor is placed from FDBK to COMM, higher gains can be achieved. This fourth mode is of limited value because of the low bandwidth and the elevated output offsets; it is thus not included in Figure 2.

The gain of this amplifier in the first two modes is set by the ratio of on-chip laser-trimmed resistors. While the ratio of these resistors is very accurate, the absolute value of these resistors can vary by as much as ±20%. Thus, when an external resistor is connected in parallel with the nominal 6.44 kΩ ± 20% internal resistor, the overall gain accuracy is somewhat poorer. The worst-case error occurs at about 2 kΩ (see Figure 4).

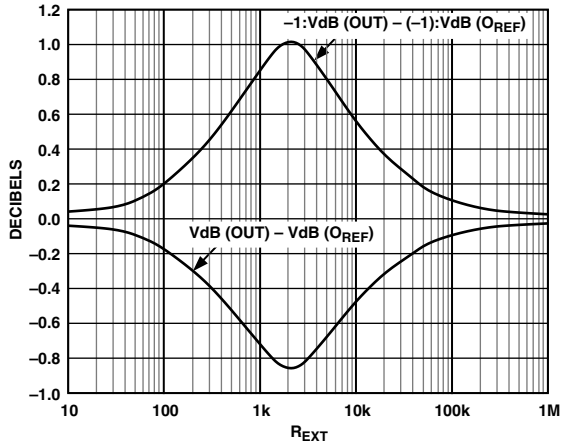


Figure 4. Worst-Case Gain Error, Assuming Internal Resistors Have a Maximum Tolerance of –20% (Top Curve) or +20% (Bottom Curve)

While the gain-bandwidth product of the fixed-gain amplifier is about 4 GHz, the actual bandwidth is not exactly related to the maximum gain. This is because there is a slight enhancing of the ac response magnitude on the maximum bandwidth range, due to higher order poles in the open-loop gain function; this mild peaking is not present on the higher gain ranges. Figure 2 shows how optional capacitors may be added to extend the frequency response in high gain modes.

CASCADING TWO AD603S

Two or more AD603s can be connected in series to achieve higher gain. Invariably, ac coupling must be used to prevent the dc offset voltage at the output of each amplifier from overloading the following amplifier at maximum gain. The required high pass coupling network will usually be just a capacitor, chosen to set the desired corner frequency in conjunction with the well-defined 100 Ω input resistance of the following amplifier.

For two AD603s, the total gain-control range becomes 84 dB (two times 42.14 dB); the overall –3 dB bandwidth of cascaded stages will be somewhat reduced. Depending on the pin-strapping, the gain and bandwidth for two cascaded amplifiers can range from –22 dB to +62 dB (with a bandwidth of about 70 MHz) to +22 dB to +102 dB (with a bandwidth of about 6 MHz).

There are several ways of connecting the gain-control inputs in cascaded operation. The choice depends on whether it is important to achieve the highest possible Instantaneous Signal-to-Noise Ratio (ISNR), or, alternatively, to minimize the ripple in the gain error. The following examples feature the AD603 programmed for maximum bandwidth; the explanations apply to other gain/bandwidth combinations with appropriate changes to the arrangements for setting the maximum gain.

Sequential Mode (Optimal S/N Ratio)

In the sequential mode of operation, the ISNR is maintained at its highest level for as much of the gain control range possible. Figure 5 shows the SNR over a gain range of –22 dB to +62 dB, assuming an output of 1 V rms and a 1 MHz bandwidth; Figure 6 shows the general connections to accomplish this. Here, both the positive gain-control inputs (GPOS) are driven in parallel by a positive-only, ground-referenced source with a range of 0 V to +2 V, while the negative gain-control inputs (GNEG) arc biased by stable voltages to provide the needed gain-offsets. These voltages may be provided by resistive dividers operating from a common voltage reference.

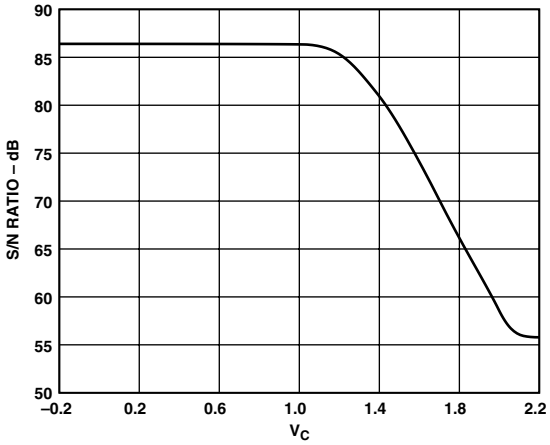


Figure 5. SNR vs. Control Voltage—Sequential Control (1 MHz Bandwidth)

The gains are offset (Figure 7) such that A2's gain is increased only after A1's gain has reached its maximum value. Note that for a differential input of –600 mV or less, the gain of a single amplifier (A1 or A2) will be at its minimum value of –11.07 dB; for a differential input of +600 mV or more, the gain will be at its maximum value of 31.07 dB. Control inputs beyond these limits will not affect the gain and can be tolerated without damage or foldover in the response. This is an important aspect of the AD603's gain-control response. (See the Specifications section of this data sheet for more details on the allowable voltage range) The gain is now

$$Gain\ (dB) = 40\ V_G + G_O \quad (3)$$

where V_G is the applied control voltage and G_O is determined by the gain range chosen. In the explanatory notes that follow, we assume the maximum-bandwidth connections are used, for which G_O is –20 dB.

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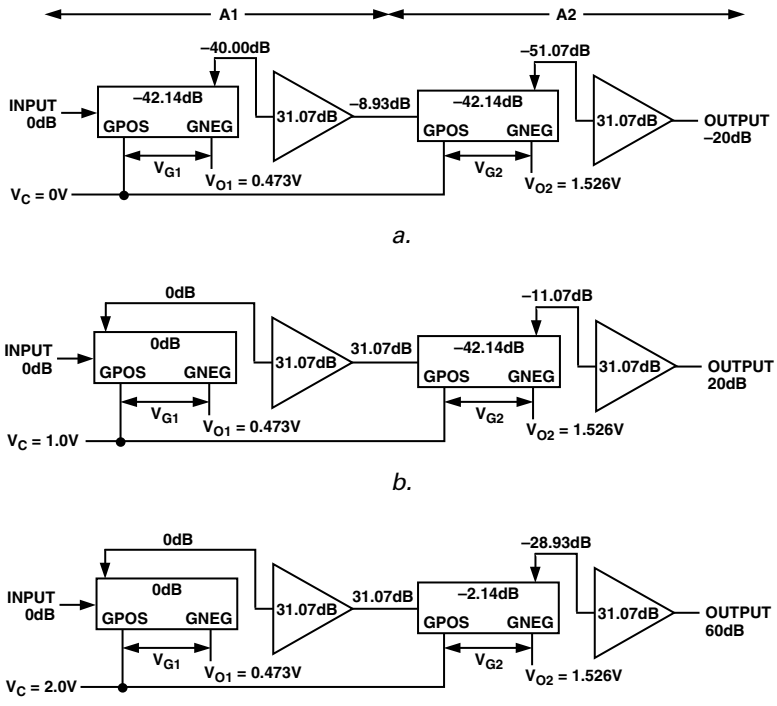


Figure 6. AD603 Gain Control Input Calculations for Sequential Control Operation

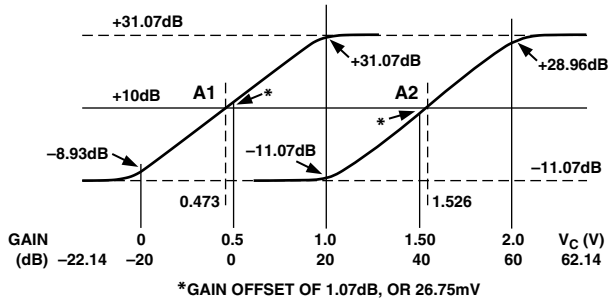


Figure 7. Explanation of Offset Calibration for Sequential Control

With reference to Figure 6, note that V_{G1} refers to the differential gain-control input to A1 and V_{G2} refers to the differential gain-control input to A2. When V_G is zero, V_{G1} = –473 mV and thus the gain of A1 is –8.93 dB (recall that the gain of each individual amplifier in the maximum-bandwidth mode is –10 dB for V_G = –500 mV and 10 dB for V_G = 0 V); meanwhile, V_{G2} = –1.908 V so the gain of A2 is "pinned" at –11.07 dB. The overall gain is thus –20 dB. This situation is shown in Figure 6a.

When V_G = +1.00 V, V_{G1} = 1.00 V – 0.473 V = +0.526 V, which sets the gain of A1 to at nearly its maximum value of 31.07 dB, while V_{G2} = 1.00 V – 1.526 V = 0.526 V, which sets A2's gain at nearly its minimum value –11.07 dB. Close analysis shows that the degree to which neither AD603 is completely pushed to its maximum or minimum gain exactly cancels in the overall gain, which is now +20 dB. This is depicted in Figure 6b.

When V_G = +2.0 V, the gain of A1 is pinned at 31.07 dB and that of A2 is near its maximum value of 28.93 dB, resulting in an overall gain of 60 dB (see Figure 6c). This mode of operation is further clarified by Figure 8, which is a plot of the separate gains of A1 and A2 and the overall gain versus the control voltage. Figure 9 is a plot of the gain error of the cascaded amplifiers versus the control voltage. Figure 10 is a plot of the gain error of the cascaded stages versus the control voltages.

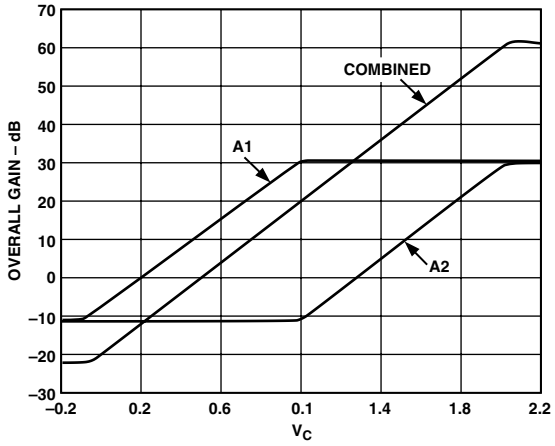


Figure 8. Plot of Separate and Overall Gains in Sequential Control

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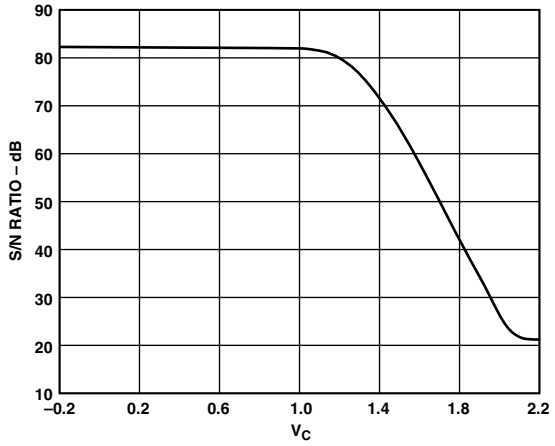


Figure 9. SNR for Cascaded Stages—Sequential Control

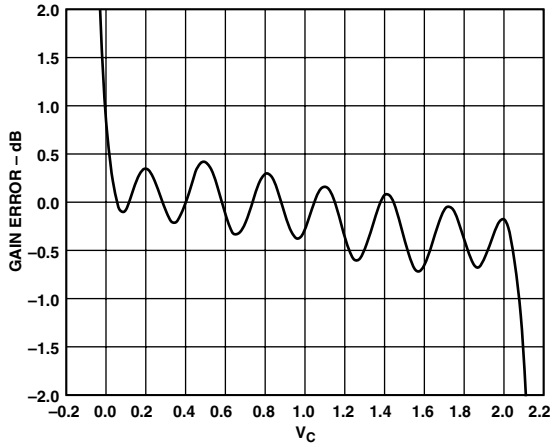


Figure 11. Gain Error for Cascaded Stages–Parallel Control

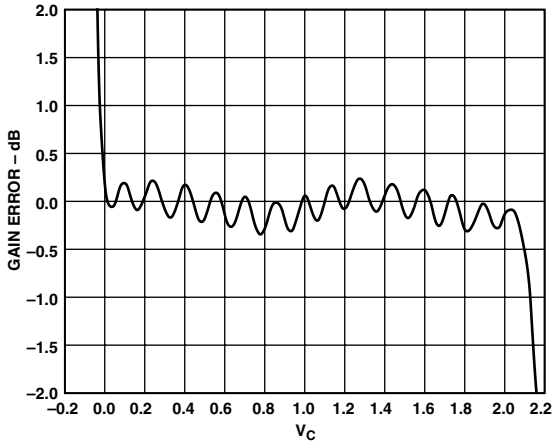


Figure 10. Gain Error for Cascaded Stages—Sequential Control

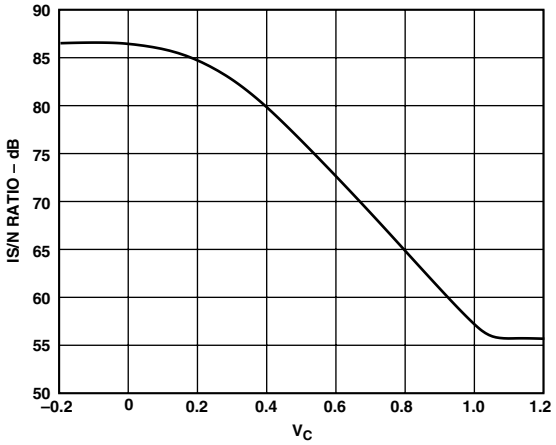


Figure 12. ISNR for Cascaded Stages–Parallel Control

Parallel Mode (Simplest Gain-Control Interface)

In this mode, the gain-control of voltage is applied to both inputs in parallel—the GPOS pins of both A1 and A2 are connected to the control voltage and the GNEW inputs are grounded. The gain scaling is then doubled to 80 dB/V, requiring only a 1.00 V change for an 80 dB change of gain:

$$Gain\ (dB) = 80\ V_G + G_O \qquad (4)$$

where, as before G_O depends on the range selected; for example, in the maximum-bandwidth mode, G_O is +20 dB. Alternatively, the GNEG pins may be connected to an offset voltage of 0.500 V, in which case, G_O is –20 dB.

The amplitude of the gain ripple in this case is also doubled, as shown in Figure 11, while the instantaneous signal-to-noise ratio at the output of A2 now decreases linearly as the gain increased (Figure 12).

Low Gain Ripple Mode (Minimum Gain Error)

As can be seen from Figures 9 and 10, the error in the gain is periodic, that is, it shows a small ripple. (Note that there is also a variation in the *output offset voltage*, which is due to the gain interpolation, but this is not exact in amplitude.) By offsetting the gains of A1 and A2 by half the period of the ripple, that is, by 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 13 shows that much lower gain ripple when configured in this manner. Figure 14 plots the ISNR as a function of gain; it is very similar to that in the "Parallel Mode."

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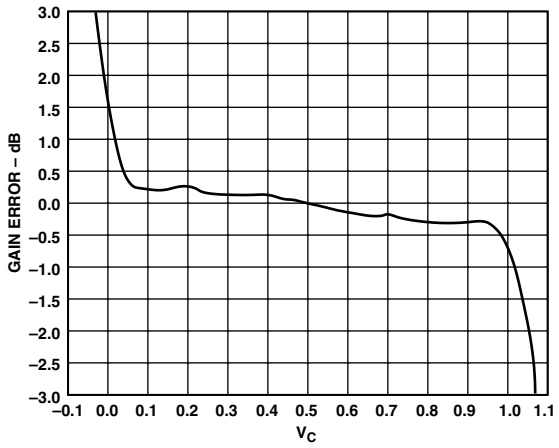


Figure 13. Gain Error for Cascaded Stages–Low Ripple Mode

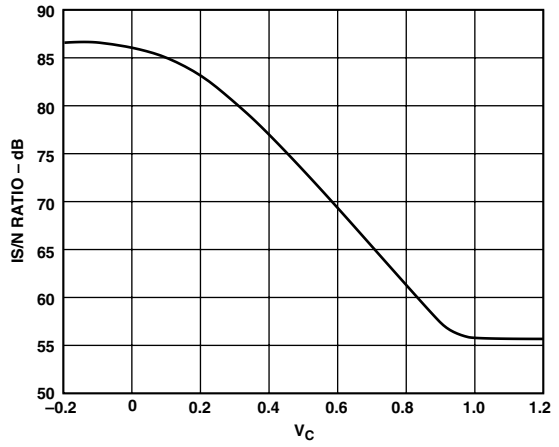


Figure 14. ISNR vs. Control Voltage–Low Ripple Mode

THEORY OF THE AD603

A Low Noise AGC Amplifier

Figure 15 shows the ease with which the AD603 can be connected as an AGC amplifier. The circuit illustrates many of the points previously discussed: It uses few parts, has linear-in-dB gain, operates from a single supply, uses two cascaded amplifiers in sequential gain mode for maximum S/N ratio, and an external resistor programs each amplifier's gain. It also uses a simple temperature-compensated detector.

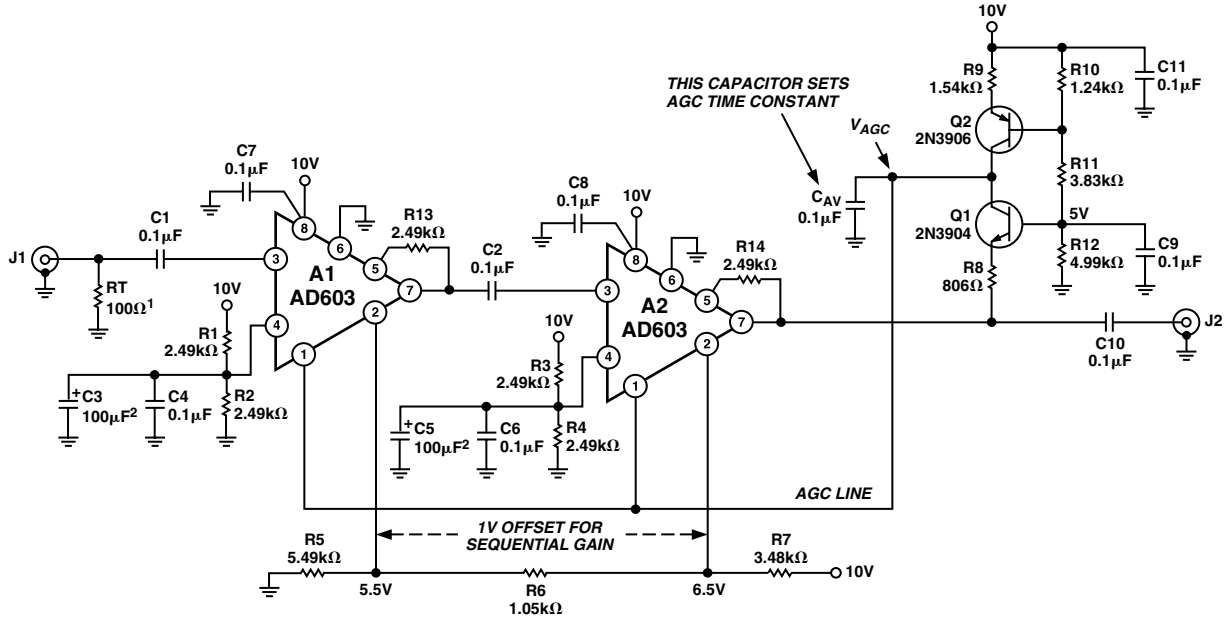
The circuit operates from a single 10 V supply. Resistors R1, R2, R3, and R4 bias the common pins of A1 and A2 at 5 V. This pin is a low impedance point and must have a low impedance path to ground, here provided by the 100 µF tantalum capacitors and the 0.1 µF ceramic capacitors.

The cascaded amplifiers operate in sequential gain. Here, the offset voltage between the pins 2 (GNEG) of A1 and A2 is 1.05 V (42.14 dB × 25 mV/dB), provided by a voltage divider consisting of resistors R5, R6, and R7. Using standard values, the offset is not exact, but it is not critical for this application.

The gain of both A1 and A2 is programmed by resistors R13 and R14, respectively, to be about 42 dB; thus the maximum gain of the circuit is twice that, or 84 dB. The gain-control range can be shifted up by as much as 20 dB by appropriate choices of R13 and R14.

The circuit operates as follows. A1 and A2 are cascaded. Capacitor C1 and the 100 Ω of resistance at the input of A1 form a time-constant of 10 µs. C2 blocks the small dc offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 16 kHz, eliminating low frequency noise.

A half-wave detector is used, based on Q1 and R8. The current into capacitor C_{AV} is just the difference between the collector current of Q2 (biased to be 300 µA at 300 K, 27°C) and the collector current of Q1, which increases with the amplitude of the



NOTES
[1]R_T PROVIDES A 50Ω INPUT IMPEDANCE
[2]C3 AND C5 ARE TANTALUM

Figure 15. A Low Noise AGC Amplifier

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output signal. The automatic gain control voltage, V_{AGC}, is the time-integral of this *error* current. In order for V_{AGC} (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must, on average, exactly balance the current in Q2. If the output of A2 is too small to do this, V_{AGC} will increase, causing the gain to increase, until Q1 conducts sufficiently.

Consider the case where R8 is zero and the output voltage V_{OUT} is a square wave at, say, 455 kHz, which is well above the corner frequency of the control loop.

During the time V_{OUT} is negative with respect to the base voltage of Q1, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the average collector current of Q1 is forced to be 300 μA, and the square wave has a duty-cycle of 1:1, Q1's collector current when conducting must be 600 μA. With R8 omitted, the peak amplitude of V_{OUT} is forced to be just the V_{BE} of Q1 at 600 μA, typically about 700 mV, or 2 V_{BE} peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7 mV/°C. Although this may not be troublesome in some applications, the correct value of R8 will render the output stable with temperature.

To understand this, first note that the current in Q2 is made to be proportional to absolute temperature (PTAT). For the moment, continue to assume that the signal is a square wave.

When Q1 is conducting, V_{OUT} is now the sum of V_{BE} and a voltage that is PTAT and which can be chosen to have an equal but opposite TC to that of the V_{BE}. This is actually nothing more than an application of the "bandgap voltage reference" principle. When R8 is chosen such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2 V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and Q2 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the square wave a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value will depend on the type of transistor used and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904/2N3906 pair and sine wave signals, the recommended value is 806 Ω.

This resistor also serves to lower the peak current in Q1 when more typical signals (usually, sinusoidal) are involved, and the 1.8 kHz LP filter it forms with C_{AV} helps to minimize distortion due to ripple in V_{AGC}. Note that the output amplitude under sine wave conditions will be higher than for a square wave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V rms. In practice, the somewhat nonideal rectifier results in the sine wave output being regulated to about 1.4 V rms, or 3.6 V p-p.

The bandwidth of the circuit exceeds 40 MHz. At 10.7 MHz, the AGC threshold is 100 μV (–67 dBm) and its maximum gain is 83 dB (20 log 1.4 V/100 μV). The circuit holds its output at 1.4 V rms for inputs as low as –67 dBm to +15 dBm (82 dB), where the input signal exceeds the AD603's maximum input rating. For a 30 dBm input at 10.7 MHz, the second harmonic is 34 dB down from the fundamental and the third harmonic is 35 dB down.

CAUTION

Careful component selection, circuit layout, power-supply decoupling, and shielding are needed to minimize the AD603's susceptibility to interference from radio and TV stations, etc. In bench evaluation, we recommend placing all of the components in a shielded box and using feedthrough decoupling networks for the supply voltage. Circuit layout and construction are also critical, since stray capacitances and lead inductances can form resonant circuits and are a potential source of circuit peaking, oscillation, or both.

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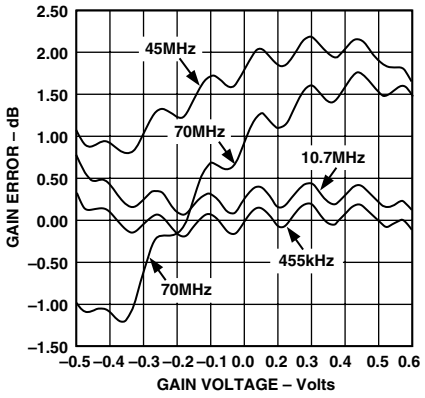


Figure 16. Gain Error vs. Gain Control Voltage at 455 kHz, 10.7 MHz, 45 MHz, 70 MHz

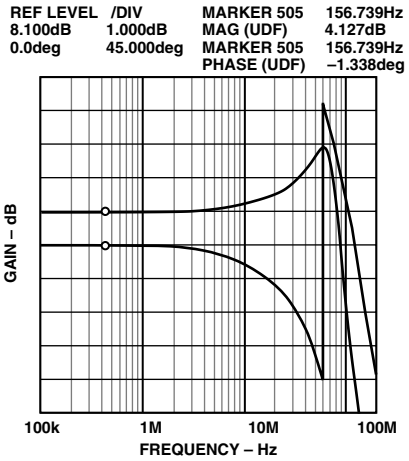


Figure 17. Frequency and Phase Response vs. Gain (Gain = –10 dB, P_{IN} = –30 dBm, Pin 5 Connected to Pin 7)

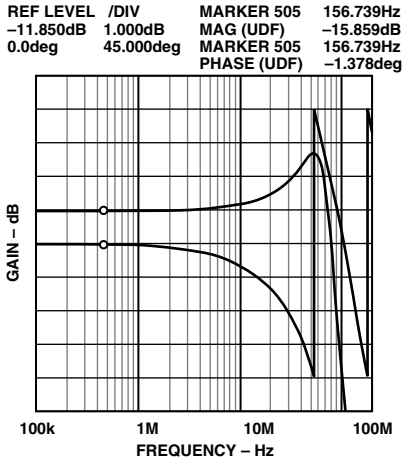


Figure 18. Frequency and Phase Response vs. Gain (Gain = +10 dB, P_{IN} = –30 dBm, Pin 5 Connected to Pin 7)

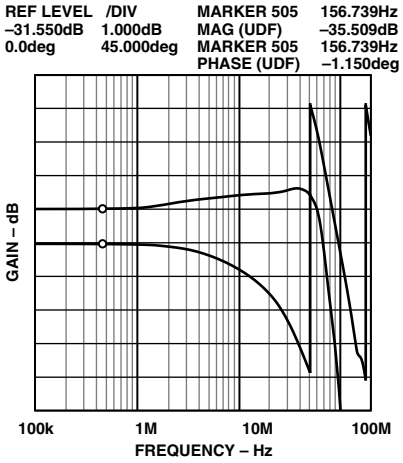


Figure 19. Frequency and Phase Response vs. Gain (Gain = +30 dB, P_{IN} = –30 dBm, Pin 5 Connected to Pin 7)

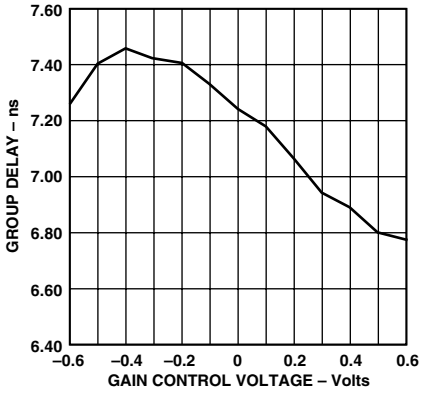


Figure 20. Group Delay vs. Gain Control Voltage

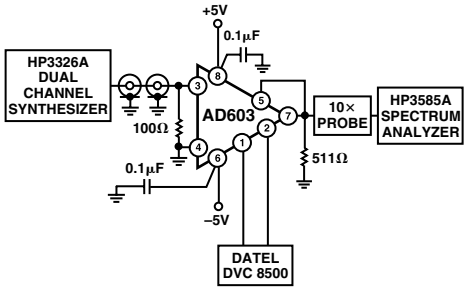


Figure 21. Third Order Intermodulation Distortion Test Setup

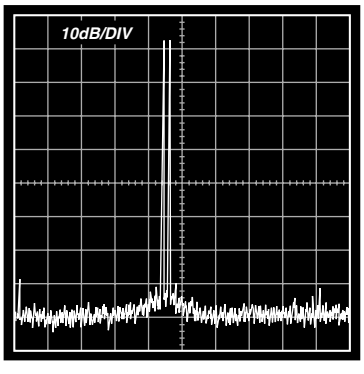


Figure 22. Third Order Intermodulation Distortion at 455 kHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm, Pin 5 Connected to Pin 7)

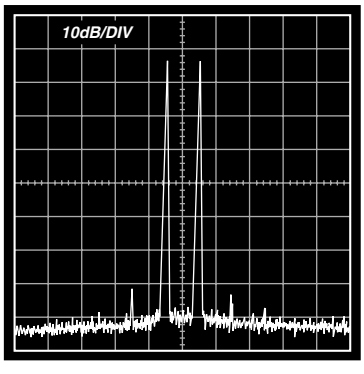


Figure 23. Third Order Intermodulation Distortion at 10.7 MHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm, Pin 5 Connected to Pin 7)

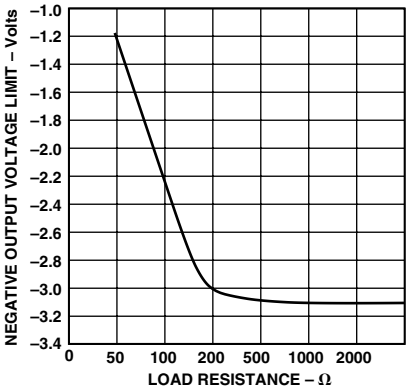


Figure 24. Typical Output Voltage Swing vs. Load Resistance (Negative Output Swing Limits First)

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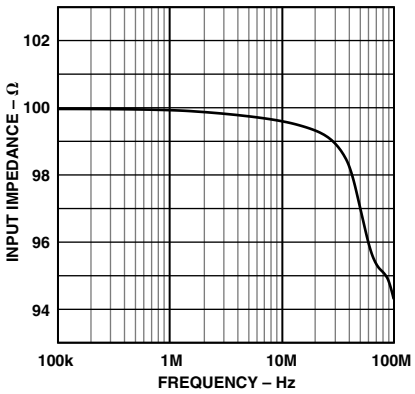


Figure 25. Input Impedance vs. Frequency (Gain = –10 dB)

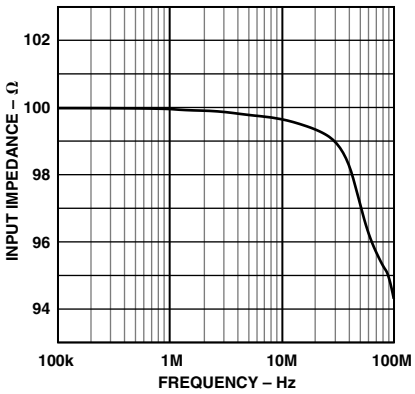


Figure 26. Input Impedance vs. Frequency (Gain = +10 dB)

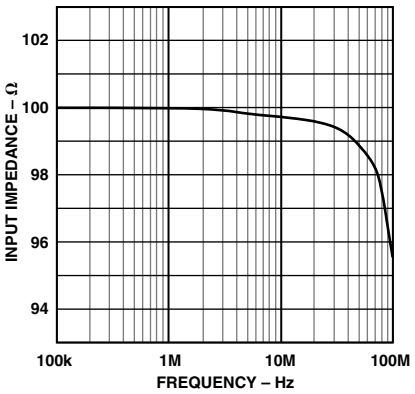


Figure 27. Input Impedance vs. Frequency (Gain = +30 dB)

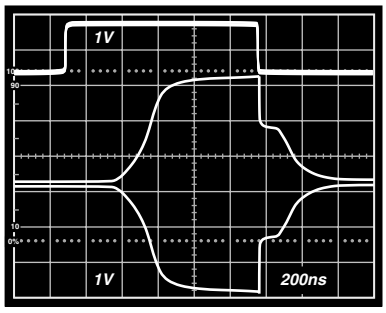


Figure 28. Gain-Control Channel Response Time

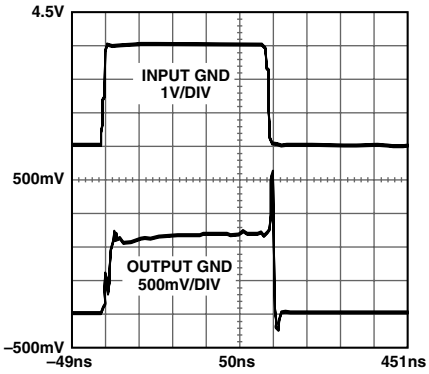


Figure 29. Input Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

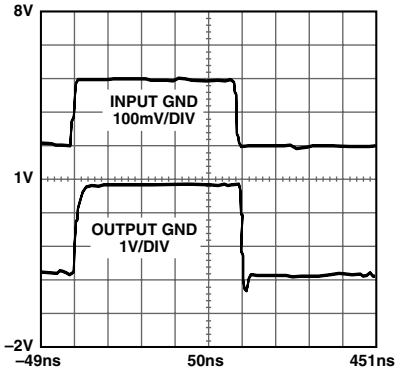


Figure 30. Output Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

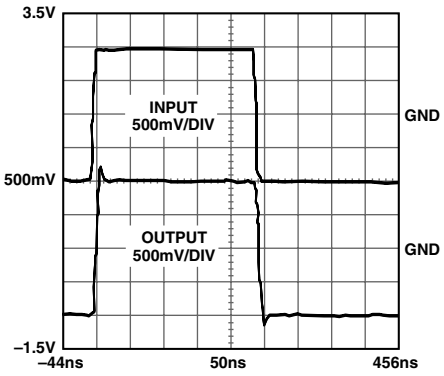


Figure 31. Transient Response, G = 0 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

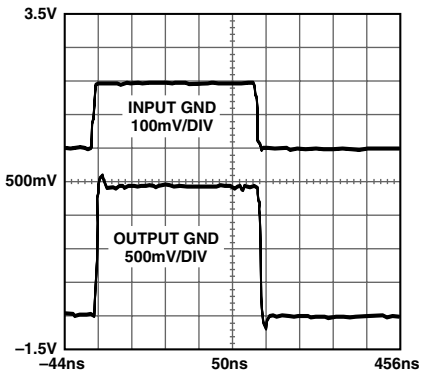


Figure 32. Transient Response, G = +20 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

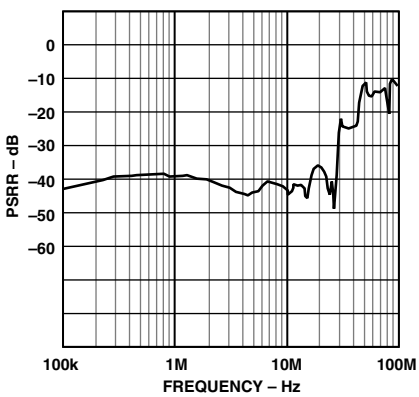


Figure 33. PSRR vs. Frequency (Worst Case Is Negative Supply PSRR, Shown Here)

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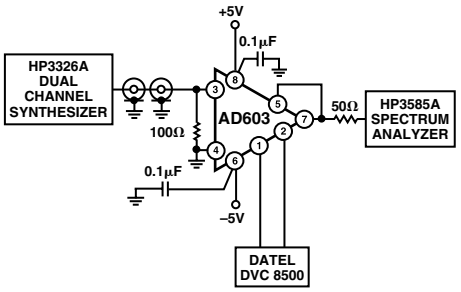


Figure 34. Test Setup Used for: Noise Figure, 3rd Order Intercept and 1 dB Compression Point Measurements

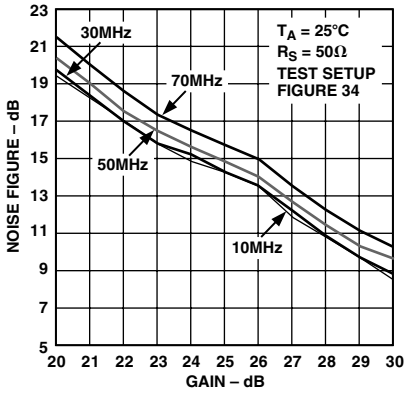


Figure 35. Noise Figure in –10 dB/ +30 dB Mode

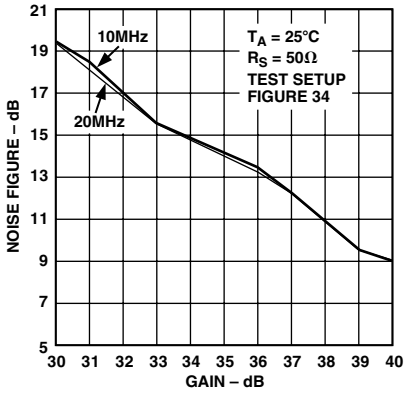


Figure 36. Noise Figure in 0 dB/40 dB Mode

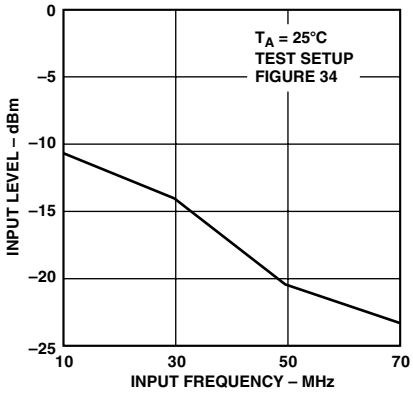


Figure 37. 1 dB Compression Point, –10 dB/+30 dB Mode, Gain = 30 dB

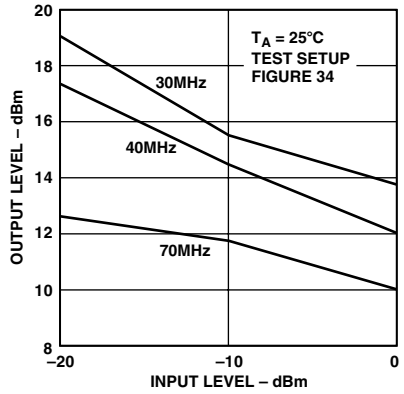


Figure 38. 3rd Order Intercept –10 dB/ +30 dB Mode, Gain = 10 dB

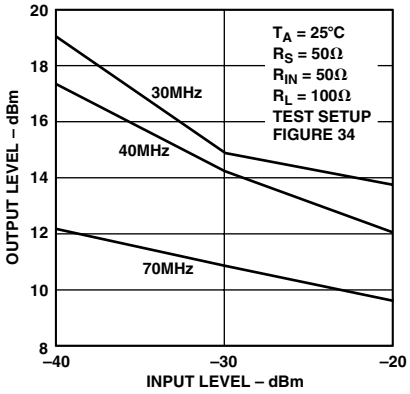


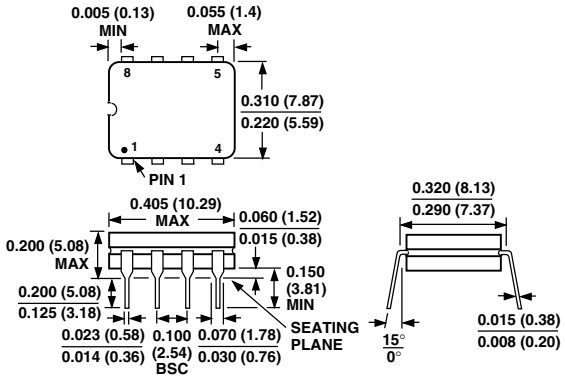
Figure 39. 3rd Order Intercept, –10 dB/ +30 dB Mode, Gain = 30 dB

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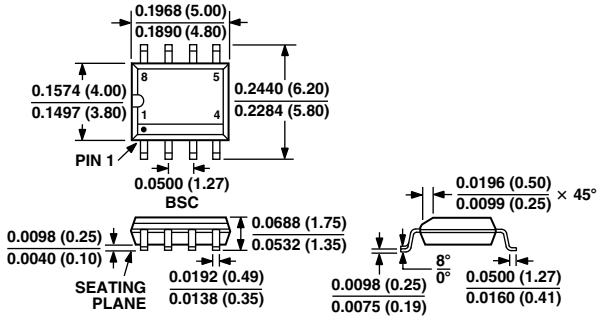
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Cerdip (Q-8)



8-Lead SOIC (SO-8)



C00539a–0–11/00 (rev. D)

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Appendix D: Linear Technology LTC1451 – 12–bit Rail to Rail DAC

Included for your reference on the following pages is the data sheet for the LTC1451 12–bit Rail to Rail DAC, provided by the courtesy of Linear Technology Corp., Milpitas, CA.

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12-Bit Rail-to-Rail Micropower DACs in SO-8

FEATURES

- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- 3V Operation (LTC1453), I_{CC}: 250µA Typ
- 5V Operation (LTC1451), I_{CC}: 400µA Typ
- 3V to 5V Operation (LTC1452), I_{CC}: 225µA Typ
- Built-In Reference: 2.048V (LTC1451)
  1.220V (LTC1453)
- Multiplying Version (LTC1452)
- Power-On Reset
- **SO-8 Package**
- 3-Wire Cascadable Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Schmitt Trigger on Clock Input Allows Direct Optocoupler Interface

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION

The LTC®1451/LTC1452/LTC1453 are complete single supply, rail-to-rail voltage output 12-bit digital-to-analog converters (DACs) in an SO-8 package. They include an output buffer amplifier and an easy-to-use 3-wire cascadable serial interface.

The LTC1451 has an onboard reference of 2.048V and a full-scale output of 4.095V. It operates from a single 4.5V to 5.5V supply.

The LTC1452 is a multiplying DAC with a full-scale output of twice the reference input voltage. It operates from a single supply of 2.7V to 5.5V.

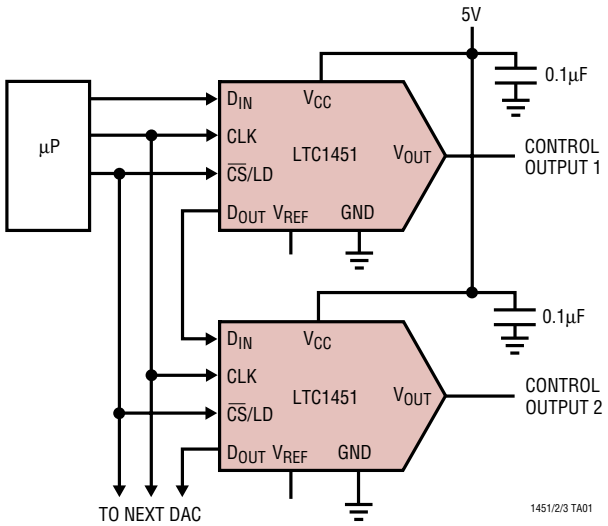
The LTC1453 has an onboard 1.22V reference and a full-scale output of 2.5V. It operates from a single supply of 2.7V to 5.5V.

The low power supply current makes the LTC1451 family ideal for battery-powered applications. The space saving 8-pin SO package and operation with no external components provide the smallest 12-bit DAC system available.

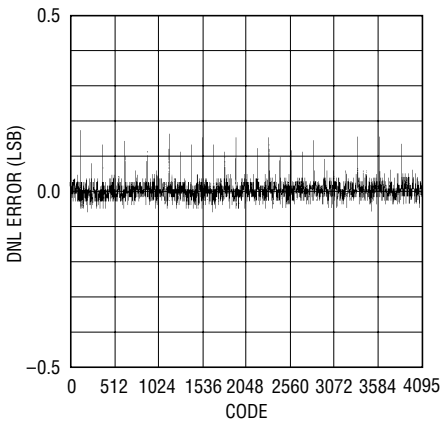
, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

Daisy-Chained Control Outputs



Differential Nonlinearity vs Input Code



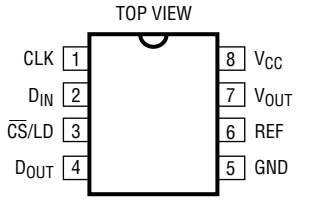
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ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to GND ..... –0.5V to 7.5V
TTL Input Voltage ..... –0.5V to 7.5V
V_{OUT}, D_{OUT} ..... –0.5V to V_{CC} + 0.5V
REF ..... –0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... –65°C to 125°C

Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER		S8 PART MARKING
LTC1451CN8	LTC1451CS8	1451
LTC1452CN8	LTC1452CS8	1452
LTC1453CN8	LTC1453CS8	1453
LTC1451IN8	LTC1451IS8	1451I
LTC1452IN8	LTC1452IS8	1452I
LTC1453IN8	LTC1453IS8	1453I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2)	●			±0.5	LSB
INL	Integral Nonlinearity	T_A = 25°C (Note 2)	 ●			±3.5 ±4	LSB LSB
V_{OS}	Offset Error	T_A = 25°C	 ●			±12 ±18	mV mV
$V_{OS}TC$	Offset Error Temperature Coefficient				±15		µV/°C
V_{FS}	Full-Scale Voltage	When Using Internal Reference, LTC1451, T_A = 25°C LTC1451	 ●	4.065 4.045	4.095 4.095	4.125 4.145	V V
		External 2.048V Reference, V_{CC} = 5V, LTC1452	●	4.075	4.095	4.115	V
		When Using Internal Reference, LTC1453, T_A = 25°C LTC1453	 ●	2.470 2.460	2.500 2.500	2.530 2.540	V V
$V_{FS}TC$	Full-Scale Voltage Temperature Coefficient	When Using Internal Reference, LTC1451 When Using External 2.048V Reference, LTC1452 When Using Internal Reference, LTC1453			±0.10 ±0.02 ±0.10		LSB/°C LSB/°C LSB/°C

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ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference (LTC1451/LTC1453)							
	Reference Output Voltage	LTC1451 LTC1453	● ●	2.008 1.195	2.048 1.220	2.088 1.245	V V
	Reference Output Temperature Coefficient				±0.08		LSB/°C
	Reference Line Regulation		●		0.7	±2	LSB/V
	Reference Load Regulation	$0 \leq I_{OUT} \leq 100\mu A$, LTC1451 LTC1453	● ●		0.2 0.6	±1.5 ±3	LSB LSB
	Reference Input Range	$V_{REF} \leq V_{CC} - 1.5V$	●			$V_{CC}/2$	V
	Reference Input Resistance		●	8	14	30	kΩ
	Reference Input Capacitance				15		pF
	Short-Circuit Current	REF Shorted to GND	●			80	mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance, LTC1451 LTC1452 LTC1453	● ● ●	4.5 2.7 2.7		5.5 5.5 5.5	V V V
I_{CC}	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1451 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1452 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1453	● ● ●	300 120 150	400 225 250	620 350 500	µA µA µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			100	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			120	mA
	Output Impedance to GND	Input Code = 0	●		40	120	Ω
AC Performance							
	Voltage Output Slew Rate	(Note 3)	●	0.4	1.0		V/µs
	Voltage Output Settling Time	(Notes 3, 4) to ±0.5LSB			14		µs
	Digital Feedthrough				0.3		nV•s
	AC Feedthrough	REF = 1kHz, $2V_{P-P}$, LTC1452			–95		dB
SINAD	Signal-to-Noise + Distortion	REF = 1kHz, $2V_{P-P}$, (Code: All 1s) LTC1452			85		dB

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ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (LTC1451LTC1452), V_{CC} = 3V (LTC1453).

SYMBOL	PARAMETER	CONDITIONS		LTC1451/LTC1452 MIN	LTC1451/LTC1452 TYP	LTC1451/LTC1452 MAX	LTC1453 MIN	LTC1453 TYP	LTC1453 MAX	UNITS
Digital I/O										
V_{IH}	Digital Input High Voltage		●	2.4			2.0			V
V_{IL}	Digital Input Low Voltage		●			0.8			0.6	V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA	●	V_{CC} – 1.0			V_{CC} – 0.7			V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA	●			0.4			0.4	V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10			±10	µA
C_{IN}	Digital Input Capacitance	Guaranteed by Design Not Subject to Test	●			10			10	pF
Switching										
t_1	D_{IN} Valid to CLK Setup		●	40			60			ns
t_2	D_{IN} Valid to CLK Hold		●	0			0			ns
t_3	CLK High Time		●	40			60			ns
t_4	CLK Low Time		●	40			60			ns
t_5	$\overline{CS}$/LD Pulse Width		●	50			80			ns
t_6	LSB CLK to $\overline{CS}$/LD		●	40			60			ns
t_7	$\overline{CS}$/LD Low to CLK		●	20			30			ns
t_8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●			150			220	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	20			30			ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

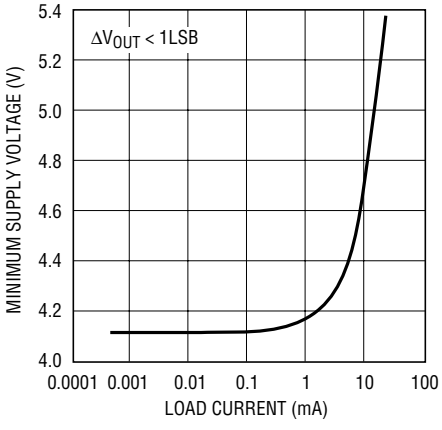
Note 3: Load is 5kΩ in parallel with 100pF.

Note 4: DAC switched between all 1s and the code corresponding to V_{OS} for the part, i.e., LTC1451: code 18; LTC1453: code 30.

Note 5: Digital inputs at 0V or V_{CC}.

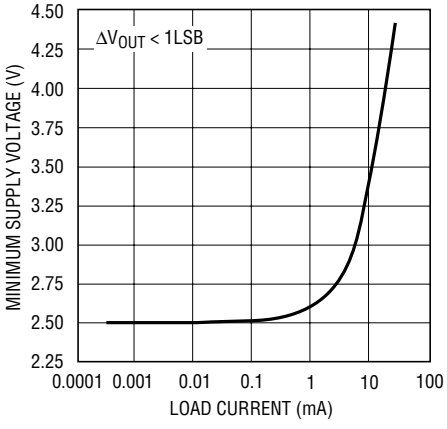
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1451 Minimum Supply Voltage vs Load Current



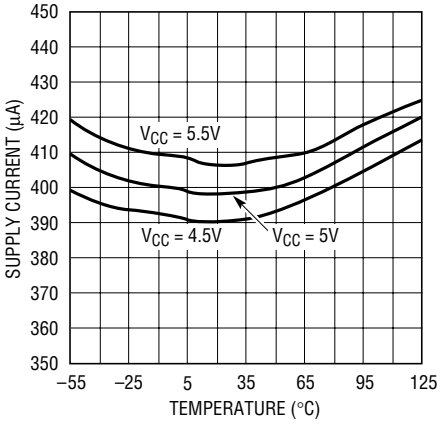
1451/2/3 G01

LTC1453 Minimum Supply Voltage vs Load Current



1451/2/3 G02

LTC1451 Supply Current vs Temperature

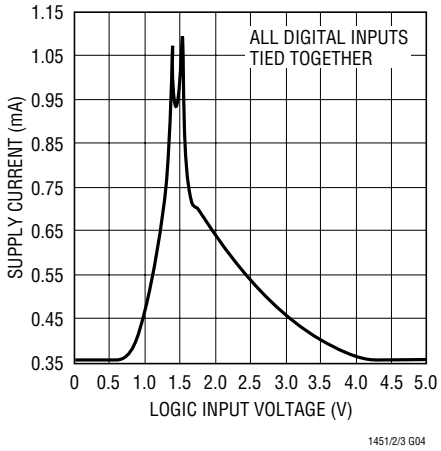


1451/2/3 G03

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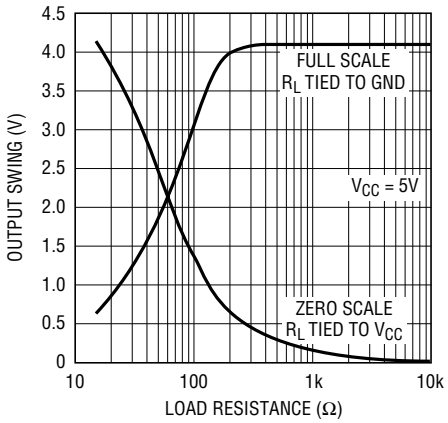
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1451
Supply Current vs Logic Input Voltage



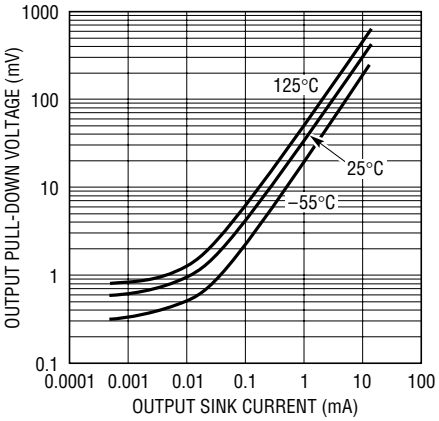
1451/2/3 G04

LTC1451
Output Swing vs Load Resistance



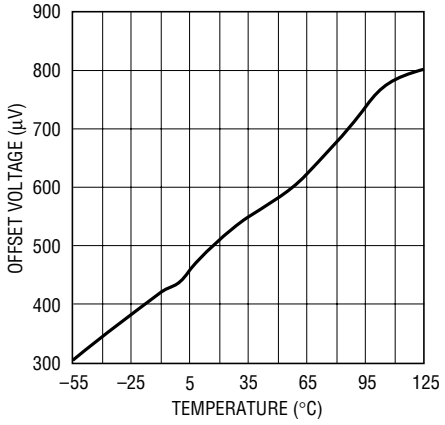
1451/2/3 G05

LTC1451
Pull-Down Voltage vs Output Sink Current Capability



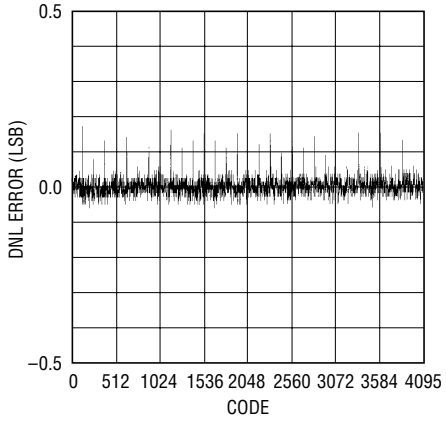
1451/2/3 G06

LTC1451
Offset Voltage vs Temperature



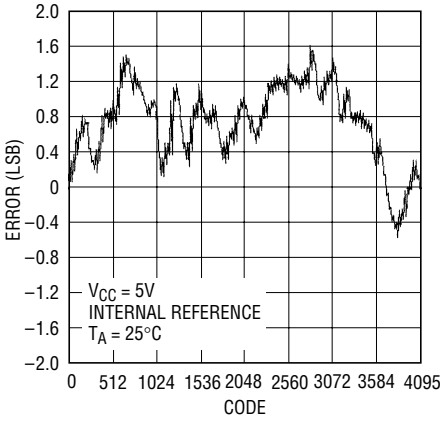
1451/2/3 G07

LTC1451
Differential Nonlinearity (DNL)



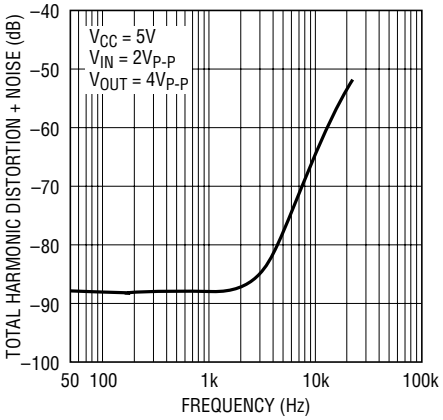
1451/2/3 TA02

LTC1451
Integral Nonlinearity (INL)



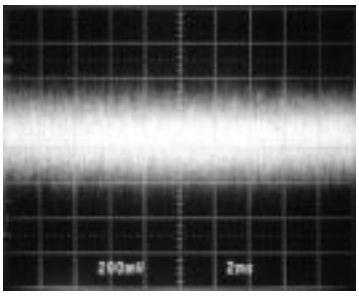
1451/2/3 G09

LTC1452
Total Harmonic Distortion + Noise vs Frequency



1451/2/3 G08

LTC1451
Broadband Output Noise



CODE = FFFH
BW = 3Hz TO 1.4MHz
GAIN = 1000

1451/2/3 G10

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PIN FUNCTIONS

CLK: The TTL Level Input for the Serial Interface Clock.

D_{IN}: The TTL Level Input for the Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{CS}$/LD: The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the CLK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT}: The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

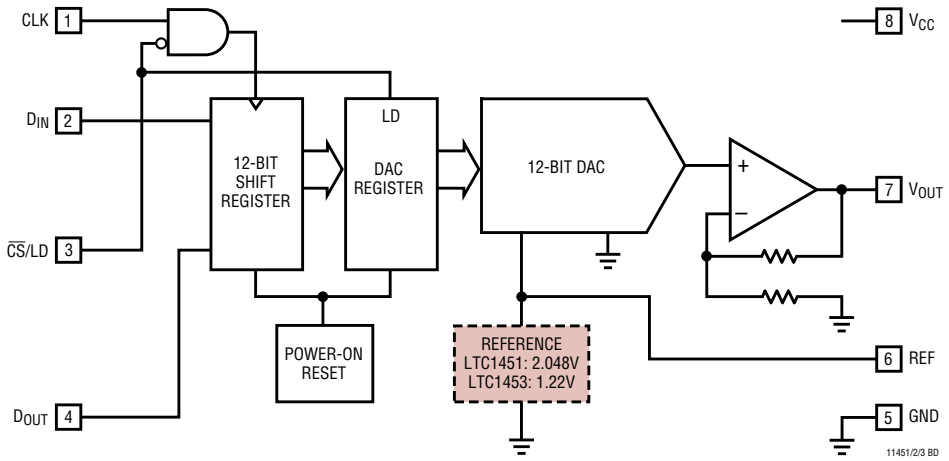
GND: Ground.

REF: The Output of the Internal Reference and the Input to the DAC Resistor Ladder. An external reference with voltage up to $V_{CC}/2$ may be used for the LTC1452.

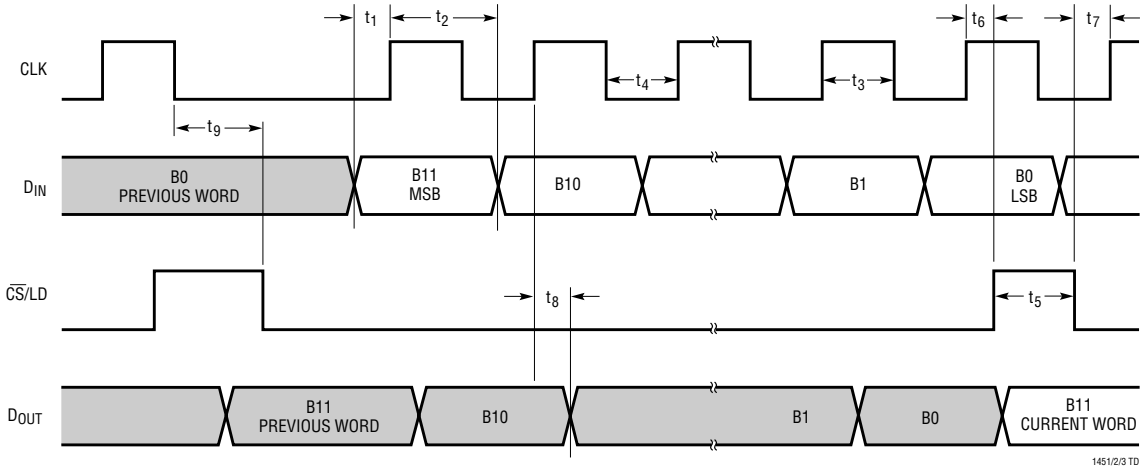
V_{OUT}: The Buffered DAC Output.

V_{CC}: The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$ (LTC1451), $2.7 \leq V_{CC} \leq 5.5V$ (LTC1452/LTC1453). Requires a bypass capacitor to ground.

BLOCK DIAGRAM



TIMING DIAGRAM



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DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): Normally, DAC offset is the voltage at the output when the DAC is loaded with all zeros. The DAC can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code \times V_{FS})/(2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

LTC1451	LSB = 4.095V/4095 = 1mV
LTC1452	LSB = V(REF)/4095
LTC1453	LSB = 2.5V/4095 = 0.610mV

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$$

V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV × sec.

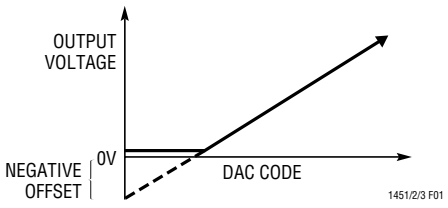


Figure 1. Effect of Negative Offset

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OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when $\overline{CS}$/LD is pulled high. The CLK is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

The buffered output of the 12-bit shift register is available on the D_{OUT} pin which swings from GND to V_{CC}.

Multiple LTC1451/LTC1452/LTC1453s may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the CLK and $\overline{CS}$/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

Reference

The LTC1451 includes an internal 2.048V reference, making 1LSB equal to 1mV (gain of 2). The LTC1453 has an internal reference of 1.22V with a full scale of 2.5V (gain of 2.05). The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The LTC1452 has no internal reference and the REF pin must be driven externally. The buffer gain is 2, so the external reference must be less than $V_{CC}/2$ and be capable of driving the 8k minimum DAC resistor ladder.

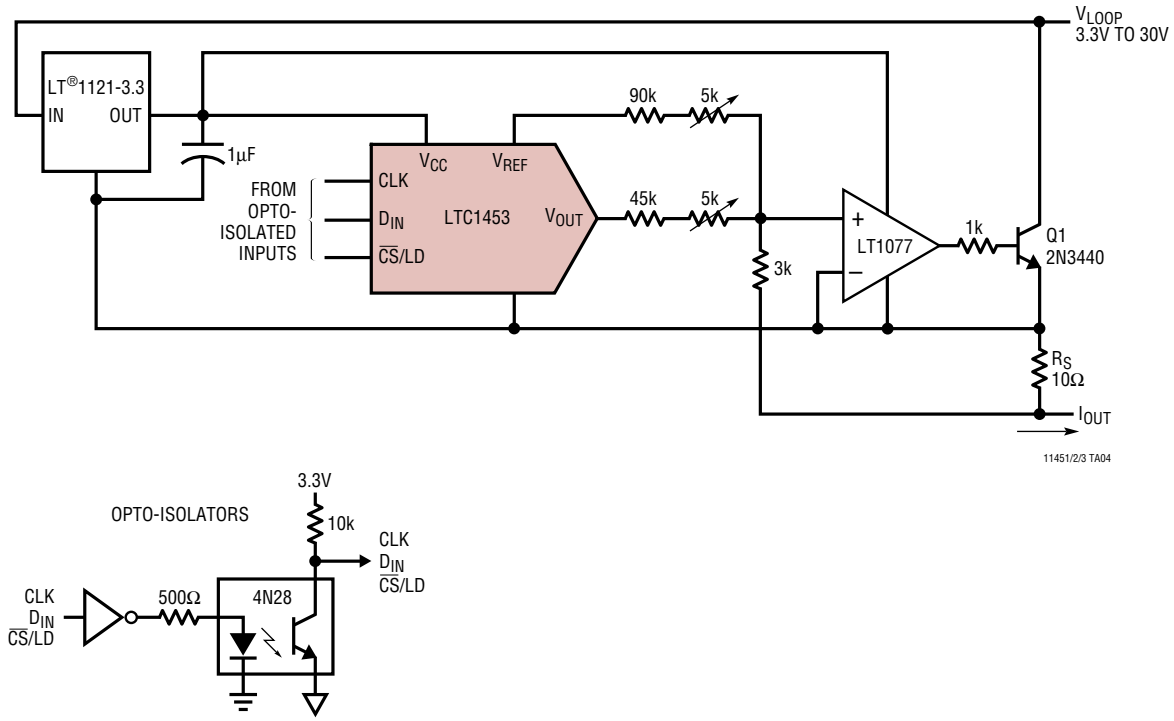
Voltage Output

The LTC1451 family's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

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TYPICAL APPLICATIONS

An Isolated 4mA to 20mA Process Controller Has 3.3V Minimum Loop Voltage



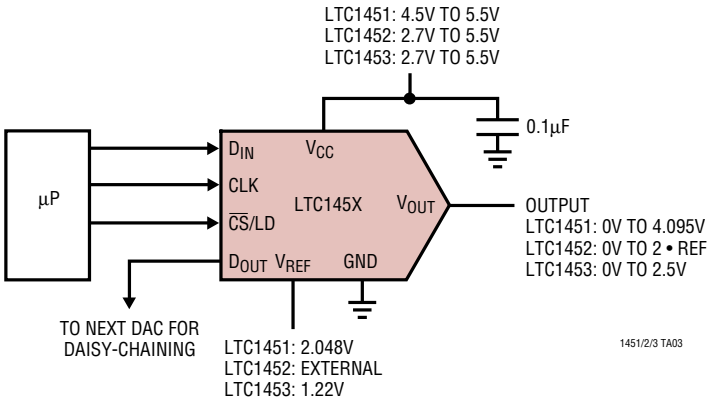
This circuit shows how to use an LTC1453 to make an opto-isolated digitally controlled 4mA to 20mA process controller. The controller circuitry, including the opto-isolation, is powered by the loop voltage that can have a wide range of 3.3V to 30V. The 1.22V reference output of the LTC1453 is used for the 4mA offset current and V_{OUT} is used for the digitally controlled 0mA to 16mA current. R_S is a sense resistor and the op amp modulates the transistor Q1 to provide the 4mA to 20mA current through this resistor. The potentiometers allow for offset and full-scale adjustment. The control circuitry dissipates well under the 4mA budget at zero-scale.

Note that although these DACs have internal Schmitt triggers and are suitable for use with slow rising edges such as produced by the above optoisolator, the use of optoisolators in a daisy-chained topology requires the addition of a gate or the use of a fast isolator on the clock signal. Setup and hold times between D_{OUT} and D_{IN} are not guaranteed unless a clock edge with a rise time of less than 100ns is provided.

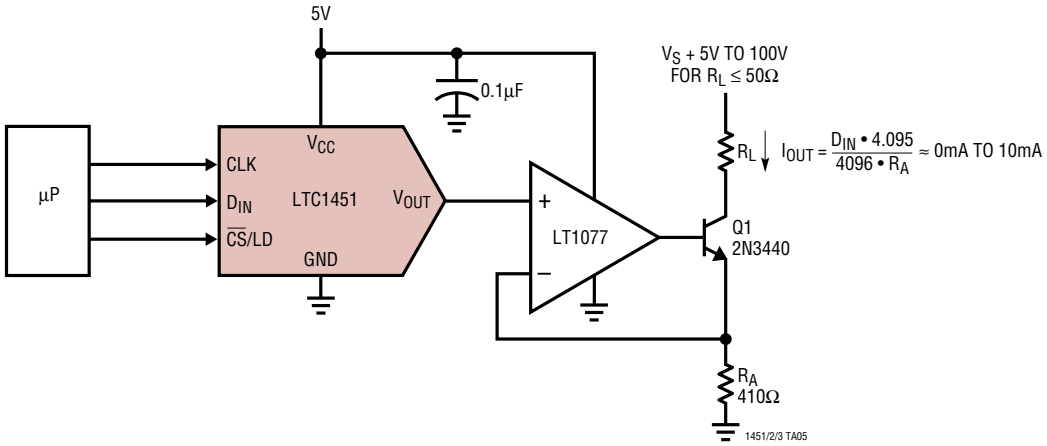
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TYPICAL APPLICATIONS

12-Bit 3V to 5V Voltage Output DAC



Digitally Programmable Current Source



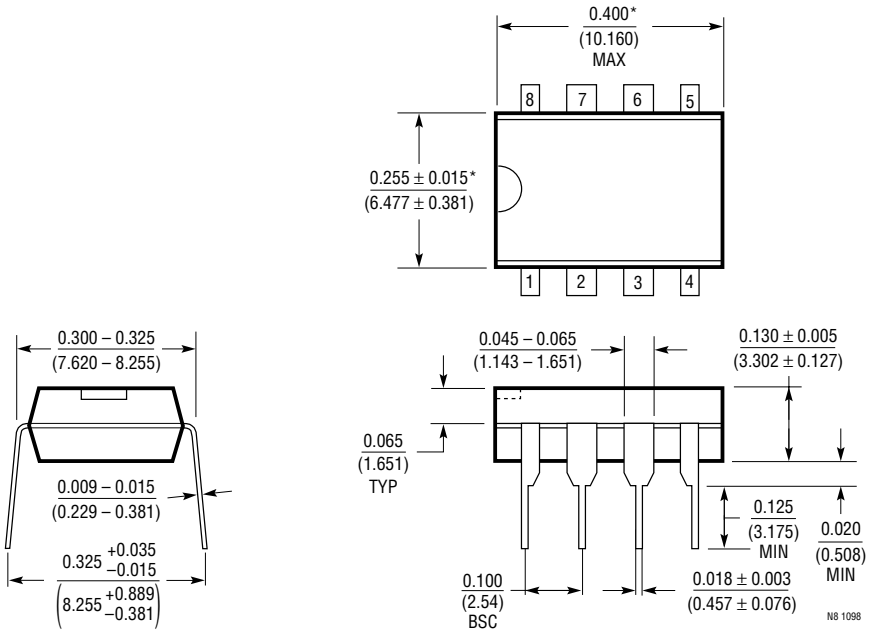
This circuit shows a digitally programmable current source from an external voltage source using an external op amp, an LT1077 and an NPN transistor (2N3440). Any digital word from 0 to 4095 is loaded into the LTC1451 and its output correspondingly swings from 0V to 4.095V. In the configuration shown, this voltage will be forced across the resistor R_A. If R_A is chosen to be 410Ω the output current will range from 0mA at zero-scale to 10mA at full-scale. The minimum voltage for V_S is determined by the load resistor R_L and Q1's V_{CESAT} voltage. With a load resistor of 50Ω, the voltage source can be as low as 5V.

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PACKAGE DESCRIPTION

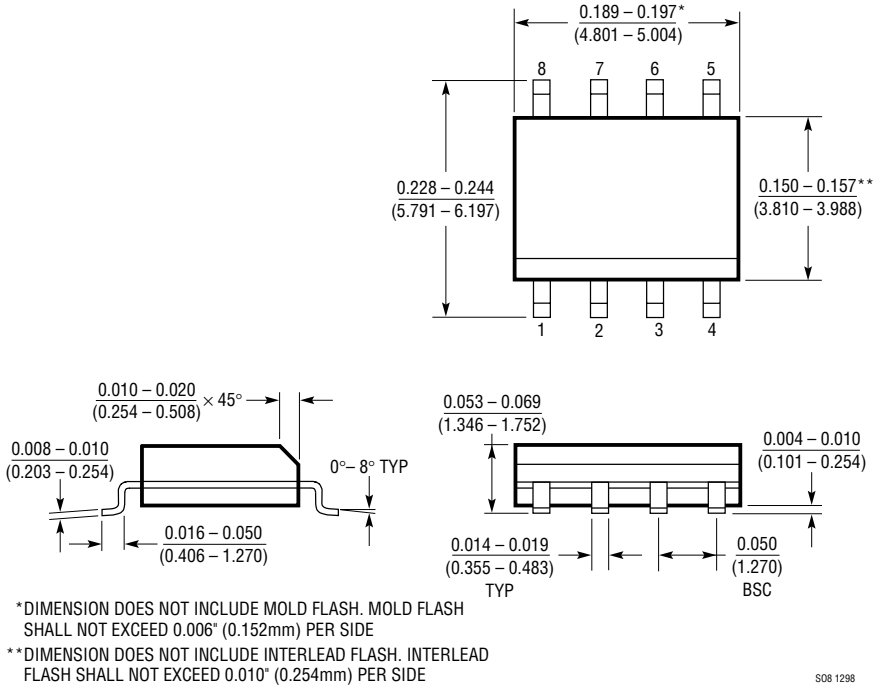
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

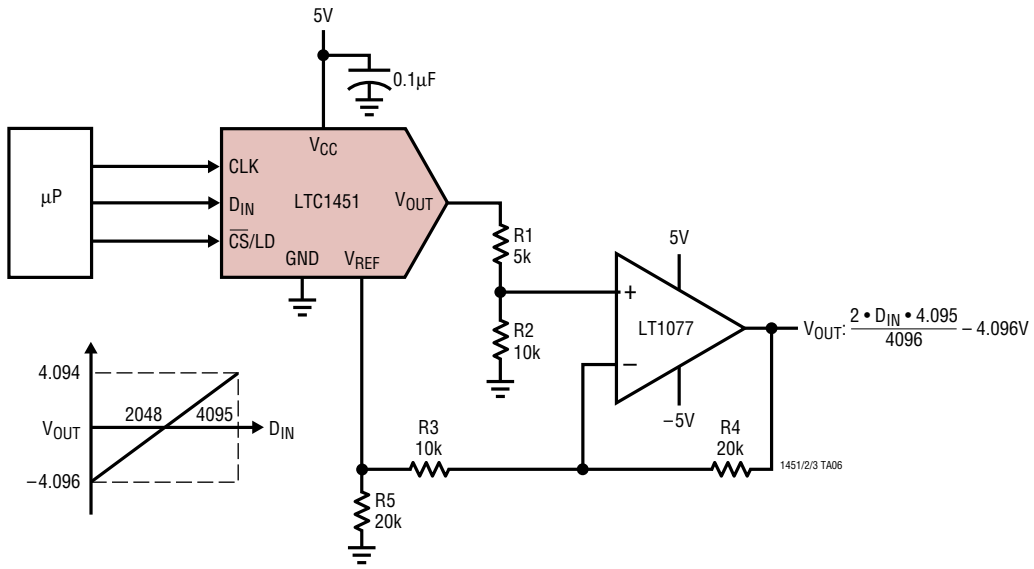
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TYPICAL APPLICATION

This circuit shows how to make a bipolar output 12-bit DAC with a wide output swing using an LTC1451 and an LT1077. R1 and R2 resistively divide down the LTC1451 output and an offset is summed in using the LTC1451 onboard 2.048V reference and R3 and R4. R5 ensures that the onboard reference is always sourcing current and never has to sink any current even when V_{OUT} is at full-scale. The LT1077 output will have a wide bipolar output swing of –4.096V to 4.094V as shown in the figure above. With this output swing 1LSB = 2mV.

A Wide Swing, Bipolar Output 12-Bit DAC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	5V to 15V Single Supply, Complete 12-Bit V_{OUT} DAC in SO-8 Package	Reference Can Be Overdriven Up to 12V, i.e., FS MAX = 12V
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8	5V with 4.096V Full-Scale Output/3V with 2.5V Full Scale
LTC1448	Dual 12-Bit V_{OUT} DAC in SO-8	V_{CC} from 2.7V to 5.5V, Output Swings to V_{REF}
LTC1655/LTC1655L	5V/3V 16-Bit V_{OUT} DAC in SO-8	Pin Conpatible with LTC1451/LTC1453
LTC1659	Single 12-Bit V_{OUT} DAC in MSOP	V_{CC} from 2.7V to 5.5V, Output Swings to V_{REF}
LTC7541	12-Bit Multiplying Parallel I_{OUT} DAC	5V to 16V Supply, 12-Bit Wide Interface
LTC7543/LTC8143	12-Bit Multiplying Serial I_{OUT} DAC	5V Supply, Clear Pin and Serial Data Output (LTC8143)
LTC8043	12-Bit Multiplying Serial I_{OUT} DAC	5V Supply, SO-8 Package

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Appendix E: Configuration EEPROM Format

E.1 Introduction

All VIM Modules are required to contain an Identification (ID) EEPROM with a checksum stored in the last location. When booted, the 'C6x processors check for the presence of VIM modules, through the presence bit on the VIM connector itself. If a module is present, the processor reads the module's ID EEPROM and generates a 16–bit checksum from the results of the readout. There are three conditions for the checksum; Valid Checksum (**0x00EE C0DE**), Bad Checksum (**0x000B ADC5**), and No VIM Module Installed (**0xFFFF FFFF**). All checksums are placed in Global SRAM at the following locations:

'C6x Processor	Global SRAM Location
Processor A	**0x0000 0900**
Processor B	**0x0000 1900**
Processor C	**0x0000 2900**
Processor D	**0x0000 3900**

If the generated checksum does not match the stored value, the processor lights its red LED, and places **BADC5** in Global SRAM. Even though the processor illuminates LED 0, the red LED, the processor is fully functional.

The bitwise layout of this register is defined in Table E–1, below.

Table E–1: VIM ID EEPROM Register – R/W @ VIM Address 0x0032 0000

Bit #	D31 – D4	D3	D2	D1	D0
Bit Name	Reserved	EEPROM_ Chip_Select	EEPROM_ Data_Out	Reserved	EEPROM_Clock
Access	Read/Write	Read/Write	Read Only	Read/Write	Read/Write
Function	Mask when reading	1 = Selected 0 = Not Selected	Stored Data	Mask when reading	Toggle to pluse Clock line

E.2 EEPROM Format Example

Shown on the next page is the contents of an EEPROM, the example shows the Pentek Model 6210, and an explanation of what each word is used for.

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E.2 EEPROM Format Example (continued)

Table E–2: EEPROM Example (Model 6210 shown)

Global SRAM Locations	EEPROM Word Location	Contents	Comments
0x0000 z900	00/01	0x00EE C0DE	Valid data flag
0x0000 z904	02/03	0x6210 0000	Model, Model Extension – Extension field is currently unused.
0x0000 z908	04/05	0x0354 2001	PCB number. This is taken from the VIM board.
0x0000 z90C	06/07	0x0001 FFFF	Assembly Rev, Option #1 – Rev A = 1, B=2, etc. space is allocated for up to 9 installed options.
0x0000 z910	08/09	0xFFFF FFFF	Option #2, Option #3 – When there are no options, **F** appears in the entire field.
0x0000 z914	10/11	0xFFFF FFFF	Option #4, Option #5
0x0000 z918	12/13	0xFFFF FFFF	Option #6, Option #7
0x0000 z91C	14/15	0xFFFF FFFF	Option #8, Option #9
0x0000 z920	16/17	0xFFFF FFFF	Module Specific Code goes in locations 16 through 61.
0x0000 z924	18/19	0xFFFF FFFF	
0x0000 z928	20/21	0xFFFF FFFF	
0x0000 z92C	22/23	0xFFFF FFFF	
0x0000 z930	24/25	0xFFFF FFFF	
0x0000 z934	26/27	0xFFFF FFFF	
0x0000 z938	28/29	0xFFFF FFFF	
0x0000 z93C	30/31	0xFFFF FFFF	
0x0000 z940	32/33	0xFFFF FFFF	
0x0000 z944	34/35	0xFFFF FFFF	
0x0000 z948	36/37	0xFFFF FFFF	
0x0000 z94C	38/39	0xFFFF FFFF	
0x0000 z950	40/41	0xFFFF FFFF	
0x0000 z954	42/43	0xFFFF FFFF	
0x0000 z958	44/45	0xFFFF FFFF	
0x0000 z95C	46/47	0xFFFF FFFF	
0x0000 z960	48/49	0xFFFF FFFF	
0x0000 z964	50/51	0xFFFF FFFF	
0x0000 z968	52/53	0xFFFF FFFF	
0x0000 z96C	54/55	0xFFFF FFFF	
0x0000 z970	56/57	0xFFFF FFFF	
0x0000 z974	58/59	0xFFFF FFFF	
0x0000 z978	60/61	0xFFFF FFFF	
0x0000 z97C	62/63	0x0000 xxxx	Word 62 should always be cleared (**0000**). Word 63 contains the byte summation of words 0 – 61.
NOTE: **z** = **0** for Processor A, **1** for Processor B, **2** for Processor C, and **3** for Processor D.			

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Appendix F: Application Note

F.1 Introduction

This Application Note covers the subject of calculating the maximum output sample rate and bandwidth specifications for the Intersil HSP50214B Digital Receiver Chip, as used on Pentek's Model 6210 VIM–2 Module. A simplified block diagram of the chip is presented for reference in Figure F–1, below.

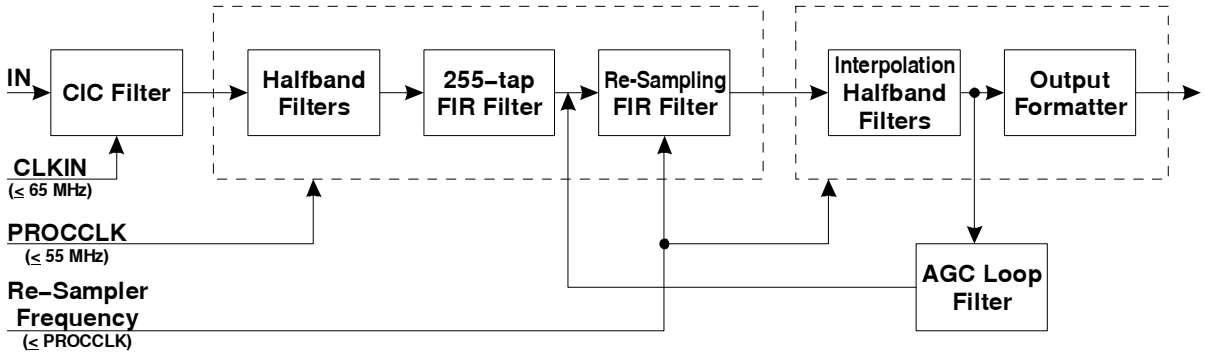


Figure F–1: HSP50214 Simplified Block Diagram

F.2 Output Sample Rate and Bandwidth Specifications

Standard (Using 64 MHz Clock; PROCCLK = 32 MHz):

Output Sampling Rate:	7.53 MHz
Output Bandwidth:	571 KHz (max.)

Maximum (Using 55 MHz Clock; PROCCLK = 55 MHz):

Output Sampling Rate:	12.9 MHz
Output Bandwidth:	982 KHz (max.)

NOTE: When using the 6210 with the standard 64 MHz clock crystal or optional 65 MHz crystal, PROCCLK must be divided by 2 (this is the default setting – set by bit D4 in the 6210's Control Register). In order to achieve the maximum chip sampling rate and bandwidth, a 55 MHz clock is required; on the standard Model 6210 (or Option 020), **PROCCLK must be divided by 2** for inputs higher than 55 MHz. Option 021 provides a 53.125 MHz oscillator, which allows PROCCLK to be equal to the A/D sample rate and DDR operation at close to the maximum output bandwidth and sample rate.

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F.3 Calculating the Low Pass Bandwidth

The specifications listed above use one halfband filter section. The throughput is set by the selected filters and the PROCCLK rate. The AGC loop filter requires 6 PROCCLK cycles for processing, so the rate into the Re–Sampler filter must be PROCCLK/6 maximum. The halfband requires 7 clocks to calculate an output; therefore, the limiting rate into the halfband for the chip is PROCCLK/7. This gives us the following halfband limits:

Standard (Using 64 MHz Clock; PROCCLK = 32 MHz):
Max. Input to Halfband Filter = 32 MHz/7 = 4.571 MHz

Maximum (Using 55 MHz Clock; PROCCLK = 55 MHz):
Max. Input to Halfband Filter = 55MHz/7 = 7.857 MHz

The usable bandwidth out of the halfband filter that guarantess a negligible (< –84dBc) alias–induced degredation of dynamic range is approximately 1/4 of the output rate of the halfband filter.

F.4 Calculating the Output Rate Using the Standard 64 MHz Clock

This example illustrates how we calculated the maximum output sample rate using the standard 64 MHz crystal (PROCCLK = 32 MHz). In this example, 2 halfband filters are activated, and the re–sampling filter is not used. Other configurations using 1 or 5 halfband filters would require a different number of clocks, resulting in a different output rate.

17 clocks are required to generate the filter output, so that the input rate into the interpolation filters is 32MHz/17 = 1.882 MHz. The output rate is four times this:

Output Sampling Rate = 4 x 1.882MHz = 7.53 MHz

F.5 Calculating the Low Pass Bandwidth Using the Standard 64 MHz Clock

This example illustrates how we calculated the maximum low pass bandwidth using the standard 64 MHz crystal (PROCCLK = 32 MHz). Once again, 2 halfband filters are activated, and the re–sampling filter is not used.

The Low Pass Bandwidth is equal to 1/8 of the halfband input rate. For the 64 MHz clock (32 MHz PROCCLK), the halfband input rate is 4.571 MHz, so the bandwidth is:

Low Pass Bandwidth = 4.571MHz/8 = 571 KHz usable full dynamic range bandwidth

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F.6 Additional Information/References

Intersil's Data Sheet #4450.2 "HSP50214B Programmable Downconverter", 2/99 is included as Appendix A of this manual.

You may also visit Intersil Corp.'s web site at www. intersil.com for the latest information, and documents referenced here:

Intersil Technical Brief TB349.1 "Calculating the Maximum Output Sample Rate and Bandwidth Specifications of the HSP50214", 1/99

Intersil Application Note AN9720.2 "Calculating Maximum Processing Rates of the PDC (HSP50214, HSP50214A and HSP50214B)", 1/99

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