Pentek 6441

Dual Channel A/D VMEbus Systems Converter

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OPERATING MANUAL

PENTEK MODEL 6441

Dual Channel, 41 MHz, 12-bit,
A/D Converter for VMEbus Systems

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Pentek Model 6441 Operating Manual
Revision History

Date	Rev	Applicable Serial #'s	Comments
02/22/96	Preliminary	9607001 - Forward	Initial product release
09/09/96	A	9607001 - Forward	Add info on Option 002 (Differential Outputs). Correct HEX column of Table 2-5 to properly indicate 12-bit outputs (FFF, not 3FFF). Step size is ≅ 490 µV, not 49 µV as stated in Section 2.3.3 (Table 2-5 reported this correctly).
03/12/98	B	9607001 - Forward	Changed the second Table 2-5 to Table 2-6. Changed the second Figure 2-3 to Figure 2-4. Corrected various typographical errors and turned various sections from passive voice into active voice. Added sections 2.3.4, 2.4 and 2.5. Moved option 002 front panel to appear after section 2.3.4.
04/22/98	C	9607001 - Forward	Added Option -030 to specifications section. Removed statement in Specs about allowing ECL External clocking. Changed sample clock logic to 2 V p-p, from 800 mV p-p. Added AC coupling information to sec. 2.3.2. Changed the analog input frequency to 10 kHz from 1 kHz.
03/02/99	D	9607001 - Forward	Corrected section 2.2.4 jumper and switch configurations for DIP switch - SW2
03/17/99	D.1	9607001 - Forward	Removed Sec. 1.7, G-link option. Consolidated Fig. 2-4 with Fig. 2-2. Revised Section 2.2.5, explains function of jumper blocks JB1 and JB2 in greater detail. Modified Table 2-7; more detailed. Deleted Section 2.5, Fig. 2-8 and Table 2-8.
04/20/99	D.2	9607001 - Forward	Figure 2-7, corrected pin assignments for option 002 to show the correct complement outputs.
03/01/00	E	9934001 - Forward	Added Sect. 1.6, Option 002. Changed Figures 2-2, 2-3 & 2-4 to reflect PC board changes (references throughout the entire manual also reflect these changes). Sec. 2.2.1, jumper blocks are now located outside the cans. Sec. 2.2.2, JP5 is now a three pin jumper. Added sect 2.2.5, Registered Mode Jumper. Revised Sec. 2.3, added sections describing Front Panels and functions of Options 008 and 101.

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Chapter 1: General Information

1.1 Introduction

Pentek's Model 6441 is a dual channel, high−speed, 12−bit A/D converter board that operates at sampling rates up to 41 MHz. It is a single−slot, 6U VMEbus board, and includes signal conditioning and clock generation circuitry. The two channels are identical and operate from the same sample clock.

Among its other uses, the Model 6441 is intended as a front end for the Pentek Models 4271, 4272 and 65xx Digital Receivers. Connections between the Model 6441 and these receivers are made with a standard 80−conductor, 0.025 in. pitch, flat ribbon cable, using supplied mating connectors. Cable assemblies are also available from Pentek.

1.2 Signal Conditioning

Each analog input accepts a ±1.0 V full scale signal from a front panel SMA connector with a 50 Ω input termination. A buffer amplifier then delivers the signal to a high−order Chebyscheff, low−pass anti−aliasing filter, which restricts input bandwidth to approximately 16 MHz. Other input filter characteristics are available on special order.

For systems in which the input signal is already bandlimited, the on−board anti−aliasing filter can be bypassed.

1.3 A/D Conversion

The Model 6441's A/D converter has resolution of 12 bits. Digitized data from both channels are available on each of two front panel 80−pin connectors. In the standard configuration of this device, separate TTL−level driver stages are provided for each channel to support more flexible connectivity to different configurations of digital receivers. In units equipped with Option 002, differential ECL drivers replace the TTL output stages.

1.4 Sample Rate Control

The sample clock generator is a 40 MHz crystal oscillator, in a standard DIP package. This oscillator is socketed, to support user replacement for special frequencies.

Alternatively, an external TTL, ECL or analog sample clock signal can be supplied through a front panel SMA connector. The A/D converter used on this unit is specified to operate at sample frequencies up to 41 MHz. This maximum sample rate is achievable only by using the external clock input. Selection of the internal oscillator or the external clock is made with an on−board DIPswitch.

NOTE

The Minimum Sample Rate on the Model 6441 is 5 MHz.

1.5 FPDP Output (Option 008)

A FPDP (front panel data port) transmit module, Option 008, can be ordered to provide a high−speed parallel TTL output interface.

FPDP is a popular industry standard interface utilized by several manufacturers for high−speed data transfers between system peripherals, array processors, and data acquisition devices.

1.6 ECL Logic (Option 002)

An ECL Logic version of the Model 6441, Option 002, can be ordered. This option pro−vides a differential ECL interface, for increased noise immunity.

1.7 VME Interface

The VMEbus interface is used only to supply power to the Model 6441. No VMEbus sig−nals are used on the board, and no VME−programmable functions exist in the unit. The board does, however, pass along the daisy−chained VMEbus signals.

1.8 Block Diagram

A block diagram of the Pentek Model 6441, Dual–Channel, 41 MHz, 12–bit A/D Converter for VMEbus systems is presented in Figure 1–1, below.

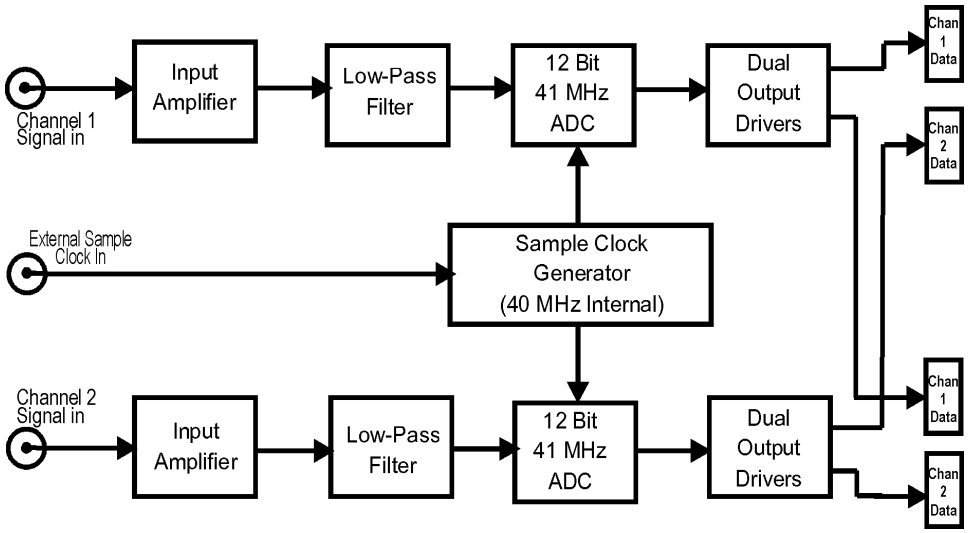


Figure 1-1: Model 6441 - Block Diagram

1.9 Specifications

Analog Inputs:

Number:	2
Type:	Single–Ended, SMA connector
Full Scale Signal:	± 1 V (2.0 V_{P-P})
Bandwidth:	10 kHz – 20 MHz (using internal 40 MHz clock)
	10 kHz – $f_{clk}/2$ (where f_{clk} is the sample clock freq.)
Option –030:	Bandwidth extended to 60 MHz
Impedance:	50 Ω
Coupling:	AC

Input Filters:

Number:	2
Passband:	DC ≥ f ≥ 16 MHz
Passband Flatness:	± 1.0 dB
Stopband:	f ≥ 24 MHz
Stopband Attenuation:	> 50 dB
Bypassing:	inserted or removed from circuit via jumper placement

1.9 Specifications (continued)

Analog to Digital Converters:

Number:	2
Type:	Analog Devices AD9042
Resolution:	12 bits
Sampling Rates:	5MHz to 41 MHz
Spur–Free Dynamic Range:	≥ 70 dB
SINAD:	≥ 60 dB
Signal/Noise Ratio:	≥ 50 dB

Sampling Clock:

Internal:	40 MHz crystal oscillator installed, switch selectable and user replaceable. Other frequencies available by special order.
External:	
Connector:	Front Panel SMA
Input Impedance:	50 Ω
Coupling:	AC
Bandwidth:	10 kHz – 65 MHz
	NOTE: Minimum Sample Rate is 5 MHz
Signal Levels:	Single–Ended or Differential (Jumper selection) Positive, negative or bipolar signals can be applied
Amplitude:	Min: 500 mV_{P-P} Max: 5 V_{P-P}
Logic:	TTL, ECL or Analog Signal

Power:	Standard	Option 002
+ 5 VDC:	1.00 A	1.00 A
+12 VDC:	0.75 A	1.00 A
– 12 VDC:	1.00 A	1.25 A

Dimensions:	Standard 6U VMEbus board
Depth:	160.0 mm (6.3 in.)
Height:	233.5 mm (9.2 in.)
Panel Width:	20.3 mm (0.8 in.)

Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at (201) 818–5900. Please save the original shipping container and packing material, in case reshipment is required.

2.2 Jumper and Switch Configurations

All user–selectable operating parameters of the Model 6441 are controlled by the settings of jumper blocks and DIPswitches on the PC board. Jumper blocks JP1, JP2, JP3, JP4 and JP6 are dual–inline, surface–mounted components. Jumper Blocks JP5, JP7 and JP8 (there is no jumper block JP8 on Option 008) are single–in–line surface–mount. Pin 1, for both styles of jumper blocks, is indicated on the board both by the numeral '1' and by a notched corner on the screened symbol beneath the block.

The pin numbering scheme for the dual–inline surface–mount jumper blocks is shown in Figure 2–1, below. The shorting jumpers used with these jumper blocks are low profile, and have their pins spaced on 2 mm centers. The Pentek part number for the jumpers that fit these blocks is 356.00015.

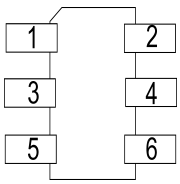


Figure 2-1: Model 6441 - Dual-In-Line Jumper Block Pin Numbering

2.2 Jumper and Switch Configurations (continued)

The shorting jumpers used with single inline surface-mount jumper blocks have their pins spaced on 0.1 inch centers. The Pentek part number for the jumpers that fit these blocks is 356.00001.

If the jumpers supplied with your unit should become lost, contact Pentek at (201) 818–5900, and we will gladly replace them for you.

The Model 6441 contains two jumper blocks for each channel that determine whether or not the low-pass, anti-aliasing input filter is present in the circuit. Another jumper block, common to both channels, configures the board to accept either a single-ended or differential reference clock signal from the front panel's EXT CLK IN connector (if this signal path is enabled). Some configurations have an additional jumper block that determines whether the output data is registered or not. One of the two DIPswitch blocks (SW1) determines the quantity that the reference clock will be divided by to create the sampling clock frequency, and the other (SW2) performs several configuration functions. The locations of the jumper blocks, DIPswitches, and other circuit elements of interest for the TTL, FPDP and ECL options are shown in Figures 2–2, 2–3 and 2–4 on pages 11, 12 and 13 respectively. Settings for the jumper blocks and DIPswitches will be discussed in the following sections.

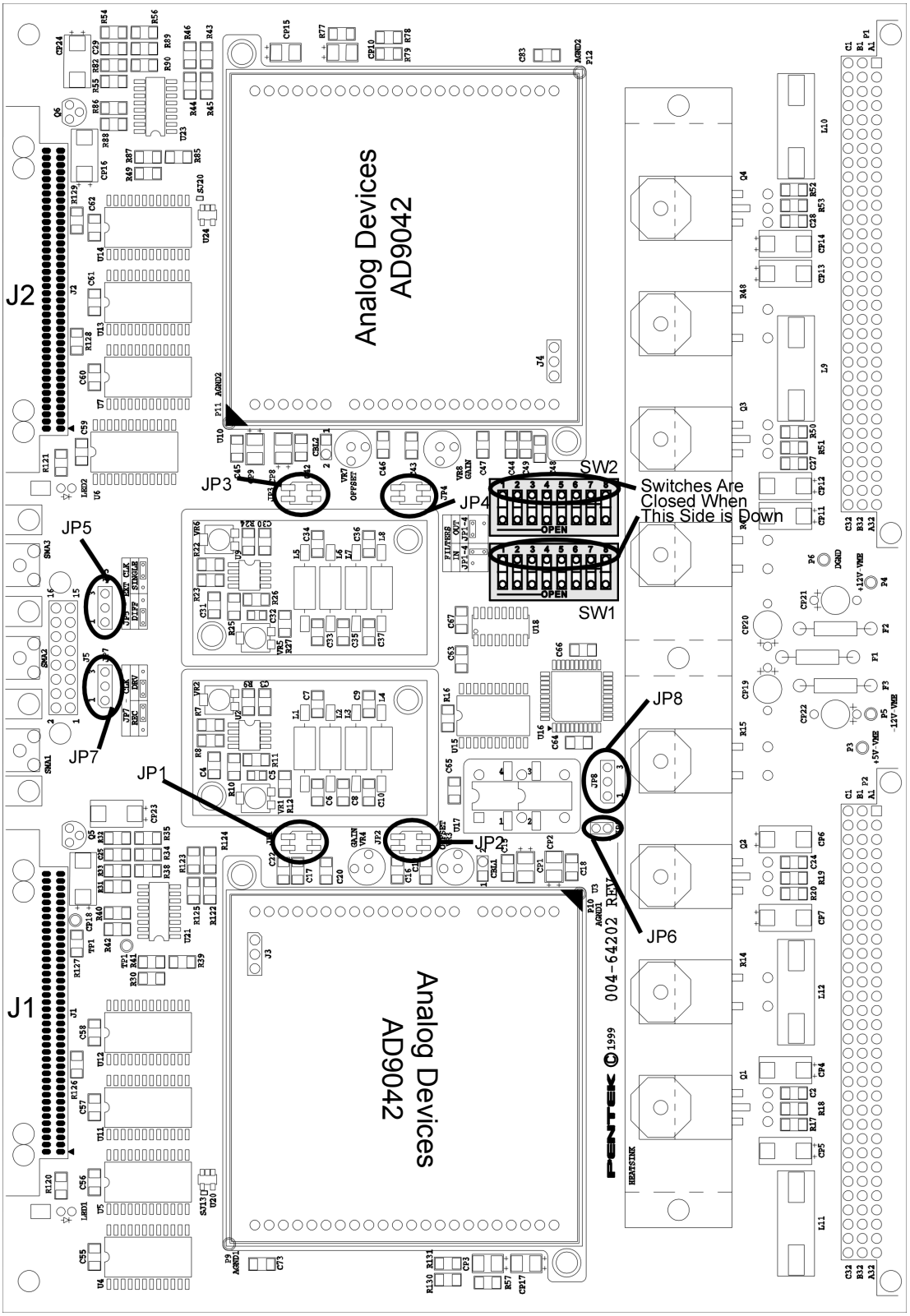


Figure 2-2: Model 6441 - Standard Configuration -
PC Board Drawing Showing Jumper Block and Component Locations

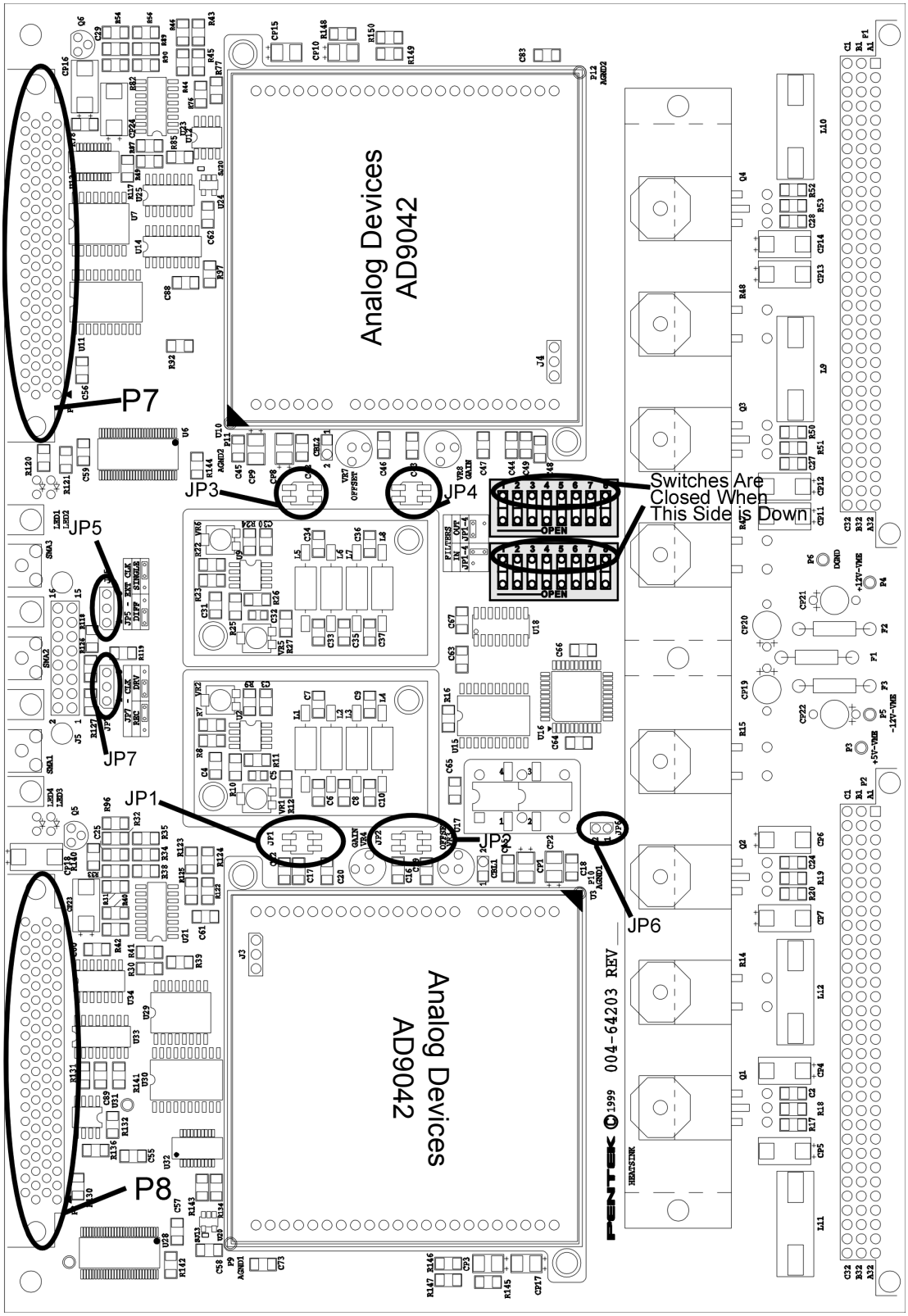


Figure 2-3: Model 6441 - Option 008 (FPDP) -
PC Board Drawing Showing Jumper Block and Component Locations

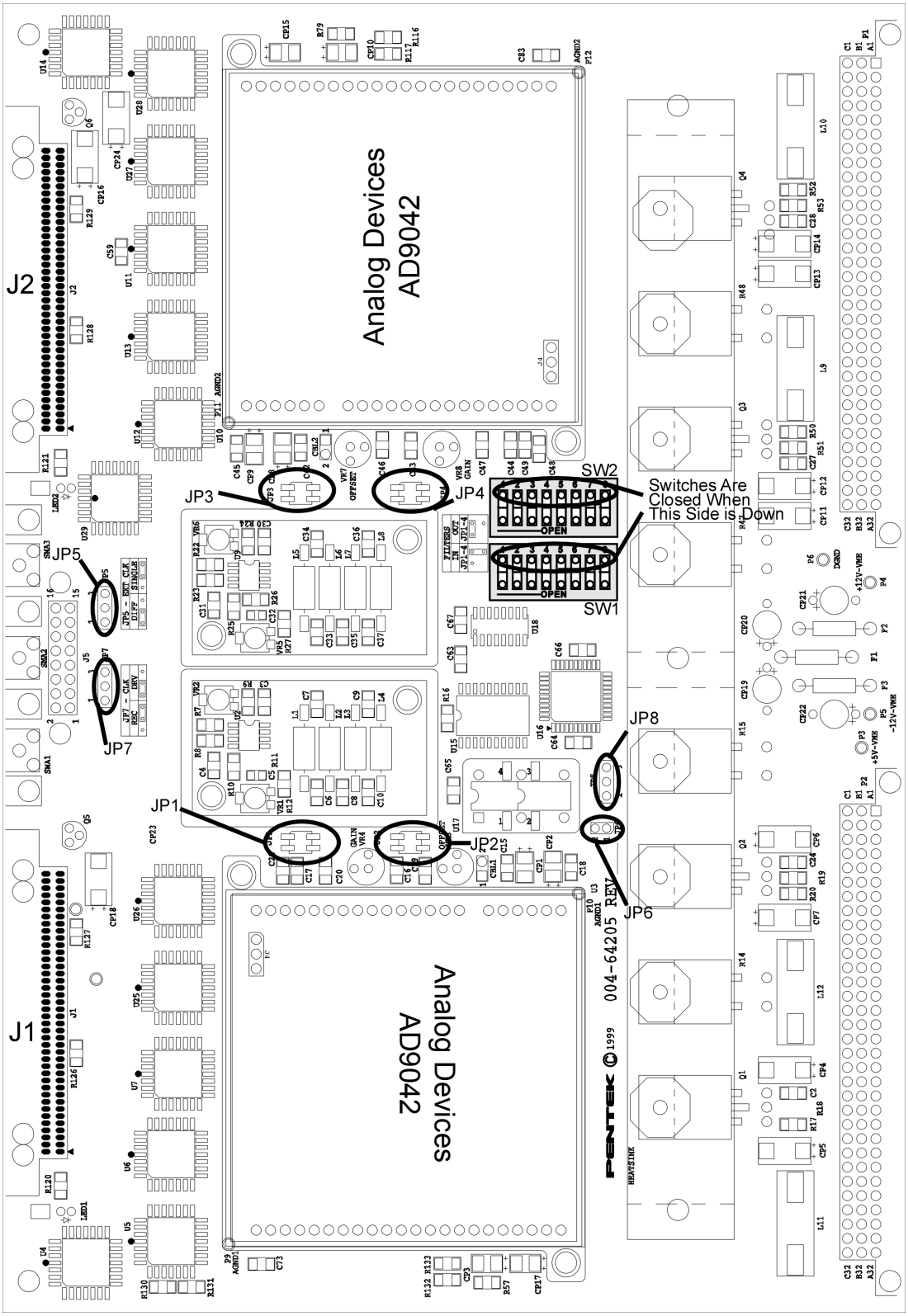


Figure 2-4: Model 6441 - Option 002 (ECL) -
PC Board Drawing Showing Jumper Block and Component Locations

2.2 Jumper and Switch Configurations (continued)

2.2.1 Filter Install/Bypass Jumper Blocks - JP1 thru JP4

The default configuration of these jumper blocks is to have the filters installed. This means that jumpers are placed between pins 1 & 2 of all four of these jumper blocks (JP1 & JP2 for channel 1, and JP3 & JP4 for channel 2). To bypass the filter (i.e., remove it from the circuit and allow the full bandwidth of the input signal to pass), place the jumpers between pins 1 & 3 at all four locations. The fourth pin on these jumper blocks is unused. Figure 2-5, below, shows how the jumpers are positioned in the input circuit, and Table 2-1, below the figure, summarizes the settings. There also is a chart included on the 6441 PC card, between the DIPswitches and the filter for channel 2, that shows how to set these jumpers. This chart is found on the standard Model 6441 as well as the ECL (Option 002) and FPDP (Option 008) versions.

Note that a jumper MUST be installed on each of these four jumper blocks, and that both jumper blocks for a given channel must have the jumper installed in the same position, or no signal will be delivered to the A/D Converter.

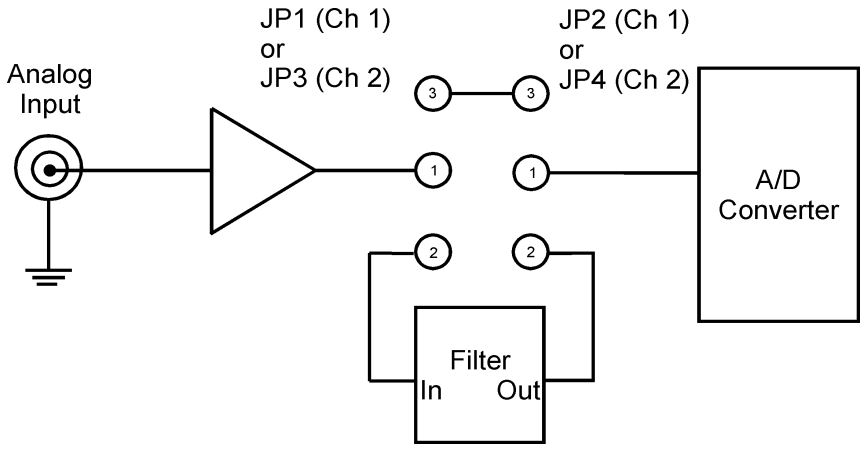


Figure 2-5: Model 6441 - Filter Install/Bypass Jumpers

Table 2-1: Model 6441 - Filter Install/Bypass Jumpers - JP1 & JP2 (Channel 1) and JP3 & JP4 (Channel 2)

Jumper Position	Filter State
1 - 2*	Installed*
1 - 3	Bypassed

* Factory Default Setting
Note: Pin #4 is unused on all four of these jumper blocks

2.2 Jumper and Switch Configurations (continued)

2.2.2 Clock Input Type Select Jumper Block – JP5

Jumper block JP5 allows the user to configure the board for either a single–ended or differential clock input signal. If a jumper is installed between pins 1 & 2 of JP5, the shielded, outer portion of the front panel's EXT CLK IN connector is isolated from ground, and connected to the "–" input of a line receiver. This allows the Model 6441 to receive a differential clock signal. (The above is also true if no jumper is installed on JP5.)

If a jumper is installed between pins 2 & 3 of JP5, then the shield of the input connector and the "–" input of the line receiver are grounded. In this configuration, the Model 6441 accepts single–ended signals at this connector. Note that if this input connector will be used, a jumper MUST be installed in one of the two positions on this jumper block. If no jumper is installed on JP5, the shield and the receiver's "–" input simply float, which will result in poor signal integrity.Table 2–2, below, summarizes the settings of jumper block JP5. There is also a chart on the 6441 PC card, between the front panel EXT CLK IN connector and the filter networks, that shows how to set this jumper.

Table 2-2: Model 6441 - External Clock Type Select Jumper - JP5

Signal Type	Jumper position
Single-Ended*	2 - 3*
Differential	1 - 2
* Factory Default Setting	

2.2.3 Oscillator Disable Jumper - JP6

JP6 is a 2-pin jumper block which, when a jumper is installed, connects the on-board crystal oscillator to the +5 V supply rail. When using the A/D converter with an external clock signal, this jumper should be removed to disable the on-card oscillator, which can add unwanted frequency components to the digitized output signal if left active. Table 2-3, below, summarizes the settings of JP6.

Table 2-3: Model 6441 - Oscillator Disable Jumper - JP6

Jumper Installed*	Jumper removed
Oscillator Enabled*	Oscillator Disabled
Install to use Internal Sample Clock	Remove to use External Sample Clock
* - Factory default setting	

2.2 Jumper and Switch Configurations (continued)

2.2.4 Internal Sample Clock Output Jumper - JP7

Placing a jumper between pins 1 and 2 of jumper block JP7 selects the internal sample clock as an output. Placing a jumper between pins 2 and 3 of jumper block JP7 allows the Model 6441 to accept an external clock signal.

On units not equipped with Option 101, the SMA connector at the center of the Model 6441's front panel, labeled EXT CLK IN, is used for either the clock input or the clock output, depending upon the setting of this jumper.

On units equipped with Option 101, pin 3 of the 15 pin Micro D connector is used for the sample clock output when JP7's jumper is between pins 1 & 2. Pin 3 of the 15 pin Micro D connector is used an input for the positive external differential clock signal when JP7's jumper is between pins 2 & 3, and pin 10 is the input for the negative external differential clock signal.

NOTE

The clock output mode is not available on Model 6441 Option 002 (ECL outputs)

2.2.5 Registered Mode Jumper – JP8

The Model 6441 provides a registered output mode, in which the output timing relationships are fixed. This mode is available when a jumper is placed between pins 2 and 3 of jumper block JP8 (the factory default setting). When configured in this manner, the only settings of SW2 that affect the output timing are switches 1 and 7, which determine reference clock settings. This is the recommended operating mode for all new applications.

If you will be using your new Model 6441 in an existing application, and depend upon a certain timing relationship at the output based on customized settings of SW2 (see Section 2.2.7 on page 19) place the jumper on JP8 between pins 1 and 2. This will enable a backward-compatible operating mode, in which the timing relationships can be changed by the DIPswitches.

NOTE

1) **The Model 6441 Option 002 (ECL outputs) ALWAYS operates in registered mode, regardless of the setting of JP8.**

2) **The Model 6441 Option 008 (FPDP) ALWAYS operates in registered mode. There is no Registered Mode Jumper (JP8) on Option 008.**

2.2 Jumper and Switch Configurations (continued)

2.2.6 Sample Rate Divider DIPswitch - SW1

The sampling clock for the Model 6441 is created by passing a reference clock signal through a frequency divider. The reference clock signal is either the on-board crystal oscillator, whose frequency is 40 MHz in the standard configuration, or a signal applied to the EXT CLK IN connector on the unit's front panel. The reference clock is selected by one of the switches on the SW2 DIPswitch block, and will be discussed in the Section 2.2.7 on page 19. The divider is set by SW1.

SW1 is a DIPswitch block containing eight switches. Each of these eight switches carries a binary weight, from 2^0 (=1, the switch closest to the filters) to 2^7 (=128, the switch closest to the heatsink). A switch in the SW1 block is closed when the side of the switch nearest to SW2 is down. The locations of SW1 and SW2 for the TTL, FPDP and ECL options are shown in Figures 2-2, 2-3 and 2-4 on pages 11, 12 and 13 respectively. Closing a switch clears the bit associated with it to the logic '0' state, and opening a switch sets the associated bit to the logic '1' state.

The clock divisor is equal to the binary value of the settings of these eight switches plus one. Thus, there are 256 different divisor settings that can be achieved with this switch, from 1 to 256. If the on-card, 40 MHz oscillator is used as the reference clock source, this allows for 256 different sample clock rate settings, from 40 MHz to 156.25 kHz. Table 2-4 on page 18, gives the switch settings for the 16 highest frequencies available using the on-card oscillator, the frequencies that will be obtained when each of the upper four switches is the only one opened, and when all are opened.

2.2 Jumper and Switch Configurations (continued)

Sample Rate Divider DIPswitch - SW1 (continued).

Table 2-4: Model 6441 - Sample Clock Divider - DIPswitch SW1 - Sample Frequencies Using 40.00 MHz Reference Clock

Switch # & Setting (0 = Closed, 1 = Open)								Clock Divider	Sample Frequency
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	1	40.000 MHz
0	0	0	0	0	0	0	1	2	20.000 MHz
0	0	0	0	0	0	1	0	3	13.333 MHz
0	0	0	0	0	0	1	1	4	10.000 MHz
0	0	0	0	0	1	0	0	5	8.000 MHz
0	0	0	0	0	1	0	1	6	6.667 MHz
0	0	0	0	0	1	1	0	7	5.714 MHz
0	0	0	0	0	1	1	1	8	5.000 MHz
0	0	0	0	1	0	0	0	9	4.444 MHz
0	0	0	0	1	0	0	1	10	4.000 MHz
0	0	0	0	1	0	1	0	11	3.636 MHz
0	0	0	0	1	0	1	1	12	3.333 MHz
0	0	0	0	1	1	0	0	13	3.077 MHz
0	0	0	0	1	1	0	1	14	2.857 MHz
0	0	0	0	1	1	1	0	15	2.667 MHz
0	0	0	0	1	1	1	1	16	2.500 MHz
0	0	0	1	0	0	0	0	17	2.353 MHz
0	0	1	0	0	0	0	0	33	1.212 MHz
0	1	0	0	0	0	0	0	65	615.385 kHz
1	0	0	0	0	0	0	0	129	310.077 kHz
1	1	1	1	1	1	1	1	256	156.250 kHz

2.2 Jumper and Switch Configurations (continued)

2.2.7 Device Configuration DIPswitch - SW2

The DIPswitch labeled SW2 may be used to configure certain operating modes of the Model 6441. SW2 Switch 6 and 8 are unused. Settings for the remaining switches are dependent on the digital receiver used, and on the setting of the Registered Mode Jumper (JP8, see Section 2.2.5 on page 16). We strongly recommend that you use the registered mode in new applications. If the unit is NOT configured for registered mode, the user may wish to experiment with these settings to determine which ones work for their specific application.

A switch in the SW2 DIPswitch block is closed when the side farthest from SW1 is pressed down. For reference, Switch 8 is closest to the heatsink. The subsections below describe the functions of each switch in the SW2 DIPswitch block. Switches 1 and 7 are discussed first, since there are conditions in which their combined settings are important. Factory default settings for SW2 are shown in Table 2-5, below.

Table 2-5: Model 6441 - Device Specific, Factory Preset DIPswitch Settings - SW2

Switch #	Function	Setting
1	Reference Clock Select	Closed (0)
2 & 3	Time & Channel Packing (Opt. 008 Only)	Open (1)
4	Channel 1 Edge Select	Closed (0)
5	Channel 2 Edge Select	Closed (0)
6	Reserved	Closed (0)
7	External Input Function Select	Open (1)
8	Reserved	Open (1)

2.2.7.1 Reference Clock Select - SW2, Switch 1

This switch determines whether the internal, 40 MHz crystal oscillator or a signal applied to the front panel's EXT CLK IN connector is used as the source of the reference clock. The reference clock is delivered to the clock divider, programmed by SW1 (see Section 2.2.6 for details), whose output is used as the sampling clock signal.

To select the 40 MHz on-card oscillator as the reference clock source, switch 1 on the SW2 DIPswitch must be closed. To select the signal applied to the EXT CLK IN connector on the front panel, switch 1 on the SW2 DIPswitch must be open. Note that if the external source is to be used as the reference, switch 7 of SW2 must be open, to select the clock reference function for the input (see Section 2.2.7.2). Also note that switch 1 is functional regardless of the settings of the registered mode jumper (see Section 2.2.5).

2.2 Jumper and Switch Configurations (continued)

2.2.7 Device Configuration DIPswitch - SW2 (continued)

2.2.7.2 Center Connector Function Select - SW2, switch 7

The SMA connector at the center of the Model 6441's front panel, labeled EXT CLK IN, can function either as a clock reference input, a sample clock output, or as an enabling gate signal for the internal sampling clock. The setting of the second switch from the end of the SW2 DIPswitch helps to determine the function of this connector.

To use the EXT CLK IN connector as a reference clock input or as a sampling clock output, switch 7 on SW2 must be open, to select the reference function for the input. See Section 2.2.4 and Section 2.2.7 for further information about selecting the reference clock input or sample clock output functions for this connector.

To use the EXT CLK IN connector as a sampling gate signal input, switch 7 of SW2 must be closed. In this case (unless your unit includes Option 101), the internal clock reference must be selected (since a clock reference signal and a gate signal cannot both be delivered through the same connector), by closing switch 1 of SW2.

Note that switch 7 is functional regardless of the settings of the registered mode jumper (see Section 2.2.5).

Table 2-6, below, summarizes the settings of switches 1 and 7 of DIPswitch block SW2.

Table 2-6: Model 6441 - Reference Clock and External Input Function Select Switch Settings - SW2, Switches 1 & 7

Switch 1 Setting	Switch7 Setting	Reference Source	Ext. Input Function	Sample Clock Operating Mode
Closed (0)	Closed (0)	Internal	Gate	Gated Internal Clock
Closed (0)	Open (1)	Internal	Reference	Internal Clocking-No Gate
Open (1)	Closed (0)	External	Gate	Gated External Clock **(Option 101 Only)**
Open (1)	Open (1)	External	Reference	External Clocking - No Gate

2.2 Jumper and Switch Configurations (continued)

2.2.7 Device Configuration DIPswitch - SW2 (continued)

2.2.7.3 Packing Mode Selection (Option 008 (FPDP Only) - SW2, Switches 2 & 3

Table 2-7, below, shows the settings for SW2, switches 2 and 3 for selecting the data packing mode on Model 6441 Option 008 (FPDP).

Table 2-7: Model 6441 - Packing Mode Selection - DIPswitch Settings - SW2

Switch 2	Switch 3	Mode
Closed (0)	Closed (0)	Time Packed
Closed (0)	Open (1)	One Channel Packed
Open (1)	Closed (0)	Invalid
Open (1)	Open (1)	Two Channels Packed

In One Channel packing mode:

- FPDP A Channel 2 data is routed to the upper 16 bits and the lower 16 bits. (Identical sample in upper and lower bits)
- FPDP B Channel 1 data is routed to the upper 16 bits and the lower 16 bits. (Identical sample in upper and lower bits)
- In Two Channel packing mode:
- FPDP A Channel 2 data is routed to the upper 16 bits of the 32-bit FPDP data output word. Channel 1 data is routed to the lower 16 bits of the 32-bit FPDP data output word.
- FPDP B Channel 1 data is routed to the upper 16 bits of the 32-bit FPDP data output word. Channel 2 data is routed to the lower 16 bits of the 32-bit FPDP data output word.

In Time packing mode:

- FPDP A Channel 2(t) is routed to the upper bits and Channel 2(t+1) is routed to the lower bits.
- FPDP B Channel 1(t) is routed to the upper bits and Channel 1(t+1) is routed to the lower bits.

2.2 Jumper and Switch Configurations (continued)

2.2.7 Device Configuration DIPswitch (continued)

2.2.7.4 Data Transfer Edge Select - SW2, Switches 4 & 5

Switches 4 and 5 are used to invert the Output Clock with respect to the data outputs. These switches are factory set according to the clock edge on which the data is transferred from the A/D Converter chip used on the card.

Setting switch 4 to the open position (1) inverts the Output Clock of Channel 1. Setting switch 5 to the open position (1) inverts the Output Clock of Channel 2. This function may be useful for custom interfacing.

The Model 6441 provides a registered output mode, in which the output timing relationships are fixed. This mode is available when a jumper is placed between pins 2 and 3 (the factory default setting) of jumper block JP8, see Section 2.2.5 on page 16. When configured in this manner, the only settings of SW2 that have an effect on the output timing are switches 1 and 7. This is the recommended operating mode for all new applications.

If you will be using your new Model 6441 in an existing application, and depend upon a certain timing relationship at the output based on customized settings of SW2, place the jumper on JP8 between pins 1 and 2. This will enable a backward-compatible operating mode, in which the timing relationships can be changed by the DIPswitches. The factory default settings of SW2, Switches 4 & 5 are shown in Table 2-5, on page 19.

NOTE

1) The Model 6441 Option 002 (ECL outputs) ALWAYS operates in registered mode, regardless of the setting of JP8 and SW2, Switches 4 & 5.

2) The Model 6441 Option 008 (FPDP) ALWAYS operates in registered mode. There is no Registered Mode Jumper (JP8) or Data Transfer Edge Select on Option 008 (FPDP).

2.3 Model 6441 Front Panels

The Model 6441 may be equipped with one of six available front panels. The front panel configuration is dependent upon the model options chosen at the time of purchase. There are three output options (Standard (TTL) Output, ECL Output (Option 002), Front Panel Data Port (FPDP) Output (Option 008)), and a 15–Pin Micro–D I/O Connector (Option 101) that may be combined with any of the output options.

The front panels on the Standard Output, ECL Output (Option 002) and the Front Panel Data Port (FPDP) Output (Option 008) models have three coaxial SMA connectors. One of these is for a common, externally applied reference clock or sampling gate signal, and the other two are the analog signal input connectors for the two channels.

The Standard Output and the ECL Output (Option 002) front panels have two male, 80–pin flat ribbon cable connectors, each of which carries the data outputs from both channels. The Model 6441 Option 008 has two Front Panel Data Ports (FPDPs) which each carry the data outputs for both channels.

The Model 6441 Option 101 has 15–Pin Micro–D I/O Connector that accepts reference clock signals and sampling gate signals along with some additional functions described in Section 2.3.3 on page 26. The Model 6441 Option 101 may be combined with any of the output options.

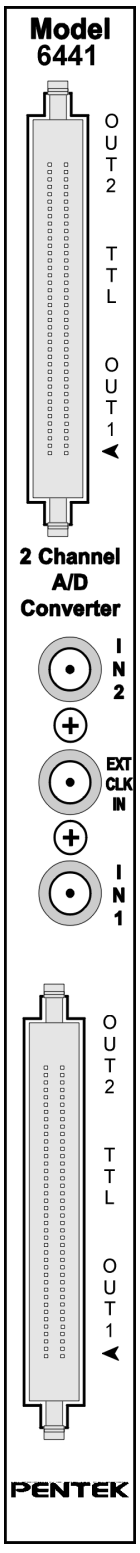


Figure 2-6: Model 6441 - Standard Front Panel

2.3 Model 6441 Front Panels (continued)

2.3.1 Analog Inputs

On the Standard Model 6441, ECL (Option 002) and FPDP (Option 008), the front panel SMA connectors labeled IN1 and IN2 are the Analog inputs. The SMA connector nearer to the top of the panel is the input to ADC channel 2, and the one nearer the bottom of the panel is the input to ADC channel 1.

The load impedance presented by these input connectors is 50 Ω. The input signal range is ± 1 V, i.e., a signal level of + 1 V will produce full scale positive output data (0x07FF), and a signal level of – 1 V will produce full scale negative output data (0x0800). (See Section 2.3.5 on page 32 for details about output data coding.) Input signal bandwidth for specified performance is from 10 kHz to 20 MHz, assuming a 40 MHz sample clock is used, or 10 kHz to *f*CLK/2 (where *f*CLK is the sample clock frequency) for sample clock rates lower than 40 MHz, with the input filter bypassed (see Section 2.2.1 on page 14). With the input filter installed, input bandwidth is reduced to 16 MHz.

Figure 2-7, below, provides a diagram of the analog input for the Model 6441.

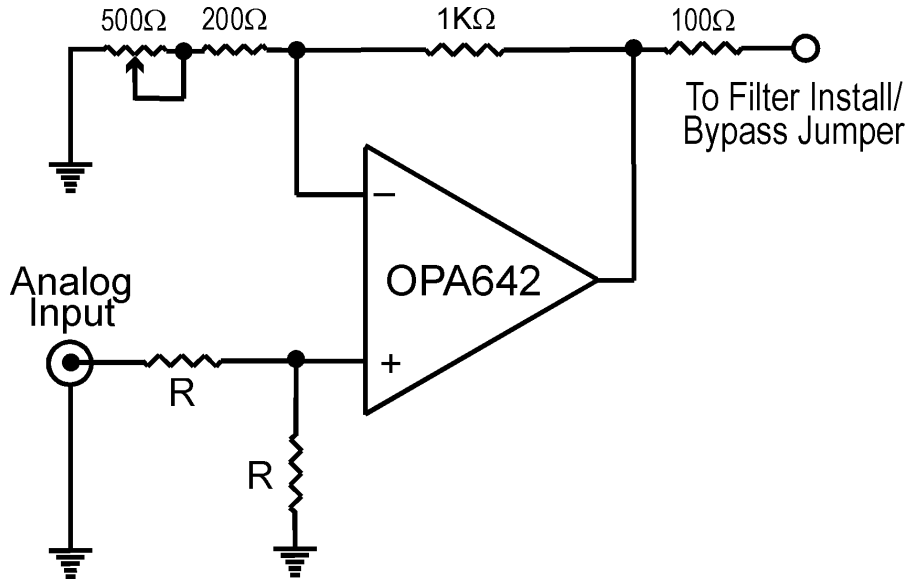


Figure 2-7: Model 6441 - Analog Input Circuit

2.3 Model 6441 Front Panel (continued)

2.3.2 External Clock Input

The SMA connector at the center of the Model 6441's front panel (for all input options, but NOT for Option 101) is for an external reference signal, which may be frequency divided to produce the sample clock. The signal applied here can also be used as an enabling gate signal for an internally-generated sample clock. When used as a gate, sampling is enabled when the gate input is at a logic low, disabled when it is at a logic high.

This input is selected when switch 1 of DIPswitch block SW2 is open. To select an external reference clock, switch 7 of DIPswitch block SW2 must be open. To select an external enabling gate signal, switch 7 of DIPswitch block SW2 must be closed (see Section 2.2.7 on page 19).

On units not equipped with Option 002 (ECL), the SMA connector can also be used as an output for the internal sample clock by placing a jumper between pins 1 and 2 of jumper block JP7 (see Section 2.2.4 on page 16).

When configured as an input, this connector is terminated in a 50 Ω impedance.

The 6441's external clock or enabling gate input may be driven by either TTL or ECL level logic signals, or by an analog signal. The minimum recommended signal amplitude at this input is 500 mV_{P-P}, and the maximum amplitude is 5 V_{P-P}. The maximum frequency for an external reference clock signal to the Model 6441 is 41 MHz

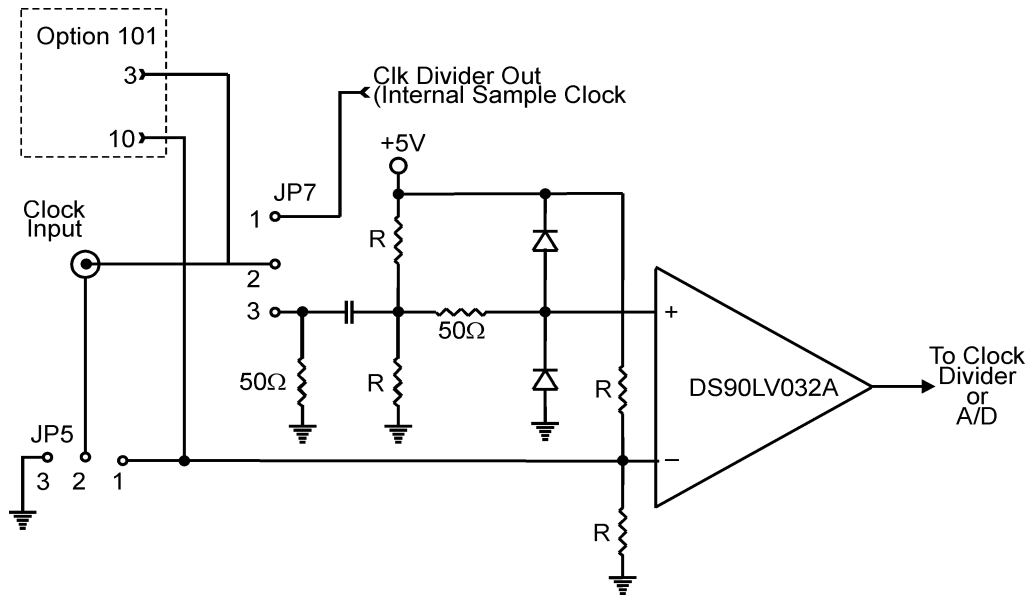


Figure 2-8: Model 6441 - Clock Input Circuit

2.3 Model 6441 Front Panel (continued)

2.3.3 Option 101: 15-Pin Micro-D I/O Connector

Model 6441 Option 101 provides a 15 pin micro D connector. Table 2-8, below, lists the signals present at each pin. The front panel of Mode 6441 Option 101 is shown in Figure 2-9, on the right. The orientation of the pins on the 15 pin micro D connector is shown in Figure 2-10 on page 27.

Table 2-8: Model 6441 - Option 101 - 15 Pin Micro D Connector Pin Assignments

Pin #	Signal
1	Channel 1 Gate In - pulled up with 10 kΩ
2	Channel 2 Gate In - pulled up with 10 kΩ
3	External Clk+ In (Clk– In at pin 10 when Diff. Clk is selected) or External Clk Out*
4	D-SS In** - directly drives pin 65 of top output connector (J2)
5	C-SS In** - directly drives pin 31 of top output connector (J2)
6	B-SS In** - directly drives pin 65 of bottom output connector (J1)
7	A-SS In** - directly drives pin 31 of bottom output connector (J1)
8	Divider Bypass External Differential Clk+ In (special option, otherwise NC)†
9	GND
10	Differential Clk– In (Clk+ In at pin 3)
11	GND
12	GND
13	GND
14	GND
15	Divider Bypass External Differential Clk- In (special option, otherwise NC)†

* Input if pins 2 and 3 are jumped on JP7; Output if pins 1 and 2 are jumped on JP7

** Not connected to SS for FPDP option

† Ext. Clk Out not available with this option; Clk In must be differential; Pin 3 becomes Ext. Clk Out (if selected) and Pin 10 is not connected

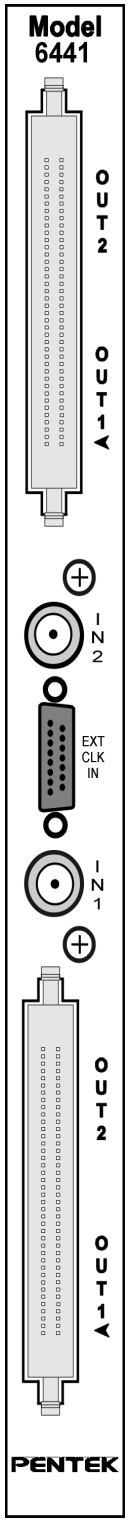


Figure 2-9: Model 6441 - Option 101 - 15 Pin Micro D Connector - Front

2.3 Model 6441 Front Panel (continued)

2.3.3 Option 101: 15-Pin Micro-D I/O Connector (continued)

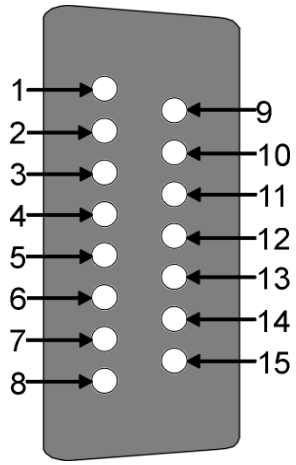


Figure 2-10: Model 6441 - Option 101 - 15 Pin Micro D Connector - Pin Numbering

2.3.3.1 Reference Clock Input (Pins 3 & 10)

In Option 101 for the Model 6441, these two pins take the place of the EXT CLK IN SMA connector on the standard unit. Please refer to Section 2.3.2 and Figure 2-8, both found on page 25, for details.

2.3.3.2 Sample Clock Input (Pins 8 & 15)

A "Clock Divider Bypass Option" exists, which allows for a differential clock to bypass the clock divider circuit of the Model 6441. With this option, pin 8 accepts the Differential "Clk+ In" signal and pin 15 accepts the Differential "Clk– In" signal. Pins 3 and 10 are not connected with this option. There is no clock out selection available with this option.

At the time of this writing, there is no option order number available for the "Clock Divider Bypass Option". This "special option" must be ordered in conjunction with Option 101. Please contact Pentek at (201) 818-5900 for more information on this option.

2.3 Model 6441 Front Panel (continued)

2.3.3 Option 101: 15-Pin Micro-D I/O Connector (continued)

2.3.3.3 Gate Inputs (Pins 1 & 2)

Pins 1 and 2 of the 15 pin micro D connector serve as gate inputs for the Model 6441 Option 101. A signal sent to one of these inputs can be used as an enabling gate for the internal sampling clock. Pin 1 is the gate input for channel 1 and Pin 2 is the gate input for channel 2. Selection of the gate input function is described in Section 2.2.7.2 and Table 2-6 on page 20.

The gate input pins on Model 6441 Option 101 have two distinct advantages over model options with SMA connectors. The first is that separate gate signals for each input channel may be applied, as opposed to a shared common gate signal. The second advantage is that, in Option 101, an external clock signal and gate signals may be applied simultaneously. Model 6441s not equipped with Option 101 allow for either a gate signal or a clock signal, but NOT both.

2.3.3.4 System Sync Inputs (Pins 4 through 7)

Pins 4 through 7 of the 15 pin micro D connector serve as System Sync inputs for the Model 6441 Option 101. These System Sync signals are not functionally used by the Model 6441 but serve as a convenient way to accept and pass on system signals to Pentek's 65xx digital receiver product family. Table 2-9, below, shows the pin-in and pin-out information for these four pins.

Table 2-9: Model 6441 - Option 101 - Sync Pin Assignments

Input Pin #	Function	Output Pin#	Connector
4	D-SS In	65	top output connector (J2)
5	C-SS In	31	top output connector (J2)
6	B-SS In	65	bottom output connector (J1)
7	A-SS In	31	bottom output connector (J1)

2.3 Model 6441 Front Panel (continued)

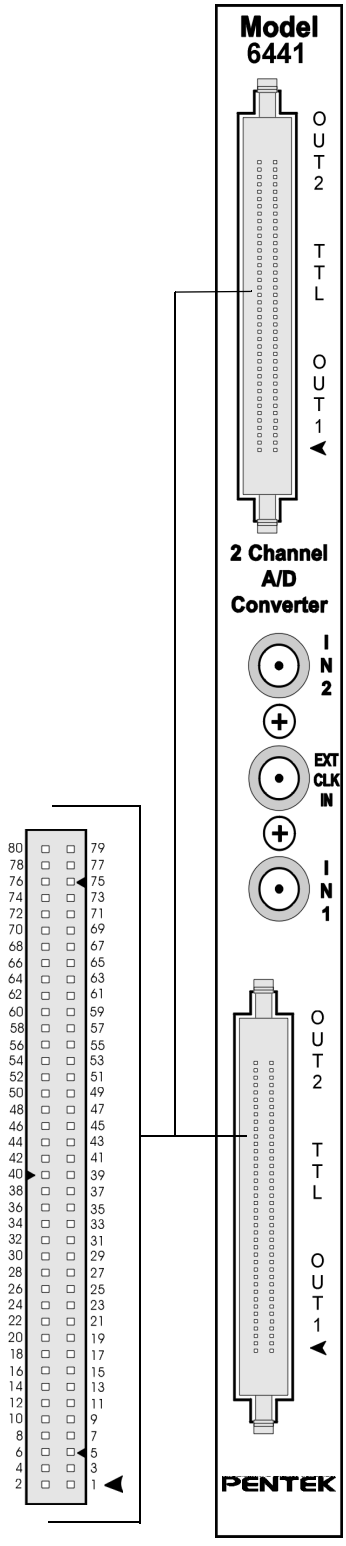
2.3.4 Standard TTL Data Output Stage

The output devices on the standard Model 6441 are 74FCT652 gates. Pin assignments for the standard output configuration of Pentek's Model 6441 are shown in the table on the left side of Figure 2-11, on page 30. The mating flat cable socket connector is 3M part number 82080-6006, and the strain relief is 3M part number 3858-080. The recommended 0.025" pitch flat cable is 3M part number 3756/80. An 80-wire ribbon cable with two 80-pin connectors is available from Pentek as Model 2117; this cable may be used to connect the 6441 to the standard versions of Pentek Digital Receiver Models 6505, 6508, 6510, 6514 and 6516, and to Model 6526 Option 019 (these models are equipped with TTL input stages). This cable may also be used to connect to the Wideband input (Channel C) on the 4272, Option 019 **IF, AND ONLY IF, THE OUTPUT STAGE OF THE 4272 IS DISABLED**. If you will be using the 6441 as a front end for a 4272 and need to drive the Wideband input and use the outputs, please contact Pentek at (201) 818-5900 to discuss custom cabling.

The Model 6441 can also be used with the Model 4271 Digital Receiver MIX Module, and the standard version of the Model 4272, if a special cable is used. This is necessary because the Model 6441's connectors contain 80 pins each, while those on the digital receivers contain only 68 pins. An 80-pin to 68-pin ribbon cable is available from Pentek as Model 2119; this cable can also be used to connect the 6441 to Pentek Models 6504 and 6509 Digital Receivers, equipped with TTL Input stages.

Figure 2-12, on page 31, shows some cabling schemes for connecting the Model 6441 to the 4271 and 4272.

Pin Assignments for Standard 6441 -Top and Bottom Output Connectors			
80	GND	79	N/C
78	GND	77	N/C)
76	GND	75	N/C
74	GND	73	GND
72	GND	71	N/C
70	GND	69	Ch2 - CK
68	GND	67	Ch2 - AS
66	GND	65	Ch2 - SS
64	GND	63	Ch2 D11 out (MSB)
62	GND	61	Ch2 D10 out
60	GND	59	Ch2 D9 out
58	GND	57	Ch2 D8 out
56	GND	55	Ch2 D7 out
54	GND	53	Ch2 D6 out
52	GND	51	Ch2 D5 out
50	GND	49	Ch2 D4 out
48	GND	47	Ch2 D3 out
46	GND	45	Ch2 D2 out
44	GND	43	Ch2 D1 out
42	GND	41	Ch2 D0 out (LSB)
40	GND	39	GND
38	GND	37	N/C
36	GND	35	Ch1 - CK
34	GND	33	Ch1 - AS
32	GND	31	Ch1 - SS
30	GND	29	Ch1 D11 out (MSB)
28	GND	27	Ch1 D10 out
26	GND	25	Ch1 D9 out
24	GND	23	Ch1 D8 out
22	GND	21	Ch1 D7 out
20	GND	19	Ch1 D6 out
18	GND	17	Ch1 D5 out
16	GND	15	Ch1 D4 out
14	GND	13	Ch1 D3 out
12	GND	11	Ch1 D2 out
10	GND	9	Ch1 D1 out
8	GND	7	Ch1 D0 out (LSB)
6	GND	5	Ch1 D1 out
4	GND	3	
2	GND	1	N/C



The mating flat cable socket connector is 3M #82080-6006, and the strain relief is 3M #3858-080.

Two of each of these items are supplied with the Model 6441.

The recommended 0.025" pitch flat cable is 3M #3756/80

Figure 2-11: Model 6441 - TTL Outputs - Front Panel Output Connectors Pin Assignments

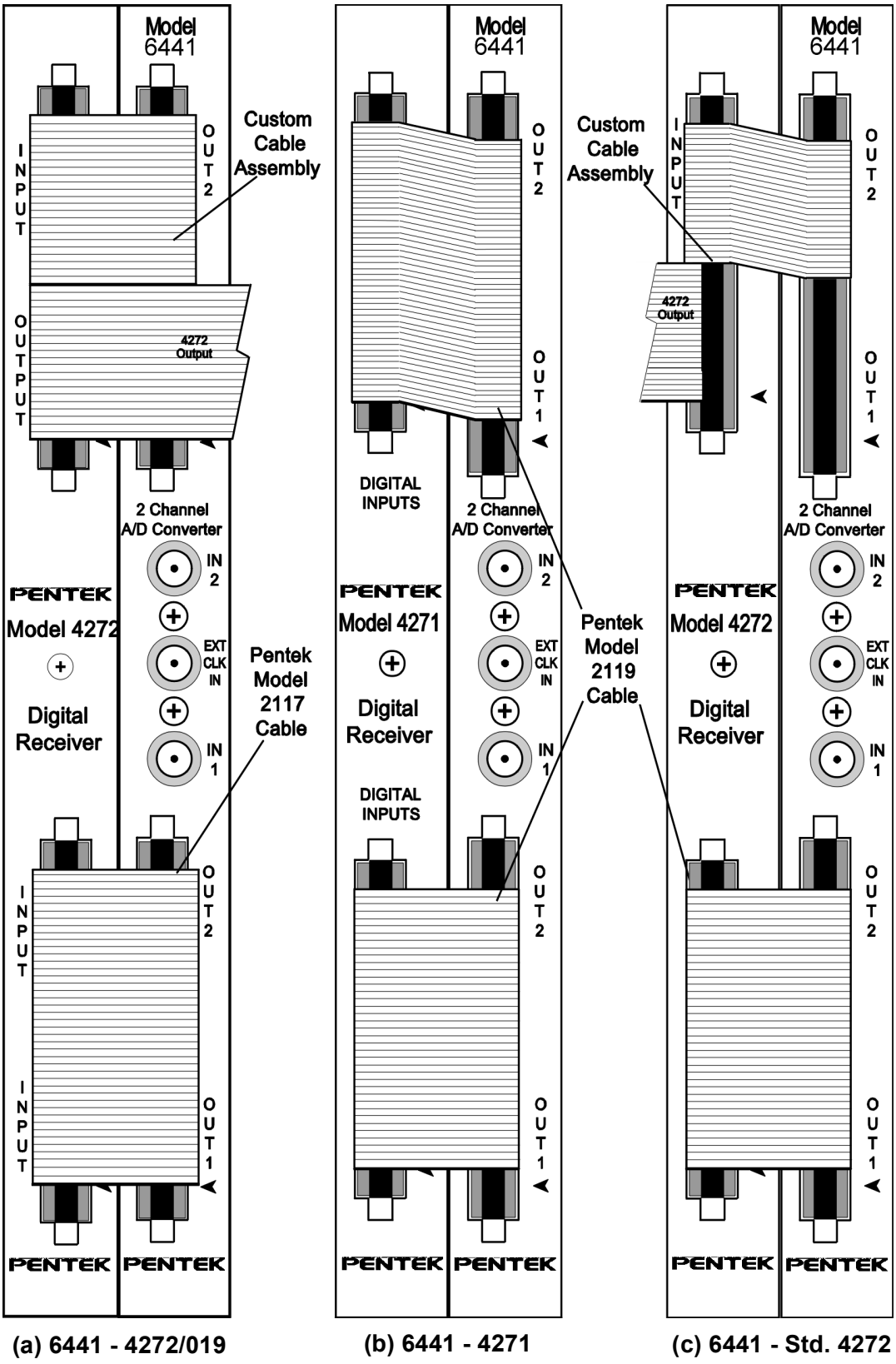


Figure 2-12: Cabling Schemes for Connecting the Model 6441 to the 4271 and 4272

2.3 Model 6441 Front Panel (continued)

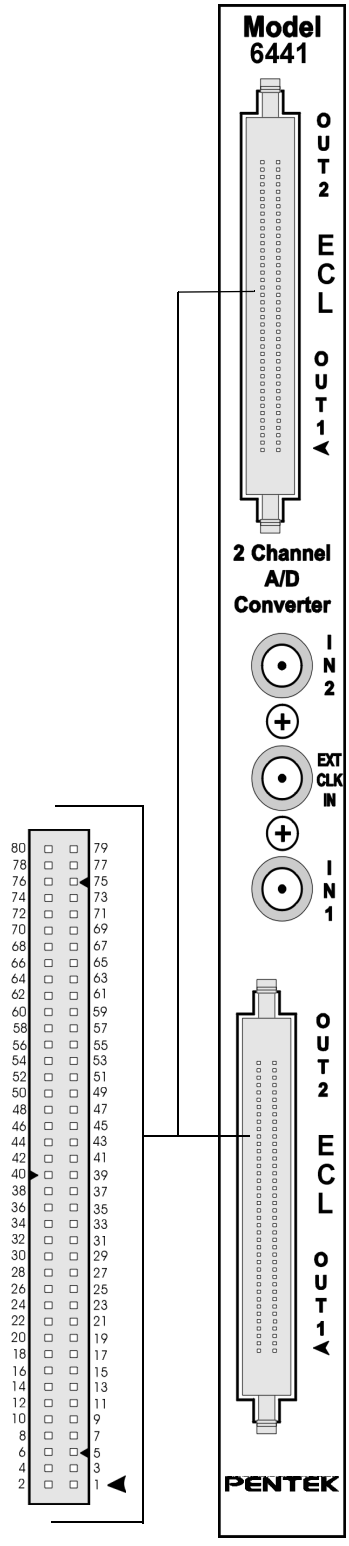
2.3.5 Option 002: ECL Data Output Stage

The output devices on the Model 6441 Option 002 (differential ECL) are MC10H604 TTL-to-Differential-ECL level translators. Pin assignments for the Model 6441 Option 002 are shown in the table at the left side of Figure 2-13, on page 33. The mating flat cable socket connector is 3M part number 82080-6006, and the strain relief is 3M part number 3858-080. The recommended 0.025" pitch flat cable is 3M part number 3756/80. An 80-wire ribbon cable with two 80-pin connectors is available from Pentek as Model 2117; this cable may also be used to connect the 6441 to Pentek Digital Receiver Models 6508 Option 012, 6510 Option 012, 6514 Option 012, 6526 Option 002 & 6532 Option 012 (these are equipped with differential ECL input stages).

The Model 6441 Option 002 can also be used with Option 012 of the Models 4271 and 4272 Digital Receiver MIX Modules, if a special cable is used. This is necessary because the connectors contain 80 pins each, while those on the digital receivers contain only 68 pins. An 80-pin to 68-pin ribbon cable is available from Pentek as Model 2119; this cable can also be used to connect the 6441 to Pentek Digital Receiver Models 6504 Option 012, and 6509 Option 004 or 012, which are equipped with differential ECL input stages.

Figure 2-12, on page 31, which shows some cabling schemes for connecting the Standard Model 6441 to the 4271 and 4272, applies to the Model 6441 Option 002 as well.

Pin Assignments for Model 6441 - Option 002 (ECL) - Top and Bottom Output Connectors			
80	ECL High	79	ECL Low
78	ECL High	77	ECL Low
76	ECL High	75	ECL Low
74	GND	73	GND
72	ECL High	71	ECL Low
70	Ch2 - $\overline{CK}$	69	Ch2 - CK
68	Ch2 - $\overline{AS}$	67	Ch2 - AS
66	Ch2 - $\overline{SS}$	65	Ch2 - SS
64	Ch2 $\overline{D11}$ out (MSB)	63	Ch2 D11 out (MSB)
62	Ch2 $\overline{D10}$ out	61	Ch2 D10 out
60	Ch2 $\overline{D9}$ out	59	Ch2 D9 out
58	Ch2 $\overline{D8}$ out	57	Ch2 D8 out
56	Ch2 $\overline{D7}$ out	55	Ch2 D7 out
54	Ch2 $\overline{D6}$ out	53	Ch2 D6 out
52	Ch2 $\overline{D5}$ out	51	Ch2 D5 out
50	Ch2 $\overline{D4}$ out	49	Ch2 D4 out
48	Ch2 $\overline{D3}$ out	47	Ch2 D3 out
46	Ch2 $\overline{D2}$ out	45	Ch2 D2 out
44	Ch2 $\overline{D1}$ out	43	Ch2 D1 out
42	Ch2 $\overline{D0}$out (LSB)	41	Ch2 D0 out (LSB)
40	GND	39	GND
38	ECL High	37	ECL Low
36	Ch1 - $\overline{CK}$	35	Ch1 - CK
34	Ch1 - $\overline{AS}$	33	Ch1 - AS
32	Ch1 - $\overline{SS}$	31	Ch1 - SS
30	Ch1 $\overline{D11}$ out (MSB)	29	Ch1 D11 out (MSB)
28	Ch1 $\overline{D10}$ out	27	Ch1 D10 out
26	Ch1 $\overline{D9}$ out	25	Ch1 D9 out
24	Ch1 $\overline{D8}$ out	23	Ch1 D8 out
22	Ch1 $\overline{D7}$ out	21	Ch1 D7 out
20	Ch1 $\overline{D6}$ out	19	Ch1 D6 out
18	Ch1 $\overline{D5}$ out	17	Ch1 D5 out
16	Ch1 $\overline{D4}$ out	15	Ch1 D4 out
14	Ch1 $\overline{D3}$ out	13	Ch1 D3 out
12	Ch1 $\overline{D2}$ out	11	Ch1 D2 out
10	Ch1 $\overline{D1}$ out	9	Ch1 D1 out
8	Ch1 $\overline{D0}$ out (LSB)	7	Ch1 D0 out (LSB)
6	ECL High	5	ECL Low
4	ECL High	3	ECL Low
2	ECL High	1	ECL Low



The mating flat cable socket connector is 3M #82080-6006, and the strain relief is 3M #3858-080.

Two of each of these items are supplied with the Model 6441.

The recommended 0.025" pitch flat cable is 3M #3756/80

Figure 2-13: Model 6441 - Option 002 (ECL) - Front Panel Output Connectors Pin Assignments

2.3 Model 6441 Front Panel (continued)

2.3.6 FPDP - Option 008

The output devices on the Model 6441 Option 008 are 74FCT16952 transceivers.

Model 6441 Option 008 provides two non-inverted FPDP (Front Panel Data Port) connectors. Table 2-10, on page 35, gives the pin assignments for these two connectors. The front panel of Model 6441 Option 008 is shown in Figure 2-14, on the right.

The mating cable socket connector, with strain relief, is KEL part number 8825E-080-175 (Pentek part # 353.08050). Two of these items are supplied with the Model 6441 Option 008. The recommended .025" pitch flat ribbon cable is 3M part number 3756/080.

Pentek Digital Receivers equipped with FPDP input stages are the Models 4271, 6508, 6509, 6510, 6514, 6516, 6532 and 6536 all with Option 008.

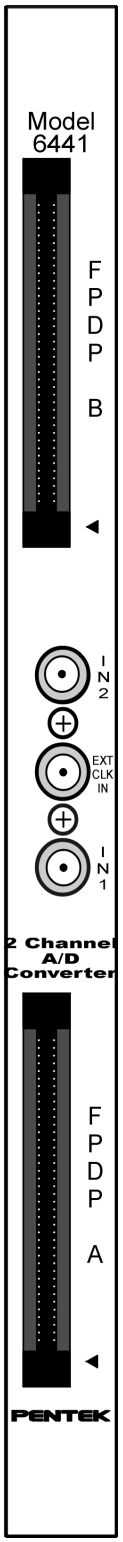


Figure 2-14: Model 6441 - Option 008 - Front Panel

2.3 Model 6441 Front Panel (continued)

2.3.6 FPDP - Option 008 (continued)

Table 2-10: FPDP Non-Inverted Output Connector Pin Assignments

Connector B				Connector A			
Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
80	GND	79	D00: N/C	80	GND	79	D00: N/C
78	D01: N/C	77	GND	78	D01: N/C	77	GND
76	D02: Ch 2 - D0 out	75	D03: N/C	76	D02: Ch 1 - D0 out	75	D03: N/C
74	GND	73	D04: N/C	74	GND	73	D04: N/C
72	D05: Ch 2 - D1 out	71	GND	72	D05: Ch 1 - D1 out	71	GND
70	D06: Ch 2 - D3 out	69	D07: Ch 2 - D2 out	70	D06: Ch 1 - D3 out	69	D07: Ch 1 - D2 out
68	GND	67	D08: Ch 2 - D4 out	68	GND	67	D08: Ch 1 - D4 out
66	D09: Ch 2 - D5 out	65	GND	66	D09: Ch 1 - D5 out	65	GND
64	D10: Ch 2 - D6 out	63	D11: Ch 2 - D7 out	64	D10: Ch 1 - D6 out	63	D11: Ch 1 - D7 out
62	GND	61	D12: Ch 2 - D8 out	62	GND	61	D12: Ch 1 - D8 out
60	D13: Ch 2 - D9 out	59	GND	60	D13: Ch 1 - D9 out	59	GND
58	D14: Ch 2 - D10 out	57	D15: Ch 2 - D11 out	58	D14: Ch 1 - D10 out	57	D15: Ch 1 - D11 out
56	GND	55	D16: N/C	56	GND	55	D16: N/C
54	D17: N/C	53	GND	54	D17: N/C	53	GND
52	D18: N/C	51	D19: N/C	52	D18: N/C	51	D19: N/C
50	GND	49	D20: Ch 1 - D0 out	50	GND	49	D20: Ch 2 - D0 out
48	D21: Ch 1 - D1 out	47	GND	48	D21: Ch 2 - D1 out	47	GND
46	D22: Ch 1 - D2 out	45	D23: Ch 1 - D3 out	46	D22: Ch 2 - D2 out	45	D23: Ch 2 - D3 out
44	GND	43	D24: Ch 1 - D4 out	44	GND	43	D24: Ch 2 - D4 out
42	D25: Ch 1 - D5 out	41	GND	42	D25: Ch 2 - D5 out	41	GND
40	D26: Ch 1 - D6 out	39	D27: Ch 1 - D7 out	40	D26: Ch 2 - D6 out	39	D27: Ch 2 - D7 out
38	GND	37	D28: Ch 1 - D8 out	38	GND	37	D28: Ch 2 - D8 out
36	D29: Ch 1 - D9 out	35	GND	36	D29: Ch 2 - D9 out	35	GND
34	D30: Ch 1 - D10 out	33	D31: Ch 1 - D11 out	34	D30: Ch 2 - D10 out	33	D31: Ch 2 - D11 out
32	GND	31	$\overline{\text{DVALID}}$	32	GND	31	$\overline{\text{DVALID}}$
30	GND	29	$\overline{\text{SYNC: N/C}}$	30	GND	29	$\overline{\text{SYNC: N/C}}$
28	GND	27	$\overline{\text{PSTROBE}}$	28	GND	27	$\overline{\text{PSTROBE}}$
26	GND	25	PSTROBE	26	GND	25	PSTROBE
24	GND	23	Reserved 1	24	GND	23	Reserved 1
22	GND	21	Reserved 2	22	GND	21	Reserved 2
20	GND	19	PIO1: N/C	20	GND	19	PIO1: N/C
18	GND	17	PIO2: N/C	18	GND	17	PIO2: N/C
16	GND	15	GND	16	GND	15	GND
14	GND	13	$\overline{\text{SUSPEND}}$	14	GND	13	$\overline{\text{SUSPEND}}$
12	GND	11	Reserved 3	12	GND	11	Reserved 3
10	GND	9	$\overline{\text{DIR}}$	10	GND	9	$\overline{\text{DIR}}$
8	GND	7	$\overline{\text{NRDY}}$	8	GND	7	$\overline{\text{NRDY}}$
6	GND	5	GND	6	GND	5	GND
4	GND	3	GND	4	GND	3	GND
2	STROB	1	GND	2	STROB	1	GND

Note:
1) All data bus signals (D31:D00) are TTL level
2) $\overline{\text{DVALID}}$ is low (i.e., true) if the $\overline{\text{SUSPEND}}$ input is HIGH and the Clock not gated off.
3) $\overline{\text{SUSPEND}}$: is a TTL level input; low is true
4) $\overline{\text{DIR}}$ is always set to TTL low, indicating that the signal levels are always outputs
5) $\overline{\text{NRDY}}$ is always set to TTL high, indicating that the unit is always ready
6) STROB is the A/D Clock at TTL level
7) PSTROBE is the A/D Clock at PECL level
8) $\overline{\text{PSTROBE}}$ is the complement of the A/D Clock at PECL level

2.3 Model 6441 Front Panel (continued)

2.3.7 Output Data Coding

2.3.7 While the Model 6441 is a 12-bit A/D converter, many of Pentek's Digital receivers have a 16-bit input stage. For this reason, the output data lines have been arranged at the data connectors such that the 12 most significant input bits of the digital receivers are driven by the outputs from the 6441. In other words, the D11 output from a Model 6441 drives the D15 input of a 16-bit digital receiver, and the 6441's D0 outputs drive the receivers' D4 inputs)

Table 2-11: Model 6441 - Output Data Coding

Input Voltage (DC, Nominal)	Binary Output Code (D11 -D0)	Hexadecimal Output Code
-1.00000 V	1000 0000 0000	0x0800
-0.99951 V	1000 0000 0001	0x0801
-0.99902 V	1000 0000 0010	0x0802
⋮	⋮	⋮
-0.00049 V	1111 1111 1110	0x0FFE
0.00000 V	1111 1111 1111	0x0FFF
+0.00049 V	0000 0000 0000	0x0000
+0.00098 V	0000 0000 0001	0x0001
⋮	⋮	⋮
+0.99902 V	0111 1111 1101	0x07FD
+0.99951 V	0111 1111 1110	0x07FE
+1.00000 V	0111 1111 1111	0x07FF

The output devices on the standard Model 6441 are 74FCT-type gates. The output data is encoded in true 2's complement format. The MSB (D11) is used as a sign bit and indicates a negative input voltage when set to the logic '1' state. All 12 bits are set to the '1' state to indicate a half scale input (i.e., 0 VDC). The 11 LSB's are decremented to indicate increasing negative input voltages with the maximum negative input voltage (– 1 VDC for the standard input signal range) resulting in an output data code of 1000 0000 0000 (0x800). An input exactly one step above half scale (≅ + 490 µVDC for the standard input signal range) produces an output code of all 12 bits cleared to the logic '0' state and a full-scale positive input voltage (+ 1 VDC for the standard input signal range) produces an output data code of 0111 1111 1111 (0x07FF). Table 2-11, above, summarizes the output data coding scheme used by the Model 6441.

2.4 Inserting the Model 6441 in the VMEbus Card Cage

Align the Model 6441 card edge with the card cage guides and push evenly on both ejector handles until the front panel seats against the upper and lower rails. Secure the unit to the cage by tightening the upper and lower retainer screws in the front panel.

2.5 Removing the Model 6441 from the VMEbus Card Cage

Loosen the upper and lower retaining screws; they are captive screws and will remain part of the panel assembly. Gently push both ejector handles apart (away from the center of the panel) until the unit unseats itself from the cage connectors. Then pull outward to remove the unit.

Never insert or remove the Model 6441 while power is applied in the card cage

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