Pentek 78661

4-Channel 200 MHz A/D Module

In Stock

Used and in Excellent Condition

Open Web Page

https://www.artisantg.com/97423-1

INSTALLATION MANUAL

MODEL 78661

4–Channel 200 MHz A/D,
With four Digital Down–Converters,
Cobalt Family PCIe Board

PENTEK

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818–5900
http://www.pentek.com

Manual Part No: 800.78661 Rev: 1.7 – November 9, 2015

Manual Revision History

Date	Revision	Comments
1/28/11	Preliminary	Initial release.
12/8/11		Sect 2.4.2, updated 71661 switch SW2 descriptions.
1/23/12	1.0	Sect 2.10.5, Sect 2.12.2 & Sect 2.12.4, added/updated Notes on input limits for PMC P14, TRIG, and SYNC/GATE connectors.
4/24/12	1.1	Sect 2.12.1, corrected external clock input voltage limit to +10 dBm.
6/8/12	1.2	Sect 2.10.6, expanded table for SERIO B connector pinouts.
7/25/13	1.3	Sect 2.4.2, corrected default setting of XMC SW2–7 – should be ON.
9/24/13	1.4	Verified & updated cross–reference links in manual.
3/24/14	1.5	Sect 2.4.2, changed XMC switch SW2–5 default to OFF, factory use only.
6/26/15	1.6	Sect 2.10.7 & Sect 2.12.4, provided Pentek Model numbers for available mating connectors.
11/9/15	1.7	Sect 2.10.7, updated GPIO connector mating cable identifier.

Warranty

Pentek warrants that all products manufactured by Pentek conform to published Pentek specifications and are free from defects in mate–rials and workmanship for a period of one year from the date of delivery when used under normal operating conditions and within the service conditions for which they were furnished. The obligation of Pentek arising from a warranty claim shall be limited to repairing or at its option, replacing without charge, any product that in Pentek's sole opinion proves to be defective within the scope of the warranty. Pentek must be notified in writing of the defect or nonconformity within the warranty period and the affected product returned to Pentek within thirty days after discovery of such defect or nonconformity. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Pentek for warranty service. Pentek shall pay for the return of products to buyer except for products returned from another country.

Pentek shall have no responsibility for any defect or damage caused by improper installation, unauthorized modification, misuse, neglect, inadequate maintenance, or accident, or for any product that has been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty described above is buyer's sole and exclusive remedy and no other warranty, whether written or oral, is expressed or implied. Pentek specifically disclaims fitness for a particular purpose. Under no circumstances shall Pentek be liable for any direct, indi–rect, special, incidental, or consequential damages, expenses, losses or delays (including loss of profits) based on contract, tort, or any other legal theory.

Copyrights

Trademarks

Pentek, Cobalt, GateFlow, and ReadyFlow are registered trademarks or trademarks of Pentek, Inc.

PCI, PCI Express, PCIe, and PCI–SIG are trademarks or registered trademarks of PCI–SIG. PLX and the PLX logo are registered trademarks of PLX Technology, Inc. Xilinx and Virtex are registered trademarks or trademarks of Xilinx, Inc.

Printed in the United States of America.

Table of Contents

Page

Chapter 1: Introduction

1.1 General Description....5
1.2 Model 78661 Features....5
1.3 Model 78661 Documentation....5
1.4 Block Diagram....6
Figure 1–1: Model 78661 Block Diagram....6
1.5 Principle of Operation....7
1.6 Specifications....8

Chapter 2: Installation and Connections

2.1 Inspection....9
Figure 2–1: Model 78661 Assembly....9
2.2 Jumper and Switch Settings....10
2.3 Removing XMC Module from PCIe Carrier....11
Figure 2–2: Removing 71661 XMC from PCIe Carrier....11
2.4 XMC Module Switches....12
Figure 2–3: Model 71661 XMC PCB Assembly Drawing, Solder Side....12
2.4.1 Switch SW1 – FPGA MGT Clock Operation....13
Table 2–1: SW1 – FPGA MGT Clock Operation....13
Table 2–2: Aux MGT Clock Frequency – Switches SW1–3:4....13
2.4.2 Switch SW2 – FPGA Configuration....14
Table 2–3: SW2 – FPGA Configuration....14
Table 2–4: FPGA Configuration Select – Switches SW2–3:4....14
2.5 XMC Module Jumpers....15
Figure 2–4: Model 71661 Main PCB Connector Side Jumpers....15
Table 2–5: Virtex–6 Program eFUSE Enable – Jumper Block J28....15
2.6 XMC Module LEDs....16
Figure 2–5: Model 71661 Main PCB, Solder Side LEDs....16
Table 2–6: PCB LED Use....16
2.7 PCIe Carrier Jumpers....17
Figure 2–6: Model 7806 PCIe Carrier PCB Connector Side – Jumpers & Switches....17
2.7.1 XMC–PCIe Serial Bus Enable....18
Table 2–7: XMC–PCIe Serial Bus Enable – Jumper Block J17....18
2.7.2 JTAG Signal Select....18
Table 2–8: JTAG Signal Select – Jumper Blocks J18, J19, J20, J21, J22....18
2.8 PCIe Carrier Switches....19
Table 2–9: XMC Modes – Switch SW1....19
2.9 PCIe Carrier LEDs....20
Figure 2–7: Model 7806 PCIe Carrier PCB Connector Side....20

Table of Contents

Page

Chapter 2: Installation and Connections *(continued)*

2.10 PCIe Carrier Connectors 21
2.10.1 Power Connector 21
2.10.2 JTAG Connector 21
Table 2–10: JTAG J4 Connector 21
2.10.3 Fan Connector 21
Figure 2–8: PCIe Carrier Block Diagram 22
2.10.4 XMC Connectors 22
2.10.5 PMC Connector (Option 104) 22
2.10.6 Gigabit Serial I/O Connectors 23
Table 2–11: Serial I/O Connector Pins 23
2.10.7 GPIO Connector (Option 104) 24
Table 2–12: GPIO Connector Pins 24
2.11 Installing the Model 78661 in a Personal Computer 25
Figure 2–9: Model 78661 Mounted in PCIe Slot 26
2.12 XMC Panel Connections 27
Figure 2–10: Model 71661 Front Panel 27
2.12.1 Clock Input Connector 27
2.12.2 Trigger Input Connector 28
2.12.3 Analog Input Connectors 28
2.12.4 Sync Bus Connector 28
Table 2–13: SYNC/GATE Connector Pins 29
2.13 XMC Panel LEDs 30
2.13.1 Link LED 30
2.13.2 User LED 30
2.13.3 Master LED 30
2.13.4 PPS LED 30
2.13.5 Over Temperature LED 30
2.13.6 Clock LED 30
2.13.7 ADC Overload LEDs 30

Chapter 1: Introduction

1.1 General Description

Pentek's Cobalt® Family Model 78661 is a multichannel, high−speed analog data converter. Using the PCI Express® half−length card format, the 78661 includes four 200−MHz, 16−bit A/D converters and four Digital Down−Converters.

The Model 78661 consists of one Pentek Model 71661 XMC module mounted on a Pentek Model 7806 XMC PCI Express carrier, assembled and tested as a single board. It is ready to plug into computer boards with PCI Express (PCIe®) bus slots.

1.2 Model 78661 Features

The Model 78661 includes the following features:

- Four 200−MHz 16−bit A/D converters
- Xilinx® Virtex®−6 FPGA, with Pentek−supplied IP Core:
  - Four−channel multiband Digital Down−Converter
  - DDC Beamformer with complex weighting and channel summation logic
  - Aurora gigabit serial interface for chaining multiple 71661 boards
- Up to 32 MB of QDRII+ SRAM or 2 GB of DDR3 SDRAM
- Clock synthesizer with programmable clock rates
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen 1 or 2) interface up to x8 wide
- LVDS connections to the Virtex−6 FPGA for custom I/O

1.3 Model 78661 Documentation

This Model 78661 Installation Manual describes the installation and connections for the 78661 PCIe assembly. Documentation of the 71661 XMC operation and programming is provided in the supplied Model 71660 Operating Manual, Pentek document #800.71660, and Model 71661 Addendum Manual, Pentek document #800.71661.

Datasheets for the programmable devices on the Model 71661 are provided in the Pentek Model 7x660 Series Supplemental Manual, part number 809.7x660. This document is available on the CD provided by Pentek, in file **`8097x660.pdf`** (PDF format).

1.4 Block Diagram

The following is a simplified block diagram of the Model 78661 A/D module.

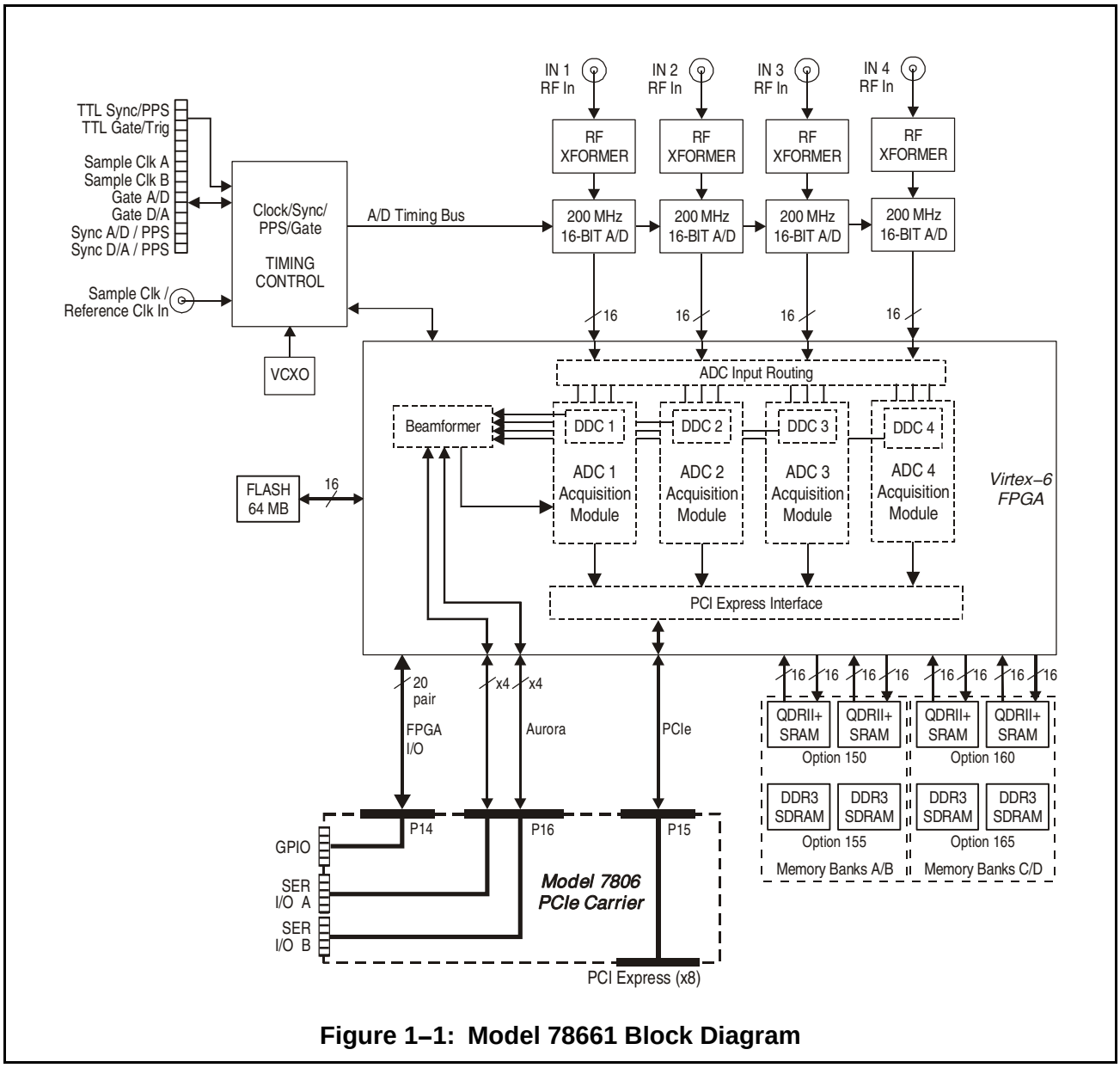


Figure 1–1: Model 78661 Block Diagram

1.5 Principle of Operation

The Model 78661 consists of one Pentek Model 71661 XMC module mounted on a Pentek Model 7806 XMC PCI Express carrier, assembled and tested as a single board. It is ready to plug into computer boards with PCI Express (PCIe®) bus slots.

The 71661 XMC is a Pentek−supplied FPGA IP Core installed in a Pentek Model 71660 XMC module. This FPGA Core includes of four multiband Digital Downconverters (DDCs) with a beamformer. Multiple 71661 modules may be linked together over an Aurora gigabit serial link to perform beamforming of up to 256 input channels.

The 71661 XMC features a Xilinx Virtex−6 FPGA for signal interfaces and processing. The FPGA is pre−configured with a four−channel digital down−converter IP core. The FPGA also provides board interfaces including PCIe and XMC. Custom I/O connections are provided to the FPGA through the optional PMC P14 connector (Option 104). Aurora gigabit serial interfaces are implemented through the XMC P16 connector.

The 71661 XMC includes four 200−MHz, 16−bit A/D converters, which provide data to the FPGA. The A/D converters provide data to the FPGA, where the data is processed by the downconverter cores.

The 71661 XMC includes up to 32 MBytes of QDRII+ SRAM, or 2 GBytes of DDR3 SDRAM. This memory is controlled by the FPGA and is organized as two or four banks, depending on the 71661 options ordered. Separate banks (separate address and data per bank) allow simultaneous access to all banks. This memory can be used as data capture, as buffer memory when transferring data between board resources or to off−board resources, or as a memory resource for custom FPGA applications.

The 71661 XMC includes an onboard VCXO and a programmable clock synthesizer for clocking, but can also accept external clocks through front panel connectors. The 71661 is equipped with an LVPECL front panel clock and sync bus that can synchronize up to four modules with built−in master/termination functions.

The 7806 Carrier provides one x8 full−duplex serial port, allowing high−speed 71661 data transfer to and from the PCIe bus using the XMC P15 connector. An XMC P16 connector provides two x4 Gigabit Serial I/O ports to support the Aurora interface. Two Serial I/O connectors (SER I/O A and B) provide access to these x4 gigabit serial paths. An optional PMC P14 connector on the carrier provides a data path to a GPIO connector (for Option 104).

1.6 Specifications

71661 XMC Signal Processing

Refer to the Model 71660 Operating Manual, Pentek document #800.71660, and to the Model 71661 Addendum Manual, Pentek document #80071661

Carrier XMC Interface

Primary XMC Interface

XMC Connector:	114−pin (XMC standard Pn5 connector), **J15**
Speed:	One x8 link supports data rates up to 4 Gbps
P15 Connectivity:	Direct interface to the PCIe bus

Secondary XMC Interface

XMC Connector:	114−pin (XMC standard Pn6 connector), **J16** VITA 42.5 Aurora Pin Assignments
Speed:	Dual x4 links support data rates up to 5 Gbps
P16 Connectivity:	One x4 link wired from **J16** rows A and B to serial I/O connector **SERI/O A** Second x4 link wired from **J16** rows D and E to serial I/O connector **SERI/O B**

Carrier PMC Interface (Option 104)

PMC Connector:	64−pin PMC standard connector, **J14**
J14 Connectivity:	Directly wired to **GPIO** connector to allow connectivity to XMC module **P14** connector for user I/O

Estimated Power Consumption

PCIe Carrier

With no XMC:	6.35 Watts typ (9.31W max)

XMC Module:	**+3.3V**	**VPWR(12V or 5V)**	**Total Power**
XC6VLX130T	2A	1.95A@12V or 4.7A@5V	30W
XC6VLX240T	2.3A	2A@12V or 4.8A@5V	32W

Physical

Dimensions, PCIe Carrier, half−length PCIe add−in card

Height:	111.15 mm (4.376 in) (including PCIe connectors)
Length:	167.65 mm (6.60 in)

Weight

PCIe Carrier:	110 grams (3.9 oz)
XMC Module:	Approximately 14 oz (400 grams), with 2−slot heatsink

Chapter 2: Installation and Connections

2.1 Inspection

After unpacking, inspect the unit carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the shipping container and packing material in case reshipment is required.

The following figure illustrates the Model 78661 assembly, with the 71661 XMC module mounted onto the PCIe carrier.

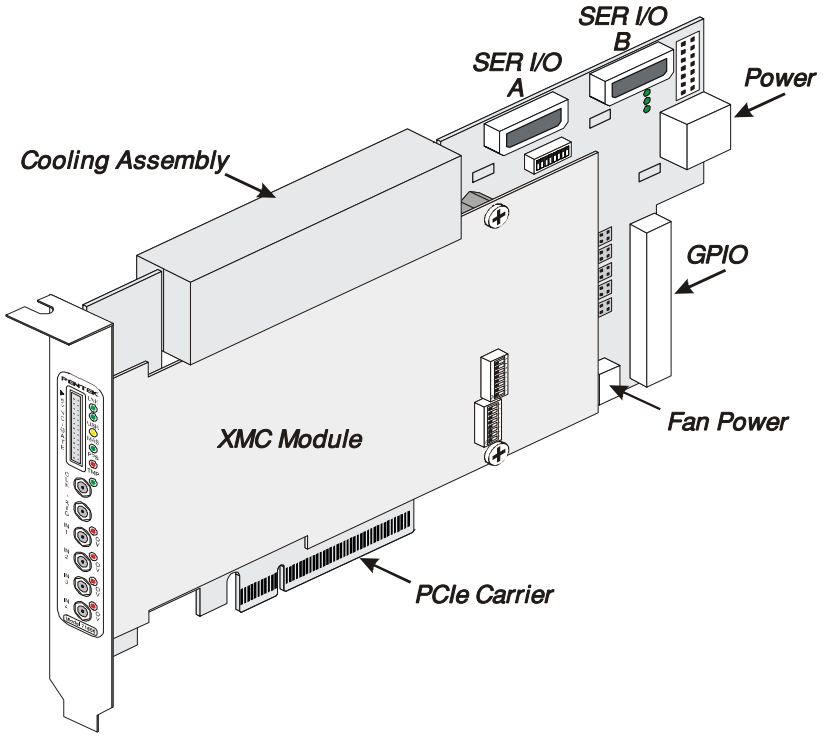


Figure 2–1: Model 78661 Assembly

Note that a cooling assembly/heat–sink may be mounted on the 78661 assembly as shipped from the factory.

2.2 Jumper and Switch Settings

The following sections describe user operating parameters that are set by shorting jumpers or DIP switches on the Model 78661.

The shorting jumpers used on the Model 78661 are for 0.020" (0.51 mm) square pins spaced on 0.079" (2.00 mm) centers. These jumpers are NorComp part number 810–002–LP1R001, or equivalent. Pentek's part number for these jumpers is 356.00015.

As shipped from the factory, all jumpers and DIP switches are installed in default positions on your board. The default operating parameters selected may or may not meet your requirements. Before installing your Model 78661, please review the following sections to determine whether you need to change any of these settings.

The Model 78661 includes one Pentek 71661 XMC module mounted on a Pentek Model 7806 XMC to PCI Express (PCIe) carrier as illustrated in Figure 2–1 on the prior page. As shipped, the 71661 XMC module is mounted onto the PCIe carrier.

- Refer to Section 2.4 for the switch settings and Section 2.5 for the jumper settings on the 71661 PCB. All switch blocks are accessible in this shipped configuration. If you need to access the jumpers on the XMC, you must first remove the XMC module from the PCIe carrier, as described in Section 2.3.

- Refer to Section 2.7 for the jumper settings and Section 2.8 for the switch settings on the carrier PCB. All switch blocks are accessible in the shipped configuration. If you need to access certain jumpers on the PCIe carrier, you must first remove the XMC module from the PCIe carrier, as described in Section 2.3.

Do not change jumpers or switches that are not described in this chapter—those are reserved for factory test and setup purposes only.

2.3 Removing XMC Module from PCIe Carrier

CAUTION

Perform all steps at a static–controlled work workstation.

1) From the solder side of the Model 78661 assembly (side opposite the 71661 XMC), unscrew the four pan–head Phillips mounting screws, as identified below.

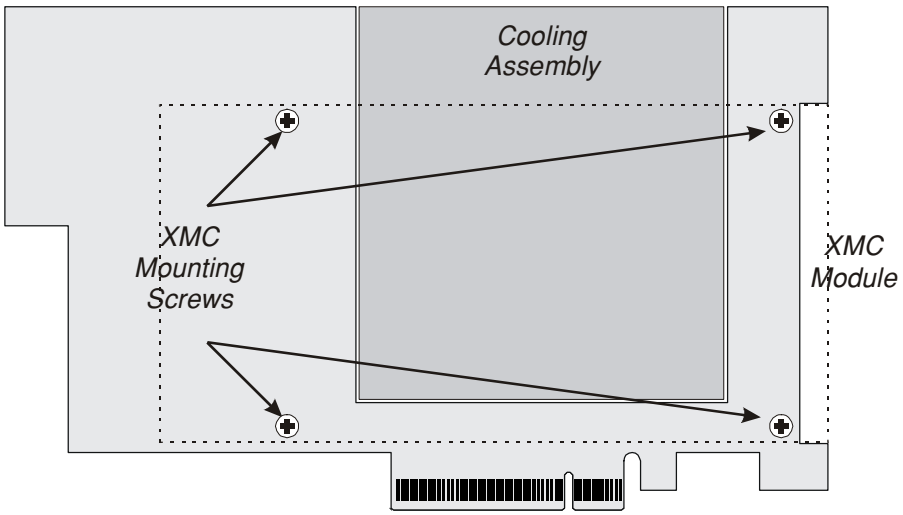


Figure 2–2: Removing 71661 XMC from PCIe Carrier

2) From the XMC module side, **GENTLY**, pull on the XMC card to disengage the card's connectors from the PCIe carrier's XMC connectors.

After jumper or switch changes, replace the XMC onto the PCIe carrier as follows.

1) Position the 71661 XMC module's front panel into the PCIe carrier's panel opening from behind the PCIe carrier slot panel, and align the XMC module so that the connectors on the XMC card are aligned over the connectors on the PCIe carrier.

2) **GENTLY but firmly**, press down on the areas of the XMC opposite the connectors to fully seat the card's connectors into the carrier. The connectors on the XMC should connect smoothly with the corresponding connectors on the carrier.

3) From the solder side of the PCIe carrier, secure the XMC to the carrier by screwing the four pan–head Phillips mounting screws (those removed above) through the PCIe carrier into the XMC module.

2.4 XMC Module Switches

The following sections describe user operating parameters that are set by two DIP switches, identified as **SW1** and **SW2**, on the Model 71661 main PCB (Pentek part number 320–71600).

As shipped from the factory, all switches are set for the configuration shipped. The operating parameters they select may or may not meet your requirements. Before installing your 78661 assembly onto a PCIe baseboard, please review the following subsections to determine whether you need to change any of these settings.

Both switch blocks are located on the solder side of the Model 71661 PCB and are accessible while the 71661 is mounted onto the PCIe carrier. An assembly drawing of the solder side of the main PCB is provided below, showing the location of switches **SW1** and **SW2** on the PCB.

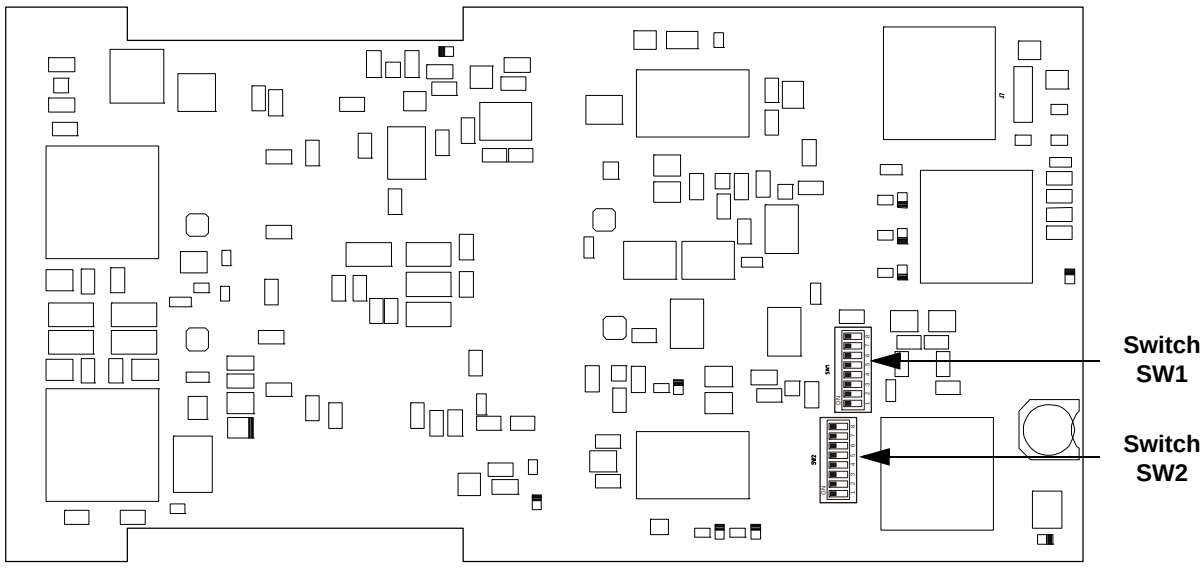


Figure 2–3: Model 71661 XMC PCB Assembly Drawing, Solder Side

Note that several user LEDs are located on the solder side of the 71661 main PCB. Refer to Section 2.6, on page 16 for description of these LEDs.

2.4 XMC Module Switches (continued)

2.4.1 Switch SW1 – FPGA MGT Clock Operation

Switch **SW1** provides user control over the FPGA MGT clocks used for the XMC interface. The following table shows the settings for this switch.

CAUTION

Use ballpoint tip only for setting DIP switches.

DO NOT USE paper clips, tweezers, or any other sharp objects, as they may damage the switch.

Table 2–1: SW1 – FPGA MGT Clock Operation

Switch	Function	ON	OFF
SW1–1	Primary PCIe Clock Frequency **	100 MHz	250 MHz *
SW1–2	Secondary PCIe Clock Frequency	100 MHz	250 MHz *
SW1–3	Auxiliary MGT Clocks (A/B/C) Frequency	See Table 2–2 below	
SW1–4			
SW1–5	Secondary PCIe Clock Disable	Disabled *	Enabled
SW1–6	Auxiliary MGT Clocks (A/B/C) Disable	Disabled	Enabled *
SW1–7	Primary PCIe Clock Source	XMC CLK0 *	250 MHz Crystal
SW1–8	Secondary PCIe Clock Source ***	XMC CLK1 *	AUX_MGT_CLK_A

* Factory Default Settings

** Switch **SW1–1** must be in the **OFF** (250 MHz) position for Pentek factory FPGA code and for any x8 or Gen 2 design.

*** Switch **SW1–8**, when in the **ON** position clock source is the XMC P16 connector.

Table 2–2: Aux MGT Clock Frequency – Switches SW1–3:4

SW1–3	SW1–4	Aux MGT Clk A/B	Aux MGT Clk C
OFF	OFF	312.5 MHZ	125 MHz
ON	OFF	156.25 MHz	125 MHz
OFF	ON	125 MHz	156.25 MHz
ON *	ON *	156.25 MHz	156.25 MHz

* Factory Default Setting

2.4 XMC Module Switches (continued)

2.4.2 Switch SW2 – FPGA Configuration

Switch **SW2** controls access to the FPGA configuration functions. The following table shows the settings for this switch.

CAUTION

Use ballpoint tip only for setting DIP switches.

DO NOT USE paper clips, tweezers, or any other sharp objects, as they may damage the switch.

Table 2–3: SW2 – FPGA Configuration

Switch	Function	ON	OFF
SW2–1	FLASH Memory Write Protect/Write Enable	Write Protected *	Write Enabled
SW2–2	Factory use only – should always be set to **ON**		
SW2–3	Select Boot Configuration at power on	See Table 2–4 below	
SW2–4			
SW2–5	Factory use only – should always be set to **OFF**		
SW2–6	no function	–	–
SW2–7	XMC JTAG Enable	XMC JTAG *	Board JTAG
SW2–8	Select whether JTAG chain includes Memory	FPGA & Memory	FPGA Only
	Note: When QDRII+ memory is installed, **SW2–8** should be set to **ON**, FPGA & Memory, or JTAG activity may interfere with QDRII+ SRAM operation.		
* Factory Default Settings			

Table 2–4: FPGA Configuration Select – Switches SW2–3:4

SW1–3	SW1–4	Configuration Select (FLASH)
ON *	ON *	Version 0 Boot Code – Gen 1 x8 PCIe
OFF	ON	Version 1 Boot Code – Gen 2 x4 PCIe
ON	OFF	Version 2 Boot Code
OFF	OFF	Version 3 Boot Code
* Factory Default Setting Refer to the 71660 Operating Manual, #800.71660, for FLASH Memory use.		

2.5 XMC Module Jumpers

The following describes user operating parameters that are set by jumper block **J28** on the Model 71661 PCB. This jumper block is located on the connector side of the Model 71661 main PCB (Pentek part number 320–71600). An assembly drawing of the connector side of the PCB is provided below, showing the location of jumper block **J28**.

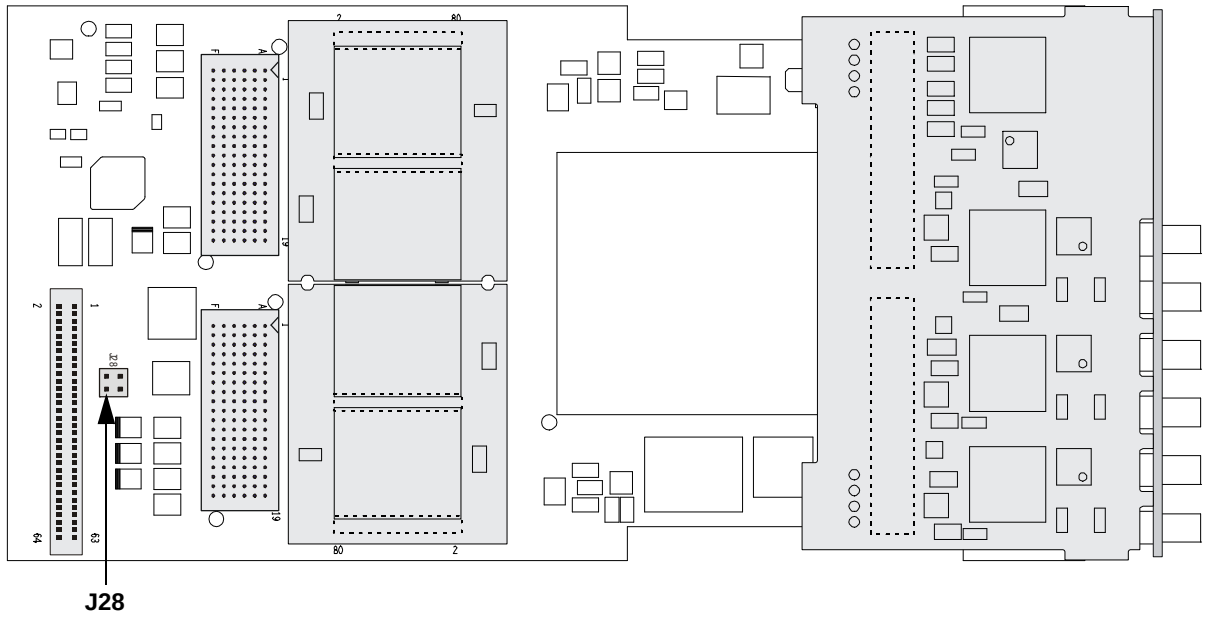


Figure 2–4: Model 71661 Main PCB Connector Side Jumpers

NOTE: To access **J28**, you must remove the XMC module from the PCIe carrier, as described in Section 2.3.

Table 2–5: Virtex–6 Program eFUSE Enable – Jumper Block J28

Jumper Pins	Function	Installed	Removed
Pins 1 – 3	Virtex–6 Program eFUSE	Enabled	Disabled *
Pins 2 – 4	no function	–	–
* Factory Default Setting			

Jumper **J28**, pins 1–3, are used to program eFUSE in the Virtex–6 FPGA. Refer to the Xilinx Virtex–6 FPGA Configuration Guide (Xilinx document UG360) for further information about using this capability.

2.6 XMC Module LEDs

The following describes the Model 71661 PCB LEDs, labeled **Dnn**, that provide general operating status of the board. These LEDs are positioned on the solder side of the PCB, as illustrated below, and are visible through the heat–sink mounted on the PCB. The use of each LED is indicted in Table 2–6 below.

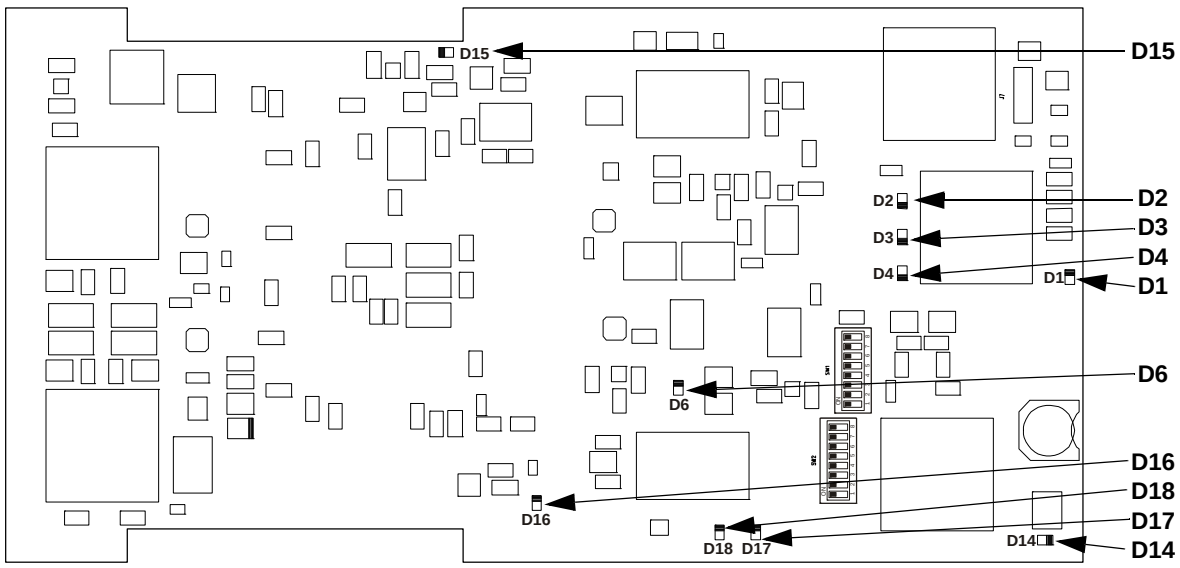


Figure 2–5: Model 71661 Main PCB, Solder Side LEDs

Table 2–6: PCB LED Use

LED	USE
D1	Yellow LED indicates PCI Express Gen 2 operation
D2 & D3	Yellow LEDs indicate PCI Express Active Lanes:
D4	Green LED indicates PCI Express link has been established
D6	Green LED for user applications
D14	Red LED indicates temperature fault from the main PCB LM83
D15	Red LED indicates temp/volt fault from the System Monitor
D16	Green LED indicates FPGA configuration done
D17	Red LED indicates FPGA configuration initiated
D18	Yellow LED indicates FPGA configuration active

	x1	x2	x4	x8
D2	Off	On	Off	On
D3	Off	Off	On	On

2.7 PCIe Carrier Jumpers

The following subsections describe user operating parameters that are set by shorting jumpers on the Model 7806 PCIe carrier PCB. Refer to Section 2.8 for the DIP switch settings on the carrier PCB.

As shipped from the factory, all jumpers on the carrier have been factory set for the configuration shipped. The operating parameters they select may or may not meet your requirements. Before installing your 78661 assembly onto a PCIe baseboard, review the following subsections to determine whether you need to change any of these settings.

The user should not change jumpers that are not described in these pages—these are reserved for factory test and setup purposes only.

The following shows the location of all jumpers and switches on the 7806 carrier PCB.

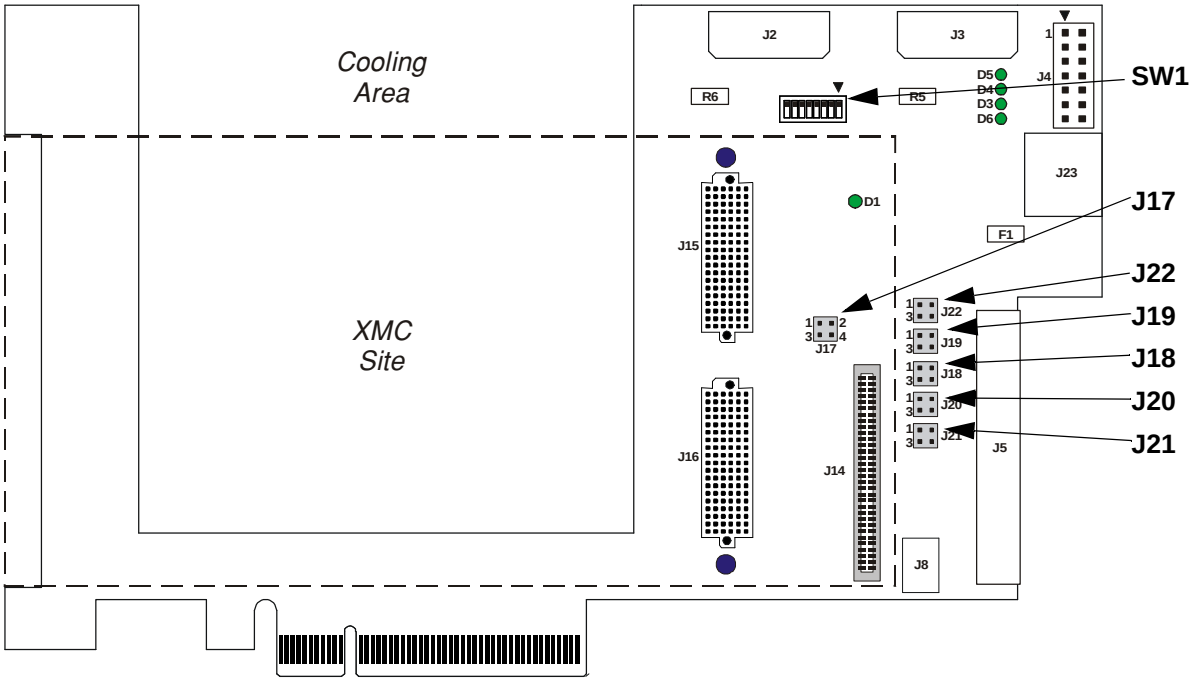


Figure 2–6: Model 7806 PCIe Carrier PCB Connector Side – Jumpers & Switches

2.7 PCIe Carrier Jumpers (continued)

2.7.1 XMC–PCIe Serial Bus Enable

Jumper block **J17** enables or disables the PCI Express SM bus (**SMDAT**/**SMCLK**) to the XMC site I^2C serial bus (**MSDA**/**MSCL**). The following table shows the jumper settings.

NOTE: To access **J17**, you must remove the XMC module from the PCIe carrier, as described in Section 2.3.

Table 2–7: XMC–PCIe Serial Bus Enable – Jumper Block J17

Jumper Pins	Function	Installed	Removed
Pins 1 – 3	PCIe SMDAT to XMC MSDA	Enabled	Disabled *
Pins 2 – 4	PCIe SMCLK to XMC MSCL	Enabled	Disabled *
* Factory Default Setting			

2.7.2 JTAG Signal Select

Jumper blocks **J18, J19, j20, j21**, and **J22** select the signal source for JTAG operation, from either the onboard **J4** JTAG connector (Section 2.10.2) or the XMC connector. The following table shows the jumper settings.

Table 2–8: JTAG Signal Select – Jumper Blocks J18, J19, J20, J21, J22

Jumper Block	JTAG Signal	Jumper Pins	Signal Source
J18	TMS (Test Mode Select)	Pins 1 – 3 *	Use JTAG J4 Connector TMS
		Pins 2 – 4	Use XMC interface XMC_TMS
J19	TCK (Test Clock)	Pins 1 – 3 *	Use JTAG J4 Connector TCK
		Pins 2 – 4	Use XMC interface XMC_TCK
J20	TDI (Test Data In)	Pins 1 – 3 *	Use JTAG J4 Connector TDI
		Pins 2 – 4	Use XMC interface XMC_TDI
J21	TDO (Test Data Out)	Pins 1 – 3 *	Use JTAG J4 Connector TDO
		Pins 2 – 4	Use XMC interface XMC_TDO
J22	TRST (Test Reset)	Pins 1 – 3	Use JTAG J4 Connector TRST_N
		Pins 2 – 4 *	Use XMC interface XMC_TRST_N
* Factory Default Setting – For proper JTAG operation, all jumpers should be set to 1–3 except J22, which should be set to 2–4.			

2.8 PCIe Carrier Switches

This section describes operating parameters that are set by DIP switches on the Model 7806 carrier PCB. See Figure 2–6 on page 17 for location of these switches on the PCB. Refer to Section 2.7 for the jumper settings on the carrier PCB.

As shipped from the factory, all switches on the carrier PCB have been factory set for the configuration shipped. The default parameters they select may or may not meet your requirements. Before installing your 78661 assembly onto a PCIe baseboard, review the following table to determine whether you need to change any of these set–tings.

Switch **SW1** selects XMC interface modes for the XMC module. The following table describes the different mode selections for each switch position.

Table 2–9: XMC Modes – Switch SW1

Switch	OFF Function	ON Function	Description
SW1–1	GA0 is pulled to 3.3V on the XMC connector *	Ties GA0 to GND on the XMC connector	Sets bit 0 of the XMC onboard EEPROM base address
SW1–2	GA1 is pulled to 3.3V on the XMC connector *	Ties GA1 to GND on the XMC connector	Sets bit 1 of the XMC onboard EEPROM base address
SW1–3	GA2 is pulled to 3.3V on the XMC connector *	Ties GA2 to GND on the XMC connector	Sets bit 2 of the XMC onboard EEPROM base address
SW1–4	MVMRO is pulled to 3.3V on the XMC connector *	Ties MVMRO on the XMC connector to GND	When MVMRO is pulled high to 3.3V, the XMC onboard EEPROM cannot be written to.
SW1–5	ROOT0 is pulled to 3.3V on the XMC connector *	Ties ROOT0 on the XMC connector to GND	When ROOT0 is pulled to GND, the XMC card can function as a root complex and assign base addresses to other devices on the PCI express and PCI buses
SW1–6	SHUTDOWN_12V_N is pulled to 3.3V *	Ties SHUTDOWN_12V_N to GND	When SHUTDOWN_12V_N is pulled to GND, the –12V XMC power supply is shut down
SW1–7	Not used		
SW1–8	Not used		
* Factory Default Setting – all Switches OFF			

2.9 PCIe Carrier LEDs

This section describes the LEDs, labeled **Dnn** on the Model 7806 carrier PCB, that provide power operating status for the board.

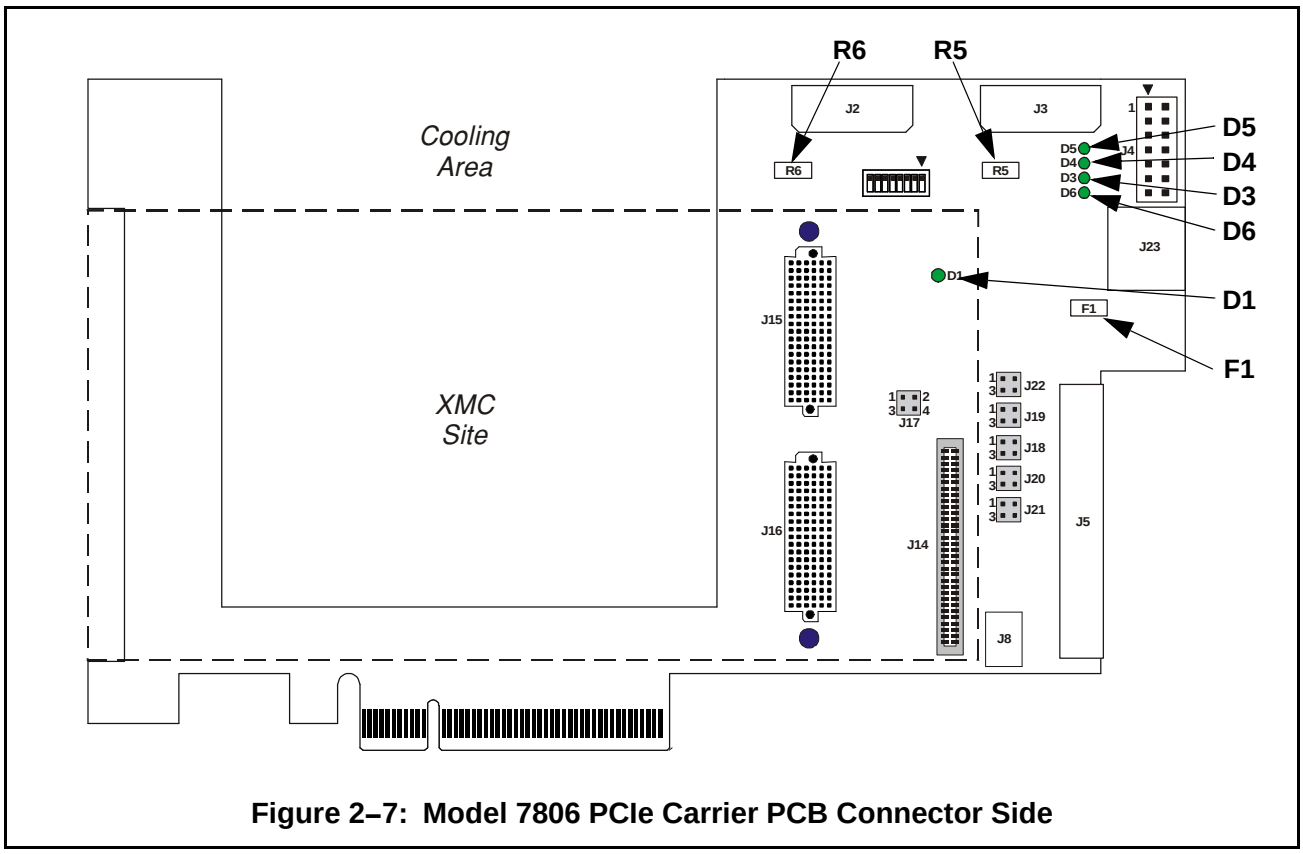


Figure 2–7: Model 7806 PCIe Carrier PCB Connector Side

The following green LEDs indicate power applied to board resources.

LED	USE
D1	Green LED indicates the presence of –12V XMC Power Supply
D3	Green LED indicates the presence of +12V at the 6–pin PCIe Power Connector (J23)
D4	Green LED indicates the presence of +3.3V from the PCIe bus (motherboard)
D5	Green LED indicates the presence of +3.3V from the onboard Power Supply
D6	Green LED indicates the presence of +12V after the Fuse **F1** *
* If **D3** is illuminated and **D6** is not, this indicates the fuse **F1** is blown.	

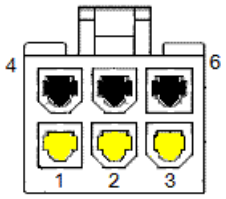
Note that you can measure the voltage across resistor **R6** (0.012 ohms) to determine the current draw for the +12 Volt supply, and the voltage across resistor **R5** (0.012 ohms) to determine the current draw for the +3.3 Volt supply. These resistors are identified in Figure 2–7 above.

2.10 PCIe Carrier Connectors

The following subsections describe the power and signal connectors on the PCIe carrier. Refer to Figure 2–7 on the prior page for location of the connectors on the PCB.

2.10.1 Power Connector

The PCIe carrier uses a 6–pin power connector, labeled **J23**, to supply +12V power to the XMC module. This is a standard PCI Express power connector used in PCs with a PCI Express bus.



Pins 1, 2, and 3 are +12 VDC
Pins 4, 5, and 6 are ground

NOTE: You **must** provide a power source to this connector or the XMC module will not operate.

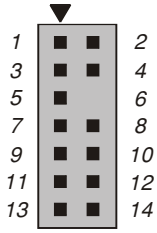
Pentek includes a PCIe to Molex adapter cable (part # 002.21790) with the Model 78661 shipment.

2.10.2 JTAG Connector

The JTAG **J4** connector provides a connection to download programs and to perform boundary–scan tests on PCIe carrier devices. This connector is reserved for Pentek factory use only. The pinout for this 14–pin header is given in the following table.

Table 2–10: JTAG J4 Connector

Signal	Pin Number		Pin Number	Signal
Gnd	1		2	+3.3 V
Gnd	3		4	TMS
Gnd	5		6	TCK
Gnd	7		8	TDO
Gnd	9		10	TDI
Gnd	11		12	TRST_N
Gnd	13		14	No Connection



2.10.3 Fan Connector

Connector **J8** on the PCIe carrier PCB provides a +12VDC power source for use by the cooling fan.

2.10 PCIe Carrier Connectors (continued)

The following is a simplified block diagram of the PCIe carrier, showing the signal paths of the PMC, XMC, GPIO, and SERIO connectors. These connectors are described in the following subsections.

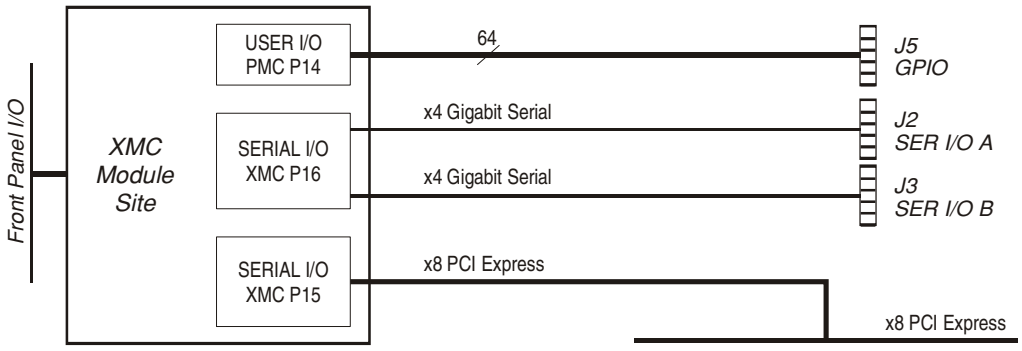


Figure 2–8: PCIe Carrier Block Diagram

2.10.4 XMC Connectors

The XMC site on the 7806 carrier provides two XMC connectors, designated **J15** and **J16**, that follow the VITA 42.0 XMC Switched Mezzanine Card Auxiliary Standard and VITA 42.3 XMC PCI Express Protocol Standard.

- **J15** provides an x8 PCI Express link between the XMC module and the 7806 PCIe bus.
- **J16** provides two x4 data links, up to 5 GHz, to two connectors (**SER I/O A & B**), for Aurora Gigabit Serial I/O. See Table 2–11 in Section 2.10.6 for the pin mapping for the **J16** to **SER I/O n** connections.

2.10.5 PMC Connector (Option 104)

Option 104 for the Model 71661 XMC module provides connections from 71661 FPGA LVDS I/O pins to the PCIe carrier using PMC connector **J14** on the 7806 PCB (see Model 71660 Operating Manual).

These signals are brought out to a 68–pin general–purpose connector on the 7806, identified as **GPIO** on the PCB. See Table 2–12 in Section 2.10.7 for the pin mapping of the PMC **P14** to **GPIO** connections.

NOTE: The **P14** signals can be configured in the FPGA as LVDS or LVTTL but are limited to 2.5V and cannot be driven with a negative voltage.

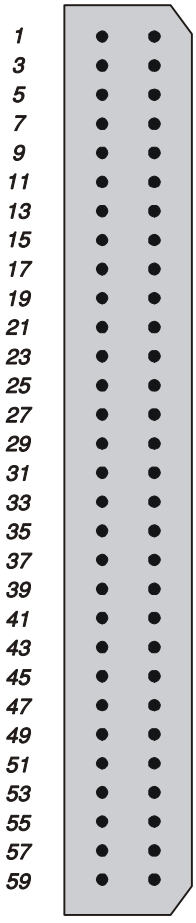
2.10 PCIe Carrier Connectors (continued)

2.10.6 Gigabit Serial I/O Connectors

Two 60–pin connectors, labeled **J2** and **J3** on the carrier PCB, provide giga–bit Aurora I/O from the XMC **P16** connector, described in Section 2.10.4. **J2** is for **SER I/O A**, and **J3** is for **SER I/O B**. The mating connector is Pen–tek part # 353.06001 (Samtec P/N QSH–030–01–L–D–A). The following table shows the pinouts of each connector.

Table 2–11: Serial I/O Connector Pins

SER A Signal	SER B Signal	Pin		Pin	SER B Signal	SER A Signal
N/C	N/C	1		2	TX_DP_4+	TX_DP_0+
N/C	N/C	3		4	TX_DP_4–	TX_DP_0–
GND	GND	5		6	GND	GND
RX_DP_0+	RX_DP_4+	7		8	N/C	N/C
RX_DP_0–	RX_DP_4–	9		10	N/C	N/C
GND	GND	11		12	GND	GND
N/C	N/C	13		14	TX_DP_5+	TX_DP_1+
N/C	N/C	15		16	TX_DP_5–	TX_DP_1–
GND	GND	17		18	GND	GND
RX_DP_1+	RX_DP_5+	19		20	N/C	N/C
RX_DP_1–	RX_DP_5–	21		22	N/C	N/C
GND	GND	23		24	GND	GND
N/C	N/C	25		26	N/C	N/C
N/C	N/C	27		28	N/C	N/C
GND	GND	29		30	GND	GND
N/C	N/C	31		32	TX_DP_6+	TX_DP_2+
N/C	N/C	33		34	TX_DP_6–	TX_DP_2–
GND	GND	35		36	GND	GND
RX_DP_2+	RX_DP_6+	37		38	N/C	N/C
RX_DP_2–	RX_DP_6–	39		40	N/C	N/C
GND	GND	41		42	GND	GND
N/C	N/C	43		44	TX_DP_7+	TX_DP_3+
N/C	N/C	45		46	TX_DP_7–	TX_DP_3–
GND	GND	47		48	GND	GND
RX_DP_3+	RX_DP_7+	49		50	N/C	N/C
RX_DP_3–	RX_DP_7–	51		52	N/C	N/C
GND	GND	53		54	GND	GND
N/C	N/C	55		56	N/C	N/C
N/C	N/C	57		58	N/C	N/C
GND	GND	59		60	GND	GND



RX_DP_[0:7] – Serial I/O Receive data from XMC P16 connector
TX_DP_[0:7] – Serial I/O Transmit data from XMC P16 connector

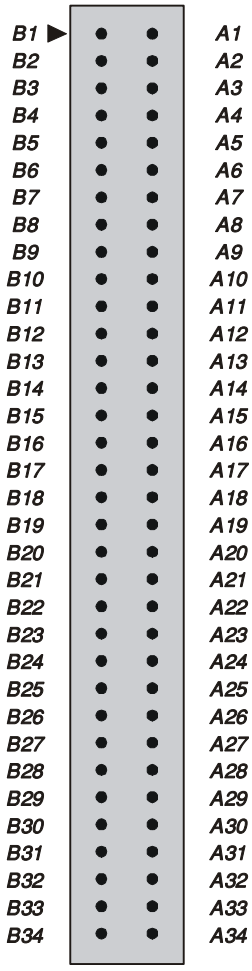
2.10 PCIe Carrier Connectors (continued)

2.10.7 GPIO Connector (Option 104)

A 68−pin connector on the back edge of the 7806 PCB, labeled **J5** on the PCB, provides I/O from the PMC **P14** connector, described in Section 2.10.5. Cables of various lengths with the mating connector are available: Pentek Model 2147. The mating connector alone is Model 2147−999. The following table identifies the 71661 FPGA LVDS signals on this connector.

Table 2−12: GPIO Connector Pins

PMC P14 Signal	Pin		Pin	PMC P14 Signal
GND	B1		A1	GND
P4_LVDS_OUT_N0	B2		A2	P4_LVDS_OUT_P0
P4_LVDS_IN_N0	B3		A3	P4_LVDS_IN_P0
P4_LVDS_OUT_N1	B4		A4	P4_LVDS_OUT_P1
P4_LVDS_IN_N1	B5		A5	P4_LVDS_IN_P1
P4_LVDS_OUT_N2	B6		A6	P4_LVDS_OUT_P2
P4_LVDS_IN_N2	B7		A7	P4_LVDS_IN_P2
P4_LVDS_OUT_N3	B8		A8	P4_LVDS_OUT_P3
P4_LVDS_IN_N3	B9		A9	P4_LVDS_IN_P3
P4_LVDS_OUT_N4	B10		A10	P4_LVDS_OUT_P4
P4_LVDS_IN_N4	B11		A11	P4_LVDS_IN_P4
P4_LVDS_OUT_N5	B12		A12	P4_LVDS_OUT_P5
P4_LVDS_IN_N5	B13		A13	P4_LVDS_IN_P5
P4_LVDS_OUT_N6	B14		A14	P4_LVDS_OUT_P6
P4_LVDS_IN_N6	B15		A15	P4_LVDS_IN_P6
P4_LVDS_OUT_N7	B16		A16	P4_LVDS_OUT_P7
P4_LVDS_IN_N7	B17		A17	P4_LVDS_IN_P7
P4_LVDS_OUT_N8	B18		A18	P4_LVDS_OUT_P8
P4_LVDS_IN_N8	B19		A19	P4_LVDS_IN_P8
P4_LVDS_OUT_CLK_N11	B20		A20	P4_LVDS_OUT_CLK_P11
P4_LVDS_IN_CLK_N11	B21		A21	P4_LVDS_IN_CLK_P11
No connect	B22		A22	No connect
	B23		A23	
	B24		A24	
	B25		A25	
	B26		A26	
	B27		A27	
	B28		A28	
	B29		A29	
	B30		A30	
	B31		A31	
	B32		A32	
	B33		A33	
GND	B34		A34	GND



2.11 Installing the Model 78661 in a Personal Computer

The Model 78661 is designed to operate in personal computers with PCI Express card slots. This assembly conforms to the standard height, half−length PCI Express Add−In Card format as per PCI Express Electromechanical Specification, Rev. 2.0.

CAUTION

REMOVE POWER to the personal computer before installation!

1) Orient the personal computer on your static−controlled work surface such that the rear panel faces you.

2) Remove the cover from the computer, to gain access to the PC's motherboard and its local bus connectors.

3) PCIe Bus connectors are usually black in color (as opposed to PCI bus connectors which are usually white, and VESA connectors which are usually brown), and are about 3½" long. Select a vacant x8 PCI express slot in which to install the Model 78661 assembly, and remove the blank expansion slot cover plate on the computer's rear panel located immediately to the RIGHT of the selected connector.

NOTE: The Model 78661 can also be installed in an x16 PCI Express slot, but will use only the x8 connections of that slot.

4) Before touching the Model 78661 assembly, touch the case of your computer's power supply, to discharge any static electrical charge that may have accumulated on you. Then, remove the 78661 assembly from its anti−static packaging.

5) Install the PCIe carrier PCB's connecting edge into the selected PCIe expansion socket, as illustrated in Figure 2−9 on the next page.

NOTE: Be certain that the card edge is properly aligned with the PCIe connector. Gentle downward pressure should be sufficient to fully seat the card edge in the connector.

DO NOT ATTEMPT TO FORCE THE CARD INTO THE SLOT!
If excessive force is necessary, then the card is probably misaligned. Damage to either the PC motherboard or the PCIe carrier board will be the most likely result of attempts at forced installations.

(Continued on next page)

2.11 Installing the Model 78661 in a Personal Computer (continued)

6) The PCIe carrier has a 6−pin power connector to supply the majority of power to the components (as illustrated in Section 2.10.1). This is a standard PCI Express power connector used in PCs with a PCI Express bus. Plug a spare power connector from your PC's power supply into this connector.

7) Secure the board to the PC chassis using a screw at the top of the PC slot panel.

8) The PC cover may now be replaced and power may be reconnected.

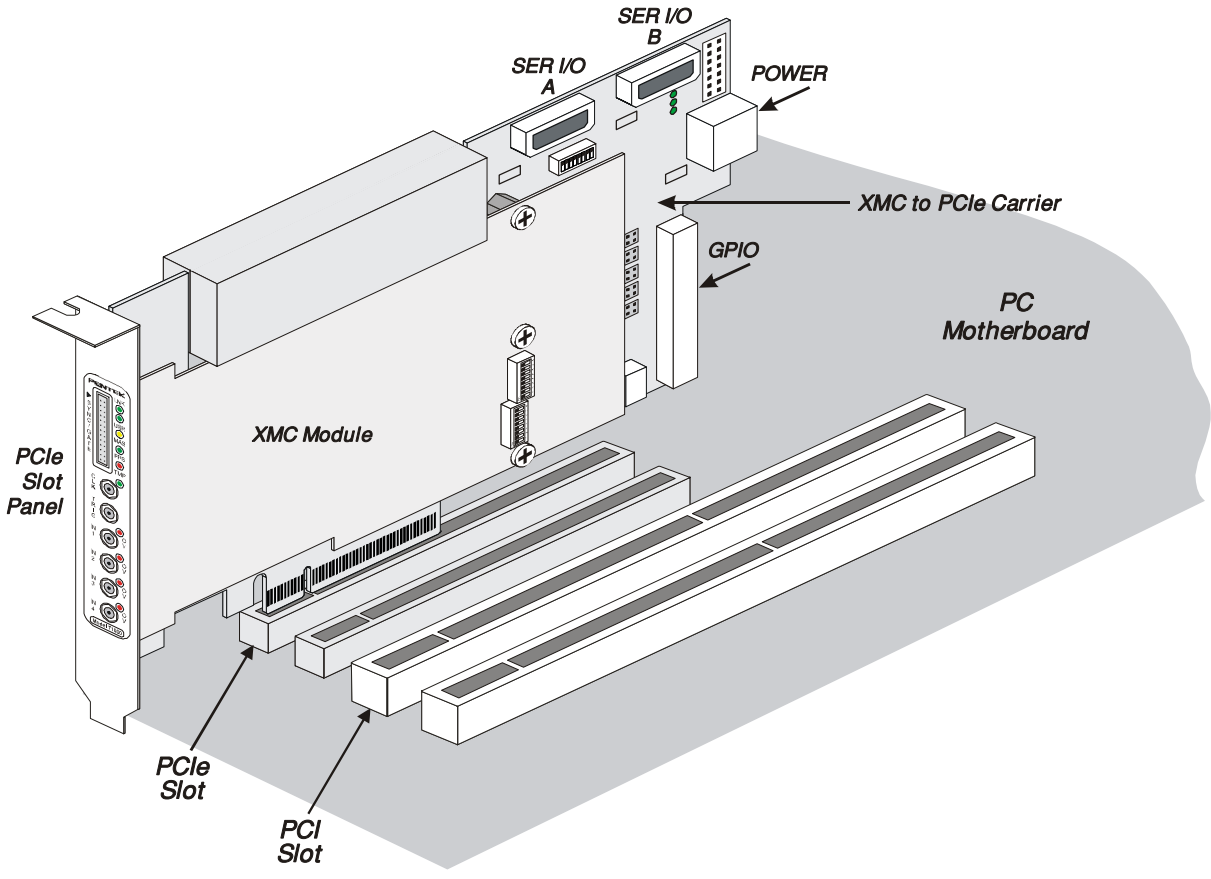


Figure 2–9: Model 78661 Mounted in PCIe Slot

This completes the installation procedure.

2.12 XMC Panel Connections

The 71661 XMC front panel, illustrated at the right, fits into the slot opening on the PCIe carrier. See Figure 2–1 on page 9 for location of the panel on the Model 78661 assembly.

The front panel includes six SSMC coaxial connectors for input/output of clock and analog signals, and a 26–pin Sync Bus input/output connector. These connectors are described in the following subsections.

The front panel also includes ten LED indicators. These are described in Section 2.13, on page 30.

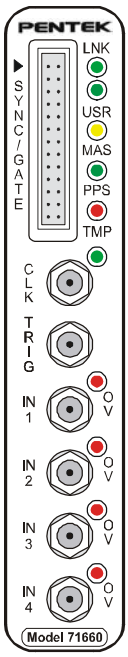


Figure 2–10: Model 71661 Front Panel

2.12.1 Clock Input Connector CLK

The front panel has one SSMC coaxial connector, labeled **CLK**, for input of an external sample clock. The external clock signal must be a sine wave or square wave of +0 dBm to +10 dBm, with a frequency range from 10 to 500 MHz.

The external clock input can be used as the sample clock for the A/D converters. This input is enabled using Sync Bus Control Register 1 (see Model 71660 Operating Manual). The clock source selected by these bits is input to a CDC7005 Clock Synthesizer that generates separate output clocks, each programmable as sub–multiples of the input frequency. One of the CDC7005 output clocks (Y0) provides ADC timing.

CAUTION

Take care that the ADC clock never exceeds the ADS5485 rated clock speed during any change of frequency with the input clock signal.

– If you are increasing the external input frequency, first reprogram the appropriate CDC7005 divider so that the ADS5485 clock does not exceed 200 MHz.

– If you are decreasing the input frequency, do not reprogram the CDC7005 divider until the input has been reprogrammed so that the ADS5485 clock does not exceed 200 MHz.

2.12 XMC Panel Connections (continued)

2.12.2 Trigger Input Connector **TRIG**

The front panel has one SSMC coaxial connector, labeled **TRIG**, for input of an external trigger. The external trigger signal must be an LVTTL signal.

The front panel TRIG input is 5V tolerant but it must NOT have any negative voltage applied. It is terminated with a 392–Ohm resistor to 3.3V and a 392–Ohm resistor to ground.

The trigger input can be used as a gate or trigger for A/D signal processing. This input is enabled using Sync Bus Control Register 2 TTL SRC bits (see Model 71660 Operating Manual).

2.12.3 Analog Input Connectors **IN 1, IN 2, IN 3, IN 4**

The front panel has four SSMC coaxial connectors for analog signal inputs, labeled **IN 1, 2**, **3**, and **4**, one for each ADC input channel.

The analog input signal has a full–scale level of +8 dBm. Each input drives an RF transformer, with 50Ω input impedance.

2.12 XMC Panel Connections (continued)

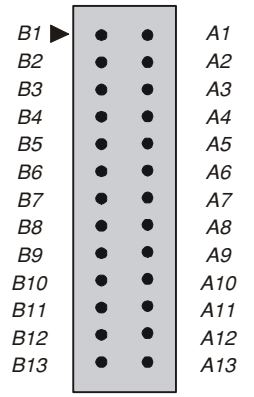
2.12.4 Sync Bus Connector SYNC/GATE

The 26−pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Low−Voltage Positive Emitter−Coupled Logic (LVPECL) Sync Bus. When the Model 71661 is a bus Master, these pins output LVPECL Sync Bus signals to other slave units. When the 71661 is a bus Slave, these pins input LVPECL signals from a bus Master. This connector also accepts two Low−Voltage TTL (LVTTL) Gate/Sync inputs.

The following table shows the **SYNC/GATE** connector pin configuration. The available mating 26−pin connector is Pentek Model 2140−998.

Table 2−13: SYNC/GATE Connector Pins

Signal	Pin		Pin	Signal
LVTTL GATE/TRIG	B1		A1	GND
LVTTL SYNC/PPS	B2		A2	GND
LVPECL GATE A−	B3		A3	LVPECL GATE A+
GND	B4		A4	GND
LVPECL SYNC A−	B5		A5	LVPECL SYNC A+
GND	B6		A6	GND
LVPECL CLK A−	B7		A7	LVPECL CLK A+
GND	B8		A8	GND
LVPECL GATE B−	B9		A9	LVPECL GATE B+
GND	B10		A10	GND
LVPECL SYNC B−	B11		A11	LVPECL SYNC B+
GND	B12		A12	GND
LVPECL CLK B−	B13		A13	LVPECL CLK B+



When connecting LVPECL Sync Bus pins to additional Model 71661 modules, the LVPECL pins on the LAST unit must be terminated. Pentek includes a terminating board, part #004.71504, with your shipment for this purpose.

The LVTTL GATE/TRIG and SYNC/PPS signals are 5V tolerant but they must NOT have any negative voltage applied. They are terminated with a 392−Ohm resistor to 3.3V and a 392−Ohm resistor to ground.

2.13 XMC Panel LEDs

The 71661 front panel has ten LED indicators, as illustrated in Figure 2–10.

2.13.1 Link LED **LNK**

The green **LNK** LED illuminates when a valid link has been established over the PCIe interface.

2.13.2 User LED **USR**

The green **USR** LED is for user applications. Refer to the LED Control Register, Model 71660 Operating Manual, for control of this LED.

2.13.3 Master LED **MAS**

The yellow **MAS** LED illuminates when this Model 71661 is set as the sync bus Master (see Sync Bus Control Register 1, Model 71660 Operating Manual). When only a single 71661 is used, it must be a Master.

2.13.4 PPS LED **PPS**

The green **PPS** LED illuminates when a valid PPS signal is detected and will blink at the rate of the PPS signal.

2.13.5 Over Temperature LED **TMP**

The red **TMP** LED illuminates when an over–temperature or over–voltage condition is indicated by any of the temperature/voltage sensors on the Model 71661 PCB.

2.13.6 Clock LED **CLK**

The green **CLK** LED illuminates when a valid sample clock is detected. For reference clock mode, this LED indicates lock to the reference clock.

2.13.7 ADC Overload LEDs **OV**

There are four red **OV** overload LEDs, one for each A/D input. Use the ADC Data Control Register, Model 71660 Operating Manual, to select the signal source for each LED, either an overload in the associated ADS5485, or an ADC FIFO overrun.