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pickering

USER MANUAL

Model No. **20-610**

Very High Density Universal Multiplexer

Designed & Manufactured by:-
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If you need assistance with your Pickering Interfaces Switching System: Switching problems, Programming or Integration within your Test System.

– Please ring Pickering Interfaces and ask for “Technical Support”.

Alternatively you may fax, email or connect to our Internet Web Site.

A full set of operating manuals, application notes and software drivers is available on CD ROM.

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Section 1
Very High Density Universal Multiplexer

1.1 Features

- Very High Density 352 Pin Multiplexer
- Single, Dual or Quad Multiplexer Operation, Switching 1, 2, 4 or 8 Poles
- Expandable to 10,000 Channels Using Internal Analogue Bus
- Automatic Isolation Switches Reduce Capacitive Loading in Large Systems
- High Quality Ruthenium Reed Relays For Maximum Reliability
- Built-In Self Test
- Suitable for Ribbon Cable Connection
- Versatile Configuration Options: “One Module for ALL Your General Purpose Multiplexer Applications”
- Lower Density 176 Pin Version Available

The Universal Very High Density Multiplexer, Model 20-610, offers the highest density of any Pickering Multiplexer, with 352 switch pins. Configurable as a single, dual or quad multiplexer with a choice of 1, 2, 4 or 8 pole switching and is expandable to over 10,000 channels.

1.1 Description

The 20-610 Universal 352 Pin Multiplexer Module is the first in a new generation of very high density multiplexers from Pickering Interfaces. One standard module offers a very large range of switching configurations plus extensive built in self-test.

The 20-610 may be easily configured for most general purpose multiplexer requirements. Just by setting on-board links the unit may be configured as a single, dual or quad multiplexer with a choice of 1, 2, 4 or 8 pole operation (total of 18 configurations). The analogue common/s may be routed to the front panel or, for large system implementation, to one of the internal analogue buses. This versatility means that one multiplexer module is suitable for many different applications.

For applications that require lower capacity a reduced density version, type 20-610-021, is available, this has 176 pins.

Up to 2816 input channels can be accommodated in one System 20 Case, over 10,000 with multiple expansion cases.

Built-in Automatic Isolation Switching connects only the currently active multiplexer switch bank, thereby keeping capacitive loading and leakage currents in large multiplexer systems to a minimum.

For a summary of switching capabilities please refer to table 1.1.

This is a double height module and **must** be mounted into a double height (6U) case.

1.2 Front Panel

The module front panels comprise of three elements:

Status Display**, 4 LED Indicators:-**

Power LED.	Connected to power system supply.
Active LED.	On whenever one or more matrix switches are closed. For a list of all active switches use the VIEW? command.
Warning LED.	Indicates that an error may be soon be failing (relay contacts reaching end of life).
Self-Test LED.	Active when self-test in progress.
Error LED.	Indicates that error found during self-test.

Serial (RS-232) Configuration/Test Port

The 20-610 has a built in RS-232 port (9600 baud software handshake), this is used to configure the module and may also used for self test and error diagnosis (this may also be done using the normal IEEE-488/RS-232 interface).

Connectors - suitable for ribbon cable connection

Connection to the module front panel is via four 96 way DIN41612 connector plugs. Because of the large number of connections that may to be made to this module (up to 384) care must be taken with user connections. IDC type DIN41612 connectors may be used. Other connector types may be available, please contact sales office for further information.

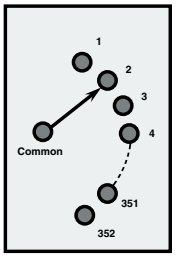


Fig .1.1 Single MUX Mode: 44, 88, 176 or 352 Channels

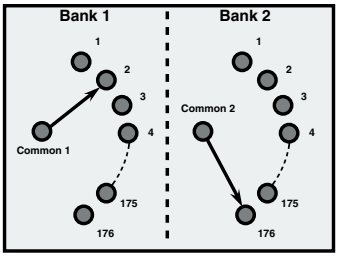


Fig 1.2 Dual MUX Mode: 44, 88 or 176 Channels

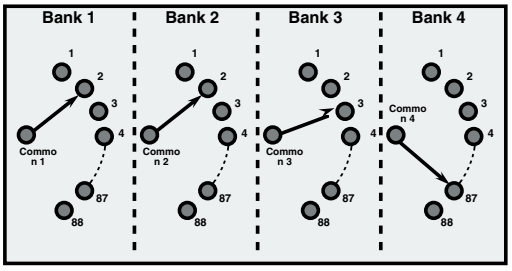


Fig 1.3 Quad MUX Mode: 44 or 88 Channels

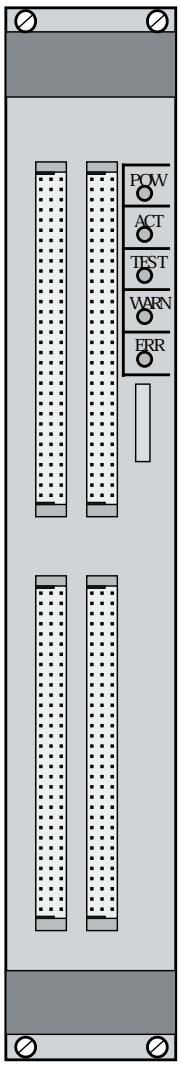


Fig 1.4 20-610 Front Panel Module Illustration

1.3 Analogue Bus

The analogue common can be routed (using internal jumpers) out to either the front panel connectors or the internal analogue bus. Routing to the front panel allows the user complete flexibility, routing to the internal analogue bus simplifies large system construction and ensures good signal isolation from external interference.

The System 10/20 backplane features a shielded 24 pole analogue bus. This would be used with a multiplexer constructed using more than one module where the selected channel will be carried along the System 20 backplane analogue bus.

The analogue bus can be brought out from the module in any of the following ways:-

1. The selected analogue common can be brought out on the front panel input connector. This also has the additional feature of keeping the analogue signal totally isolated from the backplane, improving crosstalk, dc leakage and low thermal emf performance.
2. Via a Breadboard module. Very useful if any signal conditioning, boosting etc. is to be done before bringing the signal out to the measuring device.

1.4 Width and Dimensions

All modules conform to the 6U height (262mm) Eurocard standard and are 160mm deep. Panel width is 1.8 Inches.

Switch Type	Ruthenium Reed
Max Standoff Voltage	100V
Max Power	10W
Max Switch Current	0.5A
Max Carry Current	1.2A
Path Resistance	
On (Single Module):	500mΩ (typical)
Off (Single Module):	> 10^9 Ω
Differential Thermal Offset	< 5µV
Capacitance	
Open Channel	< 6pF
Channel to Channel	< 30pF
Crosstalk (Single Chan On, 50Ω)	
Channel to Channel 10kHz	> 80dB
Channel to Channel 100kHz	> 65dB
Channel to Channel 1MHz	> 45dB
Bank to Bank 100kHz	> 80dB
Bank to Bank 1MHz	> 65dB
Bandwidth (3dB, 1 module)	> 5MHz
Noise Level (0 to 1MHz in 50Ω System)	< - 80dBm
Max Operate Time	7ms
Max Release Time	6ms
Expected Life (Operations)	
Low power load	> 10^8
Full power load	> $5x10^6$

† All the above specifications are for a complete 20-610 system consisting of eight multiplexers.

Table 1.1 Switching Specification

1.5 20-610 Operating Modes

Refer to Section 2 for further details.

The 20-610-022 very high density multiplexer operates in all of the following modes:-

Quad	88 Channel	1 Pole Switching
Quad	44 Channel	2 Pole Switching
Dual	176 Channel	1 Pole Switching
Dual	88 Channel	2 Pole Switching
Dual	44 Channel	4 Pole Switching
Single	352 Channel	1 Pole Switching
Single	176 Channel	2 Pole Switching
Single	88 Channel	4 Pole Switching
Single	44 Channel	8 Pole Switching

The 20-610-021 high density multiplexer operates in all of the following modes:-

Quad	44 Channel	1 Pole Switching
Dual	88 Channel	1 Pole Switching
Dual	44 Channel	2 Pole Switching
Single	176 Channel	1 Pole Switching
Single	88 Channel	2 Pole Switching
Single	44 Channel	4 Pole Switching

Analogue Common Connections

Route Analogue Common to Front Panel
Route Analogue Common to Internal Analogue Buses

Expansion to multi case systems is achieved by choosing one module within each case and selecting the analogue bus to front panel configuration, the analogue bus commons are then simply daisy-chained to additional cases as required.

Multi channel selection: Care must be taken when selecting many channels simultaneously not to overrate the power supply.

20-610-022 352 Pin Multiplexer, Very High Density
20-610-021 176 Pin Multiplexer, High Density
Suitable Mating Connectors: **10-967-001** 96 Way DIN 41612 Socket (with Crimp Pins) **10-967-101** 96 Way DIN 41612 IDC Socket **10-967-201** 96 Way IDC Cable (1m, other lengths to order)

Table 1.2 20-610 Product Order Codes

2.1 Creating Larger Multiplexers

When more than one module is used to make up a multiplexer – see diagram below, where seven modules are used to make up a 1232 channel 2 pole multiplexer – then all multiplexer units must have the same internal address, the location of each module within the multiplexer is given by its own bank address. Bank addresses must start at 0 and should be contiguous.

If there is a problem with any of the modules used to make up a large multiplexer then an error will be detected (use the REPORT? query to discover the cause).

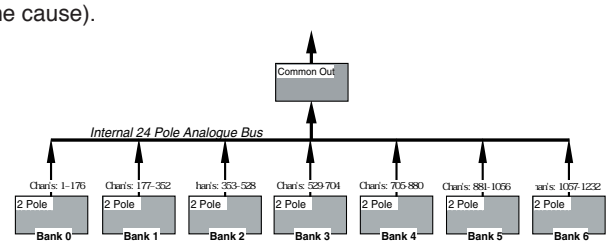


Fig 2.1 20-610 Expansion

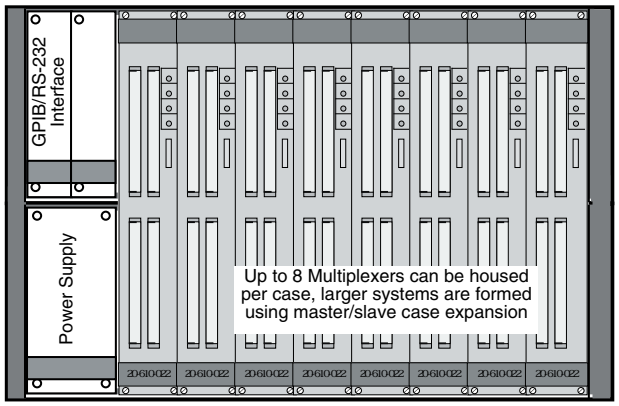


Fig 2.2 Up to 8 x 20-610 Multiplexers Can Be Held In One Case (e.g. 2816 Channel 1 Pole)

2.2 Multiplexer Configurations

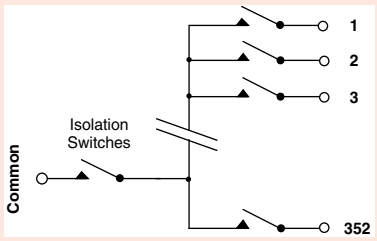
The 20-610-022 very high density multiplexer operates in all of the following modes:-

20-610-022 Multiplexer Mode	Number of Channels	Number of Poles	Front Analogue Bus	Rear Analogue Bus
Single MUX	352	1	**352/1/F**	**352/1/R**
Single MUX	176	2	**176/2/F**	**176/2/R**
Single MUX	88	4	**88/4/F**	**88/4/R**
Single MUX	44	8	**44/8/F**	**44/8/R**
Dual MUX	176	1	**176/1/F**	**176/1/R**
Dual MUX	88	2	**88/2/F**	**88/2/R**
Dual MUX	44	4	**44/4/F**	**44/4/R**
Quad MUX	88	1	**88/1/F**	**88/1/R**
Quad MUX	44	2	**44/2/F**	**44/2/R**

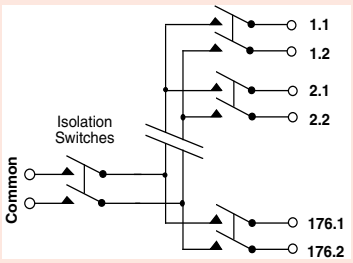
Table 2.1 20-610-022 Very High Density Configurations

20-610-021 Multiplexer Mode	Number of Channels	Number of Poles	Front Analogue Bus	Rear Analogue Bus
Single MUX	176	1	**176/1/F**	**176/1/R**
Single MUX	88	2	**88/2/F**	**88/2/R**
Single MUX	44	4	**44/2/F**	**44/2/R**
Dual MUX	88	1	**88/2/F**	**88/1/R**
Dual MUX	44	2	**44/2/F**	**44/1/R**
Quad MUX	44	1	**44/2/F**	**44/1/R**

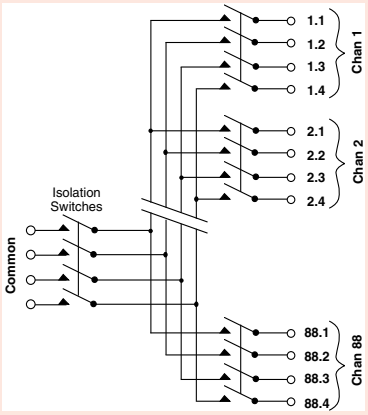
Table 2.2 20-610-021 High Density Configurations



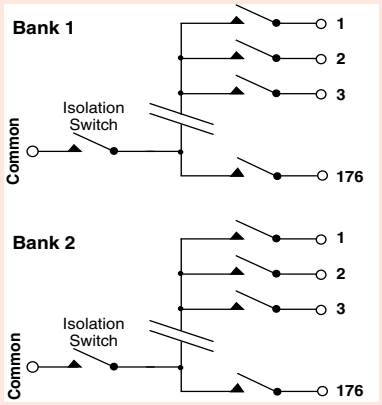
Single 352 Channel 1 Pole



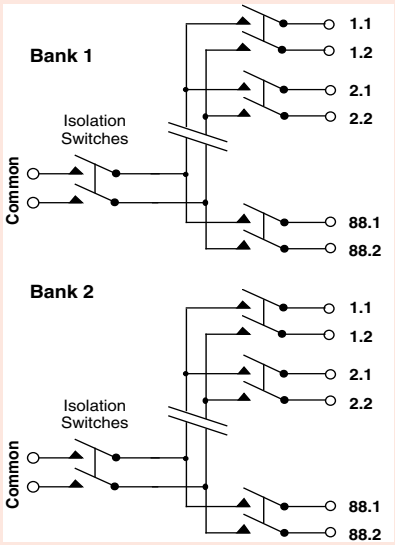
Single 176 Channel 2 Pole



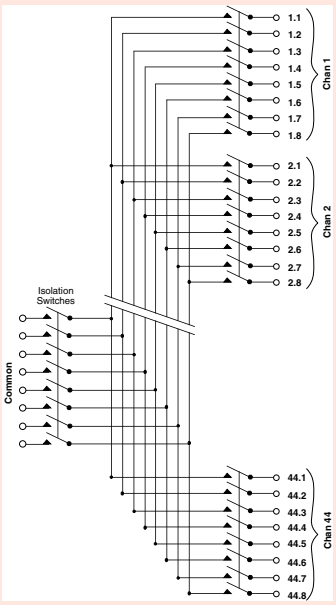
Single 88 Channel 4 Pole



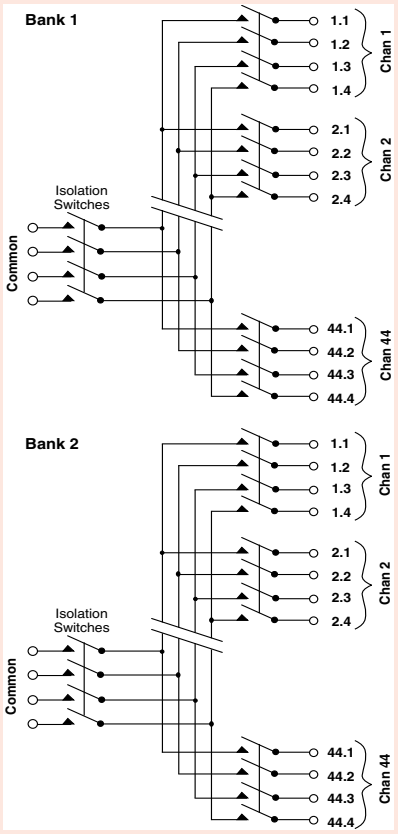
Dual 176 Channel 1 Pole



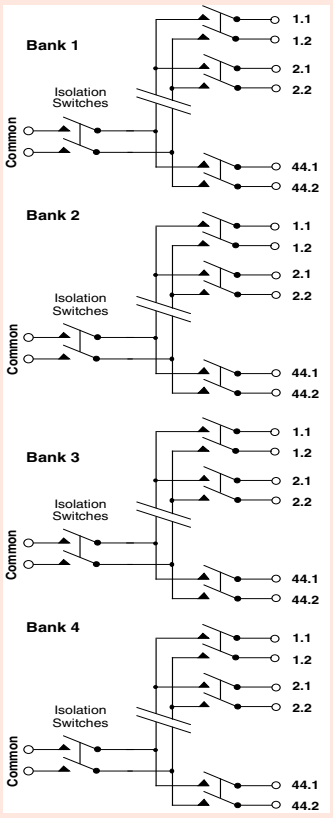
Dual 88 Channel 2 Pole



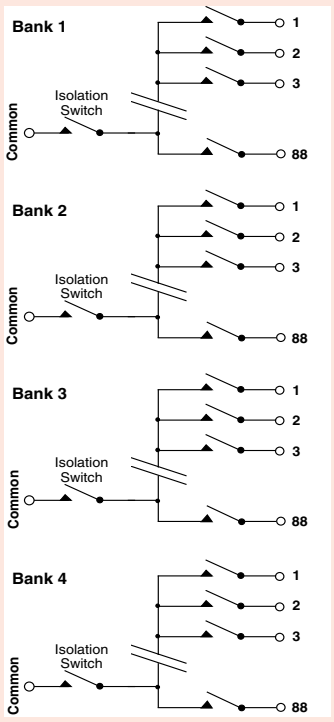
Single 44 Channel 8 Pole



Dual 44 Channel 4 Pole



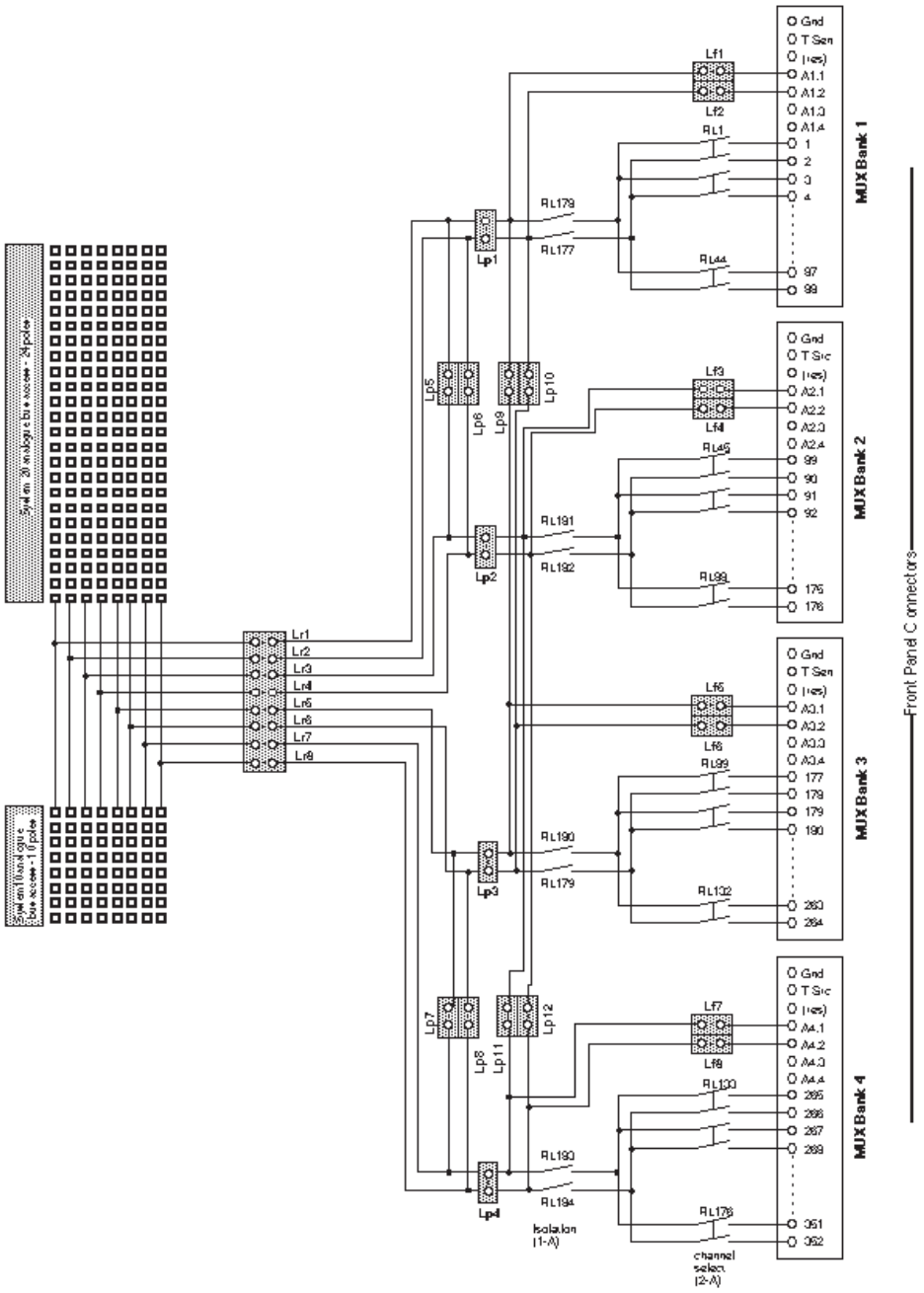
Quad 44 Channel 2 Pole



Quad 88 Channel 1 Pole

Fig 2.3 20-610-022 Very High Density Multiplexer Configurations

(20-610-021 High Density Multiplexers have exactly half the capacity of the above versions).



20-610-022 link settings

Mode	Channels	Poles	Connect Links		Comment	20-610-021 links mode code	20-610-021 links links	bank 1	common poles - NW local on bank 2	bank 3	bank 4
Quad	99	1	Front	Lf1,3,5,7	Lp1,2,3,4	No multi-chan selection	44/1/F	Lf1,3,5,7	1	1	1
Quad	99	1	Rear	Lr1,3,5,7	Lp1,2,3,4	No multi-chan selection	44/1/R	Lr1,3,5,7			
Quad	44	2	Front	Lf1,2,3,4,5,6,7,9							
Quad	44	2	Rear	Lr1,2,3,4,5,6,7,9							
Dual	176	1	Front	Lf1,5	Lp1,3,5,6,7,9	No multi-chan selection	99/1/F	Lf1,5 Lr1,5	Lp5,6,7 Lp5,6,7	1 -	1	-
Dual	176	1	Rear	Lr1,5	Lp1,3,5,6,7,9	No multi-chan selection	99/1/R					
Dual	99	2	Front	Lf1,2,5,6	Lp5,6,7,9		44/2/F		Lf1,3,5,7	1	2	1
Dual	99	2	Rear	Lr1,2,5,6	Lp5,6,7,9		44/2/R		Lr1,3,5,7			
Dual	44	4	Front	Lf1,2,3,4,5,6,7,9								
Dual	44	4	Rear	Lr1,2,3,4,5,6,7,9								
Single	352	1	Front	Lf1	Lp1,2,3,4,5,6,7,9	No multi-chan selection	176/1/F	Lf1	Lp5,7,9	1 -	-	-
Single	352	1	Rear	Lr1	Lp1,2,3,4,5,6,7,9	No multi-chan selection	176/1/R	Lr1	Lp5,7,9			
Single	176	2	Front	Lf1,2	Lp5,6,7,9,9,10		99/2/F	Lf1,5	Lp5,7	1 -	2	-
Single	176	2	Rear	Lr1,2	Lp5,6,7,9,9,10		99/2/R	Lr1,5	Lp5,7			
Single	99	4	Front	Lf1,2,3,4	Lp9,10,11,12		44/4/F	Lf1,3,5,7		1 2	3	4
Single	99	4	Rear	Lr1,2,3,4	Lp9,10,11,12		44/4/R	Lr1,3,5,7				
Single	44	9	Front	Lf1,2,3,4,5,6,7,9								
Single	44	9	Rear	Lr1,2,3,4,5,6,7,9								

Notes:
- 3 configurations not possible with lower density version (20-610-021) - same applied to 10-630A i.e. fewer configurations available using lower density version;
  quad / 22 chan / 2 pole.
  dual / 22 chan / 4 pole.
  single / 22 chan / 9 pole.
  reason - maximum number of poles for this version is 4 (the 3 above each require 9)
- the following are different for each version (i.e. 20-610-022/021)
  link diagrams
  front panel connections
  software
- pcb queries - series limiting resistors

Fig 2.4 20-610 Multiplexer Relay Layout

Showing How Configuration Links Allow The 20-610 To Operate In Many Configurations

3.1 Self-Test Function

Self-Test is invoked at power on and may also be operated under software (*TST?) or via a recessed push button. Self-Test pass is indicated on a front panel LED with a full pass/fail description available using the DIAGNOSTIC? command.

Self-Test comprises 2 levels, see Fig 3.1:-

1. **Logic Test**: Checks all logic including on-board microprocessor, relay drivers etc.
2. **Relay Coil Test**: All reed relay coils are checked for continuity.

Note: **Spare reed relays** are mounted onto the relay circuit board for fast repair, additional reed relays are available from Pickering Interfaces.

3.2 Self-Test Operation

Self Test is always run at power on. If self test is run under software control it will firstly **clear the whole multiplexer** (Manual Test will only function when the module is in a clear state). When the self-test has finished the multiplexer will be returned to an all clear state (i.e. the previous state will not be remembered!).

Please note that because of the long self-test time that your computer may time out waiting for the test result (many PC's have default timeouts set to **10 seconds**).

3.3 Detailed Self-Test Reporting using the DIAGNOSTIC? Query

The DIAGNOSTIC? query will give an ASCII string detailing any self test failures. These will include:-

Logic: μP, RAM, EPROM, Relay Drivers, Invalid Link Settings etc.

Relay Coils: Open Circuit Coil.

This string is not intended to be processed by the user's software, it is suitable for copying directly onto the screen of your control computer. This information will then indicate maintenance required (please contact Pickering for further help).

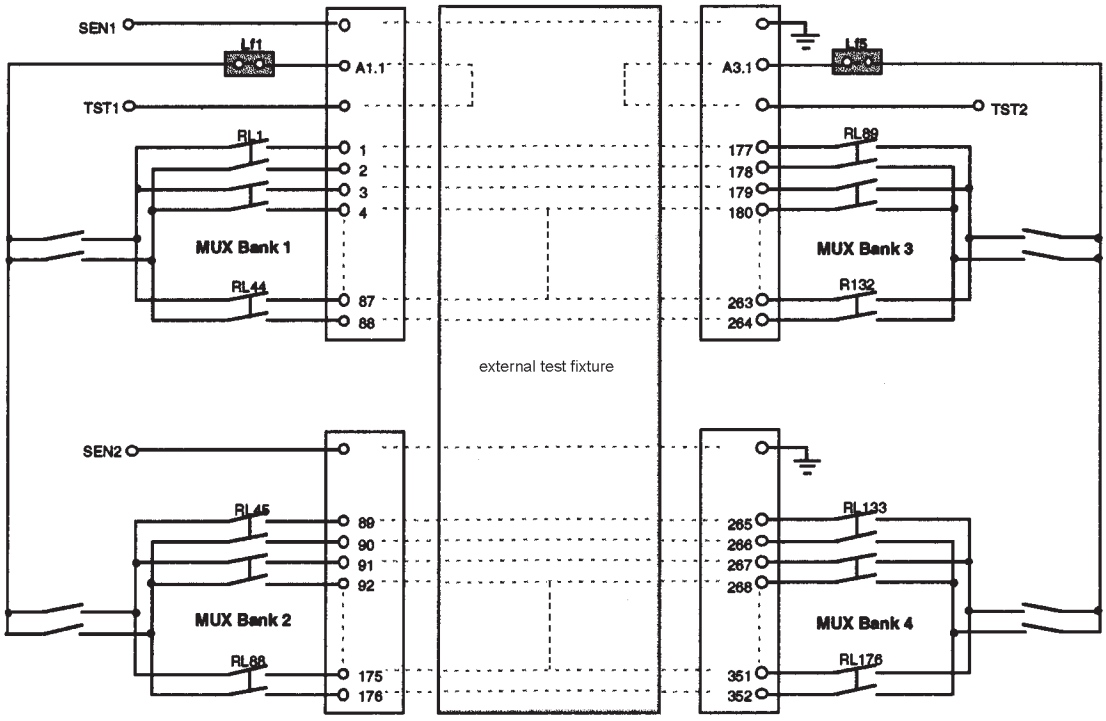


Fig 3.1 610 Relay Contact Test
(not implemented in current version)

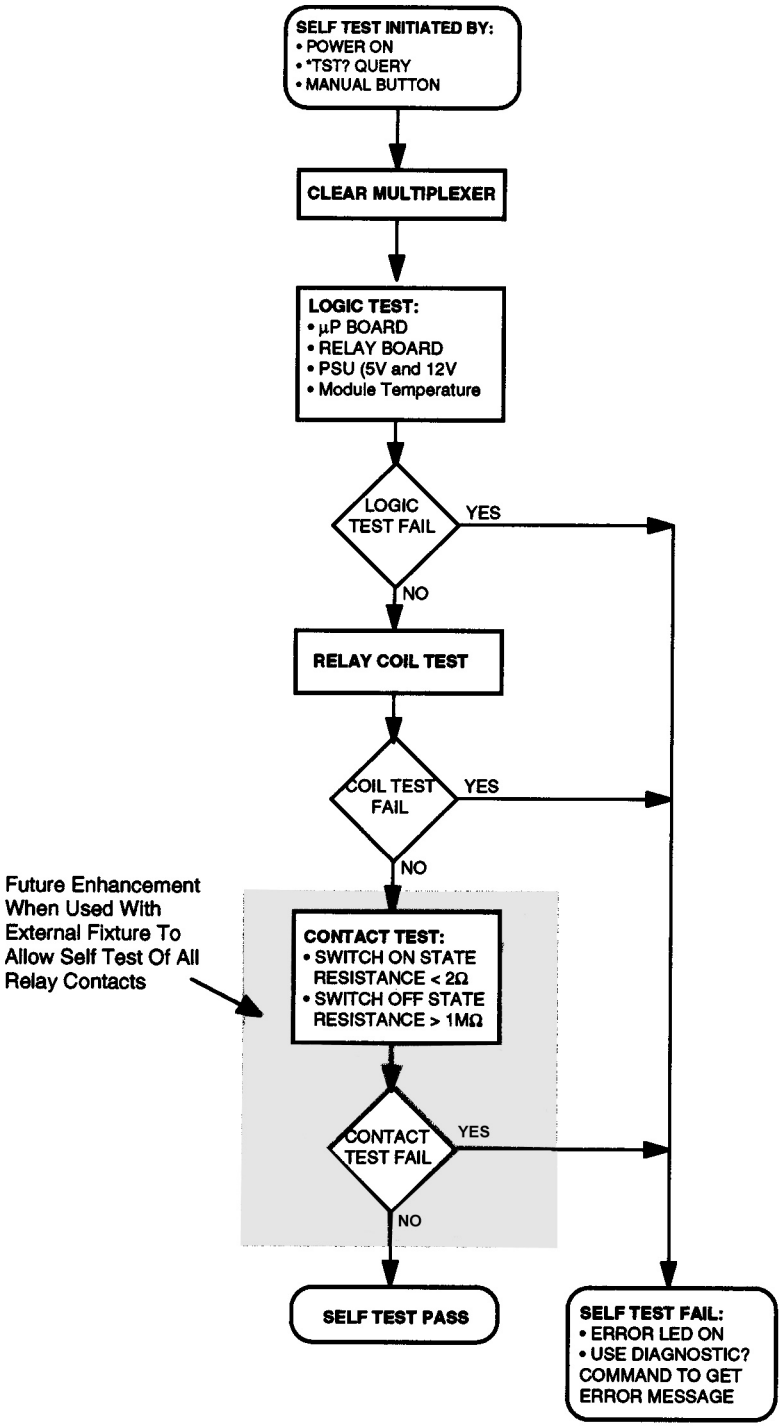


Fig 3.2 Self-Test: Basic Flow Diagram

4.1 Instruction Set

The 20-610 Multiplexer module is simple to program:-

ARESET a	Open all channels on device **a**.
CHAN a,c	Select channel **c** on multiplexer **a, bank b.**
CHAN a,b,c,s	Multi-Channel selection argument **s** allows opening/closing of any combination of channels. Also allows selection of all channels except **c** (not available in 1 pole mode on very high density 20-610-022).
DELAY t	Force a minimum delay of **t** milliseconds between two instructions
DIAGNOSTIC?	Report any Self Test errors.
RESET	Open all switches on all modules
VIEW? a	View status of device **a**.

The 20-610 module must be used in conjunction with the 10-921 or 20-910 interface module (it is not compatible with the older 10-920 interface).

4.2 Multiplexer Expansion

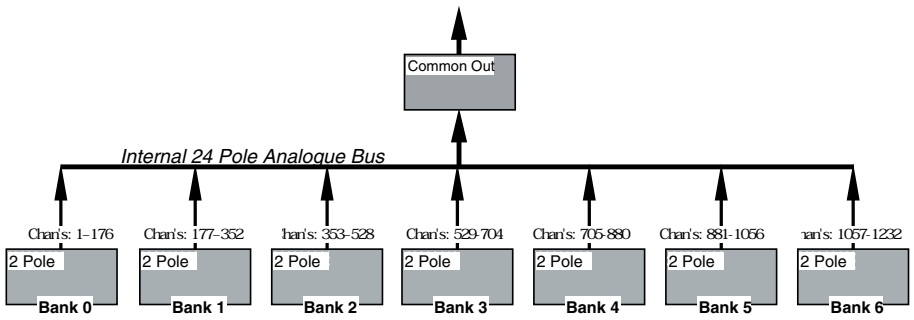


Fig 4.1 Configuring the Multiplexer System

(all modules must have the same primary address)

4.3 Configuration Specific Programming Commands

The 20-610 multiplexer module may be configured in one of the following modes:-

4.3.1 Quad/Dual Multiplexer Mode

Each module contains four or two independent multiplexers (e.g.dual 176 channel or quad 44 channel), referred to as banks 1,2, 3 and 4:

CHAN a,b,c	Select channel c on bank b of multiplexer a. Only one channel at a time is permitted to be on, automatic break-before-make is always enforced. e.g. CHAN 3,1,34 will operate the module with address 3 selecting bank 1 channel 34. CHAN 15,2,1 will operate the module with address 15 selecting bank 2 channel 1.

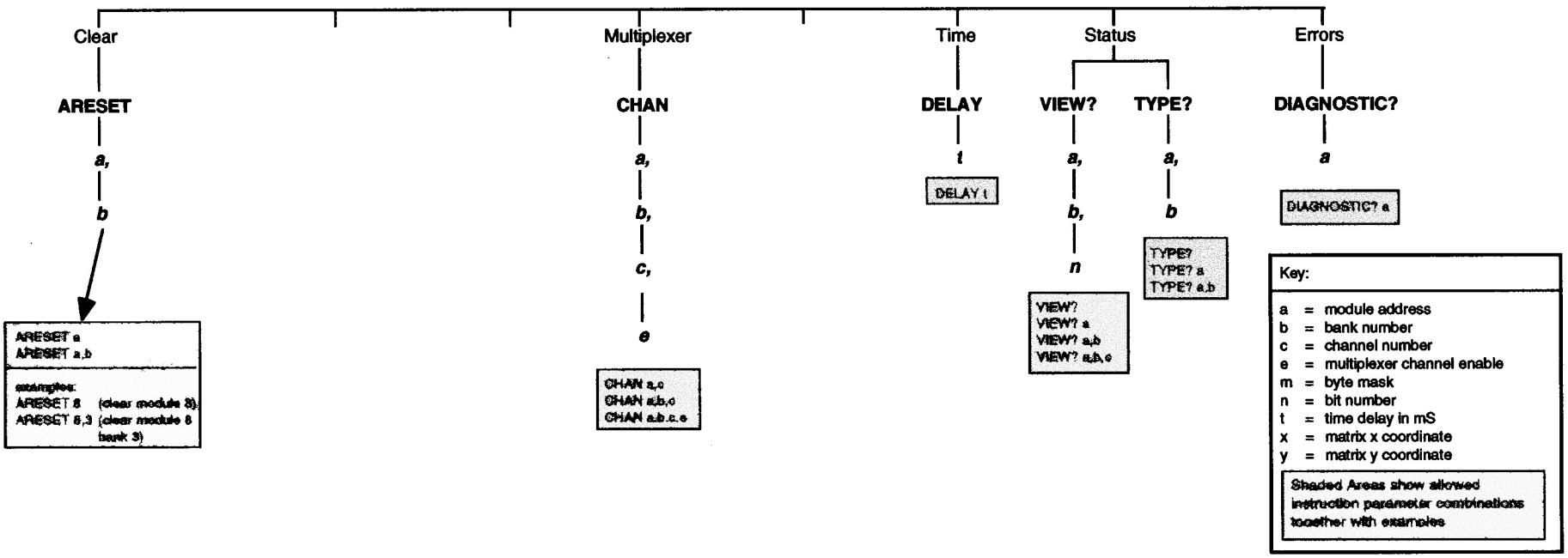


Fig 4.2 20-610 Multiplexer Module Instruction Set

4.3.2 Multiple Channel Selection (not allowed in 1 channel mode)

To operate more than one channel at any time an extra enable/disable argument, s, must be added to the CHAN command. The command will allow any combination of channels to be selected (note: not available in single pole mode):

`CHAN a,b,c,s` Select channel `c,` if `s` = 1 (i.e. `s` <> 0) on bank `b` of multiplexer `a.`
Deselect channel `c,` if `s` = 0, on multiplexer `a.`

Please make **particular note** of the following points:-

- When the multi-channel form of the `CHAN` command is used the automatic break-before-make operation of the multiplexer is disabled, it can only be enabled again by issuing a standard `CHAN a,c` command (this will first clear all selected channels on that multiplexer).
- Care must be taken not to inadvertently short any two signal source inputs together.
- The Isolation switches are always energised in multi-channel mode, therefore leakage resistance and stray capacitance will degrade.
- Multi-channel commands can **not** be used when in 1 pole mode, this is a limitation of the internal switching arrangement.

4.4 Programming Examples

Multiplexers are controlled using the CHAN and ARESET commands. The 20-640 series of multiplexers have two modes of operation:-

First, to check the size of the multiplexer at address 21.
`TYPE? 21` will return "`MUX(2x176)`". A dual 176 channel multiplexer.
To close channel 3 (bank 1) on multiplexer 21.
`CHAN 21,1,3`
Now to look at status of multiplexer 21, bank 1.
`VIEW? 21,1` will return "`3`".
To clear bank 1.
`ARESET 21,1`
Or to clear all banks.
`ARESET 21`
Now to look at status.
`VIEW? 21,1` will return "0".
`VIEW? 21` will return the status of all multiplexer banks.

Note: This module must be used with the 10-921 IEEE-488/RS-232 Interface.

Section 5
Connector Pin-Out Diagrams

The following pin out diagrams for the 20-610-022 very high density multiplexer are included:-

Quad	88 Channel	1 Pole Switching
Quad	44 Channel	2 Pole Switching
Dual	176 Channel	1 Pole Switching
Dual	88 Channel	2 Pole Switching
Dual	44 Channel	4 Pole Switching
Single	352 Channel	1 Pole Switching
Single	176 Channel	2 Pole Switching
Single	88 Channel	4 Pole Switching
Single	44 Channel	8 Pole Switching

Blank DIN 41612 Connector Sheets are in Fig 5.16 and 5.17.

Bank 1

	A	B	C
32	1	2	3
31	4	5	6
30	7	8	9
29	10	11	12
28	13	14	15
27	16	17	18
26	19	20	21
25	22	23	24
24	25	26	27
23	28	29	30
22	31	32	33
21	34	35	36
20	37	38	39
19	40	41	42
18	43	44	45
17	46	47	48
16	49	50	51
15	52	53	54
14	55	56	57
13	58	59	60
12	61	62	63
11	64	65	66
10	67	68	69
9	70	71	72
8	73	74	75
7	76	77	78
6	79	80	81
5	82	83	84
4	85	86	87
3	88	GND	GND
2	C1	-	-
1	-	SEN 1	TST 1

(MUX 1)

Bank 3

	A	B	C
32	1	2	3
31	4	5	6
30	7	8	9
29	10	11	12
28	13	14	15
27	16	17	18
26	19	20	21
25	22	23	24
24	25	26	27
23	28	29	30
22	31	32	33
21	34	35	36
20	37	38	39
19	40	41	42
18	43	44	45
17	46	47	48
16	49	50	51
15	52	53	54
14	55	56	57
13	58	59	60
12	61	62	63
11	64	65	66
10	67	68	69
9	70	71	72
8	73	74	75
7	76	77	78
6	79	80	81
5	82	83	84
4	85	86	87
3	88	GND	GND
2	C3	-	-
1	-	GND	TST 2

(MUX 3)

Bank 2

	A	B	C
32	1	2	3
31	4	5	6
30	7	8	9
29	10	11	12
28	13	14	15
27	16	17	18
26	19	20	21
25	22	23	24
24	25	26	27
23	28	29	30
22	31	32	33
21	34	35	36
20	37	38	39
19	40	41	42
18	43	44	45
17	46	47	48
16	49	50	51
15	52	53	54
14	55	56	57
13	58	59	60
12	61	62	63
11	64	65	66
10	67	68	69
9	70	71	72
8	73	74	75
7	76	77	78
6	79	80	81
5	82	83	84
4	85	86	87
3	88	GND	GND
2	C2	-	-
1	-	SEN 2	-

(MUX 2)

Bank 4

	A	B	C
32	1	2	3
31	4	5	6
30	7	8	9
29	10	11	12
28	13	14	15
27	16	17	18
26	19	20	21
25	22	23	24
24	25	26	27
23	28	29	30
22	31	32	33
21	34	35	36
20	37	38	39
19	40	41	42
18	43	44	45
17	46	47	48
16	49	50	51
15	52	53	54
14	55	56	57
13	58	59	60
12	61	62	63
11	64	65	66
10	67	68	69
9	70	71	72
8	73	74	75
7	76	77	78
6	79	80	81
5	82	83	84
4	85	86	87
3	88	GND	GND
2	C4	-	-
1	-	GND	-

(MUX 4)

Fig 5.1 Pin Out Diagram For Quad 88 Channel 1 Pole Mode

Bank 1

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C1.1	C1.2	-
1	-	SEN 1	TST 1

(MUX 1)

Bank 3

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C3.1	C3.2	-
1	-	GND	TST 2

(MUX 3)

Bank 2

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C2.1	C2.2	-
1	-	SEN 2	-

(MUX 2)

Bank 4

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C4.1	C4.2	-
1	-	GND	-

(MUX 4)

Fig 5.2 Pin Out Diagram For Quad 44 Channel 2 Pole Mode

Bank 1

	A	B	C
32	1	2	3
31	4	5	6
30	7	8	9
29	10	11	12
28	13	14	15
27	16	17	18
26	19	20	21
25	22	23	24
24	25	26	27
23	28	29	30
22	31	32	33
21	34	35	36
20	37	38	39
19	40	41	42
18	43	44	45
17	46	47	48
16	49	50	51
15	52	53	54
14	55	56	57
13	58	59	60
12	61	62	63
11	64	65	66
10	67	68	69
9	70	71	72
8	73	74	75
7	76	77	78
6	79	80	81
5	82	83	84
4	85	86	87
3	88	GND	GND
2	C1	-	-
1	-	SEN 1	TST 1

(MUX 1)

Bank 3

	A	B	C
32	1	2	3
31	4	5	6
30	7	8	9
29	10	11	12
28	13	14	15
27	16	17	18
26	19	20	21
25	22	23	24
24	25	26	27
23	28	29	30
22	31	32	33
21	34	35	36
20	37	38	39
19	40	41	42
18	43	44	45
17	46	47	48
16	49	50	51
15	52	53	54
14	55	56	57
13	58	59	60
12	61	62	63
11	64	65	66
10	67	68	69
9	70	71	72
8	73	74	75
7	76	77	78
6	79	80	81
5	82	83	84
4	85	86	87
3	88	GND	GND
2	C2	-	-
1	-	GND	TST 2

(MUX 2)

Bank 2

	A	B	C
32	89	90	91
31	92	93	94
30	95	96	97
29	98	99	100
28	101	102	103
27	104	105	106
26	107	108	109
25	110	111	112
24	113	114	115
23	116	117	118
22	119	120	121
21	122	123	124
20	125	126	127
19	128	129	130
18	131	132	133
17	134	135	136
16	137	138	139
15	140	141	142
14	143	144	145
13	146	147	148
12	149	150	151
11	152	153	154
10	155	156	157
9	158	159	160
8	161	162	163
7	164	165	166
6	167	168	169
5	170	171	172
4	173	174	175
3	176	GND	GND
2	-	-	-
1	-	SEN 2	-

(MUX 1)

Bank 4

	A	B	C
32	89	90	91
31	92	93	94
30	95	96	97
29	98	99	100
28	101	102	103
27	104	105	106
26	107	108	109
25	110	111	112
24	113	114	115
23	116	117	118
22	119	120	121
21	122	123	124
20	125	126	127
19	128	129	130
18	131	132	133
17	134	135	136
16	137	138	139
15	140	141	142
14	143	144	145
13	146	147	148
12	149	150	151
11	152	153	154
10	155	156	157
9	158	159	160
8	161	162	163
7	164	165	166
6	167	168	169
5	170	171	172
4	173	174	175
3	176	GND	GND
2	-	-	-
1	-	GND	-

(MUX 2)

Fig 5.3 Pin Out Diagram For Dual 176 Channel 1 Pole Mode

Bank 1

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C1.1	C1.2	-
1	-	SEN 1	TST1

(MUX 1)

Bank 3

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C2.1	C2.2	-
1	-	GND	TST2

(MUX 2)

Bank 2

	A	B	C
32	45.1	45.2	46.1
31	46.2	47.1	47.2
30	48.1	48.2	49.1
29	49.2	50.1	50.2
28	51.1	51.2	52.1
27	52.2	53.1	53.2
26	54.1	54.2	55.1
25	55.2	56.1	56.2
24	57.1	57.2	58.1
23	58.2	59.1	59.2
22	60.1	60.2	61.1
21	61.2	62.1	62.2
20	63.1	63.2	64.1
19	64.2	65.1	65.2
18	66.1	66.2	67.1
17	67.2	68.1	68.2
16	69.1	69.2	70.1
15	70.2	71.1	71.2
14	72.1	72.2	73.1
13	73.2	74.1	74.2
12	75.1	75.2	76.1
11	76.2	77.1	77.2
10	78.1	78.2	79.1
9	79.2	80.1	80.2
8	81.1	81.2	82.1
7	82.2	83.1	83.2
6	84.1	84.2	85.1
5	85.2	86.1	86.2
4	87.1	87.2	88.1
3	88.2	GND	GND
2	-	-	-
1	-	SEN 2	-

(MUX 1)

Bank 4

	A	B	C
32	45.1	45.2	46.1
31	46.2	47.1	47.2
30	48.1	48.2	49.1
29	49.2	50.1	50.2
28	51.1	51.2	52.1
27	52.2	53.1	53.2
26	54.1	54.2	55.1
25	55.2	56.1	56.2
24	57.1	57.2	58.1
23	58.2	59.1	59.2
22	60.1	60.2	61.1
21	61.2	62.1	62.2
20	63.1	63.2	64.1
19	64.2	65.1	65.2
18	66.1	66.2	67.1
17	67.2	68.1	68.2
16	69.1	69.2	70.1
15	70.2	71.1	71.2
14	72.1	72.2	73.1
13	73.2	74.1	74.2
12	75.1	75.2	76.1
11	76.2	77.1	77.2
10	78.1	78.2	79.1
9	79.2	80.1	80.2
8	81.1	81.2	82.1
7	82.2	83.1	83.2
6	84.1	84.2	85.1
5	85.2	86.1	86.2
4	87.1	87.2	88.1
3	88.2	GND	GND
2	-	-	-
1	-	GND	-

(MUX 2)

Fig 5.4 Pin Out Diagram For Dual 88 Channel 2 Pole Mode

Bank 1

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C1.1	C1.2	-
1	-	SEN 1	TST 1

(MUX 1)

Bank 3

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C2.1	C2.2	-
1	-	GND	TST 2

(MUX 2)

Bank 2

	A	B	C
32	1.3	1.4	2.3
31	2.4	3.3	3.4
30	4.3	4.4	5.3
29	5.4	6.3	6.4
28	7.3	7.4	8.3
27	8.4	9.3	9.4
26	10.3	10.4	11.3
25	11.4	12.3	12.4
24	13.3	13.4	14.3
23	14.4	15.3	15.4
22	16.3	16.4	17.3
21	17.4	18.3	18.4
20	19.3	19.4	20.3
19	20.4	21.3	21.4
18	22.3	22.4	23.3
17	23.4	24.3	24.4
16	25.3	25.4	26.3
15	26.4	27.3	27.4
14	28.3	28.4	29.3
13	29.4	30.3	30.4
12	31.3	31.4	32.3
11	32.4	33.3	33.4
10	34.3	34.4	35.3
9	35.4	36.3	36.4
8	37.3	37.4	38.3
7	38.4	39.3	39.4
6	40.3	40.4	41.3
5	41.4	42.3	42.4
4	43.3	43.4	44.3
3	44.4	GND	GND
2	C1.3	C1.4	-
1	-	SEN 2	-

(MUX 1)

Bank 4

	A	B	C
32	1.3	1.4	2.3
31	2.4	3.3	3.4
30	4.3	4.4	5.3
29	5.4	6.3	6.4
28	7.3	7.4	8.3
27	8.4	9.3	9.4
26	10.3	10.4	11.3
25	11.4	12.3	12.4
24	13.3	13.4	14.3
23	14.4	15.3	15.4
22	16.3	16.4	17.3
21	17.4	18.3	18.4
20	19.3	19.4	20.3
19	20.4	21.3	21.4
18	22.3	22.4	23.3
17	23.4	24.3	24.4
16	25.3	25.4	26.3
15	26.4	27.3	27.4
14	28.3	28.4	29.3
13	29.4	30.3	30.4
12	31.3	31.4	32.3
11	32.4	33.3	33.4
10	34.3	34.4	35.3
9	35.4	36.3	36.4
8	37.3	37.4	38.3
7	38.4	39.3	39.4
6	40.3	40.4	41.3
5	41.4	42.3	42.4
4	43.3	43.4	44.3
3	44.4	GND	GND
2	C2.3	C2.4	-
1	-	GND	-

(MUX 2)

Fig 5.5 Pin Out Diagram For Dual 44 Channel 4 Pole Mode

Bank 1

	A	B	C
32	1	2	3
31	4	5	6
30	7	8	9
29	10	11	12
28	13	14	15
27	16	17	18
26	19	20	21
25	22	23	24
24	25	26	27
23	28	29	30
22	31	32	33
21	34	35	36
20	37	38	39
19	40	41	42
18	43	44	45
17	46	47	48
16	49	50	51
15	52	53	54
14	55	56	57
13	58	59	60
12	61	62	63
11	64	65	66
10	67	68	69
9	70	71	72
8	73	74	75
7	76	77	78
6	79	80	81
5	82	83	84
4	85	86	87
3	88	GND	GND
2	C1	-	-
1	-	SEN 1	TST 1

Bank 3

	A	B	C
32	177	178	179
31	180	181	182
30	183	184	185
29	186	187	188
28	189	190	191
27	192	193	194
26	195	196	197
25	198	199	200
24	201	202	203
23	204	205	206
22	207	208	209
21	210	211	212
20	213	214	215
19	216	217	218
18	219	220	221
17	222	223	224
16	225	226	227
15	228	229	230
14	231	232	233
13	234	235	236
12	237	238	239
11	240	241	242
10	243	244	245
9	246	247	248
8	249	250	251
7	252	253	254
6	255	256	257
5	258	259	260
4	261	262	263
3	264	GND	GND
2	-	-	-
1	-	GND	TST 2

Bank 2

	A	B	C
32	89	90	91
31	92	93	94
30	95	96	97
29	98	99	100
28	101	102	103
27	104	105	106
26	107	108	109
25	110	111	112
24	113	114	115
23	116	117	118
22	119	120	121
21	122	123	124
20	125	126	127
19	128	129	130
18	131	132	133
17	134	135	136
16	137	138	139
15	140	141	142
14	143	144	145
13	146	147	148
12	149	150	151
11	152	153	154
10	155	156	157
9	158	159	160
8	161	162	163
7	164	165	166
6	167	168	169
5	170	171	172
4	173	174	175
3	176	GND	GND
2	-	-	-
1	-	SEN 2	-

Bank 4

	A	B	C
32	265	266	267
31	268	269	270
30	271	272	273
29	274	275	276
28	277	278	279
27	280	281	282
26	283	284	285
25	286	287	288
24	289	290	291
23	292	293	294
22	295	296	297
21	298	299	300
20	301	302	303
19	304	305	306
18	307	308	309
17	310	311	312
16	313	314	315
15	316	317	318
14	319	320	321
13	322	323	324
12	325	326	327
11	328	329	330
10	331	332	333
9	334	335	336
8	337	338	339
7	340	341	342
6	343	344	345
5	346	347	348
4	349	350	351
3	352	GND	GND
2	-	-	-
1	-	GND	-

Fig 5.6 Pin Out Diagram For Single 352 Channel 1 Pole Mode

Bank 1

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C1.1	C1.2	-
1	-	SEN 1	TST1

Bank 3

	A	B	C
32	89.1	89.2	90.1
31	90.2	91.1	91.2
30	92.1	92.2	93.1
29	93.2	94.1	94.2
28	95.1	95.2	96.1
27	96.2	97.1	97.2
26	98.1	98.2	99.1
25	99.2	100.1	100.2
24	101.1	101.2	102.1
23	102.2	103.1	103.2
22	104.1	104.2	105.1
21	105.2	106.1	106.2
20	107.1	107.2	108.1
19	108.2	109.1	109.2
18	110.1	110.2	111.1
17	111.2	112.1	112.2
16	113.1	113.2	114.1
15	114.2	115.1	115.2
14	116.1	116.2	117.1
13	117.2	118.1	118.2
12	119.1	119.2	120.1
11	120.2	121.1	121.2
10	122.1	122.2	123.1
9	123.2	124.1	124.2
8	125.1	125.2	126.1
7	126.2	127.1	127.2
6	128.1	128.2	129.1
5	129.2	130.1	130.2
4	131.1	131.2	132.1
3	132.2	GND	GND
2	-	-	-
1	-	GND	TST2

Bank 2

	A	B	C
32	45.1	45.2	46.1
31	46.2	47.1	47.2
30	48.1	48.2	49.1
29	49.2	50.1	50.2
28	51.1	51.2	52.1
27	52.2	53.1	53.2
26	54.1	54.2	55.1
25	55.2	56.1	56.2
24	57.1	57.2	58.1
23	58.2	59.1	59.2
22	60.1	60.2	61.1
21	61.2	62.1	62.2
20	63.1	63.2	64.1
19	64.2	65.1	65.2
18	66.1	66.2	67.1
17	67.2	68.1	68.2
16	69.1	69.2	70.1
15	70.2	71.1	71.2
14	72.1	72.2	73.1
13	73.2	74.1	74.2
12	75.1	75.2	76.1
11	76.2	77.1	77.2
10	78.1	78.2	79.1
9	79.2	80.1	80.2
8	81.1	81.2	82.1
7	82.2	83.1	83.2
6	84.1	84.2	85.1
5	85.2	86.1	86.2
4	87.1	87.2	88.1
3	88.2	GND	GND
2	-	-	-
1	-	SEN 2	-

Bank 4

	A	B	C
32	133.1	133.2	134.1
31	134.2	135.1	135.2
30	136.1	136.2	137.1
29	137.2	138.1	138.2
28	139.1	139.2	140.1
27	140.2	141.1	141.2
26	142.1	142.2	143.1
25	143.2	144.1	144.2
24	145.1	145.2	146.1
23	146.2	147.1	147.2
22	148.1	148.2	149.1
21	149.2	150.1	150.2
20	151.1	151.2	152.1
19	152.2	153.1	153.2
18	154.1	154.2	155.1
17	155.2	156.1	156.2
16	157.1	157.2	158.1
15	158.2	159.1	159.2
14	160.1	160.2	161.1
13	161.2	162.1	162.2
12	163.1	163.2	164.1
11	164.2	165.1	165.2
10	166.1	166.2	167.1
9	167.2	168.1	168.2
8	169.1	169.2	170.1
7	170.2	171.1	171.2
6	172.1	172.2	173.1
5	173.2	174.1	174.2
4	175.1	175.2	176.1
3	176.2	GND	GND
2	-	-	-
1	-	GND	-

Fig 5.7 Pin Out Diagram For Single 176 Channel 2 Pole Mode

Bank 1

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C1.1	C1.2	-
1	-	SEN 1	TST1

Bank 3

	A	B	C
32	45.1	45.2	46.1
31	46.2	47.1	47.2
30	48.1	48.2	49.1
29	49.2	50.1	50.2
28	51.1	51.2	52.1
27	52.2	53.1	53.2
26	54.1	54.2	55.1
25	55.2	56.1	56.2
24	57.1	57.2	58.1
23	58.2	59.1	59.2
22	60.1	60.2	61.1
21	61.2	62.1	62.2
20	63.1	63.2	64.1
19	64.2	65.1	65.2
18	66.1	66.2	67.1
17	67.2	68.1	68.2
16	69.1	69.2	70.1
15	70.2	71.1	71.2
14	72.1	72.2	73.1
13	73.2	74.1	74.2
12	75.1	75.2	76.1
11	76.2	77.1	77.2
10	78.1	78.2	79.1
9	79.2	80.1	80.2
8	81.1	81.2	82.1
7	82.2	83.1	83.2
6	84.1	84.2	85.1
5	85.2	86.1	86.2
4	87.1	87.2	88.1
3	88.2	GND	GND
2	-	-	-
1	-	GND	TST2

Bank 2

	A	B	C
32	1.3	1.4	2.3
31	2.4	3.3	3.4
30	4.3	4.4	5.3
29	5.4	6.3	6.4
28	7.3	7.4	8.3
27	8.4	9.3	9.4
26	10.3	10.4	11.3
25	11.4	12.3	12.4
24	13.3	13.4	14.3
23	14.4	15.3	15.4
22	16.3	16.4	17.3
21	17.4	18.3	18.4
20	19.3	19.4	20.3
19	20.4	21.3	21.4
18	22.3	22.4	23.3
17	23.4	24.3	24.4
16	25.3	25.4	26.3
15	26.4	27.3	27.4
14	28.3	28.4	29.3
13	29.4	30.3	30.4
12	31.3	31.4	32.3
11	32.4	33.3	33.4
10	34.3	34.4	35.3
9	35.4	36.3	36.4
8	37.3	37.4	38.3
7	38.4	39.3	39.4
6	40.3	40.4	41.3
5	41.4	42.3	42.4
4	43.3	43.4	44.3
3	44.4	GND	GND
2	C1.3	C1.4	-
1	-	SEN 2	-

Bank 4

	A	B	C
32	45.3	45.4	46.3
31	46.4	47.3	47.4
30	48.3	48.4	49.3
29	49.4	50.3	50.4
28	51.3	51.4	52.3
27	52.4	53.3	53.4
26	54.3	54.4	55.3
25	55.4	56.3	56.4
24	57.3	57.4	58.3
23	58.4	59.3	59.4
22	60.3	60.4	61.3
21	61.4	62.3	62.4
20	63.3	63.4	64.3
19	64.4	65.3	65.4
18	66.3	66.4	67.3
17	67.4	68.3	68.4
16	69.3	69.4	70.3
15	70.4	71.3	71.4
14	72.3	72.4	73.3
13	73.4	74.3	74.4
12	75.3	75.4	76.3
11	76.4	77.3	77.4
10	78.3	78.4	79.3
9	79.4	80.3	80.4
8	81.3	81.4	82.3
7	82.4	83.3	83.4
6	84.3	84.4	85.3
5	85.4	86.3	86.4
4	87.3	87.4	88.3
3	88.4	GND	GND
2	-	-	-
1	-	GND	-

Fig 5.8 Pin Out Diagram For Single 88 Channel 4 Pole Mode

Bank 1

	A	B	C
32	1.1	1.2	2.1
31	2.2	3.1	3.2
30	4.1	4.2	5.1
29	5.2	6.1	6.2
28	7.1	7.2	8.1
27	8.2	9.1	9.2
26	10.1	10.2	11.1
25	11.2	12.1	12.2
24	13.1	13.2	14.1
23	14.2	15.1	15.2
22	16.1	16.2	17.1
21	17.2	18.1	18.2
20	19.1	19.2	20.1
19	20.2	21.1	21.2
18	22.1	22.2	23.1
17	23.2	24.1	24.2
16	25.1	25.2	26.1
15	26.2	27.1	27.2
14	28.1	28.2	29.1
13	29.2	30.1	30.2
12	31.1	31.2	32.1
11	32.2	33.1	33.2
10	34.1	34.2	35.1
9	35.2	36.1	36.2
8	37.1	37.2	38.1
7	38.2	39.1	39.2
6	40.1	40.2	41.1
5	41.2	42.1	42.2
4	43.1	43.2	44.1
3	44.2	GND	GND
2	C1.1	C1.2	-
1	-	SEN 1	TST 1

Bank 3

	A	B	C
32	1.5	1.6	2.5
31	2.6	3.5	3.6
30	4.5	4.6	5.5
29	5.6	6.5	6.6
28	7.5	7.6	8.5
27	8.6	9.5	9.6
26	10.5	10.6	11.5
25	11.6	12.5	12.6
24	13.5	13.6	14.5
23	14.6	15.5	15.6
22	16.5	16.6	17.5
21	17.6	18.5	18.6
20	19.5	19.6	20.5
19	20.6	21.5	21.6
18	22.5	22.6	23.5
17	23.6	24.5	24.6
16	25.5	25.6	26.5
15	26.6	27.5	27.6
14	28.5	28.6	29.5
13	29.6	30.5	30.6
12	31.5	31.6	32.5
11	32.6	33.5	33.6
10	34.5	34.6	35.5
9	35.6	36.5	36.6
8	37.5	37.6	38.5
7	38.6	39.5	39.6
6	40.5	40.6	41.5
5	41.6	42.5	42.6
4	43.5	43.6	44.5
3	44.6	GND	GND
2	C1.5	C1.6	-
1	-	GND	TST 2

Bank 2

	A	B	C
32	1.3	1.4	2.3
31	2.4	3.3	3.4
30	4.3	4.4	5.3
29	5.4	6.3	6.4
28	7.3	7.4	8.3
27	8.4	9.3	9.4
26	10.3	10.4	11.3
25	11.4	12.3	12.4
24	13.3	13.4	14.3
23	14.4	15.3	15.4
22	16.3	16.4	17.3
21	17.4	18.3	18.4
20	19.3	19.4	20.3
19	20.4	21.3	21.4
18	22.3	22.4	23.3
17	23.4	24.3	24.4
16	25.3	25.4	26.3
15	26.4	27.3	27.4
14	28.3	28.4	29.3
13	29.4	30.3	30.4
12	31.3	31.4	32.3
11	32.4	33.3	33.4
10	34.3	34.4	35.3
9	35.4	36.3	36.4
8	37.3	37.4	38.3
7	38.4	39.3	39.4
6	40.3	40.4	41.3
5	41.4	42.3	42.4
4	43.3	43.4	44.3
3	44.4	GND	GND
2	C1.3	C1.4	-
1	-	SEN 2	-

Bank 4

	A	B	C
32	1.7	1.8	2.7
31	2.8	3.7	3.8
30	4.7	4.8	5.7
29	5.8	6.7	6.8
28	7.7	7.8	8.7
27	8.8	9.7	9.8
26	10.7	10.8	11.7
25	11.8	12.7	12.8
24	13.7	13.8	14.7
23	14.8	15.7	15.8
22	16.7	16.8	17.7
21	17.8	18.7	18.8
20	19.7	19.8	20.7
19	20.8	21.7	21.8
18	22.7	22.8	23.7
17	23.8	24.7	24.8
16	25.7	25.8	26.7
15	26.8	27.7	27.8
14	28.7	28.8	29.7
13	29.8	30.7	30.8
12	31.7	31.8	32.7
11	32.8	33.7	33.8
10	34.7	34.8	35.7
9	35.8	36.7	36.8
8	37.7	37.8	38.7
7	38.8	39.7	39.8
6	40.7	40.8	41.7
5	41.8	42.7	42.8
4	43.7	43.8	44.7
3	44.8	GND	GND
2	C1.7	C1.8	-
1	-	GND	-

Fig 5.9 Pin Out Diagram For Single 44 Channel 8 Pole Mode

The following pin out diagrams for the 20-610-021 high density multiplexer are Included:-

Quad	44 Channel	1 Pole Switching
Dual	88 Channel	1 Pole Switching
Dual	44 Channel	2 Pole Switching
Single	176 Channel	1 Pole Switching
Single	88 Channel	2 Pole Switching
Single	44 Channel	4 Pole Switching

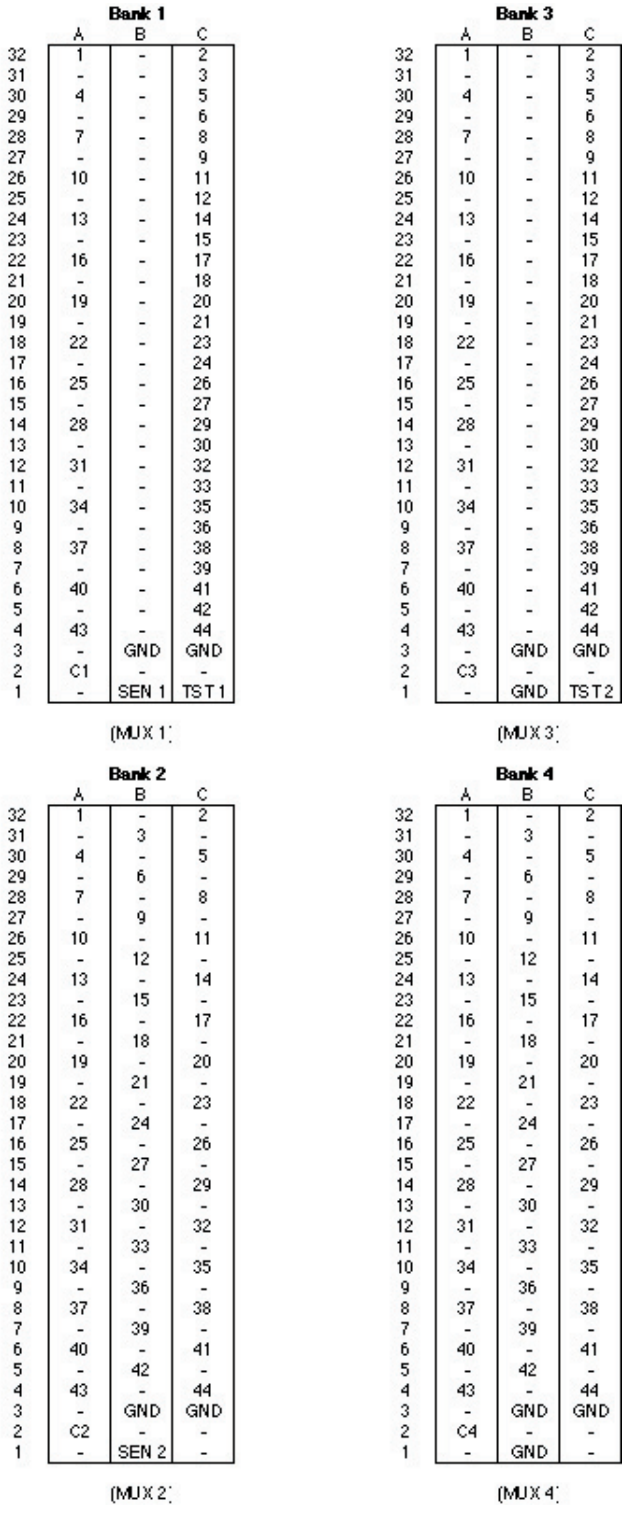


Fig 5.10 Pin Out Diagram For Quad 44 Channel 1 Pole Mode

Bank 1

	A	B	C
32	1	-	2
31	-	-	3
30	4	-	5
29	-	-	6
28	7	-	8
27	-	-	9
26	10	-	11
25	-	-	12
24	13	-	14
23	-	-	15
22	16	-	17
21	-	-	18
20	19	-	20
19	-	-	21
18	22	-	23
17	-	-	24
16	25	-	26
15	-	-	27
14	28	-	29
13	-	-	30
12	31	-	32
11	-	-	33
10	34	-	35
9	-	-	36
8	37	-	38
7	-	-	39
6	40	-	41
5	-	-	42
4	43	-	44
3	-	GND	GND
2	C1	-	-
1	-	SEN 1	TST 1

(MUX 1)

Bank 3

	A	B	C
32	1	-	2
31	-	-	3
30	4	-	5
29	-	-	6
28	7	-	8
27	-	-	9
26	10	-	11
25	-	-	12
24	13	-	14
23	-	-	15
22	16	-	17
21	-	-	18
20	19	-	20
19	-	-	21
18	22	-	23
17	-	-	24
16	25	-	26
15	-	-	27
14	28	-	29
13	-	-	30
12	31	-	32
11	-	-	33
10	34	-	35
9	-	-	36
8	37	-	38
7	-	-	39
6	40	-	41
5	-	-	42
4	43	-	44
3	-	GND	GND
2	C2	-	-
1	-	GND	TST 2

(MUX 2)

Bank 2

	A	B	C
32	45	-	46
31	-	47	-
30	48	-	49
29	-	50	-
28	51	-	52
27	-	53	-
26	54	-	55
25	-	56	-
24	57	-	58
23	-	59	-
22	60	-	61
21	-	62	-
20	63	-	64
19	-	65	-
18	66	-	67
17	-	68	-
16	69	-	70
15	-	71	-
14	72	-	73
13	-	74	-
12	75	-	76
11	-	77	-
10	78	-	79
9	-	80	-
8	81	-	82
7	-	83	-
6	84	-	85
5	-	86	-
4	87	-	88
3	-	GND	GND
2	-	-	-
1	-	SEN 2	-

(MUX 1)

Bank 4

	A	B	C
32	45	-	46
31	-	47	-
30	48	-	49
29	-	50	-
28	51	-	52
27	-	53	-
26	54	-	55
25	-	56	-
24	57	-	58
23	-	59	-
22	60	-	61
21	-	62	-
20	63	-	64
19	-	65	-
18	66	-	67
17	-	68	-
16	69	-	70
15	-	71	-
14	72	-	73
13	-	74	-
12	75	-	76
11	-	77	-
10	78	-	79
9	-	80	-
8	81	-	82
7	-	83	-
6	84	-	85
5	-	86	-
4	87	-	88
3	-	GND	GND
2	-	-	-
1	-	GND	-

(MUX 2)

Fig 5.11 Pin Out Diagram For Dual 88 Channel 1 Pole Mode

Bank 1

	A	B	C
32	1.1	-	2.1
31	-	-	3.1
30	4.1	-	5.1
29	-	-	6.1
28	7.1	-	8.1
27	-	-	9.1
26	10.1	-	11.1
25	-	-	12.1
24	13.1	-	14.1
23	-	-	15.1
22	16.1	-	17.1
21	-	-	18.1
20	19.1	-	20.1
19	-	-	21.1
18	22.1	-	23.1
17	-	-	24.1
16	25.1	-	26.1
15	-	-	27.1
14	28.1	-	29.1
13	-	-	30.1
12	31.1	-	32.1
11	-	-	33.1
10	34.1	-	35.1
9	-	-	36.1
8	37.1	-	38.1
7	-	-	39.1
6	40.1	-	41.1
5	-	-	42.1
4	43.1	-	44.1
3	-	GND	GND
2	C1.1	-	-
1	-	SEN 1	TST 1

(MUX 1)

Bank 3

	A	B	C
32	1.1	-	2.1
31	-	-	3.1
30	4.1	-	5.1
29	-	-	6.1
28	7.1	-	8.1
27	-	-	9.1
26	10.1	-	11.1
25	-	-	12.1
24	13.1	-	14.1
23	-	-	15.1
22	16.1	-	17.1
21	-	-	18.1
20	19.1	-	20.1
19	-	-	21.1
18	22.1	-	23.1
17	-	-	24.1
16	25.1	-	26.1
15	-	-	27.1
14	28.1	-	29.1
13	-	-	30.1
12	31.1	-	32.1
11	-	-	33.1
10	34.1	-	35.1
9	-	-	36.1
8	37.1	-	38.1
7	-	-	39.1
6	40.1	-	41.1
5	-	-	42.1
4	43.1	-	44.1
3	-	GND	GND
2	C2.1	-	-
1	-	GND	TST 2

(MUX 2)

Bank 2

	A	B	C
32	1.2	-	2.2
31	-	3.2	-
30	4.2	-	5.2
29	-	6.2	-
28	7.2	-	8.2
27	-	9.2	-
26	10.2	-	11.2
25	-	12.2	-
24	13.2	-	14.2
23	-	15.2	-
22	16.2	-	17.2
21	-	18.2	-
20	19.2	-	20.2
19	-	21.2	-
18	22.2	-	23.2
17	-	24.2	-
16	25.2	-	26.2
15	-	27.2	-
14	28.2	-	29.2
13	-	30.2	-
12	31.2	-	32.2
11	-	33.2	-
10	34.2	-	35.2
9	-	36.2	-
8	37.2	-	38.2
7	-	39.2	-
6	40.2	-	41.2
5	-	42.2	-
4	43.2	-	44.2
3	-	GND	GND
2	C1.2	-	-
1	-	SEN 2	-

(MUX 1)

Bank 4

	A	B	C
32	1.2	-	2.2
31	-	3.2	-
30	4.2	-	5.2
29	-	6.2	-
28	7.2	-	8.2
27	-	9.2	-
26	10.2	-	11.2
25	-	12.2	-
24	13.2	-	14.2
23	-	15.2	-
22	16.2	-	17.2
21	-	18.2	-
20	19.2	-	20.2
19	-	21.2	-
18	22.2	-	23.2
17	-	24.2	-
16	25.2	-	26.2
15	-	27.2	-
14	28.2	-	29.2
13	-	30.2	-
12	31.2	-	32.2
11	-	33.2	-
10	34.2	-	35.2
9	-	36.2	-
8	37.2	-	38.2
7	-	39.2	-
6	40.2	-	41.2
5	-	42.2	-
4	43.2	-	44.2
3	-	GND	GND
2	C2.2	-	-
1	-	GND	-

(MUX 2)

Fig 5.12 Pin Out Diagram For Dual 44 Channel 2 Pole Mode

Bank 1

	A	B	C
32	1	-	2
31	-	-	3
30	4	-	5
29	-	-	6
28	7	-	8
27	-	-	9
26	10	-	11
25	-	-	12
24	13	-	14
23	-	-	15
22	16	-	17
21	-	-	18
20	19	-	20
19	-	-	21
18	22	-	23
17	-	-	24
16	25	-	26
15	-	-	27
14	28	-	29
13	-	-	30
12	31	-	32
11	-	-	33
10	34	-	35
9	-	-	36
8	37	-	38
7	-	-	39
6	40	-	41
5	-	-	42
4	43	-	44
3	-	GND	GND
2	C1	-	-
1	-	SEN 1	TST 1

Bank 3

	A	B	C
32	89	-	90
31	-	-	91
30	92	-	93
29	-	-	94
28	95	-	96
27	-	-	97
26	98	-	99
25	-	-	100
24	101	-	102
23	-	-	103
22	104	-	105
21	-	-	106
20	107	-	108
19	-	-	109
18	110	-	111
17	-	-	112
16	113	-	114
15	-	-	115
14	116	-	117
13	-	-	118
12	119	-	120
11	-	-	121
10	122	-	123
9	-	-	124
8	125	-	126
7	-	-	127
6	128	-	129
5	-	-	130
4	131	-	132
3	-	GND	GND
2	-	-	-
1	-	GND	TST 2

Bank 2

	A	B	C
32	45	-	46
31	-	47	-
30	48	-	49
29	-	50	-
28	51	-	52
27	-	53	-
26	54	-	55
25	-	56	-
24	57	-	58
23	-	59	-
22	60	-	61
21	-	62	-
20	63	-	64
19	-	65	-
18	66	-	67
17	-	68	-
16	69	-	70
15	-	71	-
14	72	-	73
13	-	74	-
12	75	-	76
11	-	77	-
10	78	-	79
9	-	80	-
8	81	-	82
7	-	83	-
6	84	-	85
5	-	86	-
4	87	-	88
3	-	GND	GND
2	-	-	-
1	-	SEN 2	-

Bank 4

	A	B	C
32	133	-	134
31	-	135	-
30	136	-	137
29	-	138	-
28	139	-	140
27	-	141	-
26	142	-	143
25	-	144	-
24	145	-	146
23	-	147	-
22	148	-	149
21	-	150	-
20	151	-	152
19	-	153	-
18	154	-	155
17	-	156	-
16	157	-	158
15	-	159	-
14	160	-	161
13	-	162	-
12	163	-	164
11	-	165	-
10	166	-	167
9	-	168	-
8	169	-	170
7	-	171	-
6	172	-	173
5	-	174	-
4	175	-	176
3	-	GND	GND
2	-	-	-
1	-	GND	-

Fig 5.13 Pin Out Diagram For Single 176 Channel 1 Pole Mode

Bank 1

	A	B	C
32	1.1	-	2.1
31	-	-	3.1
30	4.1	-	5.1
29	-	-	6.1
28	7.1	-	8.1
27	-	-	9.1
26	10.1	-	11.1
25	-	-	12.1
24	13.1	-	14.1
23	-	-	15.1
22	16.1	-	17.1
21	-	-	18.1
20	19.1	-	20.1
19	-	-	21.1
18	22.1	-	23.1
17	-	-	24.1
16	25.1	-	26.1
15	-	-	27.1
14	28.1	-	29.1
13	-	-	30.1
12	31.1	-	32.1
11	-	-	33.1
10	34.1	-	35.1
9	-	-	36.1
8	37.1	-	38.1
7	-	-	39.1
6	40.1	-	41.1
5	-	-	42.1
4	43.1	-	44.1
3	-	GND	GND
2	C1.1	-	-
1	-	SEN 1	TST 1

Bank 3

	A	B	C
32	45.1	-	46.1
31	-	-	47.1
30	48.1	-	49.1
29	-	-	50.1
28	51.1	-	52.1
27	-	-	53.1
26	54.1	-	55.1
25	-	-	56.1
24	57.1	-	58.1
23	-	-	59.1
22	60.1	-	61.1
21	-	-	62.1
20	63.1	-	64.1
19	-	-	65.1
18	66.1	-	67.1
17	-	-	68.1
16	69.1	-	70.1
15	-	-	71.1
14	72.1	-	73.1
13	-	-	74.1
12	75.1	-	76.1
11	-	-	77.1
10	78.1	-	79.1
9	-	-	80.1
8	81.1	-	82.1
7	-	-	83.1
6	84.1	-	85.1
5	-	-	86.1
4	87.1	-	88.1
3	-	GND	GND
2	-	-	-
1	-	GND	TST 2

Bank 2

	A	B	C
32	1.2	-	2.2
31	-	3.2	-
30	4.2	-	5.2
29	-	6.2	-
28	7.2	-	8.2
27	-	9.2	-
26	10.2	-	11.2
25	-	12.2	-
24	13.2	-	14.2
23	-	15.2	-
22	16.2	-	17.2
21	-	18.2	-
20	19.2	-	20.2
19	-	21.2	-
18	22.2	-	23.2
17	-	24.2	-
16	25.2	-	26.2
15	-	27.2	-
14	28.2	-	29.2
13	-	30.2	-
12	31.2	-	32.2
11	-	33.2	-
10	34.2	-	35.2
9	-	36.2	-
8	37.2	-	38.2
7	-	39.2	-
6	40.2	-	41.2
5	-	42.2	-
4	43.2	-	44.2
3	-	GND	GND
2	C1.2	-	-
1	-	SEN 2	-

Bank 4

	A	B	C
32	45.2	-	46.2
31	-	47.2	-
30	48.2	-	49.2
29	-	50.2	-
28	51.2	-	52.2
27	-	53.2	-
26	54.2	-	55.2
25	-	56.2	-
24	57.2	-	58.2
23	-	59.2	-
22	60.2	-	61.2
21	-	62.2	-
20	63.2	-	64.2
19	-	65.2	-
18	66.2	-	67.2
17	-	68.2	-
16	69.2	-	70.2
15	-	71.2	-
14	72.2	-	73.2
13	-	74.2	-
12	75.2	-	76.2
11	-	77.2	-
10	78.2	-	79.2
9	-	80.2	-
8	81.2	-	82.2
7	-	83.2	-
6	84.2	-	85.2
5	-	86.2	-
4	87.2	-	88.2
3	-	GND	GND
2	-	-	-
1	-	GND	-

Fig 5.14 Pin Out Diagram For Single 88 Channel 2 Pole Mode

(updated 5/97)

Bank 1

	A	B	C
32	1.1	-	2.1
31	-	-	3.1
30	4.1	-	5.1
29	-	-	6.1
28	7.1	-	8.1
27	-	-	9.1
26	10.1	-	11.1
25	-	-	12.1
24	13.1	-	14.1
23	-	-	15.1
22	16.1	-	17.1
21	-	-	18.1
20	19.1	-	20.1
19	-	-	21.1
18	22.1	-	23.1
17	-	-	24.1
16	25.1	-	26.1
15	-	-	27.1
14	28.1	-	29.1
13	-	-	30.1
12	31.1	-	32.1
11	-	-	33.1
10	34.1	-	35.1
9	-	-	36.1
8	37.1	-	38.1
7	-	-	39.1
6	40.1	-	41.1
5	-	-	42.1
4	43.1	-	44.1
3	-	GND	GND
2	C1.1	-	-
1	-	SEN 1	TST 1

Bank 3

	A	B	C
32	1.3	-	2.3
31	-	-	3.3
30	4.3	-	5.3
29	-	-	6.3
28	7.3	-	8.3
27	-	-	9.3
26	10.3	-	11.3
25	-	-	12.3
24	13.3	-	14.3
23	-	-	15.3
22	16.3	-	17.3
21	-	-	18.3
20	19.3	-	20.3
19	-	-	21.3
18	22.3	-	23.3
17	-	-	24.3
16	25.3	-	26.3
15	-	-	27.3
14	28.3	-	29.3
13	-	-	30.3
12	31.3	-	32.3
11	-	-	33.3
10	34.3	-	35.3
9	-	-	36.3
8	37.3	-	38.3
7	-	-	39.3
6	40.3	-	41.3
5	-	-	42.3
4	43.3	-	44.3
3	-	GND	GND
2	C1.3	-	-
1	-	GND	TST 2

Bank 2

	A	B	C
32	1.2	-	2.2
31	-	3.2	-
30	4.2	-	5.2
29	-	6.2	-
28	7.2	-	8.2
27	-	9.2	-
26	10.2	-	11.2
25	-	12.2	-
24	13.2	-	14.2
23	-	15.2	-
22	16.2	-	17.2
21	-	18.2	-
20	19.2	-	20.2
19	-	21.2	-
18	22.2	-	23.2
17	-	24.2	-
16	25.2	-	26.2
15	-	27.2	-
14	28.2	-	29.2
13	-	30.2	-
12	31.2	-	32.2
11	-	33.2	-
10	34.2	-	35.2
9	-	36.2	-
8	37.2	-	38.2
7	-	39.2	-
6	40.2	-	41.2
5	-	42.2	-
4	43.2	-	44.2
3	-	GND	GND
2	C1.2	-	-
1	-	SEN 2	-

Bank 4

	A	B	C
32	1.4	-	2.4
31	-	3.4	-
30	4.4	-	5.4
29	-	6.4	-
28	7.4	-	8.4
27	-	9.4	-
26	10.4	-	11.4
25	-	12.4	-
24	13.4	-	14.4
23	-	15.4	-
22	16.4	-	17.4
21	-	18.4	-
20	19.4	-	20.4
19	-	21.4	-
18	22.4	-	23.4
17	-	24.4	-
16	25.4	-	26.4
15	-	27.4	-
14	28.4	-	29.4
13	-	30.4	-
12	31.4	-	32.4
11	-	33.4	-
10	34.4	-	35.4
9	-	36.4	-
8	37.4	-	38.4
7	-	39.4	-
6	40.4	-	41.4
5	-	42.4	-
4	43.4	-	44.4
3	-	GND	GND
2	C1.4	-	-
1	-	GND	-

Fig 5.15 Pin Out Diagram For Single 44 Channel 4 Pole Mode

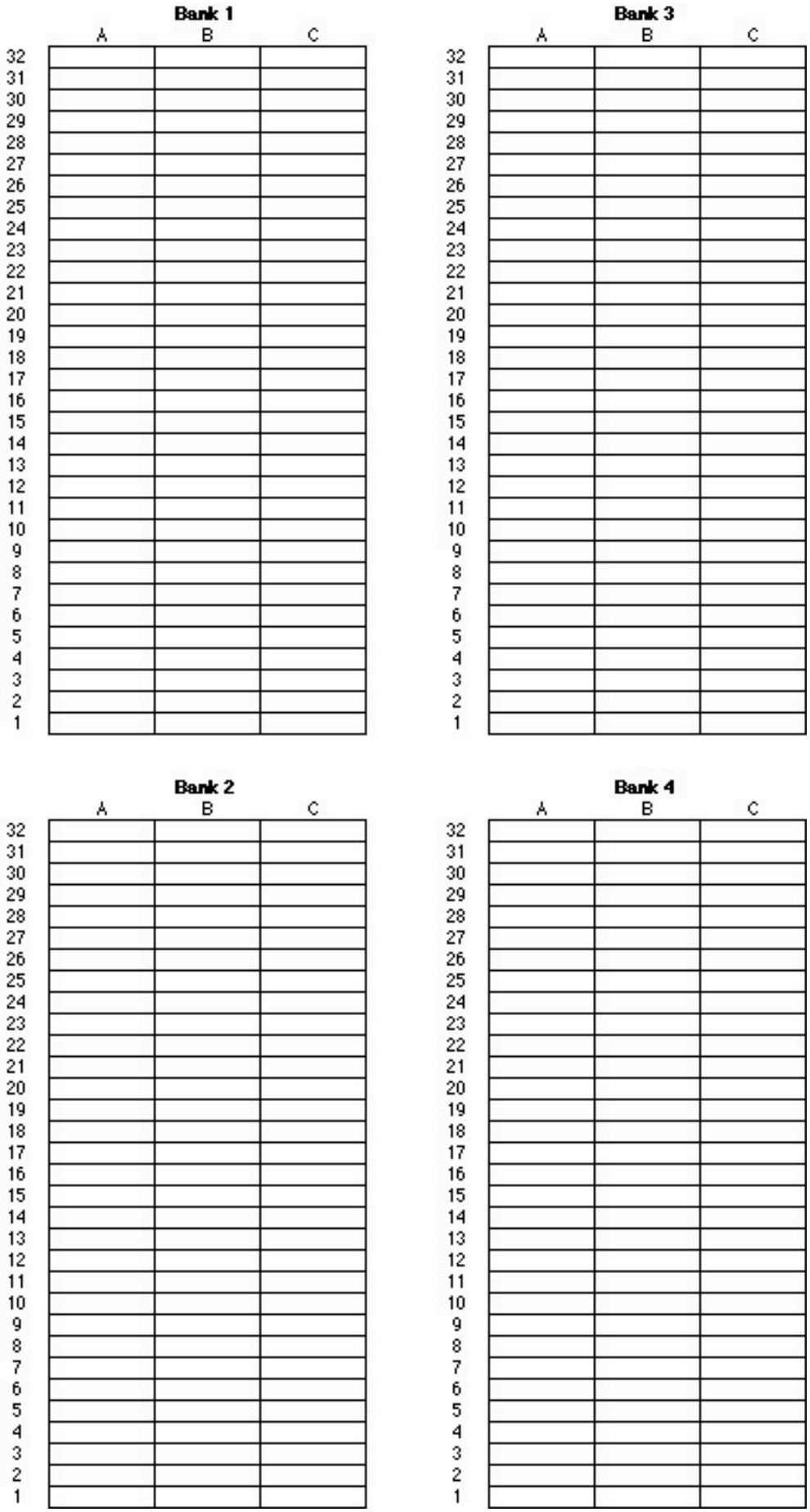


Fig 5.16 Blank Pin Out Diagram

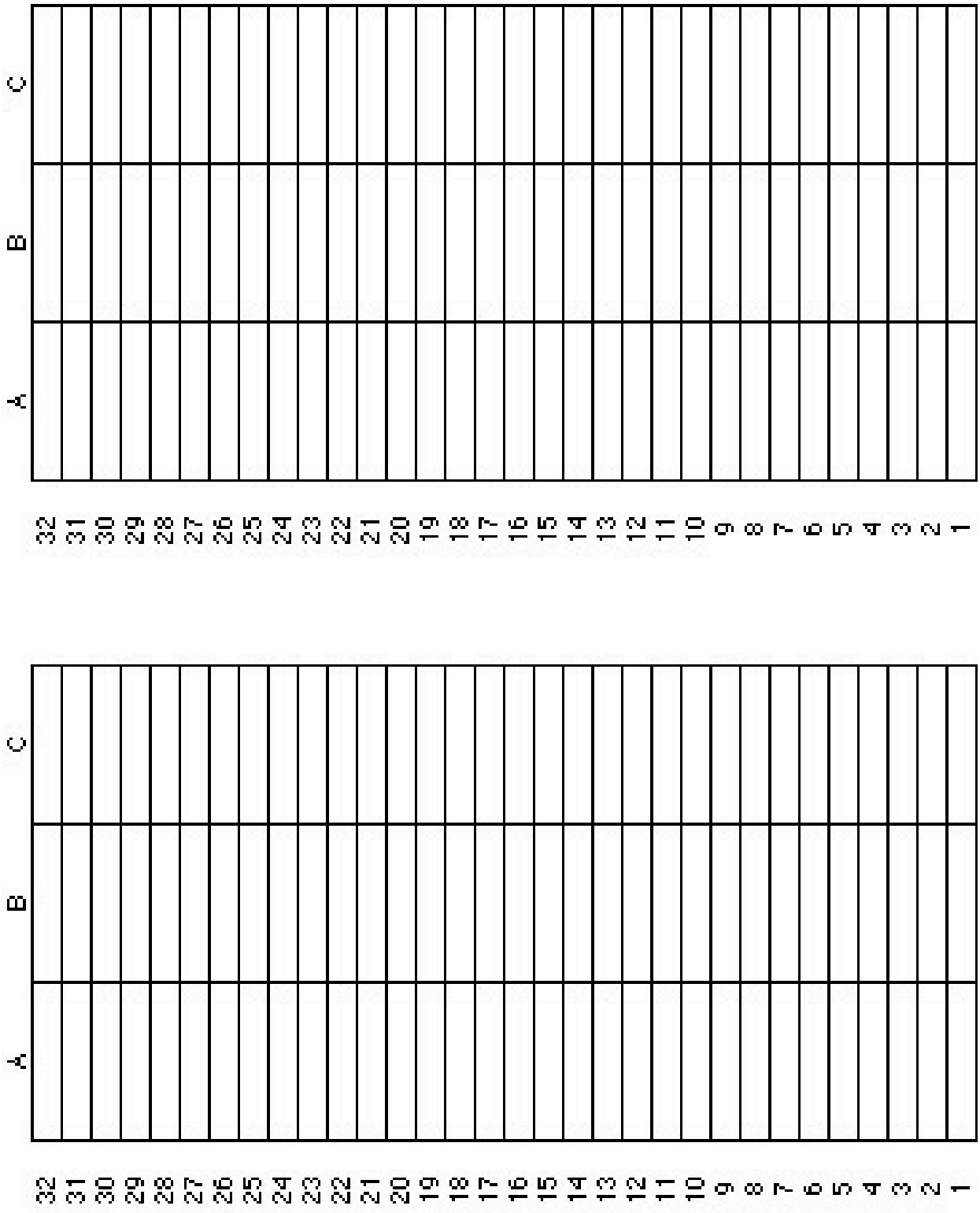
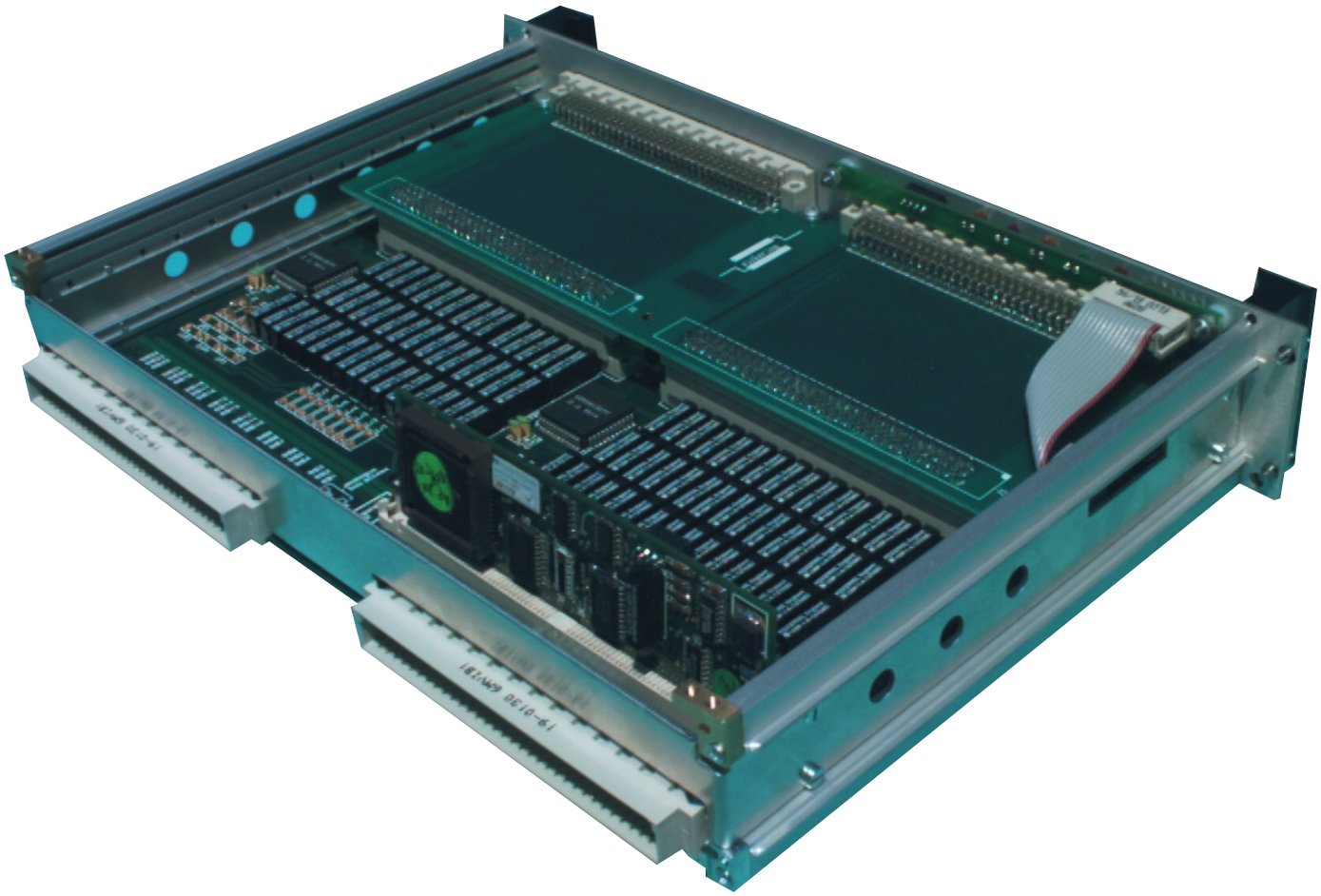


Fig 5.17 Blank Pin Out Diagram



Internal Construction of 20-610 Module

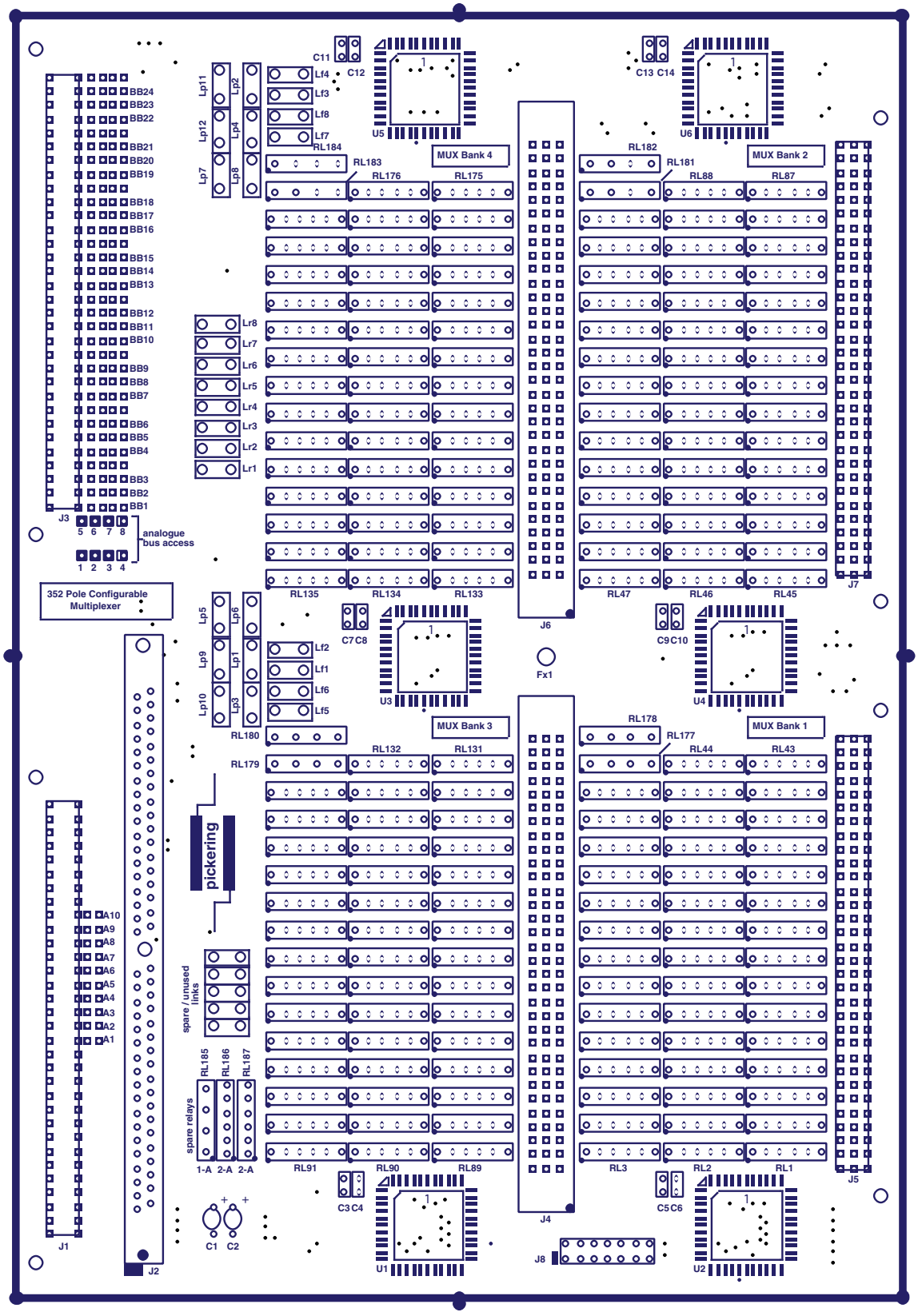


Fig 6.1 20-610 Relay PCB Layout (Top)

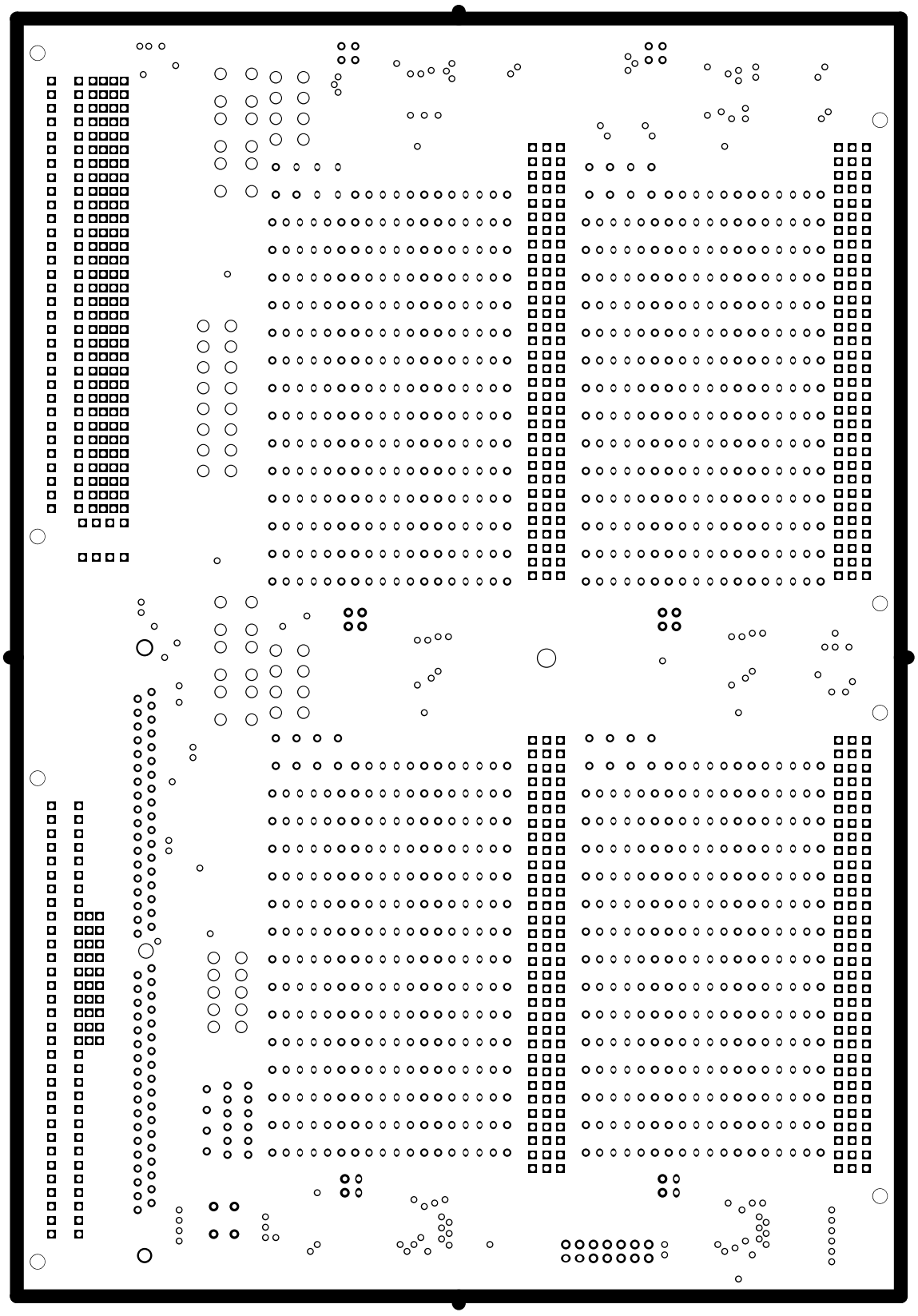


Fig 6.2 20-610 Relay PCB Layout (Bottom)

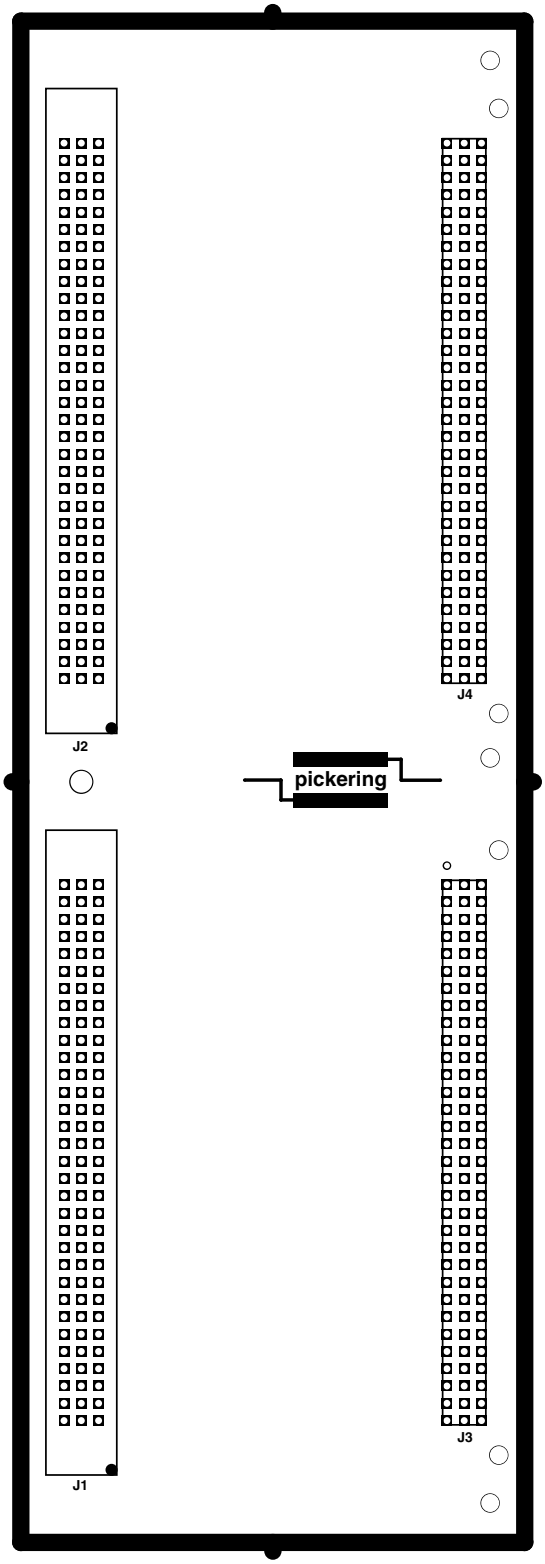


Fig 6.3 20-610 Connection PCB Layout (Top)

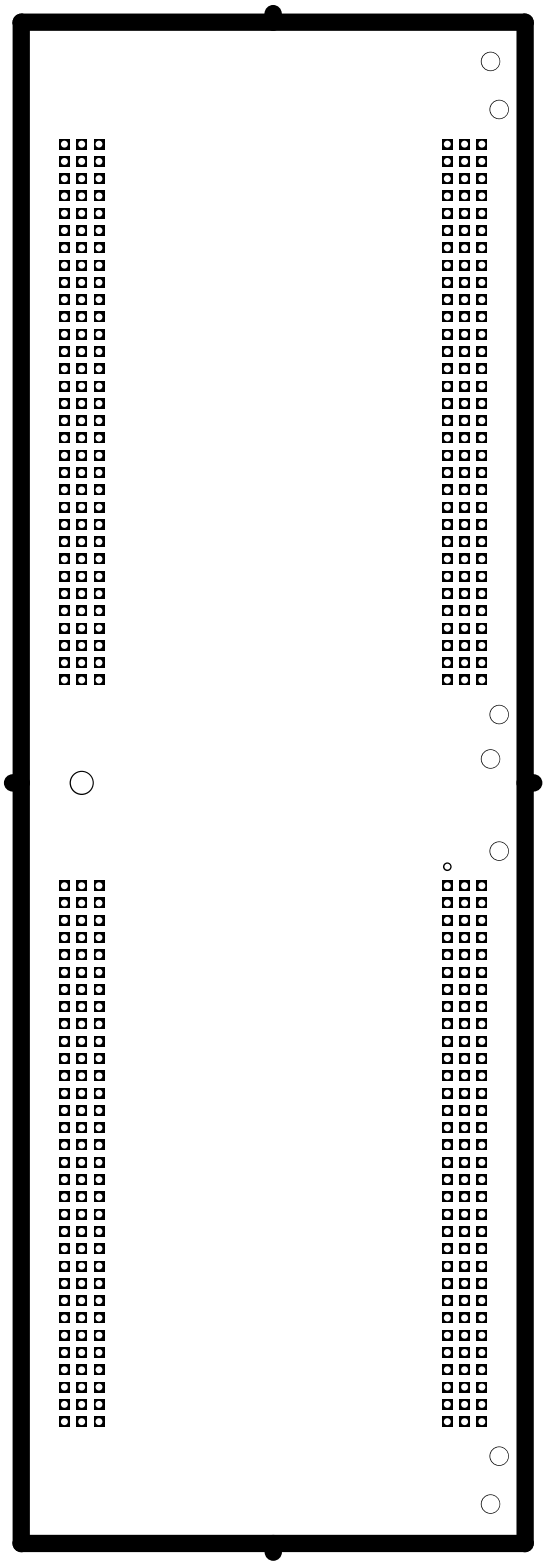


Fig 6.4 20-610 Connection PCB Layout (Bottom)

PCB location	PIL part number	Part description	Qty
C1	C/CP/003	Cap Tant 22uF 16V	omit
C2	C/CP/003	Cap Tant 22uF 16V	1
C3...C14	C/CP/001	Cap Cer 10nF 63V	12
Fx1	C/FX/130	hex threaded spacer 16mm	1
"	C/FX/085	M3 washer	1
J1,J3	C/CN/001	DIN41612C r/a 64 way plg	2
J2	C/CN/276	SIMM skt 72 way vertical	1
J4,J6	C/CN/285	DIN41612 straight 96 way pcb plg	2
J5,J7	C/CN/254	DIN41612C r/a 96 way plg	2
J8	C/CN/128	14 way mini-DIP transition	1
"	C/CN/090	14 way IDC skt	1
RL1...RL176,RL186,RL187	C/RL/073	109-2-A-12/2D	178
RL177...RL185	C/RL/056	109-1-A-12/1D	9
U1...U6	C/IC/035	UCN5818EPF 32 bit driver smt	6
config links	C/CN/152	pcb jack skt	66
" "	C/CN/156	link 0.2" uninsulated	9

Table 6.1 GPIB145r0 PCB Parts-List

PCB location	PIL part number	Part description	Qty
J1,J2	C/CN/267	DIN41612 straight 96 way pcb skt	2
J3,J4	C/CN/254	DIN41612C r/a 96 way plg	2

Table 6.2 GPIB147r0 PCB Parts-List

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