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VME PowerPC Board

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Radstone PPC603/603e/604 User Guide

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Table of Contents

Chapter 1 - Introduction

Chapter 2 - General Description

Chapter 3 - Unpacking and Inspection

Chapter 4 - Configuration

Chapter 5 - Connectors

Chapter 6 - Front Panel

Chapter 7 - Installation

Chapter 8 - Power-up and Operational Description

Chapter 9 - Functional Description

Chapter 9 - Functional Description (continued)

Chapter 9 - Functional Description (continued)

Chapter 10 - Troubleshooting

Appendix A - Specifications

Appendix B - POPPPC-20 and POPPPC-21

Chapter 1 - Introduction

Radstone's PPC603, PPC603e and PPC604, with associated peripherals and software, are the first products in Radstone's PowerFull family of VME-based PowerPC boards. They are fully compliant with the PowerPC Reference Platform (PReP) recommendations, ensuring compatibility with the abundance of PReP compliant software. Designed for users who require scalable, high performance processors, sophisticated I/O subsystems and high levels of on-board integration, Radstone's PowerFull products offer a cost-effective solution to a wide range of application requirements.

Based on industry standards, the PPC60x offers a choice of either PowerPC 603, 603e or 604 RISC CPUs, fully harnessing the power and flexibility of the chosen CPU. The PPC604 is fitted with the high-performance PowerPC 604 processor, and is aimed at users who need to solve demanding application requirements. The PPC603 uses the more economical PowerPC 603, and is ideally suited to more cost-sensitive situations. The PPC603e forms the transition between the other two processors, with higher performance than the PPC603, but lower cost than the PPC604.

Local connection of SCSI-2, Ethernet and VME64 uses PCI, as do the IEEE P1386.1 PMC sites. Each board can directly support up to two PMC slots, or up to four PMC sites may be available by using a companion carrier card. PMCs available directly from Radstone include high performance graphics, FDDI, fast Ethernet and MIL-STD-1553B, with a wide range of other PMC types available from other suppliers. Additional I/O for twin serial, parallel, audio, mouse, keyboard etc. is also available

This flexibility, together with operating system support including Windows NT, AIX, VxWorks, LynxOS, Solaris and OS-9, are key factors in making the PPC60x an ideal vehicle for applications such as communications, printing, data routing, simulation, multi-media, real-time acquisition and high performance graphics.

Objectives

This guide provides the user with sufficient information to understand the basic operation of the PPC60x hardware. The on-board firmware and other firmware (e.g. drivers and BSPs) are described in separate guides.

Audience

This guide is written to cover, as far as possible, the range of people who will handle or use the PPC60x, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding, VME and communications. There is a glossary provided at the back of this guide that explains some of the terms used and expands all abbreviations.

Scope

This guide describes all variants of the PPC60x. It does not cover any PMC modules or the carrier card.

Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the PPC60x up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

Chapter 1 (this chapter) - gives a brief introduction, this guide's objectives and audience, the structure, some warnings, conventions and related documentation.

Chapter 2 - is a slightly more detailed, but still general product description.

Chapter 3 - contains unpacking and inspection instructions.

Chapter 4 - describes board configuration.

Chapter 5 - describes the PPC60x's connectors and signals used.

Chapter 6 - describes the PPC60x's front panel.

Chapter 7 - describes installation of the PPC60x in a system.

Chapter 8 - describes power-up and subsequent operation of the PPC60x.

Chapter 9 - is a functional description.

Chapter 10 - gives troubleshooting guidelines.

Appendix A - is a board specification.

Appendix B - describes POPPPC-20 and POPPPC-21, which are I/O modules.

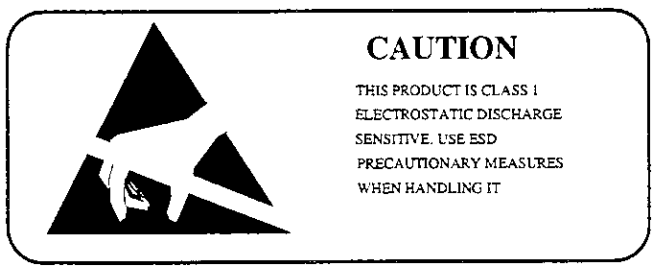
There are also a glossary and an index provided.

Warnings

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, ***toxic fumes*** may be produced due to the destruction of components.

Only use the PPC60x in backplanes that supply power on both the J1 and J2 connectors. Failure to observe this warning may result in damage to the board.

With POPPPC-20 fitted, do *not* connect the G1 (keyboard, mouse and audio) or N1 (Ethernet/10Base5 AUI) connectors to anything other than their intended, marked, interface, as damage to the board may otherwise result. Take care, when connecting Ethernet and Mouse/Keyboard cables, that they are plugged into the correct sockets.



Conventions

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention.

Information of particular importance is in **bold** typeface and is further highlighted by the NOTE box in the outside margin.

NOTE

The multipliers 'k', 'M' and 'G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when 'K', 'M' and 'G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, 'k' 'M' and 'G' mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$ $*2^{20}$ and $*2^{30}$.

NOTE

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and VMEbus terminology follows the more familiar convention that bit 0 is the LSB and bit n is the MSB.

Signal names ending in with an asterisk (*) denote active low signals; all other signals are active high.

The term PPC60x is used generically to refer to the PPC603 (using the PowerPC 603 processor), the PPC603e (using the PowerPC603e processor) and the PPC604 (using the PowerPC 604 processor). The devices are specifically referenced where necessary.

Related Documents

Due to the complexity of some of the devices used on the PPC60x, you will need to refer to the following documents for more detailed information.

VME64 Specification, ANSI/VITA 1-1994.

PCI Local Bus Specification Revision 2.1 6/95, PCI Special Interest Group.

PCI System Design Guide Rev 1.0 9/93, PCI Special Interest Group.

PowerPC Reference Platform (PReP) Specification, Version 1.0 6/94, IBM.

PowerPC Architecture Books I, II, III and IV, Motorola Inc, IBM.

PowerPC GRACKLE Peripheral Implementation Definition Book IV, Version 2.1, Motorola Inc.

NCR53C810 PCI-SCSI I/O Processor Data manual, NCR 1993.

AM79C970 PCnet-PCI Single-Chip Ethernet Controller for PCI Local Bus, AMD.

DECchip21050 PCI-PCI Bridge Data Sheet, Digital, December 1993.

82378 System I/O Data Book, Intel PCI Components Division, August 1994.

Universe User Manual, Tundra Semiconductor Corp.

IEEE P1386 Draft Standard for a Common Mezzanine Card Family: CMC.

IEEE P1386.1 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC.

AMD Flash Memory Products Data Book, 1994/1995.

Radstone X600 Modules User Guide, publication number RT5060.

CS4231 Audio CODEC Crystal Semiconductor, Victor Corporation.

SMC37C665GT Super I/O, Standard Microsystems Corporation.

Radstone PPC60x Boot Firmware User Guide, publication number RT5057.

Radstone PMC9100 User Guide, publication number RT5062.

Windows NT on Radstone PPC603/604 Installation Guide, publication number RT5063

World Wide Web Sites

Manufacturers of many of the devices used on the PPC60x maintain ftp or world-wide-web sites. Some useful sites are:

http://www.mot.com
Motorola PowerPC data is available through this site.

http://www.chips.ibm.com:80
IBM PowerPC data is available through this site.

http://www.smc.com
Standard Microsystems Corporation.

http://www.tundra.com
Universe chip information is available through this site.

The user manual for the Universe chip is available in Adobe Acrobat .pdf format via:
http://www.newbridge.com/Tundra/Products/Bus/BPI/Univdl.html

Radstone on the world-wide-web is available at:

http://www.radstone.co.uk or http://www.radstone.com

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Chapter 2 - General Description

This chapter contains a general description of the PPC60x. Chapter 9 describes the boards in more detail.

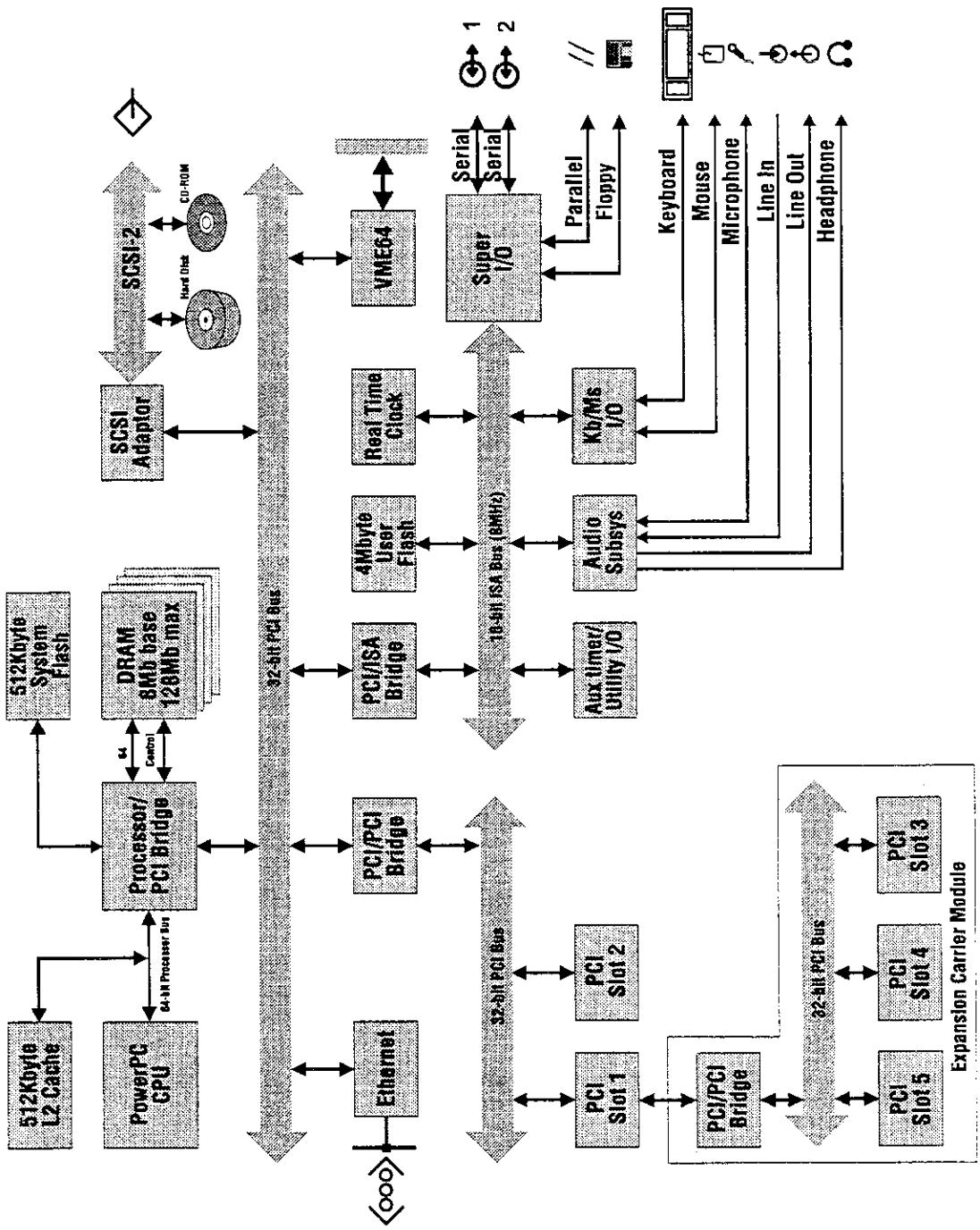
Introduction

The PPC603, PPC603e and PPC604 are highly integrated, PReP compliant VMEbus processors based on the PowerPC 603, 603e and 604 RISC CPUs respectively. All products offer an extensive range of standard functions and expansion options including: processors clocked at 66 or 100 MHz, user memory up to 128 Mbytes with ECC, on-board serial, parallel and Ethernet channels, expansion for a wide range of communications controllers, up to 4 Mbytes of Flash memory, 16-bit business audio, a fast SCSI-2 peripheral interface controller, high-resolution graphics (using a PMC module), a 64-bit VMEbus interface and direct connection for a keyboard and mouse.

On all products, expansion capabilities are provided by up to four PCI interface slots. PCI (PMC - IEEE P1386.1) provides an industry standard, high speed (132 Mbytes/second) local expansion bus, designed for graphics, high-speed communications (e.g. ATM, FDDI, ISDN, etc.), multi-media and user-defined custom functions. PCI has established itself as the leading local interconnect standard, and the wide availability of compatible devices, coupled with its adoption on an array of platforms, ensures that PCI based modules are both high-performance and low cost.

The highly integrated nature of the PPC60x makes it a true single board computer, and allows the VME interface to become an optional feature for appropriate applications. Without VME, the PPC60x still retains the ability to have up to four PMC plug-and-play sites. In many ways, this PPC60x variant resembles a high performance PC motherboard (although in a more rugged, lower profile and more compact form factor). To simplify embedded designs further, an 8-way Berg style connector can be fitted between the P1 and P2 connectors for power transfer, eliminating the need for even a basic backplane. In common with the full VME versions of the PPC60x, all the I/O modules, PMCs and operating systems are 100% compatible. The non-VME option is especially suitable for portable equipment, communication bridges, servers, industrial control, printing and mobile communications applications.

Figure 2-1. PPC60x Block Diagram



Features

- PowerPC 603 at 66 MHz, 603e at 100 MHz or 604 at 100 MHz processor options (**contact your nearest Sales office for details of further speed grades**)
- Extensive operating system support, including Windows NT, AIX, LynxOS, VxWorks and OS-9
- Wide range of shrink-wrapped application software available
- Two PCI/PMC expansion slots on-board, with optional carrier to increase total to four PCI/PMC slots
- Up to 128 Mbytes of DRAM (up to 64 Mbytes on-board) with ECC
- Flash boot ROM up to 1 Mbyte
- Real Time Clock (TOD/calendar) with 8Kx8 of user NOVRAM
- *Standard* features include:
  - On-board PCnet-PCI Ethernet controller
  - SCSI-2 I/O processor,
  - Two RS232 serial I/O channels up to 56 Kbaud,
  - Parallel/printer port with IEEE P1284 extended capabilities,
  - Keyboard/mouse interface,
  - Floppy disk controller,
  - 16-bit business audio
- *Optional* features include:
  - VME64 interface using Universe VMEbus interface chip, plus PCI to VME64 bridge
  - High-resolution graphics (via a PMC slot)
  - Up to 512 Kbytes of secondary cache
  - Up to 4 Mbytes of user Flash ROM
- Single slot 6U VME board
- Range of 3U rear-mounting I/O modules
- PReP compliant design
- ANSI/VITA 1-1994 VME64 compatible

Functional Overview

PReP

The PowerPC Reference Platform is an example implementation of a philosophy designed to allow 100% binary compatibility across different platforms based on the PowerPC processor. Aiming to achieve an open standard, PReP encourages the use of industry standard components and buses, and a wide range of operating systems. As well as providing a detailed hardware design specification, PReP also embodies a software mechanism that allows the hardware to be isolated from the application by abstraction layers. It is these abstraction layers (in effect very low level system drivers) that are the key to differentiation, scalability and future proofing. The operating systems, applications and drivers can 'sit' on these layers without needing to be aware of the underlying hardware (other than general functionality). This is fundamentally different from PCs, which use a BIOS that ultimately constrains operating systems and applications alike.

The PReP approach affords support to everything from low-level systems with PC functionality, up to high performance servers with multiple processors, buses and a wide variety of hardware.

PReP has gained wide-spread industry support, and the PPC60x builds on the PReP example to ensure full compliance. Any application written for any of the boards is therefore binary compatible (even at the driver level) across the range of PReP compliant products from both Radstone and other companies. This provides security for today's valuable software investments, as well as expansion capabilities for the future.

Processor

The PowerPC has become the most widely used of the new generation of RISC processors. Its pedigree is unequalled - jointly developed by world-leading computer companies and backed by long-term commitments from major OEMs.

The PowerPC 603, 603e and 604 are 32-bit superscalar RISC processors featuring a 64-bit external data bus, on-chip instruction and data caches, MMU and integral FPU.

The PowerPC 604 is the higher performance device, clocked at 100 MHz and employing a larger primary cache and enhanced branch prediction capabilities. The PowerPC 603 variant implements a fully static architecture and offers sophisticated power management capabilities. As a result, maximum power consumption is reduced to less than 3 Watts. The PowerePC 603e is a higher performance enhancement of the PowerPC603.

Function	PowerPC 603	PowerPC 603e	PowerPC 604
Clock	66 MHz	100 MHz	100 MHz
Cache	8 Kbytes data 8 Kbytes instruction	16 Kbytes data 16 Kbytes instruction	16 Kbytes data 16 Kbytes instruction
Performance	60 SPECint92 70 SPECfp92	120 SPECint92 135 SPECfp92	160 SPECint92 165 SPECfp92
Maximum power	3 Watts	3 Watts	18 Watts

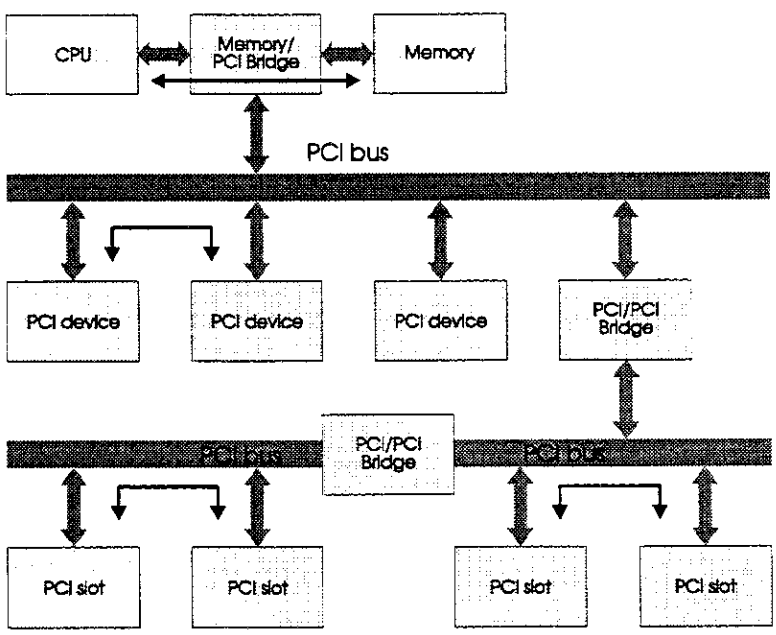
Contact your nearest sales office for details of the availability of 133 MHz 603e and 604 devices.

PCI

PCI has become a highly desirable local interface bus, due to its high bandwidth, glueless interface and low cost. The PPC60x uses PCI to provide a high-speed backbone, both for local interconnect of on-board devices (processor, Ethernet, SCSI-2, ISAbridge and VME64, all of which have direct PCI connectivity), and for communication with optional mezzanine expansion modules (PMCs). A range of PMCs are available from Radstone, including high-performance graphics, multi-channel communications, FDDI and ATM. These all fully comply with the IEEE P1386.1 standard. PCI provides a synchronous 32-bit multiplexed address and data bus (with future expansion capability to 64-bit), allowing burst data transfers to 132 Mbytes/second. The PCI mezzanine format also provides 64 I/O pins for user definition.

Using PCI to PCI bridge devices, the PPC60x can maintain concurrent bus operation. This allows applications using PMCs for routing and communications to operate efficiently in parallel without being blocked.

Figure 2-2. PCI Interconnectivity



PCI Bridge and Memory Controller

The MPC106 PCI bridge and memory controller interfaces the processor to the DRAM and the PCI bus.

PCI Carrier Card

Two PMC slots are provided as standard on the PPC60x. However, boards with greater than 64 Mbytes of DRAM only have one accessible on-board PMC slot, as the other is used by a DRAM mezzanine module providing the extra memory.

For those configurations that require additional PCI functionality, Radstone has developed a PMC Carrier Card that allows an extra three PMC modules to be fitted in an adjacent VMEbus slot. Applications requiring up to four PCI slots can therefore easily be realised. The carrier also uses one of the on-board PMC slots for its direct coupling to the PPC60x's PCI bus. This means that with the carrier card and more than 64 Mbytes of DRAM fitted, both the on-board PMC slots are used, although three PMC slots are still available via the carrier card.

The following table shows the number of PCI slots available with/without the PCC and with/without the DRAM module:

Carrier Card	DRAM Module	PCI Slots Available	VME Slots
Absent	Absent (8 to 64 Mbytes DRAM available)	2	1
	Present (64 to 128 Mbytes DRAM available)	1	1
Present	Absent (8 to 64 Mbytes DRAM available)	4	2
	Present (64 to 128 Mbytes DRAM available)	3	2

Memory

System RAM

Between 8 and 128 Mbytes of system memory is available. Up to 64 Mbytes of DRAM can be fitted directly to the main board using 16 Mbit devices in two banks of 64-bit wide DRAM, controlled by the MPC106 PCI bridge. An additional 64 Mbytes can be added via a mezzanine memory module. All system memory runs contiguously and is dual-ported between the processor and PCI.

The data is protected by Error Correction Coding capable of detecting all single bit, double bit and nibble errors, and correcting single bit errors.

System ROM

System ROM is available as 512 Kbytes or 1 Mbyte of EPROM or Flash. It holds initialisation and operating system boot routines. Two 32-pin PLCC sockets are provided for 4 Mbit Flash ROM devices supporting 5V programming, or EPROMs.

NOVRAM

For maintenance of general system parameters, such as boot options, Ethernet addresses and VME configuration, the 8 Kbytes of on-board NOVRAM provides a convenient, battery-backed storage area.

User Flash ROM

Options of 2 or 4 Mbytes of user Flash ROM supporting on-board programming are available.

Level 2 Cache

Users who may require extra performance can exploit the option of having a secondary cache fitted. The 256 or 512 Kbyte L2 cache is directly connected to the processor bus.

VMEbus Interface

The Newbridge Universe chip provides a full master/slave VMEbus interface. Features include full slot 1 (system controller) functionality, an interrupt handler, an interrupt generator, a DMA controller and support for VME64.

VMEbus slave address decoding is software configurable.

Utility I/O and Auxiliary Function Bus

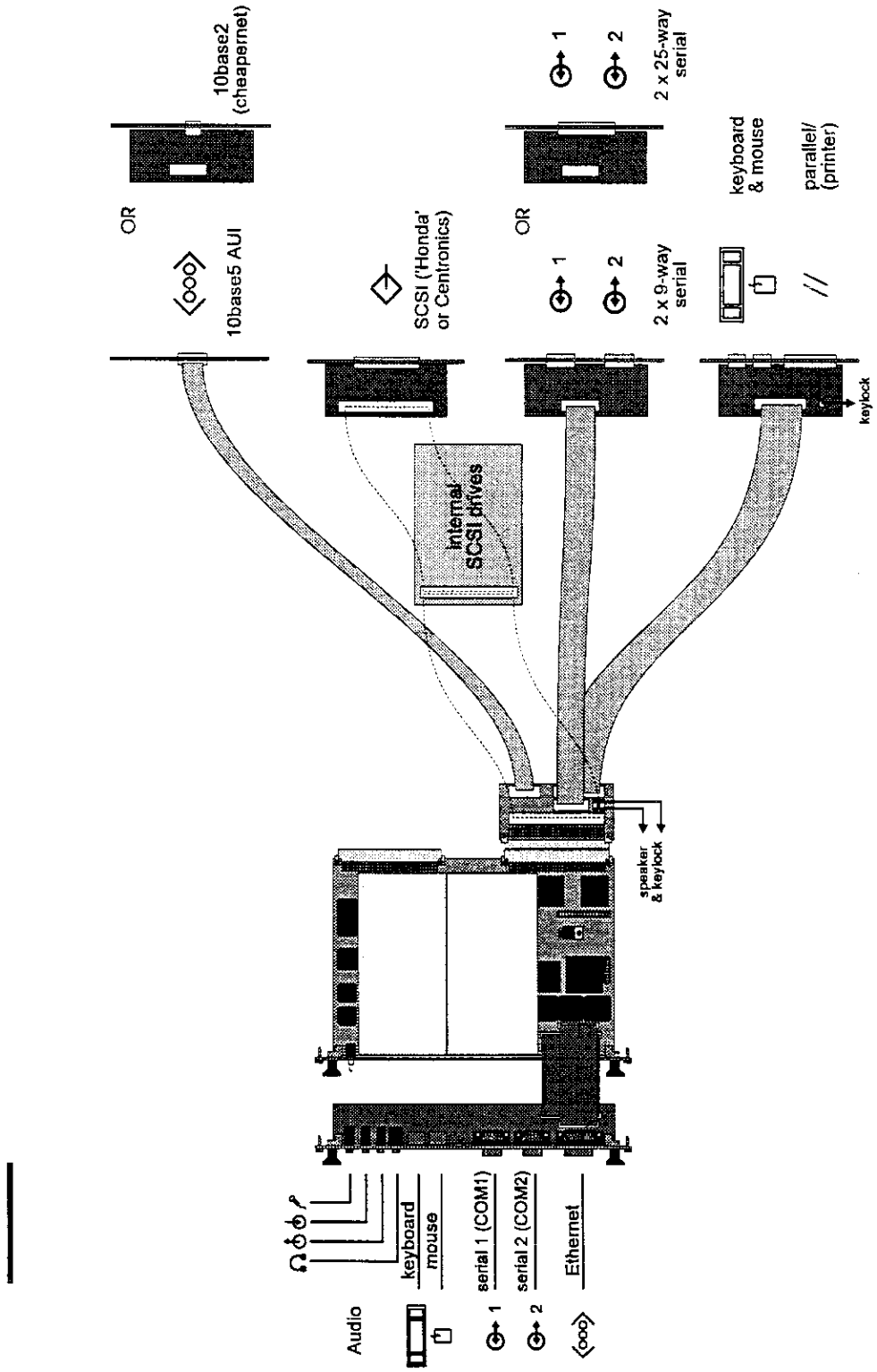
To take full advantage of low-cost, industry standard components, general purpose I/O and auxiliary functions are implemented via an ISA bus interface. Facilities provided include: a parallel/printer port, two PC-compatible serial interfaces, a floppy disk controller, a real-time clock, a keyboard/mouse interface, user Flash memory and 16-bit business audio, which comprises lines in and out, a microphone input and a headphone socket.

Input/Output

The PPC60x has a wide variety of possible I/O connectivity including fast SCSI-2, Ethernet, serial, mouse/keyboard and parallel/printer ports. To allow the greatest freedom and convenience of connecting to these ports, a range of I/O modules are available and are attached by a VME P2 transition module. Using P2 I/O minimises the effort needed to remove boards from a rack, so improving maintainability and reliability.

For those applications that require enhanced front panel connection, while still being able to route other ports (e.g. SCSI) to the rear, an optional 6U auxiliary card can be used. This connects directly to the VME processor card and provides industry standard PS/2 keyboard and mouse ports, stereo audio channels (including a headphone socket), two 9-way PC compatible serial ports and Ethernet.

Figure 2-3. Auxiliary I/O Connection



Operating System Support

PowerPC is one of the few platforms with a wide variety of operating systems ported to it, with more being added all the time. These include Windows NT, Solaris, AIX, LynxOS, VxWorks, OS-9, OS/2, pSOS and System 7.

Windows NT

A 32-bit operating system from Microsoft, Windows NT 4.0 is a pre-emptive, multi-tasking environment available in two distinct versions: Windows NT Server and Windows NT Workstation. The GUI of both is identical, employing the latest Microsoft 'look and feel', as developed for Windows 95.

Both versions include C2-level security features, LAN and peer-to-peer connectivity (including TCP/IP, IPX/SPX, DLC and NetBEUI), remote access service (via X.25 and ISDN) and system management functions (including SNMP and DM2). Also supported are the IBM presentation manager, POSIX 1003.1 and Open GL for 3D graphics applications.

Windows NT Server extends these capabilities further - incorporating RAID and disk mirroring for increased fault tolerance, and support for remote program load allowing diskless client systems to be configured.

Solaris

The Solaris PowerPC edition offers all the functionality of a mature, robust, network computing environment. Multi-threading, multi-processing, TCP/IP networking capabilities and other powerful functionality features in this secure and scalable operating system. Based on Solaris 2.5, the PowerPC edition is feature-for-feature compatible with SPARC and X86/Pentium editions, allowing access to an extensive supply of third party applications and bus/device support, including PCI, ISA and PCMCIA peripherals.

AIX

AIX is IBM's well established UNIX operating system, previously available on machines such as RS/6000. Features include: client support for TCP/IP, NFS, UDP, WABI, X11R5 and Motif. AIX can also support full symmetric multi-processing, and is rich in human centred technology features. Versions of AIX are available with ASCII only interfaces (no GUI) in either server or client only configurations.

VxWorks

A true real-time operating system, Wind River System's VxWorks has been ported to a wide variety of processor types, including x86, 680x0, SPARC and now PowerPC. VxWorks is best described as a deterministic 32-bit operating system with a UNIX-like API. A key feature of VxWorks is its excellent TCP/IP networking support over a wide variety of media including Ethernet, slip, VME-backplanes, and FDDI. In addition, BSD 4.3 sockets, UDP, telnet, ftp, rlogin, rsh, RPC and NFS are all supported.

LynxOS

Created by Lynx, LynxOS is an operating system that has been ported to a wide variety of platforms and is a real-time implementation of UNIX. LynxOS conforms to POSIX 1003.1 and is source code compatible with BSD 4.3 and System V UNIX. It also provides the real-time extensions of POSIX 1003.4, and 'threads' interface of POSIX 1003.4a. LynxOS also supports TCP/IP, NFS, X-Windows and Motif.

OS-9

OS-9 is one of the most common real-time operating systems. Primarily used for industrial control, it is both modular and scalable. This allows systems to be realised in a variety of configurations, from ROMable stand-alone kernels to full blown multi-user development systems. Recent additions to OS-9 now allow it to support sophisticated man-machine interfaces, and to target vertical applications such as multi-media telecommunications and video-on-demand.

OS-9/PowerPC is equipped with a full suite of resident, UNIX and Windows cross development tools, as well as a sophisticated feature set. This includes hierarchical file managers (for hard, floppy and optical disks and RAM); network and file transfer protocols (TCP/IP, UDP/IP, FTP, NFS, RPC, Telnet and BOOTP); priority based, pre-emptive task scheduling; UNIX-like process model and I/O facilities, and extensive interprocess communications.

Chapter 3 - Unpacking and Inspection

This chapter gives guidelines on unpacking and inspecting the PPC60x.

Unpacking

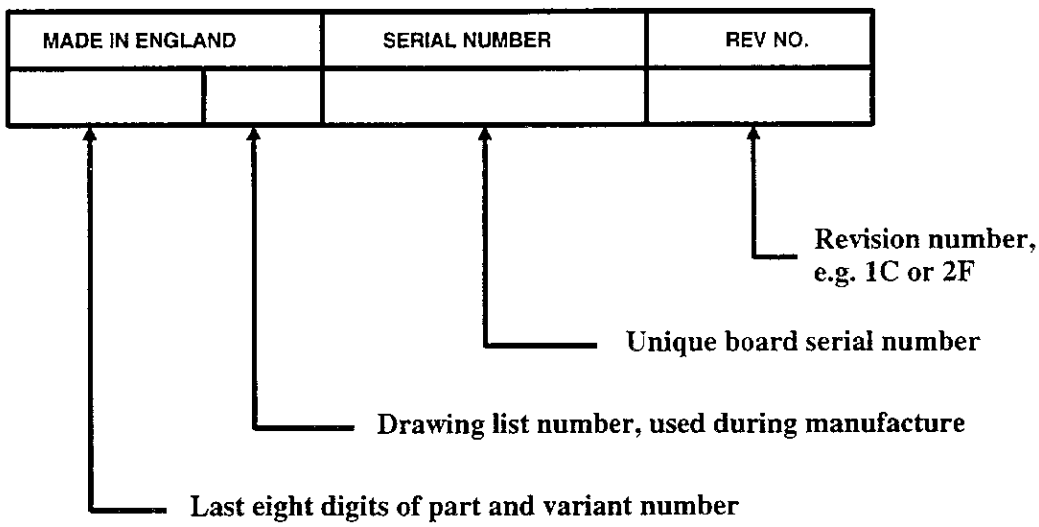
Radstone boards are protected by an antistatic envelope. Observe antistatic precautions and work at an approved antistatic work station when unpacking the board.

The PPC60x is shipped in an individual, reusable shipping box. When you receive the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent is present when the carton is opened. Keep the contents and packing materials for the agent's inspection and notify Radstone's customer service department of the incident. Retain the packing list for reference.

Assuming that there is no obvious damage, you may still want to keep the shipping carton in case you want to ship the PPC60x on elsewhere.

Board Identification

Radstone boards are identified by a label fitted to the P1 connector on the component side of the board. This label gives the revision state of the board, the root code part number (26358 for the PPC60x), the board serial number etc. as shown in the following diagram:



There is also a label on the P2 connector that lists the POPs fitted to the board. See Appendix A for a list of the available POPs.

Inspection

Assuming that the PPC60x is not obviously damaged, you can now go on to inspect it. It is possible for components (connectors, links, socketed chips etc.) to work loose or be dislodged in transit or in the process of unpacking, although this is extremely unlikely. A quick visual inspection should reveal any obviously loose components. Any defects detected should be reported to Radstone.

Now inspect the board for any loose or missing links. The board is delivered with the following default link configuration:

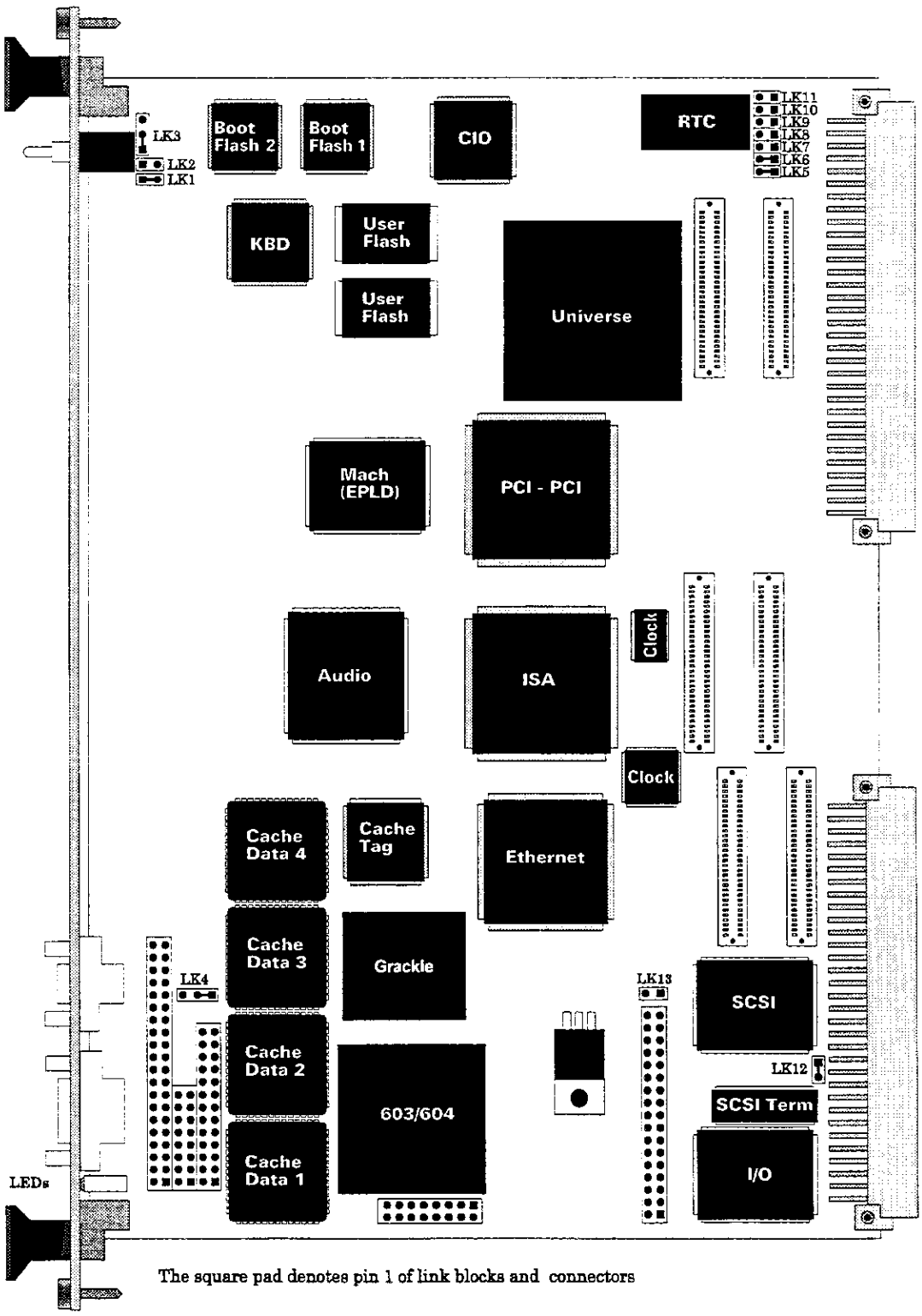
Link	Setting	Action
LK1	In	Machine check exception enabled
LK2	Out	
LK3	Pin 1 to pin 2	Writes to Flash boot ROM enabled
LK4	Pin 1 to pin 2	IEEE 802.3 (10Base5) AUI
LK5	In	Writes to user Flash ROM disabled
LK6	In	Front panel reset switch enabled
LK7	†	Factory test
LK8 to LK11	Out	ID links (board ID = 15)
LK12	In	On-board SCSI terminators enabled
LK13	Out	VME boot disabled

† Depends on the revision state of the PPC60x and the board configuration.

If POPPPC-21 is fitted, link LK4 is not fitted by default. See Appendix B for more details.

The following diagram shows the approximate positions of the links on the board and the default configuration:

Figure 3-1. Default Link Configuration

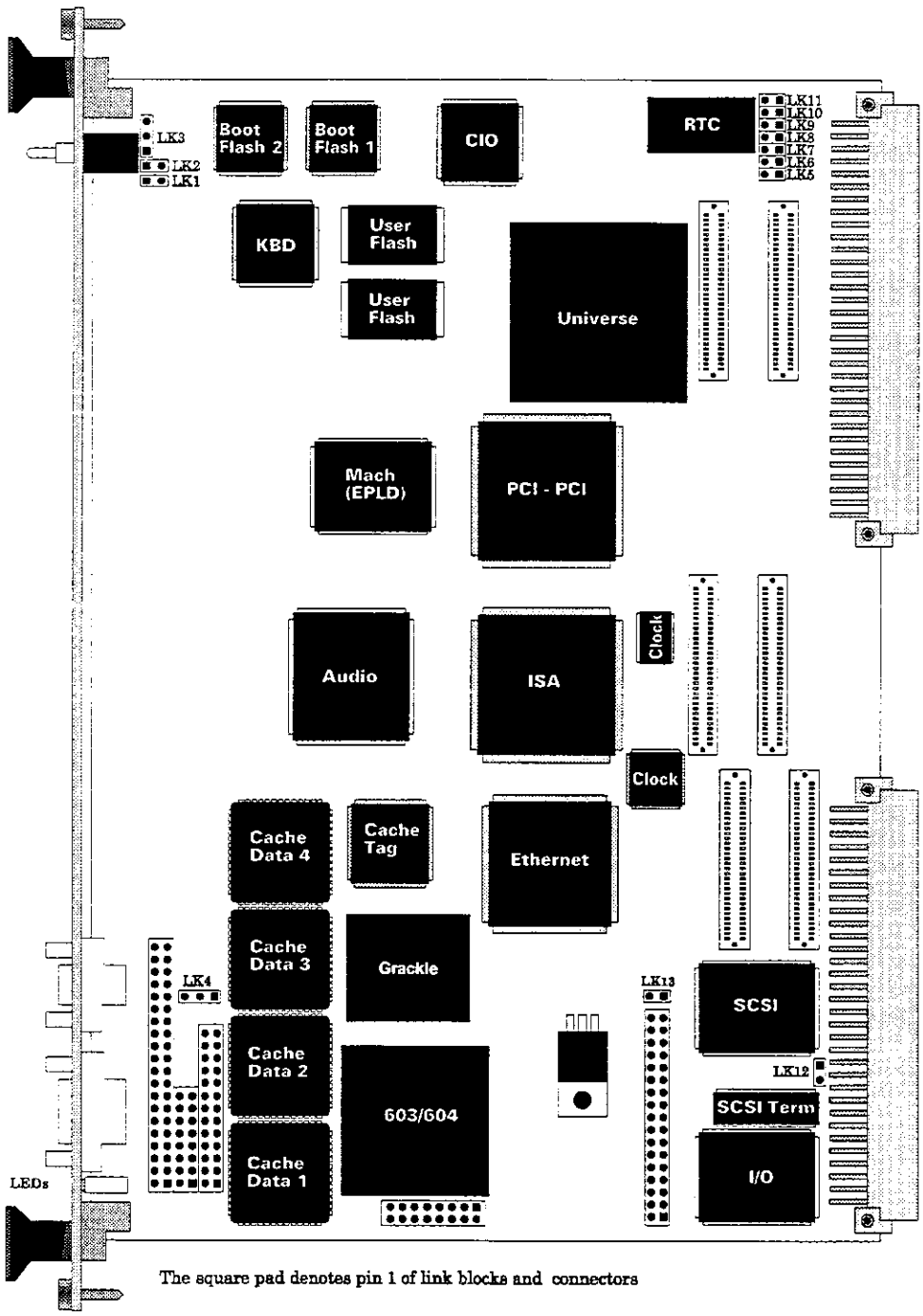


The square pad denotes pin 1 of link blocks and connectors

Chapter 4 - Configuration

This chapter describes the configuration of links on the PPC60x.

Figure 4-1. PPC60x Link Positions



The square pad denotes pin 1 of link blocks and connectors

Machine Check Option Links (LK1 and LK2)

These links determine what action to take when the MPC106 PCI bridge signals a machine check due to a non-recoverable error. The options are to ignore the machine check, request an interrupt on IRQ14 or signal a machine check to the processor. For more details, see the Machine Check Exceptions section in Chapter 9.

NOTE

These links are mutually exclusive and should not both be fitted at the same time.

LK1	LK2	Meaning
Out	Out	Machine Check ignored
Out	In	Machine Check routed to IRQ14
In	Out	Machine Check exception enabled
In	In	**Do *not* fit this combination**

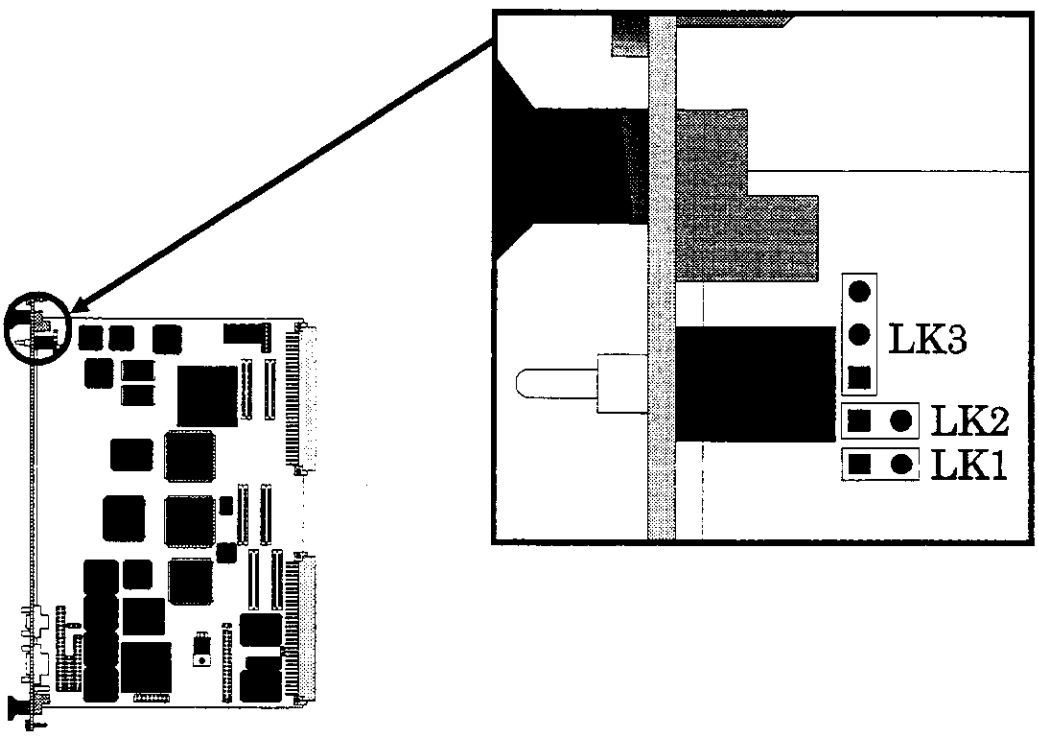
NOTE

The SCSI controller also uses IRQ14.

Flash Boot ROM Write Enable Link (LK3)

This link enables or disables writes to the Flash boot ROM, or configures the bootROM socket to accept EPROM devices.

Fitting	Meaning
Out	Disable writes to the Flash boot ROM
Pin 1 to pin 2	Enable writes to the Flash boot ROM
Pin 2 to pin 3	BootROM socket configured for EPROM



AUI Ground Option Link (LK4)

This link selects the AUI ground option, as follows:

Setting	Meaning
Out	Use L2 setting on POPPPC-21/FPX600†
Pin 1 to pin 2	IEEE 802.3 (10Base5)
Pin 2 to pin 3	Ethernet

† See Appendix B for more details.

User Flash ROM Write Disable Link (LK5)

This link enables or disables writes to the user Flash ROM.

Fitting	Meaning
In	Disable writes to the user Flash ROM
Out	Enable writes to the user Flash ROM

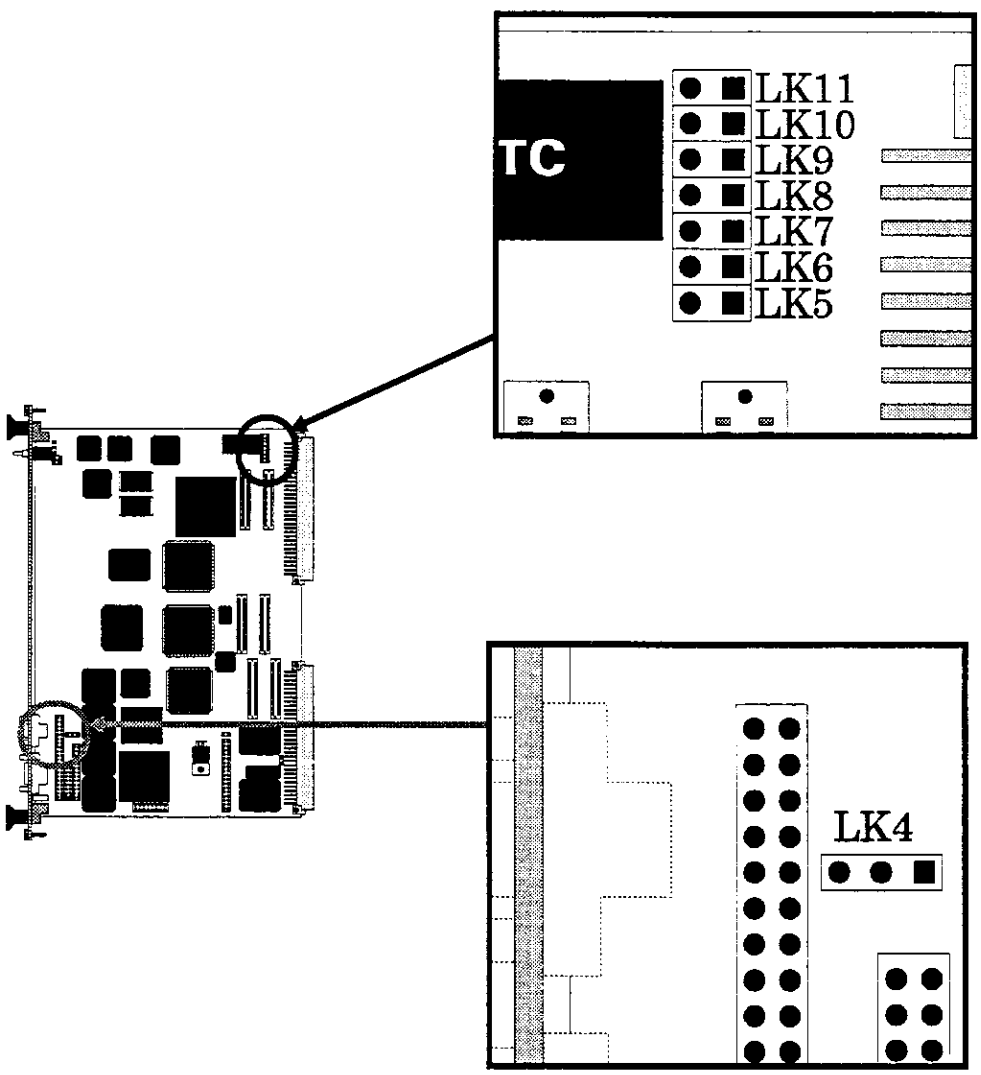
Reset Switch Enable Link (LK6)

This link enables or disables the front panel reset switch.

Fitting	Meaning
In	Enable the front panel reset switch
Out	Disable the front panel reset switch

LK7

Link LK7 is for factory test purposes only. **Do *not* change the setting of this link from that fitted at the factory.**



ID Links (LK8 to LK11)

These links form a 4-bit board ID that may be read from the board ID register (see Chapter 9). The links are decoded as follows:

LK11	LK10	LK9	LK8	Board ID
Out	Out	Out	Out	15
Out	Out	Out	In	14
Out	Out	In	Out	13
Out	Out	In	In	12
Out	In	Out	Out	11
Out	In	Out	In	10
Out	In	In	Out	9
Out	In	In	In	8
In	Out	Out	Out	7
In	Out	Out	In	6
In	Out	In	Out	5
In	Out	In	In	4
In	In	Out	Out	3
In	In	Out	In	2
In	In	In	Out	1
In	In	In	In	0

On-board SCSI Terminator Enable Link (LK12)

This link enables or disables the on-board SCSI terminators.

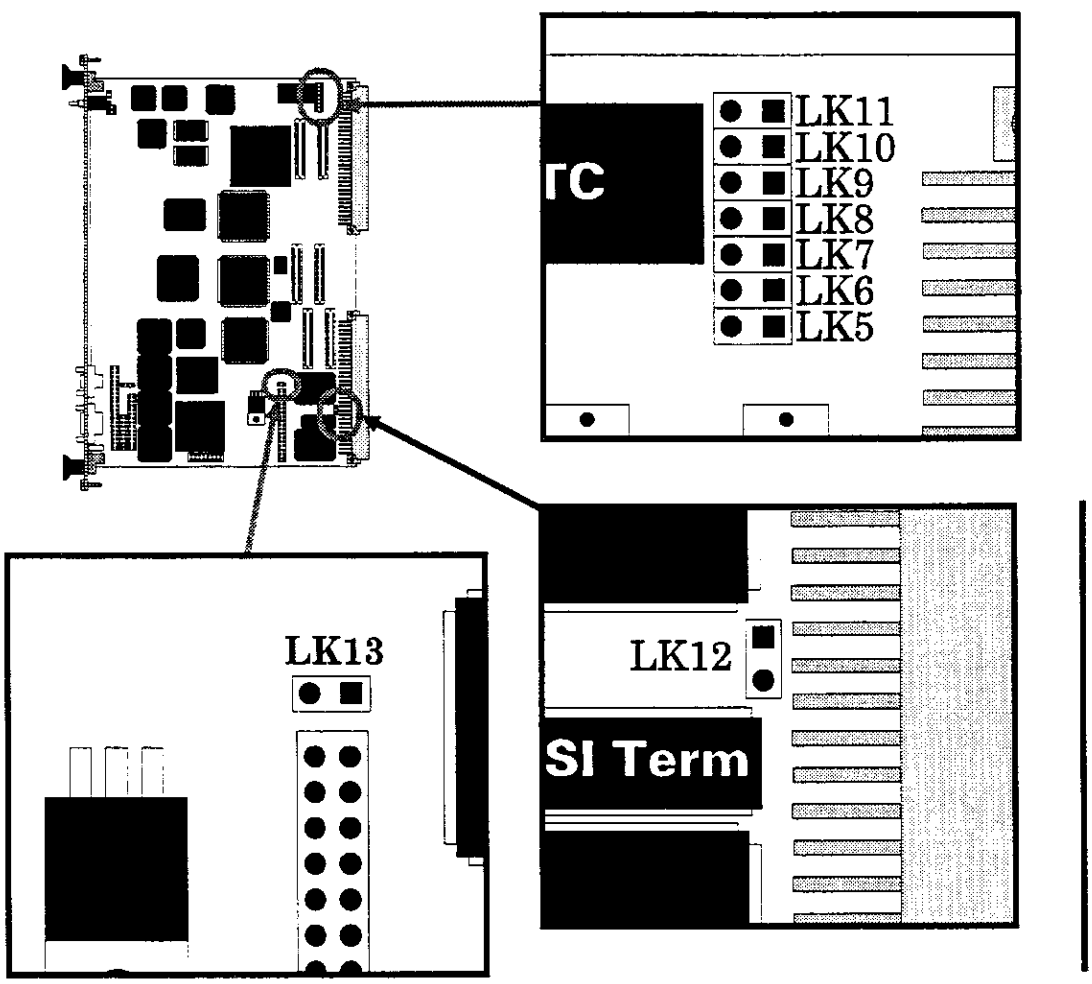
Fitting	Meaning
In	Enable on-board SCSI terminators
Out	Disable on-board SCSI terminators

VME Boot Link (LK13)

This link enables or disables booting of firmware over the VMEbus as follows:

Fitting	Meaning
In	Firmware boot over VME enabled
Out	Firmware boot over VME disabled

Use of this link relies on the default Universe configuration (see the VMEbus Interface Configuration section overleaf).



Default Link Settings

Link	Setting	Action
LK1	In	Machine check exception enabled
LK2	Out	
LK3	Pin 1 to pin 2	Writes to Flash boot ROM enabled
LK4	Pin 1 to pin 2	IEEE 802.3 (10Base5) AUI
LK5	In	Writes to user Flash ROM disabled
LK6	In	Front panel reset switch enabled
LK7	†	Factory test
LK8 to LK11	Out	ID links (board ID = 15)
LK12	In	On-board SCSI terminators enabled
LK13	Out	VME boot disabled

† Depends on the PPC60x's revision state and configuration.

If POPPPC-21 is fitted, link LK4 is not fitted by default. See Appendix B for more details.

VMEbus Interface Configuration

Several operating features of the Universe VME interface are set at power-up or reset by surface mount jumper links. All of these, except local register access, may be overridden by software. The default settings are:

Register access slave image from VMEbus:	Enabled in A32 space at 0x80000000
VME CR/CSR slave image:	Disabled
PCI slave image 0:	Enabled in PCI memory space at 0xF0000000 to 0xFFFFFFFF
Local register access:	PCI I/O space
Auto-ID scheme	Disabled

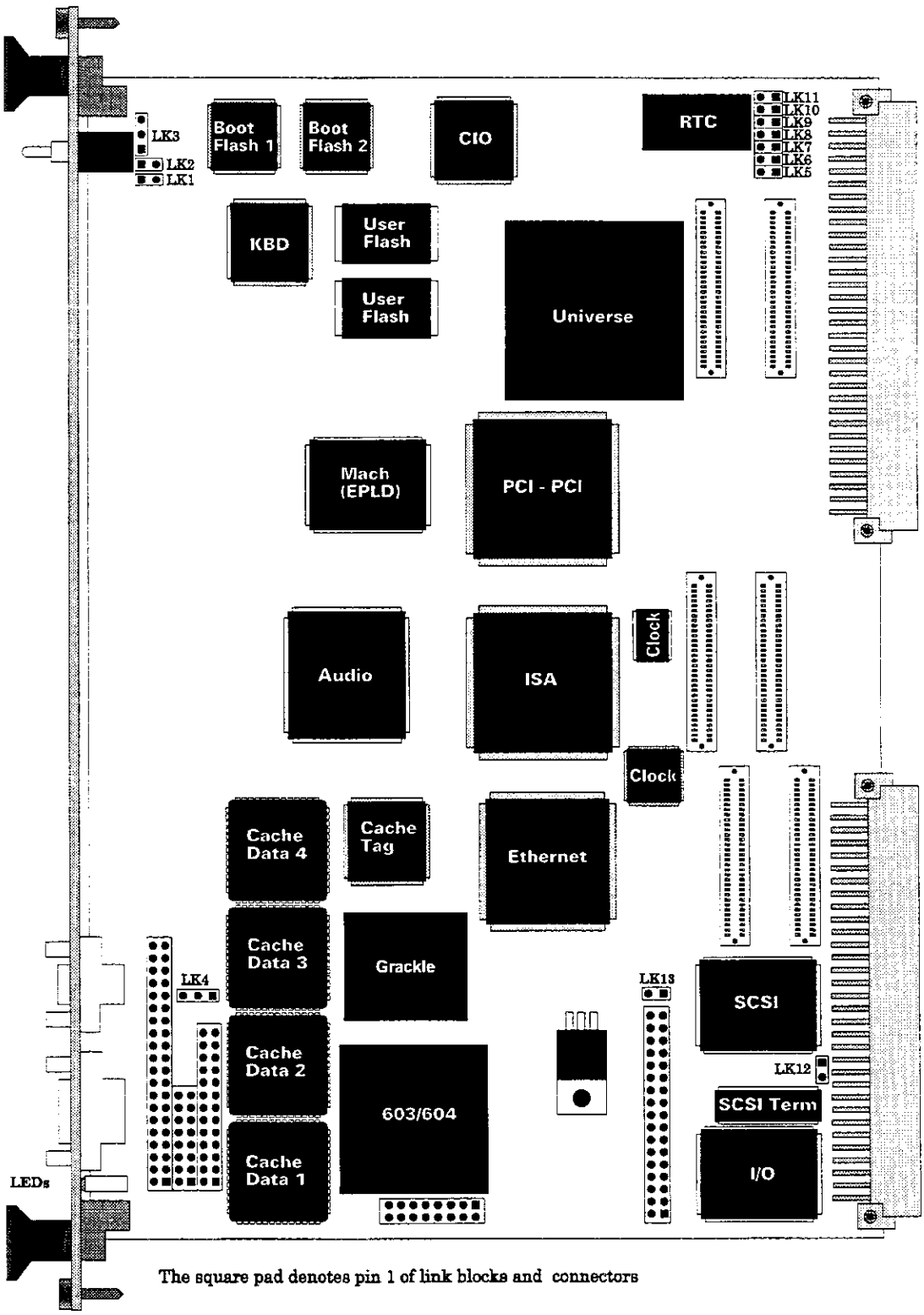
Changing the default power-up options requires surface-mount rework tools and would normally only be done at the factory. Further details are available from technical support at Radstone.

Worksheets

The following table and diagram overleaf are provided for you to record your own configuration, if this differs from the default:

Link	Setting	Action
LK1	In/Out	Machine check ignored Machine check routed to IRQ14 Machine check exception enabled **(Do not fit both LK1 and LK2 together)**
LK2	In/Out	
LK3	Out Pin 1 to pin 2 Pin 2 to pin 3	Writes to Flash boot ROM disabled Writes to Flash boot ROM enabled BootROM socket configured for EPROM
LK4	Out Pin 1 to pin 2 Pin 2 to pin 3	Use L2 setting on POPPPC-21/FPX600 10Base5 Ethernet
LK5	In/Out	Writes to user Flash ROM disabled/enabled
LK6	In/Out	Front panel reset switch enabled/disabled
LK7	Out	Factory test. **Do not change the setting of this link from that fitted at the factory**
LK8	In/Out	ID links Board ID =
LK9	In/Out	
LK10	In/Out	
LK11	In/Out	
LK12	In/Out	On-board SCSI terminators enabled/disabled
LK13	In/Out	Firmware boot over VME enabled/disabled

Delete where not appropriate.

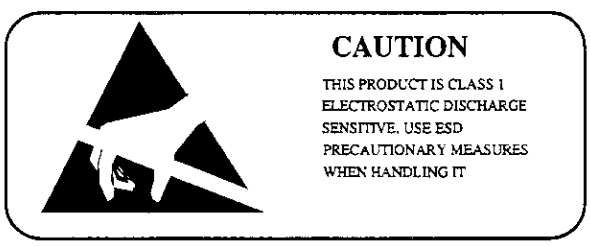


The square pad denotes pin 1 of link blocks and connectors

PMC Installation

Two single width or one double width PMC module may be fitted to the PPC60x as shown in Figure 4-2. If a DRAM mezzanine expansion board or the PMC carrier card is fitted, then only one single width PMC may be installed. If both the DRAM module and the carrier card are fitted, then there are no available PMC slots on-board the PPC60x, although there are still three PMC slots available on the carrier card.

The PPC60x is keyed to accept only 5V PMC modules. A fixing kit is supplied with each PMC module and PMC modules ordered as a POP are supplied already installed. The installation of driver software or other firmware configuration may be required to achieve full functionality of a PMC module. See the individual PMC user's guide for the exact procedure.



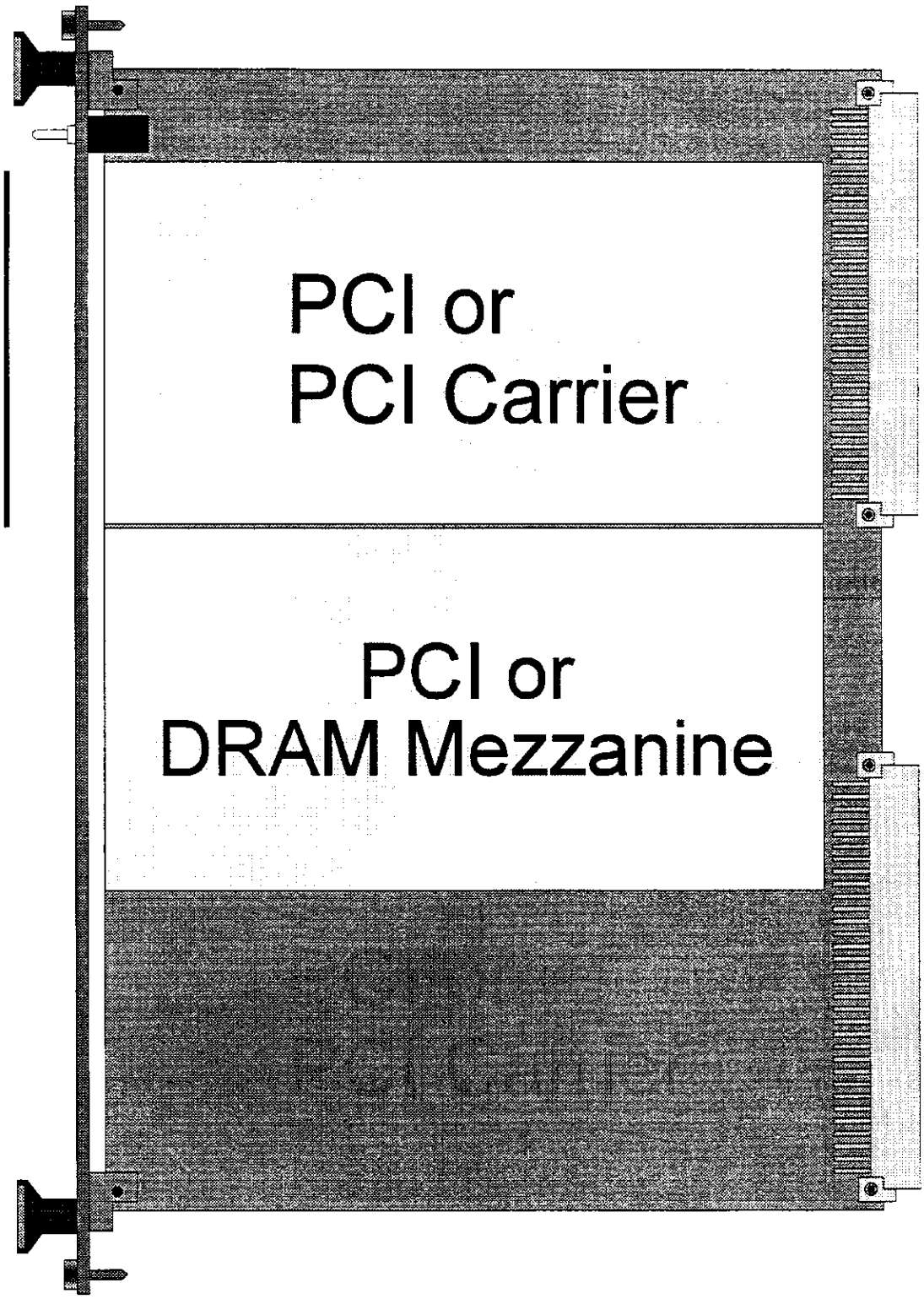
DRAM Mezzanine Installation

The DRAM mezzanine expansion board may be installed in place of one single width PMC slot as shown in Figure 4-2. A DRAM mezzanine board ordered at the same time as the PPC60x will be supplied already installed.

PMC Carrier Card Installation

The PMC carrier card may be installed in place of one single width PMC slot as shown in Figure 4-2. A carrier card ordered at the same time as the PPC60x will be supplied already installed.

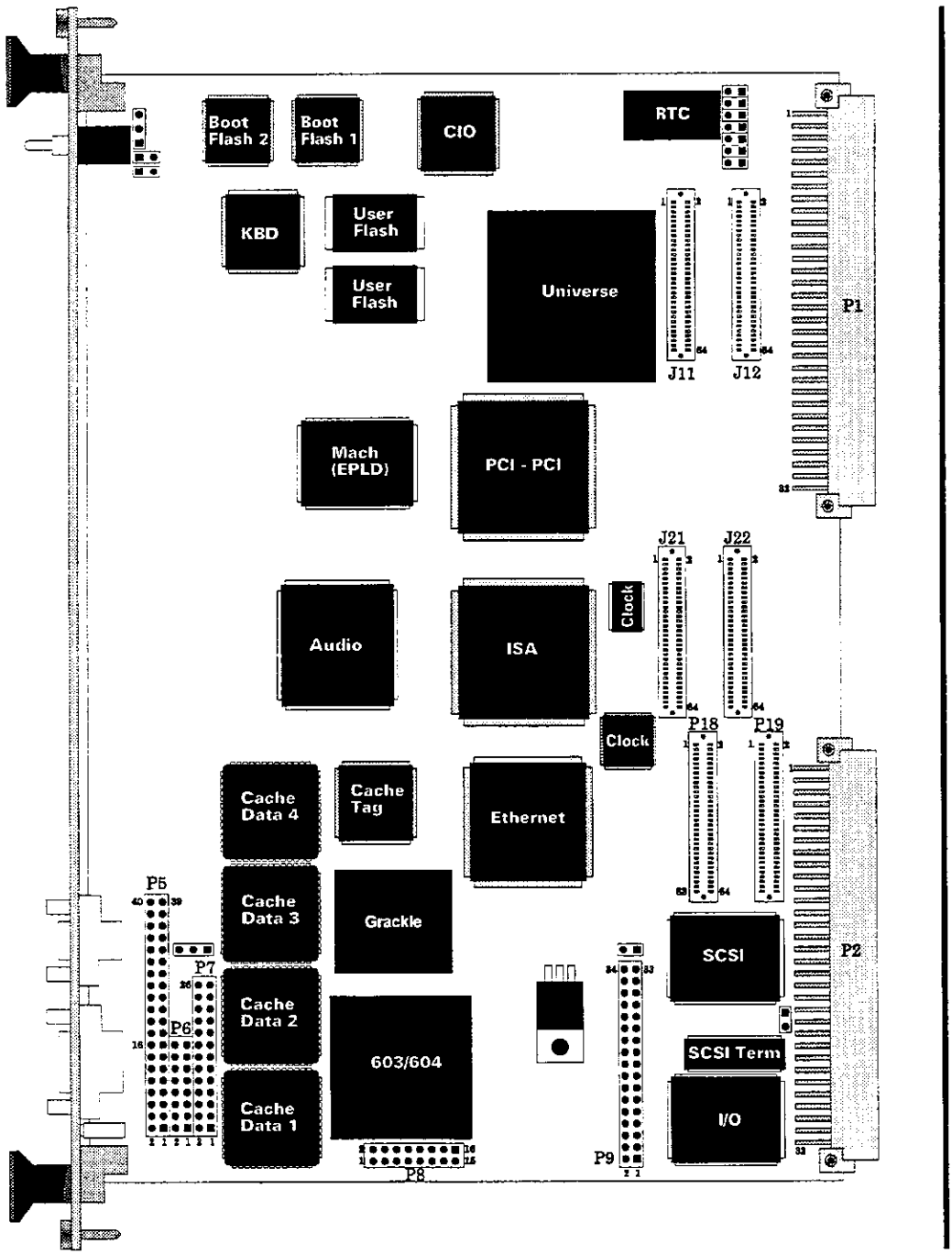
Figure 4-2. PMC Slots and DRAM Mezzanine Locations



Chapter 5 - Connectors

This chapter gives the pinouts and signal descriptions for the connectors on the PPC60x.

Figure 5-1. Connector Positions and Numbering



P1 (VMEbus) Connector Pinout

Pin Number	Row a Signal	Row b Signal	Row c Signal
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	**D03**	**BG0IN***	**D11**
5	**D04**	**BG0OUT***	**D12**
6	**D05**	**BG1IN***	**D13**
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	**SYSCLK**	**BG3IN***	**SYSFAIL***
11	**GND**	**BG3OUT***	**BERR***
12	**DS1***	**BR0***	**SYSRESET***
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	**DTACK***	**AM0**	**A22**
17	**GND**	**AM1**	**A21**
18	**AS***	**AM2**	**A20**
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERA	A17
22	**IACKOUT***	**SERB**	**A16**
23	**AM4**	**GND**	**A15**
24	**A07**	**IRQ7***	**A14**
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	**A03**	**IRQ3***	**A10**
29	**A02**	**IRQ2***	**A09**
30	**A01**	**IRQ1***	**A08**
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

P2 Connector Pinout

Pin Number	Row a Signal	Row b Signal	Row c Signal
1	DB0* (SCSI)	+5V	Collision* (Ethernet)
2	DB1* (SCSI)	GND	Collision+ (Ethernet)
3	DB2* (SCSI)	Reserved	Transmit* (Ethernet)
4	**DB3* (SCSI)**	**A24**	**Transmit+ (Ethernet)**
5	**DB4* (SCSI)**	**A25**	**Receive- (Ethernet)**
6	**DB5* (SCSI)**	**A26**	**Receive+ (Ethernet)**
7	DB6* (SCSI)	A27	+12V Fused
8	DB7* (SCSI)	A28	nSTROBE
9	DBP* (SCSI)	A29	D1
10	**ATN* (SCSI)**	**A30**	**D2**
11	**BSY* (SCSI)**	**A31**	**D3**
12	**ACK* (SCSI)**	**GND**	**D4**
13	RST* (SCSI)	+5V	D5
14	MSG* (SCSI)	D16	D6
15	SEL* (SCSI)	D17	D7
16	**C/D (SCSI)**	**D18**	**D8**
17	**REQ* (SCSI)**	**D19**	**nACK**
18	**I/O (SCSI)**	**D20**	**BUSY**
19	TERMPWR (SCSI)	D21	PERROR
20	MOUSE_CLK	D22	SELECT
21	MOUSE_DATA	D23	nAUTOFD
22	**KBD_5V**	**GND**	**nFAULT**
23	**KBD_CLK**	**D24**	**nINIT**
24	**KBD_DATA**	**D25**	**nSELECTIN**
25	S2_TXD	D26	SPEAKER_OUT
26	S2_RXD	D27	KEYLOCK_IN
27	S2_RTS	D28	S1_TXD
28	**S2_RI**	**D29**	**S1_RXD**
29	**S2_CTS**	**D30**	**S1_RTS**
30	**S2_DTR**	**D31**	**S1_CTS**
31	S2_DCD	GND	S1_DTR
32	S2_DSR	+5V	S1_DCD

VMEbus Signal Descriptions

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector.

Mnemonic	Description
A01 to A15	**Address Bus (bits 1 to 15)**. Address lines that are used to broadcast a short address
A16 to A23	**Address Bus (bits 16 to 23)**. Address lines that are used with A01 to A15 and LWORD* to broadcast a standard address
A24 to A31	**Address Bus (bits 1 to 15)**. Address lines that are used with A01 to A23 and LWORD* to broadcast an extended or 64-bit address
ACFAIL*	**AC Failure**. This shows that the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met
AM0 to AM5	**Address Modifier (bits 0 to 5)**. These are used to broadcast information such as the address size, cycle type, master identification or any combination of these
AS*	**Address Strobe**. This shows when a valid address has been placed on the address bus
BBSY*	**Bus Busy**. This is driven low by the requester associated with the current bus master to show that the master is using the bus
BCLR*	**Bus Clear**. This is generated by an arbiter to show that there is a higher priority request for the bus than the one being processed. This requests the current master to release the bus
BERR*	**Bus Error**. This is generated by a slave or bus timer to tell the master that the data transfer did not complete
BG0IN* to BG3IN*	**Bus Grant (0 to 3) In**. These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN*/BGxOUT* signals form the bus grant daisy chain, i.e. the BGxOUT* of one board forms the BGxIN* of the next board in the daisy chain
BG0OUT* to BG3OUT*	**Bus Grant (0 to 3) Out**. These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it can use the bus. Otherwise the board should pass the signal down the daisy chain
BR0* to BR3*	**Bus Request (0 to 3)**. A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.

Mnemonic	Signal Description
D00 to D31	**Data Bus**. These are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers
DS0*, DS1*	**Data Strobe 0, 1**. These are used with LWORD* and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus
DTACK*	**Data Transfer Acknowledge**. This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle
GND	The DC voltage reference for the system
IACK*	**Interrupt Acknowledge**. This is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN* pin of slot 1, where it is monitored by the IACK daisy chain driver
IACKIN*	**Interrupt Acknowledge In**. This tells the board receiving it that that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN*/IACKOUT* form the interrupt acknowledge daisy chain
IACKOUT*	**Interrupt Acknowledge Out**. This is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress
IRQ1* to IRQ7*	**Interrupt Request (1 to 7)**. These are driven low by interrupters to request an interrupt on the corresponding level.
LWORD*	**Longword**. This is used with DS0*, DS1* and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer.
Reserved	This signal is reserved for future enhancements of the VME specification.
SERA	The serial clock used to synchronise the data transmission on the serial bus.
SERB	This is used for serial data transmission.

Mnemonic	Signal Description
SYSCLK	**System Clock**. This provides a constant 16 MHz clock signal that is independent of any other bus timing
SYSFAIL*	**System Fail**. This shows that a failure has occurred in the system. This signal can be generated by any board in the system
SYSRESET*	**System Reset**. When this is low, it causes the system to be reset.
WRITE*	**Write**. This is generated by a master to show whether the data transfer cycle is a read or a write
+5VSTDBY	**+5 Volts DC Standby**. This supplies +5V DC to devices requiring battery back-up.
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power

P2 I/O Signal Descriptions

Mnemonic	Description
DB0* to DB7*	SCSI bus data
DBP*	SCSI bus data parity
ATN*	SCSI bus Attention
BSY*	SCSI bus Busy
ACK*	SCSI bus Acknowledge
RST*	SCSI bus Reset
MSG*	SCSI bus Message phase
SEL*	SCSI bus Select
C/D	SCSI bus Command/Data phase
REQ*	SCSI bus Request
I/O	SCSI bus I/O phase
TERMPWR	**SCSI bus terminator power.** Supplies power for external SCSI bus terminators. Fused at 1 Amp
MOUSE_CLK	**Mouse Clock.** Clock drive for mouse
MOUSE_DATA	**Mouse Data.** Mouse data line
KBD_5V	**Keyboard 5V.** Supplies power for the keyboard and mouse. Fused at 1 Amp
KBD_CLK	**Keyboard Clock.** Clock drive for the keyboard
KBD_DATA	**Keyboard Data.** Keyboard data line
S2_TXD	COM2 Transmit Data
S2_RXD	COM2 Receive Data
S2_RTS	COM2 Request-To-Send
S2_RI	COM2 Ring Indicator
S2_CTS	COM2 Clear-To-Send
S2_DTR	COM2 Data Terminal Ready
S2_DCD	COM2 Data Carrier Detect

Mnemonic	Description
S2_DSR	COM2 Data Set Ready
S1_TXD	COM1 Transmit Data
S1_RXD	COM1 Receive Data
S1_RTS	COM1 Request-To-Send
S1_CTS	COM1 Clear-To-Send
S1_DTR	COM1 Data Terminal Ready
S1_DCD	COM1 Data Carrier Detect
KEYLOCK_IN	**Keylock input.** Used to detect the state of an external keyswitch. May be used to implement system password protection
SPEAKER_OUT	**Loudspeaker Output.** Outputs a mono mix of Business Audio line-out and Timer2 Audio. May be used to drive 4R or 8R loudspeaker
nSELECTIN	Parallel port Select In
nINIT	Parallel port INIT
nFAULT	Parallel port FAULT
nAUTOFD	Parallel port AUTOFD
SELECT	Parallel port SELECT
PERROR	Parallel port PERROR
BUSY	Parallel port BUSY
nACK	Parallel port ACK
D1 to D8	Parallel port data bits
nSTROBE	Parallel port STROBE
+12V	**12 Volts.** Fused at 1 Amp to power external Ethernet transceiver. Also used by P2 adaptor
Receive+/-	Ethernet receive data
Transmit+/-	Ethernet transmit data
Collision+/-	Ethernet collision

PMC Connectors

J11 and J21 PMC Connector Pinout

Pin	Signal	Pin	Signal
1	TCK	2	-12V
3	Ground (0V)	4	INTA#
5	INTB#	6	INTC#
7	**BUSMODE#1**	**8**	**+5V**
9	**INTD#**	**10**	**Reserved**
11	**Ground (0V)**	**12**	**Reserved**
13	CLK	14	Ground (0V)
15	Ground (0V)	16	GNT#
17	REQ#	18	+5V
19	**+5V**	**20**	**AD[31]**
21	**AD[28]**	**22**	**AD[27]**
23	**AD[25]**	**24**	**Ground (0V)**
25	Ground (0V)	26	C/BE[0]
27	AD[22]	28	AD[21]
29	AD[19]	30	+5V
31	**+5V**	**32**	**AD[17]**
33	**FRAME#**	**34**	**Ground (0V)**
35	**Ground (0V)**	**36**	**IRDY#**
37	DEVSEL#	38	+5V
39	Ground (0V)	40	LOCK#
41	SDONE#	42	SBO#
43	**PAR**	**44**	**Ground (0V)**
45	**+5V**	**46**	**AD[15]**
47	**AD[12]**	**48**	**AD[11]**
49	AD[09]	50	+5V
51	Ground (0V)	52	C/BE[0]
53	AD[06]	54	AD[05]
55	**AD[04]**	**56**	**Ground (0V)**
57	**+5V**	**58**	**AD[03]**
59	**AD[02]**	**60**	**AD[01]**
61	AD[00]	62	+5V
63	Ground (0V)	64	REQ64#

J12 and J22 PMC Connector Pinout

Pin	Signal	Pin	Signal
1	+12V	2	TRST#
3	TMS	4	TDO
5	TDI	6	Ground (0V)
7	**Ground (0V)**	**8**	**Reserved**
9	**Reserved**	**10**	**Reserved**
11	**BUSMODE#2**	**12**	**+3.3V**
13	RST#	14	BUSMODE#3
15	+3.3V	16	BUSMODE#4
17	Reserved	18	Ground (0V)
19	**AD[30]**	**20**	**AD[29]**
21	**Ground (0V)**	**22**	**AD[26]**
23	**AD[24]**	**24**	**+3.3V**
25	IDSEL	26	AD[23]
27	+3.3V	28	AD[20]
29	AD[18]	30	Ground (0V)
31	**AD[16]**	**32**	**C/BE[2]**
33	**Ground (0V)**	**34**	**Reserved**
35	**TRDY#**	**36**	**+3.3V**
37	Ground (0V)	38	STOP#
39	PERR#	40	Ground (0V)
41	+3.3V	42	SERR#
43	**C/BE[1]**	**44**	**Ground (0V)**
45	**AD[14]**	**46**	**AD[13]**
47	**Ground (0V)**	**48**	**AD[10]**
49	AD[08]	50	+3.3V
51	AD[07]	52	Reserved
53	+3.3V	54	Reserved
55	**Reserved**	**56**	**Ground (0V)**
57	**Reserved**	**58**	**Reserved**
59	**Ground (0V)**	**60**	**Reserved**
61	ACK64#	62	+3.3V
63	Ground (0V)	64	Reserved

NOTE

The PPC60x supports only 5V powered PMC modules. The pins labelled as +3.3V are connected together and decoupled to ground to provide an AC return path.

PMC Signal Descriptions

Mnemonic	Description
AD0 to AD31	**Address/Data bits.** Multiplexed address and data bus
C_BE0 to C_BE3	**Command/Byte Enables.** During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus
FRAME*	**FRAME.** Driven low by the current master to signal the start and duration of an access
DEVSEL*	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	**Parity.** Parity protection bit for AD0 to AD31 and BE0 to BE3
IRDY*	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase
LOCK*	**LOCK.** Driven low to indicate an atomic operation that may require multiple transactions to complete
BUSMODE#1	**Bus Mode 1.** Driven low by a PMC module if it supports the current bus mode
BUSMODE#2 and BUSMODE#3	**Bus mode.** Driven by the host to indicate the bus mode. On the PPC60x this is always PCI
RST*	**Reset.** Driven low to reset the PCI bus
TRDY*	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase
PERR*	**Parity Error.** Driven low by a PCI agent to signal a parity error
SERR*	**System Error.** Driven low by a PCI agent to signal a system error
STOP*	**STOP.** Driven low by a PCI target to signal a disconnect or target-abort
INTA* and INTD*	**Interrupt lines.** Level-sensitive, active-low interrupt requests
CLK	**Clock.** All PCI bus signals except RST* are synchronous to this 33 MHz clock
REQ*	**Request.** Driven low by a PCI agent to request ownership of the PCI bus
GNT*	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	**Initialisation Device Select.** Device chip select during configuration cycles

P9 Floppy Disk Drive Connector Pinout

Pin	Signal	Pin	Signal
1	Ground (0V)	2	Density Select
3	Ground (0V)	4	Density Read 1
5	Ground (0V)	6	Data Rate 0
7	**Ground (0V)**	**8**	**Index#**
9	**Density Read 2**	**10**	**Motor Select 0#**
11	**Ground (0V)**	**12**	**Drive Select 1#**
13	Ground (0V)	14	Drive Select 0#
15	Ground (0V)	16	Motor Select 1#
17	Density Read 3	18	Direction#
19	**Ground (0V)**	**20**	**Step#**
21	**Ground (0V)**	**22**	**Write Data#**
23	**Ground (0V)**	**24**	**Write Gate#**
25	Ground (0V)	26	Track 0#
27	Density Read 4	28	Write Protect#
29	Ground (0V)	30	Read Data#
31	**Ground (0V)**	**32**	**Head Select#**
33	**Ground (0V)**	**34**	**Disk Change#**

P5 I/O Adapter Connector

This connector connects the two serial ports, Ethernet/10Base5 AUI, mouse and keyboard to the I/O Adapter board (POPPPC-21) or the front panel micro-D connectors (POPPPC-20). The pinout follows:

Pin	Signal	Pin	Signal
40	DTR2	39	RI2
38	TXD2	37	CTS2
36	RXD2	35	RTS2
34	**DCD2**	**33**	**DSR2**
32	**Serial Ground**	**31**	**Serial Ground**
30	**DTR1**	**29**	**RI1**
28	TXD1	27	CTS1
26	RXD1	25	RTS1
24	DCD1	23	DSR1
22	**Chassis Ground**	**21**	**Chassis Ground**
20	**Reserved**	**19**	**+12V Fused 1A**
18	**Ground (0V)**	**17**	**Ground (0V)**
16	Receive+	15	Receive-
14	Ground (0V)	13	Transmit-
12	Transmit+	11	Ground (0V)
10	**Collision+**	**9**	**Collision-**
8	**AUI Ground**	**7**	**AUI Ground**
6	**KBD +5V**	**5**	**KBD Ground**
4	KBD_DATA	3	KBD_CLK
2	MOUSE_DATA	1	MOUSE_CLK

Signal descriptions are given in the P2 I/O signal descriptions in this chapter.

P7 I/O Adapter Connector

This connector connects the Business Audio to the I/O Adapter board (POPPPC-21) or the front panel micro-D connectors (POPPPC-20). The pinout follows:

Pin	Signal	Pin	Signal
26	Reserved	25	Reserved
24	Reserved	23	Audio Ground
22	Speaker	21	Audio Ground
20	**Right Headphone out**	**19**	**Audio Ground**
18	**Left Headphone out**	**17**	**Audio Ground**
16	**Right Line out**	**15**	**Audio Ground**
14	Left Line out	13	Audio Ground
12	Right Line in	11	Audio Ground
10	Left Line in	9	Audio Ground
8	**Right Aux in**	**7**	**Audio Ground**
6	**Left Aux in**	**5**	**Audio Ground**
4	**Right Microphone in**	**3**	**Audio Ground**
2	Left Microphone in	1	Audio Ground

P8 RISCWatch Connector

This connector allows the connection of software debugging tools that use the processor's JTAG port to control the operation of the processor.

Pin	Signal	Pin	Signal
1	Ground (0V)	2	CKSTP~
3	Reserved	4	HRESET~
5	Reserved	6	SRESET~
7	Reserved	8	TMS
9	Reserved	10	TCK
11	+3.3V Pullup	12	Reserved
13	TRST~	14	TDI
15	Reserved	16	TDO

RISCWatch Connector Signal Descriptions

Signal	Description
Ground (0V)	Signal ground
CKSTP~	Processor Checkstop input
HRESET~	Processor Hard Reset
SRESET~	Processor Soft Reset
TMS	Processor JTAG Test Mode Select
TCK	Processor JTAG Test Clock
+3.3V Pullup	Power-on status signal to RISCWatch hardware
TRST~	Processor JTAG Test Reset
TDI	Processor JTAG Test Data In
TDO	Processor JTAG Test Data Out

P6 JTAG Connector

The JTAG connector is for factory test purposes only. It has the following pinout:

Pin	Signal	Pin	Signal
1	HRESET~	2	Ground (0V)
3	TCK	4	TRST~
5	TMS_60X	6	TMS_106
7	TMS_VME	8	TDI_60X
9	TDO_60X	10	TDI_106
11	TDO_106	12	TDI_VME
13	TDO_VME	14	CLOCK_BYPASS~
15	Ground (0V)	16	TEST_CLOCK

Other Connectors

With POPPPC-20 fitted, Ethernet/10Base5, Serial, and Keyboard, Mouse and Audio signals are available through the PPC60x front panel. With POPPPC-21 fitted, the same signals are available through the I/O adapter board. See Appendix B for the pinouts of the connectors.

Chapter 6 - Front Panel

This chapter describes the features found on the PPC60x front panel.

Reset Switch

The reset switch is a centre biased, 3-way momentary toggle switch that can be pushed up to generate a hard reset, or down to generate a soft reset. The reset switch may be disabled under hardware or software control. Software control is enabled following a power-up.

PCI Slots

There are two, numbered, PCI slots in the front panel, although depending on the amount of memory your PPC60x has and whether or not the PMC carrier card is fitted, one or other (or both) of the slots may not be available. If you have not ordered a PMC module for a PCI slot on your PPC60x, or the slot is unavailable, then Radstone will fit a blanking plate in the slot for EMC protection.

If you are fitting your own PMC module, then before fitting the module, remove the blanking plate from the appropriate slot. The module's bezel will fill the slot and will usually provide connection to the module. PMC modules are deliviered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

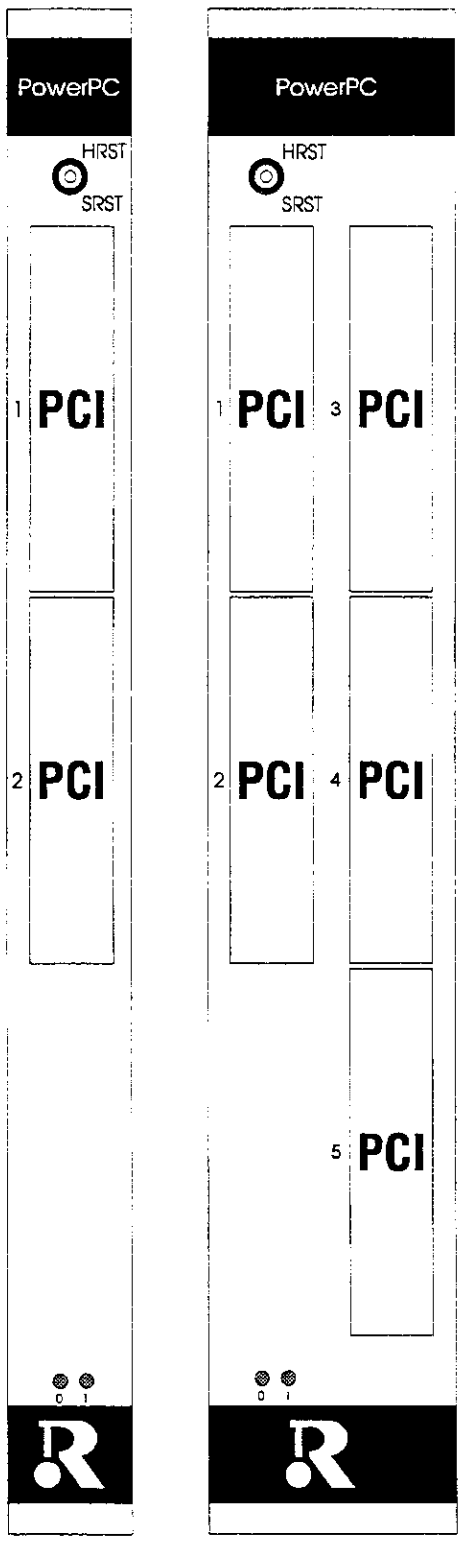
LEDs

Two software programmable LEDs (0 and 1) are mounted on the front panel. LED 0 is green and LED 1 is red. See the Software Programmable LEDs section in Chapter 9 for more details.

Connectors

Connectors are only available at the front panel when POPPPC-20 is fitted. See Appendix B for more details.

Figure 6-1. PPC60x Front Panel



Chapter 7 - Installation

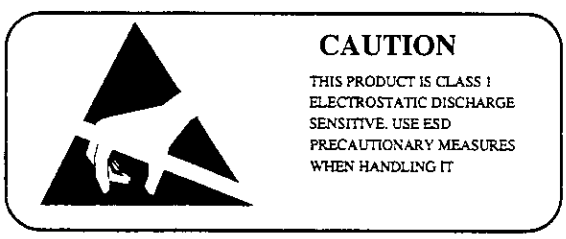
This chapter describes the installation of the PPC60x board in a system.

WARNINGS

Only use the PPC60x in backplanes that supply power on both the J1 and J2 connectors. Failure to observe this warning may result in damage to the board.

When using the Ethernet interface, there must be a maximum of 20 mΩ between the Ethernet cable shield and chassis ground.

With POPPPC-20 fitted, do *not* connect the G1 (keyboard, mouse and audio) or N1 (Ethernet/10Base5 AUI) connectors to anything other than their intended, marked, interface, as damage to the board may otherwise result. Take care, when connecting Ethernet and Mouse/Keyboard cables, that they are plugged into the correct sockets.



System Backplane Configuration Links

Before plugging the PPC60x into a development rack, you should first check the rack's backplane configuration links.

Radstone enclosures usually have two sets of links in the J1 (VMEbus) half of the backplane. The upper set of four links configures the Bus Grant (BGx) daisy chain and the lower link configures the Interrupt Acknowledge (IACK) daisy chain. They are provided so that the appropriate 'In' signal (BGxIN*/IACKIN*) at a particular slot can be connected to the corresponding 'Out' signal (BGxOUT*/IACKOUT*) at the same slot. This is only necessary when a slot position is not occupied by a board and there are boards further down the daisy chain. Some backplanes have daisy chains that automatically link the signals across empty slots. See the manual appropriate to your enclosure for further details.

NOTE

Take extra care if you are using POPPPC-21/FPX600 or the carrier card, as these occupy extra system slots, but require the daisy chains to be linked across the slots (see Appendix B).

Chassis Ground

To ensure optimum operation of the PPC60x with regard to EMC when taking I/O connections from the front panel connectors, there should always be a connection from the front panel to the chassis ground of the system. This also applies when the board is being operated on a VME bus extender. When taking I/O connections from P2, use the Radstone P2 accessory kits, or some equivalent system.

System Configuration Suggestions

Check the J2 connections of the slot before powering up (see the Warnings).

Use the default link configuration for the first power-up attempt.

Use the PPC60x in a development rack on its own at first, and only plug it in with other cards later (if other cards are to be used). This enables you to prove basic operation before tackling any system configuration issues.

Chapter 4 gives guidance on altering the PPC60x's link configuration to suit your requirements. Again, if possible, prove operation of the PPC60x on its own at first before integrating it into a system.

Use the screws at the top and bottom of the front panel to prevent cables pulling the PPC60x out of the rack (also applies to POPPPC-21 and the PMC carrier card).

To interact with the PPC60x's on-board firmware, you need to attach a serial terminal to the PPC60x. This terminal will use the serial signals on COM1 (the S1 connector, if available on POPPPC-20 or POPPPC-21). Alternatively, a PMC9100 graphics PMC module and a PS/2 compatible keyboard may be used. If these devices are used, the firmware detects their presence and uses them automatically.

Both the S1 (COM1) and S2 (COM2) interfaces are configured as DTE (9.6 Kbaud, 8 bits/character, 1 stop bit, parity disabled). However, cables supplied by Radstone permit direct connection to a terminal without use of a null-modem.

See the NCR53C810 SCSI Scripts Processor section in Chapter 9 for considerations to be taken into account when using the SCSI bus.

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Chapter 8 - Power-up and Operational Description

This chapter describes power-up and subsequent operation of the PPC60x.

Power-up

Having configured the backplane and taken note of the system configuration suggestions in chapter 7, with the PPC60x firmly secured in the rack, power-up the system.

The current on-board Boot firmware is described in the PPC60x Boot Firmware User Guide, publication number RT5057.

Operational Description

The on-board firmware for the PPC60x, which controls its operation after power-up, is described in separate user guides. This is because:

- The complexity of the firmware would lead to a chapter here that would be cumbersomely large and so possibly difficult to follow
- It allows changes to the firmware and corresponding user guide to be made without needing to change this (hardware-oriented) user guide
- It also gives the possibility of offering more than one on-board firmware package

Operating system support for the PPC60x is fully covered in Chapter 2.

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Chapter 9 - Functional Description

This chapter gives a detailed description of the PPC60x's functional blocks.

Resetting the PPC60x

There are two types of reset that may be applied to the PPC60x: 'Hard' and 'Soft'.

Hard Reset

A hard reset resets all on-board resources and causes the processor to immediately branch to 0xFFF00100. A hard reset may be generated by:

- A power-on reset
- A front panel reset switch hard reset
- A SYSRESET* from VME
- A remote reset via the PCI to VME bridge

As the hard reset signal is applied asynchronously to processor activity, it may cause a memory access to be aborted. A hard reset also disables the DRAM refresh function of the MPC106 PCI Bridge Memory Controller. As a result, memory integrity cannot be guaranteed after a hard reset.

NOTE

See the DRAM section for DRAM initialization requirements following a hard reset.

Soft Reset

A soft reset causes the processor to reach a recoverable state and then branch to either 0x00000100 or 0xFFF00100, depending on the state of the IP bit in the processor's Machine State Register. A soft reset may generated by:

- A front panel reset switch soft reset
- A software controlled ALT_RST* from the ISA bridge

The standard boot firmware does not support the use of soft reset.

The front panel reset switch may be disabled under both hardware and software control. Hardware control is described in chapter 4.

ISAbus Reset

The ISAbus may be reset under software control via the ISA Clock Divider register in the 82378ZB ISA bridge.

Memory Maps

The PPC60x supports both contiguous and non-contiguous PReP compliant memory maps. The following descriptions relate to the contiguous map unless otherwise stated. No fixed addresses are given for PCI connected resources (SCSI, Ethernet, VME bridge and PMC slots) since these addresses are configured by the boot process.

Memory Map Seen by the Processor

Processor Address Range		PCI Address Range	Cycle Type
00000000	7FFFFFFF	No PCI cycle	System memory space
80000000	8000FFFF	00000000 to 0000FFFF	ISA/PCI I/O space
80010000	807FFFFF	Reserved	Reserved
80800000	80FFFFFF	00800000 to 00FFFFFF	Alternate PCI configuration space
81000000	BF7FFFFF	01000000 to 3F7FFFFF	PCI I/O space
BF800000	BFFFFFEF	Reserved	Reserved
BFFFFFF0	BFFFFFFF	3FFFFFF0 to 3FFFFFFF	PCI/ISA interrupt acknowledge
C0000000	C03FFFFF	00000000 to 003FFFFF	User Flash ROM or PCI memory space
C0400000	C07FFFFF	00400000 to 007FFFFF	PCI memory space
C0800000	C09FFFFF	00800000 to 009FFFFF	RTC/NOVRAM
C0A00000	FEFFFFFF	00A00000 to 3EFFFFFF	PCI memory space
FF000000	FFEFFFFF	No PCI cycle	System ROM space - not implemented
FFF00000	FFF7FFFF	No PCI cycle	Flash boot ROM 1
FFF80000	FFFFFFFF	No PCI cycle	Flash boot ROM 2

PCI Memory Space Seen by the PCI Master

PCI Memory Address Range		Local Memory Cycle	Cycle Type
00000000	003FFFFF	No local memory cycle	User Flash ROM or PCI memory space
00400000	7EFFFFFF	No local memory cycle	PCI memory space
7F000000	7FFFFFFF	No local memory cycle	Reserved
80000000	FFFFFFFF	00000000 to 7FFFFFFF	System memory space

PCI I/O Space Seen by the PCI Master

PCI I/O Address Range		Local Memory Cycle	Cycle Type
00000000	0000FFFF	No local memory cycle	ISA/PCI I/O space
00010000	007FFFFF	No local memory cycle	Reserved
00800000	3F7FFFFF	No local memory cycle	PCI I/O space
3F800000	3FFFFFFF	No local memory cycle	Reserved
40000000	FFFFFFFF	No local memory cycle	Reserved

MPC106 PCI Bridge and Memory Controller

The Motorola MPC106 PCI Bridge and Memory Controller provides the host bridge between the processor bus and the PCI, a DRAM memory controller, the L2 cache controller, the Flash boot ROM interface and a central arbiter for the processor bus.

Second Level Cache

The size of the optional second level (L2) cache may be 256 or 512 Kbytes, which may be checked by reading the Equipment Present Register 1 (see the Control and Status Registers section).

Operation of the L2 cache must be set up in the MPC106 PCI Bridge Memory Controller. It may be configured for write-through or write-back operation.

Memory addresses in the range 0x0 to 0x40000000 (i.e. the lowest 1 Gbyte) are cacheable by the L2 cache.

Cache access times from the processor, referenced to the 66 MHz processor bus clock, for a 32 byte burst, are shown in the table:

Type	66 MHz Clock Cycles	Transfer Rate (Mbytes/second)
Burst read hit non-pipelined	3-1-1-1	356
Burst read hit pipelined	2-1-1-1	427

DRAM

The options available for on-board DRAM on the PPC60x are shown in the following table:

DRAM Size (Mbytes)	Banks	Organisation
8	1	1M x 72
16	2	2M x 72
32	1	4M x 72
64	2	8M x 72

The DRAM is protected by eight ECC syndrom bits per 64 data bits. All single bit, double bit and nibble errors can be detected, and single bit errors can be corrected.

Following a hard reset, the MPC106 PCI Bridge Memory Controller must be set up for the size and number of banks of DRAM (including any DRAM on a DRAM mezzanine expansion board) and the appropriate number of wait states to match the DRAM speed. This is done by the standard boot monitor firmware. The size and speed of motherboard DRAM may be checked by reading the Memory Size, Memory Presence and Memory Type Motherboard registers (see the Control and Status Registers section). At least 100µs must have elapsed from the negation of reset before enabling the DRAM. After being enabled, the DRAM must not be accessed until at least 8 refreshes have occurred. It is then necessary to initialise the DRAM to set-up valid ECC syndrom bits if ECC is to be enabled.

DRAM access times from the processor, referenced to the 66 MHz processor clock, for a 32 byte burst assuming RAS* has been precharged, are shown in the following table:

	Clock Cycles Initial Access/Subsequent	Equivalent Transfer Rate (Mbytes/second)
60ns DRAM peak burst	8-4-4-4	107
60ns DRAM sustainable burst	9-4-4-4	102

DRAM access times from the PCI, referenced to the 33 MHz PCI clock, for a 32-byte burst, are shown in the table:

	Clock Cycles Initial Access/Subsequent	Equivalent Transfer Rate (Mbytes/second)
L1 miss burst read	4-1-2-1-2-1-2-1	76
L1 miss burst write	2-1-1-1-1-1-1-1	118

Flash Boot ROM

The PPC60x may be fitted with 512 Kbytes (1 device) or 1 Mbyte (2 devices) of EPROM or Flash ROM, which holds the boot monitor firmware. Provided that you have not made any changes from the factory configuration, you can check the size of the boot ROM by reading the Equipment Present Register 2 (see the Control and Status Registers section).

The PPC60x supports one or two 4 Mbit EPROMs or 5V programming Flash ROMs in 32-pin PLCC packages for the Flash boot ROM. See Figure 4-1 in Chapter 4 for socket identification.

VME Boot Option

Fitting link LK13 (see Chapter 4) allows the PPC60x to boot code held in memory located on the VMEbus. This operation relies on the factory default power-up configuration for the VMEbus interface (see page 4-8). The VME memory must be located in A32 space at address 0xFFF00000 and must be 32 bits wide (D32).

In this mode it is possible to map the Flash boot ROM to address 0xFF000000 by setting the Configuration bit CF_FF0_LOCAL in Grackle register 0xA8. The Flash boot ROM may now be read and written as the most significant byte of every 8-byte-aligned address.

Once the Flash boot ROM is programmed, link LK13 should be removed and a hard reset carried out, Normal booting now occurs from the Flash boot ROM at address 0xFFF00000.

Peripheral Component Interconnect

The PCI is a high performance synchronous bus running at 33 MHz. The PPC60x implements a 32-bit PCI with burst data rates up to 132 Mbytes/second possible between PCI agents. The PCI bus structure of the PPC60x is shown in the block diagram in Chapter 2.

PCnet-PCI Ethernet Controller

The Am79C970 PCnet-PCI supports ANSI 802.3 10Base5 and Ethernet standards and has a direct interface to the PCI bus. It has 136-byte transmit and 128-byte receive FIFOs and a 32-bit DMA controller for access to data and descriptors in system memory. The network address is factory configured and held in NOVRAM. The PCnet-PCI requires 32 bytes of PCI I/O space. It cannot be accessed in PCI memory space.

Connection to the AUI is made through a front panel mounted 15-way micro D connector, industry standard D connector or through the P2 connector (depending on the I/O options chosen). Pinouts are given in Chapter 5. Three status LEDs (LED200 to LED202) are mounted on the back of the board behind the front panel (see the Software Programmable LEDs section). The default functions of these LEDs are receive status, link status and transmit status respectively. This may be overridden by the software.

NCR53C810 SCSI Scripts Processor

The NCR53C810 SIOP executes commands, in the form of SCSI scripts. It has a PCI interface and DMA controller, which are used to access the scripts and data held in system memory. The SIOP can transfer data at 5 Mbytes/second asynchronously and 10 Mbytes/second synchronously. The SIOP requires 256 bytes of either PCI memory or I/O space.

Connection to the SCSI bus is made through the P2 connector; the pinout is given in Chapter 5.

The PPC60x has an on-board active SCSI terminator, which may be enabled or disabled with a jumper (see the LK12 description in Chapter 4). The SCSI specification allows a maximum cable stub length of 10cm. If the SCSI bus connections are taken directly from the backplane J2 connector, then the PPC60x may be located anywhere on the SCSI bus and the terminator should be enabled only if the PPC60x is at the end of the SCSI bus. Otherwise, the PPC60x must be at the end of the SCSI bus and the terminator must be enabled.

A software programmable SCSI Activity LED (LED 205) is mounted on the back of the board behind the front panel. See the Software Programmable LEDs section and the SCSI Activity LED Register description for more details.

Universe VMEbus Bridge

The CA91C042 Universe VMEbus interface chip provides all slot 1 (system controller) functions, interrupt control, a DMA controller, interprocessor communications and block transfer support. The Universe chip requires 64 Kbytes of PCI I/O space for control and status registers. Appendix A details the VMEbus compliance of the PPC60x.

VMEbus Master Access

Four general purpose software programmable PCI slave images are available for access to the VMEbus. All of these can be configured to access VMEbus A32, A24 or A16 address space. An offset may be applied to translate the local address to a different address on the VMEbus, allowing any local address to access any VMEbus address. The start and end addresses of the A32, A24 and A16 PCI slave images may be set on any 64 Kbyte boundary in PCI memory or I/O space that is not allocated to other PCI attached devices or the user Flash EPROM. One image may be set on 4 Kbyte boundaries to accomodate access to A16 space.

One further, special purpose, PCI slave image allows mapping of A16 and A24 space. This slave image uses a 64 Mbyte window, aligned to any 64 Mbyte address in PCI memory space. The window is divided into four 16 Mbyte quadrants. The top 64 Kbytes of each quadrant will map to A16 space, while the rest of each quadrant will map to A24 space. The Address Modifiers generated are software configurable for each quadrant.

VMEbus master cycles may be coupled or write posted. Coupled cycles are not terminated on the PCI until all data has been transferred over the VMEbus. Posted writes are queued in a FIFO until the VMEbus is available for the data to be transferred.

VMEbus Slave Access

Four general purpose software programmable VMEbus slave images are available. All of these may be defined in VMEbus A32, A24 or A16 space. An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any on-board address. The start and end addresses of the A32, A24 and A16 images may be set on any 64 Kbyte boundary.

A further, special purpose, VMEbus slave image allows access to the Universe chip registers.

VMEbus slave accesses to the PPC60x may be coupled, write posted or prefetched block read. Coupled slave transfers can only proceed once the slave posted write FIFO is empty. Slave posted write cycles are queued in a FIFO until the PCI is available for the data to be transferred.

Typical single cycle access times, DS* to DTACK*, are:

Slave DRAM read = 460 ns

Slave DRAM write = 360 ns

Slave posted write = 100 ns

Indivisible Cycles on VME

The Universe chip may be programmed to generate RMW cycles on the VMEbus. Data from the read portion is compared with a 32-bit compare value, qualified with a 32-bit mask. If the comparison is true, then those bits enabled by the mask are swapped with a 32-bit swap field. Alternatively, the Universe chip's VMEbus ownership bit may be set to cause it to acquire and hold ownership of the VMEbus. This method can be used in combination with VMEbus LOCK cycles to guarantee exclusive access to a VMEbus resource.

The VMEbus slave images may be programmed to generate locked cycles on the PCI to handle RMW cycles. The Universe chip also supports VMEbus lock commands using ADOH cycles.

VMEbus Arbitration

The Universe chip's VMEbus arbiter supports PRI and RRS arbitration with BCLR* generation in priority mode.

The VMEbus requester may operate in fair or demand mode and may be configured as RWD or ROR.

(1) When System Controller:

Period	Typical (ns)
BRx*(low) to BGxOUT*(low) when bus free	125
BBSY*(high) to BGxOUT*(low)	78

(2) When non System Controller:

Period	Typical (ns)
BGxIN*(low) to BGxOUT*(low)	32

VMEbus Master Block Transfers

The Universe chip's DMA controller may be used to transfer data between the PCI and the VMEbus using D32 or D64 transfers. DMA operations on the two buses are decoupled through a bidirectional FIFO.

The DMA controller may transfer multiple blocks of data using entries in a linked-list. It can also pack/unpack data to support differing data widths on the PCI and the VMEbus.

D32 DMA

D32 DMA read from slave PPC60x	17 Mbytes/second
D32 DMA write to slave PPC60x	25 Mbytes/second
D32 DMA read from ideal VMEbus slave	25 Mbytes/second
D32 DMA write to ideal VMEbus slave	35 Mbytes/second

D64 DMA

D64 DMA read from slave PPC60x	26 Mbytes/second
D64 DMA write to slave PPC60x	28 Mbytes/second
D64 DMA read from ideal VMEbus slave	50 Mbytes/second
D64 DMA write to ideal VMEbus slave	34 Mbytes/second

VMEbus Slave Block Transfers

The VMEbus slave interface can respond to D32:BLT and D64:MBLT block transfers. The Universe chip may be programmed to pre-fetch read data for VMEbus slave block transfers, which is queued in a FIFO.

VMEbus D32 Slave Block Transfers

D32 slave block write from PPC60x	30 Mbytes/second
D32 slave block read from PPC60x	14 Mbytes/second
D32 slave block write from ideal master	36 Mbytes/second
D32 slave block read from ideal master	32 Mbytes/second

VMEbus D64 Slave Block Transfers

D64 slave block write from PPC60x	43 Mbytes/second
D64 slave block read from PPC60x	33 Mbytes/second

VMEbus Interrupts

If programmed to do so, the Universe chip responds to a VMEbus interrupt with a VMEbus interrupt acknowledge cycle. The Universe chip captures the status/ID and then raises an interrupt on the PCI. No further VMEbus interrupts are handled on that level until the processor reads the status/ID and re-arms the interrupt handler.

The Universe chip can be programmed to generate any level of VMEbus interrupt. It raises an interrupt on the PCI when the VMEbus interrupt has been acknowledged.

VMEbus Bus Errors

Assertion of VMEbus BERR* during a coupled VMEbus master cycle causes a target-abort (bus error) on the PCI. A PCI target-abort during a coupled VMEbus slave cycle causes BERR* on the VMEbus. See the Machine Check Exception section for further details of target abort.

A bus error during posted write transfers raises an interrupt to the processor (if enabled). A number of options are available, including stopping the operation and purging the offending transaction.

A bus error during a DMA operation raises an interrupt and stops the operation on the bus where the error was detected.

VMEbus Retries

The Universe chip, as a PCI target, retries the PCI master under the following conditions:

- The PCI initiator requests a coupled cycle to the VMEbus whilst the Universe is not VMEbus master
- The PCI initiator requests a coupled cycle to the VMEbus whilst the posted write FIFO still contains data
- The PCI initiator requests a posted write cycle when the posted write FIFO can accept no more entries

VMEbus Reset Options

Several Universe chip operating features are set at power-up or reset by surface mount jumpers. See chapter 4 for the default options.

PCI to PCI Bridge and PMC Slots

The DECchip21050 PCI to PCI bridge is used to isolate the primary PCI from the PMC slots and the PCI carrier card (if fitted). It also allows concurrent operation on each PCI. The bridge must be programmed by the boot process to pass the necessary addresses for any PMC modules installed. See the PCI Configuration section in this chapter.

82378ZB ISAbus Bridge

The Intel 82378ZB provides a bridge from the PCI to the ISAbus for connection of native I/O devices. This device also provides:

7 channel DMA between ISA and PCI	-	function of two 83C37s
Timer block	-	function of 82C54
Interrupt controller	-	function of two 8259s

The ISA bridge positively decodes some I/O cycles on the PCI for internal resources. It subtractively decodes and claims all PCI memory and I/O cycles not claimed by other PCI targets and forwards them to the ISAbus.

There are no ISAbus masters other than the ISA bridge in the PPC60x architecture.

Super I/O

The SMC 37C665GT Super I/O, connected to the ISAbus, contains a Floppy Disk controller, and serial and parallel ports. The IDE interface is not used on the PPC60x.

Floppy Disk Controller

Connection to the FDC is through an on-board header, via the P2 connector of the I/O adapter or, under software control, through the parallel port connection. Pinouts are given in Chapter 5.

The FDC is software compatible with the DP8473, 765A and NS82077.

Serial I/O

The Super I/O provides two serial channels containing FIFOs, software compatible with the INS8250N-B, PC16550A and PC16450. The baud rates are programmable from 50 baud up to 115.2 kbaud, including the MIDI data rate.

Connection to the serial ports is through the P2 connector (S1 is restricted to 6 wire), through front panel mounted 9-way micro-D connectors (if POPPPC-20 is fitted) or through industry standard D connectors on the front panel I/O adapter (if POPPPC-21 is fitted). Pinouts are given in Appendix B.

Parallel I/O

The parallel port includes Extended Capabilities conforming to IEEE P1284. It may, under software control, be configured as an external floppy disk drive interface.

Connection to the parallel port is through the P2 connector. The pinout is given in Chapter 5.

Keyboard and Mouse Controller

A PS/2 compatible Keyboard and Mouse interface is provided by an Intel 82C42PE with Phoenix Multikey/42G PS/2 compatible BIOS connected to the X bus.

Connections to the mouse and keyboard are through the P2 connector, a front panel mounted micro-D connector (if POPPPC-20 is fitted) or through PS/2 compatible miniature DIN connectors on the front panel I/O adapter (if POPPPC-21 is fitted). A POP is also available to fit two mini-DIN connectors on the motherboard. This option prevents one of the PMC slots being used. Pinouts are given in Appendix B.

User Flash ROM

The PPC60x may optionally be fitted with 2 or 4 Mbytes of user Flash ROM. The size of the user Flash ROM may be checked by reading the Equipment Present Register 2 (see the Control and Status Registers section).

CIO

The 85C36 CIO provides three independent 16-bit counter/timers that each have a resolution of 500 ns. Two of the counter/timers may be linked to form a 32-bit counter/timer.

The functions of the I/O port bits are described in the Control and Status Registers section.

Software Programmable LEDs

There are eight software programmable LEDs on the PPC60x.

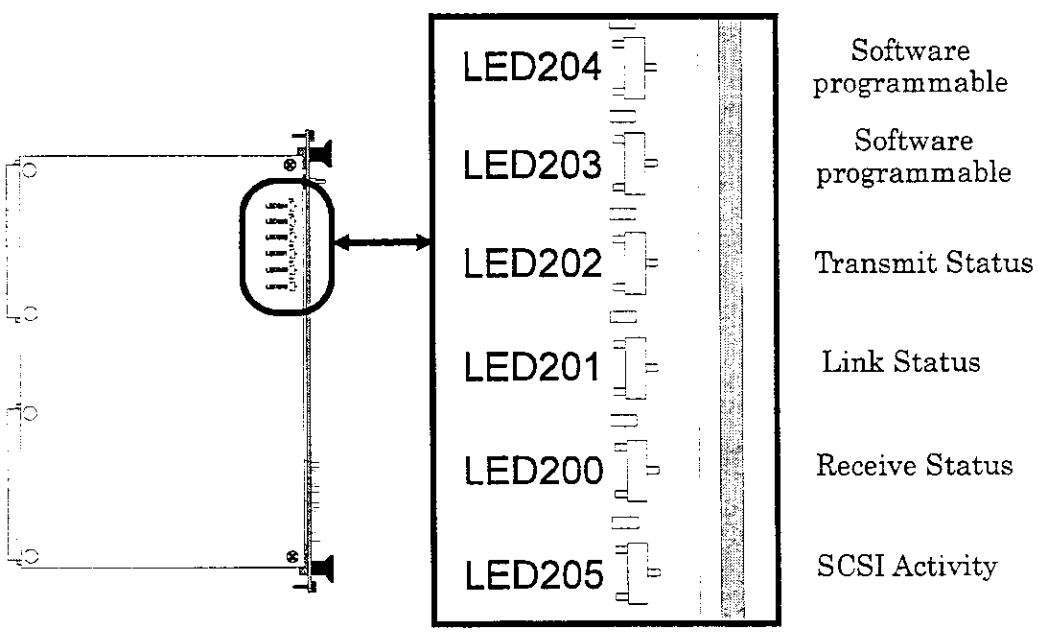
Two of them, LED 0 (green) and LED 1 (red), are mounted through the front panel (see Figure 6-1 in Chapter 6 for the location of these LEDs). They are connected to port C of the CIO (see the CIO Port C Data register description for more details). After power-up, LED 1 is on by default.

The remaining six LEDs are all surface mounted in a block on the solder side of the PCB behind the front panel.

LED200, LED201 and LED202 are Ethernet status LEDs. The default functions of these LEDs are receive status, link status and transmit status respectively, but these may be overridden by the software.

LED203 and LED204 are general purpose software programmable LEDs. They are connected to port C of the CIO, along with LED 0 and LED 1. See the CIO Port C Data register description for more details.

LED 205 is a SCSI Activity LED. See the SCSI Activity LED Register description for more details.



RTC/NOVRAM

An M48T18 provides RTC functions and 8Kx8 of battery-backed NOVRAM. The following information is derived from the M48T18 data sheet.

The battery is provided in a 'snaphat' package to allow user replacement. The SGS-Thomson part number for replacement batteries is M4T28-BR12SH1.

Battery storage life is a function of temperature. At the PPC60x's maximum specified storage temperature of 85°C, the battery has a 1% chance of failure after 2.5 years and a 50% chance of failure after 5 years. At 70°C, these times become 11 years and 20 years respectively. The M48T18 data sheet shows how to calculate the expected battery storage life, knowing the expected storage temperature and the storage period.

The battery has a rated capacity of 50mAh. At room temperature, the battery has a predicted capacity life of about 11 years with no external power. Battery capacity life is extended by powering-up the board or by turning off the clock oscillator before system power-down. For example, if the oscillator runs 100% of the time with external power applied 60% of the time, the capacity life is 10/(1 - 0.6), or 25 years.

Control and Status Registers

ISA I/O Port (Hex)	Contiguous I/O Mode Address	Non-Contiguous I/O Mode Address	Description	Type
0092	8000 0092	8000 4012	Port 92	R/W
03F3	8000 03F3	8001 F013	Media sense	RO
0803	8000 0803	8004 0003	Memory size	RO
0804	**8000 0804**	**8004 0004**	**Memory presence**	**RO**
0808	**8000 0808**	**8004 0008**	**SCSI Activity LED Register**	**WO**
080C	**8000 080C**	**8004 000C**	**Equipment present 1**	**RO**
080E	8000 080E	8004 000E	Equipment present 2	RO
0810	8000 0810	8004 0010	NOVRAM protect 1	WO
0812	8000 0812	8004 0012	NOVRAM protect 2	WO
0814	**8000 0814**	**8004 0014**	**L2 invalidate**	**WO**
0818	**8000 0818**	**8004 0018**	**Key lock**	**RO**
0854	**8000 0854**	**8004 2014**	**Board revision**	**RO**
0860	8000 0860	8004 3000	CIO port C data	R/W
0861	8000 0861	8004 3001	CIO port B data	R/W
0862	8000 0862	8004 3002	CIO port A data	R/W
0863	**8000 0863**	**8004 3003**	**CIO control**	**R/W**
0864	**8000 0864**	**8004 3004**	**ID link**	**RO**
0866	**8000 0866**	**8004 3006**	**Memory type motherboard**	**RO**
0868	8000 0868	8004 3008	Memory type mezzanine	RO
0CF8	8000 0CF8	-	PCI CONFIG_ADDR	RO
0CFC	8000 0CFC	-	PCI CONFIG_DATA	RO
-	**BFFF FFF0**	**BFFF FFF0**	**vector**	**RO**

Where: R/W = Read/Write RO = Read Only WO = Write Only

The control and status registers exist on the PPC60x for controlling or reading the status of the hardware. The addresses are as seen by the processor.

Each register is described in detail in the following pages. The register bit significance is shown in big-endian mode (i.e. from the 603/4 programmer's viewpoint).

Port 92 (Port 0x0092)

This register provides an alternate soft reset.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 6: Reserved.

Bit 7: Setting this bit causes a soft reset to occur. It must be cleared before another soft reset can be issued.

Media Sense Register (Port 0x03F3)

This register provides the floppy disk controller media sense function.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 and 1: Media ID. Driven by the PPC60x hardware.
00 = No media present
01 = 4.0 Mbyte (unformatted) media
10 = 2.0 Mbyte (unformatted) media
11 = 1.0 Mbyte (unformatted) media

Bits 2 and 3: Drive ID. Driven by the PPC60x hardware.
00 = 3.5" 1.44 Mbyte drive
01 = 3.5" 2.88 Mbyte drive
10 = 5.25" 1.2 Mbyte drive
11 = No drive present

Bits 4 and 5: Reserved

Bits 6 and 7: Selected drive. Driven by the Super I/O chip.
00 = Drive 0 selected
01 = Drive 1 selected
10 = Drive 2 selected
11 = Drive 3 selected

Memory Size Register (Port 0x0803)

This register provides information on the size of each memory bank.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 3: Reserved

Bit 4: Bank 3 size
0 = 8 Mbytes
1 = 32 Mbytes

Bit 5: Bank 2 size
0 = 8 Mbytes
1 = 32 Mbytes

Bit 6: Bank 1 size
0 = 8 Mbytes
1 = 32 Mbytes

Bit 7: Bank 0 size
0 = 8 Mbytes
1 = 32 Mbytes

Memory Presence Register (Port 0x0804)

This register provides information on which of the eight possible memory banks are populated.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 3: Reserved

Bit 4: Bank 3 populated
0 = Bank populated
1 = Bank not populated

Bit 5: Bank 2 populated
0 = Bank populated
1 = Bank not populated

Bit 6: Bank 1 populated
0 = Bank populated
1 = Bank not populated

Bit 7: Bank 0 populated
0 = Bank populated
1 = Bank not populated

SCSI Activity LED Register (Port 0x0808)

This register allows control of the SCSI activity LED (LED 205).

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 6: Reserved.

Bit 7: SCSI activity LED
0 = LED off
1 = LED on

See the Software Programmable LEDs section for the location of this LED.

Equipment Present Register 1 (Port 0x080C)

This register provides information on hardware options and the state of the SCSI Terminator power fuse.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bit 0: Reserved.

Bit 1: SCSI_FUSE_GOOD
0 = SCSI fuse bad
1 = SCSI fuse good

Bit 2: PRSNT1_2*
0 = Slot 2 PMC present (on-board)
1 = Slot 2 empty

Bit 3: PRSNT1_1*
0 = Slot 1 PMC present (on-board or on the PCC)
1 = Slot 1 empty

Bit 4: Reserved

Bit 5: L2_256K
0 = L2 cache is 512 Kbyte
1 = L2 cache is 256 Kbyte

Bit 6: Reserved

Bit 7: L2_PRES*
0 = L2 cache present
1 = L2 cache not present

Equipment Present Register 2 (Port 0x080E)

This register provides information on hardware options.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bit 0: VME_PRESENT
0 = VME not present
1 = VME present

Bit 1: AUDIO_PRESENT
0 = Business Audio not present
1 = Business Audio present

Bit 2: SFLSH2_PRESENT
0 = 0.5 Mbyte Flash boot ROM
1 = 1 Mbyte Flash boot ROM

Bits 3 to 5: Processor Speed bits
000 = 66 MHz
001 = 100 MHz
010 = 120 MHz
011 = 133 MHz
100 = 150 MHz
101 = Reserved
110 = Reserved
111 = Reserved

Bits 6 and 7: User Flash presence/size bits
00 = No user Flash
01 = 2 Mbyte user Flash
10 = 4 Mbyte user Flash
11 = Reserved

NOVRAM Protect 1 Register (Port 0x0810)

Writing any value to this register sets a flip-flop that locks-out further accesses to addresses 0x1FD0 to 0x1FDF of the NOVRAM address space. The flip-flop is only cleared by an ISAbus reset. A read of this register has no effect.

NOVRAM Protect 2 Register (Port 0x0812)

Writing any value to this register sets a flip-flop that locks-out further accesses to addresses 0x1FE0 to 0x1FEF of the NOVRAM address space. The flip-flop is only cleared by an ISAbus reset. A read of this register has no effect.

L2 Invalidate Register (Port 0x0814)

Writing any value to this register causes the L2 cache tag RAM to be reset. A read of this register has no effect.

NOTE

Disable the L2 cache before resetting the tag RAM.

Key Lock Register (Port 0x0818)

This register provides information on the state of the keylock signal. See the Keylock section.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 6: Reserved

Bit 7: Keylock
0 = Keylock signal low
1 = Keylock signal high

Board Revision Register (Port 0x0854)

This register provides information on the build state of the PPC60x.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 2: Number revision of hardware build state
3 = Revision 3
4 = Revision 4
5 = Revision5
All other values are Reserved.

Bits 3 to 7: Letter revision of hardware build state
0x0 = Revision A
0x1 = Revision B
...
0x18 = Revision Y
0x19 = Revision YA
...
0x1F = Revision YG

CIO Port C Data (Port 0x0860)

CIO port C is used to drive four software programmable LEDs.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 3: Write protect mask for bits 4 to 7 respectively:
0 = Write enabled
1 = Write protected

Bit 4: LED204, surface mounted
0 = LED on
1 = LED off

Bit 5: LED203, surface mounted
0 = LED on
1 = LED off

Bit 6: LED 1 (red), front panel mounted
0 = LED off
1 = LED on

Bit 7: LED 0 (green), front panel mounted
0 = LED on
1 = LED off

See the Software Programable LEDs section for the location of these LEDs.

LED 1 is on by default after power-up.

NOTE

CIO Port B Data (Port 0x0861)

CIO port B is not used on the PPC60x.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 7: Reserved

CIO Port A Data (Port 0x0862)

CIO port A is used to control certain hardware features.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0-1: Reserved

Bit 2: FLSH_RST~ O/P
0 = Reset User Flash to read mode
1 = User Flash normal operation

Bit 3: FLSH_RDY1 I/P
0 = User Flash 2-3 Mbytes Busy
1 = User Flash 2-3 Mbytes Ready

Bit 4: FLSH_RDY0 I/P
0 = User Flash 0-1 Mbytes Busy
1 = User Flash 0-1 Mbytes Ready

Bit 5: BRIDGE1_BUFFNE~ I/P
0 = PCI to PCI bridge buffer not empty
1 = PCI to PCI bridge buffer empty

Bit 6: BRIDGE1_DIPST~ O/P
0 = PCI to PCI bridge flush and disable write posting buffer
1 = PCI to PCI bridge write posting enabled

Bit 7: RST_SW_EN O/P
0 = Front panel reset switch disabled
1 = Front panel reset switch enabled

CIO Control (Port 0x0863)

See the CIO datasheet for a full description of the control registers.

ID Link Register (Port 0x0864)

This register allows the ID links, LK8 to LK11, to be read.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 to 3: Reserved

Bit 4: LK11
0 = Link fitted
1 = Link not fitted

Bit 5: LK10
0 = Link fitted
1 = Link not fitted

Bit 6: LK9
0 = Link fitted
1 = Link not fitted

Bit 7: LK8
0 = Link fitted
1 = Link not fitted

Memory Type Motherboard Register (Port 0x0866)

This register provides information on the type of DRAM fitted on the PPC60x. It should be used in conjunction with the memory size and presence registers.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 and 1: DRAM Speed
00 = Reserved
01 = Reserved
10 = 60ns DRAM
11 = 70ns DRAM

Bit 2: ECC_TYPE
0 = ECC
1 = Parity (not used on PPC60x Rev. 5 and later)

Bit 3: ECC
0 = ECC not fitted
1 = ECC fitted

Bit 4: REFRESH_MODE
0 = Asymmetrical (not used on PPC60x)
1 = Symmetrical

Bit 5: DRAM_TYPE
0 = Normal DRAM
1 = EDO DRAM

Bit 6: Reserved

Bit 7: Reserved

Memory Type Mezzanine Register (Port 0x0868)

This register provides information on the type of DRAM fitted on the DRAM mezzanine expansion board (if installed).

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

Bits 0 and 1: DRAM Speed
00 = Reserved
01 = Reserved
10 = 60ns DRAM
11 = 70ns DRAM

Bit 2: ECC_TYPE
0 = ECC
1 = Parity (not used on PPC60x Rev. 5 and later)

Bit 3: ECC
0 = ECC not fitted
1 = ECC fitted

Bit 4: REFRESH_MODE
0 = Asymmetrical
1 = Symmetrical

Bit 5: DRAM_TYPE
0 = Normal DRAM
1 = EDO DRAM

Bit 6: Reserved

Bit 7: Reserved

Interrupts and Error Reporting

The various external interrupt sources to the processor and their relative priorities are shown in the table below. The table also shows whether the previous state of the processor is recoverable.

Priority	Interrupt	Cause	Recoverability
0	System Reset	Power on, Hard reset	Non-recoverable
1	Machine Check	TEA* input, Address or Data Parity, Machine Check Input (MCP*), Non-maskable Interrupt (NMI*)	Non-recoverable in most cases
2	System Reset	Soft reset	Recoverable unless Machine Check occurs
3	System Management Interrupt	SMI* input	Recoverable unless Machine Check or System Reset occurs
4	External Interrupt	INT* input	Recoverable unless Machine Check or System Reset occurs

System Resets

See the Resetting the PPC60x section at the start of this chapter.

Machine Check Exception

The PCI bridge may be configured to assert TEA* to the processor for a Flash write error or an unsupported local bus cycle. The processor may be configured to take a machine check exception or enter the checkstop state.

The processor address and data parity error inputs (APE* and DPE*) are not used on the PPC60x. Address and data parity errors are reported via the machine check pin as described below.

The PCI bridge may be configured to assert the machine check input to the processor (MCP*) to signal a non-recoverable error. The processor may be configured to take a machine check exception or enter the checkstop state. Non-recoverable errors are:

- Flash write error
- Unsupported local bus cycle
- PCI PERR or SERR
- Memory read parity error
- Memory select error (address out of range)
- PCI target abort (e.g. VMEbus BERR*) or master abort

Status bits in the PCI bridge allow the cause of the exception to be determined.

Links LK1 and LK2 allow the PPC60x hardware to be configured so that machine checks are signalled as an interrupt on IRQ14 rather than on the processor's MCP* pin. These links are described in chapter 4.

If you know that a machine check may occur during a specific operation (e.g. a VMEbus BERR* during a VMEbus memory sizing operation), it may be possible to ensure that the processor is in a recoverable state after the machine check exception by using the SYNC instruction before and after the instruction that potentially causes machine check.

Non-Maskable Interrupt (NMI*)

The NMI* output of the ISA bridge is connected to the NMI* input of the PCI bridge. It is not generally required, as the PCI bridge can be configured to detect SERR on the PCI bus.

System Management Interrupt (SMI*)

The System Management Interrupt pin of the PCI bridge is connected to the SMI* output from the ISA bridge to support the power management features of the ISA bridge.

External Interrupt (INT*)

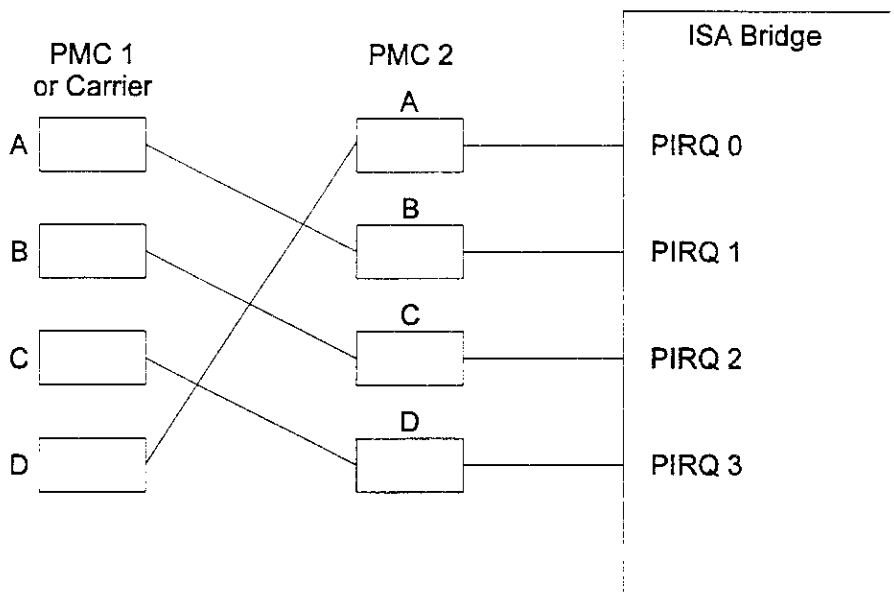
The processor external interrupt pin (INT*) is asserted for a pending interrupt from the interrupt controller in the ISA bridge. Edge sensitive interrupts are rising edge sensitive. Level sensitive interrupts are active low. The assignments shown in the following table are set up by the standard boot firmware. If you are using alternate boot firmware, it must duplicate these settings.

Interrupt priorities and modes are assigned as shown in the table:

IRQ	Priority	Mode	Source
0	1	Edge	Timer 1 Counter 0 (internal to ISA bridge)
1	2	Edge	Keyboard
2			Cascade for IRQ8 to IRQ15
3	11	Edge	S2
4	12	Edge	S1
5	13	Level	CIO
6	14	Edge	Floppy
7	15	Edge	LPT1
8	3		Unassigned
9	4	Level	Ethernet
10	5	Edge	Audio
11	6	Level	VME
12	7	Edge	Mouse
13	8		Unassigned
14	9	Level	SCSI or Alternate machine check interrupt
15	10	Level	PMC slots

PCI Interrupts

The four PCI interrupt lines (A, B, C and D) from each PMC slot are connected to the PIRQ0* to PIRQ3* inputs of the interrupt controller, as shown in the following diagram:



The PCI specification explains the rationale behind the 'rotated' interrupt connections.

PCI Configuration

The boot process must configure the base address and space type (memory or I/O) of all the PCI attached peripherals. The memory requirements of each PCI device are given in the appropriate device descriptions in this chapter.

Each PCI device also has several registers located in PCI configuration space, which is accessed by the processor through the MPC106 PCI bridge and memory controller using the CONFIG_ADDR and CONFIG_DATA registers. A full description of PCI configuration can be found in the PCI and MPC106 specifications.

The device number mapping for the PCI bus attached to the MPC106 follows:

Device Number	Function
0	MPC106 PCI bridge and memory controller
1 to 10	Not implemented
11	82378ZB ISA bridge
12	53C810 SCSI controller
13	79C970 PCnet to PCI
14	Universe VME controller
15	PCI to PCI bridge
16 to 30	Not implemented

The device number mapping for the PCI behind the PCI to PCI bridge follows:

Device Number	Function
0	PMC 1 or carrier
1	PMC 2
2 to 30	Not implemented

Keylock

The keylock input signal allows an external keyswitch to be interrogated by software. For example, the boot firmware could request a password if the keyswitch is in the locked position and a password is set up in the NOVRAM.

The keylock signal defaults to high if no external connection is made.

Chapter 10 - Troubleshooting

This chapter gives some suggestions for what to do when your PPC60x doesn't work.

1) Don't panic!

2) Use a step-by step method for looking at the problem.

3) Try to diagnose the problem type (i.e. hardware or software).

4) If all else fails, phone or fax your nearest Radstone technical support section for assistance.

Step 1 - No Power

Check that your enclosure's mains power lead is plugged into the mains outlet and into the chassis.

Check that you have switched on at the mains and at the system.

Check that you are receiving power from the mains outlet (test this with a lamp for example).

Ensure that no fuses have blown.

If the system refuses to start up, this suggests a problem with the power supply. It is essential that only qualified personnel deal with the problem from now on.

Step 2 - Power On, Unexpected Behaviour

Ensure that the board is firmly seated and secured in the rack and that all male/female connectors mate together correctly.

Check the links on the board and the system backplane.

If you are unsure of which link configuration to use, use the default configuration initially.

Check that the VME rack has terminators, if these are not built in (the manual for your rack should tell you whether the terminators are built in).

Check that the power supply is within VME limits on +5V, +12V and -12V with a digital volt meter.

Check that there is only one board configured as system controller and that this is in slot 1.

Check that there are no vacant slots in the rack without jumpers (or that an automatic daisy chaining backplane is being used).

NOTE

Take extra care if you are using POPPPC-21/FPX600 or the carrier card, as these occupy extra system slots, but require the daisy chains to be linked across the slots.

If you are still getting unexpected behaviour, try removing all other VME boards from the rack and proving the PPC60x's operation in isolation, then adding a board at a time until the offending element is found.

If you are using the SCSI bus, then check that the cable stub length is less that 10 cm. Also ensure that the bus terminator is only enabled if the PPC60x is at the end of the SCSI bus. If the SCSI connections are being taken from the backplane J2 connector, then the PPC60x may be anywhere on the SCSI bus, otherwise the PPC60x must be at the end of the SCSI bus.

If you are using Ethernet or 10Base5 through the front panel mounted AUI, ensure that the AUI ground link (LK4) is correctly connected for the appropriate ground.

The battery for the RTC/NOVRAM may be exhausted, causing corruption of passwords or environmental variables. See the RTC/NOVRAM section in Chapter 9 for more details.

Step 3 - Power On, No Terminal Display

Check that all cables are plugged in correctly.

If you have made your own cable, check that the pinout is correct.

Check that all connections are tight.

Check that the terminal is receiving power and is on.

Check that the terminal is set up for DTE (9.6 Kbaud, 8 bits/character, 1 stop bit, parity disabled).

Step 4 - Overheating

Check that no grilles are blocked in the chassis, either internally or externally.

Check that the fans are working.

Clean or replace any air filters fitted to fans.

Check that there is a free air flow around the chassis exterior (i.e. it should not be in an alcove or other confined space, or on a thick pile carpet).

Check that the enclosure is not next to a radiator or other heat source.

Step 5 - PPC60x Locks-up

Try resetting the PPC60x or powering the system down and then up again.

Debugging

When debugging software, disable the caches to make tracing the software execution easier.

When Phoning, Faxing or E-Mailing for Technical Support, Be Prepared To Give

- Your name, work address, work telephone and fax numbers, and e-mail address (if appropriate)
- A detailed description of the problem
- Any messages and error messages being generated
- What has been tried so far
- The software revision level, hardware platform, hardware revision and operating system level
- Other boards that you are using in the system with the PPC60x
- If you are reporting a bug, give detailed instructions on how to reproduce the problem and sample code, if possible (if the bug occurs in an application)

Telephone and Fax Numbers

UK

Telephone (office hours)	+44 (0)1327 359444
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North Central Region:	(708) 304 0202
South Central Region:	(214) 479 9040
North West region	(408) 727 4795
South West region	(909) 944 2560
E-mail	radstone@radstone.com

France

Téléphone	(1) 64.46.04.03
Fax	(1) 69.28.03.40

Taiwan

Telephone	(2) 218 5819 or 5829
Fax	(2) 218 6248

Australia

Telephone	(02) 874 9143
Fax	(02) 874 9150

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Appendix A - Specifications

This appendix gives a specification of the PPC60x. It also covers items such as the power requirements, the MTBF, the general measurements etc. and lists the available POPs.

VMEbus Compliance

The PPC60x conforms to the ANSI/VITA 1-1994 standard for VME64.

Master:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Slave:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Interrupt Handler:	D08(O), IH(1-7)
Interrupter:	I(1-7)
VMEbus Arbiter:	SGL, RRS, PRI, BCLR* generation
VMEbus Requester:	ROR, RWD Early BBSY* release Bus capture and hold
Bus Time-out Module:	16, 32, 64, 128, 256, 512, 1024 µS, disabled
Other Slot 1 Functions:	Slot 1 detector, IACK* daisy chain driver, SYSCLK Driver
Auto Slot ID:	VME64 specified and DY-4 proprietary

Local Resources

Processor	PowerPC 603 at 66 MHz or PowerPC 603e at 100 MHz or PowerPC 604 at 100 MHz
DRAM	8, 16, 32 or 64 Mbytes with ECC on-board. Further expansion to 128 Mbytes via a DRAM mezzanine module
L2 Cache	Up to 512 Kbytes (optional)
Flash boot ROM	512 Kbytes or 1 Mbyte in one or two 4 Mbit EPROMs or 5V programmable Flash ROMs in JEDEC standard 32-pin PLCC sockets
User Flash ROM	2 or 4 Mbytes of byte-wide 5V program
RTC/ NOVRAM	M48T18 RTC with 8Kx8 of battery backed NOVRAM
PCI	32-bit
SCSI	8-bit fast SCSI via the P2 connector
Ethernet	Ethernet or IEEE 802.3 (10Base5) via a front panel mounted AUI micro-D connector, via the P2 connector or via the front panel I/O adapter
PMC Slots	Two 5V, 32-bit IEEE P1386.1 compliant slots with front panel I/O. A further two 5V, 32-bit slots with front panel or P2 I/O on PCC
Audio	Business audio - 16-bit stereo CODEC. Connections via a front panel mounted 15-way micro-D connector (shared with the Keyboard and Mouse) or 3.5mm jacks on the front panel I/O adapter for: Stereo earphones output Stereo microphone input Stereo line-in Stereo line-out
Serial I/O	Two PC style COM ports via the P2 connector, two front panel mounted 9-way micro-D connectors or two 9-way D connectors on the front panel I/O adapter
Keyboard and Mouse	PS/2 compatible Keyboard and Mouse interface via the P2 connector, front panel mounted 15-way micro-D connector (shared with Audio) or 6-pin mini-DIN connectors on the front panel I/O adapter

Parallel I/O	Extended Capabilities port conforming to IEEE P1284 via the P2 connector	
Floppy Disk Interface	MFM 1.44/2.88 Mbyte. On-board 34-way header	
Counter/ Timers	Three independent 16-bit counter/timers with a resolution of 333ns. Two timers may be linked to form a 32-bit counter/timer	
Status LEDs	2 software programmable LEDs (0 - green and 1 - red) front panel mounted. 2 software programmable surface mount LEDs (LED203 and LED204) on the back of the board behind the front panel. 3 Ethernet status LEDs (LED200 to LED202) on the back of the board behind the front panel. 1 SCSI Activity LED (LED 205) on the back of the board behind the front panel.	
Operating Systems	Windows NT AIX 4 LynxOS VxWorks OS-9	4.0 4.x 2.2.2 5.3.x/Tornado
PCI Carrier	Compliance Slots I/O	PMC 2 Front panel or VME P2
PCI Graphics	Compliance Graphics processor VRAM I/O Miscellaneous	PMC Weitek P9100 2 or 4 Mbytes Front panel VGA connector Shared frame buffer interface
I/O Modules	P2 (3U mounting)	SCSI Two serial Parallel, Mouse and keyboard Ethernet/10Base5 10Base2
	Front panel (6U)	Audio, keyboard and mouse, Two serial
	Miscellaneous	P2 transition module (including 50-way SCSI header)

A

Power Requirements

	PPC603 8 Mbyte DRAM	PPC604 32 Mbyte DRAM	PPC604 64 Mbyte DRAM
+5 V +5 %,-2.5 %	4A	7A	7A
+12 V +5 %,-2.5 %	500mA	500mA	500mA
-12 V +5 %,-2.5 %	500mA	500mA	500mA

WARNING

Only use the PPC60x in backplanes that supply power on both the J1 and J2 connectors. Failure to observe this warning may result in damage to the board.

NOTE

Take care when using PMC modules as to how much current they require, especially from the +5V supply. The VME specification allows a maximum of 7.5 Amps to be drawn from the +5V supply in a single slot over the PPC603's specified operating temperature range. It may not be possible to support all combinations of L2 cache, DRAM and PMC modules within this limit.

EMC Regulatory Compliance and Safety

The PPC60x is designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptability.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

Environmental Specifications

Operating Environment

The PPC60x will operate under the following conditions:

Temperature range:	0 to +55°C ambient air temperature.
Cooling requirement:	A linear airflow of not less than 2.5 m/s across the board is recommended.
Relative humidity:	Up to 95% without condensation.
Thermal shock:	±5°C per minute.
Altitude:	-300 to +3000 meters (-1000 to + 10000 feet approximately).
Vibration:	10 to 100 Hz at 2 g acceleration.
Mechanical shock:	20 g for 6 ms (half sine) when mounted in a suitable racking system.

Storage Environment

The PPC60x may be stored or transported without damage within the following limits:

Temperature range:	-40 to +85°C.
Relative humidity:	Up to 95% without condensation.
Thermal shock:	±10°C per minute.
Altitude:	-300 to +16000 meters (-1000 to +50000 feet approximately).
Vibration:	10 to 500 Hz with 2 g acceleration.
Mechanical shock:	20 g for 6 ms (half sine).

Mean Time Between Failures

The calculated MTBFs for the PPC60x, for several example configurations, are shown in the table below. These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted PMC modules. The failure rates used in this calculation are based on MIL-HDBK-217F Notice 1 with commercial or non-military quality level and Ground Benign environment (at 25°C). Where a component did not comply with the MIL-HDBK, the closest equivalent, compliant component was used.

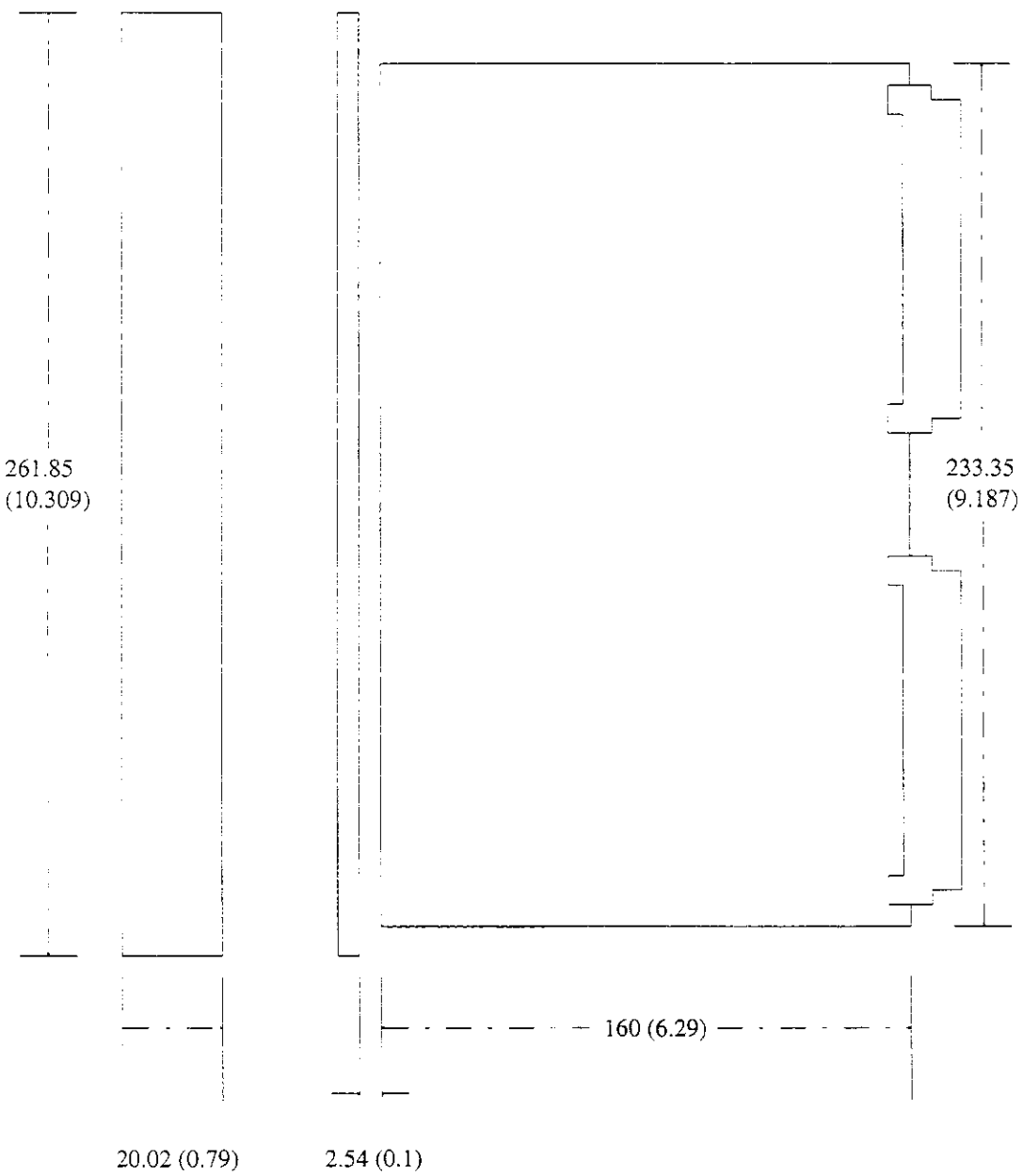
Processor	Configuration	MTBF (Hours)
PPC603	8 Mbyte DRAM, no L2 cache	35,891
PPC603e	8 Mbyte DRAM, no L2 cache	35,891
PPC604	32 Mbyte DRAM, 256 Kbyte L2 cache	30,000
PPC604	64 Mbyte DRAM, 256 Kbyte L2 cache	28,166

(see the Product Description section for an explanation of the above items)

Mechanical Construction

The PPC603 is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.

Figure A-1. VME Dimensions



Product Description

The order code is specified as PPC60x-yzz, where:

x can be 3, 3e or 4 to identify the PPC603, PPC603e or PPC604 processor respectively

y can be 0, 2 or 5 for 0, 256 or 512 Kbytes of L2 cache respectively. The preferred options are no L2 cache on PPC603 and PPC603e, and 256 Kbytes of L2 cache on PPC604

zz can be 08, 16, 32 or 64 to identify the amount of on-board EDC DRAM in Mbytes

Examples:

PPC603-008 = PPC603, no L2 cache, 8 Mbyte DRAM

PPC603e-232 = PPC603e, 256 Kbyte L2 cache, 32 Mbyte DRAM

PPC604-564 = PPC604, 512 Kbyte cache, 64 Mbyte DRAM

For other options, e.g. no VME interface, contact Radstone.

POPs

POP Code	Description
POPPPC-10	4 Mbytes of user Flash
POPPPC-15	32 Mbyte memory mezzanine
POPPPC-16	64 Mbyte memory mezzanine
POPPPC-20	I/O module bringing Ethernet, Keyboard, Mouse and two Serial channels through front panel.
POPPPC-21	Front panel I/O adapter module (FPX600).

See Appendix B for details of POPPPC-20 and POPPPC-21.

PCI Carrier Card

Order Code	Product Description
PCC/100	2 slot PMC carrier card

P2 I/O Modules (3U)

Order Code	Product Description
P2X600	P2 transition module
SIOX600 SIO2X600	Serial I/O, 25-way D-types Serial I/O, 9-way D-types
ETHX600	Ethernet AUI
10B5X600	10Base5 AUI
10B2X600	Cheapernet (10Base2)
PMKX600	Parallel and mouse/keyboard
SCSIX600 CENTX600	SCSI - Honda connector SCSI - Centronics connector
FKP2X600	Optional fixing kit

Front Panel Transition Module (6U)

Order Code	Product Description
FPX600	Mouse, keyboard, audio and two serial ports

PMC Modules

Order Code	Product Description
PMC9100/100	Graphics P9100, 2 Mbytes VRAM
PMC9100/200	Graphics P9100, 4 Mbytes VRAM
PMC9100/400	Graphics P9100, P9130 co-processor, 4 Mbytes VRAM

Operating Systems

Availability includes:

Windows NT 4.0
Solaris
AIX 4
LynxOS
VxWorks
OS-9
OS/2
pSOS
System 7

Contact Radstone for more details.

Appendix B - POPPPC-20 and POPPPC-21

This appendix describes POPPPC-20 and POPPPC-21, which are I/O modules.

Introduction

POPPPC-20 consists of a small I/O module with micro D-type connectors, and an associated front panel. The module fits over the P5 and P7 connectors on the PPC60x, bringing the signals out through the front panel via micro D-type connectors marked 'N1' (Ethernet/10Base5 AUI), 'S1' (COM1), 'S2' (COM2) and 'G1' (keyboard, mouse and audio).

WARNING

With POPPPC-20 fitted, do *not* connect the G1 (keyboard, mouse and audio) or N1 (Ethernet/10Base5 AUI) connectors to anything other than their intended, marked, interface, as damage to the board may otherwise result. Take care, when connecting Ethernet and Mouse/Keyboard cables, that they are plugged into the correct sockets.

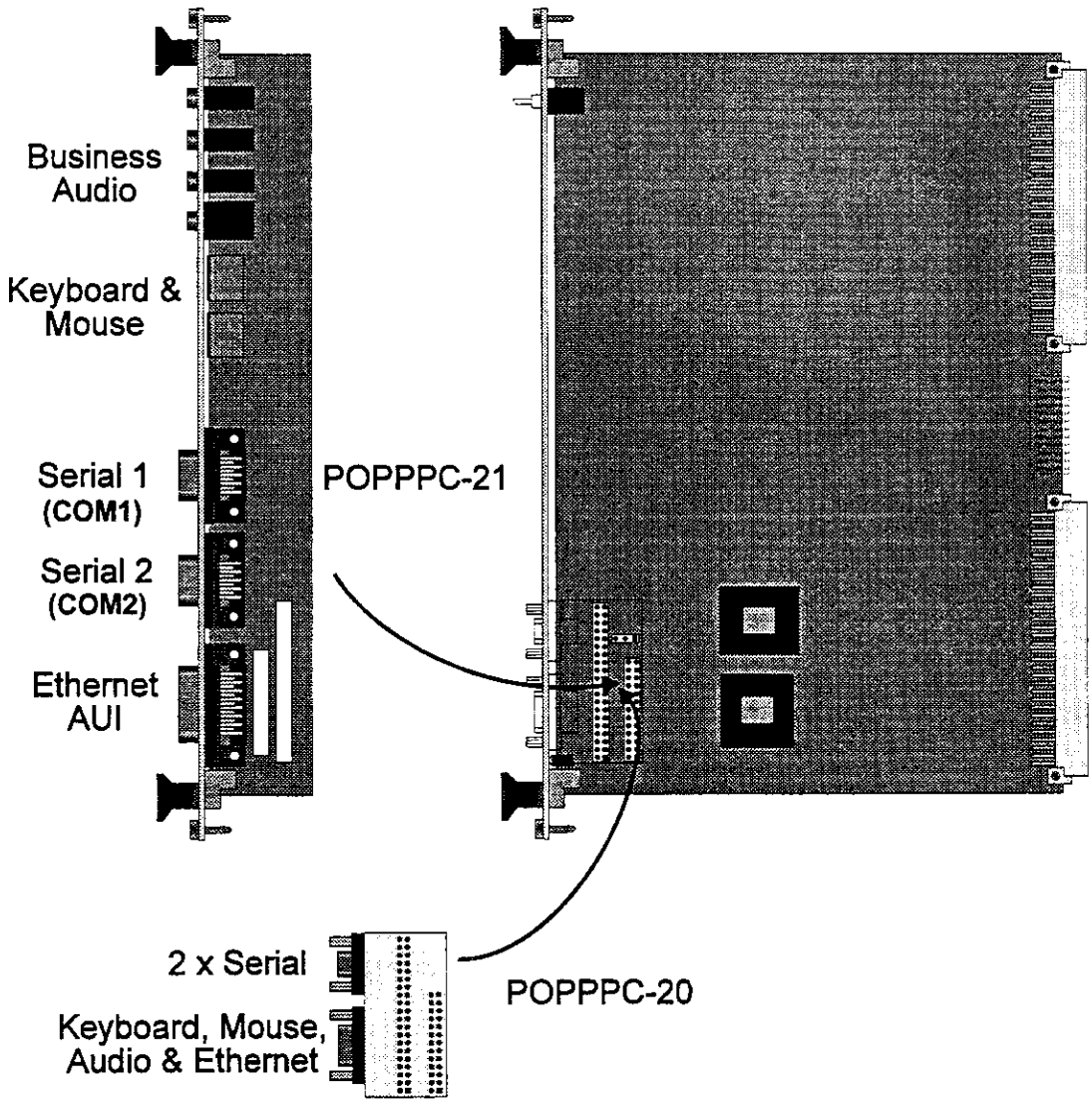
POPPPC-21 is a front panel module providing industry-standard connectors, as an alternative to the micro D-type connectors available using POPPPC-20. POPPPC-21 requires an extra system slot and, like the POPPPC-20, uses the P5 and P7 connectors on the PPC60x. If you order this module as POPPPC-21, then Radstone will factory fit it to the PPC60x. This module is also available as an X600 transition module, where it is called FPX600. If you order the module as FPX600, it will arrive as a kit of parts for you to fit to the PPC60x yourself (fully described in the X600 Modules User Guide, publication number RT5060).

NOTE

POPPPC-20 and POPPPC-21/FPX600 cannot both be fitted at the same time, as they both use the same P5 and P7 connectors.

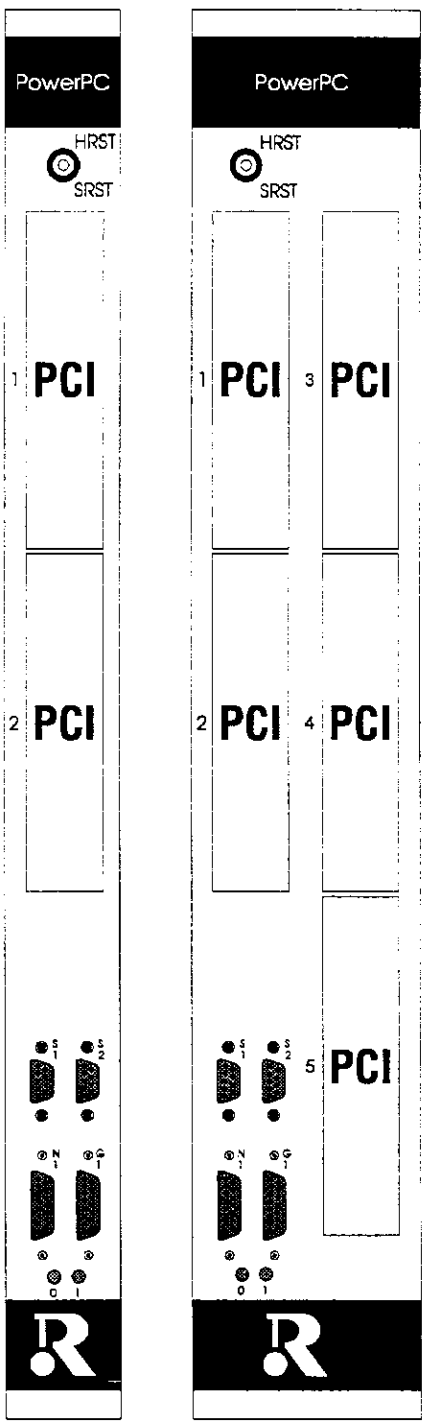
B

The following diagram shows how POPPPC-20 or POPPPC-21 fits onto the PPC60x.



POPPPC-20

The following diagram shows the PPC60x front panel with POPPPC-20 fitted.



Connectors

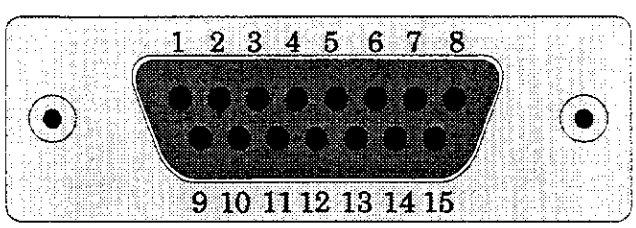
Ethernet/10Base5 AUI Connector (N1)

WARNING

Do *not* connect the N1 connector to anything other than its intended, marked, interface, as damage to the board may otherwise result. Take care, when connecting the Ethernet cable, that it is plugged into the correct socket.

This 15-way micro-D-type connector provides the Ethernet or IEEE 802.3 (10Base5) AUI for connection of a drop cable and has the following pinout. AUI Ground can be selected as signal ground (0V) for IEEE802.3 (10Base5), or chassis ground for Ethernet. See the AUI Ground Option (LK4) in Chapter 4.

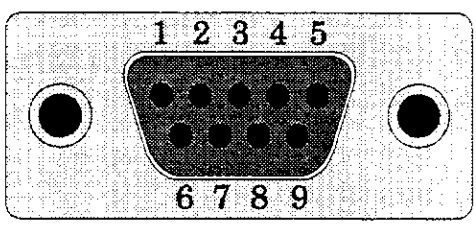
Pin	Signal
1	AUI Ground
2	Collision+
3	Transmit+
4	AUI Ground
5	Receive+
6	Signal Ground (0V)
7	Reserved
8	AUI Ground
9	Collision-
10	Transmit-
11	AUI Ground
12	Receive-
13	+12V fused 1A
14	AUI Ground
15	Reserved
Shell	Chassis Ground



Serial Connectors (S1 and S2)

These 9-way micro D-type connectors provide PC-style serial channels. They both have the following pinout:

Pin	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	Serial Ground
6	DSR
7	RTS
8	CTS
9	RI
Shell	Chassis Ground



Serial Ground is a quiet ground internally connected to 0V.

The S1 and S2 connectors are the serial channels more commonly referred to as COM1 and COM2 respectively.

NOTE

B

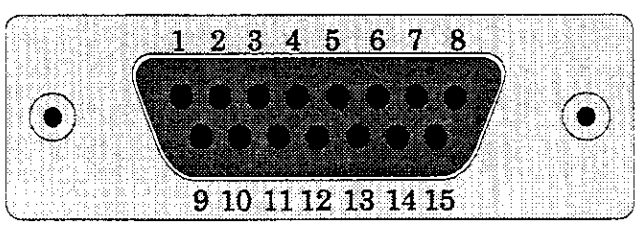
Keyboard, Audio and Mouse Connector (G1)

WARNING

Do *not* connect the G1 (keyboard, mouse and audio) connector to anything other than its intended, marked, interface, as damage to the board may otherwise result. Take care, when connecting the Mouse/Keyboard cable, that it is plugged into the correct socket.

The PS/2 Keyboard/Mouse interface and the Business Audio share a 15-way micro D-type connector that has the following pinout:

Pin	Signal
1	Left Microphone in
2	Audio Ground
3	Left Line in
4	Left Headphone out
5	Speaker
6	KBD Ground
7	MOUSE_DATA
8	KBD_DATA
9	Right Microphone in
10	Right Line in
11	Audio Ground
12	Right Headphone out
13	KBD_5V
14	MOUSE_CLK
15	KBD_CLK
Shell	Chassis Ground



Audio Ground is a quiet ground internally connected to 0V.

Signal Descriptions

Mnemonic	Description
Receive+/-	Ethernet receive data
Transmit+/-	Ethernet transmit data
Collision+/-	Ethernet collision
+12V	**12 Volts.** Fused at 1 Amp to power external Ethernet transceiver.
TXD	Transmit Data
RXD	Receive Data
RTS	Request-To-Send
RI	Ring Indicator
CTS	Clear-To-Send
DTR	Data Terminal Ready
DCD	Data Carrier Detect
DSR	Data Set Ready
MOUSE_CLK	**Mouse Clock.** Clock drive for mouse
MOUSE_DATA	**Mouse Data.** Mouse data line
KBD_5V	**Keyboard 5V.** Supplies power for the keyboard and mouse. Fused at 1 Amp
KBD_CLK	**Keyboard Clock.** Clock drive for the keyboard
KBD_DATA	**Keyboard Data.** Keyboard data line

Cables

The following cables are suitable for external connection to POPPPC-20:

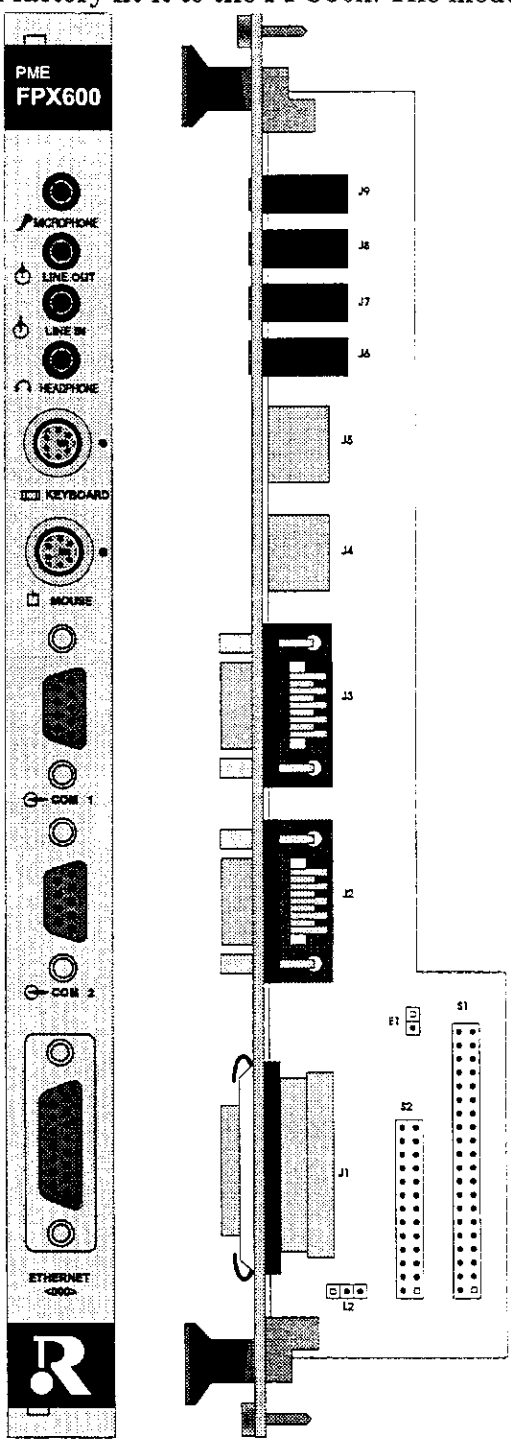
PPCMSE/D15/1 15-way micro D-type to PS/2 mouse and PS/2 keyboard cable. 1 meter long.

PPC232/D9/1 9-way micro D-type to standard 9-way D-type cable. 1 meter long.

PPCENET/D15/3 15-way micro D-type to standard 15-way D-type AUI cable. 3 meters long.

POPPPC-21

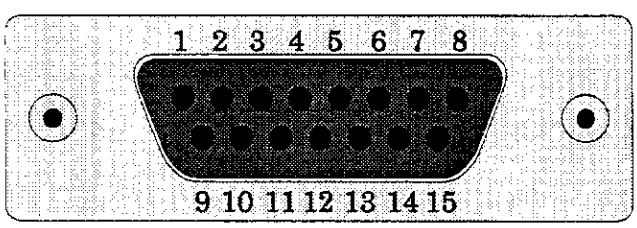
As mentioned previously, if this module is ordered as POPPPC-21, Radstone will factory fit it to the PPC60x. The module looks like:



Connectors

J1 (Ethernet/10Base5) Connector

Pin	Signal
1	AUI Ground
2	Collision+
3	Transmit+
4	**AUI Ground**
5	**Receive+**
6	**Signal Ground (0V)**
7	Reserved
8	AUI Ground
9	Collision-
10	**Transmit-**
11	**AUI Ground**
12	**Receive-**
13	12V Fused 1A
14	AUI Ground
15	Reserved
Shell	Chassis Ground



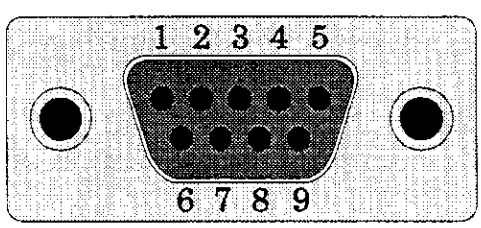
See the AUI Ground Connection Link section at the end of this appendix for more details.

J2 (COM2) Connector

Pin	Signal
1	DCD2
2	RXD2
3	TDX2
4	**DTR2**
5	**Signal Ground**
6	**DSR2**
7	RTS2
8	CTS2
9	RI2
Shell	Chassis Ground

J3 (COM1) Connector

Pin	Signal
1	DCD1
2	RXD1
3	TDX1
4	**DTR1**
5	**Signal Ground**
6	**DSR1**
7	RTS1
8	CTS1
9	RI1
Shell	Chassis Ground



J4 (PS/2 Mouse) Connector

Pin	Signal
1	MOUSE_DATA
2	Unused
3	KBD Ground
4	**KBD_5V**
5	**MOUSE_CLK**
6	**Unused**
Shell	Chassis Ground

J5 (PS/2 Keyboard) Connector

Pin	Signal
1	KBD_DATA
2	Unused
3	KBD Ground
4	**KBD_5V**
5	**KBD_CLK**
6	**Unused**
Shell	Chassis Ground

Audio Connectors

Headphones (J6)

Pin	Signal
1	Audio Ground
2	Left headphone out
3	Right headphone out

Line In (J7)

Pin	Signal
1	Audio Ground
2	Left line in
3	Right line in

Line Out (J8)

Pin	Signal
1	Audio Ground
2	Left line out
3	Right line out

Microphone (J9)

Pin	Signal
1	Audio Ground
2	Left microphone in
3	Right microphone in

Signal Descriptions

Mnemonic	Description
Receive+/-	Ethernet receive data
Transmit+/-	Ethernet transmit data
Collision+/-	Ethernet collision
+12V	**12 Volts.** Fused at 1 Amp to power external Ethernet transceiver. Also used by P2 adaptor
TXDn	COMn Transmit Data
RXDn	COMn Receive Data
RTSn	COMn Request-To-Send
RIn	COMn Ring Indicator
CTSn	COMn Clear-To-Send
DTRn	COMn Data Terminal Ready
DCDn	COMn Data Carrier Detect
DSRn	COMn Data Set Ready
MOUSE_CLK	**Mouse Clock.** Clock drive for mouse
MOUSE_DATA	**Mouse Data.** Mouse data line
KBD_5V	**Keyboard 5V.** Supplies power for the keyboard and mouse. Fused at 1 Amp
KBD_CLK	**Keyboard Clock.** Clock drive for the keyboard
KBD_DATA	**Keyboard Data.** Keyboard data line

Links

Speaker Header (E1)

THIS IS NOT A LINK, but two pins for connecting a speaker (it is sometimes also called 'SPK').

Pin 1 = Speaker

Pin 2 = Speaker Ground

AUI Ground Connection Link (L2)

With the FPX600/POPPPC-21 fitted, LK4 on the PPC60x host board can be difficult to access, so its function is replicated by L2 on the FPX600/POPPPC-21.

If POPPPC-21 is factory fitted, LK4 on the PPC60x host board is not fitted by default, meaning that this L2 link decides the AUI Ground setting.

If you fit FPX600 yourself, then it is your decision as to whether to use LK4 or L2 (although if you are ever likely to want to change between 10Base5 and Ethernet operation, then L2 is the more accessible link). Whichever you choose, ***DO NOT* use *BOTH* links**.

Out = Use the LK4 setting on the PPC60x

Pin 1 to pin 2 = AUI Ground connected to signal ground (10Base5)

Pin 2 to pin 3 = AUI Ground connected to chassis ground (Ethernet)

Pin 1 to pin 3 is not a valid linking combination.

Glossary

Note: The VMEbus signals are explained in chapter 5

3D
Three dimensional.

A16
Providing or decoding addresses on **VMEbus** address lines A01 to A15.

A24
Providing or decoding addresses on **VMEbus** address lines A01 to A23.

A32
Providing or decoding addresses on **VMEbus** address lines A01 to A31.

A64
Providing or decoding addresses on **VMEbus** address lines A01 to A31.

AC
Alternating Current.

ADO
ADdress Only cycle on the **VMEbus**.

ADOH
ADdress Only Handshake cycle on the **VMEbus**.

AIX
Advanced Interactive Executive from **IBM**.

AMD
Advanced Micro Devices. A chip manufacturer.

ANSI
American National Standards Institute.

API
Application Program Interface.

Arbiter
An arbiter accepts requests and grants control to one **requester** at a time.

ARPA
The US Defence Advanced Research Projects Agency.

ASCII
American Standard Code for Information Interchange. A 7-bit code, established by ANSI, to achieve compatibility between data services. Equivalent to the international **ISO** 7-bit code.

ATM
Asynchronous Transfer Mode.

AUI
Attachment Unit Interface. The cable that connects the **DTE** to the **MAU**. Also called the **Drop Cable**.

Backplane (VMEbus)
A **PCB** with 96-pin connectors and signal paths that bus the connected pins. Some systems have a single PCB, called the J1 backplane. This provides the signal paths needed for basic operation. Other systems also have a second PCB, called the J2 backplane. This provides the additional 96-pin connectors and signal paths needed for wider data and address transfers. The J1 and J2 sections may be combined into a single J1/J2 backplane PCB.

Bandwidth
The bandwidth is the amount of a resource that is available (or the amount that is used). For a network or bus, the bandwidth is the maximum amount of data that could be transferred in 1 second.

BBSY
Bus Busy.

BCLR
Bus Clear.

BERR
Bus ERRor.

Big-endian
Refers to the way in which multi-byte data is stored in memory. Big-endian data is stored with the most significant byte at the lowest address (68XXX style). See also **Little-endian**.

BIOS
The Basic **I/O** System featured in most **PC**s.

BLT
BLock Transfer.

BSD
Berkley Standard/Software Distribution.

BSP
Board Support Package.

BTO
The **VMEbus** Bus Time Out period. See **Timeout**.

Byte
An 8-bit data structure.

C2
A set of security policies that define how a system operates. C2 is discretionary access control, and means that users of the system own objects, control protection of those objects and are accountable for access to those objects.

Cache
A small, fast access memory between the processor and the larger, slower main memory. Used to store the most recently used instructions/data to improve overall memory access time.

Chassis
See **enclosure**.

Chassis Ground
Most applications require the chassis to be connected to earth, normally via a mains cable or separate earthing strap.

CIO
Counter/timer and parallel I/O. The 85C36 device on the **PPC60x** is a CIO.

CMC
Common Mezzanine Card.

CN
Connector.

CODEC
Coder-Decoder.

CPU
Central Processing Unit.

CR/CSR
Configuration ROM/Control and Status Register.

CSMA/CD
Carrier Sense, Multiple Access with Collision Detect. The three basic steps for accessing **Ethernet**.

CTS
Clear To Send. A serial signal. See **RTS**.

D64
Sending and receiving data 64 bits at a time over D00 to D31 on the **VMEbus**.

D32
Sending and receiving data 32 bits at a time over D00 to D31 on the **VMEbus**.

D16
Sending and receiving data 16 bits at a time over D00 to D15 on the **VMEbus**.

D08(EO)
Sending and receiving data 8 bits at a time over D00 to D07 or D08 to D15 on the **VMEbus**.

D08(O)
Sending and receiving Status/**ID** 8 bits at a time over D00 to D07 on the **VMEbus**.

Daisy Chain
A signal line that propagates a signal from board to board (or chip to chip), starting with the first slot and ending at the last slot. There are 4 **VMEbus** grant daisy chains and one VMEbus interrupt acknowledge daisy chain.

DC
Direct Current.

DCD
Data Carrier Detect. A serial signal.

DEC
Digital Equipment Corporation. An **OEM**.

Determinism
The ability of a system to respond to a repeated sequence of events or actions in exactly the same way and with the same results each time.

DIN
Deutsches Industrie Norm. A German standard.

Disk Mirroring
Two disk drives storing identical information, so that one is the mirror of the other. This gives better fault tolerance but halves the storage capacity of the disks.

DLC
Data Link Control (protocol). An **IBM** protocol.

DMA
Direct Memory Access. A direct, rapid link between a peripheral and main memory that avoids the use of the processor to transfer each item of data.

Double-word
A 64-bit structure.

DRAM
Dynamic **RAM**. Memory that must be refreshed periodically to maintain the storage of information.

Drop Cable
The cable that connects the **DTE** to the **MAU**. See **AUI**.

DSR
Data Set Ready. A serial signal.

DTE
Data Terminal Equipment. The data terminal devices themselves. A category that includes the computer.

DTR
Data Terminal Ready. A serial signal.

D-type
A connector that has the approximate shape of a capital letter 'D'.

E^2PROM (or EEPROM)
Electrically Erasable **PROM**. PROM whose contents can be erased electrically, so allowing the device to be re-used with new data.

ECC
Error Correction Coding.

ECP
Enhanced Capabilities Port.

EDO
Extended Data Out. EDO DRAM is similar to normal DRAM except that the data remains on the output pins longer, so giving the accessing device longer to read it.

EMC
Electro-Magnetic Compatibility.

Enclosure
A rigid framework that provides mechanical support for boards inserted into the **backplane**, ensuring that the connectors mate properly and that adjacent boards do not touch each other. It also guides the cooling airflow through the system and ensures that inserted boards do not disengage themselves from the backplane due to vibration or shock.

EPLD
Electrically Programmable Logic Device.

EPP
Enhanced Parallel Port.

EPROM
Erasable **PROM**. PROM whose contents can be erased through exposure to ultra-violet light, so allowing the device to be re-used with new data.

ESD
Electrostatic Sensitive Device.

Ethernet
Ethernet is a baseband, thick-wire network based on an access method called **CSMA/CD**. It was originally developed by the Xerox Corporation in 1972.

FDC
Floppy Disk Controller.

FDDI
Fiber Distributed Data Interface. A standard for fiber optic cable data transmission.

FIFO
First In First Out. A data queuing mechanism (or the implementation of it) in which the first item stored is the first item processed.

Flash Memory
A type of high-capacity **E^2PROM**.

FPU
Floating Point Unit.

FTP
File Transfer Protocol. See **TCP/IP**.

GL
Graphics Language.

GND
The Ground (0V) signal or supply rail.

GUI
Graphical User Interface. A user interface portrayed graphically (e.g. as icons, windows etc.) instead of using command lines.

Half-word
In PowerPC terminology, a 16-bit structure. Cf **word, longword**.

Handler
See **Interrupt Handler.**

I(x-y)
The **interrupter** can generate interrupt requests on **VMEbus** lines IRQx* to IRQy*.

IBM
International Business Machines. An **OEM**.

ID
Identification.

IDE
Integrated Drive Electronics.

IEEE
Institute of Electrical and Electronic Engineers.

IH(x-y)
The **interrupt handler** can generate interrupt acknowledge cycles in response to interrupt requests on **VMEbus** lines IRQx* to IRQy*.

Interrupter
An interrupter generates an interrupt request on the **VMEbus** and then provides status/**ID** information when requested by the **interrupt handler**.

Interrupt Handler
An interrupt handler detects interrupt requests on the **VMEbus**, generated by **interrupters**. It acknowledges these requests with an IACK* and responds to them by requesting Status/**ID** information.

I/O
Input/Output.

IPX/SPX
Internetwork Packet Exchange/Sequenced Packet Exchange from Novell.

ISA
Industry Standard Architecture.

ISDN
Integrated Services Digital Network.

ISO
International Standards Organisation.

JEDEC
Joint Electronic Devices Engineering Committee.

JTAG
Joint Test Action Group. A standard for board-level testing.

KBD
Keyboard.

L1 Cache
First-level **cache**.

L2 Cache
Second-level **cache**.

LAN
Local Area Network.

LCK
Lock.

LED
Light Emitting Diode. A semiconductor diode that radiates light. LEDs that emit in the visible region are used as indicators or warnings.

Little-endian
Refers to the way in which multi-byte data is stored in memory. Little-endian data is stored with the least significant byte at the lowest address. See also **Big-endian**.

Longword
A 32-bit data structure in **VME** systems. Cf **word, halfword**.

LSB
Least Significant Bit.

Master
A **VMEbus** master initiates bus cycles to transfer data between itself and a **slave** module.

MAU
Medium Access Unit or Media Attachment Unit. The transceiver unit which interfaces with the network medium.

MBLT
Multiplexed BLock Transfer.

Mezzanine
The American term for a daughter board.

MIDI
Musical Instrument Digital Interface.

MMU
Memory Management Unit.

MSB
Most Significant Bit.

MTBF
Mean Time Between Failures.

NetBEUI
Network **BIOS** Extended User Interface from IBM.

NFS
Network File Server.

Nibble
4 bits. So called because it's half a byte (honestly!).

NMI
Non-Maskable Interrupt.

NOVRAM
Non-volatile **RAM**. Memory that does not lose its information when powered down.

OEM
Original Equipment Manufacturer.

PC
Personal Computer.

PCB
Printed Circuit Board.

PCC
PMC Carrier Card.

PCI
Peripheral Component Interconnect.

PCMCIA
PC Memory Card Interface Adaptor (also People Can't Memorize Computer Industry Acronyms).

PLCC
Plastic Leadless Chip Carrier.

PLD
Programmable Logic Device.

PMC
PCI Mezzanine Card.

POP
Processor OPtion.

POR
Power On Reset.

POSIX
Portable Operating System Environment. An IEEE standard.

PPC60x
Radstone's PowerPC-based processor card. The PPC603 is based on the PowerPC 603 processor and the PPC604 is based on the the higher-specified PowerPC 604 processor, otherwise they are functionally equivalent.

Pre-emptive

A multi-tasking mechanism whereby tasks are (re)scheduled at regular intervals based on priority and external events, rather than the task being able to run to completion or some defined suspension point before the next task is scheduled (which is called co-operative). The unit of time between rescheduling is a fixed interval called a time slice.

PReP

PowerPC Reference Platform. An example implementation of a philosophy designed to allow 100% binary compatibility across different platforms, when based on the PowerPC processor.

PRI

Prioritised. A **VMEbus arbiter** that prioritises the four VMEbus request lines from BR0* (the lowest) to BR3* (the highest) and responds with BG0IN* to BG3IN*. It also informs the VMEbus **master** when there is a higher level request than that being processed, by driving BCLR* low.

PROM

Programmable **ROM**. A program in a PROM is electronically 'hard-wired', and once the program is inserted into the PROM, it cannot be altered without using a new PROM.

PS/2

Programming System 2 from **IBM**.

RAID

Redundant Arrays of Independent Disks/Drives.

RAM

Random Access Memory. Memory that can be read from or written to at any time.

Requester

A **VMEbus** requester requests use of the VMEbus when it is required by a **master**.

RI

Ring Indicator. A serial signal.

RISC

Reduced Instruction Set Computer. The basic principle is to have a small set of simple instructions that execute very quickly (i.e. in one cycle). This means that programs are longer, and sometimes more complicated, but run faster.

Rlogin

Remote Login.

RMW

Read Modify Write. An indivisible **VMEbus** cycle that is used to both read from and write to a **slave** without permitting any other **master** to access that slave during the cycle. This is most useful in multiprocessing systems where certain memory locations are used to control access to certain resources (e.g. semaphores).

ROM

Read Only Memory. Semiconductor memory whose components are not alterable by computer instructions.

ROR

Release On Request. An access scheme in which the **VMEbus requester** only relinquishes control of the bus when it is required by another requester. This has an advantage over the **RWD** scheme in that if no other **master** uses the bus, the bus request phase of a transfer is avoided.

RPC

Remote Procedure Call.

RRS

Round Robin Select. Round robin is a **VMEbus** arbitration scheme for resources in which resource **bandwidth** is shared equally between competing requests. A requester that is granted a resource on one arbitration cycle has the lowest priority on the next arbitration cycle.

RS232(C)

The normal serial interface found in most **PC**s and terminals. It usually uses a 9 or 25 pin connector.

rsh

Remote shell.

RTS
Ready To Send. A serial signal. See **CTS**.

RTC
Real Time Clock.

RWD
Release When Done. A **VMEbus** access scheme in which the **requester** relinquishes control of the bus as soon as it has finished a single data transfer cycle. This loses out to the **ROR** scheme during multiple accesses to an otherwise unused bus, as it has to request the bus each time.

RXD
Receive Data. A serial signal.

SCSI
Small Computer Systems Interface. A standard and associated hardware for general purpose communication (usually) between a processor and large capacity storage devices.

SGL
Single Level. A **VMEbus arbiter** that only responds to bus requests on BR3*. This relies on the bus request **daisy chain** to arbitrate between requests.

SIO
System I/O.

SIOP
SCSI I/O Processor.

Slave
A slave detects **VMEbus** cycles initiated by a **master** and, when these cycles specify its participation, transfers data between itself and the master.

Slot
A position where a board can be inserted into a **backplane**. If the system has both a J1 and a J2 backplane (or a combination J1/J2 backplane), each slot provides a pair of 96-pin connectors.

SMI
System Management Interrupt.

SNMP
Simple Network Management Protocol.

Socket
A communications endpoint that can be addressed, or a connection between two processes.

SPARC
Scalable Processor ARChitecture.

SPECint92
A benchmark package, produced in 1992, measuring the integer performance of a processor.

SPECfp92
A benchmark package, produced in 1992, measuring the floating point performance of a processor.

Superscalar
A superscalar processor is a processor with multiple execution units that *may* operate in parallel.

System Controller
A board in **slot** 1 of the **VMEbus backplane**. It must have a SYSCLK driver, an **arbiter**, an IACK **daisy chain** driver and a bus timer.

TBA
To Be Announced.

TCP/IP

Transport Control Protocol/Internet Protocol. A collection of network protocols that together support host-to-host communication for hosts connected to any of a number of heterogeneous networks.

Network Layer Protocols (ISO Level 3)

IP	Provides internet transaction services for Layer 4 clients. Generally considered as providing Host-to-Host datagram delivery.

Transport Layer Protocols (ISO Layer 4)

TCP	A connection oriented reliable byte-stream protocol.
UDP	An unacknowledged transaction-oriented protocol parallel to TCP

Session, Presentation and Application Layer Protocols (ISO Layers 5 to 7)

FTP	Permits exchange of complete files between computers.
Telnet	Provides virtual terminal services for interactive access by terminal servers to hosts.

TEA

Transfer Error Acknowledge.

Telnet

The ARPA application level protocol. A bi-directional, **byte**-oriented communications protocol. See **TCP/IP**.

Timeout

The elapsing of a period of time within which an action should have happened.

TOD

Time-Of-Day.

Transceiver

A combination of a transmitter and a receiver.

TXD

Transmit Data. A serial signal.

U

The U is a standard unit of height measurement (e.g. 3U). One U is 4.445 centimetres (1.75 inches).

UAT

Unaligned Address Transfer. A **VMEbus** data transfer cycle that sends or receives data in an unaligned fashion.

UDP

User Datagram Protocol. See TCP/IP.

VCC

The five volt supply rail.

VITA

VFEA (VMEbus and Futurebus Extended Architecture) International Trade Association.

VME

Versa Module Europe. Often used as an abbreviation for **VMEbus**.

VMEbus

An **ANSI/VITA** standard (1-1994) for a versatile backplane bus based on the Eurocard mechanical standard.

WABI

Windows Application Binary Interface

Word

In PowerPC terminology, a 32-bit structure. Also often refers to a 16-bit data structure in **VME** systems. Cf **halfword, longword.**

Write Posting

This is a pipelining technique that can be used by the VME interface chip to increase system performance.

In *Master Write Posting*, when a local bus **master** writes to the **VMEbus**, instead of requesting and arbitrating for the bus, transferring data to the slave and waiting for the acknowledgement, the VME interface chip acknowledges the local bus master immediately and captures the address and data to write. The local bus master can then continue with its processing and the VME interface chip requests the VMEbus and transfers the data for the host.

Slave Write Posting works in a similar way. Write operations to the VME interface chip as a VME **slave** do not wait for the chip to become local bus master, write the data to the host memory and wait for its acknowledge. The VME interface chip acknowledges immediately and captures the address and data to write. Another transfer can then take place on the VMEbus while the VME interface chip writes the data from the previous one.

X11R5

Release 5 of version 11 of the X Windows System.

X.25

An interface between **DTE** and DCE for terminals operating in packet mode on public data networks.

Index

This appendix only lists the page numbers of the main occurences of the index items. There may be other occurences of the index item in the preceeding or subsequent pages.

C

D

E

F

I

J

K

L

M

N

O

P

R

S

T

U

V

W

Blank Page