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Dual High Resolution Graphics Controller

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VCQ-M
and VFG-M

Graphics Boards User's Manual

Rastergraf

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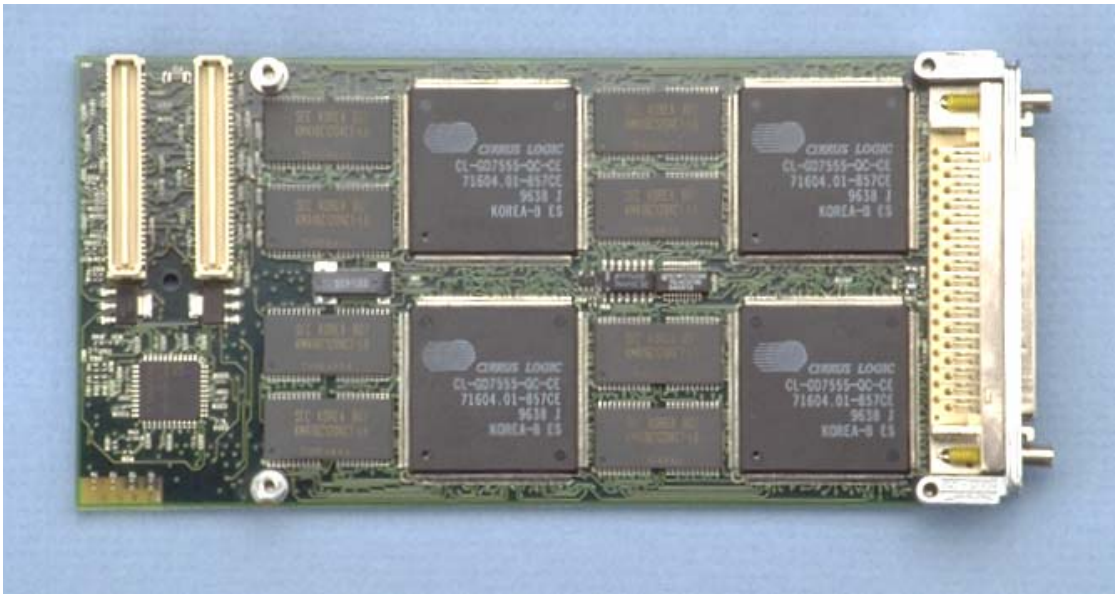

Introduction

This manual provides information about how to configure, install, and program the Rastergraf **VCQ-M** and **VFG-M** PMC (**P**CI **M**ezzanine **C**ard) graphics controllers.

This manual is broken down into four chapters:

Chapter 1: Overview
Chapter 2: Installation
Chapter 3: Programming On-board Devices and Memories
Chapter 4: Troubleshooting

Chapter 1 provides background material about the graphics boards. Understanding the information in the chapter, however, is not essential for the hardware or software installation.

If you want to perform the installation as quickly as possible, start with Chapter 2. If you have problems installing the hardware, refer to Chapter 4 or contact Rastergraf Technical Support for help.

Getting Help

This installation manual gives specific steps to take to install your Rastergraf display board. There are, however, variables specific to your computer configuration and monitor that this manual cannot address. Normally, the default values given in this manual will work. If you have trouble installing or configuring your system, first read Chapter 4, “Troubleshooting”. If this information does not enable you to solve your problems, do one of the following:

1) call Rastergraf technical support at (541) 923-5530,

2) fax your questions to (541) 923-6475,

3) or send E-mail to ***support@rastergraf.com***.

If your problem is monitor related, Rastergraf technical support will need detailed information about your monitor.

Board Revisions

This manual applies to the following board revision levels:

VCQ-M Fab Rev 0, 1
VFG-M Fab Rev 0, 1

Notices

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The information in this document is subject to change without notice. The specifications of the VCQ-M, VFG-M, and other components described in this manual are subject to change without notice. Although it regrets them, Rastergraf, Inc. assumes no responsibility for any errors or omissions that may occur in this manual.

Rastergraf, Inc. assumes no responsibility for the use or reliability of software or hardware that is not supplied by Rastergraf, or which has not been installed in accordance with this manual.

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The VCQ-M and VFG-M are manufactured and sold under license from Curtiss-Wright Controls Embedded Computing. Contact Rastergraf, Inc. for additional information.

Manual Revisions

Revision 1.0 May 25, 2001	New. Combine VCQ/VQP and VFG manuals
	Removed digital/LVDS references, Software chapter, other minor changes and updates.
	Added cautionary note that Windows support is for single monitor, no video input only.
Revision 1.1 June 13, 2001	Minor corrections
Revision 2.0 October 24, 2006	Minor corrections. Convert to Rastergraf manual. Delete VQP-M.

Conventions Used In This Manual

The following list summarizes the conventions used throughout this manual.

`Code fragments`	Code fragments, file, directory or path names and user/computer dialogs in the manual are presented in the `courier` typeface.
Commands or **program names**	Commands, or the names of executable programs, except those in code fragments, are in bold.
System prompts and commands	Commands in code fragments are preceded by the system prompt, a percentage sign (%), the standard prompt in UNIX's C shell or the hash-mark (#), the standard UNIX prompt for the Super-User.
Keyboard usage	**<CR>** stands for the key on your keyboard labeled "RETURN" or "ENTER"

Note	Note boxes contain information either specific to one or more platforms, or interesting, background information that is not essential to the installation.

Caution	Caution boxes warn you about actions that can cause damage to your computer or its software.

Warning!	Warning! boxes warn you about actions that can cause bodily or emotional harm.

Chapter 1
General Information

1.1 Introduction

The Rastergraf **VCQ-M** is a single board PMC graphics display controller. It has a two channel USB controller and four medium performance Cirrus Logic CL-GD7555 Matterhorn XVGA/SVGA compatible 64-bit graphics accelerators.

Display Channel A can function as the system VGA controller with an on-board flash PROM for VGA BIOS or OpenBoot FCode. In all other respects, the other channels are identical, and all are independent of each others. The USB and CL-GD7555s are isolated from the host PMC bus by a Texas Instruments PCI2031 PCI-PCI bridge.

The **VFG-M** is identical to the VCQ-M except that two display channels (CL-GD7555) have been replaced by Conexant Bt848A video digitizers.

A **VCQ-M** or **VFG-M** can be used in a PCI or CompactPCI bus machine by using it with a PMC to PCI or PMC to CPCI adapter board.

This chapter provides an overview of the VCQ-M and VFG-M graphics controllers. Additional sections contain a bibliography, specifications, monitor requirements, and common configurations. Installation procedures are contained in Chapter 2.

More information about Rastergraf's products can be obtained by contacting the factory or consulting Rastergraf's web page at http://www.rastergraf.com.

1.2 Functional Description

The feature set of the VCQ-M and VFG-M includes:

- **VCQ-M**: four 64-bit 50 MHz Cirrus Graphics CL-GD7555
- **VFG-M**: two 64-bit 50 MHz Cirrus Graphics CL-GD7555 plus two Conexant Bt848A Video Digitizers
- Channel 1 supports PC Compatible VGA
- Each channel is ***completely*** independent of the others
- Texas Instruments PCI2031 Transparent PCI to PCI bridge
- 2 Kb serial EEPROM
- 64 KB Flash PROM
- Up to 1280 x 1024 displayable resolution
- 16 bit overlay (when running 16 or 32 bit/pixel display)
- 4 MB/channel high speed DRAM supports multiple display pages
- Hardware pan and scroll and bitmapped cursors
- PLL controlled pixel clock
- Non-interlaced and high refresh rate displays
- Three status LEDs (controlled by host software)
- PMC single-wide module
  Single 68-pin 3M Micro-ribbon connector supplies video out and USB
- Two OPTi 82C861 USB 1.1 ports

Available software includes:

- Graphics Subroutine Package with OpenGL support
- Rastergraf custom loadable DDX module for Solaris
- Rastergraf Xvgp X Window Servers for RTOS and Linux
- Windows NT/2K/XP driver - single monitor only, no video input support
- SPARC FCode
- PC compatible VGA BIOS

1.2.1 Cirrus CL-GD7555 Graphics Controller

The Cirrus Logic ***Matterhorn CL-GD7555*** (7555) is a 64-bit graphics controller with accelerated 2D patterned lines and BLT engine, which can yield performance in excess of 30M Winmarks. Its video-color adjustment and scaling engine with EST (edge sharpening technology) provides excellent video performance.

Key Device Features:

- High speed 64-bit graphic processor with line and pattern acceleration
- Integrated VGA
- Integrated display controller
- Primary and color-key Video Overlay displays
- Integrated Color space converter
- Directly supports 8, 16, 24 bits per pixel
- Two Operand BitBLT
- Scaling with X and Y interpolation
- Interrupts from the raster line counter and the drawing completion
- 4 MB of high speed EDO DRAM memory for each display
- Dual buffers allow one command to be executed while loading another
- 33 MHz, 32-bit PCI 2.1 host interface clock
- .5 micron 3.3/5 volt CMOS custom ASIC process
- 256 fine pitch PQFP (Plastic Quad Flat Package)

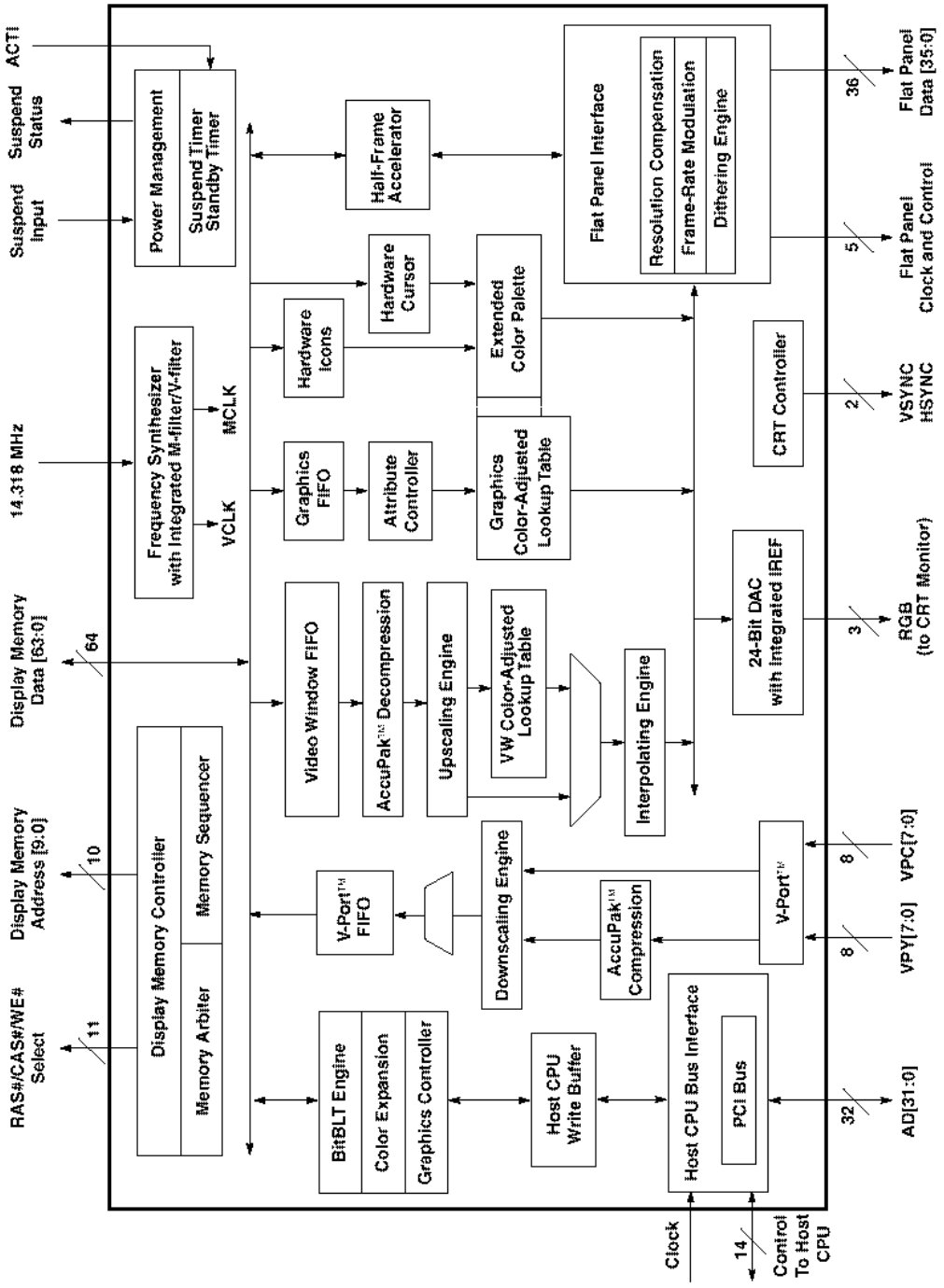
The CL-GD7555 supports 8-bit, 16-bit, and packed 24-bit true color modes and mapped RGB and YUV color formats. The CL-GD7555 includes a color-keyed overlay capability and includes a graphics cursor with a 64 x 64 x 2 bit map.

Programmable timing and control registers control the video timing, supporting up to 75 Hz vertical and up to 80 kHz horizontal refresh rates. Both interlaced and non-interlaced formats are supported. Display formats range from 640 x 480 to 1280 x 1024.

The video output is directed through an integral RAMDAC. Optional color space conversion allows data to be stored in the more efficient YUV format. It translates the primary, overlay, and 2-bit cursor pixels into 24-bit color values (8 bits each of red, green, and blue).

The boards are available with RGBHV VGA compatible analog video output which can drive a standard multi-sync monitor. On the VCQ-M and VFG-M DDC (display data channel) lines are supplied so that the monitor can be controlled by the host computer.

Figure 1-1 CL-GD7555 Block Diagram



1.2.2 USB Hub Controller

The **VCQ-M** and **VFG-M** have an OPTi 82C861 FireLink USB 1.1 compliant two channel USB hub controller which can be used to interface with devices such as mouse, trackball, keyboard, scanner, and video.

1.2.3 Video Input Digitizers (VFG-M)

The VFG-M provides video input capability, using the Conexant (Brooktree) Bt848A. On a single device, the Bt848A integrates 4-input multiplexer, an NTSC/PAL/SECAM composite and S-Video decoder, scaler, DMA controller, and PCI bus master. The Bt848A can place video data directly into CPU (host) memory for video capture applications and into the Cirrus video display frame buffer for video overlay applications. As a PCI initiator, the Bt848A can take control of the PCI bus as soon as it is available, thereby avoiding the need for on-board frame buffers. The Bt848A contains a small pixel data FIFO to decouple the high-speed PCI bus from the continuous video data stream.

The video data input may be scaled, color translated, and burst transferred to a target location on a field basis. This allows for simultaneous preview of one field and capture of the other field. Alternatively, the Bt848A is able to capture or preview both fields simultaneously. The fields may be interlaced into memory or sent to separate field buffers.

Each Bt848A is connected to its corresponding Cirrus chip via a ZoomVideo (ZV) port which enables the Bt848A to drive video data directly into display memory. Due to memory speed limitations, the ZV port input method is suitable for display resolutions of less than 1024 x 768 when using a full 640 x 480 x 15 bpp video input window.

For higher display resolutions (up to 1280 x 1024 x 16 bpp), an alternative method is used: using its PCI bus master (DMA) capability, the Bt848A transfers video data into the Cirrus over the VFG-M's local PCI bus. Moreover, using this method, both Bt848As can transfer data into one Cirrus chip, providing two full 640 x 480 video windows on one screen.

1.2.4 Board Connections

All connections are made through the front panel 68-pin high density connector. A special cable assembly splits out the monitor (RGBHV and DDC, video input (VFG only) and USB functions into separate cables.

1.2.5 Software Support

Rastergraf software support is available for many operating systems and includes:

- SDL Graphics Library Package supports multiple displays and video input on Linux and VxWorks systems;
- Windows NT/2K/XP Driver supports the graphics boards but just for a single monitor and with no video input support;
- On board Flash BIOS contains VGA BIOS or OpenBoot Fcode;
- X Windows X11R6 Server with hardware specific optimizations and multi-head support. A custom loadable DDX version is available for Solaris.
- USB support is available in Windows 2K/XP, Solaris, and Linux.

Figure 1-2 VCQ-M Block Diagram

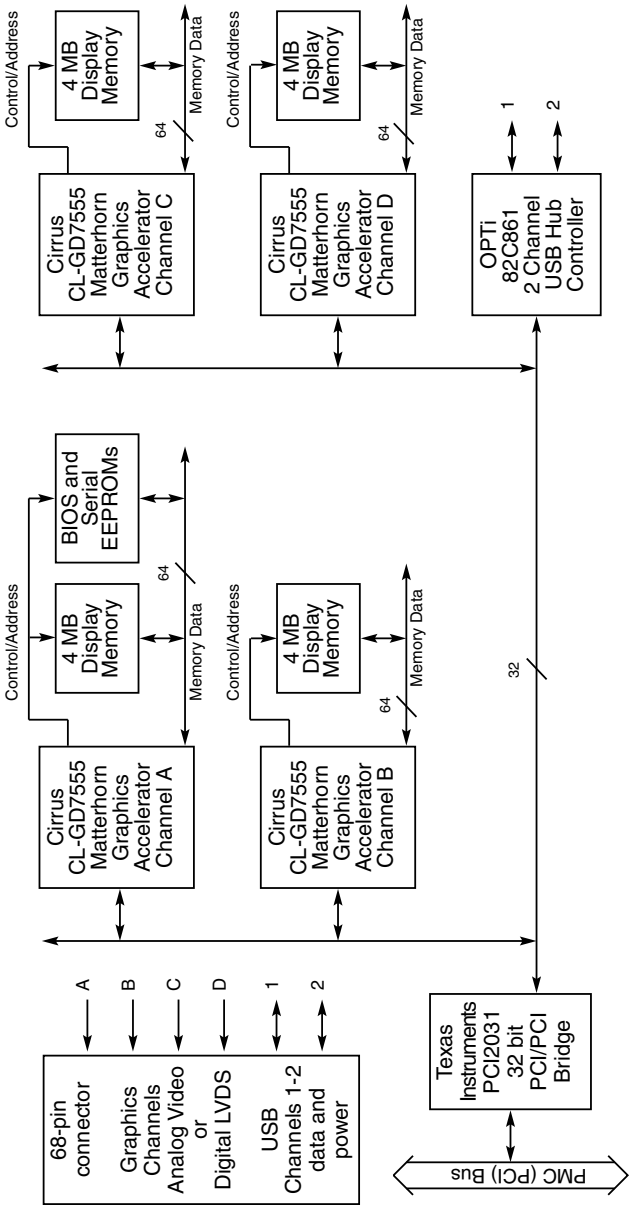
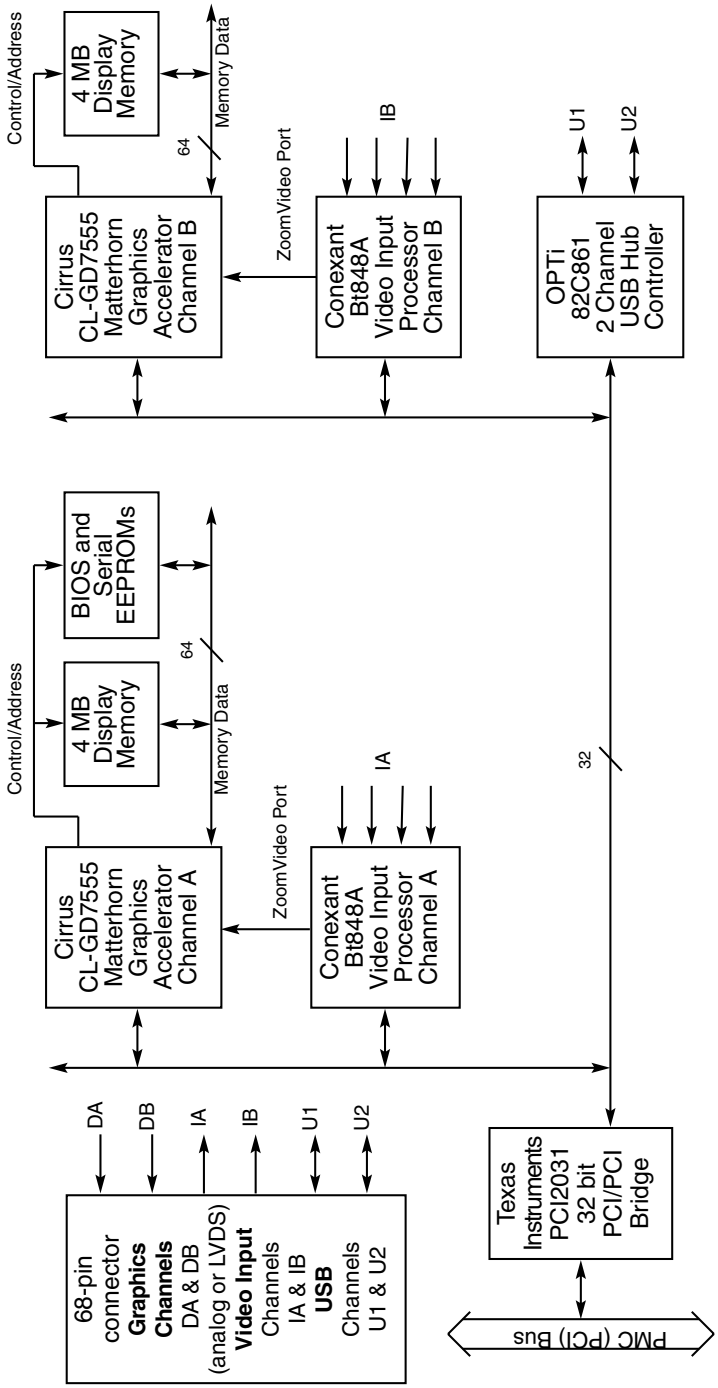


Figure 1-3 VFG-M Block Diagram



1.3 Additional References

Rastergraf documentation includes User's Manuals, Graphics Library Package Manual, and Rastergraf PX Windows Server Installation and User's Guide.

You can obtain copies of the technical literature from the Rastergraf web page (http://www.rastergraf.com).

Other sources of information:

USB Implementers Forum: http://www.usb.org/developers/index.html

PCI Local Bus 2.1 Specification — **PCI Special Interest Group**
P.O. Box 14070
Portland, OR 97214
(800) 433-5177

Graphics Textbooks

Fundamentals of Interactive Computer Graphics
Addison Wesley, 1993. — Foley and Van Dam

Principles of Interactive Computer Graphics
McGraw-Hill, 1979 — Newman and Sproull

1.4 General Specifications

Graphics Processor: The graphics boards use the 50 MHz Cirrus Logic Matterhorn CL-GD7555 64-Bit Graphics Processor, which has 64-bit line and BiTBLT functions and programmable video timing. Each graphics channel is completely independent of the others. The maximum supported frequencies are 135 MHz for the pixel clock and 100 MHz for the memory clock.

The VCQ-M has four CL-GD7555 chips. The VFG-M has two CL-GD7555 chips plus two Bt848A digitizers.

Display Memory (DRAM): The display memory for each channel is 64-bits/word, byte addressable, no-wait state, EDO DRAM, using 1M x 16 devices (only 4 MB are really usable)

4 MB of display DRAM gives three pages of 1280 x 1024 using 8-bit pixels, 1 1/2 pages using 16-bit pixels, or one page using packed 24 bpp mode.

EEPROM Memory: One 8-bit Flash EEPROM supports 64 KB 8-bit wide of permanent storage. Normally, the 48 KB Cirrus standard VGA BIOS is loaded. Alternatively, an OpenBoot compatible Fcode image can be loaded.

A 2 KBit (256 byte) serial EEPROM, programmed via PCI2031 control lines, stores bridge parameters, board serial number, and other Rastergraf and user data.

Display Output: The CL-GD7555 contains an integral color lookup table (CLUT). The CLUT supports VGA and interlaced and non-interlaced displays ranging from 640 x 480 up to better than 1280 x 1024. The RAMDAC has a 64 x 64 x 2 bitmapped cursor. The DAC outputs are 8-bits.

The 7555 ***does not*** support composite sync - an external encoder is required.

For 8-bit applications, the pixel size is 8 bits, and there is 1 byte per pixel. For 16 and 24 bit applications the pixel is divided into Red, Green, and Blue components. A color key can be used to switch the CLUT from passing the RGB components straight through to sampling the pixel to the color map, thus providing a mapped overlay value.

Scroll and Pan: Scroll - single line (smooth scroll).
Pan - anywhere on 8 pixel boundaries.

Video Digitizer (VFG-M): The VFG-M has two Conexant Bt848A Video Digitizer chips. Each device has a multiplexer that can select among four composite signals or three composite plus one S-Video (separate chrominance and luminance inputs). See section 3.6 for a complete description of the Bt848A.

PMC (PCI) Bus Access: All devices are accessible to the PMC/PCI bus through a TI PCI2031 Transparent PCI to PCI Bridge.

Bus Loading: One PCI 2.1 compatible load

Front Panel Connections: All I/O is available on the single 68-pin 3M N10268-52E2VC Mini-D ribbon connector on the front panel.

Breakout Cable: Rastergraf can provide a front panel breakout cable to supply:

Video Output for each CL-GD7555 channel

Red, Green, Blue, and TTL level DDC, vertical, and horizontal sync on a VGA compatible connector.

USB Ports

Two 4 pin USB **HOST** side connectors are provided. Switched and current limited +5 volts are also provided.

Video Input for each Bt848A channel (VFG-M only)

Four composite (NTSC/PAL/SECAM) video signals plus one Chrominance input (for S-Video). Connector is a VGA type DB-15S compatible connector. Rastergraf can supply a separate VGA to BNC cable if required.

Module Size: Standard IEEE 1386 PMC bus card, 149 mm x 74 mm.

Power Requirements: +5V +/- 5%, 1.5 A typical.

Environment:

Temperature:	0 to 70 degrees C, operating
	-55 to +85 degrees C, storage
Humidity:	10% to 90%, non-condensing

PCI bus Interrupts: The local PCI device interrupts are connected to the PMC INTA-INTD lines.

VCQ-M

INTA: Channel A CL-GD7555 and OPTi 82C861 USB
INTB: Channel B CL-GD7555
INTC: Channel C CL-GD7555
INTD: Channel D CL-GD7555

VFG-M

INTA: Channel A CL-GD7555 and OPTi 82C861 USB
INTB: Channel B CL-GD7555
INTC: Channel A Bt848A
INTD: Channel B Bt848A

Local PCI Bus IDSELs: The on-board device IDSELs are connected to the internal PCI address/data bus as follows:

VCQ-M

IDSEL16	Channel A CL-GD7555
IDSEL17	Channel B CL-GD7555
IDSEL18	Channel C CL-GD7555
IDSEL19	Channel D CL-GD7555
IDSEL20	OPTi 82C861 USB

VFG-M

IDSEL16	Channel A CL-GD7555
IDSEL 17	Channel B CL-GD7555
IDSEL 18	Channel A Bt848A
IDSEL 19	Channel B Bt848A
IDSEL 20	OPTi 82C861 USB

TI PCI2031 PCI to PCI Bridge Vendor and Device IDs

PCI Vendor ID: 0x104C

PCI Device ID: 0xAC21

PCI Subsystem Vendor ID: 0x10F0 (Vendor Code)

PCI Subsystem Device ID: 0xB400 (VCQ-M Identifier)
0xB600 (VFG-M Identifier)

Cirrus CL-GD7555 Graphics Accelerator Vendor and Device IDs

PCI Vendor ID: 0x1013

PCI Device ID: 0x0040

PCI Subsystem Vendor ID: 0x0000

PCI Subsystem Device ID: 0x0000

Conexant Bt848A Video Digitizer Vendor and Device IDs (VFG-M)

PCI Vendor ID: 0x109E

PCI Device ID: 0x0350

PCI Subsystem Vendor ID: 0x0000

PCI Subsystem Device ID: 0x0000

1.5 Monitor Requirements

Rastergraf display boards can be used with a wide variety of monitors. For best performance a monitor should have the following features:

- 5 Wire RGB with separate TTL horizontal and vertical sync
- Switchable Termination (for monitor loopthrough)
- Height, pincushion, width, phase, and position controls
- Autotracking horizontal and vertical synchronization
- High bandwidth: 70 MHz at 640 x 480
  135 MHz at 1280 x 1024
- Horizontal refresh rate: 32 kHz at 640 x 480
  70 kHz at 1280 x 1024

Note: A standard VGA type (multi-scan) monitor can be plugged directly into the breakout adapter cable.

Table 1-1 Standard Display Timing Specifications

Display Format	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 480	60 Hz	31.5 kHz	27 MHz
1024 x 768	60 Hz	60 kHz	80 MHz
1024 x 1024	70 Hz	64 kHz	85 MHz
1280 x 1024	60 Hz	64 kHz	110 MHz
1280 x 1024	67 Hz	72 kHz	125 MHz

1.6 Configuration Information

The basic graphics board includes:

- TI PCI2031 PCI to PCI Transparent Bridge
- 50 MHz Cirrus Logic CL-GD7555 Graphics Accelerator
- Maximum display size: 1280 x 1024 x 24 bpp
- hardware interrupts, pan, zoom scroll, and cursors
- analog RGBHV video output
- VGA BIOS or SPARC Fcode on channel 1
- Optional 2 Kbit serial EEPROM and 3 diagnostic LEDs
- OPTi 82C861 USB 1.1 host controller
- Two Conexant Bt848A Video Digitizers (VFG-M)

Table 1-2 Common Configurations

Model	VGA or FCode	Display heads	Digitizer heads	USB
VCQ-M	VGA	4	0	USB
VCQ-M/SO	FCode	4	0	USB
VFG-M	VGA	2	2	USB
VFG-M/SO	FCode	2	2	USB

Table 1-3 Software Support

Operating System	Software Availability	BIOS	Graphics Board	Multi-head	USB	Video In (VFG)
Solaris	**DDX, SDL**	FCode	All	Yes	Yes	No
VxWorks	**Xvgp, SDL**	VGA	All	Yes	No	Yes - SDL
LynxOS	**Xvgp, SDL**	VGA	All	Yes	No	No
Windows	**NT/2K, XP**	VGA	All	No	No	Yes
Linux	**Xvgp, SDL**	VGA	All	Yes	Yes	Yes

Notes: **DDX** means SunX compatible loadable DDX module
SDL means Graphics Library Package

Chapter 2
Installing Your Rastergraf Display Board

2.1 Introduction

There are 2 steps involved in getting your Rastergraf display board to work in your system:

- Unpack and install the Rastergraf display board.
- Install the software

This chapter shows you how to install the Rastergraf display board in your computer. Your Rastergraf software User's Manual (e.g. SDL) provides instructions on how to install the software.

2.2 Unpacking Your Board

When you unpack your board, inspect the contents to see if any damage occurred in shipping. If there has been physical damage, file a claim with the carrier at once and contact Rastergraf for information regarding repair or replacement. Do not attempt to use damaged equipment.

> **Caution**
>
> Be careful not to remove the board from its antistatic bag until you are ready to install it. It is preferable to wear a grounded wrist strap whenever handling computer boards.

Some operating systems require that you reboot your system after installing a device driver, because only after the reboot will your system utilize the driver and recognize the board. If yours is such an operating system, you might like to install your Rastergraf software **before** installing the board since you will have to shut down the computer to install the board anyway. If you want to install the software before shutting down the computer, proceed to the correct part of the relevant software manual and return to this chapter afterwards.

2.3 Preparing for Installation

The VCQ-M and VFG-M graphics boards are designed to plug into any 32-bit, 5V or 3.3V signaling, IEEE 1386 compatible single module PMC location. PMC locations are directly supported on VME and CompactPCI compatible computers.

The graphics board will also work correctly in CompactPCI, PCI, and VME systems. In the case of a CompactPCI system, you can use a PMC to CompactPCI adapter. For a PCI system, you can use a PMC to PCI adapter.

> **Note:**
>
> Older VME host or carrier boards may not supply 3.3V to the PMC connectors. Since the VCQ-M and VFG-M boards have an on-board 3.3V regulator, this should not be a problem.

2.3.1 Interrupt Settings

The graphics board, having five PCI devices behind a PCI bridge, is connected to a permuted set of the interrupt lines. See Section 1.4 for details. Since each PMC slot itself maps its interrupt lines to a permuted set of INTA-INTD, the graphics board devices will show up on different interrupt lines, according to the slot it is plugged into. Thus, the device driver may need to be changed to reflect this.

2.3.2 Board Address Settings – General information

Since the PCI bus and the graphics board are configured by the operating system and/or BIOS while booting up, there aren't any address jumpers. The address settings are programmable and are set up by the software as a result of information supplied by the OS at boot time. Refer to the Rastergraf software User's Manuals for more information.

Mapping the VCQ-M or VFG-M devices is a two stage process, as you first have to set up the PCI2031 PCI to PCI bridge, and then, through it, map the PCI and other control registers in the CL-GD7555 Graphics Accelerator chips and the 82C861 USB host, and Bt848A video digitizers (VFG-M). In all cases, the BAR (Base Address Register) sets in the chips are programmed to point to various parts of each chip, such as graphics memory and control registers.

The Rastergraf device driver will load the BARs even if the O/S or BIOS did not. If you can determine the actual PCI base address, you might even be able to probe the address spaces with an on-line debugger once the driver code has run. Section 3.3 has details on how the graphics board controls access to the on-board registers.

The ability to probe the board is dependent on the CPU memory map as implemented by the system OS and the CPU hardware. These things change from OS to OS, board to board, and vendor to vendor, making it a difficult task. Most likely, if you use Rastergraf supplied software, the board will show up and you will get pictures.

2.3.3 Address Space and Relocatability Configuration

The VCQ-M and VFG-M boards are, for the most part, "Plug and Play" devices. Their operation is almost entirely dependent on the software.

However, the CL-GD7555's control register set must be preset in hardware to appear in processor I/O or memory address space. Also, the register set can have a fixed default address range or can be relocatable, that is , to have the ability to be moved around, using a Bus Address Register (BAR) in the CL-GD7555.

Depending on the software package in use, these parameters must be set according to its requirements. Usually, this is consistent by CPU and operating system. For the sake of convenience here, the term **mode** will be used to describe the combination of the address space and relocatability, since they are set together.

The mode is programmed into the CL-GD7555 on power-up using configuration inputs temporarily allocated to memory data bus lines. The mode is set using MD34 (enable memory mapped IO) and MD40 (enable

relocatable I/O) as described in the Cirrus CL-GD7555 Hardware Reference Manual.

Table 2-2 Graphics Board I/O Register Mapping Options

Mode	MD40	MD34	Use	Address Space	Address Range
0	0	0	VGA, Xvgp	I/O Mapped	Fixed
1	0	1	none	Memory Mapped	Fixed
2	1	0		I/O Mapped	Relocatable
3	1	1	SDL	Memory Mapped	Relocatable

Depending on the graphics board model, the mode is set by 0 ohm resistors or jumper blocks. In the table above, “0” means a jumper or resistor is removed; “1” means the jumper or resistor is installed.

On some boards, the initial power-up mode can be subsequently overridden by programmed I/O commands (see Section 3.2) which changing the state of the control bits normally assigned to the Red, Amber, and Green diagnostic LEDs.

The Red, Amber, and Green LEDs are driven by PIO3, PIO2, and PIO1 (respectively) on the graphics board PCI2031 bridge chip (PCI register 0x74). If you first set PIO3 on, then the PIO1 and PIO2 map to the configuration inputs **MD40** and **MD34**, respectively. Any CL-GD7555 can be put into any mode by setting its "reload configuration" bit (SR24[3]). Each chip can be loaded independently of the others. Turning the LED "ON" is setting the configuration bit to a "1".

Table 2-3 Graphics Board Configuration Options

Graphics Board	Fab Revision	Modes Set By	Programmed I/O Override?
VCQ-M	all	Two resistors for each channel	no
VFG-M	0	Two resistors per channel	no
VFG-M	1	Two jumpers for Channels A-B	yes

2.3.2.1 Boards with Configuration Resistors

As mentioned previously, all VCQ-M and the VFG-M Rev 0 use 0 ohm resistors to set the memory mode. The following table details the modes.

Table 2-4 Graphics Board Configuration Resistors

Graphics Board	Fab Revision	Channel	MD40 Resistor Identifier	MD34 Resistor Identifier
VCQ-M	all	A	R307	R308
		B	R315	R316
		C	R407	R408
		D	R415	R416
VFG-M	0	A	R307	R308
		B	R315	R316

2.3.2.2 VFG-M Rev 1 Configuration Jumpers

In an effort to make the settings more user friendly and recognizing that it isn't necessary to provide jumpers for every channel, jumpers are provided on the Rev 1 VFG-M.

Two pairs of jumpers are used to set the characteristics for Channel A and another pair are used for Channel B. Note that the Mode is set implicitly by the jumper combinations:

Table 2-5 VFG-M Configuration Jumpers

Graphics Board	Fab Revision	Channel(s)	Mode	JP101 In/Out	JP102 In/Out
VFG-M	1	Both	0	In	In
		A B	0 3	Out	In
		Both	2	In	Out
		Both	3	Out	Out

Figure 2-1 VCQ-M Jumpers and Resistors Locations

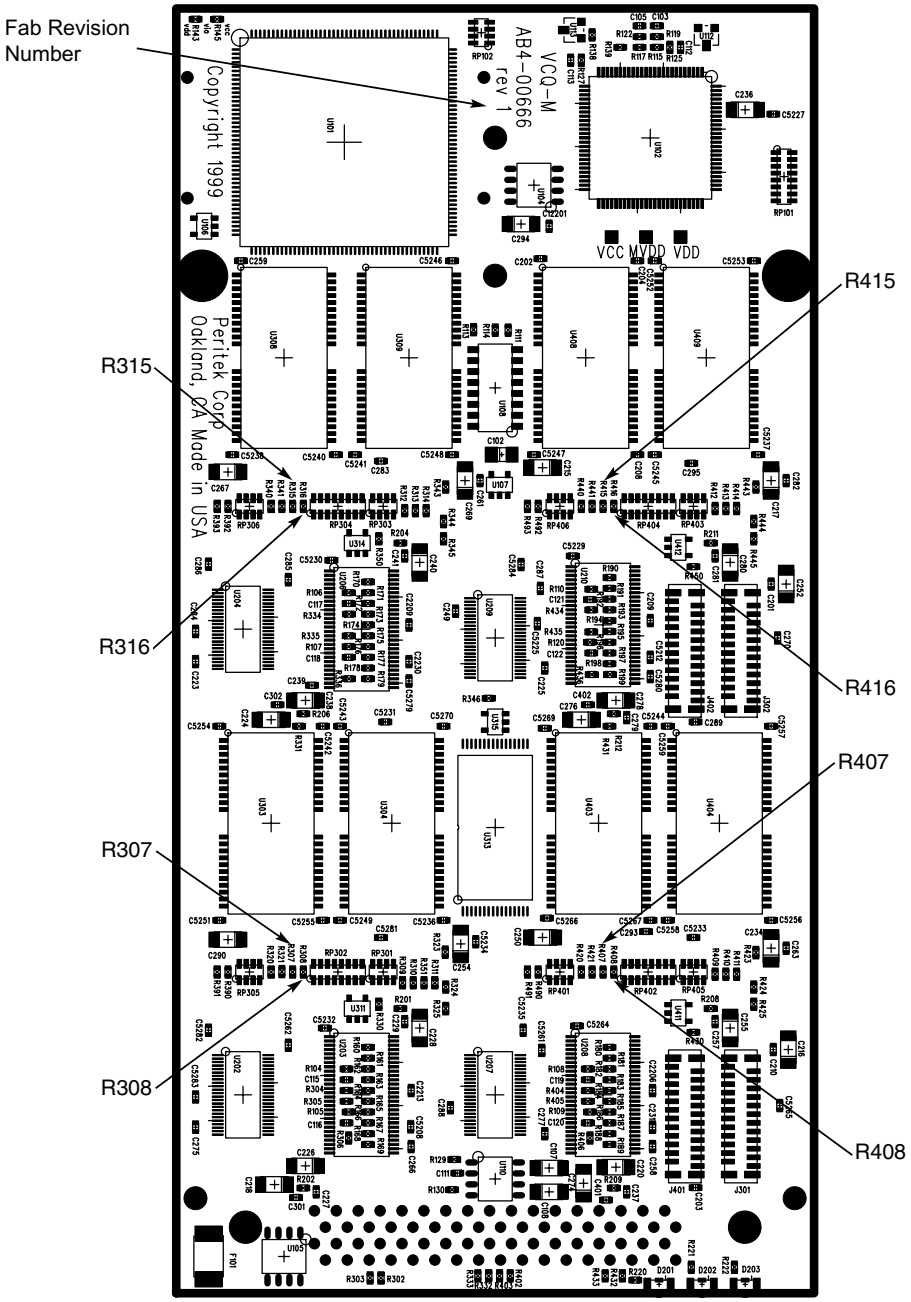
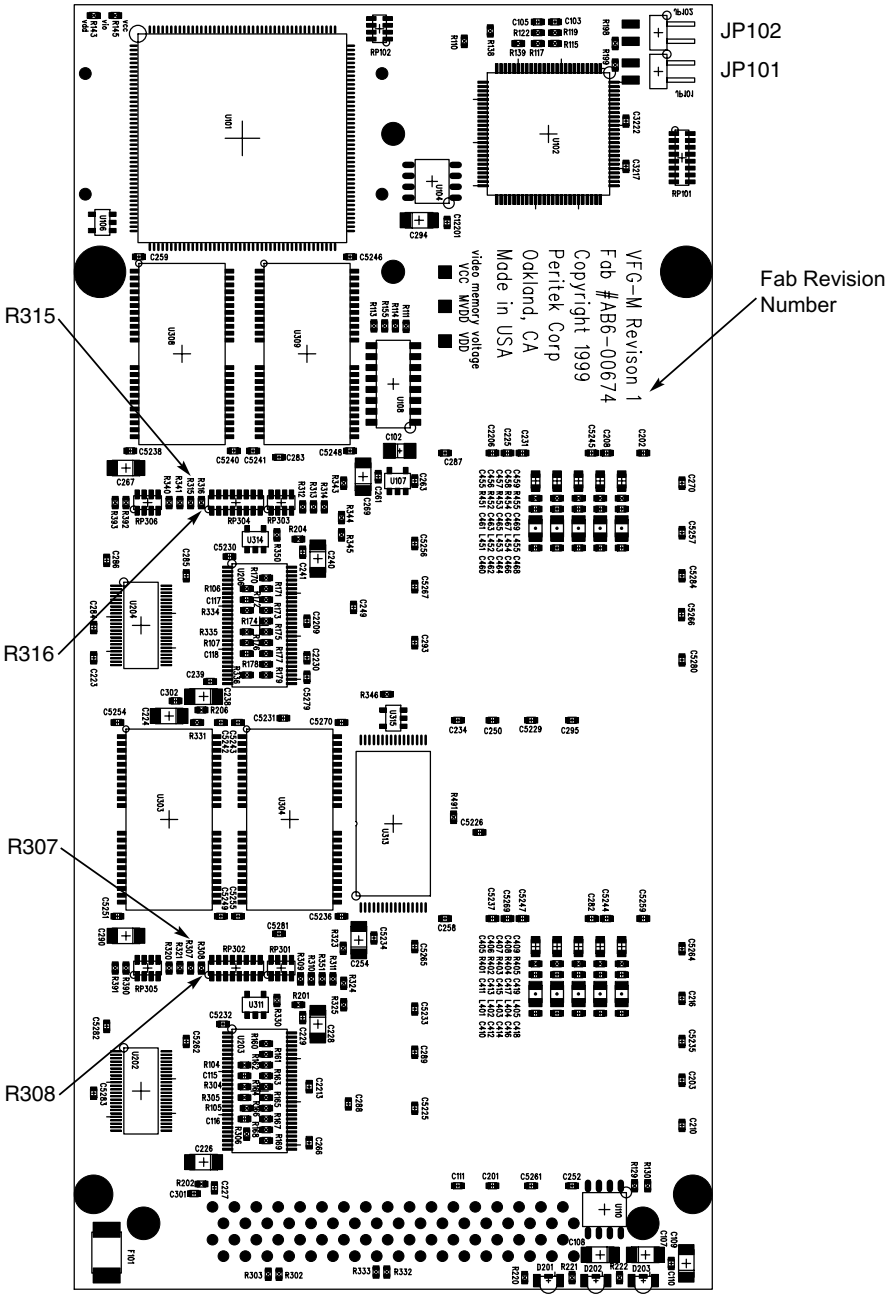


Figure 2-2 VFG-M Jumpers and Resistors Locations



2.4 VCQ-M and VFG-M Installation

> **Note:**
>
> Refer to ***Section 2.3*** for the setting the jumpers on the graphics board.

1. Shut down the operating system and **turn off the power**.

> **Warning!**
>
> Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and remove the CPU board onto which the graphics PMC board is to be installed. Identify an empty PMC location (generally there are one or two on a given CPU board).

   The graphics PMC board is a Universal PMC/PCI device and can be plugged into a PMC port which uses either 5V or 3.3V signaling.

3. Take care to optimize airflow by blocking off unused slots in the card cage, and arrange the boards to permit optimum airflow through them.

> **Caution**
>
> The static electricity that your body builds up normally can seriously damage the components on the graphics board.

4. Wear a grounded wrist strap. Touch a metal part of the computer chassis, remove the graphics board from its anti static bag, and immediately slide it into the slot.

Figure 2-3 Installation of a PMC Module into a Motorola MVME2604

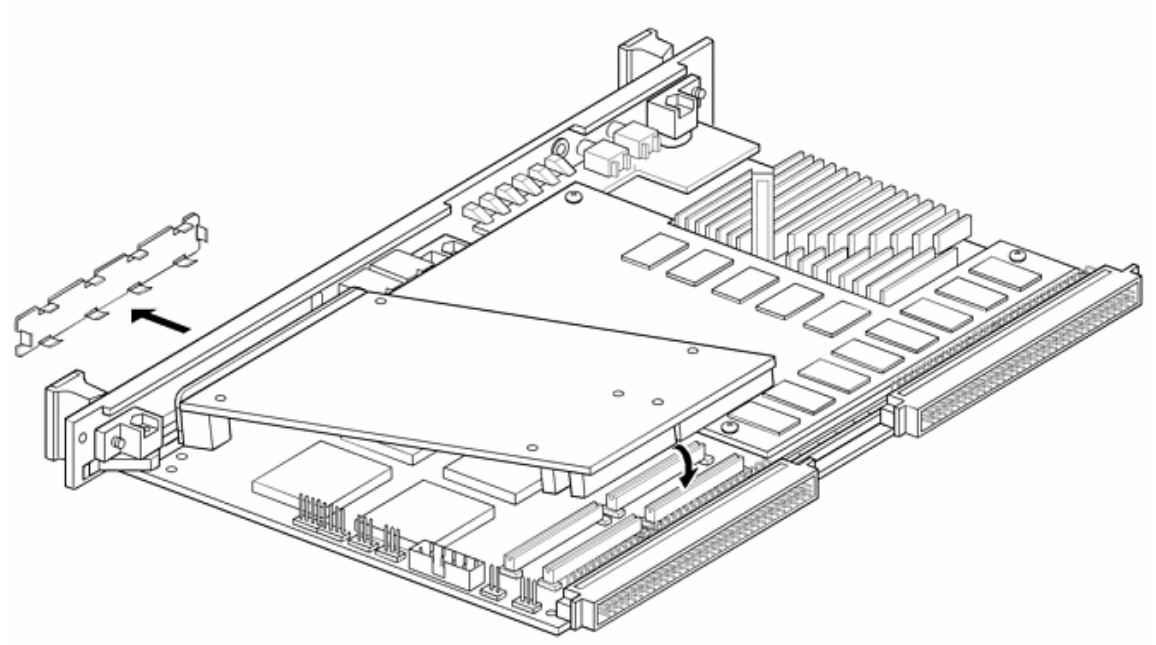
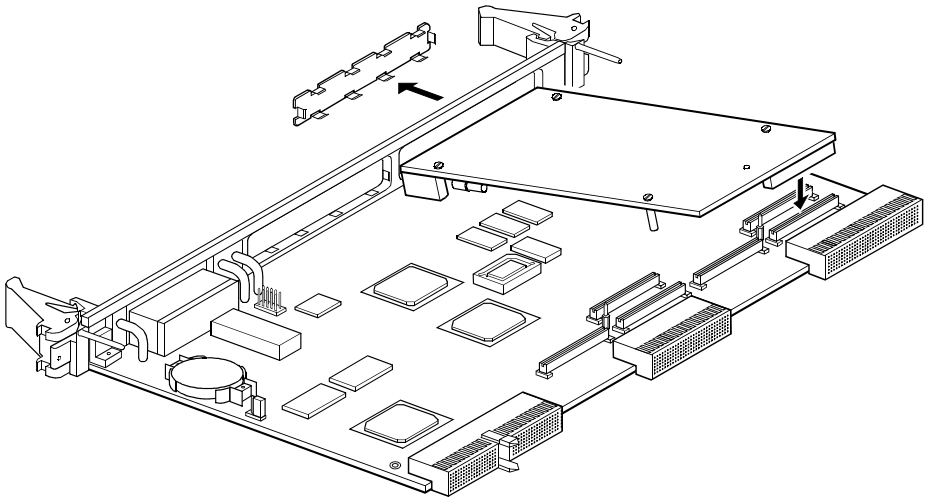


Figure 2-4 Installation of the PMC Module into a Motorola CPV3060



5. After ensuring that the board is seated correctly, install the mounting screws (two near the front and two near the PMC connectors).

Note

Sometimes the graphics board front panel can hang up going into the carrier front panel hole. This can be because there is a little rubber EMI gasket that is installed in a slot cut into the graphics board front panel. If the hole in the carrier board is “on the small side” it can be difficult if not impossible to install the graphics board. In this case, you will have to remove and discard the gasket.

6. Close the computer.

Now, go to Section 2.7.

2.5 Installing in a PCI Backplane

> **Note:**
>
> Refer to ***Section 2.3*** for the setting the jumpers on the graphics board.

You can install a VCQ-M or VFG-M into a PCI computer if you first plug the graphics board into a PMC to PCI adapter board. The adapter should be Universal PCI compatible and be designed to plug into any standard PCI 2.2 specification compatible backplane.

> **Note:**
>
> Most AT style motherboards do not supply 3.3V to the PCI connectors. If the computer is listed as PCI 2.0 or 2.1 compliant, it probably does not supply 3.3V. Since the VCQ-M and VFG-M boards have an on-board 3.3V regulator, this should not be a problem.

1. Shut down the operating system and **turn off the power**.

> **Warning!**
>
> Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and find an empty PCI slot.

   Both the VCQ-M or VFG-M and the adapter are Universal PCI devices and can be plugged into a slot which uses either 5V or 3.3V signaling protocol.

   The adapter may have a 64-bit PCI expansion connector. Note that when it is used with the VCQ-M or VFG-M, this connector is not used.

Caution

The static electricity that your body builds up normally can seriously damage the components on the graphics board.

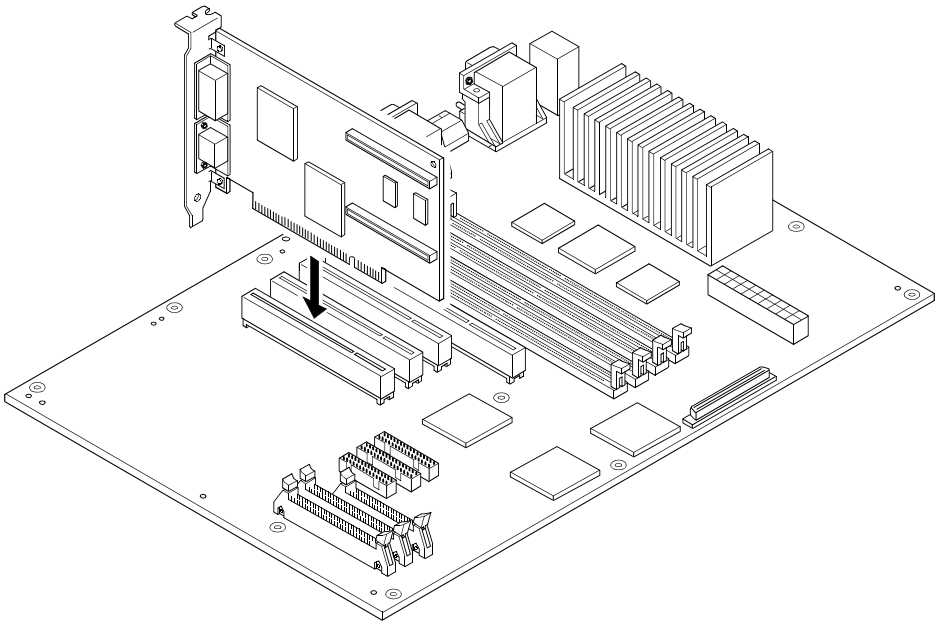
4. Wear a grounded wrist strap. Touch a metal part of the computer chassis, remove the graphics board and adapter combination from its anti static bag, and immediately slide it into the slot.

5. Remove the card slot blocking plate, and after making sure the board is seated correctly, install the screw into the place where the blocking plate was and which (now) holds the graphics board's front panel.

6. Close the computer.

Now, go to Section 2.7

Figure 2-5 Installation of a PCI Module into a Motorola MTX



2.6 Installing in a CompactPCI Backplane

You can install a VCQ-M or VFG-M into a CompactPCI computer if you first plug the graphics board into a PMC to CompactPCI adapter board.

The adapter should be Universal PCI compatible and be designed to plug into any 32-bit, 5V or 3.3V signaling CompactPCI 3U or 6U slot. The board needs only the 3U (J1) connector.

Note:

Refer to ***Section 2.3*** for the setting the jumpers on the graphics board.

1. Shut down the operating system and **turn off the power**.

Warning!

Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and identify the empty slot in the card cage that is closest to the CPU. Do not leave any slots empty between the graphics board and the CPU.

   Both the VCQ-M or VFG-M and the adapter are Universal PCI devices and can be plugged into a slot which uses either 5V or 3.3V signaling protocol. Therefore, a CompactPCI J1 connector signaling key plug is not necessary.

3. In the interest of allowing air flow, and if you have a choice, block off any unused slots in the cardcage so that fan air will not flow through them.

Caution

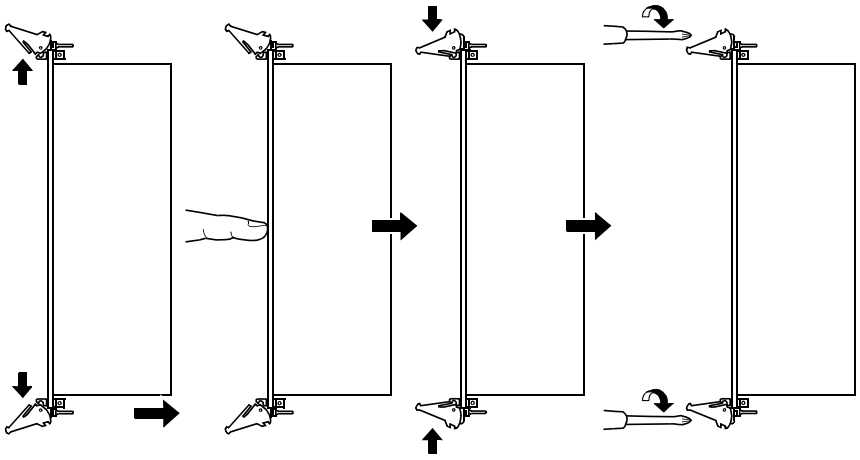
The static electricity that your body builds up normally can seriously damage the components on the graphics board.

Wear a grounded wrist strap.

4. Touch a metal part of the computer chassis, remove the graphics board from its anti static bag, and immediately slide it into the slot.

5. After making sure the board is seated correctly, lever the card in with the injector(s) and tighten the screwlock on each end of the faceplate

Figure 2-6 Installing a CompactPCI Board



6. Close the computer.

Now, go to Section 2.7

2.7 Finishing the Installation

Because the front panel on a PMC module is limited, the VCQ-M and VFG-M boards use a 68-pin connector for all "outside world" connections. Rastergraf can supply a breakout cable, MVU-6/3, that provides standard VGA and USB connectors. Section 2.8 has details that will help you should you need to make your own cable. When attaching any cable to the graphics board, be sure to snug the connector's thumbscrews down, as it may otherwise work loose and cause unreliable operation.

2.7.1 Connecting to the Monitor

Connect the MVU-6/3 breakout cable connectors to the video cables for the monitors. Check the table below for connector details. Note that the VFG-M is a little different! The connectors on the breakout cable are VGA type, host side, so you plug a mating cable into the breakout cable as if it were a connector on the computer's back panel. Make sure that the 75 ohm switch on the monitor is turned on.

When connecting to the VFG-M, you may want an additional cable that converts from VGA to BNC to make it easier to connect to the digitizer sources, You can use a standard VGA to RGBHV BNC cable or obtain one from Rastergraf if necessary.

Note

The VCQ-M and VFG-M graphics outputs supply only 5-Wire Video (RGBHV) and cannot supply composite Sync on Green.

Table 2-6 Graphics Board Cable Information

Graphics Board Model	Cable Model	VGA Connector Label	Connector Function
VCQ	MVU-6/3	**CH1**	Channel A – primary channel
		CH2	Channel B
		CH3	Channel C
		CH4	Channel D
VFG	MVU-6/3	**CH1**	Channel A – primary channel
		CH2	Channel B
		CH3	Digitizer Set B
		CH4	Digitizer Set A

2.7.2 Connecting to the USB Ports

If you are not using the USB ports, just skip on to Section ***2.7.4 Checking your Display***.

The VCQ and VFG have two USB host controller ports. The use of these ports is completely software dependent, so there really isn't anything to do but plug in your USB devices. Using the MVU-6/3 breakout cable, you can plug a keyboard in one and a mouse in the other, or, if you are using a USB expander, just use one port. Both Solaris 8 and Linux are known to work with these ports.

2.7.4 Checking your Display

> **Note**
>
> The VCQ-M and VFG-M boards can supply ONLY 5 Wire Video (RGBHV, VGA connector).

Another minor detail:

The VCQ-M or VFG-M board may, depending on its original configuration as supplied by Rastergraf, have its BIOS PROM programmed either with VGA BIOS or Sun SPARC compatible Fcode.

In either case, obviously you can only use the board in a PC or SPARC, respectively.

Now, turn on the power and check your monitor's display and proceed:

2.7.5 Any Operating System, Any Computer

If you are expecting the system monitor (BIOS, OpenBoot, etc) to set up the mapping for the graphics board, the system monitor must be new enough to be able to "look" through PCI bridges, as the VCQ-M or VFG-M board devices (are all behind a TI PCI2031 PCI-PCI "transparent" bridge. It should find the Channel A graphics chip, load and run the VGA BIOS or Fcode, and initialize the display. You will then get the usual pre-boot display. Be sure to select VGA operation according to Section 2.3 3.

2.7.6 Using a VCQ-M or VFG-M Board in a PC

Note

The VGA BIOS and Windows NT/2K/XP driver set supports a single monitor, no video input only. Windows98 and Linux SDL and Xvgp do support multihead and video input.

Single Graphics Board

If you are using a PC and the Rastergraf board is to be the system display (and you don't have another VGA controller installed), the system BIOS should find the Rastergraf board, and initialize the display.

Multiple Graphics Boards

If you do have another VGA board in the system, the order in which the boards are plugged into the backplane or motherboard will determine which board will be used for the system display.

If you have another VGA type controller in the system, the system BIOS might not use the VCQ-M or VFG-M board for display, but it may still find and configure the PCI2031 bridge and the USB controller. If the BIOS picks the wrong one, turn off the computer and swap the boards' positions. Now, the desired board should be the system display.

If your system has a non-removable VGA controller and you want to use the Rastergraf board as the system display you may have a problem. If the BIOS starts up using the built-in VGA, you may be able to disable it with a BIOS setting. Otherwise, contact the system board manufacturer. Failing these things, you are probably out of luck.

2.7.7 Using a VCQ-M or VFG-M in a SPARC Computer

If you are running on a Sun system, you should have the Rastergraf OpenBoot FCode image loaded into the graphics board. This will enable OpenBoot to correctly identify the graphics board on startup and use it as the console. The Rastergraf loadable DDX module will supports multihead operation under Solaris 8 with Xinerama.

> **Note**
>
> Currently, there is no documented support for the USB ports to serve as console mouse and keyboard.

Single Graphics Board

If the Rastergraf board is to be the system display (and you don't have another display controller installed), OpenBoot should find the Rastergraf board, and initialize the display.

Multiple Graphics Boards

If you do have another board in the system, the order in which the boards are plugged into the backplane or motherboard will determine which board is used for the system display. If OpenBoot picks the wrong one, turn off the computer and swap the boards' positions.

If your system has a non-removable controller and you want to use the Rastergraf board as the system display you may have a problem. If OpenBoot starts up using the built-in display, you may be able to disable it with an OpenBoot EEPROM setting. Otherwise, contact the system board manufacturer. Failing these things, you are probably out of luck.

2.7.8 Using a VCQ-M or VFG-M in a PowerPC System

If the CPU's firmware is VGA aware, it should initialize Channel A on the graphics board and use it as the system console. Older PowerPC (PPC) based computers may not have generic VGA support. Newer ones are not "chrp" or "prep" compliant anymore, so they don't know about Fcode. Your best bet is to use a board with a VGA BIOS in it.

Otherwise, you will have to boot using a serial terminal and only after the graphics software has been installed and run will you see anything.

2.7.9 Final Checks

If you are running in a PC, then you should get the usual familiar PC displays.

In the case of PX Windows (Linux-Xvgp) or Solaris DDX, your monitor should display a uniform stippled raster and a cross-hair cursor, which is controlled by the mouse. If you have multiple graphics boards installed all screens will be initialized and display the stipple once you have the server installed and running.

For SDL, demo programs are provided that may be run to put test patterns on the screen(s).

Pictures!

Once you have a picture on the screen, you may need to adjust the width, height, brightness, contrast, and hold controls on your monitor to get a good, centered image. If these controls don't adjust the image properly, the parameters used to set the graphics timing registers might be wrong.

If you have any trouble with any part of the installation call Rastergraf for assistance, or refer to Chapter 4.

Otherwise, proceed to the instructions supplied in your software manual.

2.8 VCQ-M and VFG-M Connectors and Cables

There is just one connector on the front panel of the VCQ-M and VFG-M graphics boards. It is a 68 pin 3M mini-D ribbon connector. This sort of connector is used because there simply isn't enough front panel space to accommodate industry standard connectors.

Custom breakout cables are available from Rastergraf that do provide standard **computer side** connectors.

Graphics Board	Cable Model	Length	Description
VCQ, VFG	MVU-6/3	1 M	68 pin to 4 VGA + 2 USB
Any	VGA-5/6	2 M	VGA to 5 BNC

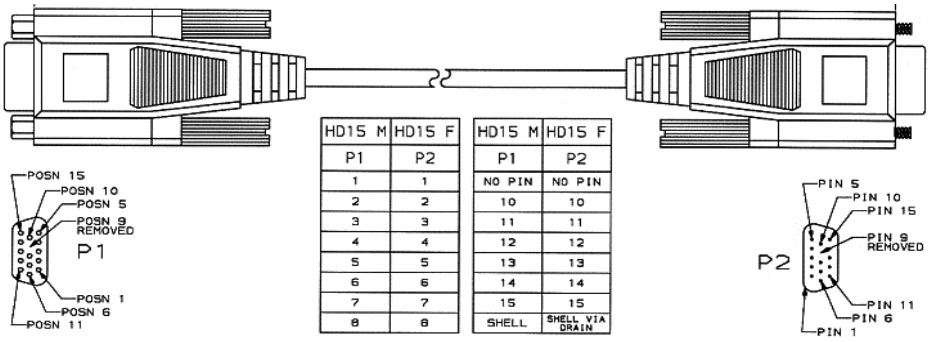
VGA Graphics

The breakout cable uses the industry standard VGA connector. The pinout has standard VGA (RGBHV) and DDC monitor control lines. A standard VGA to 5-BNC cable can be used with a monitor that requires BNCs rather a VGA connector.

The R, G, B, H, and V video outputs for each channel are driven by the CL-GD7555 RAMDAC, which is capable of driving terminated cable (75 ohms) to standard RS-330/IRE levels. Cable length should be limited to 50 feet unless you use low loss RG-59.

> **Note**
>
> The CL-GD7555 graphics chips can supply only 5 Wire (RGBHV) VGA-compatible video out, not composite sync on green. If you have problems, please contact Rastergraf for assistance.

Figure 2-7 Typical VGA Extension Cable



Video Input (VFG-M)

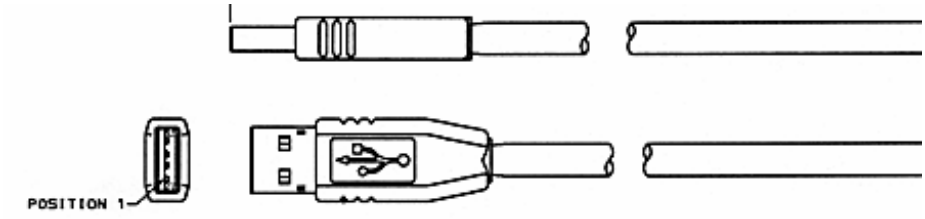
The breakout cable uses the industry standard VGA connector. The pinout has the five digitizer inputs connected to the standard VGA (RGBHV) pins so that, when desired, a standard VGA to 5-BNC cable can be used to connect to digitizer sources.

USB Ports

The USB ports support a vaiety of devices, including keyboard, mouse, and sound synthesizers.

The OPTi 82C861 USB host controller supports two USB ports and supplies switched, current limited +5 peripheral power to the USB connectors. The power lines are controlled by a Micrel USB power controller which is enabled by the 82C861. It limits power to 1A per line, and will shutdown and report an overcurrent condition to the 82C861. The USB port will return to normal when the overload is removed

Figure 2-8 Typical USB Cable End



Cable Details

Breakout Cable Connector Name	Section	Connectors	Graphics Board	Description
-	2.8.1	68-pin	VCQ	Front Panel
CH1, CH2, CH3, CH4	2.8.3	VGA	VCQ	VGA
USB1, USB2	2.8.4	USB	VCQ	USB Ports
-	2.8.2	68-pin	VFG	Front Panel
CH1, CH2	2.8.3	VGA	VFG	VGA
USB1, USB2	2.8.4	USB	VFG	USB Ports
CH3, CH4	2.8.5	VGA	VFG	Digitizers

2.8.1 VCQ-M Front Panel Connector

The VCQ-M uses a 68-pin 3M connector for the analog video and USB ports. It is necessary to build a breakout cable to make connections to standard devices. Rastergraf can supply the cable or you can build it yourself.

Table 2-6 VCQ-M Connector Pinout (sorted by Function)

Pin Number	Signal Name	Description
41	ground	Spare Ground
1	A_RED	Channel 1 Red
2	Ground	Channel 1 Red Ground
35	A_GREEN	Channel 1 Green
36	Ground	Channel 1 Green Ground
37	A_BLUE	Channel 1 Blue
38	Ground	Channel 1 Blue Ground
39	A_H_SYNC	Channel 1 Horizontal Sync
40	Ground	Channel 1 Sync Ground
3	A_V_SYNC	Channel 1 Vertical Sync
4	Ground	Channel 1 Sync Ground
6	A_VDCCKH	Channel A DDC Clock
5	ground	Channel A DDC Ground
7	A_VDCDAH	Channel A DDC Data
8	Fused +5 Volts, .1A max	Channel A +5 DDC Terminator
42	ground	Spare Ground
9	B_RED	Channel 2 Red
10	Ground	Channel 2 Red Ground
11	B_GREEN	Channel 2 Green
12	Ground	Channel 2 Green Ground
45	B_BLUE	Channel 2 Blue
46	Ground	Channel 2 Blue Ground
47	B_H_SYNC	Channel 2 Horizontal Sync
48	Ground	Channel 2 Sync Ground
43	B_V_SYNC	Channel 2 Vertical Sync
44	Ground	Channel 2 Sync Ground
50	B_VDCCKH	Channel 2 DDC Clock
49	ground	Channel 2 DDC Ground
17	B_VDCDAH	Channel 2 DDC Data
14	Fused +5 Volts, .1A max	Channel 2 +5 DDC Terminator

Table 2-6 VCQ-M Connector Pinout (continued)

61	ground	Spare Ground
55	C_RED	Channel 3 Red
56	Ground	Channel 3 Red Ground
57	C_GREEN	Channel 3 Green
58	Ground	Channel 3 Green Ground
25	C_BLUE	Channel 3 Blue
26	Ground	Channel 3 Blue Ground
59	C_H_SYNC	Channel 3 Horizontal Sync
60	Ground	Channel 3 Sync Ground
23	C_V_SYNC	Channel 3 Vertical Sync
24	Ground	Channel 3 Sync Ground
52	C_VDCCKH	Channel 3 DDC Clock
21	Fused +5 Volts, .1A max	Channel 3 +5 DDC Terminator
53	C_VDCDAH	Channel 3 DDC Data
54	ground	Channel DDC Ground
62	ground	Spare Ground
63	D_RED	Channel 4 Red
64	Ground	Channel 4 Red Ground
65	D_GREEN	Channel 4 Green
66	Ground	Channel 4 Green Ground
33	D_BLUE	Channel 4 Blue
34	Ground	Channel 4 Blue Ground
67	D_H_SYNC	Channel 4 Horizontal Sync
68	Ground	Channel 4 Sync Ground
31	D_V_SYNC	Channel 4 Vertical Sync
32	Ground	Channel 4 Sync Ground
28	D_VDCCKH	Channel 4 DDC Clock
27	ground	Channel 4 DDC Ground
29	D_VDCDAH	Channel 4 Monitor DDC Data
30	Fused +5 Volts, .1A max	Channel 4 +5 DDC Terminator
19	RUSBV1H	Channel A USB Data Pair +
20	RUSBV1L	Channel A USB Data Pair -
18	USBV1	Channel A USB Switched Power
22	GND	Channel A USB Ground
15	RUSBV2H	Channel B USB Data Pair +
16	RUSBV2L	Channel B USB Data Pair -
51	USBV2	Channel B USB Switched Power
13	GND	Channel B USB Ground

2.8.2 VFG-M Front Panel Connector

The VFG-M uses a 68-pin 3M connector for the analog video and USB ports. It is necessary to build a breakout cable to make connections to standard devices. Rastergraf can supply the cable or you can build it yourself.

Table 2-7 VFG-M Connector Pinout (sorted by Function)

Pin Number	Signal Name	Description
41	GND	Spare Ground
1	A_RED	Display Channel A Red
2	GND	Display Channel A Red Ground
35	A_GREEN	Display Channel A Green
36	GND	Display Channel A Green Ground
37	A_BLUE	Display Channel A Blue
38	GND	Display Channel A Blue Ground
39	A_H_SYNC	Display Channel A Horizontal Sync
40	GND	Display Channel A Sync Ground
3	A_V_SYNC	Display Channel A Vertical Sync
4	GND	Display Channel A Sync Ground
6	A_VDCCKH	Display Channel A DDC Clock
5	GND	Display Channel A DDC Ground
7	A_VDCDAH	Display Channel A DDC Data
8	Fused +5 Volts, .1A max	Display Channel A +5 DDC Terminator
42	GND	Spare Ground
9	B_RED	Display Channel B Red
10	GND	Display Channel 2 Red Ground
11	B_GREEN	Display Channel B Green
12	GND	Display Channel 2 Green Ground
45	B_BLUE	Display Channel B Blue
46	GND	Display Channel B Blue Ground
47	B_H_SYNC	Display Channel B Horizontal Sync
48	GND	Display Channel B Sync Ground
43	B_V_SYNC	Display Channel B Vertical Sync
44	GND	Display Channel B Sync Ground
50	B_VDCCKH	Display Channel B DDC Clock
49	GND	Display Channel B DDC Ground
17	B_VDCDAH	Display Channel B DDC Data
14	Fused +5 Volts, .1A max	Display Channel B +5 DDC Terminator

Table 2-7 VFG-M Connector Pinout (continued)

61	GND	Spare Ground
55	B_MUX0	Digitizer Channel B Mux Input 0
56	GND	Digitizer Channel B Mux Input 0 Ground
57	B_MUX2	Digitizer Channel B Mux Input 2
58	GND	Digitizer Channel B Mux Input 2 Ground
25	B_MUX3	Digitizer Channel B Mux Input 3
26	GND	Digitizer Channel B Mux Input 3 Ground
59	B_CIN	Digitizer Channel B Chrominance
60	GND	Digitizer Channel B Chrominance Ground
23	B_MUX1	Digitizer Channel B Mux Input 1
24	GND	Digitizer Channel B Mux Input 1 Ground
21, 52, 53, 54	GND	Spare Ground
62	GND	Spare Ground
63	A_MUX0	Digitizer Channel A Mux Input 0
64	GND	Digitizer Channel A Mux Input 0 Ground
65	A_MUX2	Digitizer Channel A Mux Input 2
66	GND	Digitizer Channel A Mux Input 2 Ground
33	A_MUX3	Digitizer Channel A Mux Input 3
34	GND	Digitizer Channel A Mux Input 3 Ground
67	A_CIN	Digitizer Channel A Chrominance
68	GND	Digitizer Channel A Chrominance Ground
31	A_MUX1	Digitizer Channel A Mux Input 1
32	GND	Digitizer Channel A Mux Input 1 Ground
27, 28, 29, 30	GND	Spare Ground
19	RUSBV1H	USB Channel A Data Pair +
20	RUSBV1L	USB Channel A Data Pair -
18	USBV1	USB Channel A Switched Power
22	GND	USB Channel A Ground
15	RUSBV2H	USB Channel B Data Pair +
16	RUSBV2L	USB Channel B Data Pair -
51	USBV2	USB Channel B Switched Power
13	GND	USB Channel B Ground

2.8.3 VGA Video Connectors

The VFG-M front panel connector supplies analog video to standard VGA connectors via the Rastergraf MVU-6/1 68-pin Mini-D ribbon breakout cable.

Table 2-8 VFG-M VGA Connector Pinout

VGA Pin Number	Description
1	Red
2	Green
3	Blue
4	not used
5	DDC Ground
6	Red Ground
7	Green Ground
8	Blue Ground
9	Fused +5 Volts, .25A max
10	Sync Ground
11	Ground
12	DDCDA
13	HSYNC
14	VSYNC
15	DDCCK

2.8.4 USB Connectors

The VFG-M front panel connector provides two USB host (Series A) receptacles via the Rastergraf MVU-6/1 68-pin Mini-D ribbon breakout cable.

Table 2-9 USB Connector Pinout

USB Pin Number	Description
1	Switched USB Power
2	USB Data Pair -
3	USB Data Pair +
4	Ground

2.8.5 VFG-M Video Input (VGA-style) Connectors

The VFG-M front panel connector provides four Composite NTSC/PAL/SECAM Inputs per digitizer channel plus an additional input for Chrominance. Composite Input 0 can be used with the Chrominance Input for S-Video applications.

Each input is conditioned with a low pass filter and presents a 75 ohm impedance to the driving source. The Input multiplexer is ***not*** break-before-make, so inputs will be *momentarily* connected together when switiching from one input to another.

Rastergraf can supply a second cable that converts the VGA connector to 5 BNCs: part number VGA-5/20.

Note

Note that the connector marked **CH3** is used for digitizer channel **B** and the connector marked **CH4** is used for digitizer channel **A** (sic).

Table 2-10 VFG-M Breakout Cable VGA Connector Pinout

Pin Number	Description
1	Mux Input 0
2	Mux Input 2
3	Mux Input 3
4	not used
5	Ground
6	Mux Input 0 Ground
7	Mux Input 2 Ground
8	Mux Input 3 Ground
9	Ground
10	Mux Input 1 Ground
11	not used
12	Ground
13	Chrominance Input
14	Mux Input 1
15	Ground

2.8.11 Connections to the PMC Bus

J11			
1	TCKH	n/c (-12V)	2
3	GND	INTAL	4
5	INTBL	INTCL	6
7	BUSMODE1L	+5V	8
9	INTDL	PCI-RSVD	10
11	GND	PCI-RSVD	12
13	PCICLK	GND	14
15	GND	PMCGNTL	16
17	PMCREQL	+5V	18
19	Vio	AD31H	20
21	AD28H	AD27H	22
23	AD25H	GND	24
25	GND	C/BE3L	26
27	AD22H	AD21H	28
29	AD19H	+5V	30
31	Vio	AD17H	32
33	FRAMEL	GND	34
35	GND	IRDYL	36
37	DEVSELL	+5V	38
39	GND	LOCKL	40
41	n/c (SDONL)	n/c (SBOL)	42
43	PAR	GND	44
45	Vio	AD15H	46
47	AD12H	AD11H	48
49	AD09H	+5V	50
51	GND	C/BE0L	52
53	AD06H	AD05	54
55	AD04H	GND	56
57	Vio	AD03H	58
59	AD02H	AD01H	60
61	AD00H	+5V	62
63	GND	n/c (RQ64L)	64

J12			
1	+12V	TRSTL	2
3	TMSH	TDOH	4
5	TDIH	GND	6
7	GND	PCI-RSVD	8
9	PCI-RSVD	PCI-RSVD	10
11	BUSMODE2L	byp (+3.3V)	12
13	RSTL	BUSMODE3L	14
15	byp (+3.3V)	BUSMODE4L	16
17	PCI-RSVD	GND	18
19	AD30H	AD29H	20
21	GND	AD26H	22
23	AD24H	byp (+3.3V)	24
25	IDSEL1	AD23H	26
27	byp (+3.3V)	AD20H	28
29	AD18H	GND	30
31	AD16H	C/BE2L	32
33	GND	PMC-RSVD	34
35	TRDYL	byp (+3.3V)	36
37	GND	STOPL	38
39	PERRL	GND	40
41	byp (+3.3V)	SERRL	42
43	C/BE1L	GND	44
45	AD14	AD13H	46
47	GND	AD10H	48
49	AD08H	byp (+3.3V)	50
51	AD07H	PMC-RSVD	52
53	byp (+3.3V)	PMC-RSVD	54
55	PMC-RSVD	GND	56
57	PMC-RSVD	PMC-RSVD	58
59	GND	PMC-RSVD	60
61	n/c (AK64L)	byp (+3.3V)	62
63	GND	PMC-RSVD	64

Note: **byp** means the pin is connected to a bypass capacitor on the graphics board but is otherwise not used

Chapter 3 Programming On-board Devices

3.1 Introduction

This chapter covers the special programming features of the individual devices used on the VCQ-M and VFG-M. It is intended to supply information unique to the board or to the application of a particular chip. Section 1.3 provides a list of appropriate publications which include manufacturer's data sheets and manuals.

Rastergraf offers a variety of software to support the VCQ-M and VFG-M in Solaris, Windows NT/2K/XP, VxWorks, and Linux. These offerings are covered in detail on the Rastergraf web page.

Note

Please read these sections **before** starting on this chapter:

Section 1.2 Functional description of the VCQ-M and VFG-M.
Chapter 2 Installation

This chapter includes the following sections:

Because the VCQ-M and VFG-M boards are mostly an assembly of "black box" parts, there isn't a lot of external logic that has to be documented. Thus, the following sections don't actually provide much programming information, as the chip documentation and SDL source code cover that pretty well. The sections summarize the devices and include some "hints and kinks".

You can refer to the **Rastergraf web site** for complete documentation. You can also look at the Rastergraf SDL source software itself.

The following sections assume that you have read Section 1.2 and have some knowledge of video, graphics, the PCI bus and the I^2C protocol. For detailed information concerning operation of the PCI bus, please refer to the Section 1.3, Additional References.

3.2 PCI2031 PCI to PCI Transparent Bridge

PMC (or PCI) peripheral boards are allowed to present only one PCI device load to the PMC bus. Therefore, Rastergraf uses a Texas Instruments PCI2031 Transparent PCI to PCI Bridge to enable the use of multiple PCI devices on the graphics board.

The PCI2031 contains PCI bus and local bus control and address map registers. By its nature, the PCI registers are set up during system initialization. The PCI2031 does not come up responding to any particular addresses. Host based software generally probes the PCI bus on startup, and depending on the software's capabilities, will either map the PCI2031 into system address spaces or just ignore it, leaving subsequent user software to do the job. Most newer host CPU firmware will even find the VGA-configured CL-GD7555 (Channel A).

Each local PCI device has its own PCI bus and local bus control and address map registers which are used to gain access to the chip's local functions. Once mapped, graphics memory and other on-chip functions can then be accessed through control registers and memory windows which are located in the chip's PCI/PMC memory address space. Graphics memory can be accessed using the CL-GD7555's drawing engine or directly, in "dumb frame buffer" mode.

The following table shows how much memory must be mapped by the operating system's PCI mapping code for each PCI device.

Table 3-1 Secondary PCI Device Address Mapping Requirements

Device	Graphics Board(s)	Memory Type	Required Address Space
82C861 USB Controller	VCQ, VFG	Registers	4 KB
Bt848A Channels A & B	VFG	Registers	4 KB per Channel
CL-GD7555 Channel A	All	BIOS PROM	64 KB
CL-GD7555 Channel A, B	All	Registers	1 KB per Channel
CL-GD7555 Channel A, B	All	Memory	16 MB per Channel
CL-GD7555 Channel C, D	VCQ	Registers	1 KB per Channel
CL-GD7555 Channel C, D	VCQ	Memory	16 MB per Channel

You can visit the TI web site for more PCI2031 information:
http://www.ti.com/sc/docs/folders/analog/pci2031.html

Serial EEPROM

The graphics board includes an Atmel AT24C02 (or equivalent) 2 Kb (256 bytes) I^2C Serial Electrically Erasable Programmable Read Only Memory (EEPROM). The programming of the Serial EEPROM is done through control lines on the PCI2031 PCI to PCI Transparent Bus Bridge. After a reset on the PMC host bus, the PCI2031 bridge downloads seven bytes of vendor specific data starting at EEPROM address 0. The slave address of the EEPROM must be at 10100000 for the PCI2031 to see it.

The EEPROM is programmed using the standard Philips I^2C two wire system. See http://www-eu.semiconductors.philips.com/acrobat/various/I2C_BUS_SPECIFICATION_2.pdf. In general, the method for accessing the EEPROM is to use S_GPIO0 to clock commands and data into or out of the EEPROM, with data passed to the EEPROM over S_GPIO1.

PCI2031 Signal Name	EEPROM Mnemonic	Description
S_GPIO0	SCL	Serial EEPROM clock
S_GPIO1	SDA	Serial EEPROM data input/output

Serial EEPROM Data Format

Rastergraf reserves the first 128 bytes of the 256 byte Serial EEPROM for internal use. This includes the seven PCI2031 bytes. The remaining 128 bytes are left for user data.

Table 3-2 PCI2031 Serial EEPROM File Data

Address	Data	Board	Comments
0	0xB4	VCQ-M	Subsystem ID high byte
	0xB6	VFG-M	
1	0		Subsystem ID low byte
2	0x10		Subvendor ID high byte
3	0xF0		Subvendor ID low byte
4	0		Device Mask
5	0		Device Type
6	0		Slot Number
7-255	0		Not Currently Used

3.3 CL-GD7555 Graphics Controller

The Cirrus Logic ***Matterhorn CL-GD7555*** (7555) is a 64-bit hard-wired graphics controller with accelerated 2D patterned lines and BLT engine. It provides a high performance PCI 2.1 compliant interface with no additional external logic required. Software may interact with the CL-GD7555 by directly manipulating pixels through the Memory Windows interface. The CL-GD7555, although not the most advanced graphics processor, does support a double-buffered command interface which allows the execution of one drawing command while another is being loaded in.

The CL-GD7555 is implemented in a 0.5 micron 3.3/5 volt CMOS custom ASIC process and is packaged in a 256 fine pitch PQFP (Plastic Quad Flat Package).

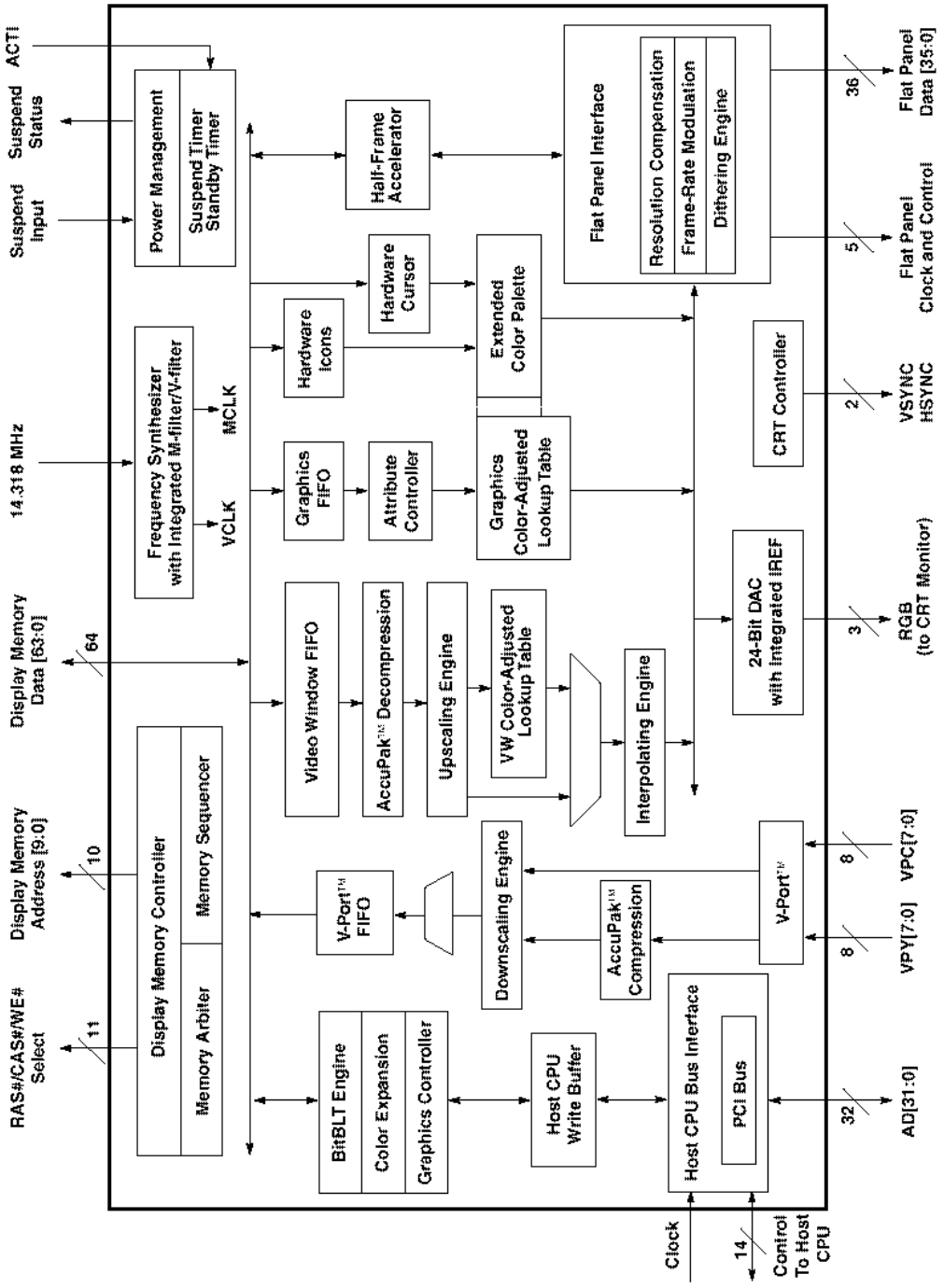
Key Device Features:

33 MHz PCI 2.1 host interface clock.
Asynchronous graphic processor.
EDO Memory controller supports high speed image transfer.
Integrated VGA.
Integrated display controller
Primary and Overlay displays
Integrated Color space converter.
Directly supports 8, 16, 24 bits per pixel
Two Operand BitBLT.
Scaling with X and Y interpolation.
Line drawing with patterning.
Interrupts from the raster line counter and the drawing completion status
4 MB of EDO DRAM display memory

The CL-GD7555 is called hard-wired because it cannot execute a program. It just has the ability to execute graphics commands given to it by the host CPU. Nevertheless, its lack of flexibility is made up for by its speed.

This manual section is devoted to describing some of the implementation details of the CL-GD7555 as used in the VCQ-M and VFG-M and reviewing some of its features. Please refer to the Rastergraf web page for a complete manual set, which contains detailed hardware and programming information.

Figure 3-1 CL-GD7555 Block Diagram



3.3.1 Memory and Video Clocks

The CL-GD7555 has a 14.318 MHz oscillator input which serves as the reference for its two on-chip PLL clocks. The CL-GD7555 derives its memory timing from the MCLK PLL which is **independent** of the video PLL clock (VCLK). Typically, the memory clock is 100 MHz, while the video clock is 135 MHz. The CL-GD7555 has internal FIFOs that take care of synchronizing display refresh memory accesses (MCLK synchronous) to display output functions (VCLK synchronous).

Note that if the VCLK frequency is very close (e.g. 1024 x 768 display) to the MCLK frequency that it is advisable to link the VCLK to the MCLK PLL to avoid PLL jitter. This is done by setting up the VCLK PLL control register correctly in the CL-GD7555, not with a (hardware) jumper.

When the graphics board powers up, MCLK defaults to 42.955 MHz and the VCLK to 25.180 MHz, which can be used to provide VGA compatible timing. Once the VGA BIOS (or, if in a non-PC environment, SDL or PX Windows software) is executed, the MCLK and VCLK PLLs can be programmed to select higher frequencies in accordance to the desired display format and memory timing.

A consequence of the dual clock nature of the CL-GD7555 is that if you read a register driven by the pixel clock (e.g. VCOUNT), you may get erratic results. You have to read the comparison flag or use interrupts to get correct results. The reason for this is simple: the VCOUNT register can change state in the middle of a CL-GD7555 read cycle. Its operations are totally asynchronous to the CL-GD7555 PCI bus interface clock.

3.3.2 Display Memory (DRAM)

The CL-GD7555 operates on memory in 1, 2, 4, or 8 byte segments. It also supports page-mode read and write memory accesses for maximum memory performance. For graphics operations, CL-GD7555-based foreground and background color registers, block fill and writemask functions are supported. The writemask operation is write enable per bit enable function which allows direct writes instead of read-modify-writes.

Note, that the CL-GD7555 **registers** must be accessed as byte (8-bit) locations by the PCI bus.

Each CL-GD7555 has four 16 Mbit (1M x 16) EDO DRAMs. You will notice that this adds up to 8 MB. However, the CL-GD7555 can only address 4 MB. Even so, in order to gain access to 4 MB, the two RAS lines (RAS0, RAS1) are OR’d together and used as RAS for the DRAM. RAS1 is connected to the high order address line for the DRAM. It is

required that 1K refresh (symmetric) parts be used. A gate delay from the OR gate ensures adequate address setup time.

Since the DRAM is single ported, the CL-GD7555 has to use a part of each horizontal line time in reading some display data from DRAM into an on-chip FIFO, from which the data is fed to a the color map and RAMDAC, to be output to the monitor.

Parameters in the CL-GD7555 allow the user to control how much drawing time is allocated versus refresh time. This can become a concern if you are using large (24 bit pixels) at high resolution, as a lot of CL-GD7555 bandwidth will be used in display refresh.

CL-GD7555 Offscreen Memory

Any memory which is not used for the active display area is considered to be offscreen memory. You can render to it and store pixmaps in it. Then, you can either pan to that newly created display or BitBLT the offscreen data to a static display window.

3.3.3 General Display Information

The display memory data is directed to the monitor via the CL-GD7555's on-chip FIFO and integral color map (RAMDAC) which provides a single programmable 24 bit wide color map (8 bits each red, green, and blue). The color map drives both the analog RGB DAC outputs.

Color Map and Overlays

The CL-GD7555 RAMDAC provides VGA compatibility, PLL pixel clocks, and a two-bit cursor with a 64 x 64 x 2 bit map.

In the case of 8 bpp operation, the pixel is used as an index into the lookup table, giving 256 colors out of a palette of 16.7 Million (2 * 24). When used in 15, 16, or 24-bit true color modes, the pixel data can be used either in direct (unmapped) or mapped modes. The mapped mode allows the pixel data to index into the color map so that the colors may be altered without having to rewrite the underlying pixel data.

There are two practical ways to support overlay. But note that the CL-GD7555 doesn't have a separate overlay Color Lookup Up Table (CLUT).

a) a programmable color key register compares the current pixel to the color key value. When there is a match, 8 bits of the pixel data is taken from the correct place in "video window" memory and used as an index to the CLUT to select an overlay color.

b) The “video window” is enabled and “punches” a hole in the normal viewable display. The pixel data is either 422 YUV data converted on the back end of the video window memory to RGB or else a packed pixel 15, 16 or 24 bit true color RGB data. The YUV data is to be preferred because it uses a lot less memory.

Graphics Cursor

The CL-GD7555 graphics cursor has a 64 x 64 x 2 bit map, position match registers, and counters triggered by the dot clock and referenced to horizontal and vertical sync.

The CL-GD7555 can supply a bit-map and/or a cross-hair cursor. The display window for the cross-hair is programmable. The CL-GD7555 CLUT has 3 cursor entries. Each table entry is a 24 bit value (8 bits each for R, G, and B). Pixel intersections between the primary, overlay, and cursor will result in a unique color, so that the pixels will still be visible. The cursor has priority over ***both*** primary and overlay pixels.

3.3.4 Other Features

The CL-GD7555 can power-power-down select unused internal functional blocks , and supports Suspend and Standby mode, VESA DPMS (display power management signaling) and DDC-2B (display data channel) monitor control. Currently, Rastergraf software support these features only under Windows NT/2K/XP.

3.3.5 The Hardware Byte Swapper

The CL-GD7555 includes a hardware byte swapper. This can be useful if you are using a PowerPC CPU to pass data to graphics memory, as the PowerPC is a big endian chip and the PCI bus and CL-GD7555 are little endian. You can save a CPU swap operation. Depending on the amount of data transferred between the CPU and the graphics memory, the swapper can give between 5 and 15% performance boost. Multiple PCI apertures support swapped and non-swapped memory access.

3.3.6 CL-GD7555 Build Options and Power-up Settings

The CL-GD7555 Technical Manual documents a number of build options and resistor settings which are read by the CL-GD7555 on power up.

Table 3-3 Resistor Options

Pin Name	Resistor Pullup	Option Chosen	Resulting Function
BIOSEN	yes	Enabled	Enables BIOS on Channel A
	no	Disabled	**Disables** BIOS on Channel B-D
INTDIS	no	Enabled	Enables PCI interrupt
MMIOEN	yes	Section 2.3	Enables Memory Mapping of registers
RIOEN	yes	Section 2.3	Enables Relocatable I/O
64KDIS	no	Enabled	Enables up to 64K BIOS
SCANEN	no	Disabled	Pin scan testing
TMEN	no	Disabled	Test mode
CMOSEN	no	Disabled	CMOS logic thresholds
XCLKEN	no	Disabled	External MCLK and VCLK
SW2-0	yes	not used	“Switch” input 2-0

3.3.7 CL-GD7555 Control Pins

The CL-GD7555 has some control pins whose uses are design dependent.

Table 3-4 Miscellaneous Control Pin Functions

Bit Name	Used	Resulting Function
ACTI	yes	Connected to USB interrupt request. Will cause CL-GD7555 to wake up if USB interrupts (probably not a useful feature).
CLK32K	yes	Used for power management features. Connected to local clock generator, F = 315 kHz.
FPVCC, FPVEE	no	
PROG2	Ch 1 only	Used only on Channel 1. Connected to write enable for 64 KB Flash PROM.
PROG1	no	
PROG0	some-times	Special feature, normally not used. Connected to A11, the display DRAM high address line (only) if 4K refresh DRAMs are used (see Section 3.4.2).

3.3.8 IDSEL Connections

Each graphics board local PCI device is connected to a unique IDSEL on the isolated side of the PCI bus, as follows:

Table 3-5 IDSEL Connections

Pin Name	Board	Bit	Resulting Function
Graphics Channel A	All	16	CL-GD7555 uses local PCI address AD16
Graphics Channel B	All	17	CL-GD7555 uses local PCI address AD17
Graphics Channel C	VCQ	18	CL-GD7555 uses local PCI address AD18
Graphics Channel D	VCQ	19	CL-GD7555 uses local PCI address AD19
Digitizer Channel A	VFG	18	Bt848A uses local PCI address AD18
Digitizer Channel B	VFG	19	Bt848A uses local PCI address AD19
USB	All	20	82C861 uses local PCI address AD20

3.3.9 Virtual Memory, Page Faults, Autoincrement Registers

When copying data into host memory from the color map auto-incrementing registers (color palettes) one must be careful about page faulting on a virtual memory machine. Before reading the color map, you should “touch” the variable(s) you are copying into to ensure that they are in CPU memory. If you don’t do this, you may get a page fault which would force a retry of the instruction. Since the color map has already been read when the page fault occurs, you will end up reading the color palette too many times.

3.4 Video Timing Parameters

The CL-GD7555 must be programmed to generate the proper video timing for the hardware configuration and display format. Rastergraf's SDL software accepts display format (e.g. 1280 x 1024, 24 bpp) and refresh requirements (e.g. 67 Hz vertical refresh) as parameters to a function call which then loads a best fit timing for the CL-GD7555 graphics chip.

Similar display format information is provided in a configuration file for Rastergraf's PX Windows server.

3.4.1 Application Note: Adjusting the Timing Parameters

Rastergraf's SDL software allows you to define the timing parameters in one of two ways:

a) the simple way, wherein you tell SDL that you are using a multiscan monitor. You specify the display active width and height (e.g. 1280 x 1024) and the Vertical Frequency, and the program figures out the rest.

b) the complete way, wherein you tell SDL exactly what you want the timing to be. You specify:

- vertical frequency in Hz
- vertical blanking in milliseconds (ms)
- vertical front porch in ms
- vertical sync width in ms
- horizontal blanking in microseconds (µs)
- horizontal front porch in µs
- horizontal sync width in µs
- display width and height

The program derives the horizontal frequency from this information.

Ordinarily, you should be able to use the monitor's data sheet to obtain a satisfactory display. If adjustments are required, this section gives you some advice on what to do. You can also supply Rastergraf with a filled-in copy of the monitor parameters sheet which follow this section. We can then assist you in solving your display problem.

Most monitors have adjustments for Horizontal Frequency, Horizontal Position, Horizontal Size, Vertical Frequency, Vertical Position and Vertical Size. It is recommended that the monitor adjustments be tried before trying monitor settings not in accord with the monitor data sheet.

To change the horizontal frequency:

The horizontal frequency is also known as horizontal refresh rate or horizontal scan rate. Indications that the horizontal frequency needs to be changed are an unviewable picture with diagonal lines. Some monitors display no picture when the horizontal frequency is out of its bandwidth. The same symptoms can be caused by no sync at all, so make sure that the cables are connected and that the monitor is configured correctly. Remember that the CL-GD7555 can supply only five wire video (RGBHV), not sync-on-green.

When the picture is out of sync, the number of diagonal lines is an indication of how close to the correct horizontal frequency you are: fewer lines are closer, more lines are farther. Remember that changing the horizontal frequency will also affect the vertical frequency. Decreasing the horizontal frequency will generally result in a wider picture.

To change the horizontal position:

To shift the image *left* **increase** the horizontal front porch by the same amount. Perform the converse procedure to move the image to the *right*.

To change the width of the image:

There are 3 ways to change the width (horizontal size) of the image.

1) Display more pixels. The aspect ratio remains the same.
2) Change the ***horizontal*** frequency. The horizontal frequency is derived from the other parameters. Increasing the horizontal frequency will result in a wider image, decreasing it will result in a narrower image.
3) Change the pixel frequency, keeping the horizontal frequency the same.

To change the vertical frequency:

The vertical frequency is also known as vertical refresh rate or vertical scan rate. Indications that the vertical frequency needs to be changed are a picture which rolls up or down. Sometimes the appearance is of multiple pictures, one on top of another, with multiple horizontal lines. An excessively slow vertical frequency will cause the image to flicker. Some monitors display no picture when the vertical frequency is out of its bandwidth. Since the same symptoms can be caused by no sync at all, make sure that the cables are connected correctly and that the monitor is configured correctly. Remember that the CL-GD7555 can supply only five wire video (RGBHV), not sync-on-green.

To change the vertical position:

To shift the image *up* **increase** the vertical front porch by the same amount. Perform the converse procedure to move the image *downward*.

To change the height of the image:

There are 2 ways to change the height (vertical size) of the image.

1) Display more lines. The aspect ratio remains the same.

2) Change the vertical frequency. Increasing the vertical frequency will result in a shorter image, decreasing it will result in a taller image.

Declaration

Rastergraf is dedicated to making your application work. We can assist in determining special video timing parameters for specific monitors and other output devices. If you need help it would be very useful if you can gather the data requested in the following form before calling us.

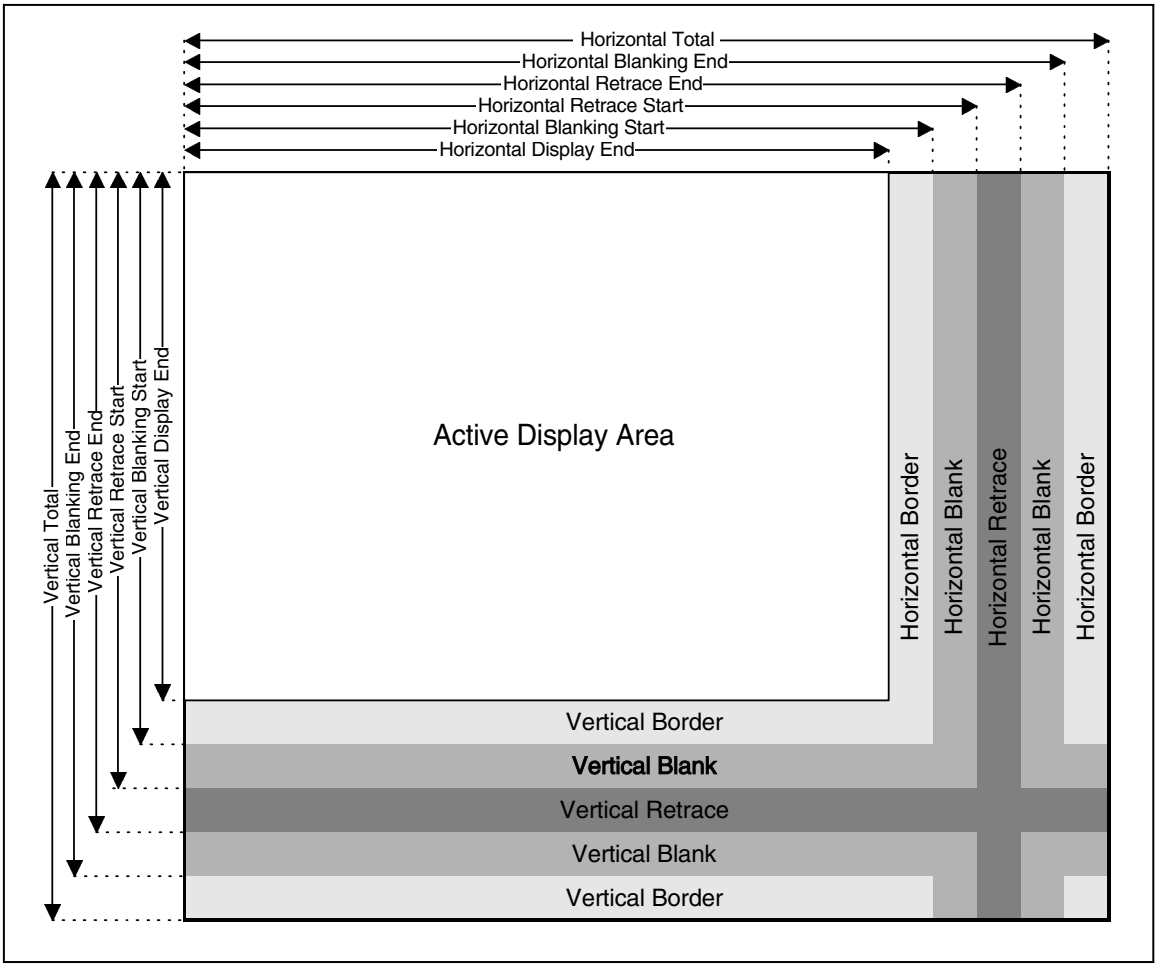
3.4.2 Other Display Features

If you take the time to read it, you will find that the CL-GD7555 manual details a number of different display features you can invoke including line doubling, overlays, and split screens. The hardest problem is that the CL-GD7555 has bits to do these things scattered all over the place, so it can take some time to unravel all that you need to do. The Rastergraf SDL software allows you to make use of some, but not all, of these functions. Please contact Rastergraf if you have questions about them.

3.4.3 Pan and Scroll

Panning and scrolling are techniques used to provide a window into a larger memory than can be displayed. This method is also called roaming. The display X (pan) and Y (scroll) starting points are changed, allowing new data areas to be displayed. This function is appropriate when using a display format which doesn't use up all 4 MB of memory. For example, a display 1280 x 1024 x 8 bpp gives you a little more than three full screens to roam around in. Routines in the Rastergraf software provide you with an easy way to pan and scroll in memory.

Figure 3-2 Video Display Timing Fields



Request for Assistance in Determining Video Timing Parameters

Submit to: Rastergraf, Inc.
Attn: Technical Support
FAX: +1 (541) 923-6475
email: support@rastergraf.com

Company Information
Company Name_____
Contact_____
Phone Number_____
Fax Number_____
email_____

Monitor Information
Monitor Brand_____ Model Number_____

Graphics Board Information
Model Number_____ Serial Number_____

Horizontal Timing Information
Note: Horizontal timings may be given in pixel units (if given) or time units.
Horizontal Pixels per Line Displayed_____
Pixel Time or Frequency (optional)_____
Horizontal Total Line Time or Frequency_____
Horizontal Front Porch_____
Horizontal Sync Width_____
Horizontal Back Porch_____

Vertical Timing Information
Note: Vertical timings may be given in line units or time units.
Vertical Lines Displayed_____ Interlaced? (Yes/No)_____
Vertical Lines Total or Frequency (Field Rate)_____
Vertical Lines Total or Frequency (Frame Rate)_____
(same as Field Rate unless interlaced)
Vertical Front Porch_____
Vertical Sync Width_____
Vertical Back Porch_____

Sync Information
Sync Polarity (+ or -): Horizontal:_____ Vertical:_____

Additional Notes
_____
_____
_____

Table 3-6 Video Timing Parameter Request Form

3.5 82C861 USB Host Controller

The OPTi ***FireLink*** 82C861 PCI-to-USB Bus Bridge is a Universal Serial Bus (USB) controller. It combines high performance features such as PCI bus mastership with compliance to OpenHCI 1.0 and USB 1.0 specifications. It is compatible with Microsoft and Solaris 8 USB drivers.

The OPTi 82C861 is a clone superset of the CMD 670/673 USB Host controller. It has some enhancements that are not used in the VCQ-M and VFG-M. You can obtain more information about the 82C861 from the Rastergraf web page or from OPTi's web page: http://www.opti.com/html/usbsolutions.html.

The 82C861's multiple-connections architecture supports concurrent operation of up to 127 physical USB devices while maintaining top speeds. Using the USB standard low-cost 4-wire cables and connectors, it supports such devices as keyboard, mouse, monitor, scanner, and printer. The 82C861 permits "Hot", insertion and removal of devices.

The 82C861's OpenHCI protocol imposes comparatively low PCI and CPU overhead, making it suitable for USB devices which require up to 12 Mb/s, the USB design limit. It supports isochronous, bulk, interrupt, and control transfer types over the same set of wires.

Isochronous (or, in non-computer-speak, isosynchronous) means all connections or circuits are synchronized using a common clocking reference. This ensures consistent delivery and minimizes jitter.

The chip also supports the transfer of multiple data and message streams between the host and devices, and provides compound device support (i.e., peripherals composed of many functions). Applications such as telephony and audio are guaranteed bandwidth and low latencies.

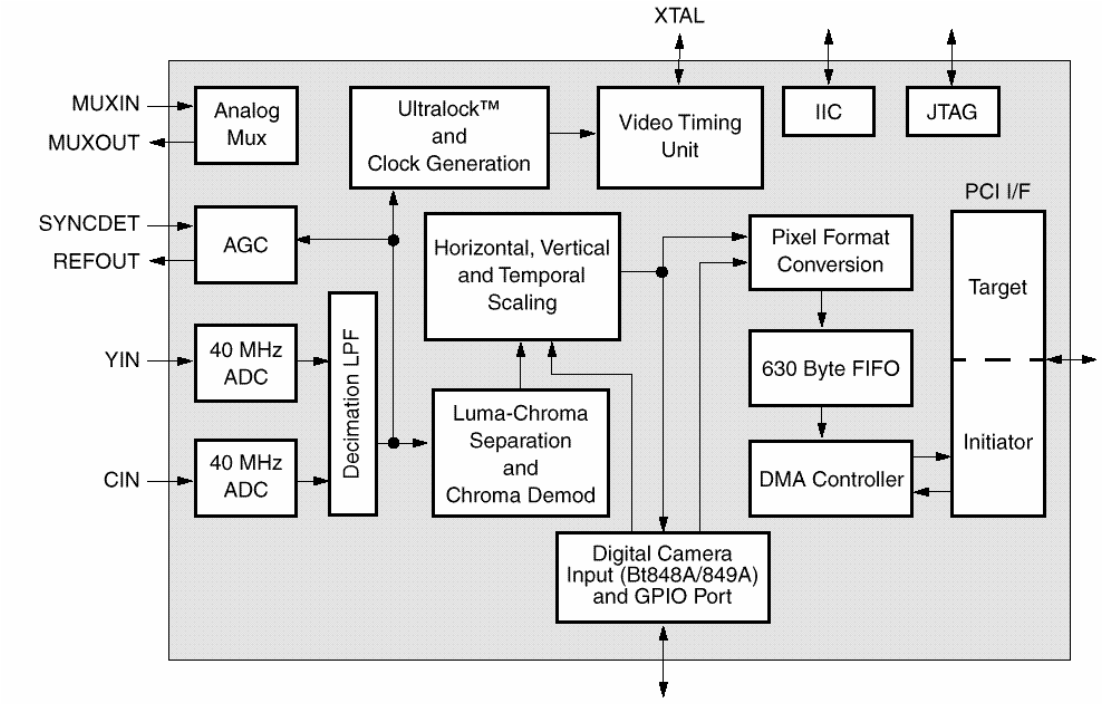
The 82C861 isochronous data transfer mode can use most of the PCI bus bandwidth, thus maximizing performance and efficiency. A wide selection of packet buffer sizes and latencies allows the maximum range of device buffering options. Flow control for buffer handling as well as an error handling/fault recovery mechanism is built into the protocol architecture.

The VCQ-M and VFG-M implement the 82C861's USB power-switching, allowing external devices to be shut off as desired. Due to a bug in the 82C861, the power indication must be hard-wired on, so you can't tell if power is actually good. But, the Micrel power control chip detects and will report overcurrent conditions, and the 82C861 will correctly report them.

3.6 Bt848A Video Digitizer (VFG-M)

Conexant's Bt848A is a complete, low-cost, single-chip solution for analog NTSC/PAL/SECAM video capture on the PCI bus. As a bus master, the Bt848A does not require any local memory buffers to store video pixel data, which significantly minimizes the hardware cost for this architecture. Bt848A takes advantage of the PCI-based system's high bandwidth and inherent multimedia capability. It is designed to be interoperable with any other PCI multimedia device at the component or board level, enabling video capture and overlay capability to be added to PCI systems in a modular fashion at low cost. The Bt848A solution is independent of the PCI system bus topology and may be used directly on a motherboard planar bus, on a card for a planar, or on a secondary bus.

Figure 3-3 Bt848A Block Diagram



3.6.1 Bt848A Features and Specifications:

Product Features

Fully PCI Rev 2.1 compliant
Auxiliary GPIO data port and video data port
Supports image resolutions up to 768 x 576 (full PAL resolution)
Supports complex clipping of video source
Zero wait state PCI burst writes
Field/frame masking support to throttle bandwidth to target
Multiple YCrCb and RGB pixel formats supported on output
Supports NTSC/SECAM/PAL analog input
Image size scalable down to icon using vertical and horizontal interpolation filtering
Multiple composite and S-video inputs
Supports different destinations for even and odd fields
Supports different colorspace/scaling factors for even and odd fields
Support for mapping of video to 225 color palette
VBI data capture for closed captioning teletext and Intercast data decoding

Applications

PC TV
Intercast receiver
Desktop video phone
Motion video capture
Still frame capture
VBI data services capture

3.6.2 Implementation

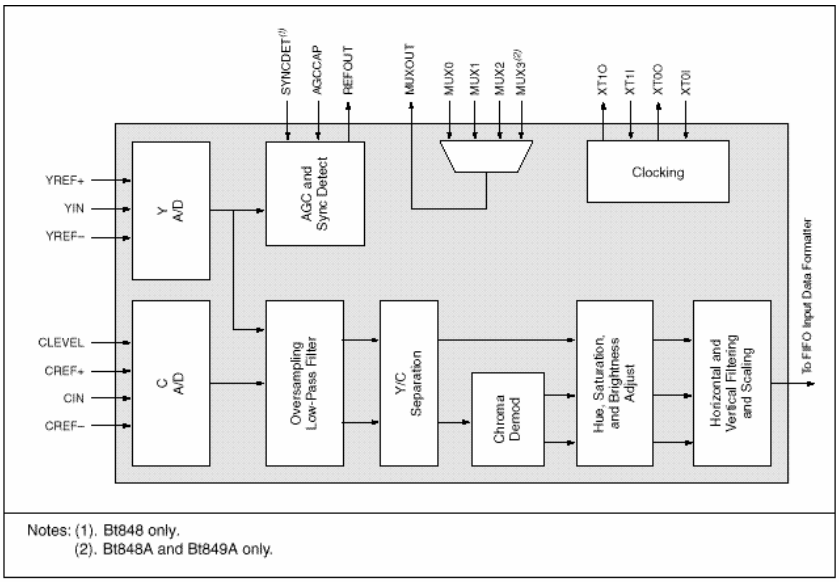
The Bt848A is packaged in a 160-pin Plastic Quad Flat Pack (PQFP) with a 28 mm x 28 mm body size. It requires only a minimum of discrete support components and no local frame buffer. It is ideal for low-cost, graphics -independent video capture solutions.

3.6.3 Video Capture Over PCI Bus

On a single device, the Bt848A integrates an NTSC/PAL/SECAM composite and S-Video decoder, scaler, DMA controller, and PCI bus master. The Bt848A can place video data directly into host memory for video capture applications and into a target video display frame buffer for video overlay applications. As a PCI initiator, the Bt848A can take control of the PCI bus as soon as it is available, thereby avoiding the need for on-board frame buffers. The Bt848A contains a small pixel data FIFO to decouple the high-speed PCI bus from the continuous video data stream.

The video data input may be scaled, color translated, and burst transferred to a target location on a field basis. This allows for simultaneous preview of one field and capture of the other field. Alternatively, the Bt848A is able to capture or preview both fields simultaneously. The fields may be interlaced into memory or sent to separate field buffers.

Figure 3-4 Bt848A Input Section Block Diagram



3.6.4 DMA Channels

The Bt848A provides two DMA channels for the odd and even fields, each controlled by a pixel instruction list. This instruction list is created by the Bt848A device driver and placed in the host memory. Instructions control the transfer of pixels to target memory locations on a byte resolution basis. Complex clipping can be accomplished by the instruction list blocking the generation of PCI bus cycles for pixels that are not to be seen on the display.

The DMA channels can be programmed on a field basis to deliver the video data in packed or planar format. In packed format, YCrCb data is stored in a single continuous block of memory. In planar format, the YCrCb data is separated into three streams that are burst to different target memory blocks. Having the video data in planar format is useful for applications where the data compression is accomplished via software and the CPU.

3.6.5 PCI Bus Interface

The Bt848A is designed to efficiently utilize the available 132 MB/sec PCI bus. The 32-bit DWORDs are output on the PCI bus with the appropriate image data under the control of the DMA channels. The video stream can easily consume bus bandwidth with average data rates varying from 44 MB/s for full size 768 x 576 PAL RGB32, to 4.6 MB/s for NTSC CIF 320 x 240 RGB16, to 0.14 MB/s for NTSC ICON 80 x 60 8-bit mode.

The pixel instruction stream for the DMA channels consumes a minimum of 0.1 MB/s. Achieving high performance throughput on PCI may be a problem with slow targets and long bus access latencies. The Bt848A provides the means for handling the bandwidth bottlenecks that sometimes occur depending on a particular system configuration. The Bt848A's ability to gracefully degrade and to recover from FIFO overruns to the nearest pixel in real-time is the best possible solution to these system bottlenecks.

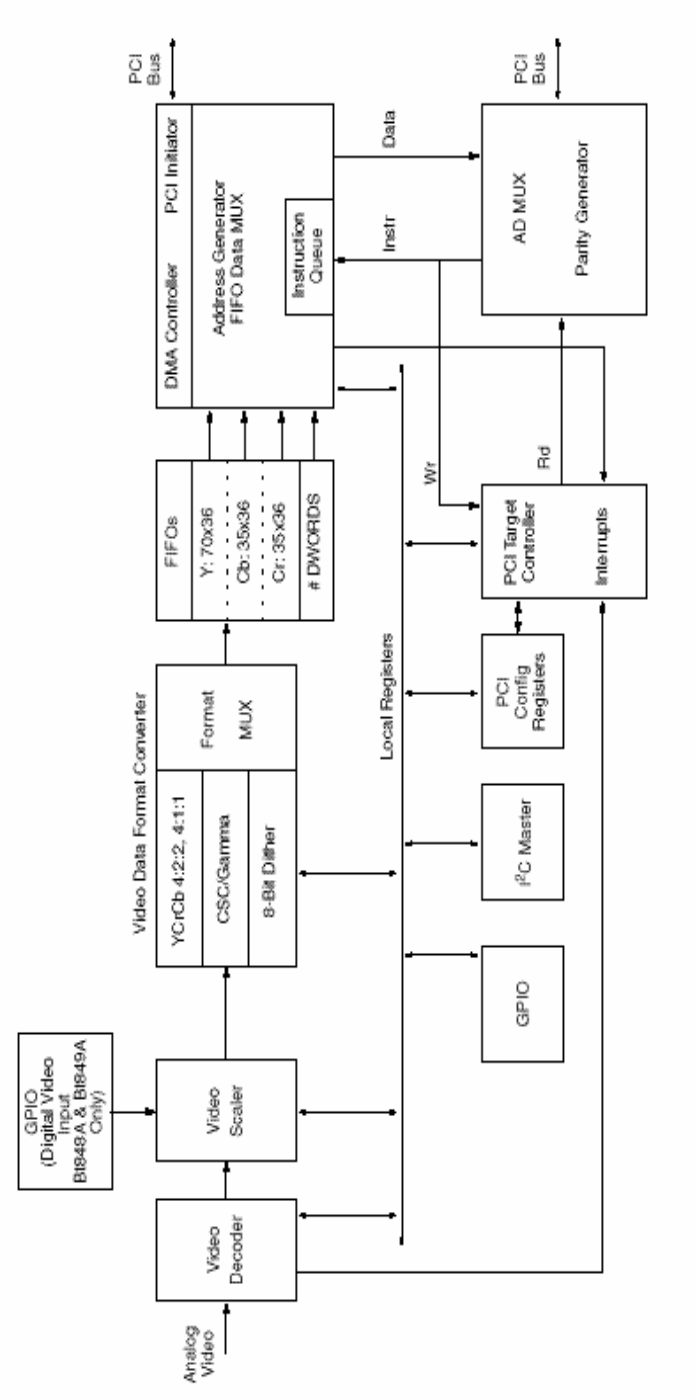
The Bt848A register set is accessed through the PCI bus. Registers can be programmed by the host using the Bt848A as a PCI target.

3.6.6 Ultralock™ and Scaling Support

The Bt848A supports Conexant's proprietary Ultralock technique that locks to an incoming analog video signal. The Bt848A will always generate the required number of pixels per line regardless of the analog video source. Ultralock is able to recognize unstable video signals caused by VCR headswitches or any other deviation and adapt the locking mechanism to accommodate the source.

The Bt848A is able to reduce the video image size both vertically and horizontally independent of arbitrarily selected scaling ratios. The X and Y dimensions can be scaled to one-sixteenth of full resolution. Vertical scaling is implemented with Conexant's industry leading 5-tap vertical filter. High quality filtering ensures applications such as Internet videoconferencing (H.323) provide the highest quality video transmissions.

Figure 3-5 Detailed Bt848A Block Diagram



3.6.7 GPIO

The Bt848A provides a 24-bit general purpose I/O bus. This interface can be used to input or output any number of general purpose I/O, up to 24 signals. Alternatively, the GPIO port can be used as a means to input or output video decoder data. For example, the Bt848A can input the video data from an external video decoder and bypass the Bt848A's internal video decoder block. Another application is to output the video decoder data from Bt848A over the GPIO bus for use by external circuitry. The GPIO port's support for burst write transfers makes the port ideal for high-speed data transmission.

3.6.8 Vertical Blanking Interval Data Capture

The Bt848A provides a complete solution for capturing and decoding Vertical Blanking Interval (VBI) data. The Bt848A can operate in a VBI line output mode, in which the VBI data is only captured during select lines. This mode of operation enables concurrent capture of VBI lines containing ancillary data and the processing of normal video image data. In addition, the Bt848A supports a VBI frame output mode, in which every line in the video frame is treated as if it were VBI line data. This mode of operation is designed for use with still frame capture/processing applications.

3.7 Interrupts

There is not a lot to say about interrupts. As required by the PCI Bridge Specification, the CL-GD7555 graphics controllers and the 82C861 USB Host controller are connected to the INTx lines as follows:

Table 3-7 PCI Interrupts

INTA: Channel A CL-GD7555 and OPTi USB 82C861
INTB: Channel B CL-GD7555
INTC: Channel C CL-GD7555
INTD: Channel D CL-GD7555

The assertion of the interrupts is under control of the graphics and USB operating software. What happens on that line at the other end (CPU side) is beyond the scope of this manual. In most cases, the interrupts are combined with other PCI slots, and the software will have to poll all PCI devices to see who made the interrupt. In some computers, such as Alphas, each PCI slot has unique PCI interrupt lines, so that it is easier to isolate down to the slot what the interrupting device is.

3.8 Diagnostic LEDs

The graphics boards have an optional set of three LEDs that can be used by host software as an aid to troubleshooting or other purposes.

The Red, Amber, and Green LEDs are driven by PIO3, PIO2, PIO1 (respectively) on the graphics board PCI2031 bridge chip (PCI register 0x74).

3.9 Flash EEPROM

The graphics board Channel A has a location for installing a 64KB 32-pin Flash EEPROM. Depending on whether the board is built for 3.3V or 5V memory, the board will use AM29LV0x0 (3.3V) or AM29F0x0 (5V), where x is either 1 or 4. The 1 or 4 corresponds to 1 Mb or 4 Mb memory size. Either will work because the high three address lines are connected to ground (=0).

The code in the PROM cannot be directly executed. It must be read by the host CPU into its memory. The CL-GD7555 has a special PROM data cycle that it executes allowing a PROM address to be asserted on the high part of the CL-GD7555's local memory data bus and PROM data to be read back on the low part of the bus.

As far as programming the flash, the CL-GD7555 design did not consider a soldered-in unprogrammed part, so there is no convenient way to write it. In order to work around this, we do a trick. We write the PROM in Display Memory address space with a data word that is actually both address and data. Here are some notes regarding programming the PROM:

PROM Read Notes

a) PROM reads only work at the PROM BAR address and if PROM is enabled (PROMBAR bit 0 = 1);

b) Enabling PROM causes a spurious PROM read. This is not desirable when executing a programming sequence. To block a spurious read, SR2F:7 (**PROG2**) bit must be set during the enable;

PROM Write Notes

a) PROM writes must be 32 bit accesses to Display Memory BAR address base + 0x200000 with address in bits 23-8 and data in bits 7-0 (of 32 bit word);

b) PROM writes only work if PROM is disabled (PROMBAR bit 0 = 0) and SR2F:7 (**PROG2**) bit set;

c) after doing writes the WE stays asserted even when PROM is enabled so one must do a (non-PROM) dummy read to de-assert WE before enabling PROM.

Chapter 4
Troubleshooting

Introduction

This chapter contains information which should assist you in tracking down installation and functional problems with your board.

4.1 General procedures

4.2 Dealing with the PCI bus

4.3 Maintenance, Warranty, and Service

4.1 General Procedures

The graphics boards were designed with reliability and durability in mind. Nevertheless, it may happen that a problem will occur. This section is devoted to aiding the user in tracking down the problem efficiently and quickly.

You may be able to locate minor problems without technical assistance. Before placing a service call, try to solve the problem by following the directions given below, in Table 4-1. If the problem can not be remedied, Rastergraf can then issue a Return Material Authorization (RMA) so that the board can be returned to the factory for quick repair.

It can happen that installing a new board will overload the computer's power supply if the power supply margins are exceeded. The first step in ascertaining if this is the problem is to calculate a power supply budget. This involves adding up the power requirements of each board in the system to see if you are within specification. Consult your computer's technical manual for information on how to correctly determine this. A typical VCQ-M or VFG-M will draw about 1.5 amps at +5 volts.

When attempting to verify that the power supply is working properly, it is not unusual to unplug everything and measure the supply without a load. While this practice is acceptable for linear supplies, switching supplies (which are very commonly used in computers) require a certain load before proper regulation is achieved. Typically, at least 5 Amps must be drawn from the +5 volt supply before the +12 volt supplies will give the proper readings.

It can also happen that if you build your own cables and you short +5 to ground on the graphics board front panel connector you may trigger the auto-resetting fuse which protect power supply pins when an overload occurs. The fuse resets automatically when an overload is removed.

Table 4-1 Basic Troubleshooting procedures

Fault	Possible Cause	Corrective Action
Control Panel dead - On/Off switch unlit	No AC power	Check power cord. It may have been dislodged when installing board.
On/Off Switch lit	No DC power	Check for correct +5 and +12 volts.
Cannot Boot	Cable(s) dislodged	During installation an unrelated cable can get dislodged.
Cannot read Rastergraf distribution media	Improperly inserted, damaged, or incorrect media.	Check insertion and position. Take care that media is “mounted” properly. Unix distribution uses TAR format.
No message on console terminal or messages are garbled	Terminal disconnected or not configured properly.	Make sure cable between terminal and computer is plugged into proper terminal port. Put terminal into Local mode and verify operation.
System crashes or you get a “Trap” message	Software not installed correctly	Check installation procedures. See Software Release Notes.
No image on Monitor	video cable(s) not connected properly or monitor is not on.	Check cables, replace if necessary. Be sure to initialize board with correct initialization parameters.
Image is smeared or doing flip-flops	Sync signals missing or monitor sync failure.	Make sure monitor accepts sync on green, that monitor is terminated, and the hold controls are adjusted properly. Check video timing parameters.
PX Windows Server is very slow to start up. Mouse movement is fast but windows are slow to open.	Graphics board to Host CPU interrupts are not being serviced.	Check interrupt pass/grant jumpers. Check operating system for correct interrupt configuration.
No response to mouse motion and/or keyboard entry.	Keyboard or mouse cable not plugged in. PX Windows board side server is crashed.	Check cabling. Reload software.
Board not detected by BIOS firmware or Operating System.		a) Check BIOS configuration b) Check board seating c) Check driver installation.

4.2 Dealing with the PCI Bus

Because of the nature of the PCI protocol and the way support has been implemented in the Operating Systems for PCI bus devices such as the VCQ-M and VFG-M, it is not possible to follow the same debugging strategies.

In fact, there are no address jumpers for these boards. Everything is configured in software through a set of on-board registers, which control the characteristics of the board as required by the PCI Specification.

The information used to program these registers is supplied to Operating System (OS) specific functions by Rastergraf's software. Ordinarily, several address map translations occur, including the CPU physical and virtual address maps and the CPU to PCI bridge address map.

The result of this is that the operation of the graphics board is very sensitive to the host CPU, as no standards have been adopted which guarantee, or even imply, universality among CPU boards, even if they use the same CPU and PCI bridge. Therefore, it is vital to ensure that Rastergraf can vouch for the board's operation in a particular CPU before you go crazy trying to figure out why it doesn't. Please contact us (support@rastergraf.com or +1 541-923-5530) if you have problems.

4.3 Maintenance, Warranty, and Service

Maintenance

The VCQ-M and VFG-M require no regular service, but if used in a particularly dirty environment, periodic cleaning with dry compressed air is recommended.

Because of the heat generated by normal operation of the graphics board and other boards in the system, forced crossflow ventilation is required. If forced ventilation is not used IC temperatures can rise to 60 degrees C or higher. Such high temperature operation causes IC failures and reduced MTBF. With proper forced air cooling IC temperatures will be less than 35 degrees C.

Warranty

The graphics boards are warranted to be free from defects in material or manufacture for a period of 12 months from date of shipment from the factory. Rastergraf's obligation under this warranty is limited to replacing or repairing (at its option) any board which is returned to the factory within this warranty period and is found by Rastergraf to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical abuse, electrical abuse, overheating, or other improper usage. This warranty is made in lieu of all other warranties expressed or implied. **All warranty repair work will be done at the Rastergraf factory.**

Return Policy

Before returning a module the customer must first request a Return Material Authorization (RMA) number from the factory. The RMA number must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

Customer should prepay shipping charges to the factory. Rastergraf will prepay return shipping charges to the customer. Repair work is normally done within ten working days from receipt of module.

Out of Warranty Service

Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs and must be covered by a valid purchase order. If extensive repairs are required, Rastergraf will request authorization for an estimated time and materials charge. If replacement is required, additional authorization will be requested.

All repair work will be done at the Rastergraf factory in Redmond, Oregon, unless otherwise designated by Rastergraf.

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