SL100/SL240 Hardware Reference for PCI, PMC, and CPCI Cards

Document No. F-T-MR-S2PCIPMC-A-0-AI

FOREWORD

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SL100/SL240 Dual-Port Memory FIFO U.S. Patent #6,259,648.

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Curtiss-Wright Controls, Inc. Embedded Computing
Data Communications
2600 Paramount Place Suite 200 Fairborn
Fairborm, OH 45324 USA
Tel: (800) 252-5601(U.S. only)
Tel: (937) 252-5601

FCC

This product is intended for use in industrial, laboratory, or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

As a component part of another system, this information technology product has no direct function and is therefore not subject to applicable European Union directives for Information Technology equipment.

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This manual introduces the FibreXtreme SL100/SL240 family of products, and provides guidance through the process of unpacking, setting up, and programming the cards.

> **NOTE**: Both the FibreXtreme SL100 and SL240 hardware are referred to throughout this manual as SL240. The software that supports both the SL100 and SL240 hardware is referred to as SL240, including the driver and API. Anything that is exclusive to the SL100 or the SL240 is described as such.

1.1.2 Scope

This manual contains the following information:

- An introduction to FibreXtreme SL240.
- Applications and topologies for SL240 boards.
- Instructions for installing and configuring the card.
- An operational overview of the product.
- General card specifications.
- Register set information.
- Programming information.
- Summary of the protocol used by the SL240 boards.
- Ordering information for all products mentioned in this manual.
- A brief introduction to the Front Panel Data Port (FPDP) interface.
- Definitions of words, phrases, and terms used in this manual.
- List of key words referenced in this manual.

The information in this manual is intended for information systems personnel, system coordinators, or highly skilled network users with at least a systems-level understanding of general computer processing, memory, and hardware operation.

1.1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7e.
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/). For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
C:\>ls
file1          file2              file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- *ANSI Z136.2-1988 American National Standard for the Safe Use of Optical Fiber Communication Systems Using Laser Diode and LED Sources*.
- *Draft Standard for a Common Mezzanine Card Family*: CMC; IEEE P1386, Draft 2.0, April 4, 1995.
- *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards*: PMC, IEEE P1386.1, Draft 2.0, April 4, 1995.
- *Fibre Channel Association Product Information Bulletin Revision*, December 9, 1994.
- *Fibre Channel Physical and Signaling Interface (FC-PH)*, Revision 4.3, June 1, 1994; Produced by the ANSI X3T9.3 standards group.
- *Fibre Channel Physical and Signaling Interface-2 (FC-PH-2)*, Revision 7.3, January 5, 1996; Produced by the ANSI X3T11 standards group.
- *Fibre Channel Physical and Signaling Interface-3 (FC-PH-3)*, Revision 8.6, April, 1996; Produced by the ANSI X3T11 standards group.
- *Front Panel Data Port Specifications, ANSI/VITA 17-1998*, Revision 1.0; February 11, 1999. Produced by the VITA Standards Organization.
- *IEC 825-1984 Radiation Safety of Laser Products, Equipment Classification, Requirements, and User's Guide, 2 parts*, 1993.
- *LinkXchange GLX4000 Physical Layer Switch User Reference Manual* (Doc. No. F-T-MR-L5XL144), Curtiss-Wright Controls, Inc.
- *PCI Local Bus Specification*, Revision 2.1, June 1, 1995; PCI Special Interest Group.
- *CompactPCI Specification*, Revision 3.0, October 1, 1999; PICMG 2.0; CompactPCI Power Interface Specification, Revision 1.0, October 1, 1999; PICMG 2.11; Keying of CompactPCI Boards and Backplanes, Revision 1.0, October 1, 1999; PICMG 2.10.
- Small Form-factor Pluggable (SFP) MultiSource Agreement (MSA), September 14, 2000, FO Transceiver Industry
- Curtiss-Wright Controls, Inc. – http://www.cwcembedded.com/.
- VITA – http://www.vita.com/.

1.3 Quality Assurance

Curtiss-Wright Controls' policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Curtiss-Wright Controls' Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation, and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain, and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Curtiss-Wright Controls' Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Curtiss-Wright Controls' registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **DTN_support@curtisswright.com**
- Fax: **(937) 252-1465**
- World Wide Web address: www. cwcembedded.com

1.5 Ordering Process

To learn more about Curtiss-Wright Controls, Inc. products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **DTN_info@curtisswright.com**
- World Wide Web address: www. cwcembedded.com

2. PRODUCT OVERVIEW

2.1 Overview

The FibreXtreme SL240 cards provide fast, low latency point-to-point or broadcast connections between sensors and processing devices. Curtiss-Wright Controls' SL240 family of products includes PCI, PCI Mezzanine (PMC), CompactPCI (CPCI) and Front Panel Data Port (FPDP) solutions. The FPDP versions are in two categories—a 6U VME- or PCI-based solution with standard FPDP connectors, and a rehostable Common Mezzanine Card (CMC).

The PCI, PMC, and CPCI versions provide this link via the PCI bus. The PCI bus is used in most standard PCs, and the PMC format is used in most popular single-board computers. CompactPCI is a 3U or 6U Euro card format PCI card designed as a more mechanically robust alternative to desktop PCI cards. The FPDP versions of the card provide this interface through a simple unidirectional parallel port. This port can be connected to existing FPDP equipment or can be integrated into new products (CMC). All of these variations interoperate completely on the link interface, providing seamless integration between diverse platforms.

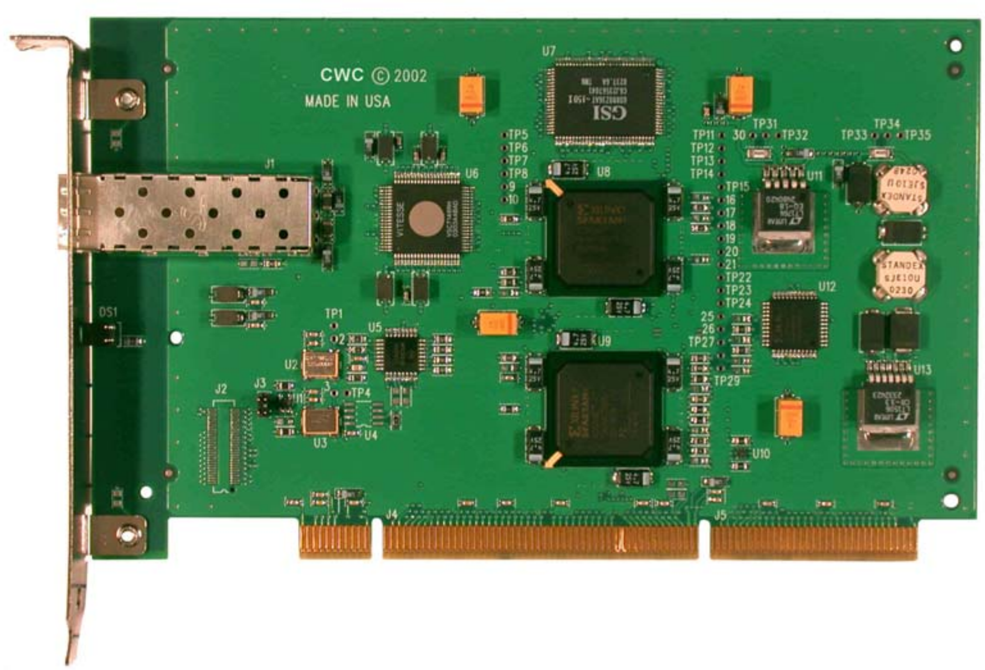

Figure 2-1 SL240 PCI 66 MHz Card

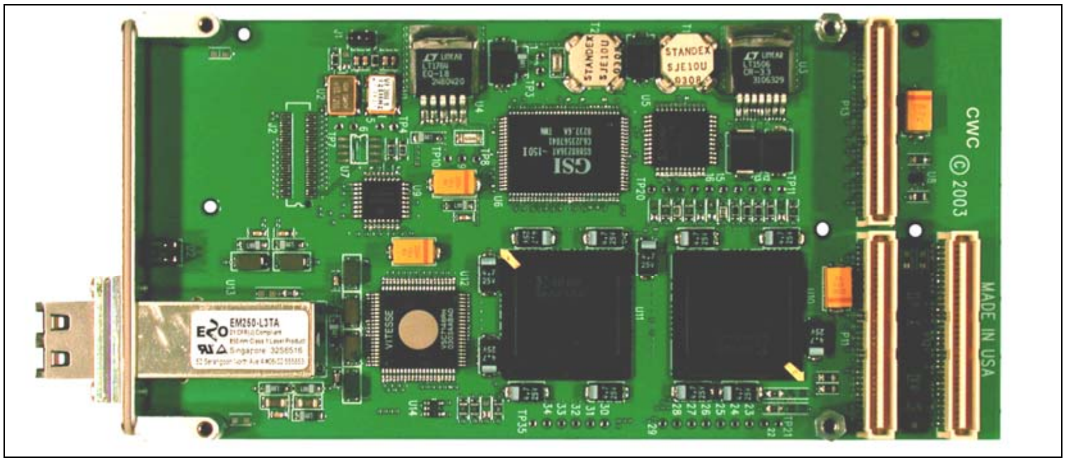

Figure 2-2 SL240 PMC 66 MHz Card

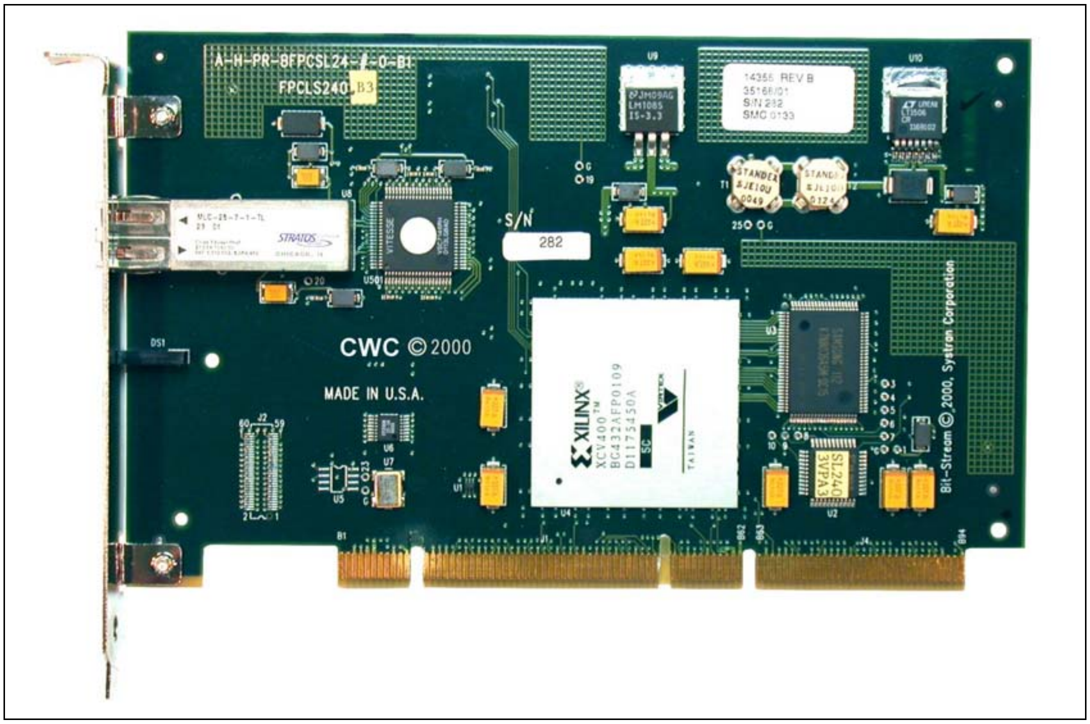

Figure 2-3 SL240 PCI 33 MHz Card

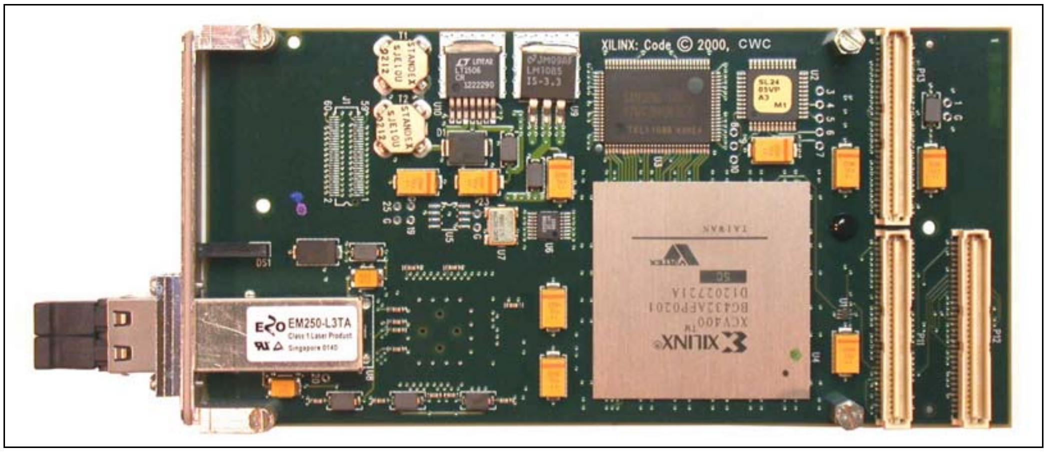

Figure 2-4 SL240 PMC 33 MHz Card

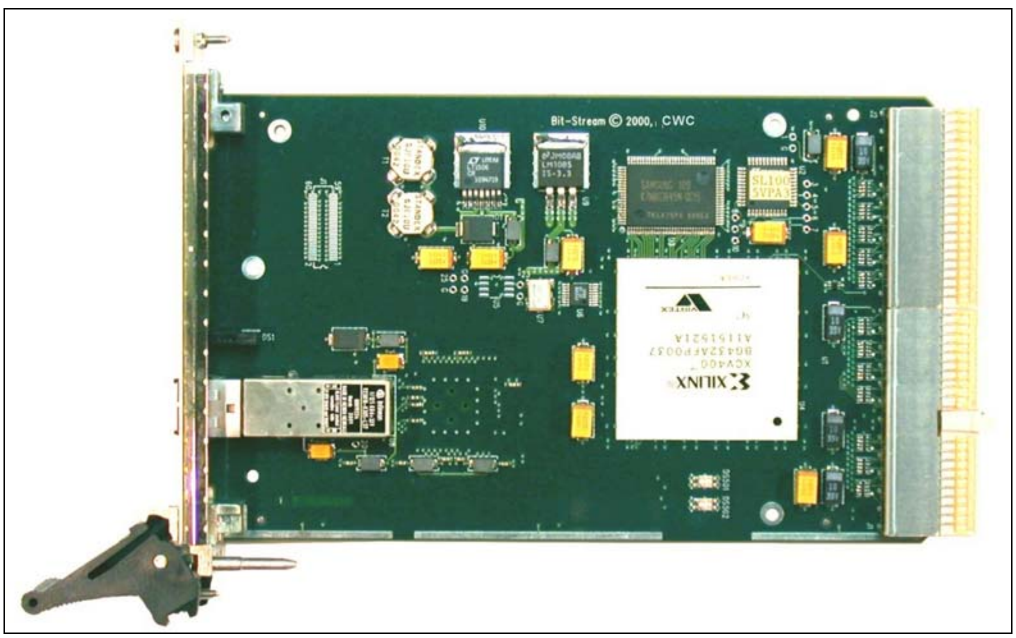

Figure 2-5 SL240 CPCI 33 MHz Card

2.2 SL240 Features

SL240 provides reliable point-to-point or broadcast interconnects between systems, with minimal overhead and very low latency. The protocol involved for this transport is based on Fibre Channel, though it is not Fibre Channel compliant. The major SL240 features are listed below:

- Uses proven 8B/10B encoding for data transmission.
- End-to-end throughput of 247 MB/s with or without frame checksums (SL240).
- End-to-end throughput of 105 MB/s with or without frame checksums (SL100).
- Minimizes implementation cost and enhances throughput by using a simple protocol.
- Provides built-in data synchronization with very little reduction in throughput.
- Integrated interrupt controller to report link failure, transaction completion, or buffer space request.
- Status LED that reports link stability.
- Loop operation with out-of-band arbitration or point-to-point operation.
- Provides a register set designed for easy programming and status retrieval.
- Four Small Form Factor (SFF) media options available—long-reach wavelength laser, long wavelength laser, short wavelength laser, and HSSDC copper.
- Small Form Factor Pluggable (SFP) on SL240 66 MHz PCI.
- SFP media options available— long-reach wavelength laser, long wavelength laser, short wavelength laser, and HSSDC2 copper.
- 64-bit operation is backward compatible to 32-bit, 33 MHz.
- SL240 66 MHz PCI support (3.3 V signaling only) in PCI and PMC form factor.
- 1 MB Receive FIFO.
- 1 KB Transmit FIFO.
- Ruggedized versions of some cards are available.

2.2.1 SFF Media Options

There are four basic SFF media options—a long-reach wavelength laser (1550 nm), long wavelength laser (1300 nm), short wavelength laser (850 nm), and HSSDC copper. The long-reach wavelength laser is required for very long distances (10 km to 50 km). Long wavelength laser interconnections are recommended for intermediate distances (300 m to 10 km). The short wavelength version is useful for intrasystem connections, such as connecting between cards on the same backplane. It is also suited for short reach intersystem connections (< 300 m). HSSDC interconnections are recommended for very short distances of 30 meters or less.

All cards use a Duplex LC style connector or HSSDC receptacle, available from most major cable manufacturers. For details concerning these connectors, contact Curtiss-Wright Controls, Inc. Technical Support.

2.2.2 SFP Media Options

The physical media interface of the SL240 66 MHz PCI design uses SFP transceiver modules. These modules are hot swappable, providing an efficient way to modify the media interface configuration as needed.

Four basic SFP media options are available for the SL240 66 MHz PCI. These media options include— a long-reach wavelength laser (1550 nm), a long wavelength laser (1300 nm) and short wavelength laser (850 nm), and HSSDC2 copper. All cards use a Duplex LC style connector or HSSDC2 receptacle, available from most major cable manufacturers.

Figure 2-6 SFP Transceiver Module

Long wavelength laser interconnections are recommended for distances longer than 300 meters, as loss in multimode fiber degrades connections with short wavelength lasers past this distance. HSSDC2 interconnections are recommended for very short distances of 30 meters or less.

The short wavelength version is useful for intrasystem connections, when connecting between cards on the same backplane. It is also suited for short reach intersystem connections (< 300 m).

The SFP transceivers comply with the Small Form-factor Pluggable transceiver MultiSource Agreement (SFP MSA) to ensure compatibility between the different transceiver manufacturers.

2.3 Applications

SL240 cards are used in a variety of topologies for a variety of applications. The following sections detail typical topologies used and some applications. Many other applications are possible in these configurations.

2.3.1 LinkXchange GLX4000 Physical Layer Switch

The GLX4000 Physical Layer Switches have the following features:

- Available in two sizes.
  - GLX4000 144 supports up to 144 non-blocking serial I/O ports.
  - GLX4000 288 supports up to 288 non-blocking serial I/O ports.
- Five port card types available for various media and data rates.
  - NRT2500, 48 port 2.5 Gbps accepts optical media Small Form Factor, Pluggable (SFP) transceiver modules.
  - RT4000, 48 port 4.25 Gbps Retimed accepts optical and copper media (SFP) transceiver modules.
  - RT10000, 12 port 10 Gbps accepts optical and copper media Small Form Factor Pluggable (XFP) modules.
  - FW1600, 48 port IEEE 1394b "Firewire" copper media.
  - ET1000, 48 port auto-negotiation 10, 100, or 1000 Mbps Ethernet with RJ-45 connectors.
- Port cards and pluggable transceivers may be mixed in one system.
- Supports Loop, Point-to-Point, One-to-Many communication links.
- Supports multiple physical media options including short wavelength (850 nm), long wavelength (1300 nm), and HSSDC2.
- Automatic port fault isolation.
- Front panel indicators.
  - “Signal Detect” for each port.
  - “Transmitter on” for each port.
  - “Heartbeat”
  - “Flash WR”
  - “Alarm”
  - “Watchdog”
- Out-of-band control through an Ethernet port.
- Can be controlled from a remote location.
- Dual-redundant hot-swappable power supplies.
- Hot-swappable fans.
- Hot-pluggable Small Form-factor transceiver modules.
- Hot-pluggable port cards.
- Multiple temperature monitoring points within the enclosure.
- Configuration data stored on a removable CompactFlash card.
- Automatic fan speed control based on enclosure temperature.
- Fan tachometer monitor.

For detailed information regarding the GLX4000 features and operation, contact Curtiss-Wright Controls, Inc. and request a copy of the *GLX4000 Physical Layer Switch Hardware Reference Manual* or visit our web site.

2.3.2 Typical Digital Signal Processing (DSP) Imaging System

With the support for 1.0625 Gbps or 2.5 Gbps link transmission rates between interconnected subsystems, SL240 is ideal for use in many of today's high-throughput data transfer applications. Figure 2-7 shows one example. This figure shows the SL100's usable data throughput rate. However, the figure is also applicable to SL240 by changing the data throughput rate to 247 MB/s.

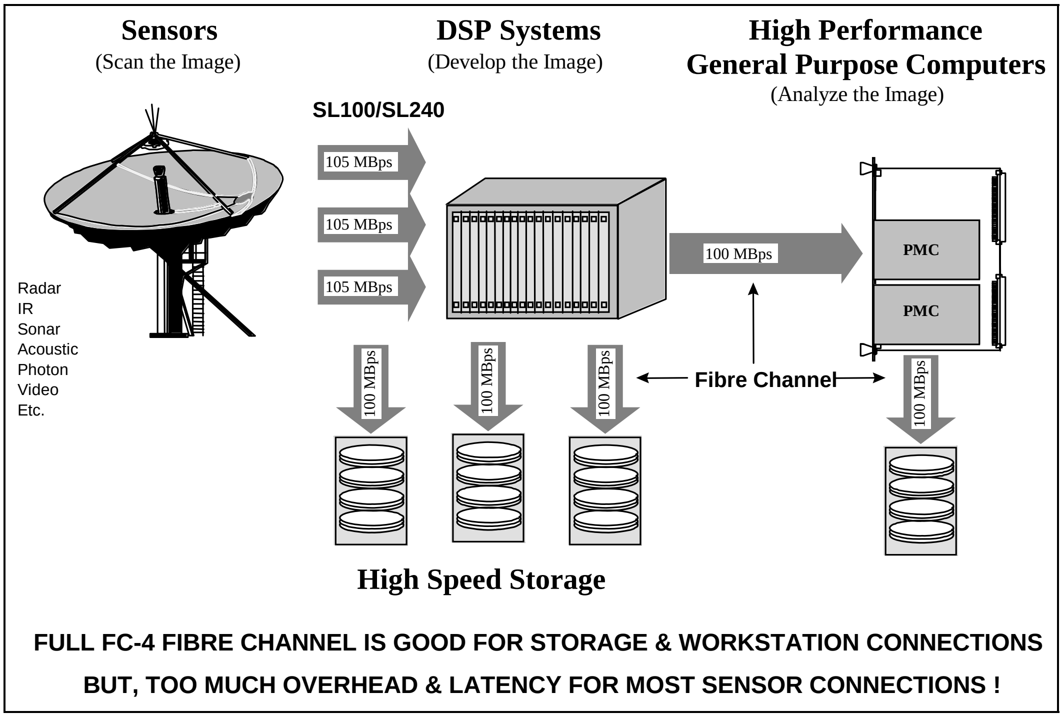

Figure 2-7 Typical Applications of FibreXtreme SL240 in Advanced DSP Systems

2.3.3 Extending FPDP

The maximum allowable length for FPDP cables ranges from 1 m to 5 m depending upon its configuration. The FibreXtreme SL240 system provides a communication link that extends the reach of FPDP while retaining simplicity, high bandwidth, and reliability. This concept is shown in Figure 2-8. The type of transceiver used determines the distance the FPDP cards can be separated. See section 2.2.1, Media Options, for details on transceivers. Using fiber optics provides electrical isolation.

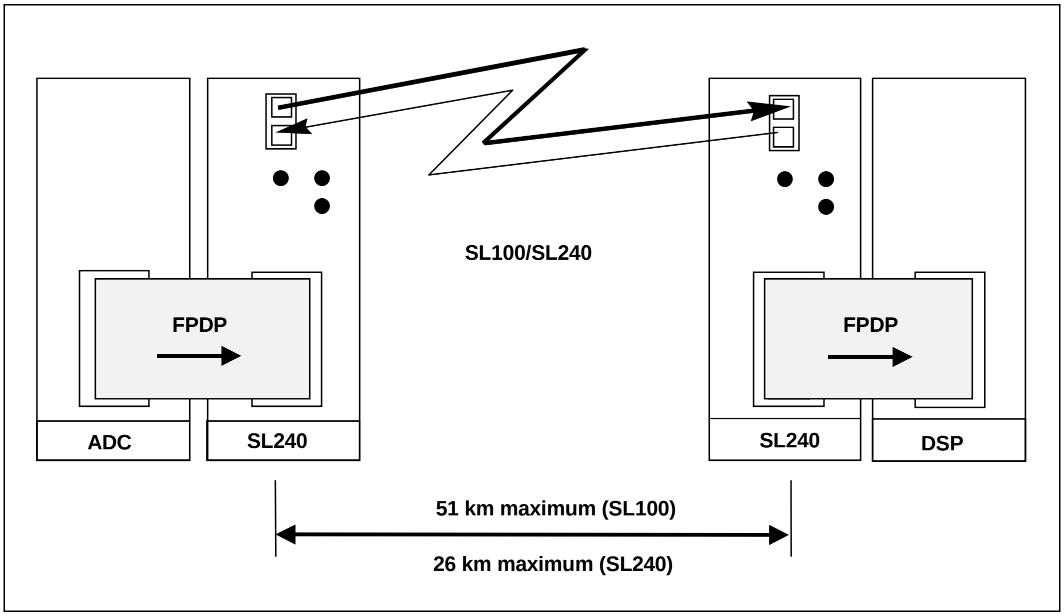

Figure 2-8 FibreXtreme SL240 Extending FPDP

2.4 Topologies

2.4.1 Typical Topologies

There are four typical topologies for the SL240 card. These topologies should cover most customer applications, though if another topology is desired contact Curtiss-Wright Controls, Inc. Technical Support to see if it is possible. The topologies are:

- Point-to-point
- Chained
- Single Master Loop
- Multiple Master Loop

2.4.2 Point-to-point

The point-to-point topology is the native mode for the SL240 card. One user option available in this mode is whether flow control is used or not. If flow control is used, the transmitter on each end will not transmit when the remote receiver is telling it to back off or the receive fiber is missing. In this mode, the maximum amount of data that can be transferred is 247 MB/s per direction (in this case, both cards are receiving and transmitting 247 MB/s at the same time). The maximum distance between the nodes is 26 km.

There are many applications for the point-to-point topology—as long as it involves only two nodes, this topology covers it. One advantage that point-to-point has over the other topologies is the ability to do simultaneous bi-directional traffic.

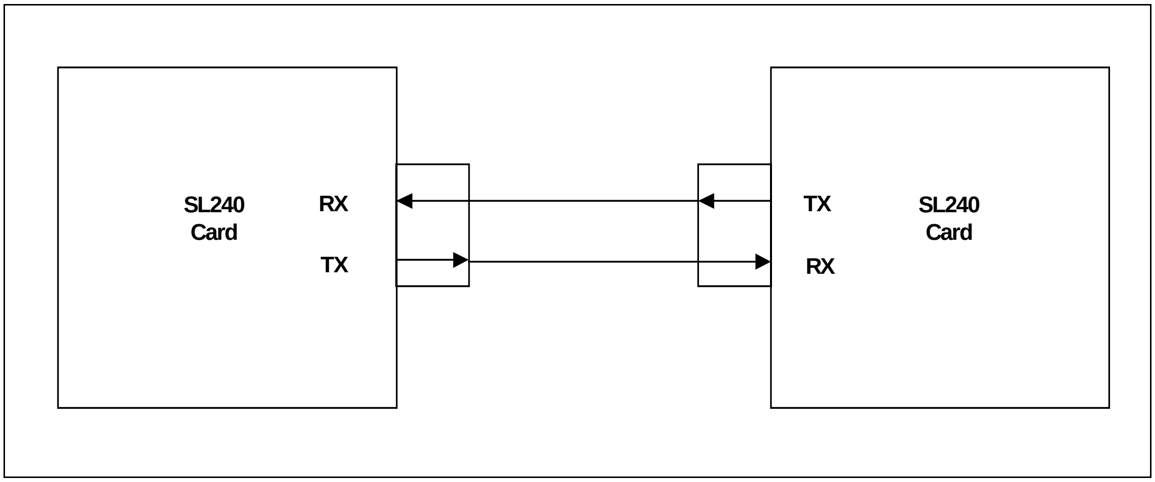

Figure 2-9 Point-to-Point Topology

2.4.3 Chained

This topology is a single transmitter on the end of a long string of receivers. No flow control is available in this topology, and the distance between the nodes is limited only by the transceivers used (10 km typical, 26 km maximum).

This topology is good for broadcasting data to multiple destinations where late data is of no use, such as video transmission applications.

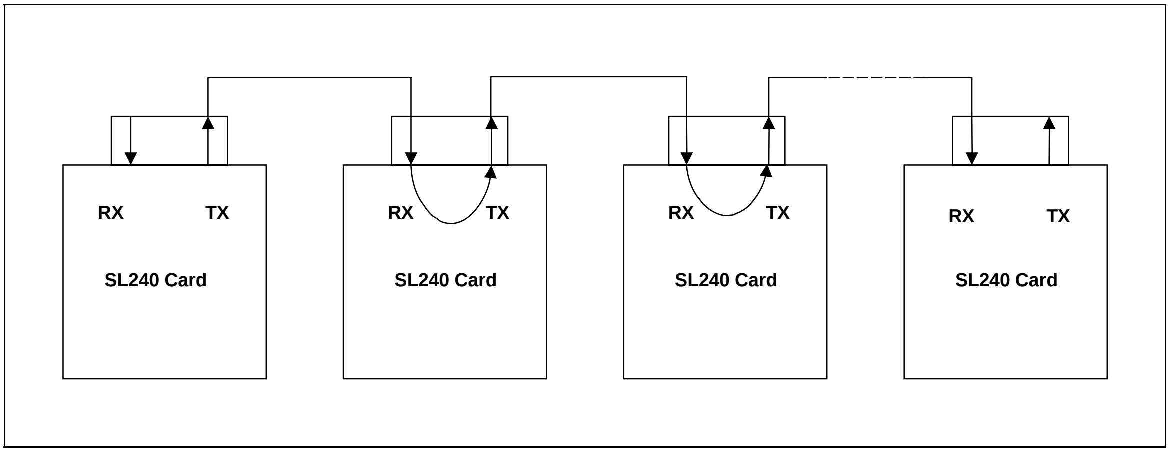

Figure 2-10 Chained Topology

2.4.4 Single Master Ring

This is one of the most useful topologies for the SL240 card. This topology allows a single transmitter to send data to a group of destinations with flow control from all of the destinations. This flow control is a single flag to the master—it can send or it cannot send data. This means that if one destination has a failure and stops removing data from its receive FIFO, it should be switched out to avoid bringing down the loop. A switch suitable for this purpose is the LinkXchange GLX4000 Physical Layer Switch, available from Curtiss-Wright Controls, Inc. Software controls mastership switching of the ring. There are rules associated with master switching listed in the “Programming Interface” section. The flow control used in this case is similar to a multi-drop FPDP bus, where any receiver can back the transmitter off.

This is the typical configuration for record-playback systems, where you have multiple signal processors and data storage elements present on the network and there is only one node (the data source or the recorder playing the data back) transmitting at a time.

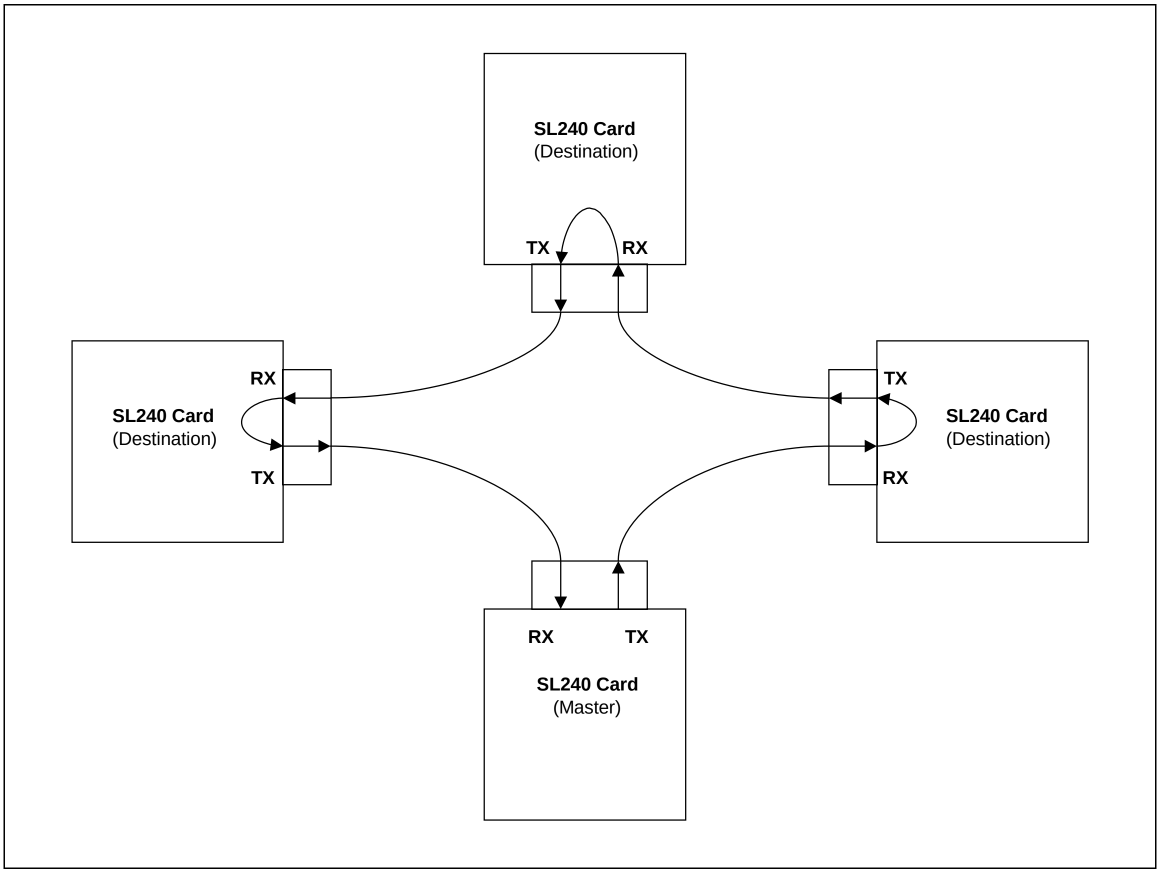

Figure 2-11 Single Master Ring

2.4.5 Multiple Master Ring

This is another form of ring topology, where there are multiple masters on the ring, and these masters have to receive data as well as transmit data to the next master. In the most complex case, each node is a master, which means that it receives data from the previous master and sends data to the next master. Flow control is not allowed in this topology for rings above two nodes, and the data cannot be passed through masters unless control guarantees that there is at least one source-only node on the ring and that no two masters will transmit at the same time. Single master rings should temporarily become multiple master rings when switching loop masters.

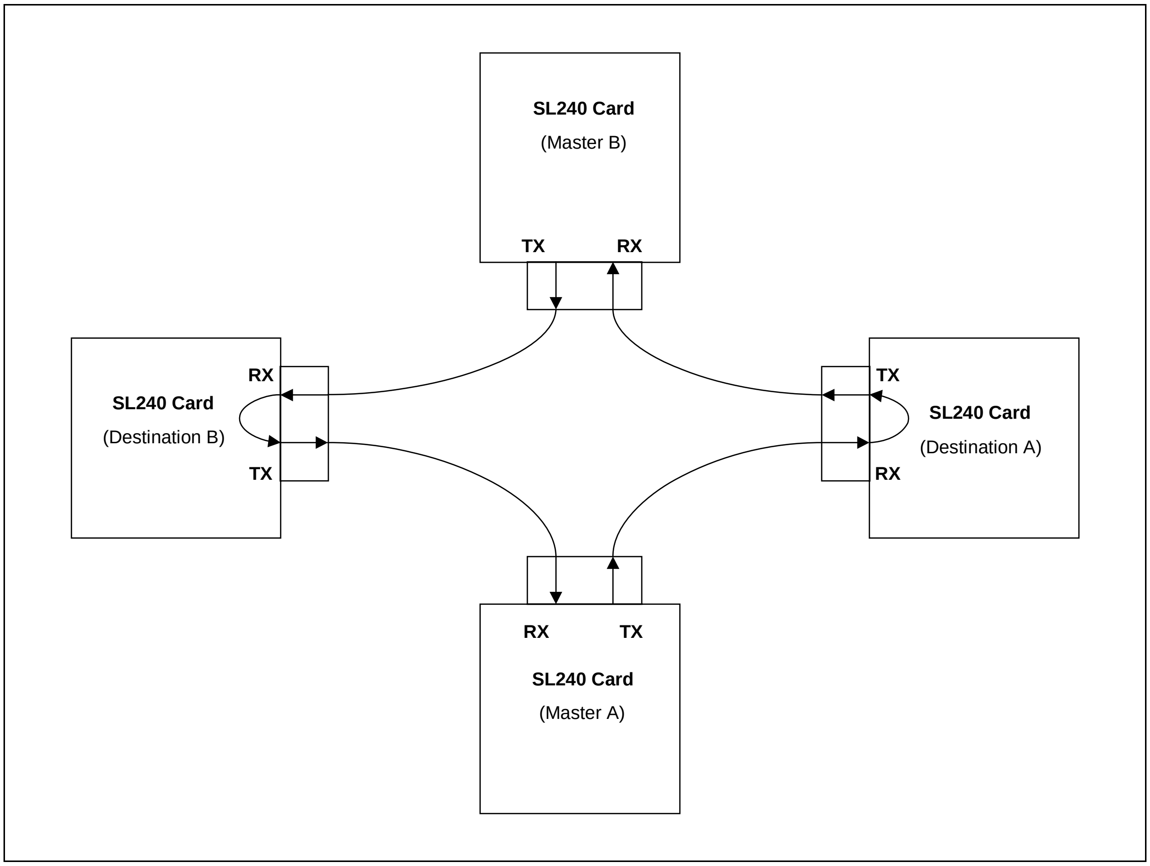

Figure 2-12 Multiple Master Ring

2.5 Status “LINK UP” LED

All of the SL240 cards are equipped with a link status indicator LED. This LED is labeled “LINK UP.” When this LED is illuminated, it indicates a signal is present on the receiver. This LED gives no indication of the validity of the signal, only that a signal is present.

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3. INSTALLATION

3.1 Overview

SL240 cards require only one slot on the host computer backplane and interface directly to a fiber-optic, HSSDC, or HSSDC2 cable.

To install an SL240 card, follow the steps below:

1. Unpack the card.
2. Inspect the card.
3. Install the card.
4. Connect the cables.

3.2 Unpack the Cards

CAUTION: Exercise care regarding the static environment. Use an anti-static mat connected to a wristband when handling or installing the SL240 card. Failure to do this may cause permanent damage to the components on the card.

Follow the steps below to unpack the card:

1. Put on the wristband attached to an anti-static mat.
2. Remove the card and anti-static bag from the carton.
3. Place the bag on the anti-static mat.
4. Open the anti-static bag and remove the card.
5. In the unlikely event that you should need to return your SL240 card, please keep the original shipping materials for this purpose.

Any optional equipment is shipped in separate cartons.

3.3 Inspect the Cards

The SL240 card consists of a single card with a built-in link interface. If the card was damaged in shipping, notify Curtiss-Wright Controls, Inc. or your supplier immediately.

3.4 Configure the SL240 66 MHz PCI Card

3.4.1 Installing SFP Modules

The physical media interface of the SL240 66 MHz PCI design uses SFP transceiver modules. These modules are hot swappable, providing an efficient way to modify the media interface configuration as needed. Always take the usual precautions against electrostatic discharge when handling SFP modules.

The SFP module contains a printed circuit board (PCB) that mates to an SFP electrical connector, located within the metal SFP receptacle cage on the SL240 66 MHz PCI card.

The SFP PCB is exposed through a cutout on the back end of the SFP module. The orientation of the SFP must be correct to insert it successfully into the receptacle cage.

To insert an SFP module, hold the module with the PCB cutout facing downward toward the Sl240 66 MHz PCI card and slide it into the receptacle cage on the card. There will be a small click as the module latches into place. The SFP module is designed to only fit into the receptacle cage a certain way. If the SFP module is inserted wrong, it will not fully slide into the receptacle cage. If this happens, remove the module and reinsert it correctly.

To remove an SFP module, press or slide the latch release on the module. This is usually a button or tab on the bottom side of the module that moves toward the rear of the card. The module will pop out slightly as the latch releases. Pull the module out of the receptacle cage.

The SL240 66 MHz PCI cards are shipped with a Dust/EMI plug for each SFP transceiver receptacle. Install these in empty receptacles to prevent contamination of internal components and to optimize EMI performance.

3.5 Install the Cards

WARNING: Turn off all power to your operating system before attempting to install the SL240 Cards.

3.5.1 SL240 PCI Card

To install the SL240 PCI card, push the card into the motherboard, as shown in Figure 3-1, steps 1 and 2, until it is firmly seated. Install the mounting screw as shown in step 3.

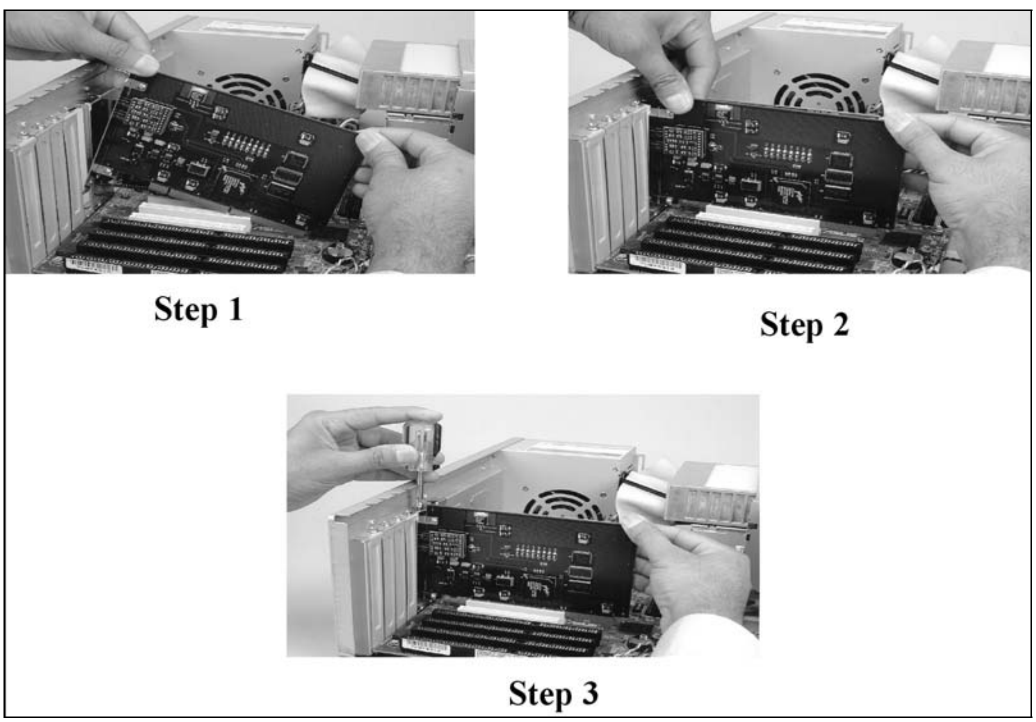


Figure 3-1 SL240 PCI Card Installation

3.5.2 SL240 PMC Card

To install the SL240 PMC card into an available carrier slot, insert the faceplate into the carrier front panel cutout until it butts up against the mating connector as shown in Figure 3-2, steps 1 and 2. Then firmly push the connectors together. Install the four mounting screws through the host PCB to fasten the SL240 PMC card in place, as shown in step 3.

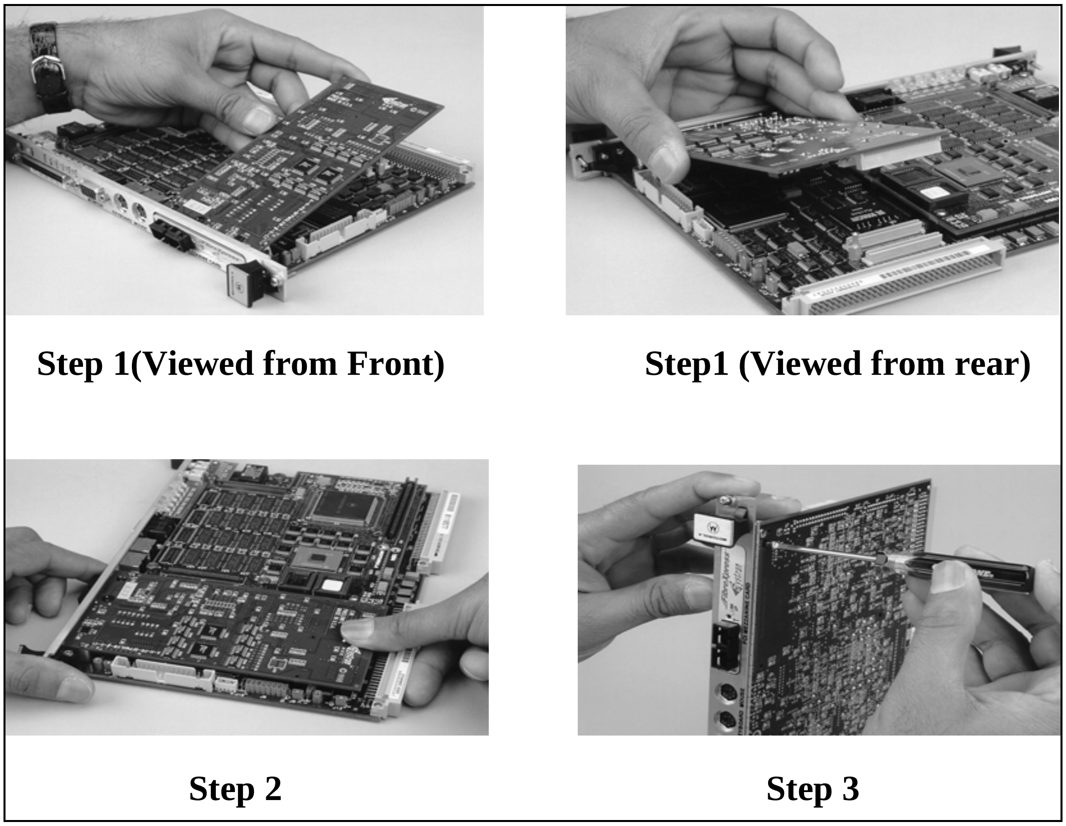
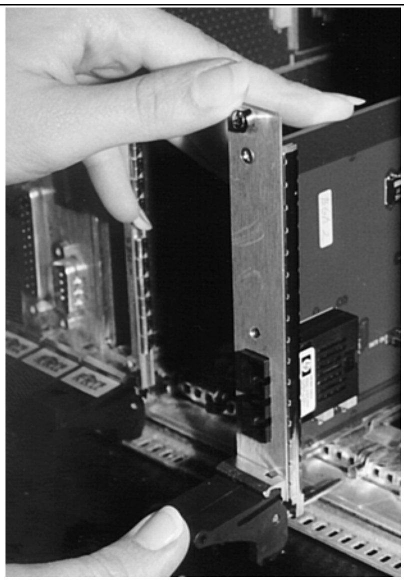


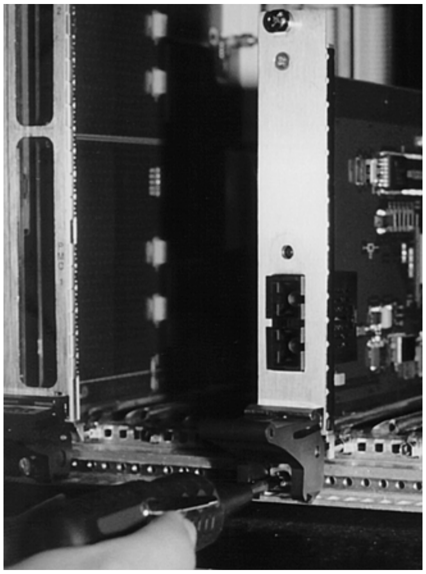
Figure 3-2 SL240 PMC Card Installation

3.5.3 SL240 CPCI Card

To install the SL240 CPCI card, push the card into the motherboard, as shown in Figure 3-3, until it is firmly seated (step 1), then install the mounting screw (step 2).



Step 1



Step 2

Figure 3-3 SL240 CPCI Card Installation

3.6 Connect the Cables

3.6.1 Transmission Media

For short wavelength laser modules, either a 50 µm or 62.5 µm core diameter cable should be used. For distances up to 300 meters 62.5 µm can be used. 50 µm cable allows distances up to 500 meters. For distances greater than 500 meters, (up to 10 kilometers,) long wavelength laser modules with 9 µm core cable should be used.

3.6.2 Fiber-Optic Cables

The two factors to consider when connecting the cables are the topology and the transmission media used. The cards can be connected in several different topologies depending on your application. See section 2.4, Topologies, for more detailed examples.

Fiber-optic Cable Precautions

CAUTION: Fiber-optic cables are made of glass and may break if crushed or bent in a loop with less than a 2-inch radius.

Look at the cable ends closely before inserting them into the connector. If debris is inserted into the transmitter/receiver connector, it may not be possible to clean the connector out and could result in damage to the transmitter or receiver lens. Hair, dirt, and dust can interfere with the light signal transmission.

Use an alcohol-based wipe to clean the cable ends.

For short wavelength laser modules, either a 50 µm or 62.5 µm core diameter cable should be used. For distances up to 300 meters 62.5 µm can be used. 50 µm cable allows distances up to 500 meters. For distances greater than 500 meters (up to 10 kilometers), long wavelength laser modules with 9 µm core cable should be used.

The optional fiber-optic cables may be shipped in a separate carton. Remove the rubber boots on the fiber-optic transmitters and receivers as well as those on the fiber-optic cables. Replace the rubber boots when cables are not in use or when the node must be returned to the factory. Attach the fiber-optic cables to the connectors on the SL240 card.

Figure 3-4 and Figure 3-5 depict the types of fiber-optic connectors needed for the SL240 card.

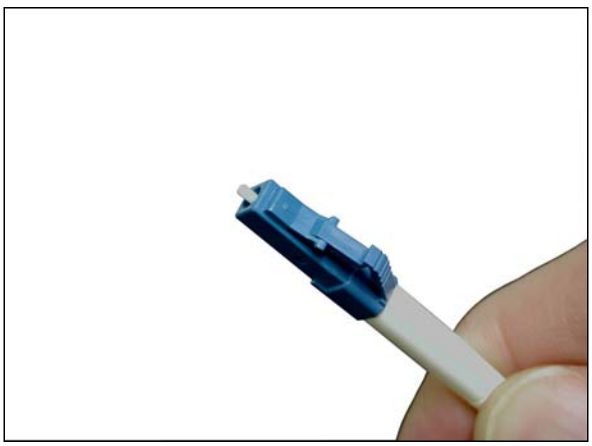


Figure 3-4 Fiber-optic Simplex LC Connector

Figure 3-5 Fiber-optic Duplex LC Connector

3.6.3 HSSDC Copper Cables

The copper media interface on the SL100 cards support 150 Ohm shielded quad cable, terminated with HSSDC connectors (“Style-2”), as shown in Figure 3-6. The HSSDC receptacle, used on the SL100 cards, is displayed in Figure 3-7. This figure also indicates the contact pin locations and Table 3-1 contains the pin assignments.

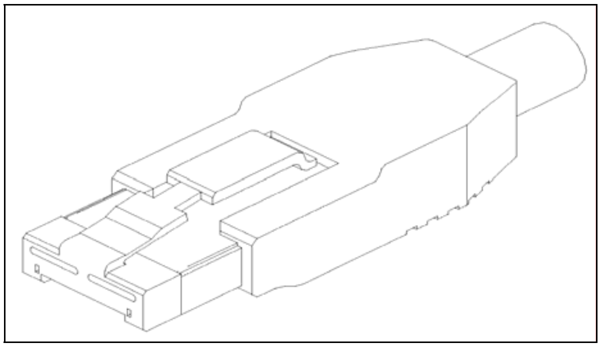


Figure 3-6 HSSDC Copper Connector

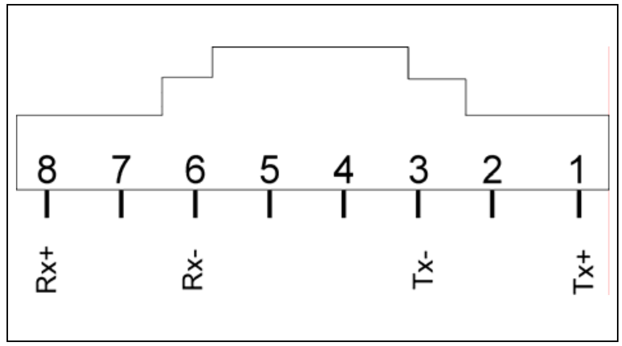


Figure 3-7 HSSDC Connector Pin Assignment

Table 3-1 HSSDC Receptacle Pin Assignments

Pin Number	Pin Description	Pin Number	Pin Description
1	Transmit +	5	NC
2	No-connect (NC)	6	Receive -
3	Transmit -	7	NC
4	NC	8	Receive +

To insure data integrity, care must be taken when selecting the appropriate HSSDC cable assembly for the SL100 application. Length boundaries for HSSDC cable assemblies are determined by the data rate of the application and if equalization circuits are present. Applications operating at 1.0625 Gbps must use equalized HSSDC cables, if cable lengths are greater than 20 meters. See Appendix D for cable descriptions, order numbers, and available lengths.

3.6.4 HSSDC2 Copper Cables

The copper media interface on the SL240 66 MHz PCI cards support shielded cable, terminated with HSSDC2 style connectors, shown in Figure 3-8. Figure 3-9 displays the HSSDC2 SFP receptacle used on the SL240 66 MHz PCI cards. This figure indicates the HSSDC2 contact pin locations and Table 3-2 contains the pin assignments.

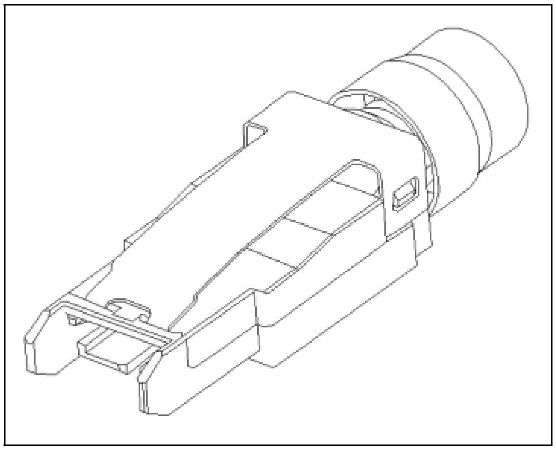


Figure 3-8 HSSDC2 Copper Connector

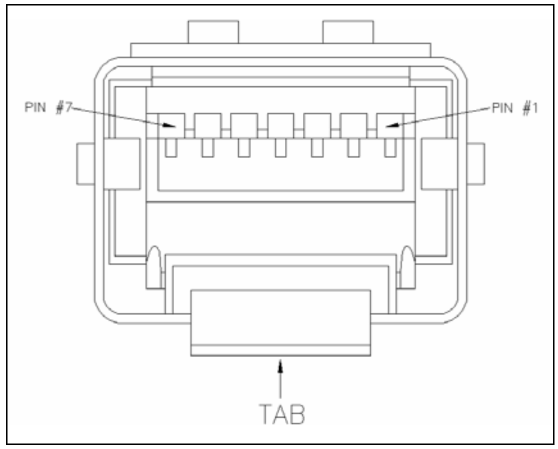


Figure 3-9 HSSDC2 Receptacle Contact Pin Locations

Table 3-2 HSSDC2 Receptacle Pin Assignments for SL100

Pin Number	Pin Description
1	Ground
2	Receive -
3	Receive +
4	Ground
5	Transmit +
6	Transmit -
7	Ground

Table 3-3 HSSDC2 Receptacle Pin Assignments for SL240

Pin Number	Pin Description
1	Ground
2	Receive +
3	Receive -
4	Ground
5	Transmit -
6	Transmit +
7	Ground

To insure data integrity, take care when selecting the appropriate HSSDC2 cable assembly for the SL240 66 MHz PCI application. Application data rate and the presence of equalization circuits determine length boundaries for HSSDC2 cable assemblies. Applications operating at 2.5 Gbps must use equalized 100 Ohm HSSDC2 cables for cable lengths greater than 5 meters. However, applications operating at 1.0625 Gbps must use equalized 150 Ohm HSSDC2 cables when cable lengths exceed 20 meters.

NOTE: The HSSDC2 cables are not interchangeable due to different keying.

3.7 Troubleshooting

If the system does not boot correctly, power down the machine, reseat the card, double-check cable connections, and turn the system back on. If problems persist, contact Curtiss-Wright Controls, Inc. Technical Support at **(800) 252-5601** or **DTN_support@curtisswright.com** for assistance.

Please be prepared to supply the following information:

Machine: ____
OS Name: ____
OS Version: ____
Card Type: ____
Card Serial #: ____
Software Part #: ____
Software S/N: ____
Problem Reproducibility: _________________________________
Problem Description: _________________________________

4. OPERATION

4.1 Overview

SL100/SL240 cards move data with very low latency between a host interface and a 1.0625 Gbps or a 2.5 Gbps link, respectively. The host interfaces available are an FPDP-like proprietary interface and a PCI interface. The advantage of the FPDP-like interface is that it requires very simplistic hardware to interface. The PCI interface will interface with any standard PCI bus, and therefore has many advantages for portability at the cost of some software overhead.

NOTE: It is not possible for SL100 and SL240 cards to communicate/operate with one another on the link because the link speeds are not compatible.

CAUTION: Do **not** break the link between two SL100/SL240 cards. The unpredictable results may affect your system. While the FPGA can recover from link break scenarios, the corresponding link and data errors caused by disruption of the link must be adequately addressed by the host interface.

4.2 Theory of Operation

The operation of SL240 cards is simple—take data from the host bus interface and transmit it across a link, or take data from the link and pass it to the host bus interface. The link protocol involved is kept minimal to reduce the latency and improve throughput, while still providing a set of useful features with which to customize your applications. The hardware offers many different features for advanced applications, while maintaining a simple interface to the most commonly used features.

NOTE: For further explanation of terms used in this chapter, refer to the FPDP Primer in Appendix E.

4.2.1 Receive Operation

The SL240 card has several options for receiving data. The most basic option is no-loop operation with data-receive enabled. In this case, data is:

1. Received from the link.
2. Decoded by the card.
3. Placed in the receive FIFO.

At this point, the operation depends on the host interface.

If it is a PCI-based card and a receive DMA is started, the data is automatically moved into the PCI address given by the DMA transaction. If no DMA is started, the data waits in the receive FIFO until the host either PIOs the data out or sets up the DMA transaction to remove it.

If it is an FPDP-based card, and /SUSPEND is not asserted, the card asserts /DVALID and proceeds to transmit the data on the FPDP interface. If /SUSPEND or /NRDY is asserted, then the data waits in the receive FIFO until these signals go away.

FPDP signals are embedded into the control words of a frame. The FPDP signals transported across are: /NRDY, /DIR, /SYNC, PIO1 and PIO2. A /SUSPEND signal is synthesized by the transmit state machine in response to how full the receive FIFO is—this is not the /SUSPEND from an FPDP port.

All FPDP signals, with the exclusion of /SYNC, are passed around the receive FIFO, and are not synchronized with the data stream. For PCI variations of this card, the FPDP signals can be read from a register once they are received from the link.

4.2.2 Transmit Operation

The transmit operation first has to collect data in the transmit FIFO for transmission. On PCI-based cards, this means that either data is PIO'd into the Transmit FIFO or a DMA transaction is set up to fill the FIFO. FPDP cards collect any data words accompanied by /DVALID on the FPDP interface. Once a data word is in the FIFO, transmission can begin. The framing-state machine first checks that there is no data in the retransmit FIFO and that the remote node is not telling this node to back off. If it is clear to send, after it transmits the next SOF it will begin filling the data frame as full as possible (up to 2048 bytes). The data is then encoded and sent out across the link. If there is data in the Retransmit FIFO or the card is being backed off from the destination, then the card waits until both conditions are clear before it starts transmission. Note that SYNC and SWDV can also be transmitted by the link logic and these two types of synchronization primitives are handled by the Transmit FIFO and transmit control logic in a similar method as standard data. Specifically, they are written to the link logic through the same interface, passed through the same internal link logic path, and are used in the assembly of link frames in a similar fashion, although the maximum frame size does differ for these types of associated Serial FPDP frames.

All FPDP signals, with the exclusion of /SYNC, are passed around the transmit FIFO, and are not synchronized with the data stream. For PCI variations of this card, the FPDP signals can be written to a register and then transmitted across the link.

4.2.3 Loop Operation

In the Loop Operation discussion below, SL100/SL240 is used generically to refer to any Curtiss-Wright Controls, Inc. SL100/SL240 card (PCI, PMC, CPCI, or CMC). Anything that applies to only a specific SL100/SL240 product will be noted as such.

Loop operation with the SL100/SL240 acts like a virtual FPDP bus where one source (the loop master) can transmit to any number of receive nodes. The link protocol is the same for this operation, except any node in the loop may assert a suspend request embedded in this data stream. This implies that if one node on the loop is not ready to receive data, the source is backed off for all nodes. This is the same way that multi-drop FPDP busses function.

The fundamental difference between a loop master and a receiving node is the loop master does not have its loop retransmission enabled. Therefore, to the loop master, it appears as if it is still in a point-to-point connection with a single node. Receiving nodes, on the other hand, have knowledge that they are in a loop configuration and must be configured as such. Note that the loop master receives all the data it transmits, so data can either be checked for errors or ignored when it is received. This checking (beyond verification of CRC and 8B/10B decoding validity) is not done in the SL100/SL240 and must be implemented by the system designer.

The receivers on the loop can choose to collect the data or ignore it off the loop. If the Receive FIFO is enabled (the node is collecting data), a suspend request may be asserted by this node as the data passes through. If it is not configured to receive the data, it simply passes the data through the Retransmit FIFO without modifying the suspend request.

Serial FPDP supports the DIR, NRDY, PIO1, and PIO2 FPDP signals. These signals do not propagate through the Transmit FIFO or the Receive FIFO and thus cannot be directly associated with the corresponding data. To guarantee a pulse on these signals is propagated to the remote Serial FPDP receiver, the pulse width from the host-bus interface must be equal to or greater than the maximum Serial FPDP frame length (512 words of data with an overhead of nine ordered sets). The use of these signals is host-specific and is explained below for each SL100/SL240 product.

For SL100/SL240 PCI-based cards (PCI, PMC, and CPCI), the values of PIO1 and PIO2 are retransmitted according to their received link values and the values of DIR and NRDY are used as follows: if the receive interface is enabled, the values transmitted are the received link values logically ORed with the PCI host-interface values; otherwise, the values are retransmitted according to their received link values. The values of these four signals sent to and received from the link are placed in the register set and then can be accessed by software. These signals are typically used for application-dependent signaling between nodes. The use of DIR and NRDY is consistent with the use of flow control (retransmission of a STOP request) for loop operation. See the VITA 17.1 Serial FPDP specification for additional details.

For SL100/SL240 CMC cards, the values of PIO1 and PIO2 are retransmitted according to their received link values and the values of DIR and NRDY are used as follows: if the receive interface is enabled, the values transmitted are the received link values logically ORed with the FPDP host-interface values; otherwise, the values are retransmitted according to their received link values. NRDY received from the link translates to /NRDY output from the FPDP receiver (FPDP-RM or FPDP-R) port. Thus, reception of NRDY from the link interface may be used to back off the FPDP transmitter, depending of the usage of /NRDY used by the respective FPDP transmit master. Curtiss-Wright Controls' SL100/SL240 CMC cards, when functioning as a FPDP transmit master, will stop the transmission of FPDP data when /NRDY is asserted by the FPDP receiver. The reception of a suspend request will indirectly back off the FPDP transmitter, as the link logic no longer transmits link data, the link Transmit FIFO will back up, which will eventually back off the FPDP transmitter via the assertion of the /SUSPEND signal. The values of these four signals (PIO1, PIO2, DIR, and NRDY) sent to and received from the link are placed on the FPDP bus and in the register set, if applicable. If placed in the register set, they can be accessed by a microcontroller via the optional microcontroller interface on the CMC carrier. The use of DIR and NRDY is consistent with the use of flow control (retransmission of a STOP request) for loop operation. See the VITA 17.1 Serial FPDP specification for additional details.

Note that NRDY as a Serial FPDP signal has no direct impact on the operation of the link logic. Rather, NRDY is passed through the link logic and its function is dependent on the respective host interface. The Serial FPDP flow control (implemented via suspend requests which are also known as STOP ordered sets) is used by the link logic and does not directly affect the interface between the link logic and host interface.

NOTE: One node on the loop MUST be in non-loop operation in order for loop operation to work correctly. One node needs to remove the data from the loop. When switching masters on the loop, both the previous master and the next master should be in non-loop operation before the previous master switches into loop mode.

4.3 Data Synchronization

The data synchronization primitive SYNC is sent across the link under user control. This primitive synchronizes with the data stream. On the PCI variations of SL240, this is written to the transmit FIFO under user control or through the transaction channels. On the FPDP variations of the card, this signal is the /SYNC line on the FPDP interface. The SYNC on PCI devices may correspond to /SYNC without /DVALID or /SYNC with /DVALID on the FPDP interface depending on the card's configuration.

Unless a non-intelligent device is used, such as a sensor, which cannot insert a periodic SYNC, SYNC should always be used to segment data transfers. It has little impact on system performance and provides a mechanism to synchronize the send and receive operations via the link. This synchronization process is especially useful at application start-up, after error conditions, and is also useful to verify the error-free flow of data during normal operation.

4.4 Configuration Options

There are many different configuration options available which affect the operation of the SL240 card. Most of these options are configured in the Link Control register (described in Appendix B).

4.4.1 Flow Control

Flow control allows a Serial FPDP receiver to throttle the data stream from a Serial FPDP transmitter. If this option is turned off, the card will continue to send data even when the receiver signals it to stop or when the link is down.

In almost every application, flow control should be enabled. Even if the application must sustain maximum link throughput, it is better to drop the data at the sending source should the system experience a temporary overload condition. In some rare cases, flow control is not desirable. In these cases, very careful system planning is required, which should be confirmed with Curtiss-Wright Controls, Inc. prior to architectural finalization. One possible exception is for applications that cannot use a duplex fiber-optic link, which means status information (link up and state of flow control) is not available from the remote node. In this circumstance, disable flow control to allow the transmitter to function without the receiver connected normally.

4.4.2 Loop Enable

The loop-enable option allows the SL240 card to transmit the received Serial FPDP data stream again. Turning on the loop enable implies that this node is designated as a receiver in the current configuration.

4.4.3 Receiver/Transmitter Enable

The transmitter-enable and receiver-enable bits in the Link Control register turn off the transmit and receive Serial FPDP data streams, respectively. Neither affects the loop operation, so data will still be retransmitted if the loop operation is enabled. This makes these options useful for record/playback systems where you wish to merely retransmit the data received without processing it. The receive-enable is useful for disabling the receive FIFO for the master in loop operation so that the data sent is not received.

4.4.4 CRC Generation/Checking

The CRC Generation/Checking option allows the SL240 card to detect data transmission errors. The card is not capable of correcting the errors. Error correction is left to application level design.

A single bit controls both generation and checking. CRC should be used in almost all applications. It offers excellent coverage of data errors and has very little impact on link throughput for maximum frame sizes. The option of disabling CRC is only retained for compatibility with older third-party devices. Both nodes on the link (or all nodes in a loop configuration) should be set to a common CRC mode or the resulting mismatch will cause data errors and/or link errors.

4.4.5 Stop on Link Error or /SYNC

There are two DMA stop conditions available to the user—stop on link error and stop on /SYNC. The stop on link error stops the DMA engine from removing data from the receive FIFO when there is a link error, such as the link going down. The stop on /SYNC option allows you to stop data from being received from the receive FIFO when a /SYNC without /DVALID is received on the output.

4.4.6 Receive FIFO Threshold Interrupt

NOTE: The Receive FIFO Threshold Interrupt is not supported in the current revision of the software. However, it may become available in a future revision.

SL240 cards can be configured to interrupt the host when the FIFO passes a certain threshold, allowing for efficient PIO transactions out of the receive FIFO. This is particularly important on data storage systems, where you do not want to remove data from the FIFO until you have a full block of data to transmit. Select one of four different thresholds through the control registers as follows:

- Not empty
- FIFO ¼ full
- FIFO ½ full
- FIFO ¾ full

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APPENDIX A

SPECIFICATIONS

TABLE OF CONTENTS

A.1 Specifications

NOTE: "Peak" current specifications are based on measurements taken while the card was transmitting and receiving large buffers of data. "Average" current specifications are based on measurements taken while the card was powered on but not transmitting or receiving any data. All current requirement measurements were taken on dual 1 GHz system.

CAUTION: Power usage is highly system dependent and varies from system to system.

A.1.1 33 MHz PCI Specifications

Physical Dimensions:................................ 174.6 mm x 106.7 mm
(6.87 inches x 4.173 inches)
Weight: .... ≈ 0.25 lbs
Operating Voltage:.................................... 4.75 V to 5.25 V
Power Dissipation:
SL100 .... 7.5 W Peak, 6.0 W Average
SL240 .... 11.5 W Peak, 9.5 W Average
Electrical Requirements:
SL100 .... +5 VDC, 1.5 Amps Peak, 1.2 Amps Average
SL240 .... +5 VDC, 2.3 Amps Peak, 1.9 Amps Average
Operating Temperature Range:.................. 0° to +50°C, with 200 LFM air (minimum)
Mean Time Between Failure (MTBF)*:
SL100, Short wavelength laser:........... 441,239 hours (50.4 years)
SL100, Long wavelength laser:........... 440,461 hours (50.3 years)
SL100, HSSDC .... 431,267 hours (49.2 years)
SL240, Short wavelength laser:........... 445,658 hours (50.9 years)
SL240, Long wavelength laser:........... 444,865 hours (50.8 years)
Storage Temperature Range:...................... -40° to +85°C

CAUTION: The *PCI Local Bus Specification* defines two signals, PRSNT1# and PRSNT2#, that indicate a PCI card is physically present in a slot and provide information on total power requirements for the PCI card. Depending on when the SL100/SL240 PCI card was manufactured, PRSNT1# and PRSNT2# may be configured to indicate the PCI card requires 7.5 W or 15 W maximum. Regardless of how PRSNT1# and PRSNT2# are configured, an SL100 PCI card dissipates 7.5 W maximum and an SL240 PCI card dissipates 11.5 W maximum.

A.1.2 33 MHz PMC Specifications

Physical Dimensions:	74.0 mm x 149.0 mm (2.913 inches x 5.866 inches)
Weight:	≈ 0.25 lbs
Operating Voltage:	4.75 V to 5.25 V
Component Density (Side View):	Side 1 – 90% (Max)** Side 2 – 90% (Max)**
Power Dissipation**:	
SL100	Side 1 – 6.5W Peak, 5.5W Average Side 2 – 2.5W Peak, 2.0W Average
SL240	Side 1 – 11.0W Peak, 9.5W Average Side 2 – 2.5W Peak, 2.0W Average
Electrical Requirements:	
SL100	+5VDC, 1.8 Amps Peak, 1.5 Amps Average
SL240	+5VDC, 2.7 Amps Peak, 2.3 Amps Average
Operating Temperature Range:	0° to +50°C, with 200 LFM air (minimum)
Mean Time Between Failure (MTBF)*:	
SL100, Short wavelength laser:	440,789 hours (50.3 years)
SL100, Long wavelength laser:	444,013 hours (50.7 years)
SL100, HSSDC	430,837 hours (49.2 years)
SL240, Short wavelength laser:	440,961 hours (50.3 years)
SL240, Long wavelength laser:	440,184 hours (50.2 years)
Storage Temperature Range:	-40° to +85°C

CAUTION: The SL100/SL240 PMC cards exceed the maximum total power dissipation specified in the *Standard for a Common Mezzanine Card Family: CMC*; IEEE P1386.

A.1.3 33 MHz CPCI Specifications

Physical Dimensions:	3U – 160 mm x 100 mm (6.299 inches x 3.937 inches) 6U – 160 mm x 233 mm (6.299 inches x 9.1732 inches)
Weight:	≈ 0.25 lbs
Operating Voltage:	4.75 V to 5.25 V
Power Dissipation:	
SL100	7.0 W Peak, 5.5 W Average
SL240	11.0 W Peak, 9.0 W Average
Electrical Requirements:	
SL100	+5 VDC, 1.4 Amps Peak, 1.1 Amps Average
SL240	+5 VDC, 2.2 Amps Peak, 1.8 Amps Average
Operating Temperature Range:	0° to +50°C, with 200 LFM air (minimum)
Mean Time Between Failures (MTBF)*:	
SL100, Short wavelength laser:	396,222 hours (45.2 years)
SL100, Long wavelength laser:	395,595 hours (45.2 years)
SL240, Short wavelength laser:	396,222 hours (45.2 years)
SL240, Long wavelength laser:	395,595 hours (45.2 years)
Storage Temperature Range:	-40° to +85°C

A.1.4 66 MHz PCI Specifications

Physical Dimensions:................................ 174.6 mm x 106.7 mm
(6.87 inches x 4.20 inches)
Weight: .... ≈ 0.25 lbs
Operating Voltage:.................................... 4.75 V to 5.25 V
Power Dissipation:
SL100 .... 8.0 W Peak, 6.0 W Average
SL240 .... 11.8 W Peak, 8.0 W Average
Electrical Requirements:
SL100 +5 VDC, 1.6 Amps Peak, 1.2 Amps Average
SL240 .... +5 VDC, 2.36 Amps Peak, 1.6 Amps Average
Operating Temperature Range:.................. 0° to +50°C, with 200 LFM air (minimum)
Mean Time Between Failure (MTBF)*:
SL100, Short wavelength laser:........... 276,007 hours (31.5 years)
SL100, Long wavelength laser:........... 279,635 hours (31.9 years)
SL100, Long-reach wavelength laser:. 203,994 hours (23.3 years)
SL100, HSSDC2 .... TBD
SL240, Short wavelength laser:........... 276,007 hours (31.5 years)
SL240, Long wavelength laser:........... 267,874 hours (30.6 years)
SL240, Long-reach wavelength laser:. 200,920 hours (22.9 years)
Storage Temperature Range:...................... -40° to +85°C

A.1.5 66 MHz PMC Specifications

Physical Dimensions:................................ 74.0 mm x 149.0 mm
(2.913 inches x 5.866 inches)
Weight: .... ≈ 0.25 lbs
Operating Voltage:.................................... 4.75 V to 5.25 V
Component Density (Side View):............. Side 1 – 90% (Max)**
Side 2 – 90% (Max)**
Power Dissipation:
SL100 .... Side 1 – 9.5 W Peak, 7.65 W Average
Side 2 – 0 W Peak, 0 W Average
SL240 .... Side 1 – 11.85 W Peak, 9.75 W Average
Side 2 – 0 W Peak, 0 W Average
Electrical Requirements:
SL100 .... +5 VDC, 1.9 Amps Peak, 1.53 Amps Average
SL240 .... +5 VDC, 2.37 Amps Peak, 1.95 Amps Average
Operating Temperature Range:.................. 0° to +50°C, with 200 LFM air (minimum)
Mean Time Between Failures (MTBF)*:
SL100, Short wavelength laser:........... 256,734 hours (29.3 years)
Rugged Level 1 .... 120,957 hours (13.8 years)
Rugged Level 2 .... 80,385 hours (9.2 years)
SL100, Long wavelength laser:........... 259,937 hours (29.7 years)
Rugged Level 1 .... 121,664 hours (13.9 years)
Rugged Level 2 .... 80,707 hours (9.21 years)
SL240, Short wavelength laser:........... 256,734 hours (29.3 years)
Rugged Level 1 .... 120,957 hours (13.8 years)
Rugged Level 2 .... 80,385 hours (9.2 years)
SL240, Long wavelength laser:........... 259,937 hours (29.7 years)
Rugged Level 1 .... 121,664 hours (13.9 years)

Rugged Level 2 .... 80,707 hours (9.21 years)
Storage Temperature Range:...................... -40° to +85°C

* The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.
** These values are calculated estimates.

> **CAUTION**: The SL100/SL240 66 MHz PMC cards exceed the maximum total power dissipation specified in the *Standard for a Common Mezzanine Card Family: CMC*; IEEE P1386.

A.2 Ruggedized PMC Environmental Specifications

The SL100/SL240 PMC products are offered at three different ruggedization levels. These levels are Standard, Rugged Level 1, and Rugged Level 2. Standard level operation specifications are defined in Sections A.1 of Appendix A. The specifications for Rugged Level 1 and Rugged Level 2 are defined in the following sections.

Current SL100/SL240 PMC standard and ruggedized products are listed in Appendix D.

A.2.1 Rugged Level 1

Temperature Range:

- Operating .... -10° to +70° C
- Storage .... -40° to +85°C

Humidity Range:

- Operating .... 0% to 95% (noncondensing)
- Storage .... 0% to 95% (noncondensing)

Altitude:

- Operating .... 25,000 ft steady; rapid decompression to 40,000 ft
- Storage .... 25,000 ft

Vibration:

- Sine... 10 g peak
10 Hz to 2 kHz
- Random .... .04 g^2/Hz
10 Hz to 2 kHz
-6 dB/octave
1 kHz to 2 kHz

Shock.. 20 g peak
½ sine wave
11 ms duration

Airflow.. 300 LFM

Conformal Coating.............................. Acrylic HumiSeal 1B31*

* Ruggedized cards are coated with HumiSeal 1B31 acrylic conformal coating. This coating is qualified to MIL-I-46058C, Type AR. More detailed information on the coating can be found at the HumiSeal website http://www.humiseal.com/.

A.2.2 Rugged Level 2

Temperature Range:	
Operating	-40° to +85° C
Storage	-40° to +85°C
Humidity Range:	
Operating	0% to 95% (noncondensing)
Storage	0% to 95% (noncondensing)
Altitude:	
Operating	25,000 ft steady; rapid decompression to 40,000 ft
Storage	25,000 ft
Vibration:	
Sine	10 g peak 10 Hz to 2 kHz
Random	.1 g^2/Hz 10 Hz to 2 kHz -6 dB/octave 1 kHz to 2 kHz
Shock	30 g peak ½ sine wave 11 ms duration
Airflow	300 LFM**
Conformal Coating	Acrylic HumiSeal 1B31*

* Ruggedized cards are coated with HumiSeal 1B31 acrylic conformal coating. This coating is qualified to MIL-I-46058C, Type AR. More detailed information on the coating can be found at the HumiSeal website http://www.humiseal.com/.

**For SL240 PMC Longwave: 600 LFM

A.3 Media Interface Specifications

A.3.1 SL100 Fibre-Optic Media Interface Specifications

Connector: Duplex LC

850 nm:

- Media: 50 µm or 62.5 µm multimode fiber
- Fibre Channel Formats: 100-M5-SN-I (1 Gbps, 50 µm fiber)
  100-M6-SN-I (1 Gbps, 62.5 µm fiber)
- Maximum Fiber Length: 550 meters with 50 µm fiber
  300 meters with 62.5 µm fiber
- Transmit Wavelength: 830 to 860 nm
- Transmit Power: -10 to -4 dBm
- Receive Wavelength: 770 to 860 nm
- Receive Sensitivity: -16 to 0 dBm

1300 nm:

- Media: 9 µm single-mode fiber
- Fibre Channel Formats: 100-SM-LL-I (1 Gbps, single-mode fiber, intermediate distance)
  100-SM-LC-L (1 Gbps, single-mode fiber, low cost long distance)
- Maximum Fiber Length: 10 km
- Transmit Wavelength: 1285 to 1330 nm
- Transmit Power: -9 to –3 dBm
- Receive Wavelength: 1100 to 1600 nm
- Receive Sensitivity: -20 to –3 dBm

1550 nm (SFP):

- Media: 8.3/125 µm single-mode fiber
- Maximum Fiber Length: 51 km
- Transmit Wavelength: 1535 to 1565 nm
- Transmit Power: 2 to 5 dBm
- Receive Wavelength: 1535 to 1565 nm
- Receive Sensitivity: -26 to –3 dBm

A.3.2 SL240 Fibre-Optic Media Interface Specifications

Connector: Duplex LC

850 nm:

- Media: 50 µm or 62.5 µm multimode fiber
- Maximum Fiber Length: 250 m with 50 µm fiber
  125 m with 62.5 µm fiber
- Transmit Wavelength: 830 to 860 nm
- Transmit Power: -8 to -4 dBm
- Receive Wavelength: 770 to 860 nm
- Receive Sensitivity: -12 to 0 dBm

1300 nm (SFP):

- Media: 9 µm single-mode fiber
- Maximum Fiber Length: 10 km
- Transmit Wavelength: 1260 to 1360 nm
- Transmit Power: -5 to 0 dBm
- Receive Wavelength: 1260 to 1580 nm
- Receive Sensitivity: -19 to 0 dBm

1300 nm (SFF):

Media.. 9 µm single-mode fiber
Maximum Fiber Length: .... 10 km
Transmit Wavelength: .... 1285 to 1335 nm
Transmit Power: .... -10 to –3 dBm
Receive Wavelength:........................... 1270 to 1355 nm
Receive Sensitivity:............................ -18 to –3 dBm

1550 nm (SFP):

Media.. 8.3/125 µm single-mode fiber
Maximum Fiber Length: .... 26 km (max), 10 km (min)
Transmit Wavelength: .... 1500 to 1580 nm
Transmit Power: .... -2 to 3 dBm
Receive Wavelength:........................... 1500 to 1580 nm
Receive Sensitivity:............................ -30 to –6 dBm

A.3.3 HSSDC Copper Media Interface: 1.0625 Gbps

Cable:.. 150 Ohm shielded, Quad
Maximum Cable Length: .... Up to 30 meters with equalized cable
Compatibility: .... 100-TW-EL-S (1 Gbps, shielded, balanced cable)
Connector:.. HSSDC (Fibre Channel “Style-2”)
Data Rate: .... 1.0625 Gbps

A.3.4 HSSDC2 Copper Media Interface: 1.0625 Gbps

Maximum Data Rate:................................. 1.0625 Gbps
Connector:.. HSSDC2 (Fibre Channel)
Cable:.. 150 Ohm shielded, Quad Copper
Maximum Cable Length: .... 30 meters (equalized cable)

A.3.5 HSSDC2 Copper Media Interface: 2.5 Gbps

Maximum Data Rate:................................. 2.5 Gbps
Connector:.. HSSDC2 (InfiniBand)
Cable:.. 100 Ohm shielded, Quad Copper
Maximum Cable Length: .... 10 meters (equalized cable)

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APPENDIX B

REGISTER SET

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TABLES

B.1 Overview

> **NOTE**: The FibreXtreme SL100 and SL240 PCI, PMC, and CPCI Cards will be referred to throughout this appendix as PCI. Anything that is exclusive to the PCI, PMC, or CPCI Cards will be described as such.

The PCI SL240 card is very easy to program. With minimal programming, the PCI SL240 card can transfer data between PCI hosts. This section details the actual bit definitions to the registers, which are explained in Appendix C (SL100/SL240 Programming).

> **NOTE**: In some cases, the Receive FIFO Threshold register shows data in the FIFO, but attempts to clear that data by reading from the FIFO fail.

B.2 Accessible resources

There are three accessible resources on the PCI SL240 card—PCI Configuration registers, the runtime register set, and the FIFO. The mechanisms for accessing these are platform specific and therefore outside the scope of this document, though the contents are detailed here.

B.3 PCI Configuration registers

The PCI SL240 card contains a standard PCI configuration space header, with the device ID of 0x4640 and the vendor ID of 0x1387. There are also two base addresses initialized for the card – the first is a 256 byte space representing the runtime registers, the second is a one-megabyte space reserved for the FIFO.

B.4 Runtime Register set

The runtime register set is accessed through 32-bit memory accesses to the Base Address 0 from PCI Configuration space. These registers represent all the configuration, control, and status registers for the PCI SL240 card. Table B-1 shows the layout of these registers in PCI space.

B.4.1 Bit Definitions

- **R/W –** Readable/Writable bit
- **R/WOC –** Readable/Write One to Clear bit
- **W –** Write-only bit
- **R –** Read-only bit

Table B-1 SL240 Register Layout

	REGISTER LAYOUT	
	4	0
0x00	Board CSR	Interrupt CSR
0x08	Link Status	Link Control
0x10	Receive FIFO Threshold	FPDP Flags
0x18	Reserved	Laser Transmitter Control
0x20	Reserved	Queue Address 0
0x28	Reserved	Queue Control 0
0x30	Transaction Length 0	Transaction CSR 0
0x38	Reserved	Reserved
0x40	Reserved	Chain PCI Address 0
0x48	Next Chain Entry 0	Chain Length/Flags 0
0x50	Reserved	Queue Address 1
0x58	Reserved	Queue Control 1
0x60	Transaction Length 1	Transaction CSR 1
0x68	Reserved	Reserved
0x70	Reserved	Chain PCI Address 1
0x78	Next Chain Entry 1	Chain Length/Flags 1
0x80 0x88 0x90 0x98 0xA0 0xA8 0xB0 0xB8 0xC0 0xC8 0xD0 0xD8 0xE0 0xE8 0xF0 0xF8	Reserved	

B.4.2 Interrupt CSR (INT_CSR) – Offset 0x00

Field	Description	Access	Reset Value
0	Transaction Channel 0 Interrupt Active – A ‘1’ indicates active, a ‘0’ indicates not active. Write ‘1’ to clear.	R/WOC	0
1	Transaction Channel 1 Interrupt Active – A ‘1’ indicates active, a ‘0’ indicates not active. Write ‘1’ to clear.	R/WOC	0
2	DMA Chain 0 Interrupt Active – A ‘1’ indicates active, a ‘0’ indicates not active. Write ‘1’ to clear.	R/WOC	0
3	DMA Chain 1 Interrupt Active – A ‘1’ indicates active, a ‘0’ indicates not active. Write ‘1’ to clear.	R/WOC	0
4	Link Error Interrupt Active – A ‘1’ indicates active, a ‘0’ indicates not active. Write ‘1’ to clear.	R/WOC	0
5	FPDP Interrupt Active – A ‘1’ indicates active, a ‘0’ indicates not active. Write ‘1’ to clear.	R/WOC	0
6	Threshold Interrupt – A ‘1’ indicates active, a ‘0’ indicates not active. Write ‘1’ to clear.	R/WOC	0
15 to 7	Reserved.	None	0
16	Enable Transaction Channel 0 Interrupt – Set to ‘1’ to enable interrupts, set to ‘0’ to disable.	R/W	0
17	Enable Transaction Channel 1 Interrupt – Set to ‘1’ to enable interrupts, set to ‘0’ to disable.	R/W	0
18	Enable DMA Chain 0 Interrupt – Set to ‘1’ to enable interrupts, set to ‘0’ to disable.	R/W	0
19	Enable DMA Chain 1 Interrupt – Set to ‘1’ to enable interrupts, set to ‘0’ to disable.	R/W	0
20	Enable Link Error Interrupt – Set to ‘1’ to enable interrupts, set to ‘0’ to disable.	R/W	0
21	Enable FPDP Interrupt – Set to ‘1’ to enable interrupts, set to ‘0’ to disable.	R/W	0
22	Enable Threshold Interrupt – Set to ‘1’ to enable interrupts, set to ‘0’ to disable.	R/W	0
31 to 23	Reserved.	None	0

B.4.3 Board CSR (BRD_CSR) – Offset 0x04

Field	Description	Access	Reset Value
0	Little Endian – Set to '1' for unswapped control registers. Setting to '0' has no effect.	R/W	1
1	Reset – Write '1' to reset the board. Writing '0' has no effect.	W	0
2	Swap data bytes – Set to '1' to 32-bit swap the data transferred through PIO transactions. '0' for unswapped transactions.	R/W	0
3	JTAG TCK# - Controls the TCK# line on the JTAG port.	R/W	0
4	JTAG TMS# - Controls the TMS# line on the JTAG port.	R/W	0
5	JTAG TDO# - Controls the TDO# line on the JTAG port.	R/W	0
6	JTAG TDI# - TDI# line from the JTAG port.	R	1
7	JTAG Enable – Enable the JTAG port on the FPGA.	R/W	0
13 to 8	Revision ID – Revision level of the board controller.	R	See desc.
14	3.3 V/5 V PCI Signaling – A '1' indicates the SL100/SL240 card uses 3.3 V PCI signaling. A '0' indicates the SL100/SL240 card uses 5 V PCI signaling.	R	See desc.
15	SL100/SL240 – A '1' indicates this is an SL240 board, a '0' indicates it is an SL100.	R	See desc.
23 to 16	Extended Revision ID – These bits are used to identify intermediate or special firmware revisions. (Note 1)	R	See desc.
24	Big Endian – Set to '1' to swap the control registers. Set to '0' for Little Endian.	R/W	0
25	64-bit transaction disable – Set to '1' to disable 64-bit transactions. Set to '0' to enable 64-bit transactions	R/W	0
26	Swap words – Set to '1' to swap words within a 64-bit transaction. Set to '0' for no swapping.	R/W	0
31 to 27	Reserved.	None	0

Note 1: Extended Revision ID.

Bits 23 and 22 of the Extended Revision ID provide information about the FibreXtreme model as follows:

00 – 33 MHz PCI based FibreXtreme products (PCI, PMC, and CompactPCI)
01 – 66 MHz PCI based FibreXtreme products (PCI and PMC)
10 – Reserved for future 33 MHz products.
11 – Reserved for future 66 MHz products.

B.4.4 Link Control (LINK_CTL) – Offset 0x08

Field	Description	Access	Reset Value
0	Allow Remote Transmitter – Set to ‘1’ to enable the remote transmitter to send link data. Set to ‘0’ to request the remote transmitter to stop sending link data. This flow control request will be ignored if the remote end is configured to ignore flow control. This signal is typically set to a '1' for most applications. It exists to provide a mechanism to disable the remote transmitter by forcing the transmitted flow control to a STOP state.	R/W	0
1	CRC Enable – Set to ‘1’ to enable the CRC checking/generation of link data. Set to ‘0’ to disable CRC checking/generation. **NOTE**: CRC should be used in almost all applications. It offers excellent coverage of data errors and has very little impact on link throughput for maximum frame sizes. The option of disabling CRC is only retained for compatibility with older third-part devices. Both nodes on the link (or all nodes in a loop configuration) should be set to a common CRC mode or the resulting mismatch will cause data errors and/or link errors.	R/W	0
2	Ignore Flow Control – Set to ‘1’ to ignore flow control from the remote end and continue transmitting when the link is down. Set to ‘0’ to stop transmission when the link goes down or the remote end is sending a STOP ordered set back. **NOTE**: In almost every application, flow control should be enabled. Even if the application must sustain maximum link throughput, it is better to drop the data at the sending source should the system experience a temporary overload condition. Some exotic conditions could apply where flow control is not desirable, but they require very careful system planning and should be confirmed with Curtiss-Wright Controls, Inc. prior to architectural finalization. One possible exception is for applications that cannot utilize a duplex fiber optic link, which means status information (link up and state of flow control) is not available from the remote node. In this circumstance, flow control should be disabled to allow the transmitter to function without the receiver connected normally.	R/W	0
3	Convert SYNC – When ‘1,’ enables detection of a received SYNC with DVALID from the link.	R/W	0
4	Stop on SYNC without DVALID – If ‘1’ then stop the Receive FIFO until software re-enables the transaction. If ‘0’ the Receive FIFO is not stopped.	R/W	0
5	Stop on receiver error – If ‘1’ then the Receive FIFO is stopped when a CRC error or FIFO overflow is taken out of its output. If ‘0’ then the Receive FIFO is not stopped.	R/W	0

Field	Description	Access	Reset Value
6	SYNC as D0 – If '1' then bit 0 of the data stream is used as /SYNC in the outgoing and incoming data stream. If '0', bit 0 is not used as /SYNC.	R/W	0
7	Reserved	None	0
8	Disable Receiver – '1' disables the link interface from placing data in the Receive FIFO. When set to '1,' this signal also prevents the modification of the DIR, NRDY, and SUSPEND flags in the retransmitted data stream if Loop (Copy) Mode is enabled. Set to a '0' for normal operation, where received link data will be placed into the Receive FIFO. When the receiver is enabled and Loop (or Copy) Mode is enabled, the status of the SUSPEND request will be updated as appropriate in the retransmitted data stream. If Loop (or Copy) mode is selected (LWRAP = '1'), the values of DIR and NRDY are used as follows: if the receive interface is enabled (Disable Receiver = '0'), the values transmitted are the received link values ORed with the host-interface values; otherwise, the values are retransmitted according to their received link values.	R/W	0
9	Disable Transmitter – A '1' disables the link interface from removing things from the Transmit FIFO. A '0' indicates normal transmit operation. Set this bit to '1' when loop mode is enabled via the LWRAP bit.	R/W	0
10	EWRAP – This signal controls loopback operation of the user interface's data stream. A '1' indicates the outgoing data stream is electronically wrapped into the incoming data stream at the serializer/deserializer. A '0' indicates non-wrapped data flow to and from the link interface. This is typically used for testing purposes.	R/W	0
11	LWRAP – This signal controls the loopback operation of the link interface's data stream and implements the Copy Mode described in the VITA 17.1 Serial FPDP specification. Set to '1' to enable loop mode, whereby the incoming data stream is electronic wrapped into the outgoing data stream internally to the FPGA. Set to a '0' for normal operation utilizing a point-to-point topology. The configuration of the nodes is intended to be static. **NOTE**: When changing loop topologies, the resulting change in the way link data is used may cause bad data or error conditions on the receiving nodes. It will be necessary to deploy a mechanism in the system to cleanup these conditions after reconfiguration.	R/W	0
12	Copy Master Mode - Set to '1' on the loop initiator device in any topology with more than two cards (e.g. loop or chained). The loop initiator will then place four IDLE ordered sets or three IDLE ordered sets plus a SWDV ordered set per fiber frame. When '0', the loop initiator will place one IDLE ordered set or one SWDV ordered set per fiber frame. All receivers in the loop or	R/W	0

Field	Description	Access	Reset Value
	chain should have this bit set to '0.' Do not set this bit to '1' on any device in a point-to-point topology (i.e. two cards) because throughput will decrease by a factor related to frame size. This bit was introduced in the revision 0x1C.13 firmware.		
13	Reserved	None	0
14	Send IDLE – Set to ‘1’ to send IDLE characters when no data is being sent. Set to ‘0’ to send empty frames when no data is being sent.	W	0
15	Reserved	None	0
16	Reset SR – Write ‘1’ to clear any latched status information from the registers. Writing ‘0’ has no effect.	W	0
17	Clear SYNC without DVALID – Write ‘1’ to release a FIFO stopped on SYNC without DVALID. Writing ‘0’ has no effect.	W	0
18	Clear Receiver Error – Write ‘1’ to release a FIFO stopped on a receiver error condition. Writing ‘0’ has no effect.	W	0
19	Erase TX FIFO – Set to ‘1’ to reset the Transmit FIFO. This bit is included for testing and special scenarios, and as such, should not be used in the majority of applications. Resetting the Transmit FIFO or Receive FIFO independently from the SL100/SL240 FPGA logic can cause undesirable effects because each 32-bit Serial FPDP data word occupies two entries in the respective FIFO and the link and host are independently filling and draining these FIFOs. Applying the FIFO resets without applying special precaution can result in a misalignment of data in these FIFOs.	W	0
20	Erase RX FIFO – Set to ‘1’ to reset the Receive FIFO. This bit is included for testing and special scenarios, and as such, should not be used in the majority of applications. Resetting the Transmit FIFO or Receive FIFO independently from the SL100/SL240 FPGA logic can cause undesirable effects because each 32-bit Serial FPDP data word occupies two entries in the respective FIFO and the link and host are independently filling and draining these FIFOs. Applying the FIFO resets without applying special precaution can result in a misalignment of data in these FIFOs.	W	0
31 to 21	Reserved	None	0

B.4.5 Link Status (LINK_STAT) – Offset 0x0C

Field	Description	Access	Reset Value
7 to 0	8B10B Errors – 8-bit counter counting the current number of 8B10B decoding errors discovered. Cleared through ‘Reset SR’ in LINK_CTL	R	0x00
8	Link Down – A ‘1’ indicates the link has gone down at some point since the last ‘Reset SR’. A ‘0’ indicates the link has not gone down since the last ‘Reset SR’. This bit is cleared through ‘Reset SR’ in LINK_CTL.	R	0
9	Link Up – This bit reflects the current status of the link. A ‘1’ indicates the link is currently up. A ‘0’ indicates the link is currently down. Note that this bit is not latched like the ‘Link Down’ bit.	R	0
10	Synchronization Error – A ‘1’ indicates the card has corrected a synchronization error on the incoming data stream. A ‘0’ indicates the card has not corrected a synchronization error on the incoming data stream. This bit is cleared through ‘Reset SR’ in LINK_CTL.	R	0
11	Checksum Error – A ‘1’ indicates the card has detected a checksum error on the incoming data stream. A ‘0’ indicates the card has not detected a checksum error on the incoming data stream. This bit is cleared through ‘Reset SR’ in LINK_CTL.	R	0
12	RX FIFO Overflow – A ‘1’ indicates the Receive FIFO has overflowed. A ‘0’ indicates the Receive FIFO has not overflowed. This bit is cleared through ‘Reset SR’ in LINK_CTL.	R	0
13	TX FIFO Overflow – A ‘1’ indicates the Transmit FIFO has overflowed. A ‘0’ indicates the Transmit FIFO has not overflowed. This bit is cleared through ‘Reset SR’ in LINK_CTL.	R	0
31 to 14	Reserved	None	0

B.4.6 FPDP Flags (FPDP_FLGS) – Offset 0x10

Field	Description	Access	Reset Value
0	Send SYNC – Write ‘1’ to send SYNC without DVALID. Writing ‘0’ has no effect.	W	0
1	PIO1 Out – State of the PIO1 line sent across the link.	R/W	0
2	PIO2 Out – State of the PIO2 line sent across the link.	R/W	0
3	DIR Out – State of the DIR line sent across the link.	R/W	0
4	NRDY Out – State of the NRDY line sent across the link.	R/W	0
7 to 5	Reserved.	None	0
8	SYNC Received – A ‘1’ indicates a SYNC without DVALID has been received. Cleared through ‘Clear SYNC’ in the LINK_CTL register. A ‘0’ indicates no SYNC has been received.	R	0
9	PIO1 In – State of the PIO1 line received from the link.	R	0
10	PIO2 In - State of the PIO2 line received from the link.	R	0
11	DIR In – State of the DIR line received from the link.	R	0
12	NRDY In – State of the NRDY line received from the link.	R	0
13	Rcvd STOP – Indicates that a STOP flow control primitive was received from the remote receiver. This bit is read only and will be dynamically changing.	R	0
14	Sent STOP – Indicates that a STOP flow control primitive was sent to the remote transmitter. This bit is read only and will be dynamically changing.	R	0
15	FIFO Overflow – Indicates that the Remote Transmitter FIFO Overflow bit was set in the received Status End of Frame primitive (EOFa or EOFn Fibre Channel ordered sets). This indicates that the remote node detected an overflow condition in its transmit FIFO. This bit is read only and will be dynamically changing.	R	0
16	Latched version of status bit 13. This bit is cleared by writing a ‘0’ to it. It should be noted that this bit might not appear to be cleared immediately after writing a ‘0’ to it. This is because another STOP may have been received immediately after clearing it.	R/W	0
17	Latched version of status bit 14. This bit is cleared by writing a ‘0’ to it. It should be noted that this bit might not appear to be cleared immediately after writing a ‘0’ to it. This is because another STOP may have been sent immediately after clearing it.	R/W	0
18	Latched version of status bit 15. This bit is cleared by writing a ‘0’ to it. It should be noted that this bit might not appear to be cleared immediately after writing a ‘0’ to it. This is because another FIFO Overflow may have been received immediately after clearing it.	R/W	0
31 to 19	Reserved.	None	0

B.4.7 Receive FIFO Threshold – Offset 0x14

Field	Description	Access	Reset Value
19 to 0	Number of 32-bit words in the Receive FIFO.	R	0
20	Rearm Threshold Interrupt – Write ‘1’ to rearm the threshold register. Writing ‘0’ has no effect.	W	0
21	Data present – A ‘1’ indicates data is present on the output. A ‘0’ indicates no data is present.	R	0
29 to 22	Reserved.	None	0
31 to 30	Interrupt Threshold – Selects one of the following levels of the Receive FIFO to interrupt on: 00 – Interrupt threshold set to Receive FIFO Not Empty 01 – Interrupt threshold set to Receive FIFO ¼ Full 10 – Interrupt threshold set to Receive FIFO ½ Full 11 – Interrupt threshold set to Receive FIFO ¾ Full	R/W	0

B.4.8 Laser Transmitter Control – Offset 0x18

Field	Description	Access	Reset Value
25 to 0	Reserved.	None	0
26	Manual laser shutdown – Set to ‘1’ to shutdown the laser. Set to ‘0’ for normal operation.	R/W	0
31 to 27	Reserved.	None	0

B.4.9 Transaction Channel 0 (Send Channel)

Send Queue Address (QADDR0) – Offset 0x20

Field	Description	Access	Reset Value
3 to 0	Reserved – Write as '0'	None	0
31 to 4	Bits 31 through 4 of PCI address for the transaction queue.	R/W	0

Send Queue Control (QCTL0) – Offset 0x28

Field	Description	Access	Reset Value
4 to 0	Producer Index for transaction queue. Maximum 32.	R/W	0
7 to 5	Reserved.	None	0
12 to 8	Consumer Index for transaction queue. Maximum 32.	R	0
15 to 13	Reserved.	None	0
20 to 16	Queue length – Place number of entries minus one here, where number of entries is a power of 2. Maximum 32.	R/W	0
23 to 21	Reserved.	None	0
24	Enable Queue – A '1' enables the queue to fetch transaction entries. Setting this bit to '0' pauses the transaction queue.	R/W	0
25	Reset Queue – Write '1' to set the consumer and producer indices to 0 – Writing '0' has no effect.	W	0
26	Abort Queue – Write '1' to this bit to abort the current transaction pending on the transaction controller. Writing '0' has no effect.	W	0
27	Reserved.	None	0
28	Stop on link error – Set to '1' to disable the controller on link errors. Set to '0' for normal operation.	R/W	0
29	Queue paused – A '1' indicates the queue is paused, '0' otherwise.	R	0
30	Entries Available – A '1' indicates there are entries in the queue to process. A '0' indicates there are no entries.	R	0
31	Preserve – When the register is written with this bit set, only the producer index is written.	W	0

Send Transaction CSR (TNS_CSR0) – Offset 0x30

Field	Description	Access	Reset Value
0	Interrupt Enable – Set to '1' to enable an interrupt on this transaction. Set to '0' for normal operation.	R/W	0
1	Skip entry – skips to the next entry when this bit is set. Set to '1' to enable. Set to '0' for normal operation.	R/W	0
2	/SYNC status – status of the /SYNC line to the controller.	R	0
3	Link error status – status of the link error line to the controller. '1' = error, '0' = no error.	R	0
4	Reserved.	None	0
5	Abort & Writeback on Link Error – Set to '1' to abort the current transaction and write the status back to the transaction entry in memory on Link Error. Set to '0' not to abort.	R/W	0
7 to 6	Reserved.	None	0
8	Send a /SYNC without DVALID after this transaction is finished. Set to '1' to send, set to '0' not to send. Do not set both bits 8 and 9.	R/W	0
9	Send a /SYNC with DVALID after this transaction is finished. Set to '1' to send, set to '0' not to send. Do not set both bits 8 and 9.	R/W	0
31 to 10	Reserved.	None	0

Send Transaction Length (TLENGTH0) – Offset 0x34

Field	Description	Access	Reset Value
31 to 0	Transaction length in 32-bit words.	R/W	0

Send Chain PCI Address (CPCIADDR0) – Offset 0x40

Field	Description	Access	Reset Value
3 to 0	Reserved (Lower four bits of PCI address must be zero).	None	0
31 to 4	PCI address for the buffer to transmit.	R/W	0

Send Chain Length/Flags (CLENFLGS0) – Offset 0x48

Field	Description	Access	Reset Value
23 to 0	Length of buffer in 32-bit words.	R/W	0
24	End Chain – Write '1' to say this is the last chain entry. Write '0' if it is not.	R/W	0
25	Reserved.	None	0
27 to 26	Data Swapping – "00" for straight, "01" to swap bytes, "10" to swap 32-bit words, "11" to swap 32-bit words and bytes.	R/W	0
28	Reserved.	None	0
29	Interrupt – Write '1' to interrupt on transfer complete, Write '0' otherwise.	R/W	0
30	Go – Set to '1' to start this transaction, '0' to stop it. If it is a chained transaction, the first action is to fetch the chain entry.	R/W	0
31	Done – A '1' indicates this channel is currently idle. A '0' indicates a DMA is in progress.	R	0

Send Next Chain Entry (CNEXT0) – Offset 0x4C

Field	Description	Access	Reset Value
3 to 0	Reserved (Lower four bits of PCI address must be zero).	None	0
31 to 4	PCI address for the next chain entry.	R/W	0

B.4.10 Transaction Channel 1 (Receive Channel)

Receive Queue Address (QADDR1) – Offset 0x50

Field	Description	Access	Reset Value
3 to 0	Reserved – Write as '0'	None	00
31 to 4	Bits 31 through 4 of PCI address for the transaction queue.	R/W	00

Receive Queue Control (QCTL1) – Offset 0x58

Field	Description	Access	Reset Value
4 to 0	Producer Index for transaction queue. Maximum 32.	R/W	0
7 to 5	Reserved.	None	0
12 to 8	Consumer Index for transaction queue. Maximum 32.	R	0
15 to 13	Reserved.	None	0
20 to 16	Queue length – Place number of entries minus one here, where number of entries is a power of 2. Maximum 32.	R/W	0
23 to 21	Reserved.	None	0
24	Enable Queue – A '1' enables the queue to fetch transaction entries. Setting this bit to '0' pauses the transaction queue.	R/W	0
25	Reset Queue – Write '1' to set the consumer and producer indices to 0 – Writing '0' has no effect.	W	0
26	Abort Queue – Write '1' to this bit to abort the current transaction pending on the transaction controller. Writing '0' has no effect.	W	0
27	Stop on /SYNC – Set to '1' to disable the controller on /SYNC received. Set to '0' for normal operation.	R/W	0
28	Stop on link error – Set to '1' to disable the controller on link errors. Set to '0' for normal operation.	R/W	0
29	Queue paused – A '1' indicates the queue is paused, '0' otherwise.	R	0
30	Entries Available – A '1' indicates there are entries in the queue to process. A '0' indicates there are no entries.	R	0
31	Preserve – When the register is written with this bit set, only the producer index is written.	W	0

Receive Transaction CSR (TNS_CSR1) – Offset 0x60

Field	Description	Access	Reset Value
0	Interrupt Enable – Set to ‘1’ to enable an interrupt on this transaction. Set to ‘0’ for normal operation.	R/W	0
1	Skip entry – Skips to the next entry when this bit is set. Set to ‘1’ to enable. Set to ‘0’ for normal operation.	R/W	0
2	/SYNC status – status of the /SYNC line to the controller.	R	0
3	Link error status – status of the link error line to the controller. ‘1’ = error, ‘0’ = no error.	R	0
4	Abort & Writeback on /SYNC – Set to ‘1’ to abort the current transaction and write the status back to the transaction entry in memory on /SYNC. Set to ‘0’ not to abort.	R/W	0
5	Abort & Writeback on Link Error – Set to ‘1’ to abort the current transaction and write the status back to the transaction entry in memory on Link Error. Set to ‘0’ not to abort.	R/W	0
9 to 6	Reserved.	None	0
10	Received SYNC without DVALID.	R	0
11	Received SYNC with DVALID. Convert SYNC must be enabled in the Link Control register for this bit to be valid.	R	0
31 to 12	Reserved.	None	0

Receive Transaction Length (TLENGTH1) – Offset 0x64

Field	Description	Access	Reset Value
31 to 0	Transaction length in 32-bit words.	R/W	0

Receive Chain PCI Address (CPCIADDR1) – Offset 0x70

Field	Description	Access	Reset Value
3 to 0	Reserved (Lower four bits of PCI address must be zero).	None	0
31 to 4	PCI address for the buffer to receive.	R/W	0

Receive Chain Length/Flags (CLENFLGS1) – Offset 0x78

Field	Description	Access	Reset Value
23 to 0	Length of buffer in 32-bit words.	R/W	0
24	End Chain – Write ‘1’ to say this is the last chain entry. Write ‘0’ if it is not.	R/W	0
25	Reserved.	None	0
27 to 26	Data Swapping – “00” for straight, “01” to swap bytes, “10” to swap 32-bit words, “11” to swap 32-bit words and bytes.	R/W	0
28	Reserved.	None	0
29	Interrupt – Write ‘1’ to interrupt on transfer complete, Write ‘0’ otherwise.	R/W	0
30	Go – A ‘1’ starts this transaction, A ‘0’ stops it. If it is a chained transaction, the first action is to fetch the chain entry.	R/W	0
31	Done – A ‘1’ indicates this channel is currently idle. A ‘0’ indicates a DMA is in progress.	R	0

Receive Next Chain Entry (CNEXT1) – Offset 0x7C

Field	**Description**	**Access**	**Reset Value**
3 to 0	Reserved (Lower four bits of PCI address must be zero).	None	0
31 to 4	PCI address for the next chain entry.	R/W	0

APPENDIX C

SL100/SL240 PROTOCOL

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FIGURES

TABLES

C.1 Overview

NOTE: The FibreXtreme SL100 and SL240 PCI, PMC, and CPCI Cards will be referred to throughout this appendix as PCI. Anything that is exclusive to the PCI, PMC, or CPCI Cards will be described as such.

The SL100/SL240 Serial FPDP protocol (also known as VITA 17.1) is designed to provide near optimal throughput while maintaining low overhead. The link transfer rate for SL100 cards is 1.0625 Gbps, and the transfer rate for SL240 cards is 2.5 Gbps. Since an 8B/10B encoding scheme is used, this corresponds to a raw data rate of 106.25 MB/s (1 MB = 10^6 bytes) for SL100 and 250 MB/s for SL240. Based on the protocol presented here, the usable throughput of this link available to the user is 105 MB/s for SL100 or 247 MB/s for SL240. All ordered sets used by this protocol are standard Fibre Channel ordered sets with the exception of positive IDLE, which is allowed for a more flexible receiver interface.

NOTE: The protocol referred to throughout this document is the protocol used by the transmitter and accepted by the receiver. The receiver does not have to see the protocol defined here to receive data. Any generic Fibre Channel data stream with an IDLE at least every 4096 words can be used.

C.2 Ordered Sets Used

Fibre Channel denotes a certain mapping of the transmission words in the 8B/10B protocol to be ordered sets, which denote special control information for Fibre Channel. These same ordered sets are used in VITA 17.1, but are assigned different meaning.

There are eighteen ordered sets used by SL240 to denote different information. Twelve of these ordered sets are used to embed five bits of data—eight start-of-frame (SOF) sets are used to embed three bits at the start of a frame, and four status-end-of-frame (SEOF) sets are used to embed two bits at the end of the frame. The SOF ordered sets embed three FPDP signals - PIO1, PIO2, and DIR.

Note that although the direction signal on FPDP is active low (/DIR), the signal transmitted on the link is active high (DIR).

The four EOF ordered sets embed the FPDP signal NRDY (once again, the inverted version of the FPDP interface’s /NRDY) and Transmit FIFO Overflow flag.

There are two additional EOF ordered sets used by SL240 to denote the actual end of frame. The Mark EOF (MEOF) denotes a frame that has SYNC associated with it, and the Frame EOF (FEOF) denotes a normal data frame. The other four ordered sets are inter-frame padding used to denote flow control information and alternate frame interpretations. Table C-1 shows the mappings from the Fibre Channel ordered sets onto the VITA 17.1 ordered sets, along with the meaning associated with each ordered set.

Table C-1 Ordered Set Mapping

Fibre Channel Ordered Set	VITA 17.1 Ordered Set	Description
SOFc1	SOF	Start of Frame: PIO1 = 0, PIO2 = 0, DIR = 0
SOFi1	SOF	Start of Frame: PIO1 = 0, PIO2 = 0, DIR = 1
SOFn1	SOF	Start of Frame: PIO1 = 0, PIO2 = 1, DIR = 0
SOFi2	SOF	Start of Frame: PIO1 = 0, PIO2 = 1, DIR = 1
SOFn2	SOF	Start of Frame: PIO1 = 1, PIO2 = 0, DIR = 0
SOFi3	SOF	Start of Frame: PIO1 = 1, PIO2 = 0, DIR = 1
SOFn3	SOF	Start of Frame: PIO1 = 1, PIO2 = 1, DIR = 0
SOFf	SOF	Start of Frame: PIO1 = 1, PIO2 = 1, DIR = 1
EOFt	SEOF	Status EOF: FIFO Overflow = 0, NRDY = 0
EOFdt	SEOF	Status EOF: FIFO Overflow = 0, NRDY = 1
EOFa	SEOF	Status EOF: FIFO Overflow = 1, NRDY = 0
EOFn	SEOF	Status EOF: FIFO Overflow = 1, NRDY = 1
EOFni	MEOF	Mark EOF: EOF for a SYNC frame
EOFdti	FEOF	Frame EOF: EOF for a normal data frame
R_RDY	SWDV	SYNC with DATA Valid: Says that the next frame will be a SYNC with DATA frame
NOS	STOP	Tells the remote transmitter to stop sending data
CLS	GO	Tells the remote transmitter it can continue to send data
IDLE	IDLE	IDLE character: Used as a padding word to maintain receiver synchronization

C.3 Frames

There are four basic frame types defined in VITA 17.1 – an IDLE frame, data frame, a SYNC without data frame, and a SYNC with data frame. The data is divided into frames so the FPDP signals are sampled at some minimum interval, and so the receiver is guaranteed to see IDLEs to maintain synchronization. SYNC is used to delimit data streams and maintain host program synchronization. This signal is under user control for PCI-based products, and is the same as the FPDP /SYNC signal for CMC/FPDP based products. Whenever a SYNC appears on the output of the Transmit FIFO, the current frame is terminated and the proper SYNC frame (SYNC with data or SYNC without data) is sent. Figure C-1 shows the four types of frames and the ordered set placement within those frames.

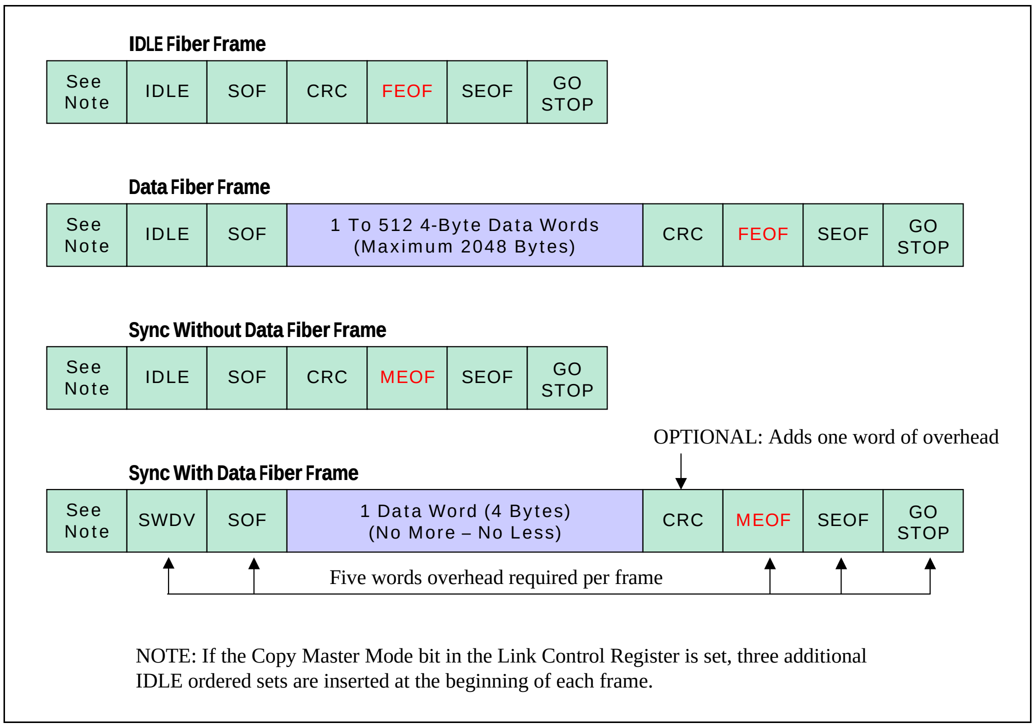

Figure C-1 VITA 17.1 Framing Protocol

C.3.1 Link Bandwidth

With CRC disabled and the Copy Mode Master bit clear ('0'), there is a five-word overhead for every frame transmitted. Since frames can contain up to 512 words of data, this results in an efficiency of 99.03%. With CRC enabled and the Copy Master bit clear, there is a six-word overhead for every frame transmitted. This results in a maximum efficiency of 98.84%. With the Copy Mode Master bit set ('1'), three additional ordered sets are added per frame. This results in an efficiency of 98.46 percent without CRC and 98.27 percent with CRC. Table C-2 gives the theoretical maximum sustained throughput based on these numbers.

Table C-2 Maximum Sustained Throughput

Card	With CRC and Copy Mode Master bit = 0	Without CRC and Copy Mode Master bit = 0	With CRC and Copy Mode Master bit = 1	Without CRC and Copy Mode Master bit = 1
SL100	105.02 MB/s	105.22 MB/s	104.41 MB/s	104.61 MB/s
SL240	247.10 MB/s	247.58 MB/s	245.68 MB/s	246.15 MB/s

NOTE: The Copy Master Mode is located in the Link Control register.

C.3.2 FPDP Signal Sample Rate

The states of the FPDP signals (PIO1, PIO2, DIR, and NRDY) are transmitted across the link at varying rates. The worst-case rate at which these signals are sampled is for CRC checked filled data frames and the Copy Mode Master bit set . In this case, the signals are sampled every 521 words. For CRC checked filled data frames and the Copy Mode Master bit clear, these signals are sampled every 518 words. Table C-3 summarizes the worst-case sampling frequencies for the different link transmission speeds (SL100 and SL240).

Table C-3 Sampling Frequencies

Card	With CRC and Copy Mode Master bit = 0	Without CRC and Copy Mode Master bit = 0	With CRC and Copy Mode Master bit = 1	Without CRC and Copy Mode Master bit = 1
SL100	51.28 KHz	51.38 KHz	50.98 KHz	51.08 KHz
SL240	120.65 KHz	120.89 KHz	119.96 KHz	120.19 KHz

NOTE: The Copy Master Mode is located in the Link Control register.

C.4 Data Transmission and Flow Control

As SL100/SL240 is seen as a point-to-point link from the transmitter, there is no need to log into the receiver node to begin sending data. SL100/SL240 boards can begin transmission as soon as they are started and data is available in the Transmit FIFO. Using the frames described above, the transmitter sets up a constant stream of frames, into which it inserts data as it becomes available. Data is only inserted if the flow control signal from the remote end is GO—if it is STOP, then the data waits in the Transmit FIFO until the signal changes. Curtiss-Wright Controls' SL100/SL240 boards use the same protocol when transmitting from either end to allow the link to operate bi-directionally. Since these data streams are independent, the maximum throughput on the link would be 210 MB/s (105 MB/s/direction) for SL100 or 494 MB/s for SL240.

The receiver should transmit the STOP signal when it has space for the data contained in 20 km of fiber or less left. Assuming 5 µs/km for the speed of light, this gives us 100 µs of data. For SL100, each 32-bit word (40 bits on the link) takes 37.64 ns, there are 2657 words stored in 20 km of cable. For SL240, each 32-bit word (40 bits on the link) takes 16 ns, so there are 6250 words stored in 20 km of cable. The first 10 km is reserved for sending the STOP signal to the transmitter, and the second 10 km is for the data already contained in the receive fiber.

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APPENDIX D

ORDERING INFORMATION

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TABLES

D.1 Overview

This appendix contains the order number for all Curtiss-Wright Controls, Inc. products mentioned in this manual. For an up to date list, or for inquiries about these products, contact Curtiss-Wright Controls, Inc. Embedded Computing Data Communications Center Sales.

D.2 Ordering Information

D.2.1 33 MHz SL100 PMC Ordering Information

Table D-1 33 MHz SL100 PMC

Order Number	Description
FHG4-PM4MWB04-00	SL100 PMC, 850 nm laser, 5 V PCI signaling voltage
FHG4-PM4SWB04-00	SL100 PMC, 1300 nm laser, 5 V PCI signaling voltage
FHG5-PM4MWB04-00	SL100 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHG5-PM4SWB04-00	SL100 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHG4-PM4HSB04-00	SL100 PMC, HSSDC, 5 V PCI signaling voltage
FHG5-PM4HSB04-00	SL100 PMC, HSSDC, 3.3 V PCI signaling voltage
FHG4-PM4MWB04-R1	Ruggedized SL100 PMC, 850 nm laser, 5 V PCI signaling voltage
FHG5-PM4MWB04-R1	Ruggedized SL100 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHG4-PM4HSB04-R1	Ruggedized SL100 PMC, HSSDC, 5 V PCI signaling voltage
FHG5-PM4HSB04-R1	Ruggedized SL100 PMC, HSSDC, 3.3 V PCI signaling voltage

D.2.2 33 MHz SL100 PCI Ordering Information

Table D-2 33 MHz SL100 PCI

Order Number	Description
FHG4-PC4MWB04-00	SL100 PCI, 850 nm laser, 5 V PCI signaling voltage
FHG4-PC4SWB04-00	SL100 PCI, 1300 nm laser, 5 V PCI signaling voltage
FHG5-PC4MWB04-00	SL100 PCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG5-PC4SWB04-00	SL100 PCI, 1300 nm laser, 3.3 V PCI signaling voltage
FHG4-PC4HSB04-00	SL100 PCI, HSSDC, 5 V PCI signaling voltage
FHG5-PC4HSB04-00	SL100 PCI, HSSDC, 3.3 V PCI signaling voltage

D.2.3 66 MHz SL100 PMC Ordering Information

Table D-3 66 MHz SL100 PMC

Order Number	Description
FHE5-PM4MWB04-00	SL100 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHE5-PM4SWB04-00	SL100 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHE5-PM4MWB04-R1	Rugged Level 1 SL100 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHE5-PM4SWB04-R1	Rugged Level 1 SL100 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHE5-PM4MWB04-R2	Rugged Level 2 SL100 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHE5-PM4SWB04-R2	Rugged Level 2 SL100 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHE5-PM4H2B04-00	SL100 PMC, HSSDC2 laser SFP pluggable, 3.3V PCI signaling voltage

D.2.4 66 MHz SL100 PCI Ordering Information

Table D-4 66 MHz SL100 PCI

Order Number	Description
FHE5-PC4MWB04-00	SL100 PCI, 850 nm SFP laser, 3.3 V PCI signaling voltage
FHE5-PC4SWB04-00	SL100 PCI, 1300 nm SFP laser, 3.3 V PCI signaling voltage
FHE5-PC4LRB04-00	SL100 PCI, 1550 nm SFP laser, 3.3 V PCI signaling voltage
FHE5-PC4H2B04-00	SL100 PCI, SFP HSSDC2, 3.3 V PCI signaling voltage

D.2.5 33 MHz SL100 CPCI Ordering Information

Table D-5 33 MHz SL100 CPCI

Order Number	Description
FHG4-CP4MWB04-00	SL100 CPCI, 850 nm laser, 5 V PCI signaling voltage
FHG4-CP4SWB04-00	SL100 CPCI, 1300 nm laser, 5 V PCI signaling voltage
FHG5-CP4MWB04-00	SL100 CPCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG5-CP4SWB04-00	SL100 CPCI, 1300 nm laser, 3.3 V PCI signaling voltage

D.2.6 SL100 FPDP Ordering Information

Table D-6 SL100 FPDP

Order Number	Description
FHG4-FP4MWB04-00	NGSL VME with one FPDP port, SL100 CMC, 850 nm laser
FHG4-FP4SWB04-00	NGSL VME with one FPDP port, SL100 CMC, 1300 nm laser
FHG4-FC4MWB04-00	PCI Carrier with one FPDP port, SL100 CMC, 850 nm laser
FHG4-FC4SWB04-00	PCI Carrier with one FPDP port, SL100 CMC, 1300 nm laser
FHG4-FC4HSB04-00	PCI Carrier with one FPDP port, SL100 CMC, HSSDC
FHG4-FM4MWB04-00	SL100 CMC, 850 nm laser
FHG4-FM4SWB04-00	SL100 CMC, 1300 nm laser
FHG4-FM4HSB04-00	SL100 CMC, HSSDC
FHG4-FM4MWB04-R1	Ruggedized SL100 CMC, 850 nm laser
FHG2-FR4MWB04-00	Modified Single FXSL VME with two FPDP ports, SL100 CMC, 850 nm laser
FHG2-FR4SWB04-R1	Ruggedized Modified Single FXSL VME with two FPDP ports, SL100 CMC, 850 nm laser
FHG2-FR4SWB04-00	Modified Single FXSL VME with two FPDP ports, SL100 CMC, 1300 nm laser
FHG4-FSMWBMWB-00	Dual FXSL VME with two SL100 CMC cards, one FPDP port per CMC card, 850 nm laser
FHG4-FSSWBSWB-00	Dual FXSL VME with two SL100 CMC cards, one FPDP port per CMC card, 1300 nm laser

D.2.7 33 MHz SL240 PMC Ordering Information

Table D-7 33 MHz SL240 PMC

Order Number	Description
FHG6-PM6MWB04-00	SL240 PMC, 850 nm laser, 5 V PCI signaling voltage
FHG6-PM6SWB04-00	SL240 PMC, 1300 nm laser, 5 V PCI signaling voltage
FHG7-PM6MWB04-00	SL240 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHG7-PM6SWB04-00	SL240 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHG6-PM6MWB04-R1	Ruggedized SL240 PMC, 850 nm laser, 5 V PCI signaling voltage
FHG7-PM6MWB04-R1	Ruggedized SL240 PMC, 850 nm laser, 3.3 V PCI signaling voltage

D.2.8 33 MHz SL240 PCI Ordering Information

Table D-8 33 MHz SL240 PCI

Order Number	Description
FHG6-PC6MWB04-00	SL240 PCI, 850 nm laser, 5 V PCI signaling voltage
FHG6-PC6SWB04-00	SL240 PCI, 1300 nm laser, 5 V PCI signaling voltage
FHG7-PC6MWB04-00	SL240 PCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG7-PC6SWB04-00	SL240 PCI, 1300 nm laser, 3.3 V PCI signaling voltage

D.2.9 66 MHz SL240 PMC Ordering Information

Table D-9 66 MHz SL240 PMC

Order Number	Description
FHE7-PM6MWB04-00	SL240 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHE7-PM6SWB04-00	SL240 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHE7-PM6MWB04-R1	Rugged Level 1 SL240 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHE7-PM6SWB04-R1	Rugged Level 1 SL240 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHE7-PM6MWB04-R2	Rugged Level 2 SL240 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHE7-PM6SWB04-R2	Rugged Level 2 SL240 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHE7-PM6H2B04-00	SL240 PMC, HSSDC2 laser SFP pluggable, 3.3V PCI signaling voltage

D.2.10 66 MHz SL240 PCI Ordering Information

Table D-10 66 MHz SL240 PCI

Order Number	Description
FHE7-PC6MWB04-00	SL240 PCI, 850 nm SFP laser, 3.3 V PCI signaling voltage
FHE7-PC6SWB04-00	SL240 PCI, 1300 nm SFP laser, 3.3 V PCI signaling voltage
FHE7-PC6LRB04-00	SL240 PCI, 1550 nm SFP laser, 3.3 V PCI signaling voltage
FHE7-PC6H2B04-00	SL240 PCI, SFP HSSDC2, 3.3 V PCI signaling voltage

D.2.11 SL240 CPCI Ordering Information

Table D-11 SL240 CPCI

Order Number	Description
FHG6-CP6MWB04-00	SL240 CPCI, 850 nm laser, 5 V PCI signaling voltage
FHG6-CP6SWB04-00	SL240 CPCI, 1300 nm laser, 5 V PCI signaling voltage
FHG7-CP6MWB04-00	SL240 CPCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG7-CP6SWB04-00	SL240 CPCI, 1300 nm laser, 3.3 V PCI signaling voltage

D.2.12 SL240 FPDP Ordering Information

Table D-12 SL240 FPDP

Order Number	Description
FHG6-FP6MWB04-00	NGSL VME with one FPDP port, SL240 CMC, 850 nm laser
FHG6-FP6SWB04-00	NGSL VME with one FPDP port, SL240 CMC, 1300 nm laser
FHG6-FC6MWB04-00	PCI Carrier with one FPDP port, SL240 CMC, 850 nm laser
FHG6-FC6SWB04-00	PCI Carrier with one FPDP port, SL240 CMC, 1300 nm laser
FHG6-FM6MWB04-00	SL240 CMC, 850 nm laser
FHG6-FM6SWB04-00	SL240 CMC, 1300 nm laser
FHG6-FSMWBMWB-00	Dual FXSL VME with two SL240 CMC cards, one FPDP port per CMC card, 850 nm laser
FHG6-FSSWBSWB-00	Dual FXSL VME with two SL240 CMC cards, one FPDP port per CMC card, 1300 nm laser
FHG2-FP6MWB04-00	Single FXSL VME Carrier with two FPDP ports, SL240 CMC card, 850 nm laser
FHG2-FP6SWB04-00	Single FXSL VME Carrier with two FPDP ports, SL240 CMC card, 1300 nm laser

D.2.13 Carrier Card (without CMC) Ordering Information

Table D-13 Carrier Card (without CMC)

Order Number	Description
FHG4-FP000000-00	NGSL VME Carrier with one FPDP port (w/o CMC card)
FHG4-FC000000-00	PCI Carrier (w/o CMC card)
FHG2-FP000000-00	Single FXSL Carrier with two FPDP Ports (w/o CMC card)
FHG2-FR000000-00	Modified Single FXSL Carrier with two FPDP Ports (w/o CMC card)

D.2.14 Short Wavelength: Multimode Fiber-Optic Cables

The following table lists the order numbers for the simplex and duplex, 50/125 μm multimode fiber-optic cables, for use with the short wavelength laser media interface.

Table D-14 LC to LC

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-M1LC3000-00	FHAC-M2LC3000-00	3 meters	LC	LC
FHAC-M1LC5000-00	FHAC-M2LC5000-00	5 meters	LC	LC
FHAC-M1LC1001-00	FHAC-M2LC1001-00	10 meters	LC	LC
FHAC-M1LC2001-00	FHAC-M2LC2001-00	20 meters	LC	LC
FHAC-M1LC3001-00	FHAC-M2LC3001-00	30 meters	LC	LC
FHAC-M1LCxxxx-00	FHAC-M2LCxxxx-00	Custom	LC	LC

Table D-15 LC to ST

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-M1LCST03-00	FHAC-M2LCST03-00	3 meters	LC	ST
FHAC-M1LCST05-00	FHAC-M2LCST05-00	5 meters	LC	ST
FHAC-M1LCST10-00	FHAC-M2LCST10-00	10 meters	LC	ST
FHAC-M1LCST20-00	FHAC-M2LCST20-00	20 meters	LC	ST
FHAC-M1LCST30-00	FHAC-M2LCST30-00	30 meters	LC	ST
FHAC-M1LCSTxx-00	FHAC-M2LCSTxx-00	Custom	LC	ST

Table D-16 SC to LC

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-M1SCLC01-00	FHAC-M2SCLC01-00	1 meter	SC	LC
FHAC-M1SCLC03-00	FHAC-M2SCLC03-00	3 meters	SC	LC
FHAC-M1SCLC05-00	FHAC-M2SCLC05-00	5 meters	SC	LC
FHAC-M1SCLC10-00	FHAC-M2SCLC10-00	10 meters	SC	LC
FHAC-M1SCLC20-00	FHAC-M2SCLC20-00	20 meters	SC	LC
FHAC-M1SCLC30-00	FHAC-M2SCLC30-00	30 meters	SC	LC
FHAC-M1SCLCxx-00	FHAC-M2SCLCxx-00	Custom	SC	LC

D.2.15 Long Wavelength: Single-mode Fiber-Optic Cables

The following table lists the order numbers for the simplex and duplex, 9/125 µm single-mode fiber-optic cables, for use with the long wavelength laser media interface.

Table D-17 LC to LC

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-S1LC3000-00	FHAC-S2LC3000-00	3 meters	LC	LC
FHAC-S1LC5000-00	FHAC-S2LC5000-00	5 meters	LC	LC
FHAC-S1LC1001-00	FHAC-S2LC1001-00	10 meters	LC	LC
FHAC-S1LC2001-00	FHAC-S2LC2001-00	20 meters	LC	LC
FHAC-S1LC3001-00	FHAC-S2LC3001-00	30 meters	LC	LC
FHAC-S1LCxxxx-00	FHAC-S2LCxxxx-00	Custom	LC	LC

Table D-18 SC to LC

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-S1SCLC01-00	FHAC-S2SCLC01-00	1 meter	SC	LC
FHAC-S1SCLC03-00	FHAC-S2SCLC03-00	3 meters	SC	LC
FHAC-S1SCLC05-00	FHAC-S2SCLC05-00	5 meters	SC	LC
FHAC-S1SCLC10-00	FHAC-S2SCLC10-00	10 meters	SC	LC
FHAC-S1SCLC20-00	FHAC-S2SCLC20-00	20 meters	SC	LC
FHAC-S1SCLC30-00	FHAC-S2SCLC30-00	30 meters	SC	LC
FHAC-S1SCLCxx-00	FHAC-S2SCLCxx-00	Custom	SC	LC

D.2.16 HSSDC Copper Media Interface: 1.0625 Gbps

Duplex, 150-Ohm shielded quad cable with HSSDC connectors, for use with the HSSDC copper media interface.

Table D-19 Duplex, Shielded Quad Cable with HSSDC Connectors

Order Number	Description
FHAC-Q2HS1000-00	1 m duplex cable, equalized
FHAC-Q2HS3000-00	3 m duplex cable, equalized
FHAC-Q2HS5000-00	5 m duplex cable, equalized
FHAC-Q2HS1001-00	10 m duplex cable, equalized
FHAC-Q2HS2001-00	20 m duplex cable, equalized
FHAC-Q2HS2501-00	25 m duplex cable, equalized
FHAC-Q2HS3001-00	30 m duplex cable, equalized
FHAC-Q2H95000-00	5 m duplex cable, HSSDC to 9-pin D-sub

D.2.17 HSSDC2 Copper Media Interface: 1.0625 Gbps

Shielded 150-Ohm Shielded Quad copper cable with HSSDC2 (Fibre Channel) connectors, for use with the HSSDC2 copper media interface.

Table D-20 Shielded 150-Ohm Quad Copper Cable with HSSDC2 (Fibre Channel) Connectors

Order Number	Description
FHAC-Q2H11000-00	1 m HSSDC2 cable, equalized
FHAC-Q2H13000-00	3 m HSSDC2 cable, equalized
FHAC-Q2H15000-00	5 m HSSDC2 cable, equalized
FHAC-Q2H11001-00	10 m HSSDC2 cable, equalized
FHAC-Q2H12001-00	20 m HSSDC2 cable, equalized
FHAC-Q2H12501-00	25 m HSSDC2 cable, equalized
FHAC-Q2H13001-00	30 m HSSDC2 cable, equalized

D.2.18 HSSDC2 Copper Media Interface: 2.5 Gbps

Shielded 100-Ohm Shielded Quad copper cable with HSSDC2 (InfiniBand) connectors, for use with the HSSDC2 copper media interface.

Table D-21 Shielded 100-Ohm Quad Copper Cable with HSSDC2 (InfiniBand) Connectors

Order Number	Description
FHAC-Q2H31000-00	1 m HSSDC2 cable, equalized
FHAC-Q2H33000-00	3 m HSSDC2 cable, equalized
FHAC-Q2H35000-00	5 m HSSDC2 cable, equalized
FHAC-Q2H31001-00	10 m HSSDC2 cable, equalized

APPENDIX E

FPDP PRIMER

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FIGURES

TABLES

E.1 FPDP Overview

This section provides a brief discussion of Front Panel Data Port (FPDP). For more information about FPDP, refer to *Front Panel Data Port Specifications, ANSI/VITA 17-1998* or go to the VITA website at: **www.vita.com/vso/**. The SL100/SL240 cards implement a serial version of FPDP on their link interface, which is standard VITA 17.1. Most of the concepts from the parallel FPDP specification are applicable to the Serial FPDP world, so they are described here.

Many real-time systems require high-speed, low-latency data transfers on a sustained basis. However, the primary bus (for example, VME bus) cannot provide the required bandwidth and latency at all times because of bus contention. The primary bus must also handle other tasks such as system control. The FPDP bus provides a solution to this problem. Using FPDP, two or more cards are connected by a simple, parallel, synchronous interface using 80-conductor ribbon cable running across the cards' front panels or through a 1.0625 Gbps or 2.5 Gbps serial interface. For parallel FPDP, devices on the FPDP bus must consist of one FPDP Transmit Master (FPDP-TM) and one FPDP Receive Master (FPDP-RM). Multiple FPDP Receiver (FPDP-R) devices may also exist on the bus. For Serial FPDP, there is one master for the bus (which acts as FPDP-TM and FPDP-RM), and one or more receiver nodes. Since only one FPDP-TM can exist on the bus, no bus contention between devices is possible. Figure E-1 shows an example VME FPDP card interconnection using parallel FPDP.

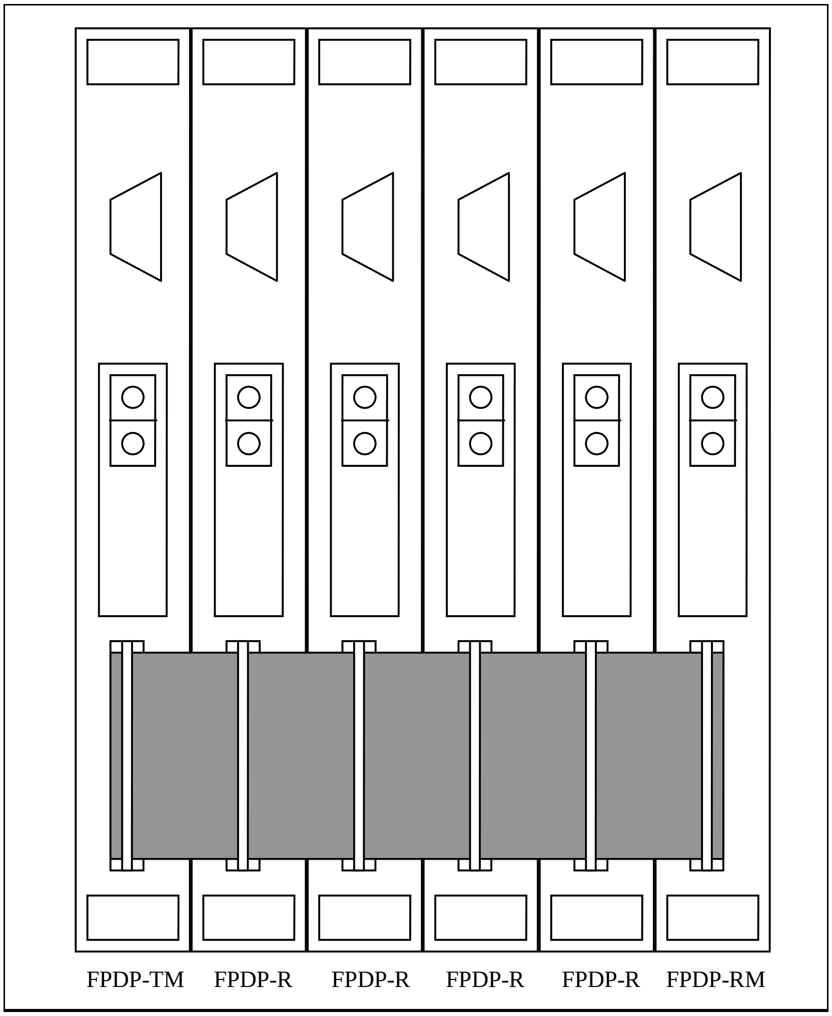

Figure E-1 Example Configuration With Multiple VME FPDP Cards Connected

Several advantages of an FPDP interface include:

- Simple hardware is required to interface to FPDP.
- FPDP does not interfere with the normal bus operations—VME or PCI traffic can continue without data transfers wasting bus bandwidth.
- No bus contention is possible because there is only one transmitter.
- No special backplane is required.
- FPDP allows connections from VME chassis to VME chassis.
- Systems may have multiple FPDP buses and thus provides scaleable bandwidth.
- Multiple FPDP busses may coexist in one chassis.
- Throughput can be accurately computed in the design stage.
- Little software development is required to move data between cards.
- Framed or unframed data may be transmitted across the FPDP link.
- Low latency.

Some additional advantages of parallel FPDP are:

- Low cost, 32-bit parallel interface provided through a ribbon cable.
- 160 MBps sustained data rate.

Some additional advantages of Serial FPDP are:

- Noise immune fiber-optic interface.
- Significantly increased transmission distance (10 km).
- Standard cards for parallel FPDP, custom backplanes, PCI (PCI/CPCI/PMC), and others available.

E.2 Terminology

Some FPDP specific terms are defined below.

FPDP TRANSMIT MASTER (FPDP-TM)

An FPDP-TM is a device that transmits data and timing signals onto the FPDP bus. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-TM may exist on an FPDP bus.

FPDP RECEIVE MASTER (FPDP-RM)

An FPDP-RM is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-RM may exist on an FPDP bus.

FPDP RECEIVER (FPDP-R)

An FPDP-R is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. As opposed to the FPDP-RM, this device does not terminate any bus signals on parallel FPDP. Multiple FPDP-R devices may exist on an FPDP bus.

E.3 Parallel FPDP Theory of Operation

E.3.1 Clock Signals

A single FPDP-TM generates a free-running clock. This clock frequency determines the maximum transfer rate on the bus. FPDP provides both a PECL (Positive Emitter Coupled Logic) and TTL strobe on the bus, with the PECL clock used for higher frequency (> 20 MHz) transfers. If designing to the CMC card, only an LVTTL clock is generated by the card's FPDP transmitter port, since it is driving to a PCB instead of a long ribbon cable.

An FPDP receiver card (FPDP-R or FPDP-RM) accepts the PECL or TTL clock generated by the transmitter and uses it as the word clock for the data transfers. This clock is generally in the range of 0 to 40 MHz on standard FPDP busses, though the FPDP specification does not state a hard maximum frequency at which the bus may be run. The CMC card has a LVTTL clock input that it uses for the word clock.

E.3.2 Data Framing

The FPDP specification does not allow for the transmission of address information. However, many systems have data coming from several cards or channels. The way to identify data from each channel is through framing. A synchronization pulse signal, /SYNC, was defined for framing purposes. The frame size is defined as the number of data items in the frame. Unframed data may also be transmitted onto the FPDP bus. The four data frame types defined by the FPDP specification are listed and described below.

- Unframed data
- Single frame data
- Fixed size repeating frame data
- Dynamic size repeating frame data

UNFRAMED DATA

- Used when the source and the organization of the data is not important.
- Used when the FPDP receivers do not need to be synchronized to the data stream.
- /SYNC is not required.

When unframed data is transmitted onto the FPDP bus, no synchronization is required. Thus, the FPDP-TM must not generate /SYNC, and the FPDP-RM and FPDP-R devices must not require a /SYNC pulse in order to correctly receive data.

SINGLE FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs between data blocks.
- /SYNC must be asserted before /DVALID is asserted.
- Synchronization occurs infrequently, perhaps only once.

When single frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse before valid data starts being transmitted. Valid data is transmitted when the data valid signal /DVALID is asserted. Thus, a /SYNC pulse must be asserted before /DVALID is asserted when transmitting single frame data. After a /SYNC pulse is asserted, the FPDP-RM and FPDP-R devices should not accept data until the first STROBE period after /DVALID is asserted. The /SYNC pulse does not have to be asserted again until before the start of the next data transmission.

FIXED SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- All data frames are the same size.

When fixed or dynamic size repeating frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse while /DVALID is already asserted. The /SYNC pulse must be asserted at the same time as the last data item of every frame. The FPDP-RM and FPDP-R devices must recognize that the current data is the last data item in current frame when both /SYNC and /DVALID are asserted. Since /SYNC is asserted at the end of a frame, the first data frame transmitted will not be synchronized. As a result, the system designer may wish to discard this first unsynchronized data frame. All data frames are the same size when fixed size repeating frame data is transmitted.

DYNAMIC SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- Data frames may vary in size.

For dynamic size repeating frame data, the behavior of the /SYNC pulse is the same as for fixed size repeating frame data, with the exception of varying sized frames.

E.4 Serial FPDP Theory of Operation

The protocol and framing for Serial FPDP are listed in Appendix C. Serial FPDP operates similar to parallel FPDP with respect to maintaining data framing with the SYNC signal, but the SYNC signal does not correlate with data frames on the fiber. Any form of data framing listed in section E.3.2 can be mapped to Serial FPDP, since the data stream and SYNCs are maintained. However, the timing may not be exactly the same as the parallel FPDP version due to link framing overhead and the fact that the link operates asynchronously to the parallel FPDP frequencies.

E.5 Parallel FPDP Signal Timing

Figure E-2 shows the timing for several FPDP interface signals. This figure is accurate for all four data framing types. See section E.3.2 for a discussion of framing. The Data Valid signal, /DVALID, is asserted by the FPDP-TM when valid data is transmitted onto the FPDP bus but not before at least 16 STROBE periods have occurred. The FPDP-TM must de-assert /DVALID when no more data remains in its buffer until valid data is again available. To avoid losing data when the receiver's FIFO is almost full, the receiver (FPDP-RM or FPDP-R) must assert the /SUSPEND signal to hold off the transmitter. The FPDP-TM must de-assert /DVALID within 16 STROBE periods and keep it de-asserted until /SUSPEND is de-asserted. Per the FPDP specification, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least one STROBE period before re-asserting /DVALID. With the FibreXtreme SL240 card, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least two STROBE periods before re-asserting /DVALID. The /SUSPEND signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

The FPDP-TM must not transmit data onto the FPDP bus until the Not Ready signal, /NRDY, is de-asserted by the FPDP-RM and FPDP-R devices. The FPDP-RM and FPDP-R devices must assert /NRDY when they are not ready to accept data and must de-assert /NRDY otherwise. The /NRDY signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

As required by the *Front Panel Data Port Specifications, ANSI/VITA 17-1998,* the FPDP-TM transmits the Data Direction signal /DIR.FPDP-RM and FPDP-R devices may receive /DIR. The /DIR signal is not given a firm definition of use. Possible uses of this signal include providing a status indication available to be read by software or to allow operation to be inhibited until /DIR is asserted. The /DIR signal may be asynchronous with other FPDP signals. An SL240 FPDP-R or FPDP-RM inverts and passes this signal from the FPDP interface to the link interface. DIR is an active-high signal on the link interface. /DIR is an active-low signal on the FPDP interface.

Two user-defined Programmable I/O (PIO) signals, PIO1 and PIO2, are reserved in the *Front Panel Data Port Specifications*. These are auxiliary signals that are not required for core FPDP functions. However, these signals can be user-defined to allow the FPDP-TM, FPDP-RM, and FPDP-R devices to transfer information that is not part of the FPDP specifications. The FPDP-TM, FPDP-RM, and FPDP-R devices must not drive either of the PIO lines immediately at power up of the system. This is to avoid the possibility of two devices driving the same PIO line simultaneously and causing damage to the driver device.

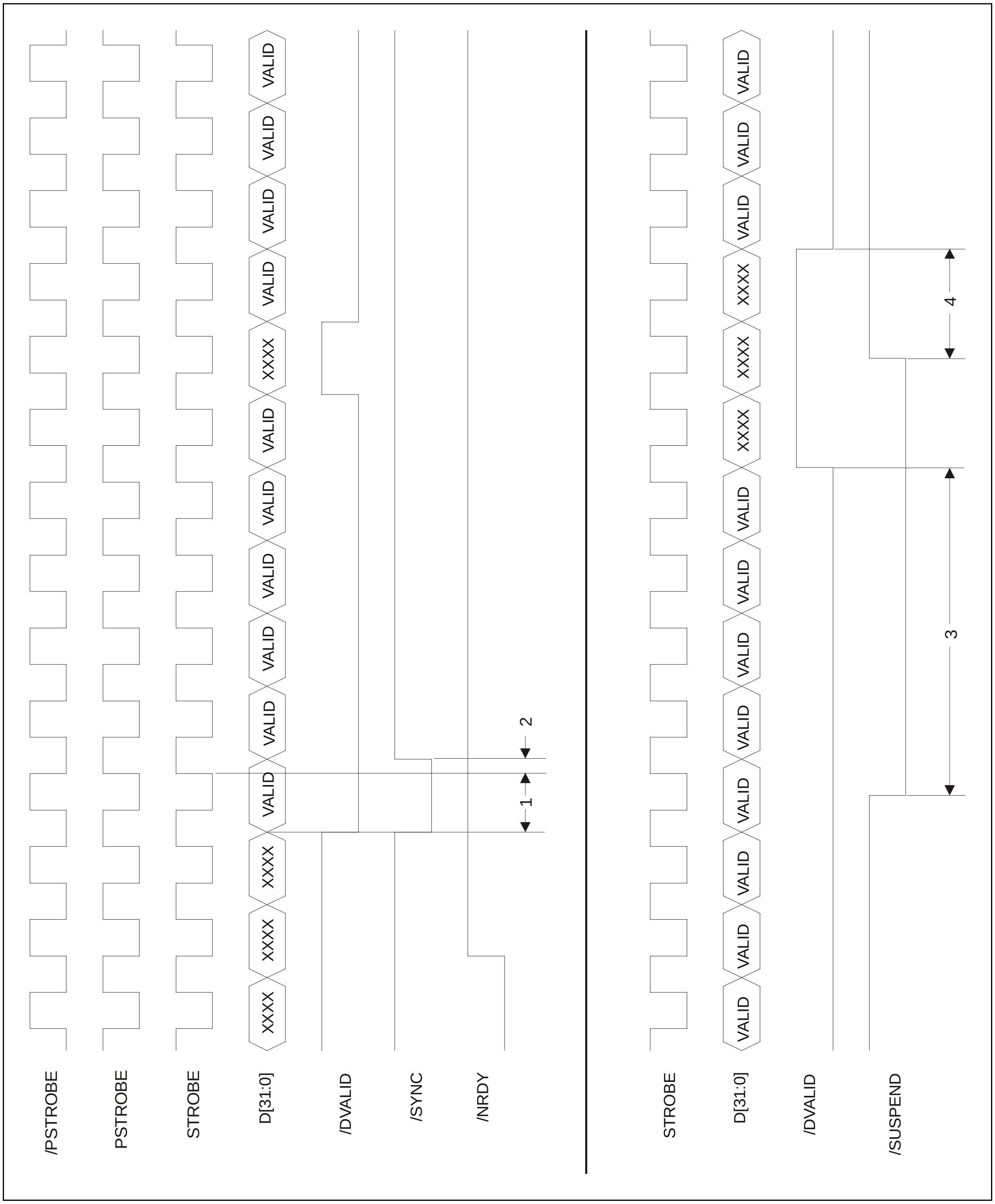

Figure E-2 Parallel FPDP Interface Timing Diagram

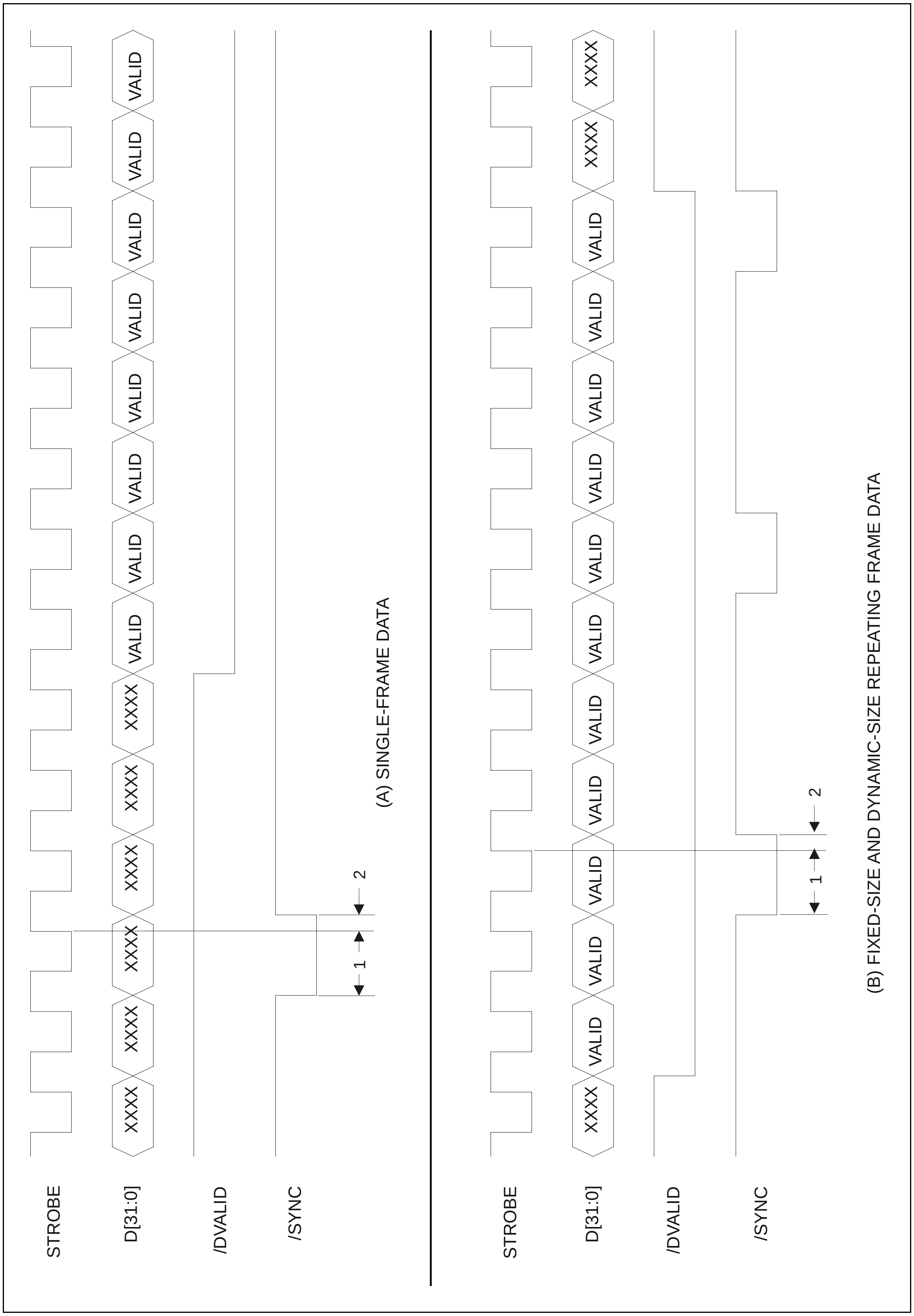

Figure E-3 FPDP Timing Diagrams Showing the Use of Framing

The timing parameters from Figures E-2 and E-3 are detailed in Tables E-1 and E-2. These timing specifications are taken from Front Panel Data Port Specifications, ANSI/VITA 17.

Table E-1 Parallel FPDP Timing Specifications

Parameter	Description	At Transmitter End of Cable	At Receiver End of Cable	FPDP Clock Used
1	Data, /DVALID, /SYNC setup time	6.0 ns min.	5.0 ns min.	TTL
1	Data, /DVALID, /SYNC setup time	5.5 ns min.	4.5 ns min.	+/- PECL
2	Data, /DVALID, /SYNC hold time	12.8 ns min.	11.8 ns min.	TTL
2	Data, /DVALID, /SYNC hold time	12.0 ns min.	11.0 ns min.	+/- PECL

Table E-2 FPDP Transmitter Interface Timing Specifications

Parameter	Description	Min	Max
3	/SUSPEND asserted to data stop	---	16 clocks
4	/SUSPEND de-asserted to data started	1 clock	---

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GLOSSARY

1x3 ----------------------------------A 3-pin connector for use with copper media.

8B/10B -----------------------------A data-encoding scheme developed by IBM for translating byte-wide data to an encoded 10-bit format.

AAL5 --------------------------------ATM Adaptation Layer for computer data.

active -------------------------------A term used to denote a port that is receiving a signal.

AL-----------------------------------See Arbitrated Loop.

ALPA--------------------------------Arbitrated Loop Physical Address.

ANSI--------------------------------American National Standards Institute.

AP-----------------------------------Access Point.

API----------------------------------Applications Program Interface.

APID -------------------------------Access Point Identification Number. A number ranging between 0 and 65535 that is assigned by the user to identify a process. All APID's attached to a single FX board must be unique.

arbitrated loop -------------------The simplest form of a Fabric topology. Has shared bandwidth, distributed topology. Interconnects NL_ports/FL_ports at the nodes/Fabric using unidirectional links. It has only one active L_port-L_port connection, so blocking is possible. A fairness algorithm ensures that no L_port is blocked from accessing the loop. Should any link in the loop fail, communication between all L_ports is terminated (see cross-point, point-to-point).

ASIC--------------------------------Application Specific Integrated Circuit. An integrated circuit designed to perform a specific function. ASICs are typically made up of several interconnected building blocks and can be quite large and complex.

ATM--------------------------------Asynchronous Transfer Mode. A network technology that transfers data in small 53-byte packets, and permits transmission over long distances. Proposed speeds range from 25 Mbps to 622 Mbps.

bandwidth -------------------------The amount of data that can be transmitted over a channel.

baud --------------------------------A unit of speed in data transmission, usually equal to one bit per second.

BIOS--------------------------------Basic Input/Output System.

bps ----------------------------------bits per second.

broadcast --------------------------Sending a transmission to all nodes on a network.

BSP ---------------------------------Board Support Package. A set of software routines written by the OS vendor or SBC vendor that provides support for a particular SBC.

burst transfers--------------------Messages are transmitted in a format that includes the initial address followed by all the data. Burst transfers eliminate the need for repeated addresses for each data block, permitting higher throughput.

channel-----------------------------A point-to-point link that transports data from one point to another at the highest speed with the least delay, performing simple error correction in hardware. Channels are hardware intensive and have lower overhead than networks. Channels do not have the burden of station management.

channel network -----------------Combines the best attributes of both channel and network, giving high bandwidth, low latency I/O for client server. Performance is measured in transactions per second instead of packets per second.

circuit ------------------------------Bi-directional path allowing communications between two L_Ports.

circuit-switched mode-----------Data transfer through a dedicated connection (Class 1).

CMC--------------------------------Common Mezzanine Card.

communications protocol ------A special sequence of control characters that are exchanged between a computer and a remote terminal in order to establish synchronous communication.

Conduction Cooled --------------Heat dissipated by transfer between solids. In the case of circuit boards, heat transfer from a thermal conductive layer in the board to a physically connected mass such as a large aluminum plate.

Convection Cooled---------------Heat dissipated by the flow of fluids. In the case of circuit boards, the typical heat dissipation is by airflow.

CPCI -------------------------------Compact Peripheral Component Interface. See PCI.

CRC --------------------------------Cyclic Redundancy Check. A code used to check for errors in Fibre Channel.

cross-point-------------------------Provides a bi-directional connection between a node (N_port) and the Fabric (F_port). Can be configured to be non-blocking by providing multiple paths between any two F_ports. Adding stations to a Fabric does not reduce the point-to-point channel bandwidth (see point-to-point).

datagram --------------------------Type of data transfer for Class 3 service. Transfer has no confirmation of receipt and rapid data transmission.

dBm---------------------------------decibels relative to one milliwatt.

direct connect links--------------An actual physical, dedicated connection between two devices with the entire bandwidth available to serve each direct link. Direct links provide a fast and reliable medium for sending large volumes of data.

DMA--------------------------------Direct Memory Access.

DMA write ------------------------The DMA engine on the bus controller writes the data from the host computer to the SRAM buffer, freeing the host CPU for other tasks. (FibreXpress board becomes a master for the bus.)

E_Port------------------------------Element Port. Used to connect fabric elements together.

ECL---------------------------------Emitter Coupled Logic.

ethernet ----------------------------A widely used shared networking technology.

exchange ---------------------------One or more sequences for a single operation that are not concurrent, but are grouped together.

F_Port------------------------------Fabric Port. The access point of the fabric for physically connecting the user's N_Port.

fabric -------------------------------A self-managed, active, intelligent switching mechanism that handles routing in Fibre Channel Networks.

fabric elements -------------------Another name for ports.

FC------------------------------------Fibre Channel.

FC-AL------------------------------Fibre Channel Arbitrated Loop. Provides a low-cost way to attach multiple ports in a loop without hubs and switches.

FCP ---------------------------------Fibre Channel Protocol. The mapping of the SCSI communication protocol over Fibre Channel.

FC-PH------------------------------Fibre Channel Physical interface. Fibre Channel Physical standard, consisting of the three lower levels, FC-0, FC-1, and FC-2.

FCSI --------------------------------Fibre Channel Systems Initiative is made up of IBM, Hewlett-Packard and Sun Microsystems. This group strives to advance Fibre Channel as an affordable, high-speed interconnection standard.

FC-SW -----------------------------Fibre Channel Switch Fabric standard. Formerly known as FC-XS: Fibre Channel Xpoint Switch. The crosspoint-switched fabric topology is the highest-performance Fibre Channel fabric, providing a choice of multiple path routings between pairs of F_ports.

Fibre Channel --------------------Fibre Channel (FC) is a serial data transfer interface technology operating at speeds up to 1 Gbps. It is defined as an open standard by ANSI. It operates over copper and fiber optic cabling at distances of up to 10 kilometers. Supported topologies include point-to-point, arbitrated-loop, and fabric switches.

FibreXpress -----------------------A Curtiss-Wright Controls, Inc. trademark name for a family of networking products that maximize the superior communication and interconnect capabilities of ANSI standard Fibre Channel. The FX200 series of 64-bit adapters support up to 200 MB per second (400 MB per second duplex) throughput. The FX100 series supports 100 MB per second throughput.

FibreXtreme ----------------------A Curtiss-Wright Controls, Inc. trademark name for a family of networking products based on the original Simplex Link technology, Curtiss-Wright Controls' FibreXtreme Serial FPDP Data Link moves data at a sustained 247 MB per second with microsecond latency. Supports up to 2.5 Gbps serial data link using a highly specialized communications protocol optimized for maximum data throughput.

FIFO--------------------------------first in first out

Firmware --------------------------Microprocessor executable code, typically for embedded type processors.

Flash--------------------------------A type of Electrical Erasable Programmable Read Only Memory (EEPROM). Erased and written to in blocks vs. bytes.

FL_Port----------------------------Fabric Loop Port. Joins an arbitrated loop to the fabric.

FPDP -------------------------------Front Panel Data Port.

frame -------------------------------A linear set of transmitted bits that define a basic transport element. A frame is the smallest indivisible packet of data that is sent on the FC.

frame-switched mode -----------Data transfer is connectionless (Classes 2 and 3) and data transmission is in frames. The bandwidth is allocated on a link-by-link basis. Frames from same port are independently switched and may take different paths.

FTP application ------------------A test application for transferring files from one computer to another.

FX-----------------------------------FibreXpress.

GLX4000 ---------------------------LinkXchange GLX4000 Physical Layer Switch.

G_Port ------------------------------A port which can function as either an F_Port or an E_Port. Its function is defined at login.

Gbps ---------------------------------Gigabits per second.

gigabit -------------------------------One billion bits, or one thousand megabits.

GLM---------------------------------Gigabit per second Link Module. A Link Module that can be used for optical or copper media.

HANDLE --------------------------Abstraction for the *Handle* in Windows and *file descriptor* in Unix.

HBA --------------------------------Host Bus Adapter.

heartbeat --------------------------A visual indicator that flashes periodically to indicate the embedded controller is functioning properly.

HIPPI ------------------------------High Performance Parallel Interface. An 800 Mbps interface to supercomputer networks (previously called high-speed channel) developed by ANSI.

HSSDC-----------------------------High Speed Serial Data Connectors and Cable Assemblies. A type of high-speed interconnect system which allows for transmission of data rates greater than 2 Gbps and up to 30 meters.

hunt group ------------------------A group of lines that are linked so that one call to the group will find the line that is free. This provides the ability for more than one port to respond to the same alias address.

I/O ----------------------------------Input/Output.

IOCB -------------------------------I/O Control Block. A block of information stored in system memory, usually of fixed length, which contains control codes and data. The IOCB is created by a host computer and sent to some other computer. The IOCB contains command/instructions, data, and memory pointers intended to direct the other computer to perform some function.

inactive-----------------------------A term used to denote a port that is not receiving a signal.

intermix----------------------------A Fibre-Channel-defined mode of service that reserves the full Fibre Channel bandwidth for a dedicated (Class 1) connection, but also allows connectionless (Class 2) traffic to share the link if the bandwidth is available.

IP------------------------------------Internet Protocol is a data communications protocol.

IPI-----------------------------------Intelligent Peripheral Interface.

insertion delay--------------------The amount of time the data is delayed for the insertion of FXSL framing protocol. It is measured from when the data becomes available at the FIFO to when the data is actually transmitted on the link. The actual values are either 188 ns in Mode-0 or Mode-1 (with no CRC), or 226 ns in Mode-2 or Mode-3 (with CRC).

KB ----------------------------------KiloBytes.

L_Port------------------------------Loop Port. Either an FL_Port or an NL_Port that supports the arbitrated loop topology.

LAN --------------------------------Local Area Network, typically less than 5 kilometers. Transmissions within a LAN are mostly digital, carrying data at rates above 1 Mbps.

latency------------------------------The delay between the initiation of data transmission and the receipt of data at its destination.

LCF---------------------------------Link_Control Facility. Provides logical interface between nodes and the rest of Fibre Channel.

Link Module ----------------------A mezzanine board mounted on the board to interface between the board and the network.

longword---------------------------32-bit or 4-byte word.

LP -----------------------------------Lightweight Protocol.

LX1500-----------------------------LinkXchange LX1500 Crossbar Switch.

LX2500-----------------------------LinkXchange LX2500 Crossbar Switch.

Mbps--------------------------------Megabits per second.

MBps -------------------------------MegaBytes per second.

MB ---------------------------------MegaBytes.

media ------------------------------Means of connecting nodes; either fibre optics, coaxial cable or unshielded twisted pair.

ms -----------------------------------Milliseconds

µs ------------------------------------Microseconds

monitor ---------------------------An application program used to display the status and change the configuration of the driver.

multicast --------------------------A single transmission is sent to multiple destination N_ports, a one-to-many transmission. Multicasting provides a way for one host to send packets to a selective group of hosts.

N_Port------------------------------Node Port. A Fibre-Channel-defined entity at the node end of a link that connects to the fabric via an F-Port.

network ---------------------------Connects a group of nodes, providing the protocol that supports interaction among these nodes. Networks are software intensive, and have high overhead. Networks also operate in an environment of unanticipated connections. Networks have a limited ability to provide the I/O bandwidth required by today's applications and client/server architectures.

NL_Port----------------------------Node Loop Port. Joins nodes on an arbitrated loop.

node--------------------------------A host computer and interface board. Each processor, disk array, workstation or any computing device is called a node. Connects to FC through a node port (N_Port).

normal write ---------------------A host CPU writes data to the SRAM buffer through the bus and bus controller (FibreXpress board operates as a slave of the bus).

ns ------------------------------------nanoseconds.

NVRAM ---------------------------Non-Volatile Random Access Memory. Generic term for memory that retains its contents when power is turned off.

OFC---------------------------------Open Fibre Control. A safety interlock system used on some FC shortwave links.

one-to-many-------------------------One node transmits to multiple nodes. See broadcast, multicast.

operation----------------------------One of Fibre Channel's building blocks composed of one or more exchanges.

out-of-band control---------------On the LinkXchange products, a method of issuing switch commands that does not use any bandwidth of the 32 switch ports.

PCB ----------------------------------Printed circuit board.

PCI -----------------------------------Peripheral Component Interface. A PC bus that allows some expansion boards to communicate directly with the CPU in either 32 bits or 64 bits at a time, this bus also permits multiplexing (more than one electrical signal to be present on the bus at one time).

physical layer switch ------------Multipurpose, non-blocking multi-port cross-point switch (See cross-point).

PIO-----------------------------------Programmed Input/Output.

PMC ---------------------------------PCI Mezzanine Card. Everything that is true for PCI cards is true for PMC except there is a footprint or card format change.

point-to-point---------------------Bi-directional links that interconnect the N_ports of a pair of nodes. Non-blocking.

port ---------------------------------A physical element through which information passes. It is an electrical or optical interface with a pair of wires or fibers—one each for incoming and outgoing data.

profiles -----------------------------Subsets of Fibre Channel standards that improve interoperability and simplify implementation. It is like a cross-section of FC, providing guidelines for implementing a particular application.

protocols ----------------------------Data transmission conventions encompassing timing, control, formatting, and data representation. This set of hardware and software interfaces in a terminal or computer allow it to transmit over a communication network, and these conventions collectively form a communications language.

retimed------------------------------"Retimed" port cards use a phase-locked loop to recover the clock from a serial data stream. They then use the recovered clock to strobe the data through a one-bit latch to minimize the accumulation of edge jitter. This process is sometimes called "reclocked." (Retimed port cards do *not* synchronize the data to a local crystal-controlled reference clock.) Non-retimed port cards do not clock the serial data stream at all. From a timing standpoint, they function as gate delays as the data passes asynchronously through them.

RISC---------------------------------Reduced Instruction Set Computer. A type of microprocessor that executes a limited number of instructions that typically allows it to run faster than a Complex Instruction Set Computer (CISC).

RJ-45 -------------------------------Short for Registered Jack-45. An eight-wire connector commonly used to connect computers onto a local-area network (LAN), especially Ethernet. RJ-45 connectors look similar to the RJ-11 connectors used for connecting telephone equipment, but they are somewhat wider.

SAP ----------------------------------Service Access Point.

SBC ----------------------------------Single Board Computer.

SCSI ---------------------------------Small Computer System Interface.

sequence ----------------------------The unit of transfer, made up of one or more related frames for a single operation.

SFF-----------------------------------Small Form Factor. Based on SFF MSA.

SFF MSA --------------------------Small Form Factor Transceiver Multisource Agreement (SFF MSA), July 5, 2000.

shared connect links-------------The ability to send and receive data without establishing a dedicated physical connection so that other devices can also use the medium. This shared link is more efficient for smaller data transmissions because the overhead of direct connect link is avoided.

SRAM -------------------------------Static Random Access Memory.

SRAM Transfer ------------------Process in which the data is transferred from the host computer to the SRAM buffer by normal or by DMA write.

SFP-----------------------------------Small Form Factor Pluggable based on MultiSource Agreement (MSA), September 14, 2000, FO Transceiver Industry.

STP-----------------------------------Shielded Twisted Pair. A type of cable media.

striping -----------------------------To multiply bandwidth by using multiple ports in parallel.

switched fabric -------------------(see the definition for “fabric”).

SYNC--------------------------------FibreXtreme Simplex Link primitive used to synchronize the source and destination cards.

SYNC with dvalid ---------------A special case of the SYNC primitive occurring in the middle of a buffer of data.

TCP---------------------------------Transmission Control Protocol.

terminal application-------------A test application that sends characters received from the keyboard and displays received characters.

throughput application ---------An application that tests the throughput for the given system.

time-out ----------------------------The time allotted for a native message to travel the network ring and return. If this time is exceeded, an automatic retransmission of the native message occurs.

topology ----------------------------Refers to the order of information flow due to logical and physical arrangement of stations on a network.

ULP----------------------------------Upper Level Protocol.

VHDL ------------------------------Very high-speed integrated circuit Hardware Description Language.

VME--------------------------------Acronym for VERSA-module Europe: bus architecture used in some computers.

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