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MAIN PROCESSOR UNIT MPU13 Unit Description

MPU13-S126en-1.4
10 November 1999
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VAISALA

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1. FUNCTIONAL DESCRIPTION

1.1. General

The MPU13[1] Main Processor Unit is an E2-size printed circuit board functioning as central processor for radiosonde data receiving systems. The card comprises a CPU (80C186 + 80C187), an EPROM, a RAM, an EEPROM, serial communication channels (15 pcs.), a calendar clock and a program storage memory. Connections to the other modules of the system are accomplished via serial channels.

[1] The letter "P" in the end of the unit type, e.g. MPU13P, denotes that the front plate of the unit is suitable for card frames of the PP15 and MW15 instruments. Otherwise the board is compatible with MPU13 unit.

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2. OPERATION

NOTE

An asterisk (*) following a signal name indicates that the signal is active at low voltage level.

2.1. CPU

The CPU consists of the processor circuits 80C186 (CPU) and 80C187 (NPU). 80C186 performs the general processing whereas 80C187 is an auxiliary processor for numeric operations. 80C187 is connected to the CPU as an I/O device having the selection signal NPS*. The output signals of NPU, namely BUSY, PEREQ and ERROR inform the CPU about the operational state of the auxiliary processor

The oscillator Q2 feeds the clock frequency of 32 MHz to the CPU, of which CPU's actual operation clock frequency of 16 MHz (CLKOUT) is formed (divided by two).

In addition to the normal processor functions, the CPU comprises the following peripheral functions: interrupt controller, generation of chip selection signals, timer/counter unit, dynamic memory refresh controller and DMA unit that is not used in this application.

2.2. Memory

2.2.1. EPROM

The EPROM memory is formed by the circuits D28 and D27. The CPU selects the EPROM memory by means of the signal UCS*, which is connected to the memory circuits via D49 or module MW45134 as signal EPCS* always as the memory map function of D49 or MW45134 is not activated. The memory addresses are connected via the latches D32 and D40. The outputs of D40 are held active during the whole EPROM memory cycle.

After a reset situation, the CPU starts the program code execution from the EPROM memory beginning from the CPU address FFFF0.

2.2.2. Dynamic RAM Memory

The DRAM memory of 2 megabytes is formed of the 1 M x 4-bit memory circuits D41, D42, D43 and D44. The memory control is performed by the logic circuit D49 or D1 in module MW45134.

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The CPU directly uses the address space 00000 - EFFFF of the DRAM memory. The rest of the memory is used through the memory map logic, see point 2.2.3 “Memory paging”.

The latches D39 and D40 store the addresses A1 - A16 at the falling edge of the signal ALE.

The logic circuit D49 or D1 in module MW45134 stores the addresses A0 and A17 - A19 as well as forms the following memory control signals:

Signal Name	Description
PDTR	Determines the direction of the bus transceiver of I/O databus.
PDEN*	Activates the bus transceiver
PALE	The signal drives the column address to the memory address bus MA0 - MA7 by activating the outputs of the latch D40.
PRD*	The falling edge of the signal stores the column address to the memory circuits.
PWR*	The rising edge of the signal writes the data on the databus AD0 - AD7 to the memory circuits D41 and D42. The signal is activated during memory write cycle if A0 = 0
PWR*	The rising edge of the signal writes the data on the databus AD0 - AD7 to the memory circuits D41 and D42. The signal is activated during memory write cycle if A0 = 0.
A18PWR	The rising edge of the signal writes the data on the databus AD8 - AD15 to the memory circuits D43 and D44. The signal is activated during memory write cycle if BHE* = 0.
3.68MHz	The signal activates the outputs of the memory circuits during memory read cycle.

Additionally, D49 or module MW45134 feeds the row and column addresses MA8 and MA9 of the memory (generation of MA8, MA9, see 2.2.3).

2.2.3. Memory Paging

The memory paging logic is implemented with the programmable logic circuit D49 or D1 in module MW45134. The circuit comprises a 4-bit map register and selection logic that feeds the CPU addresses A17, A18 and A19 as memory addresses MA8, MA9, when the memory paging is not in use or, respectively, the contents of the map register, when the memory paging is in use.

The contents of the map register is written in serial form via the input signal AD0.

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2.2.4. EEPROM

The memory circuits D21, D30, D38 and D48 constitute this memory. The EEPROM memory is located in the I/O area of the processor. The memory address is loaded by separate I/O commands to the address register circuits D47, D37 and D34. The circuit selection is performed by the decoder circuit D19.

2.2.5. Program Storage Memory

The memory circuits D10, D15, D17, D29, D36 and D46 constitute the program storage memory. The memory is located in the I/O area of the processor similarly to EEPROM. The circuit selection is performed by the decoder circuit D18. The memory sockets may be partially equipped. Either EPROM (normally) or FLASH type memory components can be used.

2.2.6. Calendar Clock

Circuit D8 is the calendar clock comprising an oscillator, clock circuit and built-in lithium battery. The circuit is connected directly to the I/O databus. Only the data line PD0 is used for the connection.

2.2.7. Serial Channels

Serial communication is handled by two 8-channel UART circuits D9 and D16. The circuits are connected to the I/O databus of the processor. The clock signal for the UARTs (3.6864 MHz) comes from crystal Q1 through circuit D50.

The channels A - G of the circuit D16 and the channels A - F of the circuit D9 are buffered on RS-232C levels to the Euroconnector X1 of the card. The channels G and H of the circuit D9 are correspondingly buffered on RS-422 levels to the connector X1. The channel H of the circuit D16 is reserved for the future internal use of the card.

The interrupt outputs of the UART circuits are connected to the interrupt inputs INT0 and INT1 of the processor via inverters.

2.2.8. Output Registers and Signals

The circuits D24 and D25, controlled by the processor, form the following output signals:

Signal Name	Description
FPWEN	Flash memory write enable
EEWEN	EEPROM write enable
AWSEL	Address/write signal select to storage memory (write signal not in use)

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EFMSEL	External FM signal select
GPO1T, GPO2T	General purpose output signals

Additionally, the outputs of the circuit D25 control the indicators OK, ERR and I/O of the card.

2.2.9. Parallel Input Signals

Signal Name	Description
TEST*	Test input forcing MPU into test mode when activated after RESET
GPI1, GPI2	General purpose inputs (not in use)
REMST	Not in use

The following signals are connected from the card edge connector via buffers and UART circuits to the processor.

2.2.10. Reset Logic

Circuit A11 generates RESET signal (RES and RES*), if the +5 V operating voltage falls below +4.5 V or if the external signal SYSRES* is in active state.

2.2.11. I/O Control and Clock Divider

The circuit D50 generates the following control and clock signals:

Signal Name	Description
PDTR	Determines the direction of the bus transceiver of I/O databus
PDEN*	Activates the bus transceiver.
PALE	Stores the I/O address to register D31.
PRD*	I/O read signal.
PWR*	I/O write signal
A18PWR	Address A18 signal to storage memory.
3.68MHz	Clock signal to UART circuits

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3. SPECIFICATIONS OF MPU13

CPU	Processor type	80C186 + 80C187
	Clock frequency	16 MHz
Main Memory	DRAM	2 MB
	EPROM	128 kB
Storage Memory	EPROM or FLASH	3 MB (maximum)
	EEPROM	128 kB
Serial Lines	RS-232-C	13 channels
	RS-422	2 channels
	Baud rates	50...38400 bps
Parallel input/output	Inputs	2 pcs, RS-323C levels
	Outputs	2 pcs, RS-323C levels
		1 pcs, TTL
Real-Time Clock	Power source	Internal battery
	Estimated life span	10 years
	Accuracy	±60 seconds/month
Power Requirements (approx.)	+ 5 V (± 5 %)	900 mA
	+ 15 V (± 5 %)	100 mA
	– 15 V (± 5 %)	50 mA
Environmental Requirements	Storage temperature	–55 ... +70 °C
	Operating temperature	0 ... +55 °C
Mechanical Data	Type of board	E2-size Printed Circuit Board
	Dimensions (D x W x H)	190 x 262 x 20 mm
	Weight	400 g

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4. TESTING INSTRUCTIONS

The MPU13 Main Processor can be tested by using its built-in test programs through serial terminal.

The tests requiring MJ11A Test Fixture are marked with (MJ) in the following instructions.

4.1. Required Equipment

- Asynchronous serial data terminal
- 10106 ZZ terminal cable
- Multimeter V, A, Ω
- Oscilloscope
- Frequency counter
- Extension card with 64-pin Euroconnector[2]
- MJ11A Test Fixture

CAUTION

Always turn of power from the unit or MJ11A prior to removing or installing a unit.

4.2. Power Consumption

(MJ) Place the unit in the MJ11A Test Fixture and connect the current meter alternately to the +5, +15 and -15 V lines. Use toggle switches S1, S2 and S3 to divert the power supply line through the meter.

Nominal power consumption figures after completion of the unit self test and with the TEST switch of the MJ11A in the OFF position are given in table 1.

Voltage (V)	Current (mA)
+15 ±0.75	20…40
+5 ±0.25	500…900
–5 ±0.25	-
–15 ±0.75	20…40

Table 1 Power Consumption

[2] If the entire testing is carried out in MJ11A the extension card is not needed.

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4.3. Clock Frequencies

To check clock frequencies, either connect unit MPU13 to an extension card or use the MJ11A.

Check the frequency and level of oscillator Q1 at D50 pin 2:

22.09…22.14 MHz, TTL

Check the frequency and level of oscillator Q2 at D50 pin 3:

31.96…32.04 MHz, TTL

4.4. Connecting the Terminal

4.4.1. In-Frame Test

Connect the terminal to the connector P1 (or S1 in MW12A) of the RAWINSONDE SET and place it in the test mode as instructed in section USE OF THE TEST PROGRAMS. Right after MONITOR mode selection, the serial channel used for the MPU13 tests connects to the terminal and title of test program is shown on monitor.

4.4.2. Test in MJ11A

Connect the terminal cable to MJ11A connector X12. Terminal settings are:

- 9600 bps
- 8 data bits, 1 stop bit
- no parity

Place the unit in the horizontally positioned Euroconnector of the MJ11A. Turn on power of the MJ11A, turn on the TEST switch and press RESET. During the reset signal, ERR and OK indicators are lit.

4.5. Test Commands

The following test monitor title text appears on the terminal and will then be followed by command prompt '*****'

MPU13 TEST MONITOR VERSION X.XX (YY-MM-DD)

4.5.1. Multiprogram

The multiprogram command is given when the initial tests are to be run. Enter the command:

M_1<cr> _ = Space, <cr> = Carriage Return or Enter

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While the test is going on, front panel indicators flash as described in the beginning of the test monitor operating instructions. Upon completion of the test, the error map is output on the terminal. In the map, the first sixteen bytes should be zeros.

A continuous test can be carried out by placing the unit in the continue mode before issuing the test command. For more information on M-command output parameters, refer to the test monitor operating instructions.

4.5.2. EEPROM

The four EEPROMs on the MPU13 board can be tested without interfering in their contents. Circuits 1 (D48), 2 (D38) and 3 (D30) are treated as one memory circuit containing identical data. When writing in, the same memory location in each circuit is occupied. When reading, data are compared and any discrepancy is omitted and replaced by correct data as far as possible.

The fourth EEPROM circuit (D21) is used apart from the back-up memories 1, 2 and 3.

4.5.2.1. EEPROM Test

Test for all EEPROM circuits are started by command:

J_9<cr>

If the test is passed, OK is output on the terminal, otherwise ERR. Information on the cause of the fault will be stored in bytes D, E and 10_H of the error map.

Additional information on the EEPROM test is available in a table upon command.

D_5<cr> ; (see also chapter 8, Additional Information)

NOTE

EEPROM tests should preferably not be run in the continue mode because the total number of EEPROM writes is limited.

4.5.2.2. Replacement of EEPROM

If tests of EEPROM circuits indicate failure proceed as follows.

Replace the chip indicated faulty by the test with a new similar one. Then the circuit must be initialized with a test monitor command. The initialization prepares the data structures of the EEPROM for data storage.

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NOTE

Initialization of circuits 1 to 3 resumes all SYSGEN settings such as line configuration and station parameters. Always set up the SYSGEN according to the local needs after initialization.

Key in the following command to invoke the mode in which the initialization command can be given (note – 2 spaces!)

Y_ _ACCE<cr>

The prompt '**!**' appears on the terminal. Key in the initialization command:

J_A_1FFF_<chip>_5AFE<cr>

where the parameter <chip> signifies the following:

<chip>	Purpose
1	Initialization of circuits 1, 2 and 3 (backed-up memory)
2	Initialization of circuit 4 (additional EEPROM)
3	Initialization of all EEPROMs 1…4

Verify that the replacement circuit operates properly by running the EEPROM test (see paragraph.4.5.2.1).

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5. USE OF THE TEST PROGRAM

5.1. Self-Test on Power-Up

The program starts when power is turned on. After initial reset, CPU registers are tested. If the registers operate without error, the 'ERROR' indicator LED is turned off and RAM testing begins. If an error is found in the RAM test, the program is interrupted and the red 'ERROR' indicator blinks continuously. If the RAM test is completed without error, a program that tests other functions will be started.

At the beginning of the test program the ports, interrupt vectors and stack pointers are initialized. The 'OK', 'ERROR' and 'I/O' LEDs flash shortly to indicate program start and the green indicator is flashed after each test phase that was passed without error. If an error is found, this is indicated by flashing the red indicator. When the program is completed, the green LED will blink as an indication, if no error has been found. However, if an error has been detected, the red 'ERROR' LED will be continously lit.

5.2. Indicators During Self-Test

With the instrument on and operating normally the indicator lights signify the following functions.

1 RESET turns on the OK and ERR LEDs.
2 ERR light goes out: end of reset signal, register test passed without error, RAM test begins.
3 OK light goes out.
4 ERR, OK and I/O flashed: RAM test passed without error, program for testing the other functions started.

The green OK LED is flashed after each test phase if passed without an error; the red ERR LED is flashed if an error has been found. A failed test can be identified even if the serial channel is not working, by counting the number of flashes after the start signal until the red LED flashes.

1	EPROM test completed.
2	Red ERR flashed (very shortly): CPU test completed
3	Clock module test completed.
4	Serial channels 0…7 test completed.
5	Serial channels 8…15 test completed.
6, 7	EEPROM test completed.
8-31	Yellow I/O flashed 24 times: program storage memory test proceeding.
32, 33	Frequency Meter test (not implemented)

6. Completion of the test program is indicated by several rapid flashes of the green OK LED if no error has been found. A steady red light is on if errors have been found. Indication of DRAM error is a continuous blinking ERR light. The duration of the tests is approx. 55 seconds.

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5.3. MPU TEST MONITOR PROGRAM

The test monitor is a program controlling the operation of various test programs. The test monitor is started after the RAM test or SELF test, if the test input (A24) is in '0' state.

The test monitor is controlled with a terminal connected to serial channel TXD2A/RXD2A (pins a3 and c3 at connector X1).

In normal command mode, the prompt '*' is shown. In the CONTINUE mode, the prompt is '%'.

Commands are entered through the terminal in the format

X_P1_P2...P10<cr>

where

X	is the command (refer to list of commands in Section 5.4)
P1...P10	refers to the command parameter comprising 1 to 4 hexadecimal characters.
_	Space
<cr>	Carriage Return or Enter

An incorrectly entered command can be canceled with the DEL key. The entire line will then have to be re-entered.

An incorrect parameter can be corrected by keying the correct value immediately after the incorrect one. The last four characters will be taken as the valid parameter.

If the monitor is in the CONTINUE mode, repeatedly calling the desired routine, its command mode can be restored by pressing the SPACE bar.

In response to an unidentified command, the monitor shows a question '**?**' mark.

5.4. List of Commands

The following commands are interpreted (the list can also be output to the terminal with the H command):

B RESTART MONITOR
C SET CONTINUE MODE
D DISPLAY
E (not in use)
F (not in use)
H HELP
J JOB
L LOOPS

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M MULTIPROGRAM
P EPROM REV. INFO
Q RESTART SYSTEM
R EPROM CHECKSUM
S SET SINGLE MODE
W WRITE HARD COPY
X LINK

5.4.1. B RESTART MONITOR

This command restarts the monitor from the beginning.

5.4.2. C SET CONTINUE MODE

This command sets the monitor to the CONTINUE mode, in which the command entered next will be called repeatedly. To return to the command mode, press SPACE.

5.4.3. D DISPLAY

This command outputs the desired test data tables or memory locations.

Command format:

D_P1_P2_P3

where

D the command
P1 the table selector as follows:
P2 and P3 see below

P1	Description
0	ERMAP 00...31 in BYTE format
1	Cumulative ERMAP 00 31 in BYTE format
2	RAM (block 0-F_H; 1 block = 65 kB) in BYTE format
3	EPROM checksum in WORD format
4	Not used
5	EEPROM information in BYTE format
6	Clock Module info in BYTE format (time)
7	Not used
8	Not used
9	Not used
A	Name of unit
B	Errors found during System Tests in BYTE format
C	Warnings in BYTE format
D	System info (ERMAP, STATUS, REVISION DATA) in BYTE format

Tables A to D are outputs from the System Tests.

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The BYTE format outputs are in direct sequence, in WORD outputs LSB is first, followed by MSB (two bytes per word), in DWORD outputs LSB is first followed by MSB part (four bytes per double word)

P2 is the starting address of the table to be output.
P3 is the last address of the table to be output.

It is not necessary to key in P2 and P3 when issuing the command. They are mainly needed only to limit memory dump. Output from memory can be paused with CTRL-S. Output is then resumed with CTRL-Q.

To interrupt output, press SPACE.

5.4.4. H HELP

This command outputs the list of commands to the terminal.

5.4.5. J JOB

This command calls utility programs associated with testing. A number of support programs can be started from the test monitor for use as tools in testing and fault tracing.

NOTE

In order to protect the circuit parameters against misuse, a password (mode '!') is used in JOBS related to EEPROMs.

The command format is

J_P1_[P2...Pn]

where
P1 is job number
P2...Pn are job-specific parameters as required

1 Read I/O port.
Reads the contents of a port and outputs it to the terminal in hexadecimal format.
P2 Address of the port. Refer to chapter "I/O Addresses".

2 Write I/O port.
P2 Port address. Refer to chapter "I/O Addresses".
P3 Data to be written to P2.

3 Clears the ERMAP and the cumulative ERMAP.

4 Set bit of output register 1 and 2.
P2 Output register select. 1 = output register 1, 2 = output register 2.

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P3 Selection of output line of the register. 0…7.
P4 Reset/Set the selected output. 0 = reset, 1 = set.

9 EEPROM test.

A EEPROM initialization.

Clears the contents of selected EEPROM memories and copies data from EEPROM test area into the circuits. The running time of the command depends on size of the EEPROM circuit. With 32 kB circuits it can be up to 35 minutes. OK is shown after successful run. In case of failure encountered in the memory, initialization is ceased and error message displayed on screen.

To get into a mode in which initialization is accepted, key in:

Y_ _ACCE

after which the prompt '**!**'appears on terminal display. The format of the command is:

J_A_P2_P3_P4

where

P2 Circuit size. 1FFF = 8 kB, 7FFF = 32 kB
P3 Circuit select for initialization. 1 = Circuits 1, 2 and 3 (D48, D38 and D30), 2 = circuit 4 (D21) and 3 = circuits 1 to 4 to be initialized.
P4 Password. Always 5AFE.

NOTE

After running the initializing command for circuits 1, 2 and 3, re-enter the SYSGEN settings before next sounding.

D Read calendar clock.

Reads and outputs the time from the calendar clock circuit. Last read out of the clock circuit can be output with the command D_6. Read clock command is effected upon pressing <cr>. Format of the time display is shown in sect. 8.2.

E Set Calendar Clock

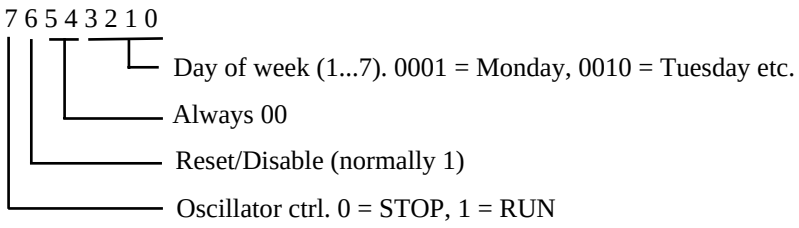
Sets calendar clock time. The clock is set upon pressing **<cr>**. Time is given in decimal numbers, except for parameter P9 which is in hexadecimal format. Command format is as follows:

J_E_P2_P3_P4_P5_P6_P7_P8_P9

P2 Year
P3 Month

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P4 Day
P5 Hour
P6 Minutes
P7 Seconds
P8 00
P9 Day of the week etc. control as follows



Example: To enable the real-time clock on Monday the parameter P9 is: $11000001_B = C1_H$

10 Calendar Clock Test.

Performs the calendar clock test and outputs the current time, the time of the preceding test pass, and the symbol of the clock type. More information available with the command D_6.

11 RUN TIME TEST

Performs one pass of the run time test. Additional data can be output with the command D_9.

P2 If set to 0, the RUN TIME TEST info, the ERROR indicator and the ERMAP (EPROM, RAM and RTES) will be cleared before the test (in CONTINUE mode before the first call).

13 EEPROM Data Comparing Test

The contents of circuits 1, 2 and 3 are compared mutually.

P2 Starting address of the comparison.
P3 Length of the memory area to be compared.

Output format:

xxxx: D1, D2, D3

where

xxxx address of memory location containing deviating data

D1 data from circuit 1
D2 data from circuit 2.
D3 data from circuit 3.

18 Serial Channel Test for Octal UART-1 (D16)

P2 Channels to be tested ('1' bit = test, '0' not tested) in hexadecimal format. The default value is 07.

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P3 Data transfer rate (value in CSR register of UART). Default = BB (=9600 bps).
P4 Loop back control: 0 = internal loop back connections of the UART, 2 = external loop back (requires loop back wires at X1 connector of MPU13).

19 Serial Channel Test for Octal UART-2 (D9)

P2 Channels to be tested ('1' bit = test, '0' not tested) in hexadecimal format. Default value = FE.
P3 Data transfer rate (value in CSR register of UART). Default = BB (=9600 bps)
P4 Loop back control: 0 = internal loop back connections of the UART, 2 = external loop back (requires loop back wires at X1 connector of MPU13).

5.4.6. L LOOPS

Support programs for signature analysis or oscilloscope measurement (not used).

5.4.7. M MULTIPROGRAM

The command

M_P1

is used to run the SELF TEST routines from the test monitor. The routines can be carried out repeatedly by setting the monitor in the CONTINUE mode before the call.

M is the multiprogram call.
P1 is the output control parameter (not necessary).

P1	Action
1	ERMAP output after each pass.
2	ERMAP output if error found during pass.
3	Stop continuous test if error found.
4	ERMAP output after each test pass and stop continuous test if error found.
5	ERMAP output and stop continuous test if error found.

To terminate execution of the test, press SPACE (must be done between test passes because the serial channel is looped back during the test).

For example:

C Sets the monitor into the CONTINUE mode.

M_6 Starts repeated execution of multiprogram test. If an error is found, the ERMAP will be output after the test pass and the monitor will put in the SINGLE mode, causing execution of the test to stop.

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5.4.8. P EPROM REV. INFO

This command outputs the revision status data of the program circuit. Output format is the following:

1 module name
2 program version number
3 Julian date
4 special.

5.4.9. Q RESTART SYSTEM

This command restarts the program from the beginning as after reset (but without hardware reset).

5.4.10. R EPROM CHECKSUM

This command outputs the calculated and programmed checksums of the program EPROM.

5.4.11. S SET SINGLE MODE

This command sets the monitor into the SINGLE mode, in which the command entered next is executed only once (default condition after program start).

5.4.12. W WRITE HARD COPY

This command controls output of test monitor commands and results to printer. Command format:

W_A auto mode according to SYSGEN settings

W_P1_P2_P3 setting chosen by user

where

P1 Channel (0…F_H)

P2 Data transfer rate (0 to 8)
0 = 1200
1 = 110
2 = 300
3 = 600
4 = 1200
5 = 2400
6 = 4800
7 = 9600
8 = 19200

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P3 Line settings
0 a b c
a = parity: 0 = none, 1 = odd, 2 = even
b = number of stop bits: 1 or 2
c = number of bits: 8 or 7

5.4.13. X LINK

This command connects the serial data terminal plugged in to P1 connector directly to the desired serial channel (processor unit).

The command format is

X_P1_P2_P3

where

X is the link (through-connect) command

P1 Channel selection ($1\text{-}10_H$)
P2 Baud rate change control
0 change baud rate of selected channel (see P3)
1 the baud rate change macro for the console
2 the baud rate change macro for the Receiver Processor (UR)

P3 Baud rate (if P2 = 0)
11 110
44 300
55 600
66 1200
88 2400
99 4800
BB 9600
CC 19200

The plain command

X

immediately returns the program to the MPU test monitor.

Data coming from the selected serial channel to the terminal is buffered in the MPU ring buffer (256 bytes). If the buffer capacity is exceeded (overrun error) the 'ERR' indicator of the MPU alights and the buffer is cleared.

List of parameters of LINK command for RAWINSONDE SET modules is given in this manual, in the end of the section 'Test Programs'.

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6. DESCRIPTION OF THE TESTS

6.1. RAM Test

The RAM test uses only CPU registers for program execution. Use of the RAM during the test is confined to writing test data into it and reading data from it. Every memory location is tested.

The test consists of five test phases after each of which the green 'OK' indicator is flashed if the test has been passed without error. If an error is found the program remains in the loop back state and the red 'ERROR' indicator is flashed; the following error message is repeatedly sent to the serial channels.

Channel	Data Transfer Rate	Error Code
1/A (to console)	19200	R<cr>
1/B (P1 connector)	300	<cr><lf>xxxx_yyyy
3/A (default to printer)	1200	<cr><lf>xxxx_yyyy

where

xxxx is the erroneously operating bits in hexadecimal format
yyyy are the error flags in hexadecimal format, see Table 2 below.

For instance, if the output is 0200 0080 the first word converted into bits gives bit 9 set, which stands for Data test 1 error. The second word corresponds to the binary value 0000/0000/1000/0000, which means that bit 7 is set = defective data line AD7 (DRAM circuit D42 on MPU13).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit number
0	0	0	0	0	0	0	0	*1*	0	0	0	0	0	0	0	Error in bin.
		0				**0**				**8**				**0**		**Error in hex**

Bit	Test	Test Data	Write	Read
0	Byte/Word R/W[3]	(3B23)	W[4]	W
1	Byte/Word R/W	(4A34)	W	LSB/MSB
2	Byte/Word R/W	(5945)	W	MSB/LSB
3	Byte/Word R/W	(6856)	MSB/LSB	W
4	Byte/Word R/W	(7767)	MSB/LSB	LSB/MSB
5	Byte/Word R/W	(8678)	MSB/LSB	MSB/LSB
6	Byte/Word R/W	(9589)	LSB/MSB	W
7	Byte/Word R/W	(A49A)	LSB/MSB	LSB/MSB

[3] R/W denotes Read and Write operation.

[4] Write and read with word operators.

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8	Byte/Word R/W	(B3AB)	LSB/MSB	MSB/LSB
9	Byte/Word R/W			
10	Byte/Word R/W			
11	Byte/Word R/W			
12	Byte/Word R/W			
13	Address test (forward addressing error)			
14	Address test (contents error)			
15	not in use			

Table 2 Error Flags in RAM Test

6.2. EPROM Test

The test reads the contents of the EPROMs and computes the checksum, which must have the correct value. If a program error is found, information about it is entered in the ERMAP.

6.3. 8087 Test

The 8087 test executes the following operations using real numbers and checks the result.

- addition of two numbers
- multiplication of two numbers
- division of two numbers.

The 'ERR' LED is turned on at the start of the test and off at the end. If the operation is never completed, the program remains in a permanent loop with the 'ERR' LED lit. The duration of test is very short which makes the flash of the LED during the test barely discernible.

6.4. Serial Channel Test (channels 0-7 and 8-15)

Internal (or, with test adapter, external) feedback is used to check the operation of status signals and error flags of selected serial channels when sending and receiving characters. A check is also made to ensure that characters are transferred without error from the transmitter to the receiver.

6.5. Program Storage Memory Test

In the program storage memory test the entire memory space of the program storage is read and the programmed circuits are tested by reading the circuit contents and comparing the result to the checksum programmed in the circuit. Simultaneously with reading the contents it is being checked that all data lines are both in 1 and 0 state during the test.

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6.6. EEPROM Test

The test is divided into two parts. The backed-up memory that is assumed to be installed in every case is tested together with the additional memory, if the latter is provided. The circuit size is either 8 kB or 32 kB. In the backed-up memory test, all memory locations are read first and all three memories are checked to verify for similar contents. If there is any discrepancy and such error can be corrected, then correction is carried out. On an average three corrections are allowed for each test pass over a long run. If there are more errors an error message is given. In the event that an error cannot be corrected an error message is given immediately.

After the read tests, a write test is made. Statistics of errors are updated in the EEPROM if no error which would prevent updating has occurred during the test pass. The additional memory test is made if additional memory has been installed and initialized. This test begins by checking the test data (read/write functions). The checksums of the data blocks are checked. In the event of an error, the error will be stored into the ERMAP.

Additional information on the EEPROM test result can be obtained by issuing the command D 5 (for DISPLAY 5) to output the EEPROM INFO table (see Chapter. 5.1).

6.7. Frequency Meter Test

Not implemented.

6.8. Calendar Clock Test

The test is carried out if the "clock set" bit (see TIME/ FLAG) has been set. The bit is controlled by the set time command so that when the time 0 is given, the bit is cleared. Otherwise the bit is set upon setting the clock.

The time read by the test from the calendar clock is stored in the EEPROM (LAST START-UP TIME); however, not when the clock is tested in mode C.

In addition to the clock logic, the clock test checks the time to ensure that it is realistic and that some time has elapsed from the previous test pass.

6.9. Run-time Test

The run-time test in back ground of the application program in case idle time available. The program tests the DRAM in 65 kB blocks one memory location at a time, proceeding through the entire memory. Also the EPROM check-sum is tested. If an error is found the 'ERROR' indicator of the MPU is lit and the ERMAP is updated with the error. The run time test can also be called from the monitor (see JOB commands).

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7. ERMAP

The ERMAP is a 16+16-byte table in which bits indicating faulty operation are stored by the tests. The bytes are listed in the table below together with the causes of the error bits. Only used Error Bytes and Bits are shown.

Error byte	Desription of Test and Error Bits
1	*CPU/8087 test*
	0 Error in addition test
	1 Error in multiplication test
	2 Error in division test
2	*RAM test*
	6 DRAM error (run-time test)
	7 DRAM error (run-time test)
3	*EPROM test*
	6 Checksum of EPROMs does not tally during self-test
	7 Checksum of EPROMs does not tally in run-time test
5	*Program Storage check-sum test*
	0 Memory circuit 1 (D44) check-sum error
	1 Memory circuit 2 (D40) check-sum error
	2 Memory circuit 3 (D30) check-sum error
	3 Memory circuit 4 (D23) check-sum error
	4 Memory circuit 5 (D15) check-sum error
	5 Memory circuit 6 (D10) check-sum error
6	*Program Storage test*
	0 Memory circuit 1 (D44) segment identification error
	1 Memory circuit 2 (D40) segment identification error
	2 Memory circuit 3 (D30) segment identification error
	3 Memory circuit 4 (D23) segment identification error
	4 Memory circuit 4 (D15) segment identification error
	5 Memory circuit 1 (D10) segment identification error
	6 Memory databus in permanent 0 state
	7 Memory databus in permanent 1 state
7, 8	*Serial Channel tests (7 = channels 0…7, 8 = channels 8…15)*
	0 Some RxRDY incorrectly at '1' state
	1 Some RxRDY incorrectly at '0' state
	2 Status error (BREAK received; frame, parity or overrun error)
	3 Incorrect character
	4 TxRDY is in '1' state right after two successive characters have been sent
	5 TxRDY is in '0' for too long time (should be in '1' state after first character being sent)
	6 TxRDY is in '0' for too long time (should be in '1' state after first character being sent)

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B *Calendar Clock test*
- 0 EEPROM read error (in clock module)
- 1 Real Time Clock (RTC) read error or no clock installed
- 2 Time not reasonable
- 3 Clock stopped or has run backwards after preceding test
- 4 EEPROM write error(in clock module)
- 7 No clock module provided on the card

D *EEPROM test for additional circuit D21*
- 0 Circuit identification error or no circuit installed
- 1 Uninitialized circuit
- 2 Write error
- 3 Test block data error (data 00 or FF_H)
- 4 Test block data error (data AA or 55_H)

E *EEPROM test for backed-up memory (serious errors)*
- 0 Addressing error in program
- 1 EEPROM test time out
- 2 Test data error
- 3 Irrecoverable read error in two or three circuits
- 4 Write error in two or three circuits
- 5 Write error in circuit 1[5]
- 6 Write error in circuit 2
- 7 Write error in circuit 3

F *Run-time test*

10 *EEPROM test*
- 0 Irrecoverable error in circuit 1[6]
- 1 Irrecoverable error in circuit 2
- 2 Irrecoverable error in circuit 3
- 3 More than one error has been corrected by read routine in long term in circuit 1
- 4 More than one error has been corrected by read routine in long term in circuit 2
- 5 More than one error has been corrected by read routine in long term in circuit 3
- 7 Uninitialised backed-up memory

---

5 In case error bit 4 is not present at the same time, the error of this type can be corrected by the read routine. The unit is still in operating condition but the circuit should be replaced as soon as possible. Applies also for circuits 2 and 3.

6 This is not a "soft" error. Corrupted data can be recovered by automatic error correction of the read routine. The unit is still in operating condition but the circuit should be replaced as soon as possible. Applies also to circuits 2 and 3.

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8. ADDITIONAL INFORMATION

8.1. EEPROM Info (D_5)

The output format is similar to ERMAP. However, meaning of the Bytes and Bits is different.

Byte	Description
00	Total errors counter (overflows)
01	Total errors counter (LSB)
02	Total errors counter (MSB)
03	Fatal error counter for circuit 1
04	Fatal error counter for circuit 2
05	Fatal error counter for circuit 3
06	Last fatal error address (MSB) for circuit 1
07	Last fatal error counter (LSB) for circuit 1
08	Last fatal error address (MSB) for circuit 2
09	Last fatal error address (LSB) for circuit 2
0A	Last fatal error address (MSB) for circuit 3
0B	Last fatal error address (LSB) for circuit 3
0C	Bits received in incorrect 0-state
0D	Bits received in incorrect l-state
0E	Bits received in incorrect state
0F	Circuit size of backed-up memory (51H=8 kB, 57H=32 kB)[7]
10	Recoverable error counter for circuit 1
11	Recoverable error counter for circuit 2
12	Recoverable error counter for circuit 3
13	Space left in additional circuit (MSB)
14	Space left in additional circuit (LSB)
15	Number of blocks in additional circuit (MSB)
16	Number of blocks in additional circuit (LSB)
17	Number of faulty blocks in additional circuit
18	Not in use
19	Not in use
1A	Not in use
18	Not in use
1C	Not in use
1D	EEPROM test pass counter (MSB)
1E	EEPROM test pass counter (LSB)
1F	Additional circuit flag (0: no additional circuit 1: 8 kB circuit, 7: 32 kB circuit

[7] If other than 51 or 57, EEPROMs are not initialized.

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8.2. Date and Time (D_6)

Byte	Description
00	Year
01	Month
02	Day
03	Hour
04	Minute
05	Second
06	Second/10
07	Control/day of week[8]
08	0FF
09	Year
0A	Month
0B	Day
0C	Hour
0D	Minute
0E	Second
0F	Flag[9]
10	Year
11	Month
12	Day
13	Hour
14	Minute
15	Second
16	Second/10
17	Control/leap year/day of week[10]
18	0: Clock module does not respond, 1: Clock mounted on card
19	Not in use
1A	Not in use
18	Not in use
1C	Not in use
1D	Not in use
1E	Not in use
1F	Not in use

---

8 See JOB E command for Time/Date setting

9 In binary format.
Use of bits: 7 6 5 4 3 2 1 0
0: If '0' clock not mounted on card
1: If '0' time has not been set
2: always '1'
4: If '1' time of the clock not reasonable
5: If '1' time of the clock in reading test less than in preceding test

10 See JOB E command for Time/Date setting

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8.3. EEPROM Write Error Codes

Bit	Description
0	Write error in circuit 1
1	Write error in circuit 2
2	Write error in circuit 3
3	Write error in three circuits, also bits 0, 1 and 2 are set
4	Write error in circuit 1
5	0
6	Address error (address >$7FFF_H$)
7	Write time-out (circuit indicated by bits 1, 2 and 3)

Table 3 EEPROM Write Error Codes

8.4. EEPROM Read Error Codes

Bit	Description
0	Circuit 1 has been corrected[11]
1	Circuit 2 has been corrected
2	Circuit 3 has been corrected
3	Correction of circuit not successful (refer to bits 1, 2, 3)
4	Irrecoverable error in more than one circuit
5	0
6	Addressing error (address > 7FFFH)
7	Write time-out during repair attempt

Table 4 EEPROM Read Error Codes

8.5. EEPROM Initialization Error Codes

If the EEPROM initialization fails, an error message and code XY_H is output on terminal display. The XY must be broken into binary value to find the set bits. If the error bit 3 is set, i.e. Y>7, refer to Table 4, otherwise Table 5.

[11] If only bit 1, 2 or 3 is present, data is OK after correction. If also bit 7 is present at the same time, bits 0, 1 and 2 indicate the circuit the contents of which were being corrected upon time-out. This applies to bits 1 and 2 as well.

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Bit	Description
0	Write error in circuit 1
1	Write error in circuit 2
2	Write error in circuit 3
3	0
4	Write error in circuit two circuits
5	Write error in three circuits
6	Address error (address >$7FFF_H$)
7	Write time-out (if only this bit is set presumably the circuit 4 is faulty)

Table 5 Initiliazation Errors of Backed-up EEPROM Circuits

If error bits 0, 1, 2, 4 and 5 appear simultaneously, the fault is related to circuit identification.

XY	Description
A8	Write error
28	Read error with test data FF
98	Write error
18	Read error with test data 00

Table 6 Initialization errors of Additional EEPROM circuit

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9. PARTS LIST

Reference	Part No	Description
Integrated circuits		
D8	10883	DS 1216
D9, D16	15859	SCC 2698 BC1N64
D11...D14	1045	74HC14
D18, D19, D26	10471	74HCT138
D20, D23	1350	74HC00
D21, D30, D38, D48	15863	X 28C256 D
D22	15914	74AC138
D24, D25	1048	74HC259
D27, D28	10494[12]	27512-3
D31, D32,D39, D40	12589	74ACT573
D34, D37, D47	15364	74HC574
D35	10473	74HCT245
D41...D44	15860	M514400-80Z
D45	15862	80C186-16
D49, D50	15866[12]	EPM 5032-2 or module MW45134
D51	15861	80C187-16
A4...A7	5850	TL 084 IJ
A9	1845	UA9638
A10	1844	UA9637
A11	15294	Max 692 CPA
Q1	10424	MTO-T1-S3
Q2	15865	MCO-1500B
Diodes		
V3	3085	1N 747 A
V6	6083	LD 52-1
V7	6080	LD 57-1
V8	6082	LD 56-1
Resistors		
R30, R31, R37, R40	10826	21R5
R38, R39	11358	110R
R29, R46	10830	1k00
R41	10721	332k
R6...R17	4052	GE V22ZA1

[12] When ordering, also version must be stated (label on chip).

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R18...R21	10409	GE V8ZA1
Resistor arrays		
RA21, RA22	10480	4 x 22R, 2 %, SIL 8
RA16	10001	4 x 100R, 2 %, SIL 8
RA23	10789	4 x 220R, 2 %, SIL 8
RA7...RA10	10408	4 x 470R, 2 %, SIL 8
RA24	0011	9 x 6k8, 2 %, SIL 10
RA2, RA11,RA13, RA14, RA17, RA19, RA20	0057	4 x 10k, 2 %, SIL 8
RA12, RA15,RA18	4633	9 x 10k, 2 %, SIL 10
Capacitors		
C30	4822	10n, 10%,100V, polycarbon
C4, C8, C23, C26, C29, C32...C40, C42	0170	470n, 20 %, 63 V ceramic
C16, C17	0685	10u, 20 %, 10 V, electrolytic tantalum
C18, C43	0610	22u, 20 %, 25 V, electrolytic tantalum
Others		
MW45134	MW45134	Replacement Module for D49

MW45134 parts:

Integrated circuits		
D1	25771	EPM7064S
Capacitors		
C1, C2, C3, C4	15621	100n, X7R, 0805
Resistors		
R1, R2, R3, R4	25263	1k0, 1%, 100ppm, 0603
Connectors		
X1, X2	25770	ASP-19064-02

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10. DIAGRAMS AND BOARD LAYOUTS

Main Processor MPU13 Block Diagram D.MP3211
Main Processor MPU13 Circuit Diagram E.MP3213
Main Processor MPU13 Components Layout E.MP2214

MW45134 Circuit Diagram MW45133
MW45134 Components Layout MW45134

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