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GPS PROCESSOR MWG201A/202A Unit Description

MWG-S203en-1.4
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VAISALA

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1. GENERAL

The GPS Processor MWG201A is a plug-in E1 size Eurocard unit. It is used to add GPS based wind finding capability to the sounding system. It contains a Control Processor, serial communication channels and signal channels to receive local GPS signal from local antenna and remote GPS signal from the radio receiver. The remote and local GPS signals are used to determine the movements of the radiosonde.

The Control Processor is a 16-bit microprocessor system with memories and math co-processor. The serial communication channels include six RS232 compatible asynchronous channels and an ARCNET type local area network.

The local signal receiver is a commercial GPS Navigation Unit, which is used for receiving satellite orbital data, synchronizing with GPS time, extracting the instantaneous vector of a mobile station and for receiving local GPS signals to be used in the differential wind calculation.

The remote signal channel consists of a frequency converter and a FSK signal demodulator. The frequency converter is used to convert the Vaisala-specific FSK frequencies to the standard BELL compatible frequencies.

The GPS Processor MWG202A does not contain the commercial Navigation Unit. It is intended to be used in multi-channel systems where one MWG201A provides local GPS data to several adjacent MWG202A units.

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2. CONTROL PROCESSOR

2.1. CPU

The MWG201A/202A contains an Intel 80C186EB type microprocessor with Intel 80C187 math co-processor and FLASH memory, which allows to load and modify applications programs via communication channels.

The central processor unit (CPU) runs at a speed of 32 MHz (actual processor clock cycle is 62.5 ns). Data (AD00-AD15) lines connect directly to memories and peripheral circuits. The address lines A00-A19 come through latches D11, D16 and D24. The read (RD#) and write (WR#) and chip select signals are used to control I/O operations to/from memories and peripheral circuits.

2.2. Program Memory

The program memory is 256 k x 16 bit FLASH type circuit. The memory chip contains the following internal blocks:

- Command Register
- Status Register
- In-circuit State Machine
- One 16-kbyte Boot Block
- Two 8-kbyte Parameter Blocks
- One 96-kbyte and three 128-kbyte Main Blocks

This type of memory makes it possible to update the program on board without removing the memory chip. An on-chip State Machine controls block erase and byte programming. All functions which are altering the memory contents (program, erase, status) are accessed via the Command Register and verified through the Status Register. WR# control writes to the control register and array blocks. High voltage (+12 V) at pin 17 (Vpp) enables erasure and programming of the device.

Boot Block contains the most important start-up routines. It is write-protected, i.e., the Vpp voltage does not enable its contents to be changed. Its contents can be modified only when the Vpp voltage is connected to the pin 14 by setting a Jumper to the connector X3.

Normally memory functions as Read-Only Memory. The first code byte, after reset, is fetched from memory location 7FFF0 (hex) in a Boot Block. The Upper Chip Select (UCS#) selects the device from pin 32, and the RD# pulse in pin 34 transfers the data to the processor by activating the output data buffers of the memory chip.

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2.3. Programming Power Supply

The circuit A1 is an adjustable voltage regulator for erasure and programming of the Flash Memory. The circuit is a serial type regulator with an internal 1.23 V reference and an error amplifier. Also regulator have a Shut Down input (pin 3) to switch the output voltage Vpp on and off. If voltage at Shut Down pin comes more positive than +2 V, output of the regulator drops to 0V.

The input voltage (+15 V) of the regulator comes to pin 8. Voltage divider R1 and R2 in the feedback loop sets the output voltage to +12 V. Capacitor C3 is needed for regulator stability and it also limits the possible voltage overshoot at switch on to a safe level.

Processor-controlled programming signal (PGM) from D19 is used to control the Shut Down input of the regulator. When PGM is in low state the transistor V5 is not conducting and the Shut Down pin is pulled high and thus the Vpp is switched off. When PGM is in high state the V2 is conducting and the regulator is switched on.

2.4. Random Access Memory

This memory is for temporary (non-volatile) storage of data and code. The memory consist of two 524 k x 8 bit CMOS Static RAM type circuits, D10 and D23.

The processor selects the Data Memory by driving the Lower Chip Select (LCS#) pin low. LCS# is active whenever the address of a memory bus cycle is within programmed address range. The active low RD# (Read) and WR# (Write) control signals determine the direction of data flow.

The RD# pulse activates the output buffers of the memory and thus makes the data available to the bus.

The WR# pulse with the BHE# and A00 signals are used to generate the byte write pulses WRL# and WRH# , which write the data from the databus to the addressed location of the memory. Low byte is written if A00=0 and BHE#=1, high byte is written when A00=1 and BHE#=0. The whole 16-bit word is written if A00=0 and BHE#=0.

2.5. Device Register

Shift register D14 and D15 are used to read the device, slot and rack codes of the MWG201A/202A. Upon start-up the code values are loaded into shift registers with CS6# and are shifted out in serial format to pin P2.4 of the microprocessor with signal CS7#. The code consist of device code (at D14 fixed to 0FH), boot code (at pins 11 and 12 of D15 fixed to 10B), slot code and rack code. The slot and rack codes depend on connections at external connector and are used to define the ARCNET address of the MWG201A/202A.

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2.6. EEPROM Memory

The EEPROM (Electrically Erasable Programmable Read Only Memory) circuit D18 (64 x 16 bits) is a non-volatile data storage for saving the serial number and possible other unit-specific information. The control signals and data in serial format are generated at D19. The output data (PMD) is connected to the Control Processor.

2.7. Reset Circuit

The circuit A2 controls the reset signals (RES and RES#), which are forced to the active state if any of the following conditions appear:

- +5 V operating voltage falls below +4.65 V
- external reset line MRES# is in 0-state

The reset output signals are held active typically 200 ms after the reset condition is disappeared.

2.8. Test Latch and the LED Lamps

Test latch (D19) is an 8-bit addressable latch, which is mainly for controlling the LED (Light Emitting Diode) lamps and the EEPROM memory. Address lines A1-A3 select the individual latch and address line A0 holds the input data, which is written to the addressed latch when input D19/14 is at low level.

System reset signal RES# sets all outputs low, which puts the error lamp ER on and also the OK lamp is held on through D17C. After reset is released OK lamp goes off but ER remains on until the Control Processor sets it off.

During system test phase after power-up the OK/ER lamps are used to output pass/fail information of the individual test routines.

Later in the system operation the OK and ER lamps are indicating the status of the system and the IO lamp is normally used to indicate activity on external communication lines.

2.9. Programmable Logic Device (PLD)

D2 is an EPLD (Erasable Programmable Logic Device) type PLD circuit, which is programmed to perform application specific logic functions. The circuit has four dedicated input pins and 32 I/O pins, which can be programmed as inputs or outputs.

Dedicated input pins are used for the following signals:

Signal	Pin	Description
40 MHz	43	40 MHz clock signal
32 MHzI	1	32 MHz clock signal

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22.1184 MHz	44	22.1184 MHz clock signal
CLK0	2	16 MHz processor clock output for timing reference

The following I/O pins are used as inputs:

Signal	Pin	Description
PWR2	4	Operation control, 0=full operation, 1=stand by
ARCRX	5	Arcnet received data
ARCSP	6	Control input for arcnet data filter 0=slow speed, 1=high speed
CS1#	7	Chip select 1, low level active
A5	8	Address5
A6	9	Address6
A7	11	Address7
RD#	12	Read, low level active
WR#	13	Write, low level active
ALE	14	Address latch enable

The following output signals are generated by the logic of the PLD:

Signal	Pin	Description
20 MHz	24	20 MHz clock, divided from 40 MHz input
32 MHzO	26	32 MHz clock, buffered from 32 MHz input
11.0592 MHz	27	11.0592 MHz clock, 22.1184 MHz input divided by 2
3.6864 MHz	28	3.6864 MHz clock, 22.1184 MHz input divided by 6
ARCRXIN	29	Arcnet received data, filtered from ARCRX input
MCS#	31	Modem chip select, driven continuously as active low
WLEN#	32	Modem address/data latch output enable, set to inactive high state by the falling edge of CS1#, set to active low state when WR# =0
RLEN#	33	Output enable of D22, active low when MRD# =0
ADRD#	34	A/D read, active low when CS1#=0, RD#=0, A05=0, A06=0 and A07=0
MRD#	36	Modem read, active low when CS1#=0, RD#=0, A05=1, A06=0 and A07=0
ADWR#	38	A/D write, active low when CS1#=0, WR#=0, A05=0, A06=0 and A07=0
MWR#	38	Modem write, active low when CS1#=0, WR#=0, A05=1, A06=0 and A07=0
PWWR#	39	Write to latch, active low when CS1#=0, WR#=0, A05=0, A06=1 and A07=0
MLD	40	Modem address/data latch enable, active high when CS1#=0, WR#=0 and A05=1, A06=0, A07=0 or A05=0, A06=1, A07=1
MALE	41	Modem ALE, active high when CS1#=0, WR#=0, A05=1, A06=1 and A07=1

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3. FM SIGNAL CHANNEL

3.1. General

The Vaisala GPS radiosonde transmits the detected GPS signals in digital format. The modulation type is FSK (Frequency Shift Keying) and the bit rate in 1200 bits/s. The FSK modulation can have two formats:

- BELL 202 standard, where the FSK frequencies are 1200/2200 Hz
- Vaisala specific FSK, where the FSK frequencies are 3200/4200 Hz

In the MWG201A/202A the Vaisala-specific frequencies are converted to the BELL 202 frequencies to be compatible with the standard Modem chip, which is used for data demodulation.

The frequency conversion is performed by generating a difference frequency of the Vaisala FSK frequencies and the 2000 Hz local oscillator frequency. Before conversion the FM signal is bandpass filtered to avoid producing unwanted frequency components.

3.2. FM Input Selector

The FM input selector A14 has the following input channels:

- FMI1, internal channel 1 from system connector pin a3
- FMI2, internal channel 2 from system connector pin c20
- FME, external channel from front panel EXT FM IN connector
- FREQ1, test frequency from D3, used for testing purposes.

Channels FMI1 and FMI2 are AC-coupled through C64 and C63.

Channel FME is connected through bandpass RC-filter and a differential amplifier A16. The filter passband (-3 dB) is from 700 to 5700 Hz and the channel gain at center frequency 2 kHz is -6 dB.

The FM input channel is selected by control signals EA0-EA2 from D8.

The output of the selector is connected to the bandpass filter and also directly to the FSK selector (A13). The bandpass filter connection is used for Vaisala FSK frequencies and the direct FSK selector connection is used for BELL 202 FSK.

3.3. Bandpass Filter

The filter is an active 6th-order RC-filter, which is built by cascading three 2nd-order filter sections. The operational amplifier A15 is used as an active filter element. The filter passband (-3 dB) is from 3 kHz to 4.5 kHz and the

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attenuation at 1 kHz and at 10 kHz is more than 35 dB. The propagation time delay differences in the passband are less than 500 microseconds. The filter gain at center frequency is approximately 17 dB.

3.4. Frequency Conversion

The frequency converter for generating the difference frequency of the 3200/4200 Hz FSK and 2000 Hz oscillator frequencies is built by using the analog signal multiplier circuit A12. The output W of the multiplier is according to the formula:

$$W = (X * Y) / 10 + Z$$

The FM signal from the bandpass filter (AFM2) is connected through the simple RC-filter C36 and R37 to the x-input of the multiplier.

The other multiplier input is a 2 kHz signal FFREQ from the timer of the processor D3. This square wave signal is first lowpass filtered to remove the odd harmonics.

The lowpass filter is a 8th-order, switched capacitor type filter chip A17. FFREQ is first attenuated and pre-filtered by R26, R30 and C67 to prevent aliasing, then AC-coupled by C58, biased to +2.5 V DC-level and connected to the input of the filter A17. The corner frequency of the filter is the clock frequency divided by 50 and is set to 2 kHz by the 102.4 kHz clock frequency FCLK from the timer of the DUART1 D8. The 2 kHz output signal is filtered by R54, C41 to remove the clock ripple and then AC-connected to the y-input of the multiplier A12.

The multiplier output contains the difference frequency components of the input frequencies (4200/3200 Hz and 2000 Hz) and thus the Vaisala specific FSK frequencies 4200/3200 Hz are converted to the standard BELL 202 FSK frequencies 2200/1200 Hz. Also the sum frequencies (6200/5200 Hz) are generated but these are rejected in the Modem filters. The multiplier output is connected to the FSK selector A13.

The clean analog operating voltages +5VA and +2.5VA required for the filter A17 are supplied by the linear voltage regulator A8. The regulator input voltage is +15V and the feedback loop with internal reference sets the output voltage to +5 V. The Capacitor C42 is needed for regulator stability. The +2.5VA is produced from +5VA by voltage divider R43/R39.

3.5. FSK Selector

The FSK selector is used to select standard BELL 202 FSK frequencies directly from input selector or converted FSK frequencies from multiplier A12 to be connected further via gain control block to the FSK demodulator D9.

The channel is selected by control signals FA0-FA2 from DUART D8. The input signals AFM2 and FREQ1 are used for testing purposes.

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3.6. Gain Control

The FSK signal level is controlled by the Digital to Analog Converter (DAC) A11, which is used to set the gain of the operational amplifier A10/7.

The FSK Signal is fed via the lowpass filter (R48, C33) and buffer amplifier A10/1 to DAC's Feed Back input (RFB) from which it is internally, trough fixed resistor, connected to IOUT pin. The Amplifier output A10/7 is connected to DAC's reference input (VREF) from where it is internally, through DAC's adjustable ladder resistor network, connected to the same IOUT pin. Thus the gain of the amplifier can be controlled by the ladder resistor network, which is acting as the variable resistor in the negative feed back loop of the amplifier.

The gain equation of the amplifier is:

Vout = - (4096 / DW) x Vin; where DW = DAC's control word (1...4095)

DAC's output control word is loaded serially by using DADIN as data input, DACLK as clock input and DALD# as load input. First the 12 data bits are clocked into DAC's shift register and then DALD# is activated to load the DAC's actual output data register. As an example a load sequence for DW=810 (hex) is shown below.

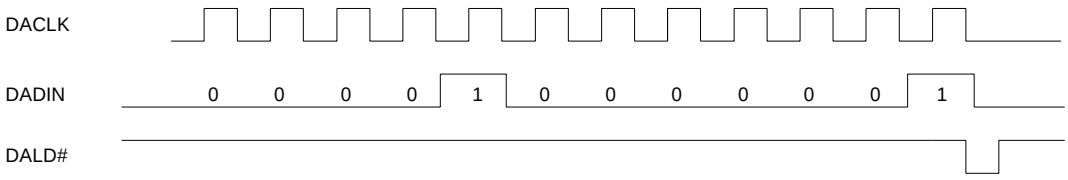


Figure 1 A control sequence for control word 819 (hex)

The output FSK signal from amplifier is fed through scaling resistors R9, R10 to the Modem for FSK demodulation. For software based gain control the FSK signal is rectified and fed through scaling resistors R25, R24 to the A/D converter A7.

3.7. Modem

The single chip Modem (D9) provides all the functions of a Bell 202 compatible Modem. The chip includes high and low band filters and the automatic gain control maintains a signal level constant to the demodulator. The FSK Demodulator involves detecting the received frequencies 1200 Hz (mark corresponding to a binary 1) and 2200 Hz (space corresponding to a binary 0) and decoding them into the binary values 1 and 0. The received data output signal is connected to the serial line CH5A.

The bus interface timing of the Modem is not directly compatible with the requirements of the high speed control processor and thus the Modem and the Modem data bus are controlled by the signals MCS#, MRD#, MWR#, MALE, MLD, WLEN# and RLEN#, which are generated by the PLD chip D2 (see section PLD for detailed signal descriptions).

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The processor data write cycle to the Modem is performed as follows:

1. The processor performs a write cycle to address CS1+6. This loads the modem address from processor databus to the latch D25 by activating the signal MLD.
2. The processor performs a write cycle to address CS1+7. This loads the modem address from the latch D25 to the modem D9 by activating the signals WLEN# and MALE. WLEN# activates the outputs of the latch and MALE loads the address to the modem.
3. The processor performs a write cycle to address CS1+1. This loads the data from processor bus to the modem D9 by activating the signals MLD, WLEN# and MWR#. Signals MLD and WLEN# drive the data to the modem bus and MWR# writes the data to the modem.

The processor data read cycle from the Modem is performed as follows:

1. The address is latched as in the case of the write cycle.
2. The address is loaded as in the case of the write cycle.
3. The processor performs a read cycle to address CS1+1. This reads the data from the modem by activating signal MRD# and drives the data further to the processor bus by activating the signal RLEN#.

The interrupt request MINT# of the modem is connected to the input of DUART D4.

3.8. A/D Converter

A/D converter A7 is a software configurable 8-bit, 8-channel device with simultaneous track-and-hold, reference and 8 x 8 bit internal RAM.

The configuration data of the input multiplexer is loaded on the rising edge of ADWR# pulse, through bi-directional data pins. During power up tests the multiplexer is configured as multi channel, bipolar, single-ended inputs and later in the operation a single channel configuration is used. When updating the configuration register the INH-bit is written high for all except the last ADWR# to prevent the starting of the conversion until the multiplexer is set.

On the falling edge of ADWR#, all active input channels are sampled simultaneously. The interrupt pin, INT1#, goes low at the beginning of the conversion, and channels are converted sequentially starting with the lowest selected channel. When INT1# goes high, the conversion is completed. The results are then stored in the internal RAM and the processor reads the RAM contents with consecutive ADRD# pulses, starting from the data of the lowest channel. In normal sonding operation (after testing phase) only the input channel 1 (ADFSK) is configured as active and thus a single ADRD# pulse is used to read the result.

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The conversion time for one channel is 4.9 us with the 3.6864 MHz external clock signal.

The 2.5V reference output voltage (REFO) is externally connected to the reference input REFI. With this reference the voltage range of the converter is 0 ... 2.5V.

The input signals of the A/D converter are according to the table 3-1. External scaling resistors are used to adjust the signal levels suitable for the converter input range. The rectified FSK signal is for software based gain control and the other input signals are for testing purposes.

Signal	**Channel**	**Description**
ADFSK	1	rectified FSK signal
ADVPP	2	programming voltage for the FLASH ROM
ADBV	3	supply voltage for the GPS module memory backup
ADVM	4	GPS Module supply voltage
ADVA	5	+2.5 V analog supply voltage
ADV	6	+/-15 V operating voltages
ADT	7	optional external voltage input
GND	8	ground

Table 1 The input signals of the A/D converter

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4. GPS MODULE

The GPS Module is an independent GPS receiver for local channel L1-band GPS signals. The Module is installed on the Main Board of the MWG201A. The GPS Processor MWG202A does not contain the GPS Module.

The local signal is connected from Local GPS Antenna to the Module via the front panel Local Ant. connector (X6) by using coaxial cabling. The current limited supply voltage +5 V is connected via the Module to the Low-Noise-Amplifier of the Local Antenna. The RF signal and the supply voltage share the same path.

The GPS Module has two serial communication channels (A and B). The channel A is used for communication with the Control Processor and channel B can be used to connect external data sources directly to the Module. The hand-shake signals RTS (request to send) and CTS (clear to send) are provided for channel B in the front panel connector P1.

The reset input is provided for full initialization of the Module. The input signal is MANRES# and it is controlled by signal MRES# from the processor D3.

The time reference output signal one-pulse-per-second (1PPS) is provided by the Module. The signal has one second period and its rising edge is synchronized to the GPS time within an accuracy of a microsecond. The duration of the high state of the pulse is from 1 to 2 milliseconds. The 1PPS signal is connected via DUART 1 to the processor D3 and in addition it is available at the front panel connector P1 and at the system connector X1.

The Module has a two-color LED lamp, where the red flashes at approximately every three seconds are used to indicate that the Module is operating and the green flashes between the red ones are indicating the number of the Satellites in track.

The Module uses +5V operating voltage (+VM) and in addition the back-up power +BV is provided for the non-volatile memory of the Module. The back-up power is supplied by a large capacitor C10, which is charged to approximately +4.2V from +5V operating voltage or from optional stand-by voltage STDC via the diodes V32 and V29 or V30. The resistors R42 and R44 are for current limiting and the zener diode V31 is clamping the maximum capacitor voltage to approximately +4.2V .

The typical back-up time with fully charged capacitor is 48 hours and the time can be made unlimited by using optional STDC supply.

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5. I/O OPERATIONS

5.1. Power Control

The MWG201A/202A has the following operating modes:

1. Normal operation
2. Stand-by with GPS Module power off
3. Power down with GPS Module off and system clock signals disabled

The Control Processor is selecting the operating mode by using Control Register D12 outputs PWR1 and PWR2. GPS Module power is switched on/off by PWR1 and the system clocks are disabled by PWR2.

PWR1 (output D12/4) is inverted by D20E and connected to the Gates of dual P-Channel MOSFET (Metal-Oxide Semiconductor Field Effect Transistors) Transistors. With PWR1=0 the Gate-to-Source voltage (VGS) is thus 0 V and the V33 is off. With PWR1=1 the VGS= -5 V and V33 is on. The switching speed is decreased by connecting the control signal through R58 and C31.

PWR2 is connected to the input pin 4 of the EPLD D2. Output clock signals from EPLD are enabled when PWR2=0 and disabled when PWR2=1. If output clocks are disabled the Unit remains on power down state until reset is activated. The power down mode is for possible future use.

After power-up or system reset both control signals are low and thus clock signals are enabled and GPS Module power is off.

5.2. ARCNET Interface

Arcnet Controller, D5 contains an internal microsequencer which performs all of the control operations necessary to carry out the Arcnet token passing protocol and network configuration.

The processor transmits data by loading the data packed along with its destination node number into the RAM buffer of the Controller and by issuing a command to enable the transmitter. First, the Controller waits for a token, then it sends an enquiry to the destination node. If the node is free to receive, it responds with an acknowledgment and the Controller performs the transmit sequence. If the transmit sequence is completed successfully, the receiving node sends another acknowledgment to the transmitter and alerts its control processor by interrupt signal. The processor then reads the received data from the RAM buffer of the Controller.

Timing signal (20 MHz) to D5 comes from oscillator Z1 through D2 where the oscillator frequency is divided by 2. Controller chip is selected with the CS0# line of the processor and its registers are selected for processor access with address lines A1, A2 and A3. The internal 2-kbyte buffer memory are accessed indirectly through these registers. Processor RD# and WR# pulses determine the data direction on the bus. Interrupt signal is inverted and connected to the INT0 input of the processor.

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The controller is connected to the network through the bi-directional differential Line Transceiver D26. The line is protected against voltage transients by bi-directional transient suppressors.

In the receive mode the driver section of the transceiver is disabled by the 1-state of the controller TXEN output, which is inverted in connection to the transceiver pin 3. The receiver section of the transceiver is permanently enabled and the received data ARCRX is connected through D2 to the controller RXIN input. The D2 contains a programmable data filter, which is used to filter out the short transient states from the incoming serial data. The filter length is approximately 400 ns in slow speed mode (ARCSP is the low state) and 50 ns in high speed mode (ARCSP is the high state).

During the transmit sequence, the controller enables the transmitter by driving pin 3 high and the inverted transmit data from output pin P1 is driven to the line by the transmitter.

5.3. Serial Channels

The MWG201A/202A has six serial channels for external and internal serial communication. All external channels have RS232 compatible line drivers and receivers and protected against voltage transients.

Channels 1 and 2 are provided by the processor D3. Both channels are supported by the internal programmable baud rate generators which are, in the asynchronous mode, supplying an 8 x baud clock. Channel 1 has internal connection to the interrupt controller and channel 2 is using external connection to the interrupt input INT4.

Channel 1 is the main system channel and is connected to the system connector pins a25 (TXD1) and a26 (RXD1).

Channel 2 is the second system channel and is connected to the system connector pins c25 (TXD2) and c26 (RXD2).

Channels 3 and 4 are provided by the DUART 1 (Dual Universal Asynchronous Transmitter/Receiver) D8. External 3.6864 MHz clock is used to get the standard baud rates for the channels. The D8 is selected by CS2# and controlled by signals WR#, RD# and A01-A04. The INT2# signal is used to interrupt the processor.

The channel 3 is used for communication between the Control Processor and the GPS Module (channel A). The data from the processor (TD3) is connected through A9/8 to the GPS Module. The data output from the GPS Module (RXD3) through resistor R68 (signal TRXD3) has two connections: connection to the DUART 1 input signal RD3 through receiver gate D21E and connection to the system connector pin X1/b14. The parallel MWG202A units in multi-channel systems are using the connection to the system connector as data input to receive the local GPS data from the master MWG201A Processor.

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The serial channel 4 is divided into four branches (CH4A, CH4B, CH4C and CH4D). The other end of each branch is connected to the channel multiplexer (A4,A5) and the opposite ends have the following connections:

- CH4A is connected to the B channel of the GPS Module
- CH4B is connected to the front panel connector P1 and to the system connector
- CH4C is channel B of DUART 1
- CH4D is connected to the system connector.

The channel multiplexer (A4, A5) is controlled by the DUART 2 parallel outputs (RA00, RA01, SA00, SA01) and can be used to make any connection between branches.

Channels 5 and 6 are provided by the DUART 2 (D4). External 3.6864 MHz clock is used to get the standard baud rates for the channels. The D4 is selected by CS3# and controlled by signals WR#, RD# and A01-A04. The INT3# signal is used to interrupt the processor.

Channel 5 is connected to channel switch A3, which is controlled by the DUART 2 outputs (TA00...02) and can be used to make the following connections:

1. Switches 1 and 2 closed. Modem data (TD5A) is connected to the DUART input (RD5B) and to the system connector (TXD5C).
2. Switches 3 and 4 closed. DUART input and output are connected to the system connector.

Channel 6 input and output (RD6, TD6) are connected to the system connector (signals RXD6, TXD6) for use as a general purpose serial communication.

5.4. Parallel I/O

Input signal IP1 and outputs OP0, OP1 are for testing purposes.

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6. USE OF THE TEST PROGRAM

6.1. MWG201A/202A 80C186 Diagnostics

6.1.1. User Interface

LED indicators function as follows during the Power Up Test (Self Test) that is carried out automatically after power-up or Reset.

1. On Reset the OK and ERR LEDs are lit.

2. When Reset ends the OK LED will go out.

3. The BOOT program controls the LEDs until all LEDs are lit indicating exit from the BOOT program.

4. All the LEDs are turned off to indicate that CPU register test starts.

5. When the CPU register test is passed without errors the OK LED is flashed. If the CPU register test detects an error, the ERR LED will be lit and the CPU executes HLT instruction whereby program execution will be stopped with the HLT command (Halt).

6. The RAM test is carried out next. The test consists of the following subtests:

   - 5555 hex and AAAA hex data test
   - FFFF hex data test
   - RAM address test
   - 0000 data test

   The OK-LED is flashed after each subtest if no errors are found. If an error is found the ERR LED is lit and program execution halted by HLT (Halt) command (CPU executes HLT instruction). However, if the test input from pin a24 is 0, the program execution will continue and result in an attempt to start the test monitor.

7. Both OK and IO LEDs will be lit when RAM tests are passed without errors.

8. All LEDs are switched off when the main diagnostics function startup and initialization is completed.

9. After each subtest the OK LED is flashed, if no errors were found and the ERR LED is flashed, if errors were found. The subtest returning an error can be identified by counting the flashes after the start indication (flash of both OK and IO as described above in 7 and 8). This is useful in case the serial channel does not work.

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The list and sequence of tests to be performed depend on the test mode used. The tests in different modes are presented in paragraph 6.1.3.16 Z Change Monitor Mode.

10. End of Power Up Test with no errors is indicated with flashing the OK LED rapidly ten times. If errors were detected, the ERR LED will be lit and it stays lit.

6.1.2. Test Monitor

The test monitor is a program that allows monitoring and controlling the operation of the test program. The test monitor is automatically started after the RAM test, if the test input pin a24 is connected to the ground or it can be started from the application program with the command *.

The test monitor is controlled from a terminal (RS232/9600bd) connected to serial channel 1 (RXD1 pin a26, TXD1 pin a25).

After starting up the monitor program asks for the test mode to be used. The selected mode determines which tests will be executed with command M (refer to the test list given in connection with command Z).

The commands are entered from the terminal in format

X P1 P2···P10<Enter>

where

X	is the command (refer to the list of commands)
P1-P10	are control parameters for the command. Each parameter consist of 1-4 hexadecimal characters, i.e. 0…9 or A…F (only upper case characters are accepted).

Help commands can have different format, e.g. HD<Enter> (HD is help for display command) .

The command and parameters are separated with a <space> .

The command is rejected, if a parameter has more than 4 characters or characters other than the 0...9 or A...F are used.

Incorrect character entries can be corrected with the <DEL> key.

The commands are upper case characters except command k (Write Word To The I/O Port) and command r (Read Word From The I/O Port).

The test monitor responds with the text "Unknown Command" to any unidentified command input.

The test monitor responds with a question mark "?" and rejects the command if any key other than the space bar is pressed after the command character (exceptions to that are the help commands where the other command character is keyed in right after the "H").

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When the test monitor is running in continuous mode operation (entered with command C) and the last command is automatically called repeatedly, the command mode can be restored by pressing the space bar. The command mode is restored only when the current test round is completed.

The command C n<Enter> repeats n times the last entered command with its parameters.

The output (started with command D) can be interrupted by pressing CTRL-S. To resume output press CTRL-Q. To end the output press <space>.

The executed commands (10 last commands) together with the related parameters are saved in Command History - a list from which they can be repeated or edited as required. With command S it is possible to switch the save commands option on or off. The default setting is to have the commands saved into the Command History (S 1<Enter> saving on (default); S 0<Enter> saving off).

For editing a command, use the following keys:

<	move to the left on the command line
>	move to the right on the command line
+	toggles editing mode between insert/overwrite
DEL	deletes characters from the left side of the cursor
CR <Enter>	carries out the command

6.1.3. Commands

The following commands are accepted (to output the list on the terminal, give the command H for help):

B Jump to Boot Program or B 1 Restart Test Monitor
C Execute Previous Command N-times
D Display
G Execute Command From The Command History
E Identification info
H Help
J Job
K Write Byte To I/O Port
k Write Word To I/O Port
L Display Command History With Parameters
M Multitest
P Program Version
Q Restart Card
R Read Byte From I/O Port
r Read Word From I/O Port
S Enable/Disable Command Saving Into The Command History
V Test Monitor Version
W Set Identification Info
Z Change Monitor Mode

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The help commands are as follows:

HD Help for the Display command
HJ Help for the Job command
HM Help for the Multitest command

6.1.3.1. B Jump to Boot Program or B 1 Restart Test Monitor

Starts the Boot Program, which remains waiting for the program to be loaded from the serial channel or ARCNET. The command B 1<enter> restarts the test monitor.

6.1.3.2. C Execute Previous Command N times

Command C carries out the previous command N times, e.g. the command C 1 carries out the previous command once more. In case N is 0, i.e. the command is entered as C<Enter> or C 0<Enter>, the previous command will be repeated until space bar is pressed which returns the test monitor to the command mode.

6.1.3.3. D Display

Displays test results and memory contents as follows:

D 0 S	S=0 Displays Ermap in hexadecimal format S<>0 Displays Ermap in binary format
D 1 S	S=0 Displays the cumulative Ermap in hexadecimal format S<>0 Displays the cumulative Ermap in binary format
D 2 S O L T	Displays the memory contents as follows: S = Segment address 0-F O = Offset address 0-FFFF L = Length of output 1-FFFF T = Output format (Data Type) 0-4 0 = Byte output in hexadecimal format 1 = Word output in hexadecimal format 2 = Double Word output in hexadecimal format 3 = Byte output in hexadecimal format without formatting 4 = Byte output in binary format
D 3 A L T	Displays test results stored by the tests from the test result table as follows: A = Address in test result table 0-1FF L = Length of output 1-200 T = Output format (Data Type) 0-4 See above for details on T
D 4	Displays Peripheral Control Block (PCB) registers of the CPU

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D 5	Displays measurement results stored by the tests
D 6 S	Displays the measurement results of the selected test Parameter S is used to specify the required output as follows: 0= All values measured will be displayed 5 = 6 = DUART1 test 7 = DUART2 test 8 = Voltage test 9 = Test of adjustable amplifier (D/A converter) 10 = Band pass filter test 11 = Low pass filter test 12 = Fsk signal path test 13 = Ashtech module test 14 = Modem test 20 = I/O signal test

6.1.3.4. E Identification Info (Display / Save)

E	Displays the identification information of the card - serial number of the unit - revision number of the unit HW - eventual license number related to the device If the search of the identification information does not succeed, the display will show 'ERROR XX' where 'xx' is the contents of Ermap memory allocated to EEPROM tests. In case the information to be displayed is not installed in the system, the text 'Not installed' will be displayed.

6.1.3.5. G Execute Command From The Command History

Command G retrieves a command saved in the Command History along with its parameters for editing or execution. The first parameter is used for selecting the desired command from the Command History. The command L<Enter> outputs the entire contents of the Command History.

6.1.3.6. H Help

Command H outputs a list of commands or the help for a specified command.

6.1.3.7. J JOB

Command J is used to carry out the following tasks:

J	Clears Ermap and cumulative Ermap
J 1 address (0-FFFF)	Reads byte from memory
J 2 address (0-FFFF) data	Writes data (byte) to memory, reads it and outputs byte from the specified address

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J 3 SegmentAddr (0-F)	Changes segment address for commands J 1 and J 2
J 4 address (0-FF)	Reads word from the Peripheral Control Block of the CPU
J 5 address (0-FF) data	Writes word to the Peripheral Control Block of the CPU Note: This command may interfere with the program execution if written carelessly (e.g. chip selects)
J 6 S1 S2	Activates EEPROM commands S1 = password 1 S2 = password 2 Note The command is valid only for one J command except for commands J 9 and J 10.
J 7	Displays the contents of EEPROM within the range 0-31Hex. Operates only once after command J 6
J 7 63	Displays the contents of the whole EEPROM. Operates only once after command J 6
J 8 S3 Y	Checking and initializing EEPROM S3 = password 3 If Y = 313 the EEPROM commands need not be activated again (command J 6)
J 8 S4 S5	Erases EEPROM memory S4 = password 4 S5 = password 5
J 8 S4 S6 data	Writes the whole EEPROM full with specified data (word) S4 = password 4 S6 = password 6
J 9 address(0-3F)	Displays memory location of EEPROM (word). If EEPROM commands have not been activated, 0-31Hex will be accepted as address
J 10 address(0-3F) data	Writes to EEPROM memory location (word). If EEPROM commands have not been activated, 0-31Hex will be accepted as address: The followíng is displayed after the command: XXXX =>YYYY/ S where XXXX=contents of memory location before writing YYYY =contents of memory location after writing S = OK when writing ok = ERR 01 when writing not completed
J 11	Displays the contents of device code register in the following format: DeviceCode=XX BootCode=X SlotCode=DD RackCode=X X = hexadecimal number D = decimal number

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J 12 0	Displays time in format: h=hours m=minutes s=seconds ms=milliseconds
J 12 1	Starts the timer (clock) and displays time
J 12 2	Stops the timer (clock) and displays time
J 13	
J 14 CH N S	Outputs voltage test carried out with A/D converter at the required channel. Control parameters: CH = channel to be measured (0-7) N = number of measurements to be carried out (the sample intervals are not regular) S = 0 Outputs the mean value of measurements S = 1 Outputs the maximum value measured S = 2 outputs the minimum value measured S = 3 Outputs the difference between maximum and minimum values (amplitude)
J 15 Mux Ch	Sets Mux channel Ch to to multiplexer
J 16 M1 M2	Sets multiplexers 1 and 2. If parameter > 7, the state of the corresponding multiplexer will not be changed. M1= Channel of Multiplexer 1. M2= Channel of Multiplexer 2.
J 17 VAL	Sets D/A-converter (adjustable amplifier). Parameter VAL (0...FFF) is used to control amplification so that value 0 sets maximum amplification.
J 18 CTRU CTRL	Starts DUART1 timer. CTRU = more significant byte of the timer CTRL = less significant byte of the timer. If both parameters are zeros, the timers are set with default value generating the frequency of 102.4KHz
J 19 CNTR	Starts CPU timer 0. Frequency = 2 000 000/$CNTR_H$ If CNTR is zero, the timer will be stopped.
J 20 CNTR	Starts CPU timer 1. Frequency = 2 000 000/$CNTR_H$ If CNTR is zero, the timer will be stopped.
J 21	Sets test frequencies to CPU timer1 (ffreq=2kHz) and DUART1 timer (test signal 102.4 kHz).
J 22 MASK DIR	Sets power-save controls. Control parameters: MASK= masks the function (removes) from the command bit by bit as follows: bit 0 = 1 power supply for the receiver module is not disconnected bit 4 = 1 clock signals are not disconnected. DIR = 0 sets power-save state DIR = 1 restores normal state

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J 23	Outputs the characters received on the modem of the test terminal. Output is terminated with ESC keyed in on the test terminal.
J 24 D1 D2 D3	As J23, but also sets the following commands ready: J 15 1 2 (if D1<>0, the command will not be carried out) J 15 2 0 (jos D2<>0, the command will not be carried out) J 17 180 (jos D3<>0, the command will not be carried out)
J 25 R S	Sets serial channel multiplexers R = control of circuit A4 (0...3) S = control of circuit A5 (0...3)
J 26 T	Sets routing switches for serial channels (A3) T = 0 No connection T = 1 Modem output to DUART2A input T = 2 Modem output to pin B/12 of connector X1 T = 3 Modem output to DUART2A input and pin B/12 of connector X1 T=4 DUART2A output to pin B/12 (out)of connector X1, B/13(in) to input of DUART2A
J 27 LATCH PIN STATE	Sets the state of a specified latch circuit to state 0 or 1 LATCH = selects the circuit (0,1) PIN = selects the pin (0...7) STATE = sets the state (0, 1)
J 28 STATE S1	Sets or clears the test flag "Ashtech on board" from the eeprom-memory. STATE=0 Clears the flag STATE=1 Sets the flag S1 Password 1 If writing to EEPROM does not succeed, ERR will be output, otherwise OK
J30 REG DAT	Writes REG to the modem register and DAT to data register.
J31 REG	Outputs contents of modem register REG.
J32	Generates test signal and connects the signal from cpu timer to the modem to help modem fault tracing. Signal is alternating 1200 Hz and 220 0 Hz. Each signal lasts for 0.5 s. Signal is stopped by keying ESC.
J33 PIN	Sets or clears manres# signal. PIN = 0 manres# = "High" PIN = 1 manres# = "Low"

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6.1.3.8. K and k Write Data To I/O Port

With command K, byte is written to I/O Port and with command k, word is written to I/O Port.

K address(0-FFFF) data	Writes data (byte) to I/O Port
k address(0-FFFF) data	Writes data (word) to I/O Port

6.1.3.9. L Display Command History With Parameters

Displays the contents of the Command History (L<Enter>). The "blank" commands in the Command History are displayed as -. See also description of command G.

6.1.3.10. M Multitest

This command is used to run either all tests (except RAM test) or only a specified test belonging to the valid mode. When required, OK/ERR is displayed according to the test result.

If E = 1 either OK (tests passed without errors) or ERR and Ermap (errors found in the test) will be output. If E = 11, the test is stopped after the test in which an error is found. If E = 1 and D = 1 and an error (or errors) is detected, only Ermap will be output (no OK/ERR).

If D = 1, the output after the test will indicate whether an error was found in the test or not (OK/ERR and the name of the test carried out).

The parameters E and D need not be specified whereby the above outputs are not made.

M 0 E D	All tests will be carried out, except RAM test.
M 1 E D	CPU/NMI/Timer2/Device Code Register Test is carried out. Tests, that NMI interrupt is not on (CPU pin 17 must be connected to logical 0). Starts Timer2 that uses internal clock, lets Timer2 count 25 ms and checks Interrupt Status Register (INTSTS) to verify the activation of interrupt request of Timer2. The device code (identifies the card) and boot code (identifies CPU type, 186 or 188) is checked from the Device Code Register.

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M 2 E D	FLASH memory test. Tests that the FLASH memory contents is correct and the address and data lines of FLASH memory are working. Test is carried out by calculating the checksums of the programs in the FLASH memory and by comparing these to the checksums calculated and stored at the programming stage. The program module name, version and Julian date will be output as well as OK or ERR according to the results of the respective module test. The above information is stored in the test results table from which they can be displayed with command D 3 0 50 (outputs 80-bytes from address 0).
M 3 E D	EEPROM memory test. The identification and revision information in the EEPROM will be checked in this test.
M 4 E D	ARCNET controller COM20020 test. Checks that the lines between the CPU and COM20020 (interrupt, address, data, chip select, reset, read, and write lines), the registers of COM20020 and RAM (2k*8bit) of COM20020 are working.
M 5 E D	Mathematics processor test
M 6 E D	DUART1 serial channel circuit test.
M 7 E D	DUART2 serial channel circuit test.
M 8 E D	Voltage test. All voltages connected to A/D converter are checked.
M 9 E D M 10 E D	Test of adjustable amplifier. The level of test signal FREQ is measured after the amplifier with twelve different D/A settings. Band pass filter test. The attenuation of the analog band pass filter of Vaisala FSK channel is measured at different frequencies
M 11 E D	Low pass filter test. The operation of the low pass filter filtering the "FFREQ" signal to the mixer is checked.
M 12 E D	Test of the analog part of FSK signal path. The operation of multiplexers (mux1 and mux2) is checked by measuring signals connected through them.
M 13 E D	Ashtech module test. This test asks the Ashtech module for the results of its own power-up test. The test is carried out only if the bit "Ashtech on board" in the EEPROM memory is set (if the test is carried out, the bit "test executed" in the additional information is set).
M 14 E D	Modem test. The frequencies 1200 and 2200Hz are generated to the modem with CPU timer. The carrier detect, serial data output and int. operation are checked during the test. Moreover, the level of identifying the low received signal is measured.

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M 20 E D SEL	Tests I/O signals. Please note that before carrying out I/O tests, you have to either give command V or carry out the EEPROM test (M 3) to make the card version recognition work properly. The I/O signals of the card are tested using test adapter card/cards. With parameter SEL, the desired subtest can be selected as follows: SEL = 0 All tests are carried out. = 1 Test for slot and rack signals = 2 Test for serial channels 4D, 5C, 6, 4B2 and 4B1 = 3 Test for serial channel 2 (cpu ser.ch1) = 4 Test for input signals FMI1, FMI2 and FME+/- = 5 Test for power output of the Ashtech module antenna amplifier = 6 Test for the 1pps signal coming from the Ashtech module = 7 Test for 1PPSIO, IP1, RTS and CTS signals = 8 Test for the battery back-up of the Ashtech module memory = 9 Test for manres# signal = A Test for Ashtech serial channel A = B Test for Ashtech serial channel B

6.1.3.11. P Program Version

Outputs the module names, version and Julian date (the first digit is the year and next three digits the Julian date) of the programs in the FLASH memories.

The above mentioned information is stored in the test result table and it can be output with command D 3 0 50 (displays 80-bytes from the address 0).

6.1.3.12. Q Restart Card

Progam execution is started as after Power Up or Hardware Reset ("software reset", not hardware reset).

6.1.3.13. R and r Read Data From I/O Port

Reads and outputs byte (command R) or word (command r) from I/O Port.

R address (0-FFFF)	Reads data (byte) from I/O Port
r address (0-FFFF)	Reads data (word) from I/O Port

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6.1.3.14. S Enable/Disable Command Saving Into The Command History

S 0	Disables Command Saving into the Command History
S 1	Enables Command Saving into the Command History (default value)

6.1.3.15. V Test Monitor Version

Outputs the version and date of the test monitor.

6.1.3.16. Z Change Monitor Mode

The command Z is used to specify the subtests to be carried out with command Multitest, i.e. M 0. Suitable test sets have been predefined for different test conditions and equipment. Moreover, it is possible to build a test set of one's own from optional tests.

The following table lists the parameters for command Z and the tests to be carried out:

Z	Ouputs the test mode in question
Z 1 P 1 P2	Sets an optional test set. If P1 and P2 = 0, the selection bits of the current test mode are output.
Z 2	MWG201A processor card only
Z 3	MWG201A connected to test adapter MWG201T-1
Z 4	MWG201A, test adapter MWG201T-1 and test adapter MWG201T-2
Z 5	MWG201A and ASHTECH
Z 6	MWG , ASHTECH and test adapter MWG201T-1
Z 10	As power-up test

In parameter P1 each selection bit represents one test that will be carried out if the bit in question is one. With parameter P2, the tests to be carried out in I/O signal test, are chosen. The following table lists all the tests for command M and the bits representing each test. Moreover, the table indicates which tests are included in the predefined test sets.

Number one in column Mode means that the test of that row is carried out in the mode in question with monitor command M 0. Character x in column Mode means that the box in question can contain one or blank as selected (test will be carried out/not be carried out).

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Test selector 1 (P1)

Bit	Mode							Test
	1	2	3	4	5	6	10	
0								-
1	x	1	1	1	1	1	1	CPU test
2	x	1	1	1	1	1	1	Code memory test
3	x	1	1	1	1	1	1	EEPROM test
4	x	1	1	1	1	1	1	COM2002(ARCNET)test
5	x	1	1	1	1	1	1	Mathematics processor test
6	x	1	1	1	1	1	1	DUART1 test
7	x	1	1	1	1	1	1	DUART2 test
8	x	1	1	1	1	1	1	MWG voltage test
9	x	1	1	1	1	1	1	Adj. amplifier test
10	x	1	1	1	1	1	1	Band pass filter test
11	x	1	1	1	1	1	1	Low pass filter test
12	x	1	1	1	1	1	1	FSK path test
13	x			1	1	1	1	ASHTECH test *)
14	x	1	1	1	1	1	1	Modem test
15	x		1		1	1		I/O signals test

*) The test is carried out if the bit "Ashtech on board" is set in EEPROM-memory.

Test selector 2 (P2)

Bit	Mode							Test
	1	2	3	4	5	6	10	
0								-
1								-
2								-
3								-
4	x					1		GPS module antenna power output test
5	x					1		1PPS signal pulse frequency test
6								-
7								-
8	x			1				GPS module battery backup test
9	x			1				Manres# signal test
10	x			1				ASHTEC serial channel A test
11	x			1				ASHTEC serial channel B test
12								IP0/1PPS signal test
13								-
14								-
15								-

The I/O signal tests that are not mentioned in the table above are always carried out when I/O test is carried out.

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6.1.4. Ermap

If an error is detected during the test, an error indicator of one bit is saved to a table referred to as Ermap.

Ermap is cleared at the beginning of each test cycle, i.e., it contains data only on the errors found during the last test cycle. In a cumulative test, the errors found during the whole test are collected to a table called Cumulative Ermap. In both Ermap tables the meaning of the bits is the same.

Ermap can be output with command D<Enter> (or D 0<Enter>).

The cumulative Ermap can be output with command D 1<Enter>.

Both tables can be cleared with command J <Enter>.

In the table on the next page the bits marked with x indicate that subtest reports error condition when the bit in question is 1 (a bit marked with x can be either 0 or 1).

Ermap

byte	bit	bit	bit	bit	bit	bit	bit	bit	
	7	6	5	4	3	2	1	0	
0	x	x	x	x	x	x	x	x	Trap code
1	x	x	x	x					CPU error
2		x	x	x				x	Memory error
3			x	x	x	x	x	x	EEPROM error
4			x	x		x	x	x	I/O signal error2
5									
6	x	x	x	x	x	x	x	x	DUART1 error
7	x	x	x	x	x	x	x	x	DUART2 error
8	x		x	x	x	x	x	x	Voltage error
9				x	x	x	x	x	Adj. amplifier error
A	x	x	x	x	x	x	x	x	Band pass filter test
B				x	x	x	x	x	Low pass filter error
C	x	x	x	x	x	x	x	x	FSK path error
D	x	x	x	x	x	x	x	x	ASHTECH error
E	x	x	x	x	x	x	x	x	Modem error
F	x	x	x	x	x	x	x		I/O signal error

Ermap byte 1 CPU error

Bit	**Meaning when the bit in question is 1**
4	NMI interrupt is active (CPU pin 17 must be connected to logical 0)
5	Interrupt request of Timer2 (uses internal clock) has not been activated in Interrupt Status Register (INTSTS).
6	Device code (identifies the card) read from Device Code Register is not correct
7	Boot code (identifies CPU type, 186 or 188) read from Device Code Register is not correct

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Ermap byte 2 Memory error

Bit	Meaning when the bit in question is 1
0	The checksum calculated from FLASH memory that is connected to the Upper Chip Select UCS* does not match with the checksum calculated and saved at programming stage.
1	-
4	1. Interrupt line (INT0) of CPU and ARCNET controller COM20020 is short-circuited to logical 0 or 1. 2. Fault in the line between CPU and ARCNET controller.
5	Error in register test of ARCNET controller COM20020 1. Fault in lines between CPU and ARCNET controller. 2. Fault in ARCNET controller.
6	Error in RAM test (2k*8bit) of ARCNET controller COM20020. 1. Fault in lines between CPU and ARCNET controller. 2. Fault in ARCNET controller.

Ermap byte 3 EEPROM error

Bit	Meaning when the bit in question is 1
0	Write timeout.
1	Write error. After writing, read data <> written data.
2	Circuit not initialized or initialization identification faulty.
3	Incorrect serial number.
4	Incorrect license number.
5	Incorrect HW revision number.

Further information on the results stored by the EEPROM test can be received with command D 3 50 14 (outputs 20-bytes from address 50hex).

Byte	Meaning
0-1	Random data (High byte -> Low byte)
2	Status after writing Random data
3-4	Test counter (High byte -> Low byte)
5	Status after writing test counter
6-7	50th word of EEPROM (must be 5A5A)
8-B	Serial number (High byte -> Low byte)
C-F	License number (High byte -> Low byte)
10-11	Revision number (High byte -> Low byte)
12-13	Test counter (High byte -> Low byte)

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Ermap byte 4 I/O signal error 2 (test adapter MWG201T-2 connected)

Bit	Meaning when the bit in question is 1
0	Error in the test of GPS module battery back-up capacitor. See additional information 60_H...64_H.
1	Error in manres" signal test. See additional information 68_H
2	Error in serial channel 4A (ASHTECH B) test. See additional information $5A_H$ and 20_H...57_H
3	-
4	Error in serial channel TXD3/RXD3. Received character ><sent character. See additional information byte $6A_H$
5	Error in serial channel TXD3/RXD3. Received character ><sent character. See additional information byte $6B_H$
6	-
7	-

Additional information on results stored by I/O signal test (ASHTECH module connector) is received using command D 6 20.

Ermap byte 6 DUART1 error

Bit	Meaning when the bit in question is 1
0	Incorrect status in data test of serial channel A
1	Incorrect data in data test of serial channel A.
2	Interrupt request for serial channel Aor timer operates incorrectly. (For more information, see next table)
3	Error in break detection of serial channel A.
4	Incorrect status in data test of serial channel B.
5	Incorrect data in data test of serial channel B
6	Interrupt request of serial channel B operates incorrectly
7	Error in break detection operation of serial channel B

Further details on the results of DUART1 serial channel test can be obtained with command D 6 6.

The stored test results for serial channel A are located in addresses 0...F, and the test results for serial channel B are in addresses 10...1F.

Timer test is carried out only in connection with serial channel A test.

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Byte ch a	ch b	should be	Meaning
0	10	0C	Status after reset
1	11	00	Status after sending the first character
2	12	0D	Status after receiving the first character
3	13	01	Status after two characters sent in a row
4	14	0F	Status after receiving two characters in a row
5	15	0F	Status when four characters have been received
6	16	0C	Status when all characters have been read
7	17	8D	Status after receiving the break signal
8	18	51	First character received
9	19	32	Second character received
A	1A	F3	Third character received
B	1B	04	Fourth character received
C		00	Extension of Ermap. If the error is detected in interrupt signal tests, the bit 4 sets. If the error is detected in timer test, the bit 1 sets.
	1C	00	
D		30..70	Lsb value of timer test counter
	1D	09	Timer test ISR register value, when timer interrupt (or timeout) has occurred.
E		0B	Msb value of timer test counter
	1E	00	
F	1F	1E	Interrupt signal state at different stages of the test

Ermap byte 7 DUART2 error

Bit	Meaning when the bit in question is 1
0	Incorrect status in data test of serial channel A
1	Incorrect data in data test of serial channel A.
2	Interrupt request of serial channel A or timer operates incorrectly. (For more information, see next table)
3	Error in break detection of serial channel A.
4	Incorrect status in data test of serial channel B.
5	Incorrect data in data test of serial channel B
6	Interrupt request of serial channel B operates incorrectly
7	Error in break detection operation of serial channel B

Further details on the results of DUART2 serial channel can be obtained with command D 6 7.

The test results of serial channel A stored by this test are located in addresses 0...F, and the test results for serial channel B are in addresses 10...1F.

Timer test is carried out only in connection with serial channel A test.

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Byte ch a	ch b	should be	Meaning
0	10	0C	Status after reset
1	11	00	Status after sending the first character
2	12	0D	Status after receiving the first character
3	13	01	Status after two characters sent in a row
4	14	0F	Status after receiving two characters in a row
5	15	0F	Status when four characters have been received
6	16	0C	Status when all characters have been read
7	17	8D	Status after receiving the break signal
8	18	51	First character received
9	19	32	Second character received
A	1A	F3	Third character received
B	1B	04	Fourth character received
C		00	Extension of Ermap. If the error detected in interrupt signal tests, the bit 1 sets. If the error detected in timer test, the bit 4 sets.
	1C	00	
D		30..70	Lsb value of timer test counter
	1D	09	Timer test ISR register value, when timer interrupt has (or timeout) occurred.
E		0B	Msb value of timer test counter
	1E	00	
F	1F	1E	Interrupt signal state at different stages of the test

Ermap byte 8 Voltage error

Bit	Meaning when the bit in question is 1
0	FSK signal level too high during the test
1	Flash circuit programming voltage Vpp incorrect
2	The voltage of memory battery back-up capacitor of the GPS-module falls during the test
3	+5V of the GPS-module faulty
4	Operating voltage (+5VA or +2.5VA) of the filter incorrect
5	+/-15V incorrect
6	
7	The level of input connected to the converter ground (Ain8) too high

Further details on the test results stored by the voltage test can be obtained with command D 6 8.

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Byte	Range	Meaning
0	<3	FSK-signal level during the test
1	$6A_H..75_H$	Flash programming voltage on
2	$2A_H..31_H$	Flash programming voltage off
3	$10_H..6E_H$	Voltage of the memory back-up capacitor of the GPS module U_{t0}
4	>=U_{t0}	Voltage of the memory back-up capacitor of the GPS module U_{t1}
5	$61_H..70_H$	Supply voltage of the GPS module on
6	$<10_H$	Supply voltage of the GPS module off
7	$64_H..6E_H$	Supply voltage of the filter (+5V,+2.5V)
8	$31_H..9B_H$	+/-15V
9	-	External input
A	<3	Ground
B	<4	Ripple of Flash programming voltage
C	<7	Ripple of GPS module supply voltage
D	<4	Ripple of filter supply voltage
E	<4	Ripple of +/-15V
F	-	External input ripple

Ermap byte 9 Adj. amplifier error

Bit	Meaning when the bit in question is 1
0	The measured signal level is not within the limit values with dac value 800_H
1	The measured signal level is not within the limit values with dac value 100_H
2	The measured signal level is not within the limit values with dac value 40_H
3	The measured signal level is not within the limit values with dac value 8_H
4	The measured signal level is not within the limit values with dac value 1_H
5	-
6	-
7	-

Further details on the test results stored by the Adj. Amplifier test can be obtained with command D 6 9.

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byte	Range	Meaning
0	$0_H..5_H$	Signal level when dac value = 800_H
1		Signal level when dac value = 400_H
2		Signal level when dac value = 200_H
3	$10_H..20_H$	Signal level when dac value = 100_H
4		Signal level when dac value = 80_H
5	$65_H..80_H$	Signal level when dac value = 40_H
6		Signal level when dac value = 20_H
7		Signal level when dac value = 10_H
8	$B0_H..D0_H$	Signal level when dac value = 8_H
9		Signal level when dac value = 4_H
A		Signal level when dac value = 2_H
B	$B0_H..D0_H$	Signal level when dac value = 1_H
C... F	0	

Ermap byte A Band-Pass Filter error

bit	Meaning when the bit in question is 1
0	Too little attenuation below the lower limit frequency
1	Too much attenuation above the lower limit frequency
2	Too much attenuation below the upper limit frequency
3	Too little attenuation above the upper limit frequency
4	6 kHz test signal (measured before input mux) faulty
5	1.8 kHz test signal (measured before input mux) faulty
6	Low pass filter after multiplexers does not work
7	Signal before filter (after input multiplexer) faulty

Further details on the test results stored by the Band-Pass Filter Test are obtained with command D 6 10..

Byte	Range	Meaning
0	$05_H..1A_H$	Input signal level when FREQ is 6 kHz
1	$20_H..40_H$	Input signal level when FREQ is 1.8 kHz
2	$55_H..6A_H$	AFM1 signal level when FREQ is 1.8 kHz
3	$<40_H$	Level measured after the filter when FREQ is 1.8 kHz
4	$>A0_H$	Level measured after the filter when FREQ is 3.0 kHz
5	$>A0_H$	Level measured after the filter when FREQ is 3.8 kHz
6	$>A0_H$	Level measured after the filter when FREQ is 4.5 kHz
7	$<40_H$	Level measured after the filter when FREQ is 6 kHz
8..F	0	

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Ermap byte B Low-pass Filter error

Bit	Meaning when the bit in question is 1
0	The measured level is not the required when FFREQ is 1.0 kHz.
1	The measured level is not the required when FFREQ is 2.0 kHz.
2	The measured level is not the required when FFREQ is 2.5 kHz.
3	The measured level is not the required when FFREQ is 3.0 kHz.
4	The measured level is not the required when FFREQ is 4.5 kHz.
5	-
6	-
7	-

Further details on the test results stored by the Low-pass filter test can be output with command D 6 11.

Byte	Range	Meaning
0		AFSK level when FFREQ is 1 kHz
1		AFSK level when FFREQ is 2 kHz
2		AFSK level when FFREQ is 2.5 kHz
3		AFSK level when FFREQ is 3 kHz
4		AFSK level when FFREQ is 4.5 kHz
5	0	
6	$45_H..55_H$	Coefficient corrected level when FFREQ is 1 kHz
7	$35_H..45_H$	Coefficient corrected level when FFREQ is 2 kHz
8	$09_H..15_H$	Coefficient corrected level when FFREQ is 2.5 kHz
9	$01_H..05_H$	Coefficient corrected level when FFREQ is 3 kHz
A	$0_H..01_H$	Coefficient corrected level when FFREQ is 4.5 kHz
B	0	
C	0	
D	0	
E		Level of AFM2 signal
F		Level of AFM2 signal (correction coefficient)

Ermap byte C FSK-path error

Bit	Meaning when the bit in question is 1
0	Pin 9 of multiplexer 1 is not in GND
1	Pin 12 of multiplexer 1 is not in GND
2	Pin 9 ofmultiplexer 2 is not in GND
3	Pin 12 of multiplexer 2 is not in GND
4	AFM1 signal level wrong
5	AFM2 signal level wrong
6	AFSK signal level wrong
7	FREQ1 signal level wrong

Further information on the test results stored by the FSK-path test can be output with command D 6 12.

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Byte	Range	Meaning
0	$0_H..5_H$	Level measured at pin 9 (gnd) of multiplexer 1.
1	$0_H..5_H$	Level measured at pin 12 (gnd) of multiplexer 1.
2	$20_H..40_H$	Level measured at pin 7 (FREQ1) of multiplexer 1.
3	$20_H..40_H$	Level measured at pin 5 (AFM2) of multiplexer 2.
4	$10_H..30_H$	Level measured at pin 6 (AFSK) of multiplexer 2.
5	$5_H..1A_H$	Level measured at pin 7 (FREQ1) of multiplexer 2.
6	$0_H..5_H$	Level measured at pin 12 (gnd) of multiplexer 2.
7	$0_H..5_H$	Level measured at pin 9 (gnd) of multiplexer 2
8..F	0	not used

Ermap byte D ASHTECH error

bit	Meaning when the bit in question is 1
0	Serial channel (DUART1 A) transmitter does not work (not ready for send)
1	Timeout of serial channel (DUART1 A) receiver
2	Timeout - Faults in 1PPS signal at DUART ip0
3	1PPS signal's pulse repetition rate is not approximately 1 second
4	Error in RAM memory test
5	Error in nonvolatile RAM memory test . This error bit sets, if the battery back-up capacitor (1F) of the GPS module is emptied. If this error does not occur in connection with rebooting , there is no equipment failure.
6	Erroneous data in ASHTECH error data
7	ROM checksum error

Further details on the test results stored by the ASHTECH test can be output with command D 6 13.

Word	Range	Meaning
0	0000, 0001 or 0011	Test executed flag. Test is carried out, if bit 6 in the EEPROM address 0 is set. 0=the test has not been carried out 1=the test has been carried out 11=the test has been carried out with hardware rev.A properties (rev. > 40 (28_H))
1	FFF0	Test result for RAM memory test
2	0000	Test result for nonvolatile RAM memory test
3	FFFF	Test result 2 for nonvolatile RAM memory test
4	0000	Always zero.
5	0000	ROM memory test result
6	0000	-
7	BF68... C738	1PPS signal pulse repetition rate (1 second = C350 = 50000 = 20µs per pulse

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Ermap byte E MODEM error

bit	Meaning when the bit in question is 1
0	Modem ID incorrect
1	Carrier detect bit in modem DR-register set, or interrupt identified without signal. Refer to details under byte 1
2	Carrier detect bit in modem DR-register not set, or interrupt not identified as test signal connected to modem. Refer to details for byte 1
3	Modem receive data (in DR register) erroneously 0, when f-in =1200Hz .
4	DUART received signal (break) from the modem. If bit 3 is not set, the fault is probably in modem-DUART connection.
5	Modem receive data (in DR register) erroneously 1, when f-in =2200Hz .
6	DUART has not received signal (break) from the modem. If bit 5 is not set, the fault is probably in modem-DUART connection.
7	The level at which 'low received signal' (long loop-bit in DR register of the modem) is incorrect

Further information on the results of the MODEM test can be output with command D 6 14.

Byte	Range	Meaning
0	Bit 7=0, bit 6=1	Circuit ID.
1		Extension of Ermap (to ermap bits 1 and 2). Bit: 0 = Carrier detect bit in DR register set without signal 1 = Interrupt identified in DUART2/ ip0 without signal 4 = Carrier detect bit in DR register not set 5 = Interrupt not identified in DUART2/ ip0.
2		Low-byte of signal level indicator
3	$08...0E_H$	High-byte of signal level indicator (High numerical value = weak signal)
4	FF_H	DUART2/ input port value (after resetting the circuits)
5	41_H, 60_H 61_H	Modem/ DR value (after resetting the circuits).
6	$0C_H$	DUART2/ status register value (after resetting the circuits)
7	FE_H	DUART2/ input port value (During signal 1200Hz)
8	68_H	Modem/ DR value (During signal 1200Hz)
9	$0C_H$	DUART2/ status reg.value (During signal 1200Hz)
A	FF_H	DUART2/ input port value (During signal 2200Hz)
B	48_H	Modem/ DR value (During signal 2200Hz)
C	$8D_H$	DUART2/ status register value (During signal 2200Hz)
D	0	-
E	$B0_H$	Status of modem control register 1 at test end.
F	30_H	Status of modem control register 2 at test end.

Ermap byte F I/O-signal error
For factory tests only.

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7. PARTS LIST

MWG201A ONLY:

Reference	Part No	Description
Assembly ref. 003	MW45027	RF-in cable, SMA/SMA, 9cm, RG188
Assembly ref. 004	MW45035	Isolation Sheet
Assembly ref. 005	18540	GPS Receiver Module, 12 channel, two RS-232 I/O ports

MWG202A ONLY:

Reference	Part No	Description
Assembly ref. 010	MW45048	Support Plate

MWG201A & MWG202A:

Reference	Part No	Description
Assembly ref. 001	MW45030	Front Panel Assembly
Assembly ref. 002	16166	Plastic Label
Assembly ref. 006	2717	Hexag. tapped spacer, AV5.5/M3-9
Assembly ref. 007	0840	Rivet, 2.5x9.9, Al.Cu.Mg L86
Assembly ref. 008	10948	Marking Sticker, Static Sensitive Warning
Assembly ref. 009	15223	Sticker Set
Integrated Circuits		
A1, A8	15981	LP 2951 ACM, Voltage Reg, 1.2...29 V, 100 mA, SO-8 I
A2	15927	MAX 691 EWE, Supervisor, SO-16W
A3	15928	DG 445 DY, Analog Switch Quad SPST CMOS, SO-16
A4, A5	16058	DG 409 DY, 8-Channel/2x4-Channel Analog Multip. CMOS, SO-16 I
A6, A9, A15	16731	TL 084 ID, 4 x Op. Amp.General Purpose FET Input, SO-14 I
A7	16881	MAX155AEWI, 8-bit, A/D Converter, 8-Ch. S/Mult.T/H&Ref, S0-28W
A10, A16	16730	TL 082 ID, 2 x Op.Amp..General Purpose FET Input, SO-8 I

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A11	18006	MAX543BCSA, D/A Converter, 12-bit, Serial-Input Multiplying DAC, SO-8 C
A12	18108	AD633JR, Analog Multiplier, SO-8 C
A13, A14	16699	DG 408 DY, 8-Chan./2x4-Chan Analog Mux, CMOS, SO-16 I
A17	18511	MAX295EWE, SC-Filter, 8th Order, Lowpass, 0.1 Hz...50 kHz, SO-16W
D1	18105	N80C187-16, 80-bit Math Coprocessor, 16 MHz, CMOS, PLCC-44 C
D2	17474	7032-LI-44-12, EPLD 36 Input / 36 Output, EPM, PLCC-44
D3	16877	TN80C186EB-16, 16-bit CPU, PLCC-84
D4, D8	15920	SCC 2692 AE1A44, DUART, PLCC-44 C
D5	16632	COM20020 IJLP, ARCNET Controller, PLCC-28 I
D6	18401	E28F400BXT-60, 4 Mbit (256k x 16; 512k x 8), Boot Block Flash, CMOS, 60 ns, TSOP-56 I
D7, D13, D20, D21	15964	74HC14, Inverter, 6xSchmitt-Trigger, SO-14 I
D9	16723	SSI 73K302L-IH, Modem, Bell 212A, 103, 202, PLCC-28 I
D10, D23	16551	HM 628512 LFP-7, 4Mbit (512kx8) Static RAM CMOS, 70 ns, SOP-32 C
D11, D16, D22, D24, D25	16507	74AC573, 8-D-Type Transparent Latch Non-inverter, SO-20W I
D12, D19	15972	74HC259, Latch, 8-bit Addressable Latch, 1 of 8 Decoder, SO-16 I
D14, D15	16735	74HC165, 8-bit Shift Register, Parallel Load, SO-16 I
D17	16530	74HC32, 4x2-Input OR Gate, SO-14 I
D18	16734	CAT93C46JI, 1 kbit Serial EEPROM, SO-8 I
D26, D27	16732	SN65ALS176, Diff. Bus Transceiver, SO-8 I

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Transistors, Diodes		
V1, V2, V6-10,V12,V18-21	15979	SM15T30C, Diode, Transil, Bi-directional, 30 V, 1.5 kW/1 ms, SOD-15
V3, V4, V25-V27, V29, V30, V32	16004	LL-103A, Diode, Si Schottky, 40 V, 200 mA, Minimelf
V5	15495	SST3904, Transistor, NPN, 40 V, 200 mA, 250 MHz, SOT-23
V11, V13	15980	SM15T15CA, Diode, Transil, Bi-directional, 15 V, 1.5 kW/1 ms, SOD-15
V14-17	16869	SMBYT03.200, Diode, Si, 200 V, 3.00 A, 25 ns, SOD-15
V22	16700	SMM120TG5H-LC, Diode, LED, green, 90 deg, 2 mA
V23	16702	SMM120TR5H-LC, Diode, LED, red, 90 deg, 2 mA
V24	16701	SMM120TY5H-LC, Diode, LED, yellow, 90 deg, 2 mA
V28, V31	16587	RLZ5230B, Diode, Zener, 4.7 V, 5 %, 400 mW, Minimelf
V33	17442	SIX-SI9953DY, Transistor, FET, 2xFET P20 V, 2.3 A, 0.25 R, SO-8
V34-V39	16634	BYM12-150, Diode, Si, 150 V, 1 A, Melf
V40, V41	17332	P6SMB6.8AT3, Diode, Transil, 6.8 V, 600 W / 1 ms, SOD6
Oscillators		
Z1	17477	SG-615YH, Crystal, 40 MHz, 200 ppm
Z2	15865	VX 4231-3200, Crystal, 32 MHz, 100 ppm, MDIL-8C
Z3	10424	VX 8111-22,1184, Crystal, 22.1184 MHz, 100 ppm, MDIL-14
Resistor Networks		
RA1, RA3-RA9	16834	8 x 10k, 2 %, SO-16
RA2	18313	8x1k, 2 %, SO-16
Resistors		
R1, R18, R24, R27, R30, R37, R38, R40, R41, R44, R49	18123	10k, 1 %, 50 ppm, 0.1 W, 0805
R2	18415	88k7, 1 %, 50 ppm, 0.1 W, 0805
R3	18604	332k, 1 %, 50 ppm, 0.1 W, 0805
R4-R6, R36, R48, R54	18117	1k0, 1 %, 50 ppm, 0.1 W, 0805

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R7, R8	18130	1M0, 1 %, 50 ppm, 0.1 W, 0805
R9, R69	18603	82k5, 1 %, 50 ppm, 0.1 W, 0805
R10, R12, R15	18596	4k75, 1 %, 50 ppm, 0.1 W, 0805
R11, R25, R65	18126	61k9, 1 %, 50 ppm, 0.1 W, 0805
R13, R52	18597	30k1, 1 %, 50 ppm, 0.1 W, 0805
R14, R60, R61	18125	47k5, 1 %, 50 ppm, 0.1 W, 0805
R16	18606	68k1, 1 %, 50 ppm, 0.1 W, 0805
R17, R64	18598	20k, 1 %, 50 ppm, 0.1 W, 0805
R19, R29, R50	18599	39k2, 1 %, 50 ppm, 0.1 W, 0805
R20-R23, R31, R34	18600	475R, 1 %, 50 ppm, 0.1 W, 0805
R26	18159	8k25, 1 %, 50 ppm, 0.1 W, 0805
R28	18414	56k2, 1 %, 50 ppm, 0.1 W, 0805
R35, R55, R58, R62	18127	100k, 1 %, 50 ppm, 0.1 W, 0805
R39, R43	18120	2k0, 1 %, 50 ppm, 0.1 W, 0805
R42, R68	18601	221R, 1 %, 100 ppm, 0.1 W, 0805
R45, R46	18602	3k65, 1 %, 50 ppm, 0.1 W, 0805
R47, R59	18411	33k2, 1 %, 50 ppm, 0.1 W, 0805
R51	18605	200k, 1 %, 50 ppm, 0.1 W, 0805
R53	18607	15k, 1 %, 50 ppm, 0.1 W, 0805
R56	18609	36k5, 1 %, 50 ppm, 0.1 W, 0805
R57	18017	5k11, 1 %, 50 ppm, 0.1 W, 0805
R63	18608	243k, 1 %, 50 ppm, 0.1 W, 0805
R66	18128	274k, 1 %, 50 ppm, 0.1 W, 0805
Capacitors		
C1, C2, C4, C5, C7-C9, C14-C19, C21-C29, C31, C32, C34, C35, C37, C43-C45, C54, C57, C58, C60, C61	15621	100 nF, 10 %, 50 V, Ceramic, 0805
C3, C11, C12	16789	10 µF, 20 %, 35 V, Tantalum, Size D (7.3 x 4.3)
C6, C42	15590	1 µF, 20 %, 16 V, Tantalum, Size A (3.2 x 1.6)
C10	18269	1 F, -20...+80 %, 5.5 V, Electrolytic, H8xD21.5
C13	17061	47 µF, 20 %, 10 V, Tantalum, Size D (7.3 x 4.3)
C20, C47, C49, C63, 64	16390	2.2 nF, 10 %, 63 V, Ceramic, 0805
C30	15492	1 µF, 20 %, 35V, Tantalum, Size B (3,5 x 2,8)
C33, C36, C40, C41, C46, C48	16908	22 nF, 10 %, 63 V, Ceramic, 0805
C38, C62, C67	15160	10 nF, 10 %, 63 V, Ceramic, 0805
C39	17504	6.8 µF, 20 %, 10 V, Tantalum, size B (3.4 x 2.6)

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C51, C52, C55, C56, C65, C66	18524	1nF, 5 %, 50 V, Ceramic, 0805
Connectors		
TP1 - TP4	0172	E-309/6, Pin
X1	16017	C096MS-C1A-0,8/5G132, Series C, Euro, 96/96N male, 90 deg,
X2, X3	16929	SBL-320-SP122-TG, 32N, socket/tin
X4	19400	70182-0137, 2x10N, socket/tin
Miscellaneous		
	2796	Wire, Hook-Up, 1x0.4 mm, Cu/Sn
	4613-0	Wire, Hook-Up, AWG26 1x (19x0.102) 0.13 mm^2, black, MIL-W-16878 D E
	4613-1	Wire, Hook-Up, AWG 26 1x (19x0.102) 0.13 mm^2, brown, MIL-W-16878-D E
	4613-2	Wire, Hook-Up, AWG 26 1x (19x0.102), 0.13 mm^2, red, MIL-W-16878-D E
	4613-3	Wire, Hook-Up, AWG 26 1x (19x0.102), 0.13 mm^2, orange, MIL-W-16878-D E
	4613-4	Wire, Hook-Up, AWG 26 1x (19x0.102), 0.13 mm^2, yellow, MIL-W-16878-D E
	4613-5	Wire, Hook-Up, AWG 26 1x (19x0.102), 0.13 mm^2, green, MIL-W-16878-D E
	11960	Shrinkable Tubing, transparent, OD 1/16 in (1.6 mm), PVF 1/16 KYNAR
	PCB0135	FR-4, 1.6mm, 8-layer panel
	0306	Slot screw, M 2.5 x 8/A4m, DIN 84
	3939	Spring Washer, B3, A4, DIN 127
	4765	Slot Screw, M 3x6/A4m, DIN 84
	7067	Spring Washer, B 2.5, A4, DIN 127

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8. DIAGRAMS AND BOARD LAYOUTS

GPS Processor MWG201A/202A Block Diagram MW35010
GPS Processor MWG201A/202A Circuit Diagram MW35009
GPS Processor MWG201A/202A Components Layout MW35028

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APPENDIX 1. SPECIFICATIONS

1. SIGNAL INPUTS

Local GPS

Frequency	1575 MHz (L1-band)
Signal level	-130 ... -50 dBm
Connector	SMA, female
LNA power	+4.5 ... 5.1 V, 125 mA max.

Remote GPS (FM)

Signal type	Bell 202 FSK (1200/2200 Hz) or Vaisala FSK (3200/4200 Hz, 1200Bd)
Max. signal level	
Bell 202 FSK	20 Vp-p
Vaisala FSK	2 Vp-p (in the band 2 kHz ... 6 kHz)
Vaisala FSK	20 Vp-p (below 2 kHz or above 6 kHz)
Sensitivity	50 mVp-p
Level control	Automatic
Impedance	5 kOhm (minimum)
Coupling	AC
Connectors	Lemo ERA OS 302CNL (Ext FM) and Euroconnector (System connector)

2. GPS RECEIVER MODULE

Type	Ashtech Sensor II
Features	
Nbr of channels	12
Time to first fix	30/90 seconds (warm/cold)

RTCM input

Data format	RTCM 104
Data types	1,2,3,6,9,16
Handshake lines	RTS and CTS
Signal levels	RS232-C
Connector	9-pin male D (at front panel)

Outputs

Position and satellite information	NMEA 0183
Carrier phase	Yes
Time pulse	1 PPS

Memory back-up	min. 24 hours

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3. CONTROL PROCESSOR

CPU

Processor type	80C186EB with 80C187
Clock rate	16 MHz (32 MHz oscillator)

Memory

SRAM	1024 kByte
FLASH PROM	512 kByte
EEPROM	128 Byte

Communication channels

Serial lines	RS232-C, six channels
Local Area Network	Arcnet

4. GENERAL

Power requirements

+5V (±5%)	800 mA max. (excluding LNA)
+5V (±5%)	200 mA stand-by
+15V (±5%)	100 mA max.
-15V (±5%)	100 mA max.

Operating conditions

Temperature	+5 ... +55ºC
Humidity	Non-condensing

Storage conditions

Temperature	-55 ... +80ºC
Humidity	Non-condensing

Dimensions and mass

Unit type	E1-size printed circuit board
Lenght, width, height	190 x 128 x 20.6 mm
Weight	290 g

System connector

Connector type	96-pin male Euroconnector
Status indicators	OK, ER and I/O Led lamps

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APPENDIX 2. SYSTEM CONNECTOR SIGNAL LAYOUT

System connector is a 96-pin, 3-row male Euroconnector

Pin/Row	a	I/O	b	I/O	c	I/O
1	GND		GND		GND	
2						
3	FMI1	I			GND	
4	Slot0#	I			Slot1#	I
5	Slot2#	I			Slot3#	I
6					Rack0#	I
7	Rack1#	I	FREQ2	O		
8			OP0	O		
9			OP1	O		
10	ADT1	I	1PPSIO	I/O		
11			IP1			
12	TxD4D	O	TxD5C	O	TxD6	O
13	RxD4D	I	RxD5C	I	RxD6	I
14	TxD4B	O	TRxD3	I/O		
15	RxD4B	I				
16						
17						
18						
19						
20					FMI2	I
21						
22	Gnd		Gnd		Gnd	
23	Arc+	I/O			Arc-	I/O
24	Test#	I				
25	TxD1	O			TxD2	O
26	RxD1	I			RxD2	I
27	Reset#	I				
28	STDC	I				
29	+5V	I	+5V	I	+5V	I
30	-15V	I	-15V	I	-15V	I
31	+15V	I	+15V	I	+15V	I
32	GND		GND		GND	

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APPENDIX 3. SYSTEM CONNECTOR SIGNAL LIST

Signal	Pin	Description	Level
GND	a1,b1,c1,c3, a22,b22,c22, a32,b32,c32	Ground	
+5 V	a29,b29,c29	+5 V operating voltage	
+15 V	a31,b31,c31	+15 V operating voltage	
-15 V	a30,b30,c30	-15 V operating voltage	
FMI1	a3	Demodulated internal telemetry signal input from Radio Receiver	-15...+15 V
Slot0#... Slot3#	a4,c4,a5,c5	Binary coded slot position number 0...15, optional input for multi unit systems	CMOS
Rack0#... Rack1#	c6,a7	Binary coded rack identification number 0...4, optional input for multi rack systems	CMOS
Freq2	b7	Test frequency output	CMOS
OP0,OP1	b8,b9	Test signal outputs	CMOS
ADT1	a10	Optional A/D input	0...+2.5 V
1PPSIO	b10	One-pulse-per-second input/output	0...+5 V
IP1	b11	Test signal input	CMOS
TxD4D	a12	Data output for serial channel 4D	RS232C
RxD4D	a13	Data input for serial channel 4D	RS232C
TxD5C	b12	Data output for serial channel 5	RS232C
RxD5C	b13	Data input for serial channel 5	RS232C
TxD6	c12	Data output for serial channel 6	RS232C
RxD6	c13	Data input for serial channel 6	RS232C
TxD4B	a14	Data output for serial channel 4B	RS232C
RxD4B	a15	Data input for serial channel 4B	RS232C
TRxD3	b14	Data output/input for serial channel 3	RS232C
FMI2	c20	Optional internal telemetry signal input from Radio Receiver	
Arc+,Arc-	a23,c23	Optional Arcnet communication line input output	-7...+10 V
Test#	a24	Test input to start test monitor program after reset, not used in normal operation	CMOS
TxD1	a25	Data output for serial channel 1, main serial control channel	RS232C
RxD1	a26	Data input for serial channel 1, main serial control channel	RS232C
TxD2	c25	Data output for serial channel 2	RS232C
RxD2	c26	Data input for serial channel 2	RS232C
MRES#	a27	Optional external reset input	CMOS

Notes: 1. All CMOS levels are for +5 V logic.
2. Signal marked by # are 0-level active.

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APPENDIX 4. FRONT PANEL CONNECTORS

P1 Connector

Serial port 4 with handshake controls is for optional external communication.

A one-pulse-per-second (1PPS) output from GPS Module is available.

Type of connector: 9 pin male D connector
Corresponding cable connector: 9 pin female D connector

P1 connector signal list and layout:

Signal	Pin	Description	Level
GND	5	Ground	
RxD4B	2	Data input for serial channel 4B	RS232C
TxD4B	3	Data output for serial channel 4B	RS232C
RTS	7	Request to send for channel 4B	RS232C
CTS	8	Clear to send for channel 4B	RS232C
1PPS	9	1 PPS output synchronized to GPS time	0...+5 V

GPS ANT Connector

Signal input for GPS local antenna.

Type of connector: SMA female
Corresponding cable connector: SMA male

NOTE

The center wire of the cable feeds the supply voltage +4.8 VDC to the antenna amplifier.

EXT FM IN Connector

Demodulated telemetry signal input from optional external Radio Receiver .

Type of connector: Lemo ERA OS 302 CNL 200
Corresponding cable connector: Lemo F OS 302 NR 042

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APPENDIX 5. LIST OF SIGNALS

The following signal names are used throughout the text and drawings of the MWG201A.

Signal	Description
1PPS	One-pulse-per-second
1PPSIO	One-pulse-per-second input/output
A00...19	Address signal
A/D	Analog to digital converter
AD00...15	Address/Data bus signal
ADBV	Backup voltage test to A/D
ADFSK	FSK signal to A/D
ADRD	A/D read signal
ADT	Optional test voltage to A/D
ADV	Operating voltages test to A/D
ADVA	Analog supply voltage test to A/D
ADVM	Module supply voltage test to A/D
ADWR	A/D write signal
AFM	FM line
AFSK	FSK line
AGND	Analog ground
ALE	Address latch enable
ANT	Antenna, antenna signal
ARC	ARCNET line
ARCSP	ARCNET speed
ARCRX	ARCNET received data
BHE	Byte high enable
BV	Backup voltage
CH1...6	Serial line channel
CLK	Clock
CPU	Central prosessing unit
CS1...7	Chip select
CTS	Clear to send
D/A	Digital to analog converter
DACLK	D/A clock
DADIN	D/A data in
DALD	D/A load
EA00..02	Analog multiplexer address
ERLT	Error light
EXT	External
FA00...02	Analog multiplexer address
FCLK	Filter clock
FFREQ	Filter frequency
FM	Frequency modulation
FME	External FM signal
FMI	Internal FM signal

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FREQ	Frequency
FSK	Frequency shift keying
GND	Ground
GRN	Green
INT	Internal
INT0...3	Interrupt
IOLT	Input/Output light
IP1	Input pin
kB	Kilobyte
LA16...19	Latched address
LCS	Lower chip select
MAD00...07	Modem address/data
MB	Megabyte
MALE	Modem address latch enable
MCS	Modem chip select
MHz	Megahertz
MINT	Modem interrupt
MLD	Modem load
MRD	Modem read
MRES	Master reset
MWR	Modem write
NCS	Numeric chip select
NPU	Numeric processor unit
OKLT	OK light
ONCE	On circuit emulation
OP0...1	Output pin
OSC	Oscillator signal
PGM	Programming
PMD	Program data
PWR	Power
PWWR	Power control write
RA00...01	Analog multiplexer address
RACK0...1	Rack code
RAM	Random access memory
RD	Read
RD1...6	Received data
REG	Voltage regulator
RES	Reset
RESO	Reset output from CPU
RESM	Reset for module
RLEN	Read latch output enable
ROM	Read only memory
RTS	Request to send
RXD1...6	Received serial line data
SA00...01	Analog multiplexer address
SHT1...3	Sheet
SINT	Serial channel interrupt
SLOT0...3	Card slot address
STDC	Standby direct current

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TA00...02	Analog switch address
TD1...6	Transmitted serial data
TXD1...6	Transmitted serial line data
TEST	Test control line
TP	Test point
UART	Universal asynchronous receiver/transmitter
UCS	Upper chip select
VPP	Programming voltage
WLEN	Write latch output enable
WR	Write pulse, write
WRH	Write high byte
WRL	Write low byte
YEL	Yellow

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