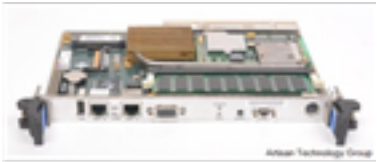
Ziatech ZT 5550

Pentium cPCI Single Board Computer



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Intel® NetStructure™ ZT 5550 High Availability Processor Board

Hardware User Manual

Revision History

Revision Date	Revision History
12/17/01	ZT 5550 Revision D release. Global format update.

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12/17/2001

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Manual Organization

This manual describes the operation and use of the ZT 5550 High Availability Processor Board. Pre-configured systems such as the ZT 5083 High Availability System are available from Intel for applications requiring 99.999% availability. Refer to the *Intel® NetStructure™ ZT 5083 15U High Availability Platform* data sheet available on Intel's website for additional information.

Chapter 1, "Introduction," introduces the key features of the ZT 5550 CPU. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 5550 against the needs of a specific application.

Chapter 2, "Getting Started," provides setup information for the ZT 5550 and its optional boards. It summarizes what you need to know in order to install and configure the boards in your system and should be read before attempting to use the boards.

Chapter 3, "Configuration," describes the switches and cuttable traces on the ZT 5550 CPU. This chapter details factory default settings and provides information allowing you to tailor your board to the needs of specific applications.

Chapter 4, "High Availability," briefly describes the main hardware and software components of Intel's Redundant CPU Architecture for High Availability systems. A section on frequently asked questions (FAQ) is also provided.

Chapter 5, "Hot Swap," defines many hot swap related terms, with emphasis on the Pin Staging and Power Ramping aspects of hot swappable applications.

Chapter 6, "Reset," explains how reset works on the ZT 5550.

Chapter 7, "System Monitoring and Alarms," explains how to access various system monitoring devices and alarming functions on the ZT 5550 CPU and ZT 4804 RPIO Transition Board.

Chapter 8, "Enhanced IDE Controller," provides an introduction to the ZT 5550's Enhanced IDE Interface Controller. It covers drive configuration, software device drivers, and the ZT 5550's support for CompactFlash IDE disk drives and optional remote drive(s).

Chapter 9, "Watchdog Timer," explains the operation of the ZT 5550's watchdog timer used to monitor user applications. Sample code is provided to illustrate how the watchdog's functions are used in an application.

Chapter 10, "Timers," explains the operation of the ZT 5550's two custom timers. These timers provide a unique 32-time stamp for use by telecommunications applications. These custom timers are distinct from the standard counter timers residing in the PIIX4 device.

Chapter 11, "Flash Memory and SRAM," discusses on-board flash memory, battery-backed SRAM, and the BIOS Recovery Module. The FLASH.EXE utility program for re-programming the BIOS is also discussed.

Appendix A, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 5550. It provides illustrations showing the connector locations and board dimensions, as well as connector pinouts.

Appendix B, "Thermal Considerations," describes the thermal requirements for reliable operation of the ZT 5550. It covers basic thermal requirements, specifics about maintaining and verifying the heat pipe temperature, and details about monitoring the output of an optional fan-sink tachometer.

Appendix C, "System Registers," provides detailed descriptions of the system and SMBus registers used to configure and monitor operation of the ZT 5550.

Appendix D, "Agency Approvals," presents UL, CE, and FCC agency approval and certification information for the board.

Appendix E, "Data Sheet Reference," provides links to data sheets for many of the devices located on the board.

Appendix F, "Customer Support," offers technical assistance and warranty information, and the necessary information should you need to return your ZT 5550 for repair.

1. Introduction

This chapter provides a brief introduction to the ZT 5550. It includes a product definition, a list of product features, a "ZT 5550 Connector Plate" figure, a functional block diagram, and a description of each block. Unpacking information and initial board configuration instructions are provided in Chapter 2, "Getting Started."

See Chapter 3, "Configuration," for configuration details and Appendix A, "Specifications," for complete power and temperature requirements, as well as connector locations, descriptions, and pinout tables.

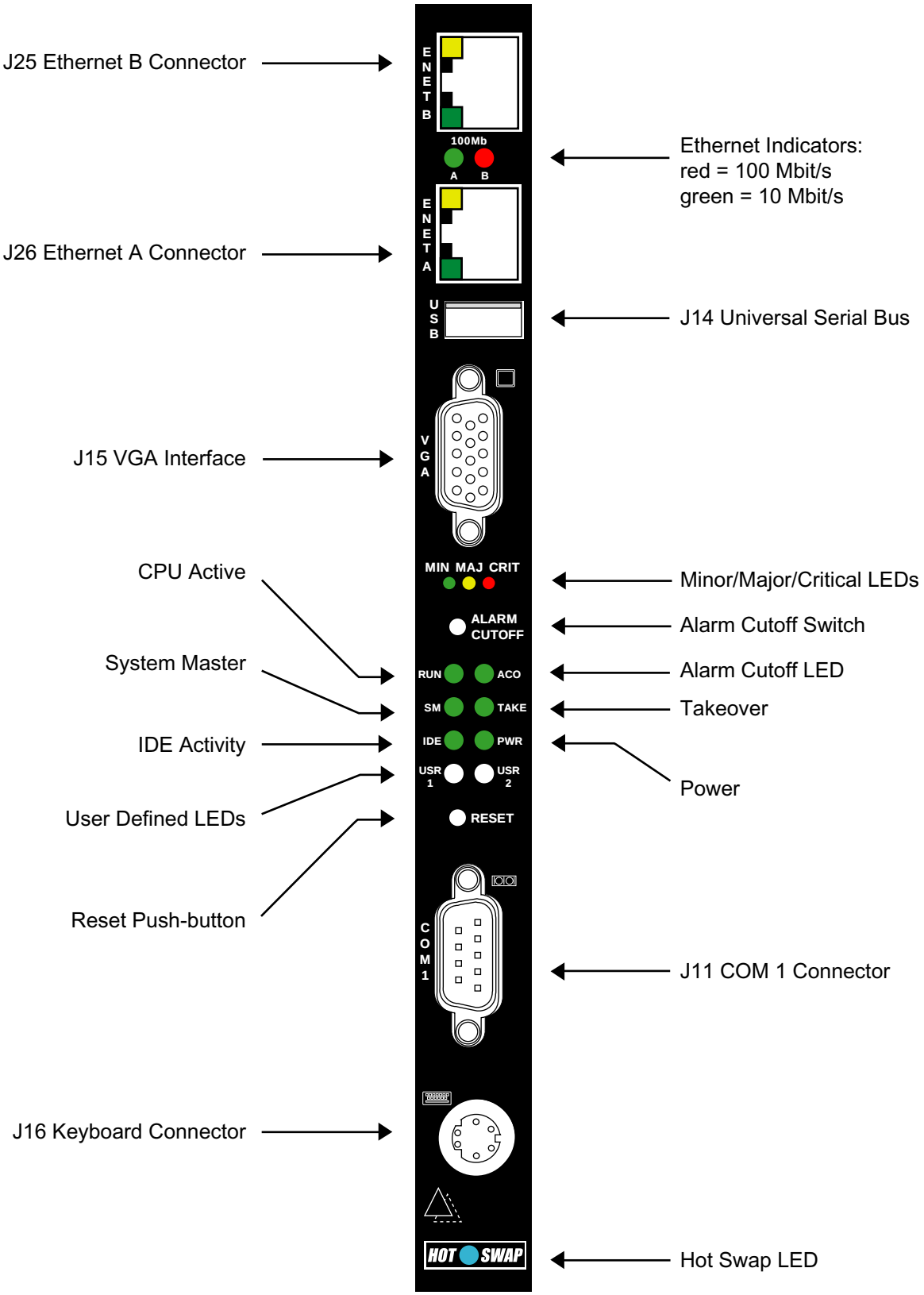
Product Definition

The ZT 5550 is an Intel Pentium III processor-based single board CompactPCI* computer. Two ZT 5550 CPUs can be used on the same backplane, as an Active/Standby System Master pair, or as a Split Mode (Revision D and later boards) Standby System Master pair, to provide redundancy for the ZT 5083 and ZT 5084 High Availability (HA) Systems designed for mission-critical telecommunication and industrial control applications requiring 99.999% availability. The ZT 5083 and ZT 5084 systems incorporate redundant ZT 5550s, power supplies, and cooling fans in a single enclosure. Each ZT 5550 can be an Active, Standby, or Split Mode (Revision D and later boards) Host CPU. Resource management and database information is synchronized between the Active, Standby, and Split Mode (Revision D and later boards) Hosts via a bi-directional serial channel and an Ethernet* channel.

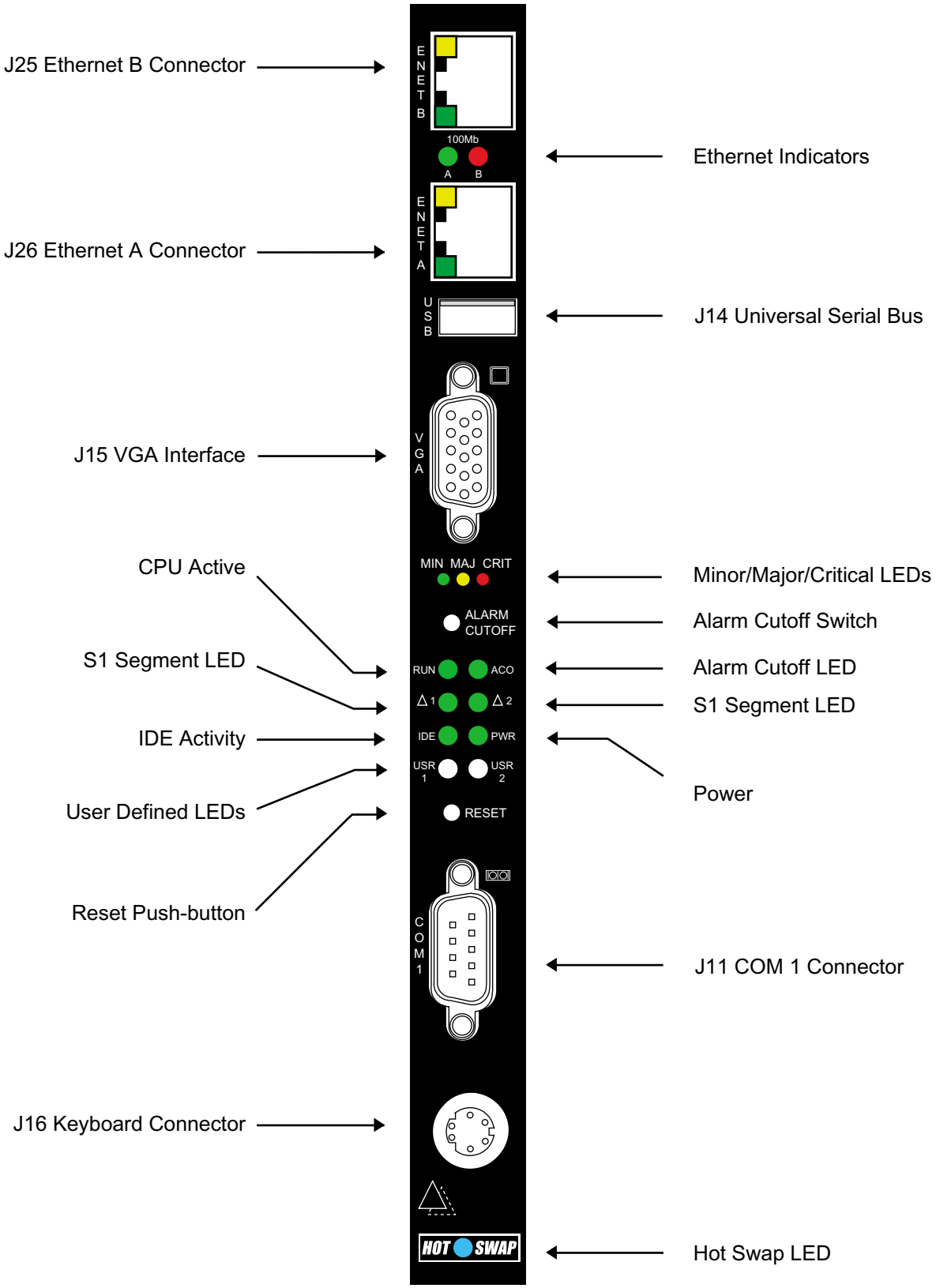
The ZT 5550 utilizes the Intel Pentium III Processor Mobile Module: Embedded Module Connector 2 (EMC-2) to provide extremely high PCI performance and the latest in memory and I/O technology. An active ZT 5550 is designed to function in the System Slot controlling the CompactPCI backplane.

Each ZT 5550 supports attachment of an optional 6U I/O Expansion Board (such as the ZT 96072 or ZT 96073). I/O Expansion boards (IOX) are designed to greatly expand the I/O capability of the ZT 5550. Rear-panel access to the CPU/IOX combination can be provided by rear-panel I/O (RPIO) transition boards (such as the ZT 4804 and ZT 4802).

ZT 5550 Revision C and Earlier Faceplate



ZT 5550 Revision D and Later Faceplate



Features

- Acts as a CompactPCI System Slot device in either HA or non-HA systems. Up to 14 peripheral devices (assumes non-HA system) can reside on dual CompactPCI bus segments
- CompactPCI Specification, PICMG* 2.0, Version 3.0 compliant
- CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0 compliant as a 5V platform component
- Intel Pentium III Processor Mobile Module (EMC-2)
- Single 6U CompactPCI slot form factor (two slots with ZT 96072 or ZT 96073 IOX board)
- Built-in numeric coprocessor support (Intel Pentium III)
- 16 KB of CPU instruction cache
- 16 KB of CPU data cache
- 512 KB pipelined burst L2 cache
- PCI mezzanine interface (Primary PCI bus)
- Dual 10/100 Mbit/s Ethernet interfaces
- Supports 64-bit PCI segment-to- segment transfers between the dual backplane bus segments.
- Supports 64, 128, or 256 MB of ECC SDRAM in a 168-pin DIMM socket in a single CompactPCI slot
- 4 MB of flash memory
- 128 KB of battery-backable SRAM
- CompactFlash memory socket
- Standard AT* peripherals include:
  - Two enhanced interrupt controllers (8259)
  - Three counter/timers (one 8254)
  - Real-time clock/CMOS RAM (146818)
  - Two enhanced DMA controllers (8237)

  - 8042 compatible keyboard controller

- Two 16C550 RS-232 serial ports (COM1 at front panel, COM1 and COM2 at rear panel)
- Universal Serial Bus (USB)
- System Management Bus (SMBus)
- Two Stage Programmable Watchdog Timer
- Additional 32-bit and 16-bit programmable Timers
- Push-button reset
- Software programmable LEDs
- DC power monitors (3.3V and 5V)
- I/O expansion options
- Five-year warranty

Functional Blocks

Below is a functional block diagram of the ZT 5550. The following topics provide overviews of the ZT 5550's functional blocks.

High Availability

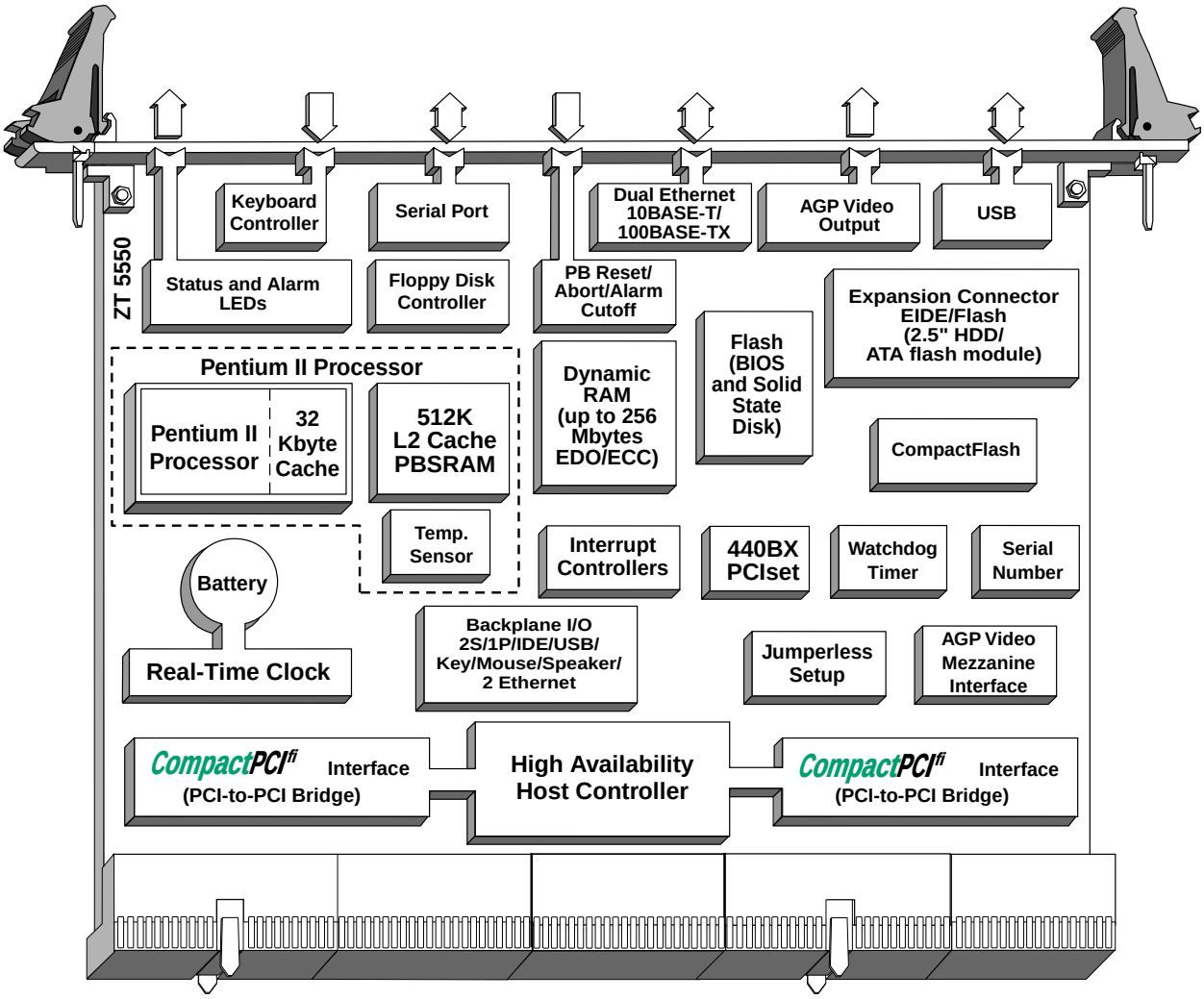
Intel's High Availability architecture incorporates redundant ZT 5550 CPUs, power supplies, and cooling fans in a single enclosure. The redundant CPU is in "hot standby" mode backing up the Active CPU. Resource management and data base information is synchronized between the Active and the Standby Hosts via a bi-directional serial channel and an ENET channel. The system minimizes duplication of expensive peripherals through an N+1 hot swappable peripheral board architecture. The additional (+1) 'standby' peripheral is online and ready for use should another peripheral fail.

Each redundant ZT 5550 provides a communications channel (COMM) for inter-CPU messaging, fault detection, and data base synchronization. It is based on 100Mbps Ethernet hardware and utilizes a standard communications driver (COMM DRV).

Interface to the dual CompactPCI buses is provided by PCI-to-PCI (P2P) bridges. The Host Controller (HC) controls these bridges such that the P2P on the Standby CPU is isolated from the backplane. Arbitration of the CompactPCI buses is provided by additional logic within the HC.

See Chapter 4, "High Availability," for more details.

Functional Block Diagram



CompactPCI Bus Interface

The ZT 5550 operates in a 6U CompactPCI system. The CompactPCI standard is electrically identical to the PCI local bus standard but has been enhanced to support rugged industrial environments and more slots. Additionally, when used in a Hot Swap compliant backplane and in accordance with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*, the ZT 5550 supports hosting hot swappable peripherals in a powered system. The ZT 5550 can also function in a standard (non-Hot Swap) CompactPCI system.

Rear-Panel I/O

The following I/O signals are routed out the J3 Rear-Panel User I/O Connector.

- COM1
- COM2

- Floppy
- Ethernet A
- Ethernet B
- Front Panel Eject LED
- SMBus
- Speaker
- Keyboard
- USB (Port 1)
- PS/2 Mouse
- IDE secondary channel

Dual CompactPCI System Slot Interfaces

The ZT 5550 features two Intel 21154 PCI-to-PCI bridges to support both the J1/J2 and J4/J5 CompactPCI Bus Segments. The 21154 is compliant with the *PCI Local Bus Specification, Revision 2.1.* Each System Slot Interface provides the isolation, arbitration, and clocks for seven PCI peripheral cards, meaning support for up to 14 CompactPCI peripherals (all bus masters) without the need for an external bridge board.

Special features of the 21154 include:

- 33 MHz PCI bus operation
- 64-bit PCI transparent operation with 32-bit or 64-bit devices between backplane bus segments

Intel Pentium III Processor

The ZT 5550 uses the Intel Pentium III Processor Mobile Module (EMC-2), a small, highly integrated assembly containing an Intel Pentium III mobile processor and its immediate system-level support. The processor module contains a power supply for the processor's unique voltage requirements, system memory (L2 cache), and the core logic required to bridge the processor to the standard system buses. The module interfaces electrically to its host system via a 3.3V PCI bus, a 3.3V memory bus, and some Intel 443BX Host Bridge control signals.

The Intel Pentium III Processor Mobile Module includes 32 KB of code and data cache (L1 cache). Additionally, the Pentium III Processor Mobile Module contains a secondary 512 KB cache (L2 cache) to further enhance memory performance.

I/O Expansion Connector

The ZT 5550's 100-pin, 2 mm, stacking I/O Expansion Connector (J6) routes VGA, IDE (secondary), and floppy signals between the CPU and an Intel I/O Expansion board (such as the ZT 96072 and the ZT 96073).

SMBus (Alarming Functions)

The ZT 5550 incorporates the System Management Bus (SMBus) for access to several system monitoring and alarming functions. The SMBus allows the ZT 5550 to monitor on-board operating voltages and temperatures.

Since the HC comes out of PCI reset with the SMBus isolated from the backplane, the system BIOS (or user software) is required to enable SMBus access to the backplane. The system BIOS provides a user setup option to determine how the SMBus should be enabled. The SMBus Isolation Control functions are implemented in the HC with the register mapped at BAR Offset 7Ah as shown in the "SMBus Isolation Control" table.

Board and processor temperatures are monitored and can be set to interrupt at programmable thresholds. The SMBus is supported with an Intel software driver that can be used to read and program the various devices.

Additionally, the SMBus is accessible to certain optional rear-panel transition boards (such as the ZT 4804) via rear-panel user I/O connector J3.

Intel's optional alarm software may be purchased for telecommunication alarm applications, where data logging, programmable alarms, and system management is desired. This software utility provides program notification and visual indication of events and event statuses. See Chapter 7, "System Monitoring And Alarms," for more information.

SMBus Isolation Control

BAR Offset	Register Symbol	Register Name	Default Value	Access	Size	Reset
7Ah	SMB	SMBus Isolation Control	00h	R/W	8 bits	PCIRST
Bit	**Description**			**Access**	**Default**	
7:1	**Reserved –** Reserved for future use			none	XX	
0	**SMBus Enable** – When this bit is 0, the SMBus is disconnected from the backplane. When this bit is set to 1, the SMBus is connected to the backplane.			R/W	0	

AGP Mezzanine

The ZT 5550 provides a 114-pin AGP mezzanine connector for interfacing to an Intel AGP Video Mezzanine Adapter (such as the ZT 96079). The CPU - AGP adapter combination

occupies only a single CompactPCI slot. The AGP bus supports 32 bits of data and runs at a speed of 66 MHz, giving it a theoretical bandwidth of 266 MB/s in 1x AGP mode, or 533 MB/s in 2x AGP mode (two transfers per clock cycle).

The topic "AGP Video" in Appendix E, “Data Sheet Reference,” contains a link to an Intel website detailing its “Accelerated Graphics Port Technology”. The site also provides a link to the AGP Specification.

PCI Mezzanine

The PCI bus (Primary, Bus 0) mezzanine interface (J7) provides 3.3V PCI signaling to Intel I/O expansion boards and optional mezzanine adapter boards that may be attached to the ZT 5550.

Dual Ethernet Interfaces

The ZT 5550 provides two Ethernet interfaces (ENET A / ENET B) through the industry standard Intel 21143 PCI-Ethernet Bridge. The Physical Interface (PHY) is provided by the Level One* LXT970 Dual-Speed Fast Ethernet Transceiver.

Both 10 Mbit/s and 100 Mbit/s Ethernet protocols are automatically detected through each of two RJ-45 connectors on the faceplate. Status LEDs on the faceplate indicate transmit and receive activity and 100 Mbit operation for each channel.

In a non-HA system, both ENET channels are available through rear-panel user I/O connector J3. In an HA system, ENET B is directed out J5 to serve as a communications channel (COMM) for inter-CPU messaging, fault detection, and data base synchronization.

The topic "Ethernet" in Appendix E, “Data Sheet Reference,” contains links to the data sheets for the Ethernet devices used on the ZT 5550.

Memory and I/O Addressing

A single, 168-pin, SDRAM DIMM is used on the ZT 5550 for local memory. The ZT 5550 supports modules of 32, 64, 128 and 256 MB. The SDRAM is implemented as Error Correcting Coded (ECC), which will correct single bit errors (97% of all DRAM errors are single bit errors) and report multiple bit errors to the operating system.

The ZT 5550 also provides 4 MB of on-board flash memory. The flash memory contains the system BIOS. The remainder may be allocated as solid-state drive. A 128 KB battery-backable SRAM device is also provided for application use, or for video emulation in cases where the CPU has no local video.

See the “Memory Configuration” and “I/O Configuration” topics in Chapter 2 for more information.

Serial I/O

The ZT 5550 provides two 16C550 PC-compatible serial ports:

Front Panel: COM1 directed out J11
Rear Panel: COM1 and COM2 directed out J3

The serial ports are implemented with a 5V charge pump technology to eliminate the need for a ±12V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 KB. The serial ports are configured as DTE. The COM1 RS-232 transceiver enable can be software controlled.

Since the HC comes out of PCI reset with the COM1 transceiver disabled, the system BIOS (or user software) is required to enable COM1. The system BIOS provides a user setup option to determine how COM1 should be enabled. The COM1 Isolation Control functions are implemented in the HC with the register mapped at BAR Offset 0Bh as shown in the "COM1 Isolation Control" table.

The ZT 5550's serial controller resides in the National Semiconductor* PC87309 SuperI/O* device. The topic "SuperI/O" in Appendix E, "Data Sheet Reference," provides a link to the data sheet for this device.

COM1 Isolation Control

BAR Offset	Register Symbol	Register Name	Default Value	Access	Size	Reset
0Bh	COM1	COM1 Isolation Control	00h	R/W	8 bits	PCIRST
Bit	**Description**			**Access**	**Default**	
7:2	Reserved			none	XX	
1	**COM1 Active Host Enable** – This bit has meaning only when bit 0 of this register is cleared to 0. When COM1[0] = 0, and this bit is set to 1, the COM1_ENA output is put in high impedance only when this host is in Active mode. This function is disabled when HA = 0.			R/W	0	
0	**COM1 Unconditional Enable** – When this bit is set to 1, the COM1_ENA output is put in high impedance regardless of the HC operating mode. In practice, COM1_ENA is routed to the active-high COM1 transceiver ENABLE input, which has a passive pull-up.			R/W	0	

Interrupts

Two enhanced, 8259-style interrupt controllers provide the ZT 5550 with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs

- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Serial I/O
- Keyboard
- Floppy disk
- IDE interface
- On-board PCI devices
- Digital I/O
- Printer Port
- Counter/Timers
- Real-Time Clock
- CompactPCI backplane (21154)

Enhanced capabilities include the ability to configure each interrupt level for active high-going edge or active low-level inputs.

The ZT 5550's interrupt controllers reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix E, “Data Sheet Reference,” provides a link to this data sheet.

Counter/Timers

Three 8254-style counter/timers are included on the ZT 5550 as defined for the PC/AT*. Operating modes supported by the counter/timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot.

The ZT 5550's Counter/Timers reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix E, “Data Sheet Reference,” provides a link to this data sheet.

In addition to the 8254-style counter/timers provided in the 82371EB (PIIX4E) device, the ZT 5550 also provides two custom timers offering unique functions to telecommunications applications. These timers reside in the custom Host Controller device and are described in Chapter 10, “Timers.”

DMA

Two enhanced, 8237-style DMA controllers are provided on the ZT 5550 for use by the on-board peripherals. DMA channel 2 is reserved for a future peripheral such as an optional floppy drive. DMA channels 1 or 3 are assigned to the parallel printer port for ECP mode support

The ZT 5550's DMA controllers reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix E, “Data Sheet Reference,” provides a link to this data sheet.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose, battery-backed, CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS setup information. The system BIOS is also Year 2000 (Y2K) Compliant.

The ZT 5550's Real-Time Clock resides in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix E, “Data Sheet Reference,” provides a link to this data sheet.

Power Ramp Circuitry

The ZT 5550’s power ramp circuitry prevents glitches to the power supply and disruption to CompactPCI peripherals caused by insertion or removal of the CPU. Power ramp circuitry allows the board's voltages to be ramped in a controlled fashion, thereby eliminating any large voltage or current spikes caused by removing or inserting the board while the system is still under power. This controlled ramping is a requirement of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*.

The ZT 5550's hot swap controller unconditionally resets the board when it detects that the 3.3V, 5V, and 12V supplies are below an acceptable operating limit. These limits are defined as 4.75V (5V supply), 3.0V (3.3V supply), and 10.0V (+12V supply).

Fault current sensing is also provided. If a board fault (short circuit) or over-current condition is detected, the hot swap controller automatically removes power from the ZT 5550 components and the “Fault/Power” indicator LED turns red.

See Chapter 5 “Hot Swap” for more information. You may also wish to obtain the complete *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0.* A link to PICMG’s website is provided in the topic "Hot Swap" in Appendix E, “Data Sheet Reference.”

Reset

The ZT 5550’s various reset types can be tailored to the needs of specific applications.

- Backend Power Down
- Hard Reset
- Soft Reset
- NMI

See Chapter 6, “Reset,” for more information. See the PIIX4E data sheet to learn more about the Reset and Control Register within the Intel 82371EB (PIIX4E) device. A link to the data sheet is provided in the topic "PIIX4" in Appendix E, “Data Sheet Reference.”

Two-Stage Watchdog Timer

The ZT 5550's custom two-stage watchdog timer circuit is contained in the High Availability Host Controller. The watchdog timer monitors system operation and is programmable for one of eight different timeout periods (from 0.25 s to 256 s). When the watchdog times out, the first-stage timeout (T1) is driven first, followed by the second-stage (T2) 250ms later. T1 results in an NMI or a CPUINIT, depending on DIP switch configuration. When the switch is closed, CPUINIT is asserted; when open, NMI is asserted. T2 results in a hard reset. Watchdog T1 and T2 can be independently disabled.

See Chapter 9, “Watchdog Timer,” for more information about the ZT 5550’s Watchdog Timer implementation. Chapter 9 also includes sample code showing how to use the watchdog in an application.

Universal Serial Bus (USB)

The emerging Universal Serial Bus (USB) provides a common interface to slower-speed peripherals. In the future, functions such as keyboard, serial ports, printer port, and mouse ports will be consolidated into USB, greatly simplifying the cabling requirements of future computers. The ZT 5550 provides a front panel USB port (J14, Port 0). A second USB port (Port 1) is directed through the ZT 5550’s rear-panel I/O connector J3.

The ZT 5550's USB Host Controller resides in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix E, “Data Sheet Reference,” provides a link to the data sheet for this device.

Enhanced IDE Controller

The ZT 5550 includes an Enhanced IDE controller for optional internal (CompactFlash socket) or external (IOX, RPIO) EIDE drives. The EIDE controller is covered in more detail in Chapter 8, “Enhanced IDE Controller.”

The EIDE controller resides in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix E, “Data Sheet Reference,” provides a link to the data sheet for this device.

Floppy Controller

The ZT 5550 includes a Floppy Disk Controller for optional external (IOX, RPIO) floppy drives. The floppy controller resides in the National Semiconductor PC87309 SuperI/O device. The topic "SuperI/O" in Appendix E, “Data Sheet Reference,” provides a link to the data sheet for this device.

Keyboard Controller

The ZT 5550 includes an on-board PC/AT keyboard controller, available through front-panel connector J16. Keyboard signals are also available through rear-panel I/O connector J3.

The ZT 5550's keyboard controller resides in the National Semiconductor PC87309 SuperI/O device. The topic "SuperI/O" in Appendix E, "Data Sheet Reference," provides a link to the data sheet for this device.

Mouse

The ZT 5550 includes signals for a PS/2 style mouse, available through rear-panel I/O connector J3. The mouse is also available through front panel connector J16 when an IBM* ThinkPad* style "Y" cable is used. The system BIOS supports standard PS/2 bus mouse devices. Use of the PS/2 mouse leaves both serial ports available for other communication.

The ZT 5550's mouse controller resides in the National Semiconductor PC87309 SuperI/O device. The topic "SuperI/O" in Appendix E, "Data Sheet Reference," provides a link to the data sheet for this device.

Speaker Interface

For external speaker interfacing, the ZT 5550 supports an external AT-compatible speaker through connector J23. The speaker outputs are also available through rear-panel I/O connector J3.

LED Indicators

The LEDs located on the connector plate are defined below. See the "Programming the LEDs" topic in Chapter 2 for software code used to program the User LEDs.

- **Ethernet Channels A and B:**
  - Status LEDs, one per channel: green = 100Base-T; off = 10Base-T
  - RJ-45 LEDs, two per connector: green = data receive; yellow = data transmit
- **MIN MAJ CRIT** (Minor = green; Major = yellow; Critical = red)
- **RUN** (CPU Activity): green = run; red = halt
- **ACO** (Alarm Cutoff): red = cutoff
- **SM** (System Master) (Revision C and earlier boards): green = this CPU Active; no light = this CPU Standby; red = configuration mode; orange = Active Host in reset
- **TAKE** (Takeover) (Revision C and earlier boards): green = friendly; red = hostile
- **S1 and S2 Segment LEDS** (Revision D and later boards):

S1 LED	S2 LED	Meaning
Green	Green	Active both Segments
Green	Black	Active S1 - Armed for takeover
Green	Red	Active S1 - Not Armed for takeover
Green	Orange	Active in System Slot in non-HA backplane
Black	Green	Active S2 - Armed for takeover
Black	Black	Standby both Segments
Black	Red	Not Defined
Black	Orange	Not Defined
Red	Green	Active S2 - Not Armed for takeover
Red	Black	Non-Active in Config Mode
Red	Red	Non-Active in Local Reset
Red	Orange	Active S2 - in Reset
Orange	Green	Installed in Peripheral slot
Orange	Black	Not Defined
Orange	Red	Active S1 - in Reset
Orange	Orange	Active both - in Reset

- **IDE** (Local EIDE disk activity) green = active; off = inactive
- **PWR** (Power): green = power on; red = fault
- **USR1 USR2**: (Bi-color user LEDs)
- **HOT SWAP**: blue = board removal is allowed

Software

The Intel Netstructure Embedded BIOS is loaded in flash on board the ZT 5550. The BIOS is user-configurable to boot an operating system from local flash memory, a fixed or floppy drive, a CD-ROM drive, or over a network. The BIOS also supports the BIOS Boot Specification (BBS) to allow devices with BBS Option ROMs to be selectable in the boot order menu.

The ZT 5550 is compatible with all major PC operating systems. Intel provides additional operating system support when the ZT 5550 is purchased in conjunction with an Intel NetStructure development system (for example, the Intel NetStructure ZT 5083 15U High Availability Platform). This support may include additional drivers for NetStructure products such as peripherals and flash drives. Software device drivers for the ZT 5550 can be found at:

http://www.ziatech.com/software/matrix.htm.

The following operating systems are supported:

- Windows* 2000 Professional OS or Windows 2000 Server OS
- Industry standard version of Linux*
- Comprehensive board support package (BSP) for VxWorks*. The CompactPCI VxWorks-Tornado II BSP streamlines the implementation of VxWorks on the ZT 5550. The VxWorks Tornado development system must be purchased directly from WindRiver.

2. Getting Started

This chapter summarizes the information you need to make the ZT 5550 CPU operational and should be read before attempting to use the board.

Unpacking

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Intel for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to Intel. Refer to the "Customer Support" section for assistance information.

Caution: Like all equipment utilizing MOS devices, the ZT 5550 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 5550 to handle the board.

System Requirements

The following topics briefly describe the basic system requirements and configurable features of the ZT 5550 CPU board. Links are also provided to other chapters and appendices containing more detailed information.

Connectivity

The ZT 5550 is designed to operate in a backplane providing CompactPCI buses on connectors J1/J2 and J4/J5. When used with the ZT 4804 RPIO Transition board, the backplane's rear panel connector on J3 must be available and have through-pins to the ZT 5550's J3 connector. See the "Connectors" topic in Appendix A for complete descriptions and pinout tables for all the board's connectors.

For specific backplane requirements in a High Availability system, see the "System Backplane" topic in Chapter 4.

LPT1 Signaling

The ZT 5550 CPU does not direct LPT1 signals out the J3 Rear-Panel I/O connector. Therefore, if your system includes a ZT 5980 System Utility Board and/or a ZT 4800 Rear-panel I/O board, be aware that the LPT1 interfaces on these boards will not work with the ZT 5550 CPU, and hardware that may be connected to these interfaces can be damaged in a ZT 5550 implementation.

Warning: ZT 5550 users should not connect hardware to the ZT 5980 or the ZT 4800 LPT1 interfaces!

Electrical and Environmental Requirements

The parameters given below should be maintained to avoid improper operation and possible damage to the board.

The ZT 5550 requires +5VDC ± 5% @ 2.2A typical, 3.8A maximum; +3.3VDC ± 5% @ 2.7A typical, 4.4A maximum; +12VDC ± 5% @ 250mA typical, 350mA maximum.

Intel recommends vertical mounting. Depending on your configuration, the ZT 5550 is supplied with a heatpipe to allow operation between 0° and approximately 50° C ambient. Heatpipe configurations require 250 LFM (linear feet per minute) of airflow across the board.

The maximum power dissipation of the EMC-2 module is 14 W. External airflow must be provided if operating above 25° C ambient. Because the ambient temperature (around the heatsink) can easily exceed 25° C in an enclosed card rack, it is strongly recommended that a “fan tray” below the card rack be used to supply external airflow. The relative humidity should be less than 95%, non-condensing.

Maintain these parameters to avoid improper operation and possible damage to the board. See Appendix A, “Specifications,” and Appendix B, “Thermal Considerations,” for more details.

Switches and Cuttable Traces

The ZT 5550 CPU Board provides several switch and cuttable trace configuration options for features that cannot be provided through the BIOS Setup Utility. Refer to Chapter 3, “Configuration,” for location figures and descriptions.

Memory Configuration

The ZT 5550 addresses up to 4 GB of memory. The address space is divided between memory local to the board and memory located on the CompactPCI bus (or buses). Any memory not reserved or occupied by a local memory device (SDRAM/flash) is available to the CompactPCI bus.

The ZT 5550 is populated with several memory devices:

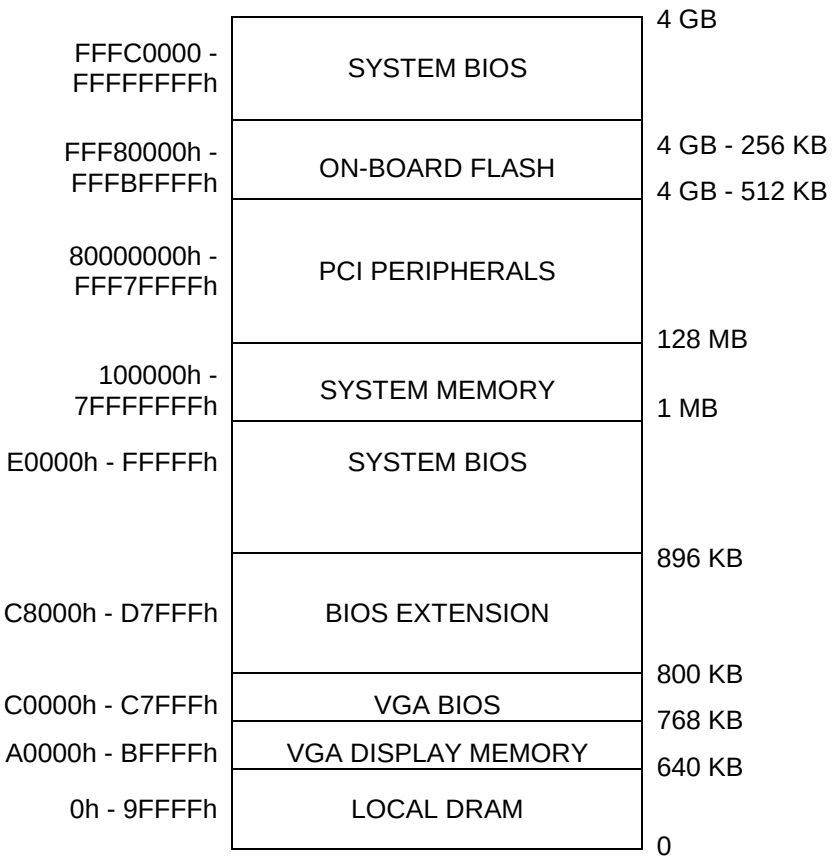
SDRAM	Industry-standard, 168-pin, DIMM socket (J10) supports SDRAM modules up to 256 MB.
Flash	4 MB flash device soldered directly to the board contains the BIOS, and optionally space for use as solid state drive.
SRAM	128 KB battery-backed static RAM device.

The “Memory Address Map Example” illustration shows example memory addressing for the ZT 5550.

I/O Configuration

The ZT 5550 addresses up to 64 KB of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the CompactPCI bus. Any I/O space not occupied by a local I/O device is available for the CompactPCI bus. The ZT 5550 is populated with several I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Map" illustration.

Memory Address Map Example



I/O Address Map

*Onboard ISA peripherals addressed between 100h - 7FFh decode 11 bits of address (A0 - A10). Therefore, these peripherals will alias throughout the 16-bit I/O space at the following ranges:

- x100-x3FFh
- x500-x7FFh
- x900-xBFFh
- xD00-xFFFh

PCI devices can fully utilize the address space from D00 - FFFFh, since subtractive decoding is used for the onboard ISA devices.

D00h	— FFFFh	PCI*	64 K
CF8h	— CFFh	PCI Config/RST Control	
780h	— CF7h	PCI Reserved	
780h	— 77Fh	LPT ECP Registers	
400h	— 777h	RESERVED	
3F8h	— 3FFh	COM1	1 K
3F0h	— 3F7h	Floppy / IDE Registers	
3E0h	— 3EFh	Reserved	
3B0h	— 3DFh	VGA Registers	
380h	— 3AFh	Reserved	
378h	— 37Fh	LPT	
300h	— 377h	Reserved	
2F8h	— 2FFh	COM2	768
200h	— 2F7h	Reserved	
1F8h	— 1FFh	Reserved	512
1F0h	— 1F7h	Primary IDE Registers	
178h	— 1DFh	Reserved	
170h	— 177h	Secondary IDE Registers	
100h	— 16Fh	Reserved	
F0h	— FFh	Coprocessor	256
E0h	— EFh	Digital I/O	
C0h	— DFh	On-board Slave DMA Controller	
B4h	— BFh	Reserved	
B2h	— B3h	APM Registers	
B0h	— B1h	Reserved	
A0h	— AFh	On-board Slave Interrupt Controller	
93h	— 9Fh	Reserved	
	92h	Fast RESET and Gate A20	
90h	— 91h	Reserved	
81h	— 8Fh	On-board DMA Page Registers	
	80h	Diagnostic Port	
	79h	ZT 5550 Watchdog Timer Register	
	78h	ZT 5550 System Register 0	
70h	— 77h	On-board Real-Time Clock	
60h	— 6Fh	Keyboard and System Ports	
50h	— 5Fh	Reserved	
40h	— 4Fh	On-board Timer/Counters	
30h	— 3Fh	Reserved	
2Eh	— 2Fh	87309 SuperI/O Configuration	
22h	— 2Dh	Reserved	
20h	— 21h	On-board master Interrupt Controller	
0h	— 1Fh	On-board Master DMA Controller	0

Programming the LEDs

The ZT 5550 includes two user-controlled bi-color (red/green) Light-Emitting Diodes (LEDs) located on the connector plate. The LEDs are software programmable through System Register 7 (Port E5h). The LEDs are turned off after a power cycle or a reset.

As shown below, two bits are used to control the state of each LED. Bits 0 and 2 change the LED from red to green; Bits 1 and 3 turn the LED on or off. Since a bi-color LED is used, there are three states for the LED: green, red, and off.

User LED1		**User LED2**	
E5h Bit 1 = 1	LED1 is ON	E5h Bit 3 = 1	LED2 is ON
E5h Bit 0 = 1	Green	E5h Bit 2 = 1	Green
E5h Bit 0 = 0	Red	E5h Bit 2 = 0	Red
E5h Bit 1 = 0[1]	LED1 is OFF	E5h Bit 3 = 0[1]	LED2 is OFF

Note: [1] Indicates 'off' condition after power-on or hard reset.

The LED bits are in the same register as other functions. It is important **not** to change the state of other bits in this register when modifying the User LED status. The following code demonstrates the mechanism for modifying the bits for LED1:

```
; set USR1 LED ON (GREEN)
cli                             ; clear interrupts
in    al, E5h                   ; read current state
and   al, FCh                   ; preserve other register bits
or    al, 03h                   ; set USR1 LED (GREEN and enabled)
out   E5h, al                   ; output new value for register
sti                             ; re-enable interrupts
; set USR1 LED ON (RED)
cli                             ; clear interrupts
in    al, E5h                   ; read current state
and   al, FCh                   ; preserve other register bits
or    al, 02h                   ; set USR1 LED (RED and enabled)
out   E5h, al                   ; output new value for register
sti                             ; re-enable interrupts
; set USR1 LED OFF
cli                             ; clear interrupts
in   al, E5h                    ; read current state
and  al, FDh                    ; set bit 3 to turn off LED
out  E5h, al                    ; output new value for register
sti                             ; re-enable interrupts
```

Video Interface Selection

When used without IOX or RPIO boards, the ZT 5550 provides front-panel video only (J15—an AGP video board is also required for front panel video). A ZT 5550 used in combination with certain IOX and RPIO boards supports both front- and rear-panel video. Interfaces are enabled through software on the CPU and switch settings on the IOX board. Details on rear-panel video configuration in multi-board systems are presented in the "Configuration" chapter of IOX board manuals.

Removing Mezzanine Boards

Your system may implement an I/O Expansion board (such as the ZT 96072 or ZT 96073) or a Intel mezzanine adapter (such as the ZT 97074 AGP Video Adapter). Mechanical connection of IOX boards and mezzanine adapters is reinforced by metal or nylon stand-offs screwed through mounting holes in each board.

Caution: To avoid damage to the CPU, IOX boards, and mezzanine adapters install or remove boards at a static-free workstation. When disconnecting boards, Intel recommends removing only the screw attaching the board to the stand-off. If it is necessary to remove the stand-off from the CPU, be aware that on some CPUs washers may be located between the PCB and the stand-off. Be sure to retain and re-install these washers to their original position if they are removed for any reason.

Care should also be taken when installing and removing boards to prevent premature wear or accidental bending of pins and receptacles. When removing a board, try to disengage the pins evenly across the length of the connector instead of prying only from one side. It may be helpful to gently wiggle the board from side-to-side when removing it.

BIOS Configuration Overview

This topic presents a brief introduction to the Intel NetStructure Embedded BIOS. For more detailed information about the BIOS and other utilities, see the *Intel NetStructure Embedded BIOS* software manual. The Intel NetStructure Embedded BIOS has many separately configurable features. These features are selected by running the built-in Setup utility.

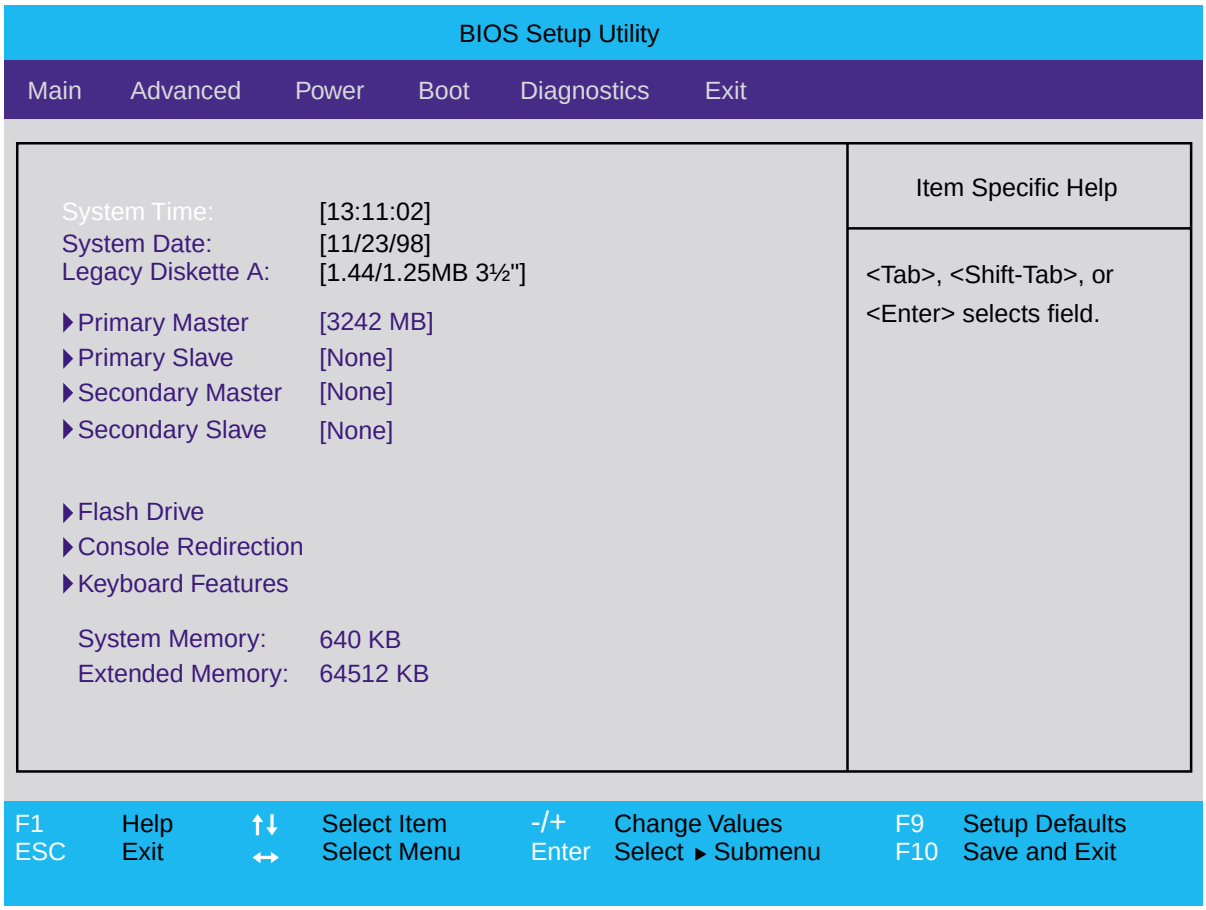
Setup is a utility you use to configure your system. The system configuration settings are saved in a portion of the battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot up or reset. The configuration is protected by a checksum word for system integrity. To access the Setup utility, press the "F2" key during the system RAM check at boot time.

When Setup runs, an interactive configuration screen displays. See the "Setup Screen" illustration below for an example. Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the Setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the Setup screen. Context sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the Setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the + or – keys to change the value of a parameter.

Items in the main portion of the screen that have a triangular mark to their left are submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press the “Enter” key.

Setup Screen



Console Redirection

Console Redirection allows users to monitor the ZT 5550’s boot process and to run the ZT 5550’s SETUP utility from a remote serial terminal. Connection is made either directly through a serial port or through a modem.

The Console Redirection feature is most useful in cases where it is necessary to communicate with an Intel single board computer, such as the ZT 5550, in an embedded application without video support.

See the *Intel NetStructure Embedded BIOS Software Manual* for more information about Console Redirection.

Identifying Media Options

It may be helpful to review the *ZT 5550 High Availability Software Manual for Windows NT** for an overview of ZT 5550 software considerations prior to installing software on the board. For detailed information about your operating system, refer to the documentation provided by the operating system vendor.

The "Media Options" table below identifies the media options that may be available to you depending on the boards in your system. Use it to determine the target and distribution media you will use to install software on the ZT 5550 CPU.

Media Options

Media	Possible Device Locations	Cable Interfaces
On-board flash device	ZT 5550 CPU — a portion of this 4 MB device may be available as solid state drive, used to contain user programs and data. This feature requires a driver. Intel provides drivers (on the BSP CD-ROM) for several operating systems.	N/A
IDE devices Hard Drive: CD-ROM: CompactFlash:	 • ZT 96072 IOX — J8, 44-pin, 2.5", Primary • ZT 96073 IOX — J7, 44-pin, 2.5", Primary • Utility board installed in a peripheral slot • External or in media bay (if applicable) • Utility board installed in a peripheral slot • External or in media bay • ZT 5550 CPU — J9, 50-pin, Primary	The ZT 4804 RPIO board provides a 40-pin interface (J9) to the CPU's secondary IDE channel. The channel is also available via a 40-pin latching ribbon cable connector on the back side of certain backplanes.
Floppy devices	• ZT 96073 IOX — J8, 26-pin • Utility board installed in a peripheral slot • External or in media bay (if applicable)	**ZT 4804:** J10, 34-pin floppy cable connector. **ZT 4802:** J6, 34-pin floppy cable connector. Some backplanes provide a 34-pin latching ribbon cable interface to the CPU's floppy signals.
SCSI devices Hard Drive/ CD-ROM:	• Utility board installed in a peripheral slot • External or in media bay (if applicable)	**Front-panel** access to a PMC SCSI controller that may be installed on the ZT 96072 IOX board PMC1 position. **Rear-panel** access to the controller may be available on the ZT 4802 RPIO board's J9 (PMC1) 68-pin SCSI interface.

3. Configuration

The ZT 5550 is user configurable to meet the requirements of specific applications. Most configuration options are selected through the BIOS Setup utility, discussed in the "BIOS Configuration Overview" topic in Chapter 2. Some options cannot be software controlled and are configured with switches or cuttable traces. Switch options are made by closing or opening the desired switch. Cuttable trace options are made by installing and removing surface mount zero Ω resistors. Details on rear-panel video configuration are provided in the "Configurations" chapters of IOX Board manuals.

This chapter details the ZT 5550's switch and cuttable trace options. Illustrations showing the locations of switches and cuttable traces are also included.

Switch Options and Locations

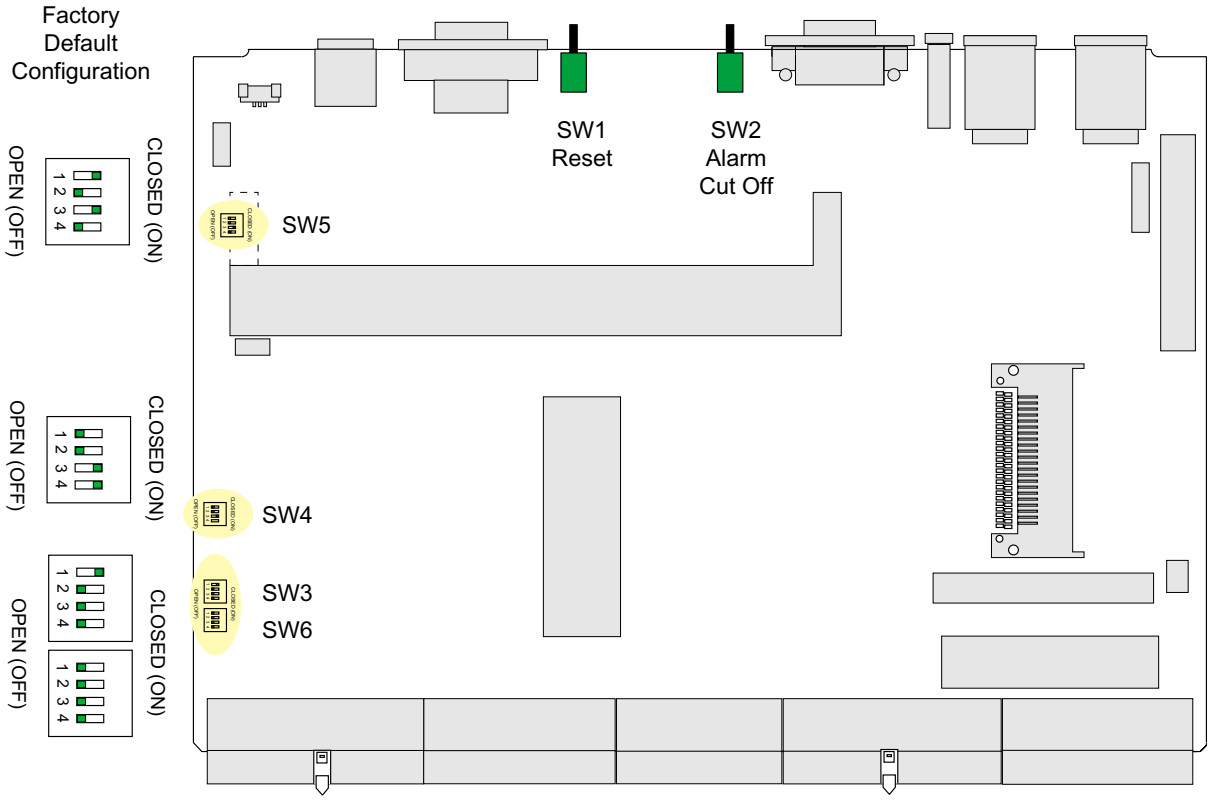
The ZT 5550 contains four banks of switches on the component side of the board and two push-button switches on the connector plate. These are listed and briefly described in the "Switch Cross-Reference" table below.

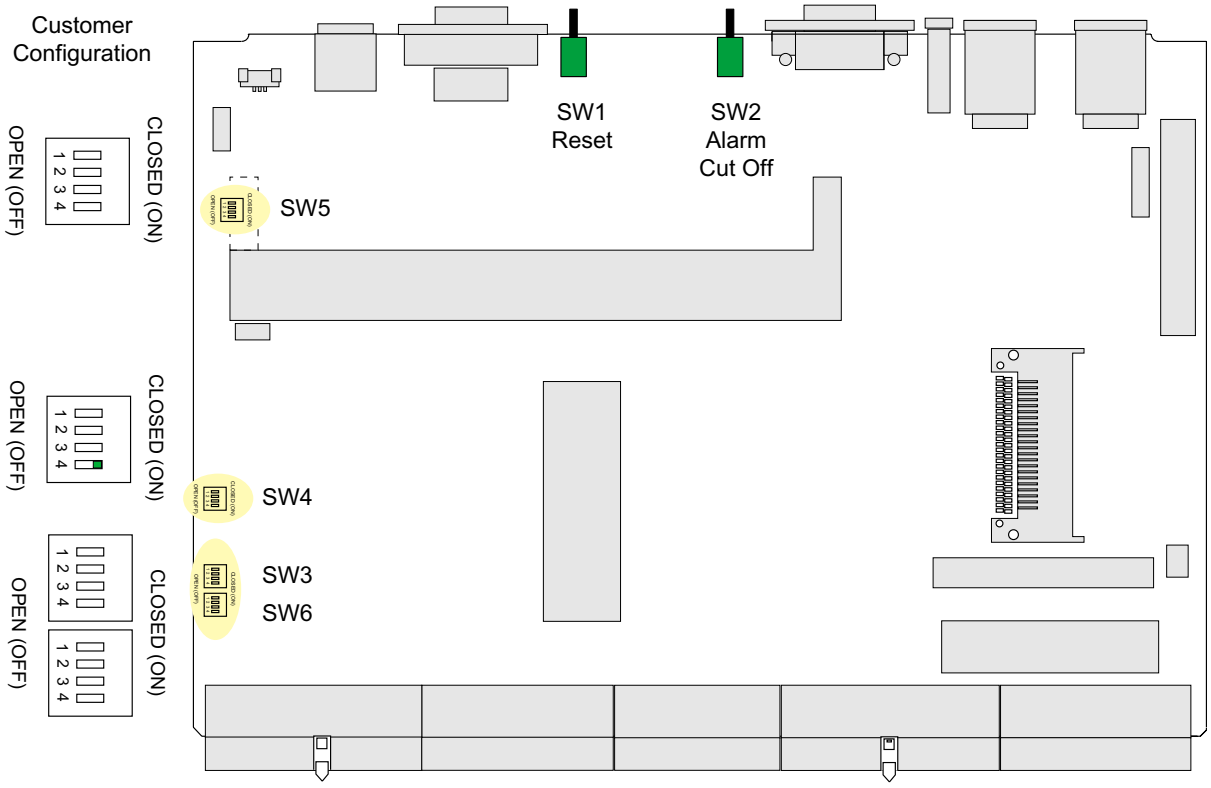
Factory default and customer switch configuration is shown in the "Factory Default and Customer Switch Configuration" figure. The customer portion of the figure provides a blank jumper layout; use this to document your configuration if it differs from the factory default. This will allow you to easily restore the configuration if it is changed.

Switch Cross-Reference Table

Function	Switch
Reset	SW1 (push-button on front panel)
Alarm Cut Off	SW2 (push-button on front panel)
CMOS Clear/Battery Backup	SW3-1, -2
SRAM Battery Backup	SW3-3
Soft Reset Mode Select	SW3-4
Ethernet Channel/Port Select	SW4-1, -2
Configuration Mode Preset	SW4-3
Reserved	SW4-4
BIOS Recovery	SW5-1
Port 80 Test Code	SW5-2
IDE Master/Slave Selection	SW5-3
Flash Write Protect	SW5-4
Console Redirection	SW6-1
Software Configuration	SW6-2, -3, -4

Factory Default and Customer Switch Configuration





Switch Descriptions

The following topics list the switches in numerical order and provide a detailed description of each switch. Switches are titled in the form “SWx-N,” where “x” is the switch number and “-N” is the switch position (for example, SW4-2 means “switch number 4, position 2”).

SW1 (Reset)

SW1 is a push-button on the ZT 5550's front panel. Pressing SW1 for **less** than 2 s issues a soft reset; pressing SW1 for **more** than 2 s issues a hard reset. Reset is discussed in more detail in Chapter 6.

Note: There are two possible modes for soft reset, depending on the position of SW3-4. This functionally may change on future revisions of the ZT 5550.

SW2 (Alarm Cut Off)

SW2 is a push-button on the ZT 5550's frontplate providing a control function local to the ZT 5550. When SW2 is pressed, the switch closure is latched and activates the SMBus ALERT# signal. Switch state can be read by application software via the SMBus. The latched software can then toggle the frontplate ACO LED (via SMBus) and transtition any ZT 4804 audible relay alarm output signals required.

SW3-1, -2 (CMOS Clear/Battery Backup)

These switches are used to battery back and clear the CMOS memory (contained in the real-time clock). When closed, SW3-1 connects the CMOS memory to the on-board battery. To clear the CMOS, open SW3-1 and close SW3-2. After 2 s, return SW3-2 to the open position and SW3-1 to the closed position. Factory default is SW3-1 closed and SW3-2 open.

Warning: Do not have SW3-1 and SW3-2 closed at the same time. Doing so will significantly shorten battery life.

SW3-1	SW3-2		CMOS Configuration RAM
Closed	Open	Default	Normal operation - battery backed
Open	Closed		Clear CMOS (return to default after clearing)

SW3-3 (SRAM Battery Backup)

This switch is used to battery-back the 128 KB SRAM device. This feature is useful when the SRAM contains configuration data the user wants to retain during periods when the ZT 5550 may be powered-off. Factory default is SW3-3 open.

Caution: Battery-backing the SRAM significantly shortens battery life, especially if the CMOS memory is also battery-backed (SW3-1 = open). However, infrequent power-offs for brief periods are acceptable.

SW3-3		Function
Open	Default	SRAM not battery backed
Closed		SRAM battery backed

SW3-4 (Soft Reset Mode Select)

This switch selects whether an NMI or a CPUINIT is issued on soft reset, according to the table below. The status of this switch is monitored by System Register 5 (E3h, bit 5). Factory default is SW3-4 open. Reset is discussed in more detail in Chapter 6.

Note: This functionality may change on future revisions of the ZT 5550.

SW3-4		Function
Open	Default	Issue CPUINIT on soft reset
Closed		Issue NMI on soft reset

SW4-1, -2 (Ethernet Channel/Port Select)

These switches are used to route Ethernet channels A and B to front- or rear-panel Ethernet connectors, according to the table below. By default, both channels are configured for front-panel Ethernet access (both SW4-1 and SW4-2 open).

Note: There are two possible modes for rear-panel Ethernet B. See the SW4-3 topic for details.

SW4-1		**Ethernet Channel A**
Open	Default	Software Controlled through BIOS setup utility
Closed		Force to front panel (J26)
SW4-2		**Ethernet Channel B**
Open	Default	Software Controlled through BIOS setup utility
Closed		Force to front-panel (J25)

SW4-3 (Configuration Mode Preset)

Use this switch to force the Configuration Mode Command bit in the HC to be set when a PCI Reset or CPU Init occurs.

Note: This functionality may change on future revisions of the ZT 5550.

SW4-3		**Function**
Open		No preset
Closed	Default	Preset Configuration Mode bit

SW4-4 (Reserved)

This switch is reserved for Intel and should not be operated by the user.

SW5-1 (BIOS Recovery)

This switch allows booting from a module in the BIOS Recovery Socket (T3H1). When SW5-1 is closed (On), the board boots from the BIOS in the on-board flash memory. When SW5-1 is open (Off), the board boots from the module in the BIOS Recovery Socket (T3H1). SW5-4 must be open to re-flash the BIOS. The status of this switch is monitored by System Register 5 (E3h, bit 6). See the "BIOS Recovery Module" topic in Chapter 11 for details on how to flash the BIOS. Factory default is closed.

SW5-1		Function
Open		Boot from the BIOS recovery socket (T3H1)
Closed	Default	Normal operation (boot from flash)

SW5-2 (Port 80 Test Mode)

When closed, this switch sets Port E0h to decode accesses to I/O Port 80 in addition to E0h. The system BIOS outputs Port 80 POST codes during bootup. The Port 80 data is output on Port 0, bits 0 to 7. These bits are accessible at the I/O Expansion connector J6, pins A8-15. Use Port 80 test mode for debugging custom software and hardware. The Port E0h register is also accessible at its default address (E0h). Factory default is open.

SW5-2		Function
Open	Default	Normal operation
Closed		Port 80 Test Mode enabled

SW5-3 (IDE Master/Slave Selection)

This switch is used to configure IDE devices on the primary channel for master or slave operation. The CompactFlash card (J9) must be configured as the master IDE device (SW5-3 = closed), unless you have an IOX board carrying a hard drive configured as the master IDE device (usually this means it is unjumpered).

If the drive on the IOX board is jumpered for "Cable Select", the master/slave relationship between the drives is toggled through SW5-3. Changes to master/slave status automatically appear in the BIOS Setup utility.

The ZT 5550 is shipped with no device installed in J9, therefore SW5-3 is open by default (slave operation). See the "CompactFlash Input Characteristics" topic in Chapter 8 for more information.

CompactFlash Card on CPU; No IDE Drive on IOX Board

SW5-3	Function
Open	Slave configuration is not allowed in this case.
Closed	CompactFlash device is IDE Master.

CompactFlash Card on CPU and IDE Drive on IOX Board

SW5-3	Function
Open	CompactFlash device is IDE Slave (assumes device on IOX is jumpered correctly).
Closed	CompactFlash device is IDE Master (assumes device on IOX is jumpered correctly).

SW5-4 (Flash Write-Protect)

Close this switch to write-protect the BIOS and flash disk portion of the flash memory. Open this switch to use the FLASH.EXE utility to recover from a corrupted BIOS (see SW5-1 topic above). The status of this switch is monitored by System Register 5 (Port E3h, bit 7). Factory default is open.

SW5-4		Function
Open	Default	Flash disk/BIOS read/write
Closed		Flash disk/BIOS read only

SW6-1 (Console Redirection)

Open this switch to disable console redirection. The status of this switch is monitored by the user's software through System Register 5 (Port E3h, bit 0) to provide user-configurable features. When open, these switches read back a 0; when closed they read back a 1. Factory default is open.

SW6-1		Function
Open	Default	Console Redirection Disabled
Closed		Console Redirection Enabled

SW6-2, -3, -4 (Software Configuration)

The status of these switches is monitored by the user's software through System Register 5 (Port E3h, bits 1-3) to provide user-configurable features. When open, these switches read back a 0; when closed they read back a 1. Factory default is open.

SW6-2, -3, -4		Read-back
Open	Default	0
Closed		1

Cuttable Trace Options and Locations

The ZT 5550 contains several cuttable traces (zero Ω shorting resistors) that allow the user to configure certain options not configurable through the BIOS Setup Utility. The "Cuttable Trace Locations" figure shows the placement of the ZT 5550 cuttable traces. The "Cuttable Trace Definitions" table provides a quick cross-reference for the ZT 5550 cuttable trace descriptions that follow.

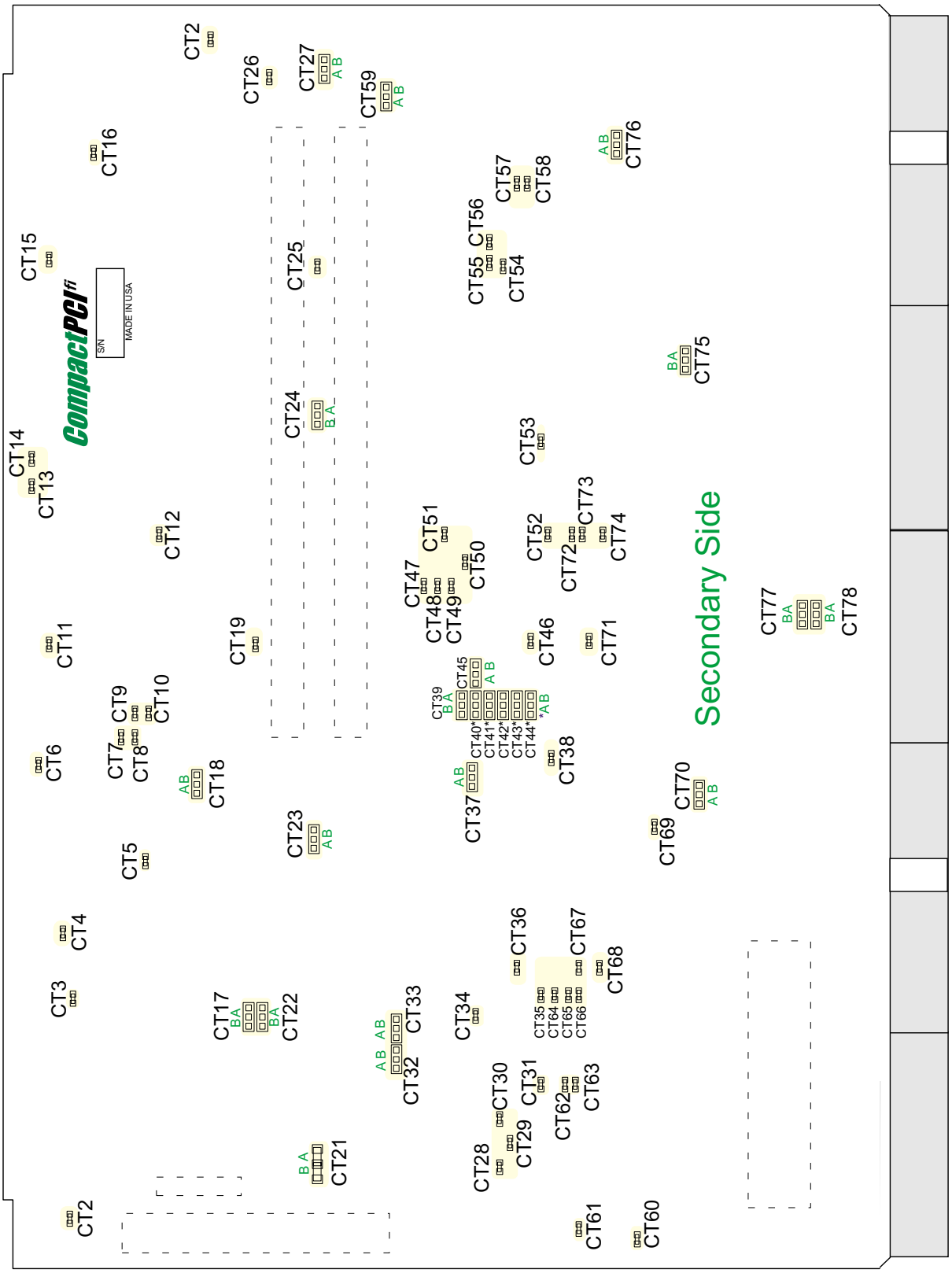
There are two types of cuttable traces on the ZT 5550: single-option, and double-option. **Single option cuttable traces** are implemented using 0603 surface mount pads. A zero Ω shorting resistor is then soldered between these pads to make the connection. **Double option cuttable traces** (CTx, CTy, CTz) are implemented using three 0603 surface mount pads. The zero Ω shorting resistor is then soldered between one set of pads, depending on the chosen option.

Caution: The ZT 5550 has additional cuttable traces not documented in this manual (other than appearing on the "Cuttable Trace Locations" drawing). These are reserved for Intel and should not be modified by the user. Modifications to documented cuttable traces should only be performed by a qualified technician familiar with surface mount soldering techniques. The product warranty is voided if the board is damaged by customer modifications.

Cuttable Trace Definitions

CT#	Default	Description
CT2 - 4, CT6, CT11, CT13-15, CT20	Out	Connect logic ground to chassis ground
CT7 - CT10	Factory	Reserved
CT12	Out	Floppy MSENO not connected to DRATE0
CT27	Out	No voltage for optional fan sink on J27 pin 1
CT79	A	CompactFlash Socket Voltage Select

Cuttable Trace Locations



Cuttable Trace Descriptions

The following topics list cuttable traces in numerical order and provide a detailed description of each cuttable trace listed.

CT2-4, CT6, CT11, CT13-15, CT20 (Connect Chassis GND to Logic GND)

The connectors on the ZT 5550's connector plate are on an isolated chassis ground. These connectors can be connected to the ZT 5550 logic ground by installing these eight cuttable traces. All these cuttable traces should be in or all out. The factory default is all out.

Position		Function
All In		Connectors on connector plate connected to logic ground.
All Out	Default	Connectors on connector plate on an isolated chassis ground.

CT7-CT10 (Reserved)

These reserved cuttable traces are set at the factory and should not be modified by the user.

CT12 (Floppy DRATE0 to MSEN0)

Some manufacturer's floppy drives require a connection between the floppy drive MSEN0 pin and the floppy controller's DRATE0 pin. Install CT12 if your system requires this. The factory default is out.

Position		Function
In		Floppy MSEN0 pin connected to controller's DRATE0 pin.
Out	Default	Floppy MSEN0 pin not connected to controller's DRATE0 pin.

CT27 (FAN Voltage Selection)

CT27 selects the voltage for an optional fan sink to cool the processor module. Power for the fan is supplied by connector J27, pin 1. The A position selects +5V operation; the B position selects +12V operation. Factory default is both out.

Position	Function
A	+5V on J27 pin 1 for fan sink operating voltage.
B	+12V on J27 pin 1 for fan sink operating voltage.
Both out	Default

CT79 (CompactFlash Socket Voltage Select)

The factory default configuration sets the ZT 5550's CompactFlash socket (J9) to 5.0V operation (CT79 in position A). This setting requires the CompactFlash card to have "Type 2" or "Type 3" input characteristics. SanDisk* currently manufactures cards meeting these specifications. Setting the CompactFlash socket to VCC = 5.0V has the advantage of allowing master/slave operation with a drive mounted on certain Intel IOX boards (such as the ZT 96072 and the ZT 96073).

Position		Function
A	Default	CompactFlash operates at VCC = 5.0V
B		CompactFlash operates at VCC = 3.3V

Caution: If the CompactFlash socket (J9) is set for VCC = 3.3V operation (CT79 = B position), *do not* connect a disk drive on the ZT 96072 or ZT 96073 IOX boards. Doing so will damage the CompactFlash device.

4. High Availability

For many critical applications, reliance on single CPU systems represents a big gamble. This is because a single CPU, however reliable, remains a potential single point of failure. In a single processor system, a failed CPU causes a system to be down for the time it takes a service person to replace the board. In remote areas this could take several hours or even days.

Intel's redundant CPU architecture provides 99.999% availability, greatly minimizing the possibility of a failed CPU causing system downtime. The system provides redundant CPUs, power supplies, and cooling fans in a single enclosure. The presence of a redundant CPU allows the transfer of control from a failed CPU to the Redundant CPU. Switchover from a failed CPU to its redundant CPU takes about 10 ms.

Resource management and data base information is synchronized between the Redundant Hosts via a bi-directional serial communications channel and an ENET channel. The system minimizes duplication of expensive peripherals through an N+1 hot swappable peripheral board architecture. The additional (+1) 'standby' peripheral is online and ready for use should another peripheral fail.

This chapter describes the components that comprise Intel's High Availability architecture. Chapter 8, "ZT 5550 CPU Configuration," documents the switches (SW4-1, SW4-2, SW4-3) used to configure the board for High Availability operation.

If you are using Windows NT Operating System, refer to the *ZT 5550 High Availability Software Manual for Windows NT* for information on how to configure and control the ZT 5550's High Availability (HA) features according to application requirements.

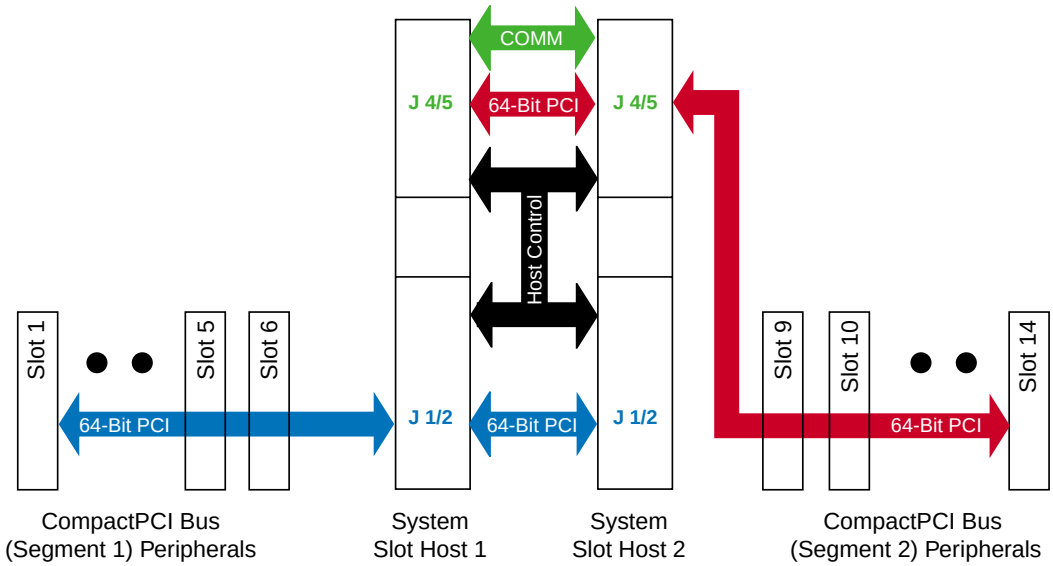
If you are using VxWorks Operating System, refer to Intel's *Redundant System Slot* Software User Manual for information on how to configure and control the ZT 5550's High Availability (HA) features according to application requirements.

Core Technology Approach

The core technology of Intel's High Availability System is described in the following topics. Intel's approach makes the following assumptions:

- Because the host CPUs reside on the main CompactPCI buses, the possibility exists that a hard bus failure could halt the system (deemed an acceptable compromise in the interests of cost).
- If a CPU fails and control of the PCI bus is to pass to the Redundant CPU, a certain minimum functionality must remain in the PCI-to-PCI (P2P) bridges on each host CPU.
- A "Host Controller" with basic logic on each CPU must remain operable so that control can be transferred from the failing Host to the Redundant Host.
- The changeover from one host to the other must be accomplished without requiring a system reset to recover.

HA System Backplane Architecture



Modes of Operation

The High Availability System has three main modes of normal operation.

- Active-Standby mode allows one CPU to be the Active CPU and be in control of both bus segments. The other CPU is the Standby CPU and is isolated from the backplane.
- Active-Active mode (Revision D and later boards) allows each CPU to be active on a different segment while being isolated from the other. For example, one CPU is active on the J1-J2 segment while being isolated from the J4-J5 segment, while the other CPU is active on the J4-J5 segment and isolated from the J1-J2 segment.
- Locked Active-Active mode (Revision D and later boards) is identical to Active-Active mode except that no takeover can occur. This guarantees that each segment is independent of the other, allowing for two identical systems within one enclosure.

System Backplane

The system backplane supports two CompactPCI buses accessible by each of the two redundant CPUs. Each CPU has the capability of controlling one, two, or zero bus segments. This allows both CPUs to be active on separate segments or for one CPU to control both segments. At any given time, one and only one CPU controls a bus segment and the Redundant CPU is isolated from that bus segment..

The backplane also has separate buses for CPU to CPU communication (COMM) and Host Control functions. The “HA CPU Architecture” figure illustrates the backplane for the HA system in which a total of 12 peripheral slots are provided with 32- or 64-bit capability.

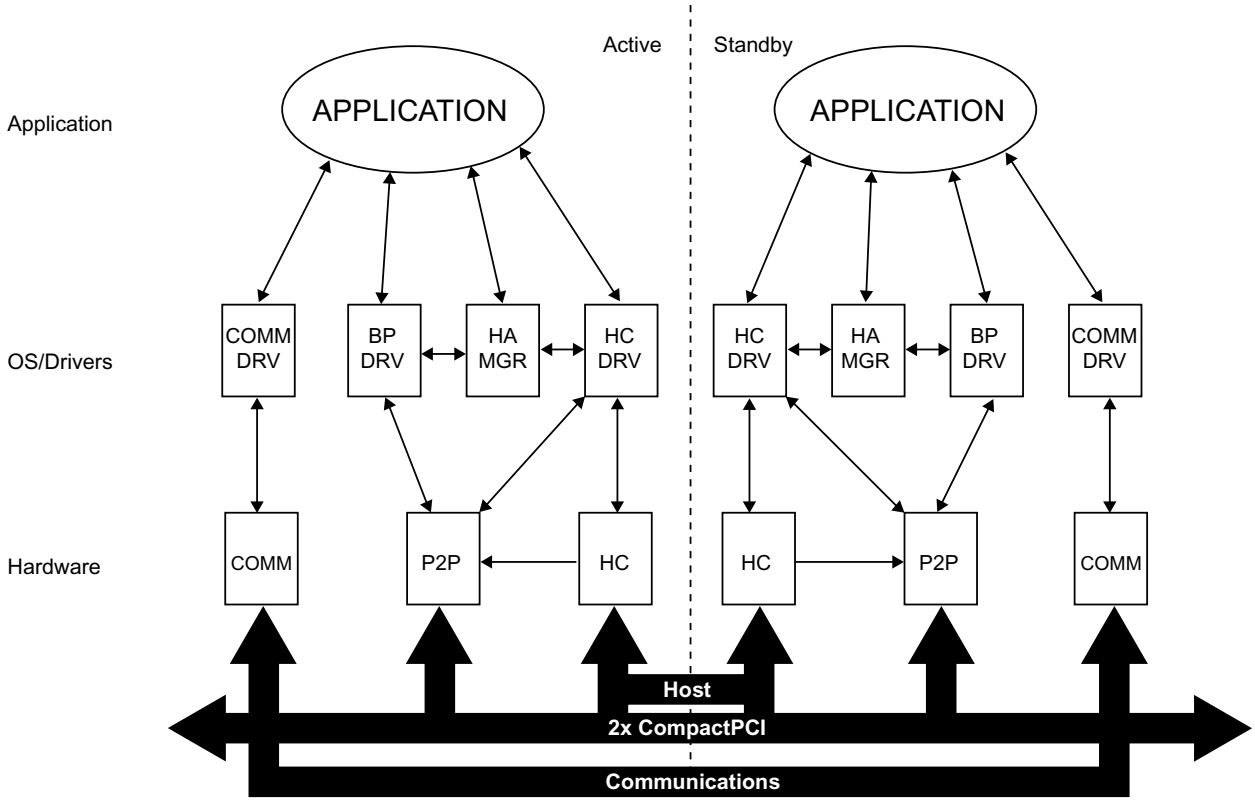
System CPUs

HA CPUs are fully PC compatible and support an optional carrier board providing I/O expansion capability.

Each redundant HA CPU provides a communications channel (COMM) for inter-CPU messaging, fault detection, and data base synchronization. It is based on 100Mbps Ethernet hardware and utilizes a standard communications driver (COMM DRV).

Interface to the dual CompactPCI buses is provided by PCI-to-PCI (P2P) bridges. The Host Controller (HC) controls these bridges such that on an inactive bus segment the P2P is isolated from the backplane. Arbitration of the CompactPCI buses is provided by additional logic within the HC.

HA CPU Architecture

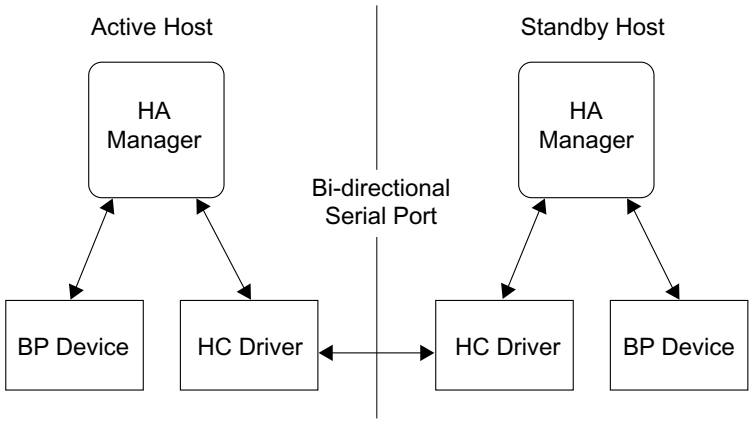


Software Considerations

The five software components in Intel's High Availability System are listed and illustrated below and discussed in the following topics.

- Application
- Host Controller Driver (HC.DRV)
- Communications Drivers (COMM.DRV)
- HA Manager (HA.MGR)
- Backplane Device Drivers (BP.DRV)

Inter-Host Communication Architecture



Application

The application is system-specific and supplied by the customer. The application supports operation in Active, Standby, or Split mode (Revision D and later boards), database synchronization, and communication with the HC, HA and BP drivers.

Since the host application is customer-specific, you will not know in advance what tasks it has been designed to perform. However, in order to work in Intel's HA system, the application will require certain attributes, including:

- The host application on one Redundant Host must maintain synchronization with the host application on the second Redundant Host. This might simply mean maintaining redundant databases, or other resource management.
- While the host application is not required to coordinate peripheral initialization or any other PCI configuration issues during a takeover, it should be ready (depending on the application) to continue processing when a takeover occurs so that few, if any, transactions are lost.

Host Controller Driver (HC.DRV) and Host Controller

The task of controlling an HA system is performed mostly by the Host Controller and the Host Controller Driver (HC.DRV). The HA Host Controller (HC) is a CompactPCI target device. The Host Controller is responsible for controlling:

- Live insertion and removal of system boards
- Backplane bus maintenance
- Active Host fault detection and processor board level isolation strategy

Working together, the Host Controller Driver and the Host Controller device provide:

- Failure Detection - either hardware or software
- Failure Isolation - to keep the failure from affecting the rest of the system
- Failure Identification - identify what went wrong in order to fix it
- Remediation - executing a takeover (switching to Redundant CPU)
- Re-Alignment - reconfiguration of redundant unit

The HC driver also provides a means of allowing a host application to:

- Access the Host Controller's diagnostics
- Access and modify the Host Controller's fault isolation and recovery strategy
- Access and modify the Host Controller's watchdog characteristics

High Availability Manager (HA.MGR) and Host Controller

The HA Manager (HA.MGR) is an Intel supplied virtual driver that manages some of the high level functions within a high availability system. These functions include hot swapping CPUs or peripherals, watchdog timer, and event logging for system management.

The Host Controller is also responsible for transmitting peripheral device configuration information from one domain to another (for instance, Active system communicates to the Standby system). A Kernel Level process in each domain is responsible for distributing data packets received from the host controller through a bi-directional serial (BDS) communication port. The High Availability Manager handles this task.

The transmitted message packets contain information usually pertaining to resource configurations of devices residing in the opposite domain. This configuration information could refer to the PCI bridge memory frame, I/O ports, DMA channels, or allocated IRQs. Through the BDS, the Standby HA Manager receives from the Active domain configuration data, which it then sends to each of its drivers (or their associated device objects) in order to create mirror images of the drivers on the Active Host.

Standard Communications Driver (COMM.DRV)

A standard communications driver (COMM.DRV) is used with 100Mbps Ethernet hardware to provide inter-CPU messaging, fault detection, and database synchronization between the Active and Standby domains.

Backplane Device Drivers (BP.DRV)

Backplane Device Drivers (BP.DRV) are customer-supplied and comply with the Intel-provided HA driver guidelines listed below. These guidelines allow the drivers to communicate with peripherals during normal and takeover conditions.

- Ready State Initialization
- HA/Takeover Capable
- Hot Swap Aware

Ready State Initialization

Upon boot up, drivers and devices on the Active Host are fully initialized as they would be in a non-HA system. But because a Redundant Host that is inactive on a segment has no visibility past its local P2P bridge, its devices and drivers must be designed to partially initialize up to a “ready state”; that is, given as much configuration information as is readily available about the system’s backplane devices.

Prior to a takeover, configuration data unavailable to the Standby Host due to its bus isolation is passed to it from the Active Host through the BDS for handling by the HA Manager. The HA Manager then in turn passes the configuration packets to the respective device drivers on the Standby Host so that the device object structures can be fully initialized.

HA/Takeover Capable

During a takeover, the Standby Host’s device driver performs the following functions:

1. The Standby Host’s backplane device driver must disable bus mastering of all backplane devices to prevent data flooding. When a Standby Host takes over, the data packets being passed along the backplane may be in an unknown state. Therefore, the backplane device driver disables the PCI arbiter and revokes all grants on the PCI bus.

2. The backplane device driver must then complete its own initialization process, and cleanup any outstanding queues and/or actions that were in process when the takeover was initiated.

3. After the backplane device driver completes initialization and device cleanup has been performed, bus mastering may be re-enabled.

The main difference between a driver on the Active Host and a driver on the Standby Host is that the Active Host side driver must initialize the peripheral’s chipset. The Standby Host

driver, on the other hand, inherits during a takeover an initialized board and completes driver initialization before continuing normal activities.

Hot Swap Awareness

Since High Availability systems require hot swappable peripherals, the customer-supplied device drivers must be hot swap aware and configure themselves accordingly. A hot swap device driver is able to detect the removal of its device object through a bus-generated interrupt and to notify the host application.

Following reinsertion of a new device, another interrupt is generated and the device driver initializes the peripheral board's chipset, re-enables bus mastering, notifies the host application (if applicable), and resumes normal operation. The system resources previously allocated to the removed board remain the same so that the new device can operate correctly.

Frequently Asked Questions

Q: Will a dual CPU system require switching out the backplane, or does the current backplane accommodate the future addition of two CPUs?

A: Intel's HA approach utilizes a dual system slot backplane, meaning that existing non-HA backplanes will need to be switched out because they do not have multiple "System Slots".

Q: What family of Intel processors is Intel utilizing?

A: The Pentium III 500 MHz Mobile Module processors from Intel's Embedded Processor group. These processors require very low operating power while providing high performance. Also, future processors will offer increased performance.

Q: Will the system support Symmetric Multiprocessing (SMP) across the two CPU boards?

A: SMP will not be supported across the two CPU boards.

Q: Do the CPUs load share?

A: In an Active-Standby configuration, with one board active on both segments, the Active CPU board has access to all peripheral slots. Any bus master on either CompactPCI bus segment can communicate directly with any other peripheral on its bus segment or through the Active CPU (transparently) to any other peripheral on the other bus segment. However, the two CPUs do not interleave bus transactions; one or the other is in control of the bus at all times.

Though the Standby CPU is isolated from the backplane, it is not idle: it can receive program execution information over the ENET connection, perform independent on-board I/O, verify correct program execution on the other CPU, maintain data tables or data bases, etc.

When the boards are configured for Active-Active mode (Revision D and later boards), each CPU has control of one bus segment and thus the loading is naturally more evenly distributed. Any bus master on a CompactPCI bus segment can communicate directly with any peripheral on its own bus segment.

Q: How does the system support data concurrency between the two processor boards?

A: It is the application's responsibility to maintain program concurrency to the desired resolution via dedicated 100BASE-T Ethernet connections.

Q: How does the system support accurate Program Counter (PC) transference?

A: PC resolution between the two CPU boards is not provided. The application provides data and status information for program resumption after a takeover occurs.

Q: What causes a takeover?

A: There are many conditions under which a takeover can occur: a watchdog timer time-out on either CPU, a hardware fault detection on the Active processor, and many more. All of these are software configurable in software protected logic within the Host Controller logic.

Q: What is the takeover sequence?

A:

a) Takeover initiated, caused by hardware fault or software.

b) For Active-Standby mode, the once Standby CPU becomes the currently Active CPU and if the failed, once Active, CPU survives the takeover it becomes the Standby CPU. For Active-Active mode (Revision D and later boards), one CPU assumes an Active mode on both segments and the other CPU becomes the Standby CPU.

c) The Host Controller disables grants to backplane devices.

d) The Host Controller notifies the HA Managers on both hosts that a takeover has occurred.

e) The new Standby CPU HA Manager sends IRP_MN_HALT_DEVICE to all backplane drivers on the new Standby CPU. This happens only if the new Standby CPU was able to survive the takeover (i.e., takeover does not cause a power down or reset of the new Standby CPU).

f) The new Active CPU HA Manager disables bus mastering on all backplane devices and re-enables grants to backplane devices.

g) The new Active CPU HA Manager sends IRP_MN_START_DEVICE to all backplane drivers on the new Active CPU.

h) The new Active CPU HA Manager enables backplane interrupt after all backplane drivers have completed IRP_MN_START_DEVICE.

Q: What is required to develop a working system?

A:

a. Define for your application the points of synchronization that must be maintained between the Active and Standby CPU.

b. When developing your takeover strategy, determine what to write to the host controller configuration registers.

c. Provide drivers for your custom CompactPCI cards based on Intel's High Availability driver model.

d. In order to communicate with the hot Standby CPU, develop an application capable of interfacing with the Intel provided ENET drivers.

Q: What is the best-case for processor switchover time?

A: Assuming that the Standby processor is in step (for instance, the OS is up and running and all drivers are installed), hardware switch over time is on the order of microseconds.

Software latency contributes to the bulk of switchover time delays in a worst-case scenario. This time is spent getting the newly Active CPU to the point where the previously Active CPU was executing.

Assuming that the takeover was caused by a fault detection, time would be spent power cycling the faulted processor in order to execute the hardware diagnostics and load the OS and device drivers before the application could resume operation.

Q: What is the performance impact of keeping the Standby processor board updated?

A: On the CompactPCI bus there is no performance impact. But, as the question implies, the Active CPU board must pay the overhead associated with maintaining contact with the Standby processor via Ethernet.

While the amount of overhead depends on the application, in general it is a trade off between the degree of synchronization during normal operation and the amount of catch up the newly Active CPU must do during a takeover: greater synchronization means more ongoing overhead but probably a smoother takeover; less ongoing synchronization means less ongoing overhead but a potentially bumpier takeover.

Q: Is the dual processor board solution fault tolerant?

A: This depends on one's definition of fault tolerant. Yes, a redundant CPU system can tolerate faults in the following ways: the newly Active CPU can isolate a failed, formerly Active CPU. The failed, formerly Active CPU can be isolated from the backplane or it can be powered down.

The ability to power down and power up the system allows diagnostics to be run to determine if the takeover occurred for a hardware or a software reason. If the takeover

occurred due to software, the CPU may again be functional and not need to be replaced. If the takeover occurred due to faulty hardware, it will need service.

At the system level, the backplane is a potential single point of failure; however, 99.999% availability for the system is still achievable.

Q: How does clustering compare with what you are doing?

A: A cluster is defined here as a group of autonomous desktop servers that work together as a single system. Autonomous means they have everything they need to be standalone, particularly processors, memory, storage, and peripherals.

Advantages of clusters include multiple commercial sources, ease of implementation, N+1 redundancy, and scalability. Scalability means that you can expand a cluster's aggregate processing power by adding systems to the cluster, either for increasing job speed, or for accommodating tasks involving higher transaction volume. Cluster disadvantages include incremental loss in processing power if a node fails, expensive peripheral duplication if the application requires a lot of I/O, and the takeover time can be on the order of 30-90 s.

In contrast, the high availability N+1 peripheral architecture described here is ideal for OEMs building unique servers with custom and typically expensive peripherals. The N+1 architecture's advantages include reduced cost if many peripherals are needed, smaller system envelope, quick take over times, and all hot-swappable components. Disadvantages include higher system development time because drivers need modification and application code must maintain synchronization.

ZT 5550 CPUs operating in Active-Active mode exhibit cluster characteristics due to the isolated bus segments. Failover control can provide for recovery of a down CPU segment; locked split mode can preserve true cluster operation.

Q: How does Intel's HA system fit into the PICMG High Availability proposal?

A: Directly, it doesn't. The CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0 definition for High Availability addresses only peripherals, not CPUs or HA systems. But our hot swappable CPUs can be replaced without halting system operation. We also support the entire three-tier hot swap definition given in the Hot Swap Specification (basic, full and high availability).

In our solution, peripherals wanting to be hot swapped are automatically detected by the CPU and the application is notified. Finally, our high availability backplane supports the enable and health signals in anticipation of a future interface to these signals.

5. Hot Swap

This chapter describes some of the features of CompactPCI Hot Swap as they apply to the ZT 5550. For a complete definition of CompactPCI Hot Swap, obtain a copy of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*, available for a nominal fee from PICMG at http://www.picmg.org.

What is Hot Swap?

Hot Swap was added to the CompactPCI standard to allow for the orderly insertion and extraction of boards without adversely affecting system operation. The Hot Swap capability is necessary in order to repair faulty boards or reconfigure a system. The PICMG Hot Swap subcommittee released the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*.

Definition of Hot Swap Terminology

Several Hot Swap-specific terms are defined below. Two of these terms (Pin Staging and Power Ramping) are described more fully in the following topics.

Basic Hot Swap: A system meeting the basic Hot Swap requirement of *pin staging* and *power ramping*. The ZT 5550 implements pin staging to facilitate power ramping to avoid glitching backplane power when accidentally removed and inserted.

Full Hot Swap: A system utilizing the *dynamic configuration* features of the CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0. Boards meeting the Full Hot Swap requirements have the following hardware: a hot swap “Control and Status Register,” capability to drive the “ENUM” signal, a blue LED, and an ejector switch connected to the operation of the ejector handle. These requirements are for peripheral boards and do not apply to the ZT 5550.

High Availability: An attribute of a system designed to continue running (maintaining availability) in the event of a system component failure.

Pin Staging: The *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0* describes a specific arrangement of CompactPCI connector pin lengths. Three lengths are specified. Long pins engage first (disengage last), medium pins engage second, and short pins engage last (disengage first). Refer to the following topic "Pin Staging".

Power Ramping: The back end power is ramped up at a controlled rate upon board insertion. This voltage ramping limits the surge currents induced on the operating CompactPCI system. See the following topic "Power Ramping" for more information.

Pin Staging

The *CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0* defines a set of staged (multi-length) pins in the CompactPCI connector that cause connections to be made in an orderly fashion when inserting a card. Likewise, when a card is removed, the connections

are broken in a reverse order. The ZT 5550 takes advantage of this pin staging. The order of pin contact is described below:

1. **Long length pins** contact first (disengage last) to supply “Early Power” to interface circuitry on the ZT 5550. These pins are +5V, +3.3V, GND, and VIO. Special circuitry powered from these pins applies a 1V “precharge” voltage to the PCI signals *before* they make contact with the bused PCI signals on the backplane.

2. **Medium length pins** contact second as the board is inserted and are the precharged PCI signal pins. The precharge voltage keeps the pin and gate capacitance from causing transients on the PCI bus that might corrupt PCI transactions.

3. **Short length pins** contact third (disengage first) as the board is fully inserted. After these pins contact, the board is allowed to power-up. The back-end power is ramped up to avoid “glitching” the system's DC bus. All four voltages are ramped (+5V, +3.3V, +12V, -12V). On the ZT 5550, these voltages are at their final value within 100ms after the board is fully inserted.

Power Ramping

The System Master drives the CompactPCI clock signals and provides backplane arbitration. If these functions are not provided in a redundant manner (as in an HA system), removing the System Master prevents the remaining boards in the system from operating properly along the CompactPCI bus, even if one or more of the peripheral boards support hot-swapping.

However, some systems are designed to allow peripheral boards to operate independently from the CompactPCI bus (as in a system implementing the telecommunications TDM bus). If the System Master is removed accidentally from such a system during field service, the peripheral boards continue to operate as long as the power is not disrupted by the reinsertion of the System Master. To prevent power disruption (glitching) during reinsertion, the ZT 5550 provides power ramping.

6. Reset

This chapter discusses the various reset types and reset sources on the ZT 5550. Because many embedded systems have different requirements for board reset functions, the incorporation of this sub-system on the ZT 5550 is designed to provide maximum flexibility.

Reset Types and Sources

The ZT 5550's reset types are listed below. The sources for each reset type are detailed in the following topics.

- **Master Reset:** All on-board devices are reset. If this occurs on the Active CPU, and a Standby CPU is available in the system, a takeover occurs. If a Master Reset occurs on the Active CPU or if no Standby is available, PCIRST# is driven on the backplane.
- **Backend Power Down:** The backend logic is powered off and a hard reset occurs. If this occurs on the Active CPU, and a Standby CPU is available in the system, a takeover occurs.
- **Hard Reset:** All on-board devices except the Host Controller are reset. If this occurs on the Active CPU, PCIRST# is driven on the backplane. The HC can be configured to perform a takeover if a hard reset occurs on the Active CPU.
- **Soft Reset:** CPU initialization only. Other devices are not reset.
- **NMI:** Non-maskable interrupt. Though not a reset in the strict sense, an NMI can have the same effect as other resets.

Master Reset Sources

In a non-HA system, a Master Reset occurs in the event of any of the hard reset sources below except for a PIIX4 Reset Control Register reset. In an HA system, the ZT 5550 has two potential Master Reset Sources.

Self Reset

When the Master Reset Command bit is set in the Host Control Command Register in the HC, a Master Reset occurs. If this occurs on the Active CPU, and a Standby CPU is available in the system, a takeover occurs. Refer to the *ZT 5550 High Availability Software Manual for Windows NT* for information on using this function.

HA Reset (J5-C17)

The HA Reset may be asserted by the redundant CPU. A Standby CPU may assert this reset to the local CPU in the event of a failed takeover attempt to force the HC into reset. An Active CPU may assert this reset to a Standby by setting the Reset Standby bit in the

Host Control Command Register in the HC. Refer to the *ZT 5550 High Availability Software Manual for Windows NT* for information on using this function.

Backend Power Down Sources

Backend power down sources will hold the rest of the ZT 5550 in hard reset during board extraction, low voltage, or overcurrent fault conditions

Board Extraction

When a board is extracted from an enclosure (specifically, when the short “board select” pin is disengaged or de-asserted by the redundant CPU), the Hot Swap controller unconditionally removes backend power from the board, turns off the “Fault/Power” LED, and holds the ZT 5550 in reset.

Low Voltage

When the 3.3V, 5V, and 12V supply voltages are detected to be below an acceptable operating limit, the Hot Swap controller unconditionally removes backend power from the board, turns off the “Fault/Power” LED, and holds the ZT 5550 in reset.

Overcurrent Fault

If a power fault condition (overcurrent) is detected, the Hot Swap controller removes backend power and turns the “Fault/Power” LED indicator red. The ZT 5550 is held in reset.

Hard Reset Sources

There are several hard reset sources on the ZT 5550. Each of these sources (in some cases, if enabled) cause the PIIX4 to assert several hardware reset signals on the board. These signals include the CPURST (CPU reset), PCIRST# (CompactPCI reset), and the RSTDRV (ISA reset).

After assertion, the CPU reboots and begins instruction execution from FFFFFFF0h (the boot vector). In an HA system, backplane PCIRST# can be individually masked or asserted in the HC. Refer to the *ZT 5550 High Availability Software Manual for Windows* for information on backplane resets. Hard reset sources include the following.

Watchdog Timer Second Stage Timeout (System Register Address 79h)

The watchdog timer is programmable to generate a hard reset if it is not strobed within 250ms after a first stage time-out. The watchdog timer’s “Control and Status Register” (System Register 2, Port 79h) allows the BIOS or user applications to determine if the source of the most recent reset was the watchdog second stage time-out. See Chapter 9, “Watchdog Timer,” for more information.

CompactPCI Bus Push-Button Reset Signal, PRST# (J2-C17)

Asserting the PRST# signal from the CompactPCI backplane causes a hard reset. This functionality may be disabled individually for an Active or Standby CPU.

If you are using Windows NT Operating system, refer to the *ZT 5550 High Availability Software Manual for Windows NT* for information on disabling this function.

If you are using VxWorks Operating System, refer to the *Redundant System Slot* Software User Manual for information on disabling this function.

Push-Button Resets Held for Longer Than 2 s

When depressed for longer than 2 s, the SW1 push-button on the ZT 5550 and the ZT 4804 RPIO (J3-A4) boards generate a hard reset. Depressing either of these buttons for less than 2 s generates a soft reset, or NMI, described below.

System Register CF9h (PIIX4 Reset Control Register)

Bits 1 and 2 in this register are used by the PIIX4 to generate a hard reset or a soft reset. During a hard reset, the PIIX4 asserts CPURST, PCIRST#, and RSTDRV, and resets its core and suspend well logic. The topic "PIIX4" in Appendix E, “Data Sheet Reference,” provides a link to the PIIX4 data sheet.

Soft Reset Sources

There are several sources for soft resets on the ZT 5550. These include:

Watchdog Timer First Stage Timeout (System Register Address 79h)

The watchdog timer is programmable to generate a first stage timeout if it is not strobed within a programmable time-out period. When SW3-4 is open and a first stage timeout occurs, an INIT is issued to the CPU.

The watchdog timer’s “Control and Status Register” (System Register 2, Port 79h) allows the BIOS or user applications to determine the source of a particular reset (watchdog time out, power up, power out-of-range/low voltage, etc.). See Chapter 9, “Watchdog Timer,” for more information.

System Register CF9h (PIIX4 Reset Control Register)

Bits 1 and 2 in this register are used by the PIIX4 to generate a hard reset or a soft reset. During a soft reset, the PIIX4 asserts INIT to the CPU. This causes the processor to enter “real mode”, initialize its internal registers, and begin instruction execution from FFFFFFF0h (the boot vector).

The "PIIX4" topic in Appendix E, “Data Sheet Reference,” provides a link to the PIIX4 data sheet.

Push-Button Resets Held Less than 2 s

When depressed for less than 2 s, the SW1 push-buttons on the CPU and the ZT 4804 RPIO board generate a soft reset or an NMI, depending on the configuration of SW3-4. When SW3-4 is closed, an NMI is issued to the CPU; when SW3-4 is open, an INIT is issued to the CPU.

Keyboard Controller Reset

The keyboard controller generates a keyboard controller reset when FEh is written to port 64h. This causes the PIIX4 to assert INIT to the CPU.

Keyboard CTRL-ALT-DEL

Simultaneously pressing these keys calls a BIOS function that reboots the system.

Note: This method does not work under operating systems that trap calls to this BIOS function.

NMI Sources

The PIIX4 is configured by default to generate an NMI to the CPU when it detects an IOCHK from the ISA bus or when it detects a SERR# or PERR# from the PCI bus. While there are many potential sources for SERR# or PERR#, the following sources assert IOCHK:

Watchdog Timer First Stage Timeout (System Register Address 79h)

The watchdog timer is programmable to generate a first stage timeout if it is not strobed within a programmable time-out period. When SW3-4 is closed and a first stage timeout occurs, an NMI is issued to the CPU. The watchdog timer's "Control and Status Register" (System Register 2, Port 79h) allows the BIOS or user applications to determine the source of a particular reset, such as watchdog time out, power up, or power out-of-range/low voltage. See Chapter 9, "Watchdog Timer," for more information.

Push-button Resets Held Less than 2 s

When depressed and released in less than 2 s, the SW1 push buttons on the CPU and the ZT 4804 RPIO board generate a soft reset or an NMI, depending on the configuration of SW3-4. When SW3-4 is closed, an NMI is issued to the CPU; when SW3-4 is open, an INIT is issued to the CPU.

7. System Monitoring and Alarms

The ZT 5550 performs system monitoring and alarming functions using the flexible, industry standard System Management Bus (SMBus). The SMBus consists of a two-wire interface and an alert signal. This two-wire interface is based on the I^2C (ACCESS.bus) interface to provide messages to and from devices. Each device has an associated address on the bus and may interrupt the processor using the alert signal.

The SMBus devices reside on the ZT 5550 CPU, the optional ZT 4804 RPIO Transition Board, and on certain backplanes. The table below provides an overview of the device locations and functions for CPU monitoring and RPIO monitoring. The SMBus driver from Intel provides an API interface for each device. Refer to the *ZT 5083 System Management High Availability Software User Manual* for more information.

The ZT 5550 has circuitry on board for monitoring the output of an optional fan-sink tachometer. The tachometer output is routed to connector J27, pin 3. The fan tachometer output pulses as the fan rotates. The pulsing fan tachometer output is routed directly to the DS1780 System Health Monitor device. Most fan tachometers have an output rate of approximately 100 Hz; this input therefore changes states approximately every 5ms.

SMBus Address Map

The table below lists the location, function, and address of each SMBus device used on the ZT 5550 and the ZT 4804 RPIO boards.

Device	**ZT 5550 CPU Function**	**Address**
PCF8574(#1)	Power supply DEG and FAL monitoring ACO input monitoring Visual critical, major, and minor LED indicator control	0100 010
DS1780	CPU voltage and temperature monitoring	0101 111
SDRAM DIMM (1 and 2)	Signal Presence Detect (SPD) PROM in DIMM #1 Signal Presence Detect (SPD) PROM in DIMM #2	1010 000 1010 001
MAX 1617	Module and processor core temperature monitoring	1001 110
CY2310NZ	Clock generator	1101 001
Device	**ZT 4804 RPIO Function**	**Address**
PCF8574(#2)	Audio/visual critical, major, and minor relay output controls Visual critical, major, and minor LED indicator controls	0100 000
PCF8574(#3)	Two external optically isolated user inputs ACO input switch (on/off) monitoring	0100 001

8. Enhanced IDE Controller

This chapter provides an introduction to the ZT 5550's Enhanced IDE Controller. It covers the ZT 5550's support for remote or internal EIDE disk drives.

The ZT 5550's EIDE controller provides two EIDE channels for interfacing with up to four drives. The EIDE controller is incorporated into the Intel PIIX4E (82371EB) chipset, thus it utilizes the Peripheral Component Interconnect (PCI) bus to give exceptional EIDE performance. The EIDE controller can sustain a maximum transfer rate of 33 MB/s between the EIDE drive buffer and PCI. The "PIIX4" topic in Appendix E, “Data Sheet Reference,” provides a link to the PIIX4 data sheet.

Features of the EIDE Controller

- IBM-AT compatible
- Supports PIO and Bus Master EIDE
- On-board CompactFlash EIDE flash drive
- “Ultra DMA/33” Synchronous DMA Operation
- Bus Master IDE transfers up to 33 MB/s
- Individual software control for each EIDE channel
- 32-bit, 33 MHz, high performance PCI bus interface
- Primary and Secondary channels for interfacing up to four devices

Disk Drive Support

The ZT 5550 supports internal and external EIDE disks drives. These configurations are described below. The “Identifying Media Options” topic in Chapter 2 describes many disk drive connection options that may be available depending on the boards in your system.

Note: Configuration of switch SW5-3 and cuttable trace CT79 may be required for proper EIDE operation.

Internal Disks

The ZT 5550 supports two configurations for internal EIDE disk drives:

The **CompactFlash** option (see topic below) directs the EIDE primary channel to J9, a CompactFlash connector supporting a flash memory card configured as solid state drive.

The **I/O Expansion** option directs the EIDE primary channel through the I/O Expansion connector J6 to a drive mounted on an Intel I/O Expansion Board.

External Disks

The CPU's secondary EIDE channel is routed out rear-panel I/O connector J3 and, depending on the boards in your system, may be accessible at:

- An internal 40-pin IDE connector on certain RPIO boards.
- A 40-pin latching ribbon cable connector on the back side of certain backplanes.
- A Utility Board installed in a peripheral slot.

I/O Mapping

The I/O map for the EIDE interface varies depending on the mode of operation. The default mode is "compatibility mode," meaning that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h and interrupt IRQ15. No memory addresses are used.

CompactFlash Option

The ZT 5550 provides on-board solid state IDE capability through CompactFlash connector J9, a 50-position right angle surface mount header. This connector is designed to accommodate CompactFlash expansion cards which appear to the system as a hard drive and are automatically supported by most operating systems.

Master/slave status is configured through SW5-3. The CompactFlash card must be configured as the master IDE device, unless you have an IOX board carrying a hard drive configured as the master IDE device (usually this means it is unjumpered).

If the drive on the IOX board is jumpered for "Cable Select", the master/slave relationship between the drives is toggled through SW5-3. Changes to master/slave status automatically appear in the BIOS Setup utility. The ZT 5550 is shipped with no device installed in J9, therefore SW5-3 is open by default (slave operation) in case your order includes an IOX board implementing a hard drive.

CompactFlash Input Characteristics

By default, the ZT 5550's CompactFlash socket (J9) is set to 5.0V operation (CT79 in position A). This setting requires the CompactFlash card to have "Type 2" or "Type 3" input characteristics, as shown in the "CompactFlash Input Characteristics" table below. SanDisk currently manufactures cards meeting these specifications. Since most 2.5" disk drives require VCC = 5.0V, setting J9 to this voltage has the advantage of allowing master/slave operation between a CompactFlash card and a 2.5" drive mounted on an IOX board.

CompactFlash Input Characteristics Table

Type	Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
			VCC = 3.3 (CT79B)[1]			VCC = 5.0 (CT79A)[2]			
1	Input Voltage CMOS	Vih Vil	2.4		 0.6	4.0		 0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		 0.6	2.0		 0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

This table is based on one provided in the *CompactFlash Specification Revision 1.3*. The shaded area represents operation not supported on the ZT 5550.

Notes:

[1] Factory default configuration.

[2] CompactFlash cards with “Type 1” input characteristics (operating from VCC = 5.0V) should not be used because the 4.0V minimum input voltage requirement is not met by the ZT 5550 (ZT 5550 EIDE channels V_{OH} = 2.8V).

Caution: If the CompactFlash socket (J9) is set for VCC = 3.3V operation (CT79 is in the B position), *do not connect a disk drive on the ZT 96072 or the ZT 96073 I/O Expansion Boards. Doing so will damage the CompactFlash device!*

Device Drivers

The EIDE interface works with all applications by default. To fully utilize the EIDE interface, you may install additional drivers to increase the performance under MS-DOS*, Windows 3.X, Windows 95, Windows NT, IBM OS/2*, SCO*, UNIX* and Novell* Netware*. Contact the vendors of individual operating systems for the latest drivers for the Intel PIIX4E (82371EB) EIDE interface.

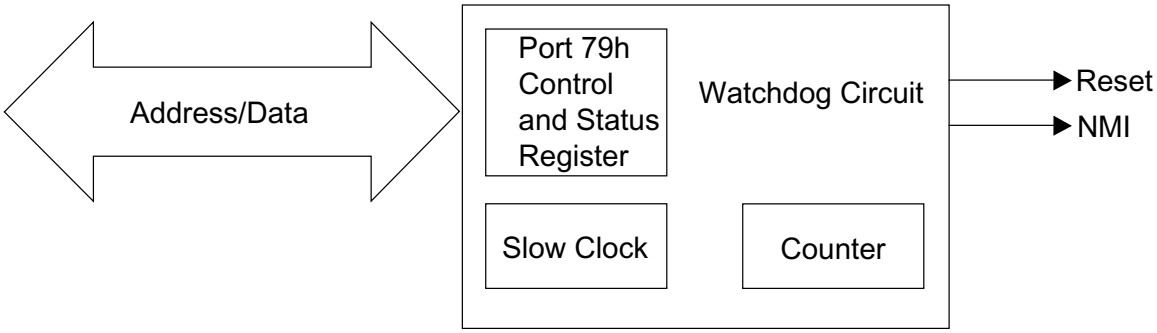
Note: You may have difficulty installing the QNX* operating system, ver. 4.24, on CompactFlash cards. If problems occur, restart the install program and specify regular IDE drivers (Fsys.ide) instead of the default EIDE drivers (Fsys.eide).

9. Watchdog Timer

The primary function of the watchdog timer is to monitor ZT 5550 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are:

- Programmable two-stage timeout
- Enabled and disabled through software control
- Armed and strobed through software control

Watchdog Timer Architecture



Watchdog Timer Operation

The ZT 5550's custom watchdog timer circuit is implemented in the High Availability Host Controller. The watchdog timer contains a “Control and Status Register” (documented in this manual as System Register 2, Port 79h). The register allows the BIOS or user applications to determine if the source of the most recent reset was a watchdog time out. When the watchdog times out, T1 is driven first, followed by T2 250 ms later. Watchdog T1 and T2 can be independently disabled.

The first-stage timeout (T1) results in an NMI or a CPUINIT, depending on the position of SW3-4. When this switch is closed, CPUINIT is asserted; when open, NMI is asserted. The second-stage (T2) results in a hard reset.

Eight T1 timeout intervals are selectable through bits 0-2 of the register. Minimum timeout period = 250ms. Maximum timeout period = 256 s. The watchdog is strobed by reading the register. This restarts the timer.

Power Up Initialization

The watchdog timer's programmable logic is only initialized by power-on reset. This ensures that the T1, T2, T1 ENABLE, and T2 ENABLE status and control bits power up to

deasserted states, allowing the BIOS or user applications to determine if the most recent reset source was the second-stage (T2) watchdog timeout.

Time Out Values

The watchdog timer has its own separate slow clock source that runs at a maximum frequency of 32 Hz. The watchdog is guaranteed to timeout in no less than the programmed minimum value.

Using the Watchdog in an Application

The following topics are provided to help you learn how to use the watchdog in an application. The watchdog's T1 and T2 functions are described and sample code is provided. T1 and T2 are controlled through the watchdog's "Control and Status Register" (documented in this manual as System Register 2, Port 79h).

Watchdog Reset

An application using the reset feature enables the watchdog reset, sets the terminal count period, then periodically strobes the watchdog to keep it from resetting the system. If a strobe is missed, the watchdog assumes that an application error has occurred and resets the system hardware.

Enabling the Watchdog Reset

C code for enabling the watchdog reset might look like the following:

```
#define WD_RESET_EN_BIT_SET      0x20

void EnableWatchdogReset(void){
   Unsigned char WdValue;               // Holds watchdog register values.
                                        //
   WdValue = inb(WD_CSR_IO_ADDRESS);    // Read the current contents of the watchdog
                                        // register.
   WdValue |= WD_RESET_EN_BIT_SET;      // Assert the enable bit in the local copy.
   outb(WD_CSR_IO_ADDRESS,WdValue);     // Assert the enable in the watchdog
                                        // register.
}
```

Setting the Terminal Count

The terminal count determines how long the watchdog waits for a strobe before resetting the hardware. C code for setting the terminal count might look like the following:

```
#define WD_CSR_IO_ADDRESS        0x79    // IO address of the watchdog
#define WD_T_COUNT_MASK   0x07    // Bit mask for terminal count bits.
#define WD_500MS_T_COUNT  0x01    // Terminal count values . . . .
#define WD_1S_T_COUNT             0x00    //
#define WD_250MS_T_COUNT  0x00    //
.
.
.
void SetTerminalCount(void){
   Unsigned char WdValue;                // Holds watchdog register values.
                                         //
   WdValue = inb(WD_CSR_IO_ADDRESS);     // Get the current contents of the watchdog
                                         // register.
   WdValue &= ~ WD_T_COUNT_MASK;         // Mask out the terminal count bits.
   WdValue |= WD_500MS_T_COUNT;          // Set the desired terminal count.
   outb(WD_CSR_IO_ADDRESS,WdValue);      // Furnish the watchdog register with the new
                                         // count value.
}
```

Strobing the Watchdog

Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid resetting the system hardware. C code to strobe the watchdog might look like the following:

```
void StrobeWatchdog(void){
   Inb(WD_CSR_IO_ADDRESS);               // A single read is all it takes.
}
```

Watchdog NMI

When enabled, an NMI precedes a watchdog reset by 250 ms. The NMI generation feature gives the application 250 ms to perform essential tasks before the hardware is reset. Before using watchdog NMI, ensure the following:

- The code for performing the essential tasks is included in an interrupt service routine (ISR).
- The ISR is chained to the existing NMI ISR.
- The watchdog first-stage timeout (T1) is enabled in the “Control and Status Register” (documented in this manual as System Register 2, Port 79h).
- First-stage timeout is configured to assert NMI (SW3-4 = open).

Chaining the ISRs

Save the original NMI ISR vector so that it can be invoked from the new watchdog NMI ISR. Alter the interrupt vector table so that the NMI ISR vector is overwritten with a vector to the watchdog ISR. C code to do this in MS-DOS might look like the following:

```
#define NMI_INTERRUPT_VECTOR_NUMBER 2

void interrupt far (*OldNmiIsr)();


void HookWatchdogIsr(void){

   //
   // To be absolutely certain the interrupt table is not accessed by an NMI (This is
   // quite unlikely.), the application could  disable NMI in the chip set before
   // installing the new vector.
   //
                          .
                          .
                          .
   //
   // Install the new ISR.
   //
   OldNmiIsr = getvect(IsrVector);                          // Save the old vector.
   setvect(NMI_INTERRUPT_VECTOR_NUMBER, WatchdogIsr);   // Install the new.
}
```

Enabling the Watchdog NMI

To activate the NMI feature, enable it in the watchdog register (Port 79h). The code to do this might look like the following:

```
#define WD_NMI_EN_BIT_SET 0x10

void EnableWatchdogNmi(void){

   Unsigned char WdValue;              // Holds watchdog register values.

                                       //

   WdValue = inb(WD_CSR_IO_ADDRESS);   // Read the current contents of the watchdog //
                                       register.

   WdValue |= WD_NMI_EN_BIT_SET;       // Assert the enable bit in the local copy.

   outb(WD_CSR_IO_ADDRESS,WdValue);    // Assert the enable in the watchdog

                                       // register.
}
```

NMI Handler

Because the NMI may have originated from another source such as a RAM Error Correction Code (ECC) error, the NMI handler cannot assume that the NMI occurred due to a watchdog time out. Therefore, the NMI handler must check the watchdog status register before taking watchdog-related emergency action. When the NMI handler completes handling the emergency, it invokes the original NMI Handler (discussed above). The code to do this might look like the following:

```
#define WD_NMI_DETECT_BIT_SET    0x40          // Bit that indicates an NMI occurred, set.
                                               //
void WatchdogIsr(void){                        //
                                               //
   //
        // Did the watchdog cause the NMI?
        //
   if(inb(WD_CSR_IO_ADDRESS) & WD_NMI_DETECT_BIT_SET){
                                               //
           TripAlarm();                        // Take care of essential tasks.
                                               //
           TurnOffTheGas();                    //
   }                                           //
   _chain_intr(OldNmiIsr);                     // Invoke the originally installed ISR.
}
```

Other Watchdog NMI Uses

The watchdog NMI feature can be used independently of the watchdog reset feature. It can also be used without actually causing NMIs. For example, the CPU board could be configured such that the watchdog does not actually drive the NMI line. In this case, in a multi-tasking operating system, one thread could be responsible for strobing the watchdog and a second thread could monitor the NMI bit of the watchdog register. The second thread could then take emergency action if the first thread falters. Code for checking the bit is provided in the “NMI Handler” topic above.

Watchdog INIT

When SW3-4 is closed, a first-stage timeout results in a CPUINIT. This soft reset reinitializes the processor and begins executing the BIOS. This mechanism may be used instead of an NMI which, despite its name, can be masked.

10. Timers

The ZT 5550 provides two custom timers in addition to the standard counter timers contained in the PIIX4 device. These additional timers provide unique functions (listed below) for use by telecommunications applications such as time stamp or periodic interrupt generation.

Each timer consists of a clock source, an initial count register, a down counter, a control register, and an output. The two timers are identical except that Timer 0 has a 32-bit initial count register and counter, and Timer 1 has a 16-bit initial count register and counter.

There are four potential clock sources for each timer, which are selectable in the control register. The available sources include three fixed frequency clocks with periods of 838 ns, 61.035 us, or 488.28 us. The fourth available source is the output from the alternate timer to allow timer cascading for a 48-bit effective timer.

Timer Operation

The initial count register is write only and stores the value that is loaded into the counter. When the counter is loaded and enabled, it begins counting down at the frequency of the selected source. When the counter reaches zero, the output is strobed and the output flag is set on the next rising edge of the clock source.

If the appropriate Timer Interrupt Mask is cleared in the INTM register in the HC, an interrupt is issued. The output flag is cleared automatically after a read of the Timer Control register.

The counter only counts when the Enable bit is set in the Timer Control register. When the counter is not enabled, it does not count down, and it holds its current value until it is reloaded or enabled. When it is enabled, it begins counting down from its current value.

Loading the Counter

The timer can be configured in the Timer Control register to load the initial count into the counter based on three different events:

1. A write to the initial count register

2. A read of the current count

3. When the output is strobed

When the Write Mode bit is set, the counter re-loads after each time the initial count is written into the initial count register. If the Write Mode bit is cleared, writing the initial count does not cause the new initial count to be immediately loaded, but allows the new initial count to be loaded at the next load event.

When the Read Mode field is set to reload, the counter loads whenever the counter is read. Otherwise, a read does not re-load the counter.

The Timeout Mode bit determines what the timer will do when the counter reaches zero. If this bit is cleared, the counter stops counting when it times out. If the bit is set, the counter is reloaded with the value in the initial count register on the rising edge of the clock source following the counter timeout.

If you are using Windows NT Operating System, refer to the *ZT 5550 High Availability Software Manual for Windows NT* for information on how to configure and control these timers according to application requirements.

If you are using VxWorks Operating System, refer to the *Redundant System Slot* Software User Manual for information on how to configure and control these timers according to application requirements.

11. Flash Memory and SRAM

The ZT 5550 implements several non-volatile memory devices supporting a variety of functions. These devices are listed below and described in the following topics.

Flash	4 MB CMOS 5V-only Uniform Sector Flash Memory (AMD 29F032B-120EC)
SRAM:	128 KB Low Power Static RAM (Samsung KM681000CLT-7L)
BIOS Recovery Module:	256 KB 12V Bulk Erase Flash Memory (AMD 28F020-120JC)

Flash

The ZT 5550 provides 4 MB of onboard flash memory and contains the system BIOS. In addition, the flash device may contain space usable for a non-volatile solid state drive. The size of the solid state drive is configurable through the BIOS Setup Utility. A device driver is required for drive emulation. This solid state drive can be used to contain user programs and data; however, since it is a flash memory, it has a limited write cycle life (approximately 1,000,000 cycles). See the *Intel NetStructure Embedded BIOS Software Manual* for more information on the solid state drive and available device drivers.

The flash device is divided into 16 pages mapped into a window in extended memory. Access to the flash disk is transparent to the user and handled by a software driver. The driver used depends on the operating system. Write-protect the flash memory through switch SW5-4.

The BIOS portion of the flash memory is mapped as a 256 KB block in lower memory at C0000h – FFFFFh (768 KB to 1 MB). To reprogram the BIOS or update it if it becomes corrupted, use the FLASH.EXE utility available from Intel and discussed later in this chapter.

The remainder of the flash memory is user programmable. The following information is required for successful flash programming:

1. The base address of the flash window.
2. The size of the flash window.
3. The portions of flash reserved for other purposes.
4. The flash device programming method.
5. How to map a page of flash memory.
6. How to write-protect the flash device through software.

Refer to the “Intel System Information Structure” appendix in the *Intel NetStructure Embedded BIOS* software manual for instructions on how to determine items 1-4. System Register 1 (Port 78h) controls items 5 and 6.

BIOS Recovery Module

The ZT 5550 provides a 256 KB Bulk Erase memory device programmed with the BIOS for use if the ZT 5550's BIOS becomes corrupted. The device allows the board to boot when powered on. The board is shipped with the device pre-installed in a 32-pin socket (T3H1) shown in the “BIOS Recovery Socket Location” figure. System Register 5 (E3h, bit 6) allows software to monitor whether the boot source is the recovery module or the 4 MB onboard flash device discussed in the previous topic.

To boot from the boot socket:

1. Remove the board from the enclosure.
2. Open switch SW5-1 to boot from the BIOS Recovery Module.
3. Make sure flash write protection is disabled (SW5-4 = open).
4. Re-insert the board in the enclosure. After the board powers on, reprogram the on-board flash by using the FLASH.EXE utility (see the “Flash Utility Program” topic below for detailed instructions).
5. After flashing the BIOS, remove the board from the enclosure and close switch SW 5-1.
6. If desired, enable flash write protection (SW5-4 = closed).
7. Re-insert the board in the enclosure.

Flash Utility Program

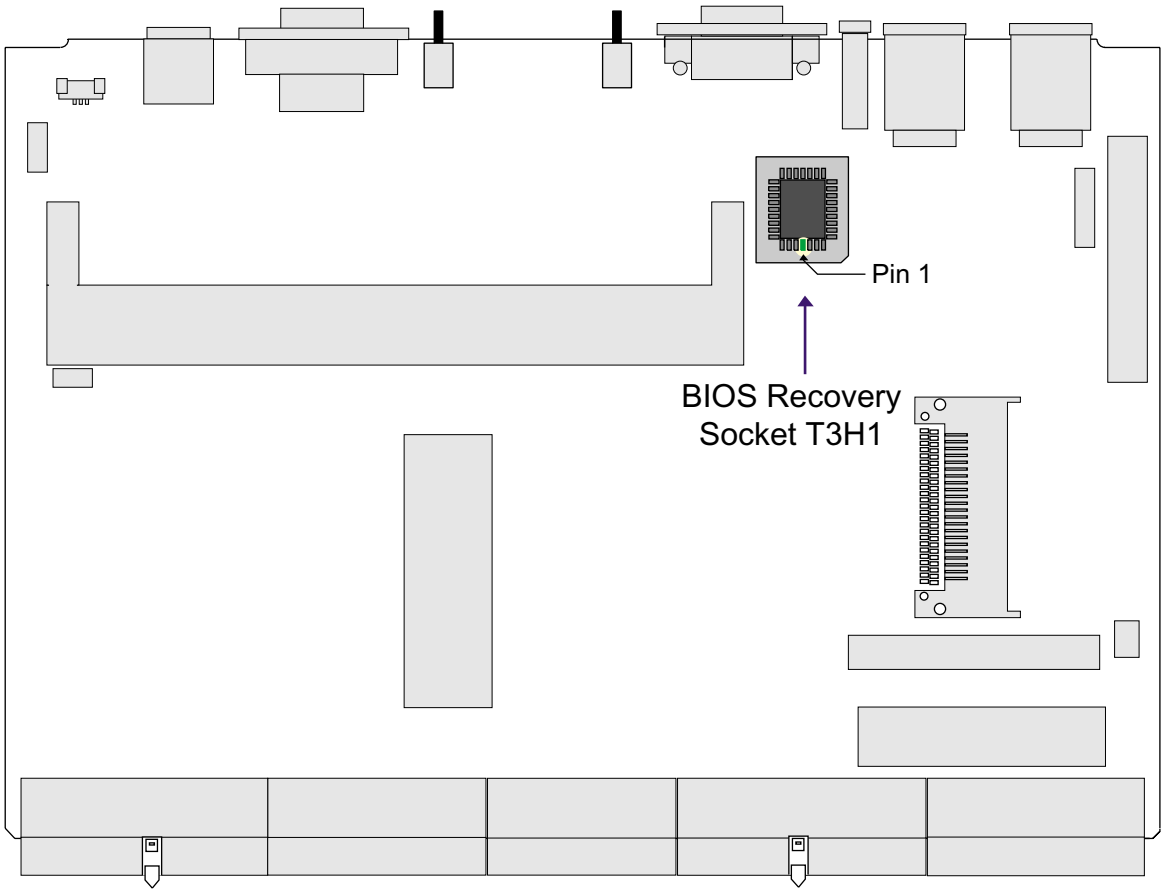
FLASH.EXE is a utility program that comes with the Intel Software Development Kit. It allows the user to quickly modify the BIOS in the on-board flash memory. This eliminates the need for a PROM programmer and frees the user from having to remove boards and chips from the system. Before attempting to program the flash, make sure that the Flash Write-Protect switch SW5-4 is open.

To reprogram the BIOS on the ZT 5550, use the following syntax at an MS-DOS prompt:

```
FLASH  /b  BIOS.XXX
```

where BIOS.XXX is the BIOS image for the ZT 5550. See the *Intel NetStructure Embedded BIOS* software manual for more information on the flash utility.

BIOS Recovery Socket Location



SRAM

The ZT 5550 provides a 128 KB SRAM device for use by the application. The SRAM can be battery-backed through switch SW3-3. The device is redundantly mapped in a 256 KB window at FFF80000h - FFFBFFFFh and FFFA0000h - FFFBFFFFh. Both the on-board flash memory and the SRAM device are accessed through this window. Device selection is controlled by System Register 1 (78h, bit 3).

The SRAM device can also be used for video emulation when no local video is available. Video emulation uses the 4 K space FFF90000h - FFF90FFFh in the video display area of memory (FFFA0000h - FFFBFFFFh). Note that when no local video is available, any battery-backed data in the FFF90000h - FFF90FFFh range is overwritten by the BIOS during bootup.

A. Specifications

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 5550. It includes connector descriptions and pinouts, as well as illustrations of the board dimensions and connector locations.

Electrical and Environmental Specifications

The topics listed below provide the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 5550 at these maximums. See the "DC Operating Characteristics" topic in this appendix for operating conditions.

Supply Voltage, Vcc	6.5V
Supply Voltage, Vcc3	4.5V
Supply Voltage, AUX +	15V
Supply Voltage, AUX -	-15V
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	<95% at 40° Celsius

Operating Temperature

The ZT 5550's heatpipe allows a maximum ambient air temperature of 50° C with 250 LFM (linear feet per minute) of airflow. The maximum power dissipation of the EMC-2 module is 14W. External airflow must be provided if operating above 25° C ambient.

Because the ambient temperature (around the heatsink) can easily exceed 25° C in an enclosed card rack, it is strongly recommended that a "fan tray" below the card rack be used to supply external airflow. Appendix B, "Thermal Considerations," contains a "Required Airflow vs. Ambient Temperature" graph, as well as details on monitoring the processor temperature.

DC Operating Characteristics

Supply Voltage, Vcc	4.75V minimum; 5.0V typical; 5.25V maximum
Supply Voltage, Vcc3	3.14V minimum; 3.30V typical, 3.46V maximum
Supply Voltage, AUX +	11.4V minimum; 12.0V typical; 12.6V maximum
Supply Voltage, AUX -	-11.4V minimum; -12.0V typical; -12.6V maximum

Supply Current: (Numbers below assume a 500 MHz processor. These numbers are unaffected by the amount of SDRAM installed).

Icc	2.2A typical; 3.8A maximum
Icc3	2.7A typical; 4.4A maximum
AUX + (12V)	250mA typical; 350mA maximum

Battery Backup Characteristics

Battery Voltage	3V
Battery Capacity	250mAh
Real-Time Clock Requirements	8µA maximum (Vbat = 3V, Vcc=0V)
Real-Time Clock Data Retention	31,250 Hours/ 3.7 years minimum (not powered) 45,458 Hours/ 5.2 years minimum (with Vcc power applied 8 hours per day)
Electrochemical Construction	Long life lithium with solid-state polycarbon monofluoride cathode.

Reliability

MTBF	54,000 hours (approximately 6.2 years)
MTTR	5 minutes

Mechanical Specifications

The topics listed below provide the following mechanical specifications:

- Board dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)

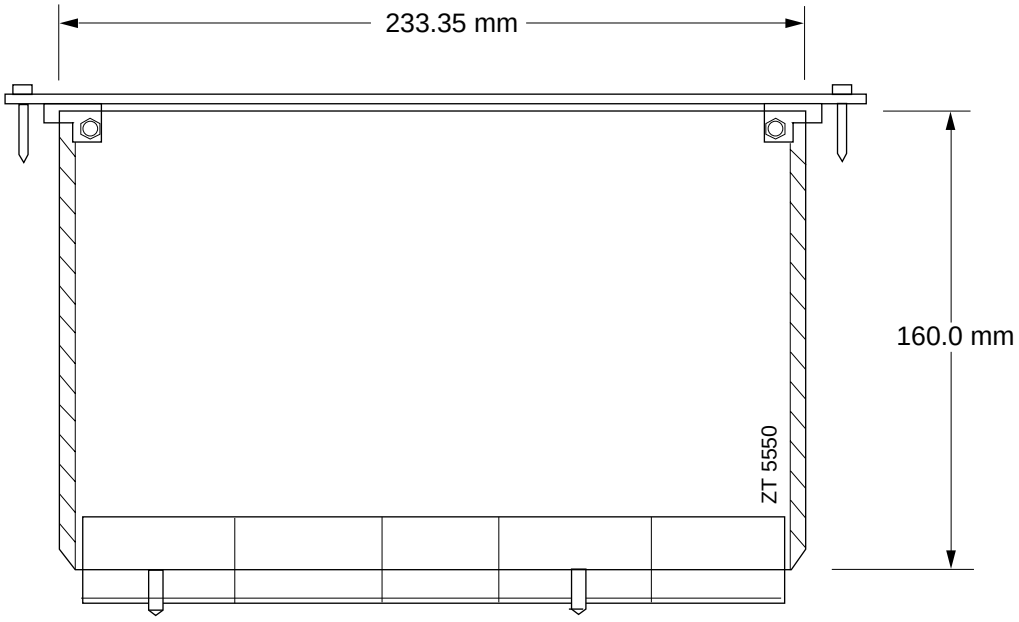
Board Dimensions and Weight

The ZT 5550 meets the *CompactPCI Specification, PICMG 2.0, Version 2.1* for all mechanical parameters. In a CompactPCI enclosure with 0.8 in spacing, the ZT 5550 requires one card slot with the integrated heatpipe.

Mechanical dimensions are shown in the "Board Dimensions" illustration and outlined below.

Board Length	160 mm (6.299 in)
Board Width	233.35 mm (9.187 in)
Board Thickness	1.6 mm (0.063 in)
Board Weight	0.625 kg (1 lb, 4.1 oz) w/ heatpipe and 256 MB of SDRAM

Board Dimensions



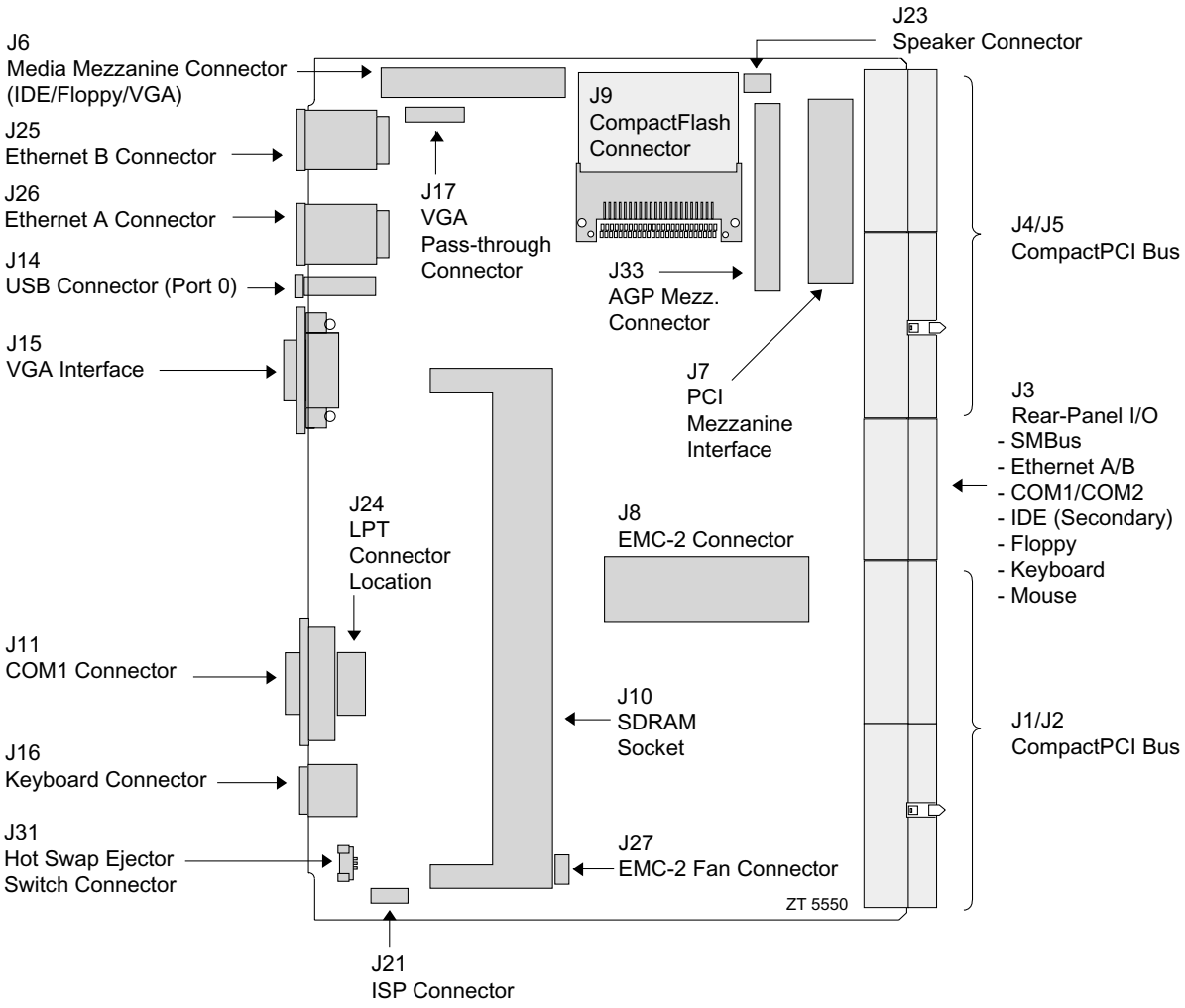
Connectors

As shown in the "Connector Locations" figure, the ZT 5550 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table. A detailed description and pinout for each connector is given in the following topics.

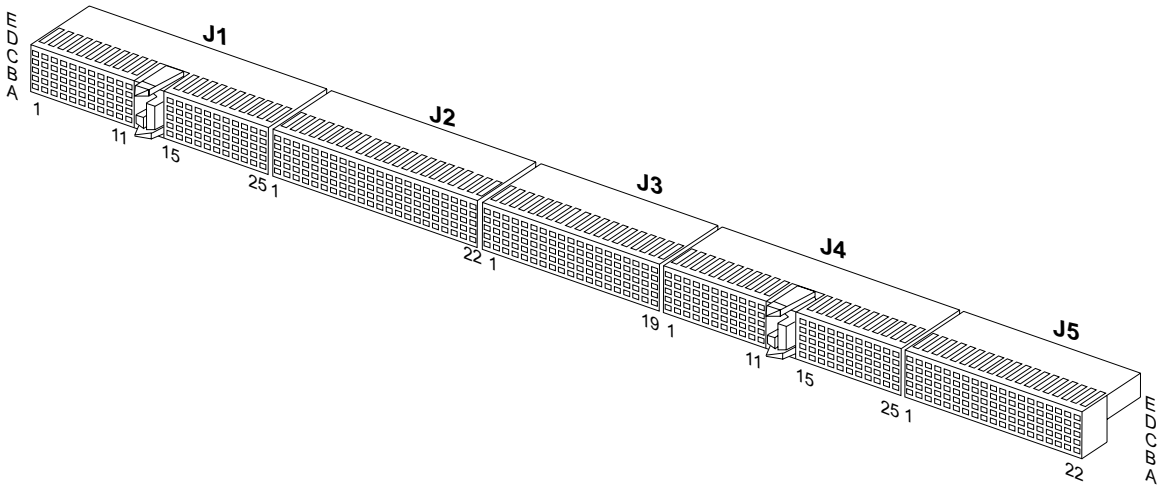
Connector Assignments

Connector	Function
J1	CompactPCI Bus Connector (32-bit, 110-pin, 2 mm x 2 mm, female)
J2	CompactPCI Bus Connector (64-bit, 110-pin, 2 mm x 2 mm, female)
J3	Rear-Panel User I/O Connector (95-pin 2 mm x 2 mm, female)
J4	CompactPCI Bus Connector (32-bit, 110-pin, 2 mm x 2 mm, female)
J5	CompactPCI Bus Connector (64-bit, 110-pin, 2 mm x 2 mm, female)
J6	I/O Expansion Connector (100-pin, 2 mm)
J7	PCI Mezzanine Interface Connector (150-pin, 2 mm)
J8	EMC-2 Mobile Module Processor Connector; Reserved for Intel use
J9	CompactFlash Connector (50-pin, CF Card Slot Header)
J10	SDRAM Connector (168-pin)
J11	COM1 Serial Port (9-pin, D-Shell)
J14	Universal Serial Bus Connector (4-pin, USB, Port 0)
J15	VGA Interface (15-pin, D-Shell)
J16	Keyboard Connector (6-pin, DIN)
J17	Video Mezzanine Pass-Through Connector (16-pin)
J23	Speaker Connector (2-pin)
J25	Ethernet Connector B (8-pin, RJ-45)
J26	Ethernet Connector A (8-pin, RJ-45)
J27	Fan-Sink Power Connector (3-pin)
J31	Hot Swap Ejector Switch Connector (3-pin)
J33	AGP Video Mezzanine Interface (114-pin)

Connector Locations



Backplane Connectors Pin Locations



J1 (CompactPCI Bus Connector)

J1 is a 110-pin, 2 mm x 2 mm, female 32-bit CompactPCI connector (AMP 352068-1). Rows 12-14 are used for connector keying. See the "J1 CompactPCI Bus Connector Pinout" table for pin definitions and the "Backplane Connectors Pin Locations" figure showing pin placement.

J1 CompactPCI Bus Connector Pinout

Pin#	Z	A	B	C	D	E	F
25	(GND)	5V	REQ64#	**ENUM#**	3.3V	5V	GND
24	(GND)	AD[1]	5V	**V(I/O)**	AD[0]	ACK64#	GND
23	(GND)	3.3V	AD[4]	AD[3]	**5V**	AD[2]	GND
22	(GND)	AD[7]	GND	**3.3V**	AD[6]	AD[5]	GND
21	(GND)	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	(GND)	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	(GND)	3.3V	AD[15]	AD[14]	**GND**	AD[13]	GND
18	(GND)	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	(GND)	3.3V	SDONE	SBO#	**GND**	PERR#	GND
16	(GND)	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	(GND)	3.3V	FRAME#	IRDY#	**PWRON#**	TRDY#	GND
KEY							
11	(GND)	AD[18]	AD[17]	AD[16]	**GND**	C/BE[2]#	GND
10	(GND)	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	(GND)	C/BE[3]#	**RH_SYSEN#**	AD[23]	**GND**	AD[22]	GND
8	(GND)	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	(GND)	AD[30]	AD[29]	AD[28]	**GND**	AD[27]	GND
6	(GND)	REQ#	GND	**3.3V**	FB_CLK	AD[31]	GND
5	(GND)	BRSVP1A5	BRSVP1B5	**PCI_RST#**	**GND**	GNT0#	GND
4	(GND)	BRSVP1A4	HAPPY#	**V(I/O)**	INTP	INTS	GND
3	(GND)	INTA#	INTB#	INTC#	**5V**	INTD#	GND
2	(GND)	TCK	5V	TMS	TDO	TDI	GND
1	(GND)	5V	-12V	TRST#	+12V	5V	GND
Pin#	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

= long pins = short pins All others = medium length pins

Note: Row F GND pins are long length as is standard for *CompactPCI*.

J2 (CompactPCI Bus Connector)

J2 is a 110-pin 2 mm x 2 mm right-angle female 64-bit Compact PCI connector (AMP 352152-1). See the "J2 CompactPCI Bus Connector Pinout" table for pin definitions and the "Backplane Connectors Pin Locations" figure showing pin placement.

Note: The SMBus connections have moved from C/D/E21 to C/D/E19 (revision D and later boards).

J2 CompactPCI Bus Connector Pinout

Pin#	Z	A	B	C	D	E	F
22	(GND)	GA4	GA3	GA2	GA1	GA0	GND
21	(GND)	CLK6	GND	RSV	RSV	RSV	GND
20	(GND)	CLK5	GND	RSV	GND	HEART	GND
19	(GND)	GND	GND	SMD	SMC	SMA#	GND
18	(GND)	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	(GND)	BRSVP2A17	HA	PRST#	REQ6#/FTHSI	GNT6#/FTHSO	GND
16	(GND)	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
15	(GND)	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND
14	(GND)	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	(GND)	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	(GND)	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	(GND)	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	(GND)	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	(GND)	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	(GND)	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	(GND)	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	(GND)	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	(GND)	C/BE[5]#	64EN#	V(I/O)	C/BE[4]#	PAR64	GND
4	(GND)	V(I/O)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3	(GND)	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	(GND)	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	(GND)	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin#	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

J3 (Rear-Panel User I/O Connector)

J3 is a 95-pin, 2 mm x 2 mm female connector (AMP 352171-1) providing rear-panel user I/O. See the "J3 Rear-Panel User I/O Connector Pinout" table for pin definitions and the "Backplane Connectors Pin Locations" figure showing pin placement.

Signals for the following functions are directed out this connector:

- USB
- SMB
- Mouse
- Keyboard
- Front-Panel Eject LED
- EIDE secondary channel
- Speaker
- RPIO ID
- Ethernet A
- Ethernet B
- COM1
- COM2
- Floppy
- NMI
- PRST#

J3 Rear-Panel User I/O Connector Pinout

Pin#	Z	A	B	C	D	E	F
19	(GND)	PWRGD	IOCS16#	SIORDY	SMALRT#	IRQ15	GND
18	(GND)	SMDATA	SMCLK	CS3S#	CS1S#	RPID	GND
17	(GND)	DDS15	DDS14	DDS13	DDS12	EJECT#	GND
16	(GND)	DDS11	DDS10	DDS9	DDS8	SDDAK#	GND
15	(GND)	DAS0	DAS1	J3VCC	DAS2	SDDRQ#	GND
14	(GND)	DDS7	DDS6	DDS5	DDS4	SDIOW#	GND
13	(GND)	DDS3	DDS2	DDS1	DDS0	SDIOR#	GND
12	(GND)	DR0#	MSEN0	MTR0#	INDEX#	WDATA#	GND
11	(GND)	DR1#	DSKCHG#	MTR1#	DENSL	RDATA#	GND
10	(GND)	WP#	HDSEL#	DIR#	TRK0#	STEP#	GND
9	(GND)	WGATE#	RXA-	J3GND	HSLED	USB+	GND
8	(GND)	J3GND	RXA+	J3VCC	CTB	USB-	GND
7	(GND)	RXB-	J3GND	TXB-	CTA	J3GND	GND
6	(GND)	RXB+	J3GND	TXB+	J3GND	TXA-	GND
5	(GND)	ABORT#	MSDAT	SPKR	KBDAT	TXA+	GND
4	(GND)	PRST#	MSCLK	J3VCC	KBCLK	S1RXD	GND
3	(GND)	S1CTS	S1RTS	S1DSR	S1DCD	S1TXD	GND
2	(GND)	S2RIN	S2DTR	S1RIN	S1DTR	S2RXD	GND
1	(GND)	S2CTS	S2RTS	S2DSR	S2DCD	S2TXD	GND
Pin#	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

J4 (CompactPCI Bus Connector)

J4 is a 110-pin, 2 mm x 2 mm, female 32-bit CompactPCI connector (AMP 352068-1). Rows 12-14 are used for connector keying. See the "J4 CompactPCI Bus Connector Pinout" table for pin definitions and the "Backplane Connectors Pin Locations" figure showing pin placement.

J4 CompactPCI Bus Connector Pinout

Pin#	Z	A	B	C	D	E	F
25	(GND)	5V	REQ64#	**ENUM#**	3.3V	5V	GND
24	(GND)	AD[1]	5V	**V(I/O)**	AD[0]	ACK64#	GND
23	(GND)	3.3V	AD[4]	AD[3]	**5V**	AD[2]	GND
22	(GND)	AD[7]	GND	**3.3V**	AD[6]	AD[5]	GND
21	(GND)	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	(GND)	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	(GND)	3.3V	AD[15]	AD[14]	**GND**	AD[13]	GND
18	(GND)	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	(GND)	3.3V	SDONE	SBO#	**GND**	PERR#	GND
16	(GND)	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	(GND)	3.3V	FRAME#	IRDY#	**RH_PWRON#**	TRDY#	GND
KEY							
11	(GND)	AD[18]	AD[17]	AD[16]	**GND**	C/BE[2]#	GND
10	(GND)	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	(GND)	C/BE[3]#	**PRES**	AD[23]	**GND**	AD[22]	GND
8	(GND)	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	(GND)	AD[30]	AD[29]	AD[28]	**GND**	AD[27]	GND
6	(GND)	REQ#	GND	**3.3V**	CLK	AD[31]	GND
5	(GND)	BRSVP1A5	BRSVP1B5	**PCI_RST#**	**GND**	GNT0#	GND
4	(GND)	BRSVP1A4	RH_HPY#	**V(I/O)**	INTP	INTS	GND
3	(GND)	INTA#	INTB#	INTC#	**5V**	INTD#	GND
2	(GND)	TCK	5V	TMS	TDO	TDI	GND
1	(GND)	5V	-12V	TRST#	+12V	5V	GND
Pin#	Z	A	B	C	D	E	F

= long pins = short pins All others = medium length pins

Note: Row F GND pins are long length as is standard for *CompactPCI*.

J5 (CompactPCI Bus Connector)

J5 is a 110-pin 2 mm x 2 mm right-angle female 64-bit Compact PCI connector (AMP 352152-1). See the “J5 CompactPCI Bus Connector Pinout” table below for pin definitions and the “Backplane Connectors Pin Locations” figure showing pin placement.

J5 CompactPCI Bus Connector Pinout

Pin#	Z	A	B	C	D	E	F
22	(GND)	GA4	GA3	GA2	GA1	GA0	GND
21	(GND)	RCLKOUT	GND	HCSDO	RSV	RSV	GND
20	(GND)	CLK5	GND	HCSDI	GND	RSV	GND
19	(GND)	GND	GND	RST_RH#	RH_CLKIN	RSV	GND
18	(GND)	RXHB-	RXHB+	J5GND	GND	BRSVP2E18	GND
17	(GND)	J5GND	GND	PRST#/HA_RST#	REQ6#/RH_GNT7#	GNT6#/S_GNT7#	GND
16	(GND)	TXHB-	TXHB+	CMODE#	GND	BRSVP2E16	GND
15	(GND)	J5GND	GND	RH_CMODE#	REQ5#	GNT5#	GND
14	(GND)	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	(GND)	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	(GND)	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	(GND)	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	(GND)	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	(GND)	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	(GND)	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	(GND)	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	(GND)	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	(GND)	C/BE[5]#	64EN#	V(I/O)	C/BE[4]#	PAR64	GND
4	(GND)	V(I/O)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3	(GND)	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	(GND)	CLK2	CLK3	RH_PRES	GNT2#	REQ3#	GND
1	(GND)	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin#	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

J6 (I/O Expansion Connector)

J6 is a 100-pin 2 mm connector (two 50-pin COMM CON 50690) carrying I/O signals between the CPU and an optional IOX board (such as the ZT 96072 or ZT 96073). See the “J6 I/O Expansion Connector Pinout“ table below for pin definitions.

J6 I/O Expansion Connector Pinout

Pin#	A	B	C	D
25	GND	GRNIN	PMC1-BUSMODE1	PMC2-BUSMODE1
24	REDIN	GND	PMC1-BUSMODE2	PMC2-BUSMODE2
23	GND	BLUIN	PMC1-BUSMODE4	PMC2-BUSMODE4
22	VCCVID	GND	GND	IDE_RST
21	GND	HYSYNCIN	DD8	DD7
20	VSYNCIN	GND	DD9	DD6
19	GND	DDCDATIN	DD10	DD5
18	DDCCLKIN	VID_EN#	DD11	DD4
17	DRIVE_VCC	VCC	DD12	DD3
16	DRIVE_VCC	MTR1#	DD13	DD2
15	DIGIO7	INDEX#	DD14	DD1
14	DIGIO6	WGATE#	DD15	DD0
13	DIGIO5	DSKCHG#	NC	GND
12	DIGIO4	DRO#	GND	DDRQ0
11	DIGIO3	MSEN0	GND	DIOW#
10	DIGIO2	DR1#	GND	DIOR#
9	DIGIO1	MTR0#	CSEL	IORDY
8	DIGIO0	DENSL	GND	DDAK0#
7	BEDSEL	DIR#	ISA1O16#	IRQ14
6	12V	STEP#	PDIAG	DA1
5	12V	WDATA#	DA2	DA0
4	GND	TRK0#	CS3P#	CS1P#
3	GND	WP#	GND	IDEACK
2	GND	RDATA#	VCC	VCC
1	GND	HDSEL#	XTAT	GND

J7 (PCI Mezzanine Interface Connector)

J7 is a 150-pin, 2 mm connector (three 50-pin COMM CON 50690) providing the PCI local bus interface to optional mezzanine adapters and I/O expansion boards that may be attached to the CPU. J7 provides a complete 32-bit PCI interface. This connector is CompactPCI compatible. See the “J7 PCI Mezzanine Interface Connector Pinout” table below for pin definitions.

J7 PCI Mezzanine Interface Connector Pinout

Pin#	A	B	C	D	E	F
25	5V	REQ64#	RSVD	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	GND	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	MZ_ID1	MZ_ID2	GND	PERR#	GND
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	CLK1	RSVD	RSVD	RSVD	RSVD	RSVD
13	RSVD	CLK2	RSVD	RSVD	RSVD	RSVD
12	REQ1#	RSVD	GNT1-	RSVD	RSVD	RSVD
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ0#	GND	3.3V	CLK0	AD[31]	GND
5	NC	NC	RST#	GND	GNT0#	GND
4	SERIRQ	GND	V(I/O)	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

J9 (CompactFlash Connector)

J9 is a 50-pin Surface Mount Right Angle CF Card Slot Header (AMP 120615-1) designed to accommodate a CompactFlash card. Refer to the CompactFlash Specification, Revision 1.X for pinout and device information. The topic "CompactFlash" in Appendix E, “Data Sheet Reference,” provides a link to the CompactFlash Association’s website.

J10 (SDRAM Connector)

J10 is a 168-pin connector (AMP 1-390171-0) accommodating the SDRAM module used for system memory. The topic "SDRAM" in Appendix E, “Data Sheet Reference,” provides a link to the specification for this connector.

J11 (COM1 Serial Port)

J11 is a 9-pin D-shell connector (AMP 179952-3) providing a front-panel COM1 interface on the ZT 5550’s connector plate. COM1 signals are also directed out rear-panel user I/O connector J3. See the “J11 COM1 Serial Port Pinout” table below for pin definitions.

J11 COM1 Serial Port Pinout

Pin#	Function	Pin#	Function	Pin#	Function
1	DCD	4	DTR	7	RTS
2	RXD	5	GND	8	CTS
3	TXD	6	DSR	9	RIN

J14 (Universal Serial Bus Connector)

J14 is the Port 0 Universal Serial Bus (USB) interface connector (AMP 440260-1). J14 can be used simultaneously with the Port 1 USB connector on an optional RPIO board (such as the ZT 4804). See the “J14 Universal Serial Bus Connector Pinout” table below for pin definitions.

J14 Universal Serial Bus Connector Pinout

Pin#	Function
1	Vcc (Fused)
2	DATA-
3	DATA+
4	GND

J15 (VGA Interface)

J15 is an HD15, 15-pin, female, D-shell connector (AMP 177514-9) providing a front-panel interface for VGA signals routed from the J17 Mezzanine Video Pass-Through Connector. See the “J15 VGA Interface Pinout” table for pin definitions.

J15 VGA Interface Pinout

Pin#	Signal	Pin#	Signal	Pin#	Signal
1	RED	6	RGND	11	NC
2	GRN	7	GGND	12	SDA
3	BLUE	8	BGND	13	HSYNC
4	NC	9	VCC	14	VSYNC
5	DGND	10	SGND	15	SCL

J16 (Keyboard Connector)

J16 is a 6-pin mini-DIN connector (AMP 749180-1) for standard PS/2-style keyboard devices. Keyboard signals are also directed out rear-panel user I/O connector J3. The mouse is also available through front panel connector J16 when an IBM ThinkPad style "Y" cable is used. See the “J16 Keyboard Interface Connector Pinout” table below for pin definitions.

J16 Keyboard Connector Pinout

Pin#	Function	Pin#	Function
1	KBDAT	4	Vcc (Fused)
2	MDAT	5	KBCLK
3	GND	6	MCLK

J17 (Video Mezzanine Pass-Through Connector)

J17 is a 2-row x 8 pin, 2 mm surface mount socket (Samtec SQT-108-01-L-D) used to pass signals from a mezzanine video adapter (such as the ZT 96079) to the J15 VGA Interface connector on the front panel. See the “J17 Video Mezzanine Pass-Through Connector Pinout” table for pin definitions.

J17 Video Mezzanine Pass-Through Connector Pinout

Pin#	Signal	Pin#	Signal	Pin#	Signal	Pin#	Signal
1	RED	5	DGND	9	VCC	13	HSYNC
2	GRN	6	RGND	10	SGND	14	VSYNC
3	BLUE	7	GGND	11	NC	15	SCL
4	NC	8	BGND	12	SDA	16	NC

J23 (Speaker Connector)

J23 is a 2-pin connector (Molex 39-27-0021) for connection to an optional PC speaker. See the “J23 Speaker Connector Pinout” table below for pin definitions.

J23 Speaker Connector Pinout

Pin#	Function
1	SPK1
2	SPK2

J25 / J26 (Ethernet Connectors)

J25 (ENET B) and J26 (ENET A) are RJ-45 Ethernet connectors (Stewart SI-40231) providing both 10 Mbit (10BASE-T) and 100 Mbit (100BASE-TX) protocols. Two LEDs are located inside each RJ-45 connector: yellow indicates data transmission, green indicates data reception.

Depending on application requirements, configuration of switches SW4-1, -2 (front panel/rear-panel access) and/or SW4-3 (HA/non-HA system) may be necessary. See the “J25/J26 Ethernet B/A Connectors Pinout” table below for pin definitions.

J25/J26 Ethernet Connectors Pinout

Pin#	Function
1	TX+
2	TX-
3	RX+
4-5	Unused pair
6	RX-
7-8	Unused pair

J27 (Fan Sink Power Connector)

J27 is a 3-pin connector (AMP 173981-3) used to supply power to an optional fan for cooling the EMC-2 module. See the “J27 Fan Sink Connector Pinout” below for pin definitions.

J27 Fan Sink Power Connector Pinout

Pin#	Function
1	PWR
2	GND
3	FAN TACH

J31 (Hot Swap Ejector Switch Connector)

J31 is a 3-pin connector (Molex 53398-0390) connecting the Hot Swap switch to the board's lower ejector. This switch is tied to logic on the ZT 5550 to sense a board extraction or insertion. See the “J31 Hot Swap Ejector Switch Connector Pinout” below for pin definitions.

J31 Hot Swap Ejector Switch Connector Pinout

Pin#	Function
1	Common
2	Latched
3	Unlatched

J33 (AGP Video Mezzanine Interface)

J33 is a 114-pin AMP Mictor Series 25 receptacle (AMP 767054-3) providing an interface for an Intel AGP Video Mezzanine Adapter (such as the ZT 96079). See the "J33 AGP Video Mezzanine Interface Pinout" table on the following page for pin definitions.

J33 AGP Video Mezzanine Interface Pinout

Column A Pins	Signal	GND Pins	Signal	Column B Pins
1	spare	GND	12V	1
2	5.0V	—	spare	2
3	5.0V	—	Reserved*	3
4	GND	—	GND	4
5	USB+	GND	USB-	5
6	GND	—	GND	6
7	INTB#	—	INTA#	7
8	CLK	—	RST#	8
9	GND	GND	GND	9
10	REQ#	—	GNT#	10
11	VCC3.3	—	VCC3.3	11
12	ST0	—	ST1	12
13	ST2	GND	Reserved	13
14	RBF#	—	PIPE#	14
15	spare	—	spare	15
16	SBA0	—	SBA1	16
17	VCC3.3	GND	VCC3.3	17
18	SBA2	—	SBA3	18
19	SB_STB	—	Reserved	19
20	SBA4	—	SBA5	20
21	SBA6	GND	SBA7	21
22	GND	—	GND	22
23	AD31	—	AD30	23
24	AD29	—	AD28	24
25	VCC3.3	GND	VCC3.3	25
26	AD27	—	AD26	26

Column A Pins	Signal	GND Pins	Signal	Column B Pins
27	AD25	—	AD24	27
28	AD_STB1	—	Reserved	28
29	AD23	GND	C/BE3#	29
30	Vddq3.3	—	Vddq3.3	30
31	AD21	—	AD22	31
32	AD19	—	AD20	32
33	AD17	GND	AD18	33
34	C/BE2#	—	AD16	34
35	Vddq3.3	—	Vddq3.3	35
36	IRDY#	—	FRAME#	36
37	VCC3.3	GND	VCC3.3	37
38	DEVSEL#	—	TRDY#	38
39	Vddq3.3	—	STOP#	39
40	PERR#	—	Spare	40
41	GND	GND	GND	41
42	SERR#	—	PAR	42
43	GND	—	GND	43
44	C/BE1#	—	AD15	44
45	Vddq3.3	GND	Vddq3.3	45
46	AD14	—	AD13	46
47	AD12	—	AD11	47
48	AD10	—	AD9	48
49	AD8	GND	C/BE0#	49
50	Vddq3.3	—	Vddq3.3	50
51	AD_STB0	—	Reserved	51
52	AD7	—	AD6	52
53	AD5	GND	AD4	53
54	AD31	—	AD2	54
55	Vddq3.3	—	Vddq3.3	55
56	AD1	—	AD0	56
57	SMB0	GND	SMB1	57

B. Thermal Considerations

This appendix describes the thermal requirements for reliable operation of the ZT 5550. The thermal performance of non-Intel systems must comply with these requirements. To monitor the junction temperature of the CPU, use the Intel SMBus Device Driver or BIOS Diagnostics as described in the "Thermal Verification" topic below.

Thermal Requirements

The ZT 5550 comes from the factory with an integrated heatpipe for cooling the processor module. The heatpipe allows a maximum ambient air temperature of 50° C with 250 linear feet per minute (LFM) of airflow. The maximum power dissipation of the processor (EMC-2) module is 14 W. External airflow must be provided if operating above 25° C ambient. Because the ambient temperature (around the heatsink) can easily exceed 25° C in an enclosed card rack, it is strongly recommended that a "fan tray" below the card rack be used to supply external airflow.

The topic "Thermal" in Appendix E, "Data Sheet Reference," contains a link to Thermacore Incorporated. Visit their site for a good explanation of heatpipe technology.

For applications not using the integrated heatpipe, a fan/heatsink combination is recommended. It may be useful in such applications to use a tachometer signal to monitor fan rotation. The "Tachometer Monitoring" topic describes the tachometer monitoring circuitry on the ZT 5550.

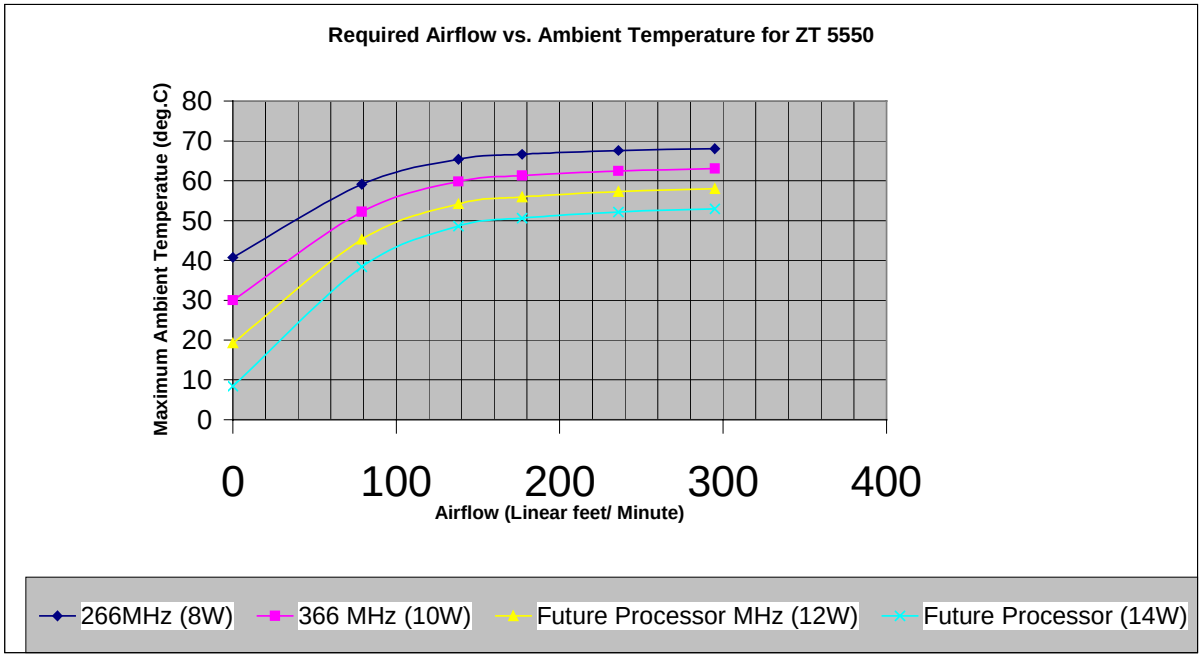
Heat Pipe Temperature Range

The heat pipe used on the ZT 5550 reaches a thermal lock condition at temperatures above 95° C. Thermal lock is caused by water in the pipe vaporizing and being too hot to condense and transfer heat to the heat exchanger fins. Maintaining the specified airflow prevents high temperature thermal lock by allowing the temperature of the heat pipe collector plate to stay below 90° C.

Also, heat transfer is slowed if the heat pipe is too cold. In this condition the water has difficulty vaporizing and migrating to the heat exchanger fins. This condition corrects itself as the processor heats up from operation.

The "Required Airflow vs. Ambient Temperature" graph below shows the ZT 5550 airflow requirements based on the absolute maximum processor core temperature (100° C). Intel does not guarantee reliable operation if the module temperature exceeds 55° C and core temperature exceeds 100° C.

Required Airflow vs. Ambient Temperature



Thermal Verification

Because reliable long-term operation of the ZT 5550 depends on maintaining proper temperature, Intel strongly recommends that you verify the operating temperature of the EMC-2 processor module and processor core in your final system configuration. The EMC-2 processor temperature is monitored via the System Management Bus (SMBus). Use Intel's SMBus Device Driver or the BIOS Diagnostics to obtain readings of the MC-2 module and processor core temperature.

The BIOS Diagnostics offers the simplest method with which to monitor module and core temperatures. Access the BIOS Diagnostics through the BIOS Setup Utility (discussed in the "BIOS Configuration Overview" topic in Chapter 2), select the Diagnostics tab and view the "Processor Core" and "EMC Module" temperatures. Intel does not guarantee reliable operation if the module temperature exceeds 55° C and core temperature exceeds 100° C.

Temperature Monitoring

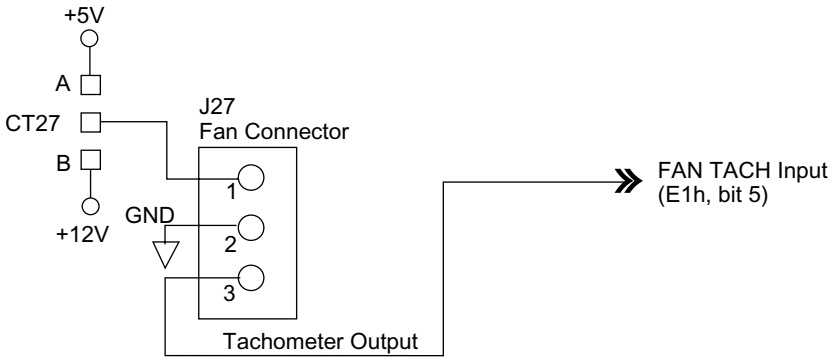
The ZT 5550's Intel Pentium III processor Mobile Module (EMC-2) incorporates Active Thermal Feedback (ATF) sensing compliant with the ACPI Rev 1.0 specification. Active Thermal Feedback is discussed in detail in the *Intel Pentium III Processor Mobile Module: Mobile Module Connector 2 (MMC-2), #243668-002* data sheet. The topic "Pentium III Processor" in Appendix E, "Data Sheet Reference," contains a link to the data sheet.

Tachometer Monitoring

The ZT 5550 has circuitry on-board for monitoring the output of an optional fan-sink tachometer. The tachometer output is routed to connector J27, pin 3. The tachometer output pulses as the fan rotates. The output is routed directly to the DS1780 System Health Monitor device. Most fan tachometers have an output rate of approximately 100 Hz; this input therefore changes states approximately every 5ms.

The topic "Thermal" in Appendix E, “Data Sheet Reference,” contains a link to the *Dallas Semiconductor* DS1705 3.3 and 5.0 Volt Micromonitor* data sheet.

Tachometer Monitoring Input Circuitry



C. System Registers

The ZT 5550 provides several system registers to control and monitor a variety of functions. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under their control.

System Registers 1 and 2 are in an on-board PLD and accessible at ports 78h and 79h, respectively. System Registers 3 through 7 are in the on-board 16C50A Digital I/O ASIC device and accessible at ports E1h through E5h. As Digital I/O ASIC inputs, these registers are inverting; thus, a logic high (+5V) is read as a logic low.

Your system may include a ZT 4804 Rear-Panel I/O Transition board providing an SMBus interface between itself and the ZT 5550, as well as two user inputs and six alarm relay outputs This appendix also documents the ZT 4804's SMBus input and output registers. See the "ZT 4804 RPIO SMBus Registers" at the end of the appendix for descriptions of these registers.

System Register Definitions

The System Registers are accessible as follows:

	I/O Address	Register Name	Default Value	Access	Size
PAL	78h	System Register 1	0x00	R/W	8 bits
	79h	System Register 2	0x00	R/W	8 bits
Digital I/O ASIC	E1h	System Register 3	0x00	RO	8 bits
	E2h	System Register 4	0x01	R/W	8 bits
	E3h	System Register 5	0x00	RO	8 bits
	E4h	System Register 6	0x00	R/W	8 bits
	E5h	System Register 7	0x00	R/W	8 bits

System Register 1 (78h)

I/O Address: 78h
Default Value: 0x00
Size 8 bits
Attribute: R/W

Bit	Description	Default
7:4	**Flash Paging**. These bits are used to map one of the 16 pages of flash memory into the flash window, as shown in the table below. These pages are numbered 0 - 15, with page 0 being at the lowest address of the device and page 15 being at the highest address. Flash programming is further discussed in Chapter 11. Bit 7 / Bit 6 / Bit 5 / Bit 4 / Page 0 / 0 / 0 / 0 / 0 0 / 0 / 0 / 1 / 1 0 / 0 / 1 / 0 / 2 0 / 0 / 1 / 1 / 3 0 / 1 / 0 / 0 / 4 … / … / … / … / … … / … / … / … / … 1 / 1 / 1 / 1 / 15	0
3	**SRAM Select**. 0=standard flash, 1=SRAM	0
2	**Reserved**. This bit should always be written as 0	0
1	**Flash Write Enable**. 0=write-protected, 1=writable. Flash is hardware write-protected through switch SW5-4.	1
0	**Reserved**. This bit should always be written as 0	0

System Register 2 (79h)

I/O Address: 79h
Default Value: 0x00
Attribute: R/W

Bit	Description
7	**Reset Detection Bit** **Read Value:** 0=Watchdog has not timed out since power up or since this bit was last cleared; 1=Watchdog timed out and the Reset output was asserted. Bit 5, Reset Enable (below) must be set for this bit to assert. **Write Value:** 0=Clear this bit; 1 = No effect. **Power Up Value:** =0.
6	**First Stage Timeout Detection Bit** **Read Value:** 0=Watchdog has not timed out since power up or since this bit was last cleared; 1=Watchdog timed out and the First Stage Timeout output was asserted. Bit 4, First Stage Timeout Enable (below) must be set for this bit to assert. **Write Value:** 0=Clear this bit; 1=No effect. **Power Up Value:** =0.
5	**Reset Enable** **Read Value:** 0, 1=value written to the bit. **Write Value:** 0=Reset operation of the watchdog is not enabled. When the watchdog times out, neither the Reset Detection status nor the Reset output will be asserted. 1=Reset operation of the watchdog is enabled. When and if the watchdog times out: • The Reset output asserts for one clock count. • The RstDet status bit goes high and stays high until cleared by software. • Reset action actually occurs a clock cycle after the NMI action. **Power Up Value:** =0. **Value After Timeout** =0. If “PCI Reset” occurs for non-watchdog reasons, value =0.

(System Register 2 - 79h continued)

4	**First Stage Timeout Enable** **Read Value:** Reflects the value written to the bit. **Write Value:** 0=First Stage Timeout operation of the watchdog is not enabled. When the watchdog times out, neither the First Stage Timeout status bit nor the First Stage Timeout output is asserted. 1=First Stage Timeout operation of the watchdog is enabled. When and if the watchdog times out: • The First Stage Timeout output asserts for one clock count. • The First Stage Timeout status bit goes high and stays high until cleared by software. **Power Up Value:** =0. **Post Time Out Value** =0 **Value After Timeout** =0. If "PCI Reset" occurs for reasons not watchdog related, Value =0.
3	**Reserved:** This bit is reserved. It has no user function and should always be written as 0. **Power Up Value** =0.
2:0	**Terminal Count (TrmCnt2…TrmCnt0):** **Read Value:** Reflects the value written to the bit. **Write Value:** These bits determine the terminal count of the watchdog timer in seconds. Their value has the following meaning: Bit 2, Bit 1, Bit 0. The minimum timeout period is given. The watchdog times out in no less than the minimum value. The nominal timeout period is 30% longer than the minimum. 000 = 250 ms 100 = 32 s 001 = 500 ms 101 = 64 s 010 = 1 s 110 = 128 s 011 = 8 s 111 = 256 s **Power Up Value** =000

System Register 3 (E1h)

I/O Address: E1h
Default Value: 0x00
Size 8 bits
Attribute: RO

Bit	Description
7	**Reserved.** This bit is reserved and should not be modified by the user.
6	**ENUM.** This bit reports that a hot swap peripheral card has been installed or removed from the system. This bit should always be written as 0.
5:0	**Reserved.** These bits are reserved and should not be modified by the user.

System Register 4 (E2h)

Address Offset: E2h
Default Value: 0x01
Size 8 bits
Attribute: R/W

Bit	Description
7:4	**Serial # ID.** These bits are used by the built-in diagnostic software for reading board serial numbers. The serial numbers are stored in the DS2401 Silicon Serial Number devices located on CPUs, mezzanine boards, and rear-panel boards, etc., and allow boards to be uniquely identified in a system. Bits 4 - 7 read serial numbers as follows: **Bit 7** = ZT 4804; **Bit 6** =ZT 96072; **Bit 5** =ZT 4802; **Bit 4** = ZT 5550
3:0	**Reserved.** These bits are reserved and should not be modified by the user.

System Register 5 (E3h)

Address Offset: E3h
Default Value: 0x00
Size 8 bits
Attribute: RO

Bit	Description
7	**Flash Write-Protect Status**. This bit reads back the status of switch SW5-4. A 0 means that the flash is **not** write-protected by SW5-4; a 1 means the flash **is** write-protected by SW5-4.
6	**Boot Source Monitoring.** This bit allows software to monitor the boot source as selected by SW5-1. When SW5-1 is open (boot from BIOS Recovery socket T3H1), this bit reads back a 0. When SW5-1 is closed (boot from BIOS contained in onboard flash), this bit reads back a 1.
5	**Soft Reset Mode Monitoring.** This bit allows software to monitor the position of SW3-4 (Soft Reset Mode Select switch). When SW3-4 is open, this bit reads back a 0. When SW3-4 is closed, this bit reads back a 1.
4	**Reserved.** These bits are reserved and should not be modified by the user. Do not write software that requires these bits to be read as 0.
3:0	**Software Configuration**. These bits are used to provide configuration information to the user's software by monitoring the status of the Software Configuration SW6 positions listed below. An open switch reads back a 0; a closed switch reads back a 1. The bits correspond to switch positions as follows: **Bit 0** = SW6-1; **Bit 1** = SW6-2; **Bit 2** = SW6-3; **Bit 3** = SW6-4

System Register 6 (E4h)

Address Offset: E4h
Default Value: 0x00
Size 8 bits
Attribute: R/W

Bit	Description
7:5	**Reserved.** These bits are reserved and should not be modified by the user.
4:0	**Geographic Addressing.** CompactPCI defines several signal additions to the PCI specification. One of these is GA[4..0], used for geographic addressing on the backplane. Geographic addressing uniquely differentiates each board based upon the physical slot into which it has been inserted. Each backplane connector in a CompactPCI system has a unique encoding for GA[4..0]. See the *CompactPCI Specification, PICMG 2.0, Version 3.0* for more information on geographic addressing. The bits correspond to signals as follows: **Bit 0** = GA0; **Bit 1** = GA1; **Bit 2** = GA2; **Bit 3** = GA3; **Bit 4** = GA4.

System Register 7 (E5h)

Address Offset: E5h
Default Value: 0x00
Size 8 bits
Attribute: R/W

Bit	Description
7	**Video/Keyboard Enable**. This bit is used to allow software to enable video and keyboard interfaces. A 1 routes video signals to the video pass through connector J17 and keyboard signals to connectors J16 and J3; a 0 disables the video and keyboard signals. Software control of these interfaces can be overridden via a switch setting on the IOX board (ZT 96072 or ZT 96073)
6	**Software Reset**. This bit issues a software reset to the CPU. Writing a 1 to this bit resets the board.
5:4	**Reserved.** These bits are reserved and should not be modified by the user.
3:2	**User LED 2.** These bits set the status of User LED 2. Bit 2 sets the LED's color as follows: 0=red; 1=green. Bit 3 enables/disables the driver for the LED as follows: 0=disabled; a 1=enabled.
1:0	**User LED 1.** These bits set the status of User LED 1. Bit 0 sets the LED's color as follows: 0=red; 1=green. Bit 1 enables/disables the driver for the LED as follows: 0=disabled; a 1=enabled.

ZT 4804 RPIO SMBus Registers

The ZT 4804's SMBus implementation provides two 8-bit registers for I/O and control functions. These registers are presented below.

ZT 4804 SMBus Output Register

Bit	Description
7	Control the ACO LED state
6	Clear the ACO switch latch state
5	Control the Minor Visual relay state
4	Control the Minor Audible relay state
3	Control the Major Visual relay state
2	Control the Major Audible relay state
1	Control the Critical Visual relay state
0	Control the Critical Audible relay state

ZT 4804 SMBus Input Register

Bit	Description
7	Read the state of option strap bit ID1
6	Read the state of option strap bit ID0
5	Read the status of the local 3.3V DC-DC converter
4	Read the state of the ACO switch latch
3	Not used
2	Not used
1	Read the state of the EXT2 input
0	Read the state of the EXT1 input

D. Agency Approvals

This appendix presents agency approval and certification information for the ZT 5550 High Availability System Master CPU Board with Pentium III Processor.

UL 1950 Certification

Underwriters Laboratories, Inc.*

Safety: UL Safety of Information Technology Equipment, including Electrical Business Equipment IEC 950 and UL 1950 (UL file # E179737)

CE Certification

The ZT 5550 meets intent of Directive 89/336/EEC for Electromagnetic Compatibility & Low-Voltage Directive 73/23/EEC for Product Safety. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 50081-1 Emissions:

EN 55011	Class A Radiated CISPR Pub 22
EN 605555-2	AC Power Line Harmonic Emissions CISPR Pub 22

EN 50082-1 Immunity:

EN 61000 4-2	Electro-static Discharge (ESD)
EN 61000 4-3	Radiated Susceptibility 30 to 100 MHz
ENV 50204	900 MHz Carrier
EN 61000 4-4	Electrical Fast Transient Burst (EFTB)
EN 61000 4-5	Surge, per Power Cord
EN 61000 4-6	Conducted Immunity 150 KHz to 30 MHz
EN 61000 4-8	Power Frequency Magnetic Fields
EN 61000 4-11	Voltage dips, Variations, & Short Interruptions

Low Voltage Directive 73/23/EEC:

UL 1950/EN 60950	Safety of Information Technology Equipment, Including Electrical Business Equipment

FCC Regulatory Information

Regulatory information Federal Communications Commission (FCC) (USA only)

Warning: This equipment has been tested and found to comply with the limits for a Class A or B digital device, pursuant to FCC 47 CFR Part 15, Subpart B, Class A or B of the FCC Rules. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

Intel system RFI and Radiated Immunity tests were conducted with Intel-supported peripheral devices and Intel shielded cables. Changes or modifications not expressly approved by Intel could result in EMI interference. FCC compliance was achieved under the following conditions:

- Shielded signal cables and a shielded power cord.
- Shielded cables on all I/O ports.
- Cable shields connected to earth ground via metal shell connectors.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above are implemented; failure to do so could compromise the FCC compliance of the equipment containing the system.

E. Data Sheet Reference

This appendix provides links to data sheets, standards, and specifications for the technology designed into the boards in your system.

AGP Video

For more information on Intel's Accelerated Graphics Port (AGP) technology, visit their website at:

http://developer.intel.com/technology/agp/

Board Serial # ID

Refer to the Dallas Semiconductor *DS2401 Silicon Serial Number* data sheet for more information about the DS2401 device. The data sheet is in Adobe* Acrobat* format (PDF) and available online at:

http://dbserv.maxim-ic.com/quick_view2.cfm?qv_pk=2903

CompactFlash

For more information about CompactFlash, visit the CompactFlash Association's website at:

http://www.compactflash.org/

CompactPCI

The *CompactPCI Specification, PICMG 2.0, Version 3.0* can be purchased from PICMG (PCI Industrial Computers Manufacturers Group) for a nominal fee. A short form specification in PDF format is also available on PICMG's website at:

http://www.picmg.org/compactpci.stm

Ethernet

Refer to the Intel *21143 PCI/CardBus* LAN Controller* data sheet for more information on the Ethernet LAN Controller. The data sheet is available online at:

http://developer.intel.com/design/network/

Refer to the Intel *LXT970 Dual-Speed Fast Ethernet Transceiver* data sheet for more information on the ZT 5550's Ethernet Physical Interface. The data sheet is in Adobe Acrobat format (PDF) and available online at:

http://www.intel.com/design/network/

Hot Swap

For a complete definition of CompactPCI Hot Swap, obtain a copy of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0.* The document is available for a nominal fee from PICMG at:

http://www.picmg.org

PCI-to-PCI Bridge

To obtain data sheets for the PCI-to-PCI bridges used on the ZT 5550 CPU (21154), visit the Intel website addressed below.

http://developer.intel.com/design/bridge/datashts/

Pentium III Processor

For more information about Intel Pentium III Processor Mobile Module, see the Intel *Pentium III Processor Mobile Module: Mobile Module Connector 2 (MMC-2)* data sheet and the *Mobile Pentium III Processor Specification Update*. Both documents are in Adobe Acrobat format (PDF) and are available online at:

http://developer.intel.com/design/mobile/datashts/245304.htm

http://www.intel.com/design/mobile/SPECUPDT/245306.htm

PIIX4

For more information on the following ZT 5550 functions, refer to the Intel *82371AB (PIIX4) PCI ISA IDE Xcelerator* data sheet and the Intel *82371EB (PIIX4E)* specification update.

- USB
- Counter/Timers
- DMA controllers
- Real-Time Clock
- Interrupt controllers

- Reset Control register
- EIDE Interface Controller

Both documents are available online at:

http://developer.intel.com/design/chipsets/datashts/index.htm

http://developer.intel.com/design/chipsets/specupdt/index.htm

SDRAM

Specifications for the SDRAM module used on the ZT 5550 are in Adobe Acrobat format (PDF) and are available online at:

http://developer.intel.com/technology/memory/pcsdram/

SuperI/O

Refer to the National Semiconductor *PC87309 SuperI/O Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging* data sheet for more information on the following ZT 5550 functions:

- Floppy Disk controller
- Serial Port controller
- Mouse and Keyboard controller
- Parallel Port

The data sheet is available online at:

http://www.national.com/ds/PC/

Thermal

For more information on the heat pipe implemented on the ZT 5550, visit Thermacore's website at:

http://www.thermacore.com

Refer to the Dallas Semiconductor *DS1705 3.3 and 5.0Volt Micromonitor* data sheet for more information about the DS1705 micromonitor. The data sheet is in Adobe Acrobat format (PDF) and is available online at:

http://dbserv.maxim-ic.com/quick_view2.cfm?qv_pk=2761

For more information about the key features of the integrated thermal sensor within the Mobile Pentium III Processor and Pentium III processor Mobile Module, refer to the Intel *AP-825 Mobile Pentium II Processor and Pentium II Processor Mobile Module Thermal Sensor Interface Specifications.* This document provides a specification for the programming interface and describes the key registers needed in order to program the thermal sensor. The document, available in Adobe Acrobat format (PDF), is available online at:

http://developer.intel.com/design/mobile/applnots/243724.htm

User Documentation

The latest Intel NetStructure product information and manuals are available on the Intel NetStructure Website at http://www.intel.com/network/csp/products/cpci_index.htm.

F. Customer Support

This appendix offers technical and sales assistance information for this product, and information on returning an Intel NetStructure product for service.

Technical Support and Return for Service Assistance

For all product returns and support issues, please contact your Intel product distributor or Intel Sales Representative for specific information.

Sales Assistance

If you have a sales question, please contact your local Intel NetStructure Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information is available at Intel's website, located at http://www.ziatech.com.

Intel Corporation

1050 Southwood Drive

San Luis Obispo, CA 93401 USA

Tel (805) 541-0488

FAX (805) 541-5088

Warranty Information

Intel NetStructure products manufactured by Intel are covered from the date of shipment by a warranty against defects in materials and workmanship. See the Intel website (http://www.intel.com/network/csp/products/cpci_index.htm) for warranty details.