Ziatech ZT 6500

Single Board Computer with Pentium Processor

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ZT 6500

Single Board Computer
with Pentium® Processor

ZIATECH CORPORATION

CONTENTS

WHAT'S IN THIS MANUAL?

This manual describes the operation and use of the ZT 6500 Single Board Computer with Pentium® Processor. The following summarizes the focus of each major section in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 6500. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 6500 against the needs of a specific application.

Chapter 2, "Getting Started," summarizes the information needed to install and configure your ZT 6500.

Chapter 3, "CompactPCI Interface," presents a detailed description of the ZT 6500 interface to the CompactPCI bus. The topics discussed include compatibility and interrupt structure.

Chapter 4, "Interrupt Controller," describes the two Intel-compatible 8259 cascaded interrupt controllers. This chapter summarizes and illustrates the interrupt sources and the interrupt controllers' programmable registers.

Chapter 5, "Counter/Timers," discusses the three programmable counter/timers. It includes a diagram of the counter/timer architecture, a summary of operating modes, and descriptions of the programmable registers.

Chapter 6, "DMA Controller," provides an overview of ZT 6500 DMA architecture and DMA controller operation. Descriptions of DMA controller programmable registers are also included.

Chapter 7, "Real-Time Clock," lists the major features of the real-time clock and provides register descriptions.

Chapter 8, "Serial Controller," discusses operation of the two serial ports and provides register descriptions.

Chapter 9, "IEEE 1284 Parallel Port Interface," contains descriptions of the programmable registers for the IEEE-1284 compatible printer interface.

Chapter 10, "Optional Floppy Disk Interface," covers the mounting and enabling of an optional local floppy disk interface.

Chapter 11, "System Registers," provides register descriptions and a brief overview of the System registers used to control and monitor a variety of functions on the ZT 6500.

Chapter 12, "Watchdog Timer," explains operation of the watchdog timer and includes code for arming and strobing the timer.

Chapter 13, "Parallel I/O," explains the operation and use of the ZT 6500's digital I/O outputs.

Chapter 14, "Programmable LED," provides code for turning the LED on and off.

Chapter 15, "Thermal Considerations," addresses the special cooling issues associated with the Pentium processor.

Chapter 16, "Flash Memory," discusses on-board Flash memory, including the system BIOS EEPROM. Recovery from BIOS EEPROM corruption and BIOS EEPROM modification are covered in this chapter.

Appendix A, "Board Configuration," describes the software configuration registers, jumpers, and cuttable traces on the ZT 6500. This appendix details factory default settings as well as information to tailor your board to a specific application.

Appendix B, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 6500. It also provides illustrations of cables and connector pinouts, and tables showing connector pin assignments.

Appendix C, "PIA System Setup Considerations," offers tips for safely connecting the parallel I/O to external devices.

Appendix D, "PCI Configuration Space Map," presents the generic layout of the PCI Configuration Header for all PCI compliant devices. It also contains a table showing the PCI bus mapping of the ZT 6500's on-board devices.

Appendix E, "Customer Support," offers a product revision history, technical assistance and warranty information, and the necessary information should you need to return your ZT 6500 for repair.

Appendix F, "Agency Approvals," presents agency approval and certification information for the ZT 6500 Single Board Computer.

ERRATA

A system including a ZT 6500 and a peripheral master may experience the following condition: When the peripheral master accesses peripherals other than those on board the ZT 6500, the ZT 6500 chipset asserts DEVSEL erroneously and will not allow any master, even the ZT 6500, to own the bus, thereby hanging the system. If you experience this problem, please contact Ziatech Corporation. There are no known issues with a peripheral master accessing peripherals or memory on board the ZT 6500.

Note for ZT 6620 customers

Ziatech does not support use of the ZT 6620 Wide SCSI Interface Revision D in systems with the ZT 6500. Earlier revisions of the ZT 6620 are supported for use with the ZT 6500.

CHAPTER 1. INTRODUCTION

This chapter provides a brief introduction to the ZT 6500. It includes a product definition, a list of product features, a functional block diagram, and a description of each block. Unpacking information and installation instructions are found in Chapter 2, "Getting Started."

PRODUCT DEFINITION

The ZT 6500 is a highly integrated, single board computer that is factory configured to operate with the Pentium® (P54C) family of microprocessors. The board meets the needs of a wide range of industrial control and processing applications.

The ZT 6500 does not require a CompactPCI™ bus backplane to operate. The ZT 6500 is able to operate stand-alone in many applications because of the large selection of the most commonly needed peripheral devices. On-board peripheral devices include:

- 2 or 4 Mbyte Flash file system for disk support
- Optional floppy disk interface
- Keyboard controller
- Serial I/O
- Printer interface
- Speaker interface
- Interrupt controllers
- Counter/timers
- Watchdog timer
- Real-time clock

FEATURES OF THE ZT 6500

- CompactPCI Bus Specification, Rev. 2.1 compliant
- Supports Pentium processor CPUs to 200 MHz
- Built-in numeric coprocessor support (Pentium)
- 16 Kbytes of CPU cache (expandable with L2 cache)

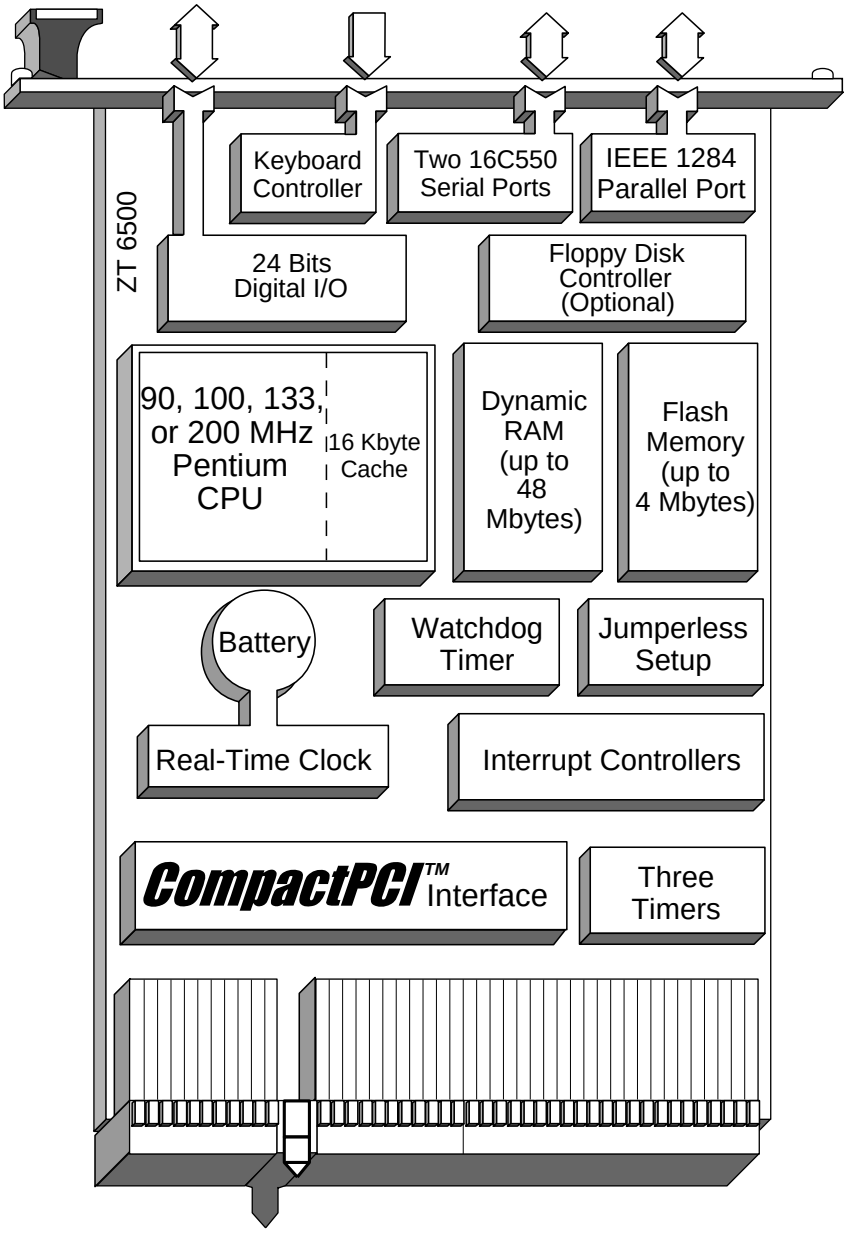
- Optional floppy disk interface (local to ZT 6500)
- 8, 16, 32, or 48 Mbytes of DRAM memory
- 2 Mbytes of Flash memory (expandable to 4 Mbytes)
- Standard AT® peripherals include:
  - —Two enhanced interrupt controllers (8259)
  - —Three counter/timers (one 8254)
  - —Real-time clock/CMOS RAM (146818)
  - —Two enhanced DMA controllers (8237)
  - —8042 compatible keyboard controller
- Centronics printer port (ECP/EPP compatible)
- Two 16C550 RS-232 serial ports
- Single stage watchdog timer
- Speaker interface
- On-board high efficiency 3.3 V DC-DC converter
- Push-button reset
- Software programmable LED
- DC power monitors (3.3 V and 5 V)
- Compatible with the following software: MS-DOS®, OS/2®, UNIX®, QNX®, VRTX32®, Windows™ 3.1 and 3.11, Windows 95, and Windows NT
- +5 V-only operation (fan/heatsink requires +12 V)
- Burned in at 55° Celsius and tested to guarantee reliability
- Five-year warranty

DEVELOPMENT CONSIDERATIONS

Ziatech offers a DOS software development system for ZT 6500 applications. Ziatech DOS is Microsoft's MS-DOS residing on the ZT 6500. The DOS system provides a development platform similar to a PC, enabling applications to be developed quickly. DOS includes support for many of the ZT 6500 peripherals and is supported by a large number of development tools such as program editors, compilers, assemblers, and debuggers. Refer to the Ziatech system manual for configuration and operating instructions.

FUNCTIONAL BLOCKS

The figure below illustrates a functional block diagram of the ZT 6500. The following topics provide overviews of the functional blocks.



Functional Block Diagram

CompactPCI Bus Interface

The ZT 6500 operates in a CompactPCI system. The CompactPCI standard is electrically identical to the PCI local bus standard but has been enhanced to support

rugged industrial environments and more slots. The standard is based upon a standard 3U card size and uses a rugged pin-in-socket connector.

See Chapter 3, "CompactPCI Interface" for a detailed description of the ZT 6500 interface to the CompactPCI bus architecture.

Pentium Processors

The ZT 6500 supports the second generation Pentium processor family, commonly referred to as the P54C. The P54C is a 3.3 V processor and operates at higher frequencies and lower power than did the first generation Pentium (P5). The ZT 6500 operates the external microprocessor bus at either 50, 60, or 66 MHz. The P54C operates internally at 1.5x, 2x, 2.5x, or 3x the microprocessor bus, supporting potential Pentium internal operation at up to 200 MHz.

The "Pentium Processor Comparison" table indicates the possible operating frequencies of the ZT 6500. The PCI bus always operates at 1/2 the external microprocessor bus speed. Not all processor speeds are offered by Ziatech, nor will Intel necessarily offer all speeds below. Contact Ziatech for latest product offerings.

The Pentium processor includes 16 Kbytes of cache (referred to as L1 cache). This L1 cache supports both write-through and write-back cache. A secondary 256 Kbyte cache (L2 cache) option is available to further enhance memory performance. Contact Ziatech for details on availability of the L2 cache option.

Pentium Processor Comparison

Processor Speed (MHz)	Internal Clock Multiplier	External Processor Speed	PCI Operating Frequency
90	1.5X	60.0	30.0
100	1.5X	66.6	33.3
120	2.0X	60.0	30.0
133	2.0X	66.6	33.3
150	2.5X	60.0	30.0
166	2.5X	66.6	33.3
200	3.0	66.6	33.3

Memory and I/O Addressing

The ZT 6500 includes two custom 72-pin DRAM sockets that can accommodate up to 48 Mbytes of local DRAM. In addition to DRAM, the ZT 6500 can support up to 4 Mbytes of flash memory. The flash memory contains the system BIOS, with the remainder allocated as solid state disk.

All memory and I/O addresses are forwarded to the PCI bus; thus any device on the PCI bus has access to the full memory and I/O address range. Any I/O or memory addresses that are not actively decoded are taken (subtractively decoded) by the ISA bridge on the ZT 6500. All of the ZT 6500's on-board peripherals are located on the ISA side of the bridge or on the bridge itself.

Digital I/O

The ZT 6500 contains three 8-bit digital I/O ports for a total of 24 digital I/O lines. Each line is programmable as an input or an output with readback. The outputs sink 12 mA and do not glitch during power-up or power-down. The 24 lines are available through the multi-I/O connector.

Serial I/O

Two 16C550 PC-compatible serial ports are available. The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through the multi-I/O frontplane connector. The ZT 90206 cable converts the serial interface to a standard 9-pin D-shell connector. A null-modem option is available to convert the DTE configuration to DCE. Adapter board options are also available to convert the RS-232 interface to an RS-485 interface. For more information on ZT 6500's serial ports, see Chapter 8, "Serial Controller."

Interrupts

Two enhanced 8259 style interrupt controllers provide a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Fixed and rotating priorities
- Individual input masking

Interrupt sources include:

- Counter/timers
- Serial I/O
- Real-time clock
- Keyboard
- Printer
- Floppy disk
- IDE interface
- Digital I/O
- CompactPCI backplane (four interrupts)

Enhanced capabilities include the ability to configure each interrupt level for active high going edge or active low level inputs.

See Chapter 4, "Interrupt Controller," for more information on the ZT 6500's two interrupt controllers. This chapter summarizes and illustrates the interrupt sources and the interrupt controllers' programmable registers.

Counter/Timers

Three 8254 style counter/timers are included on the ZT 6500 as defined for the PC/AT. Operating modes supported by the counter/timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot. See Chapter 5, "Counter/Timers," for more information.

DMA

Two enhanced 8237 style DMA controllers are provided on the ZT 6500 for use by the on-board peripherals. DMA channel 2 is assigned to the optional floppy drive and DMA channels 0 or 3 (cuttable trace options CT5 and CT6) are assigned to the parallel printer port (for advanced mode support—see chapter 9, "IEEE-1284 Parallel Port Interface).

See Chapter 6, "DMA Controller," for more information.

RESET

The ZT 6500 is automatically reset with a precision voltage monitoring circuit that detects when Vcc is below the acceptable operating limit of 4.75 V. In addition, the on-board 3.3 V power supply is monitored and resets the ZT 6500 when below 3.0 V. Other sources of reset include the watchdog timer, local pushbutton switch, and the CompactPCI bus reset signal, PRST* (CT21 must be installed).

The ZT 6500 responds to any of these reset sources by initializing local peripherals and driving the CompactPCI bus reset, PCIRST*.

Watchdog Timer

The watchdog timer optionally monitors system operation. Failure to strobe the watchdog timer within a set time period results in a system reset. Chapter 12, "Watchdog Timer," explains operation of the watchdog timer and includes code for arming and strobing the timer.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS SETUP information.

Chapter 7, "Real-Time Clock," lists the major features of the real-time clock and provides register descriptions.

Keyboard Controller

The ZT 6500 includes an on-board PC/AT® keyboard controller that is available through the multi-I/O connector.

IEEE 1284 Parallel Port/Printer Interface

The ZT 6500 includes an IEEE® 1284 compatible parallel port for connection to a printer or other parallel port devices such as software keys required by many application packages. The parallel port is ECP/EPP compatible.

The printer interface is available through the multi-I/O frontplane connector. An optional cable (ZT 90206) is available to interface the parallel port to a 25-pin D-shell connector for software key or printer support. The mode (Normal, Extended, EPP, ECP) for the printer interface is selectable through the BIOS SETUP mechanism (see the section "ZT 6500 Setup" in Chapter 2).

Chapter 9, "IEEE 1284 Parallel Port Interface," contains descriptions of the programmable registers for the IEEE-1284 compatible printer interface.

Speaker Interface

The ZT 6500 supports an external AT-compatible speaker through the multi-I/O frontplane connector.

Optional Floppy Interface

The ZT 6500 can be ordered (Option F1) with an on-board floppy interface connector for connection to a floppy drive. This option is useful in development systems for transferring files and installing software. This option includes a 3.5", 1.44 Mbyte floppy drive mounted on a carrier board that is attached to the solder side of the ZT 6500. When used in the CompactPCI backplane, the floppy drive occupies one additional slot to the left of the ZT 6500. See Chapter 10, "Optional Floppy Interface" for more information.

CHAPTER 2. GETTING STARTED

This chapter summarizes the information needed to make the ZT 6500 operational. Read this chapter before attempting to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Do not return any product to Ziatech without a Return Material Authorization (RMA) number. The "Returning for Service" section in Appendix E, "Customer Support," explains the procedure for obtaining an RMA number from Ziatech.

WHAT'S IN THE BOX?

The items listed below are included with a ZT 6500 order. System level products, such as the DOS development package, include additional items not shown. If a system level product has been ordered, refer to the system manual for the packing list.

- ZT 6500 Single Board Pentium Computer in anti-static bag (save the anti-static bag for storing or returning the ZT 6500)
- Optional PCI peripherals
- Optional cables

WARNING!

Like all equipment utilizing MOS devices, the ZT 6500 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 6500 to handle the board.

SYSTEM REQUIREMENTS

The ZT 6500 is designed for use with or without a CompactPCI bus backplane. The ZT 6500 is electrically, mechanically, and functionally compatible with the *CompactPCI Bus Specification, Rev. 2.1*.

Ziatech recommends vertical mounting. The ZT 6500 is supplied with an integrated processor fan/heatsink to allow operation between 0° and 55° C ambient. Refer to Appendix B for additional specifications.

MEMORY CONFIGURATION

The ZT 6500 addresses up to 4 Gbytes of memory. The address space is divided between memory local to the board and memory located on the CompactPCI bus. Any memory not reserved or occupied by a local memory device (DRAM/Flash) is available to the CompactPCI bus.

The ZT 6500 is populated with several memory devices. Local DRAM is contained in a unique stackable memory architecture that supports up to 48 Mbytes of DRAM (using 16-Mbit DRAM technology). Each module is either 4 Mbytes or 8 Mbytes. Memory modules must be added in pairs due to the 64-bit memory architecture of the Pentium processor. Each layer of DRAM (up to three layers) must be configured differently to allow the stacked module to provide discrete addressing for the layer pair.

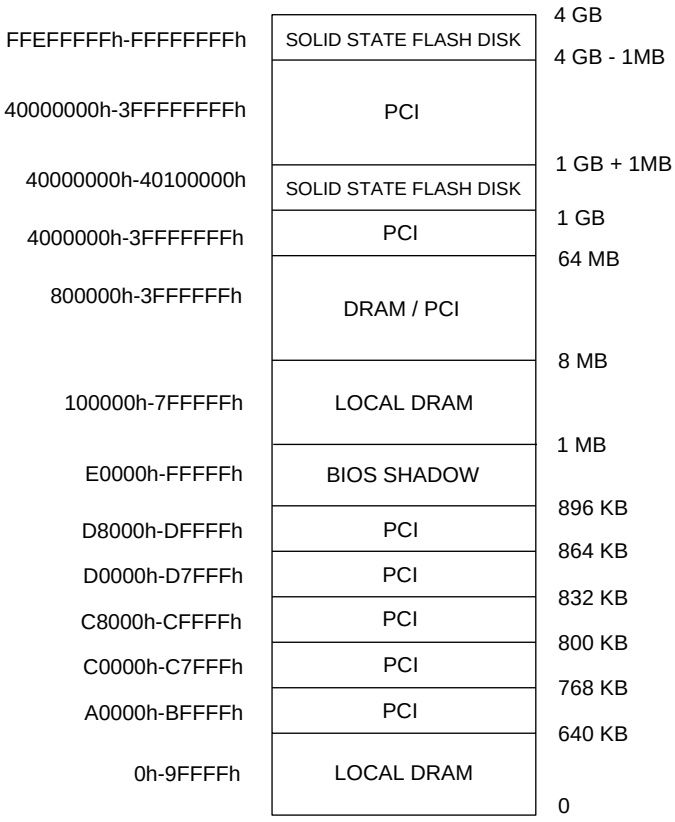
Additional DRAM may be installed on the ZT 6500 after the system has been purchased. Before contacting Ziatech to order additional DRAM, please take a moment to determine the amount of DRAM that is already loaded (how many layers and what size). The "Typical DRAM Configurations" table on the following page lists the typical DRAM configurations that are possible with the ZT 6500. Single sided DRAM modules have DRAM on just one surface. Double sided DRAM modules have DRAM on both sides.

Local Flash memory is soldered directly to the board. There is space for one Flash device, which may be either a 2 Mbyte or a 4 Mbyte device. The 2 Mbyte device does not require +12 V operation. The 4 Mbyte device does require +12 V +/- 5% for programming operations.

The "Memory Address Map" illustration on the following page shows default memory addressing for the ZT 6500.

Typical DRAM Configurations

Total System Memory	Number and Type of Modules
8 Mbytes	Two 4-Mbyte modules (layer 1)—single sided
16 Mbytes †	Four 4-Mbyte modules (layers 1 & 2)—single sided
16 Mbytes	Two 8-Mbyte modules (layer 1)—double sided
32 Mbytes	Four 8-Mbyte modules (layers 1 & 2)—double sided
48 Mbytes	Six 8-Mbyte modules (layers 1, 2 & 3)—double sided



ZT6500F02-01

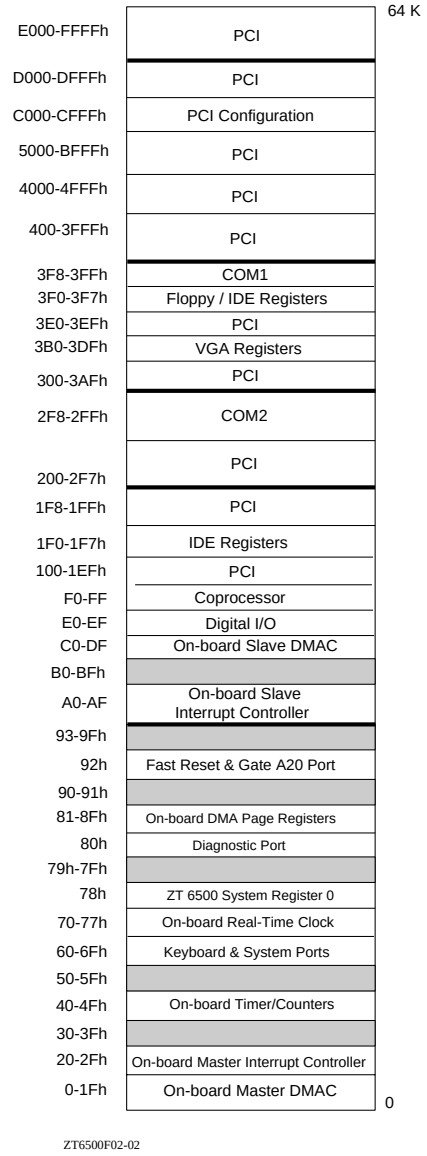
Memory Address Map

† Upgraded systems only

I/O CONFIGURATION

The ZT 6500 addresses up to 64 Kbytes of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the CompactPCI bus. Any I/O space not occupied by a local I/O device is available for the CompactPCI bus.

The ZT 6500 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Map" illustration.



I/O Address Map

CONNECTOR CONFIGURATION

As shown in the "Connector Locations" drawing below, the ZT 6500 includes several connectors to interface to application-specific devices. A brief description of each connector is given below. Refer to the "Connectors" section in Appendix B, "Specifications," for more complete connector descriptions, pinouts, and cable information.

Connector Assignments

J1 Multi-I/O connector including DMA, Interrupts

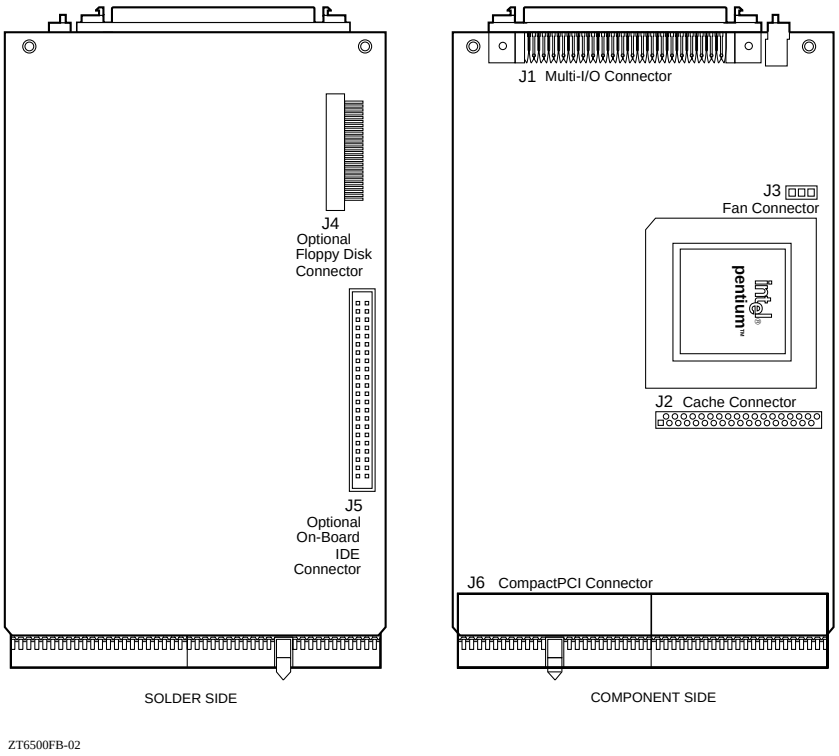
J2 Optional L2 cache module

J3 Fan Connector

J4 Floppy disk controller interface (OEM Option)

J5 IDE hard disk interface (available only as a special option)

J6 CompactPCI local bus interface



Connector Locations

JUMPER DESCRIPTIONS

The ZT 6500 includes a few jumper options for features that cannot be provided through the software SETUP mechanism. The jumpers are all located in the upper left corner of the board near the battery. Refer to Appendix A, "Board Configuration," for details.

ZT 6500 SETUP

The following topics present a brief introduction to the setup and configuration of the ZT 6500. For documentation specific to the BIOS and other utilities, see the Ziatech Industrial BIOS manual (shipped with Ziatech Development Systems).

System Configuration Overview

The Ziatech Industrial BIOS and MS-DOS operating system software is preprogrammed in the ZT 6500's on-board Flash memory. The BIOS includes embedded support to allow the ZT 6500 Flash memory to be used as a solid-state drive (SSD) in the MS-DOS environment. Ziatech also supplies SSD support for other popular operating systems such as Windows NT and QNX (contact Ziatech for SSD drivers for specific operating systems).

The ZT 6500 is configured during the boot sequence by the BIOS. The BIOS uses system configuration information stored as SETUP parameters.

> To access the SETUP utility, either boot the system and press the **"S"** key during the system RAM check or, run the SETUP.COM utility from the MS-DOS prompt.

The SETUP parameters are saved in the battery-backed RAM portion of the ZT 6500's real-time clock device.The SETUP parameters can also be saved in a file format, or as the programmed BIOS defaults.

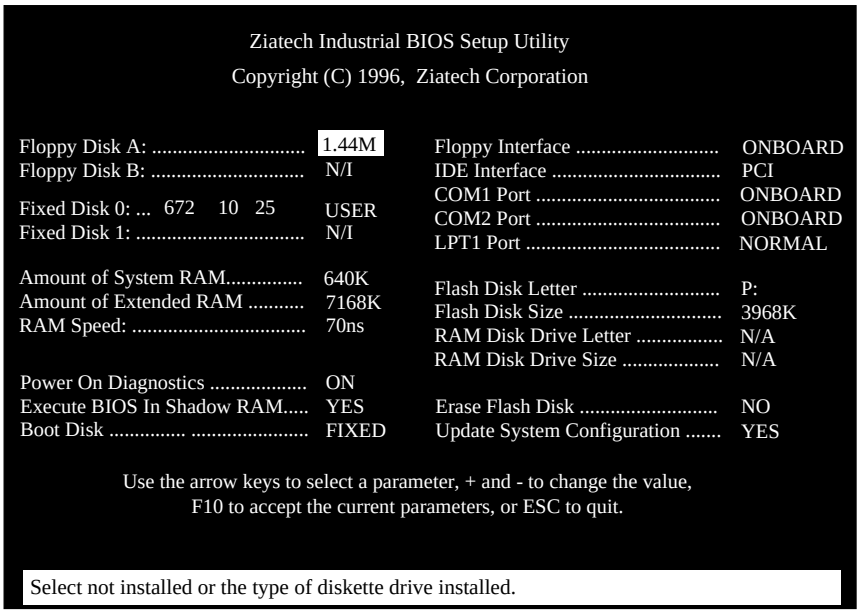
When SETUP is run, an interactive configuration screen is displayed, as shown in the "BIOS SETUP Utility Screen Example" illustration on the following page.

Note: the SETUP program is a generic utility used for all Ziatech processor boards. Some parameters not applicable to the ZT 6500 may be labeled "N/A".

The BIOS SETUP screen is organized as a single screen. The SETUP screen allows the user to select options for such items as base memory and extended memory size selection, boot source, hard disk type, and floppy disk type.

The parameters in the SETUP screen are easily changed. Use the arrow keys to select a parameter, then press + or - to step through the valid choices for that parameter. A dynamic help line at the bottom of the screen helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter

invalidates another parameter, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them.



ZT6500F02-03

BIOS SETUP Utility Screen Example

System Configuration Example

It is usually necessary to install an operating system such as Windows NT or QNX on the ZT 6500 system. This section describes the generic OS installation process. For OS-specific information, refer to the documentation provided by the OS vendor.

Note: if the installation requires a CD-ROM drive, the appropriate drivers must first be installed in order to access the CD-ROM drive.

1. Use the SETUP utility (shown in the "BIOS SETUP Utility Screen Example" illustration above) to configure the appropriate peripheral devices. Note that the Fixed Disk parameters (used for EIDE drives) include an "AUTO" setting which will cause SETUP to query the drive to determine the correct geometry (cylinders/heads/sectors).

2. Select the proper boot source in the SETUP utility depending on the OS installation media that will be used. For example, if the OS includes a bootable installation floppy, select "FLOPPY" for "Boot Disk" and reboot the system with the installation floppy installed in the floppy drive.

3. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. See the "ZT 6500 On-Board Device PCI Bus Mapping" table in Appendix D for a list of the PCI devices used on the ZT 6500.

4. When installation is complete, the system should be rebooted and the SETUP "Boot Disk" parameter should be set for the appropriate boot media.

CHAPTER 3. CompactPCI INTERFACE

The ZT 6500 operates with the CompactPCI bus architecture to support additional I/O and memory mapped devices as required by the application. This chapter gives a brief overview of the CompactPCI architecture and its effect on the operation of the ZT 6500.

Information about some important differences between the *CompactPCI Specification, Rev. 2.1* and the ZT 6500 implementation is provided in "ZT 6500 Specifics" in the "CompactPCI Pin Definitions" section later in this chapter.

For more detailed information on CompactPCI, the complete specification can be purchased from PICMG (PCI Industrial Computers Manufacturers Group) for a nominal fee. A short form specification is also available on Ziatech's web site at http://www.ziatech.com.

CompactPCI OVERVIEW

CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification*. It has been optimized for industrial and/or embedded applications that require a more robust mechanical form factor than Desktop PCI. CompactPCI uses industry standard mechanical components and high performance connector technologies to provide a system well suited for rugged applications. CompactPCI provides a system that is electrically compatible with the PCI Specification, allowing low cost PCI components to be used. CompactPCI is an open standard supported by the PICMG (PCI Industrial Computer Manufacturers Group), which is a consortium of companies involved in utilizing PCI for embedded applications.

INTENDED APPLICATIONS

CompactPCI appeals to customers that require the following capabilities:

- PCI performance
- 32- and 64-bit data transfers
- 8 PCI slots per system
- Industry standard software support
- 3U small form factor (100 mm by 160 mm)
- 6U form factor (233 mm by 160 mm)
- Eurocard packaging
- Wide variety of available I/O

APPLICABLE DOCUMENTS

For more information on the PCI Local Bus Specification you should reference the following list of publications.

- *PCI Local Bus Specification*, PCI Special Interest Group, 5200 N. E. Elam Young Parkway, Hillsboro, Oregon, USA, 9724-6497, (503) 696-2000
- IEC 297-3, *Eurocard Specification*, Bureau Central de la Commission Electrotechnique Internationale, 1 rue de Varembe, Geneva, Switzerland, 011.412.291.90228
- IEC-1076-4-101, *Draft Specification for 2 mm Connector Systems*, International Electrotechnical Commission, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY, USA 10036
- IEEE 1101.1-1991, *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors*, Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331
- IEEE P1101.10-3.X, *IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE 1101.1 Equipment Practice,* Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331
- ANSI/VITA 1-1994, *VME64 Specification,* VITA, 10229 N. Scottsdale Rd., Suite B, Scottsdale, AZ, USA, 85253

FEATURE SET

The following topics provide an overview of the key features of CompactPCI, including PCB form factor, the CompactPCI connector, and system modularity.

Form Factor

The form factor defined for CompactPCI boards is based upon the Eurocard industry standard. Both 3U (100 mm by 160 mm) and 6U (233 mm by 100 mm) board sizes are defined. The figure "3U 64-Bit CompactPCI Form Factor" on the following page shows a 3U style board.

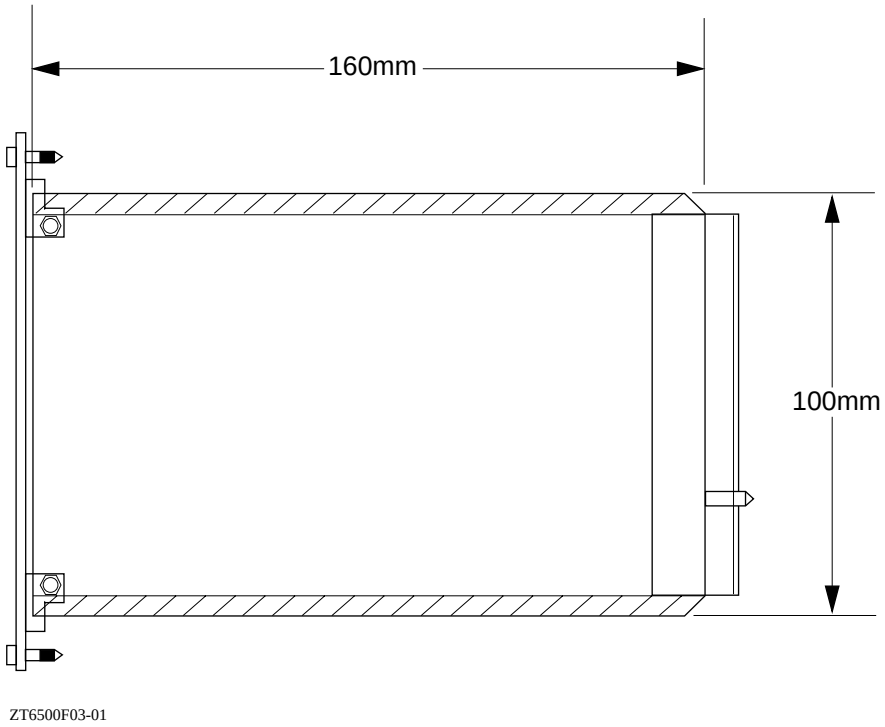
A CompactPCI system is composed of up to eight CompactPCI card locations with 20.32 mm (0.8 inch) board center-to-center spacing. The CompactPCI backplane consists of one System Slot, and up to seven Peripheral Slots.

The System Slot provides arbitration, clock distribution, and reset functions for all boards on the bus. The System Slot is responsible for performing system initialization by managing each local board's IDSEL signal. Physically, the System Slot may be

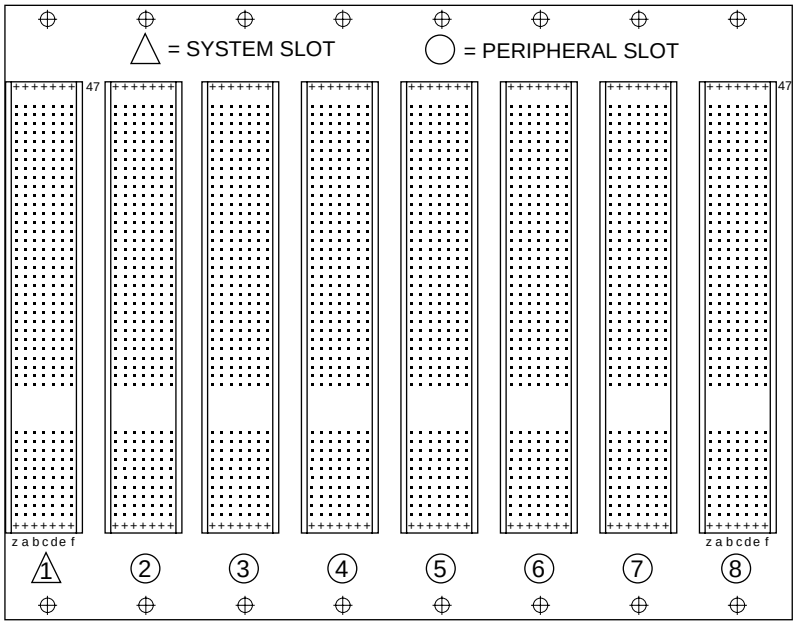
located at either end of the backplane. For simplicity, the CompactPCI specification assumes the System Slot is located on the left when the backplane is viewed from the connector side. ***The ZT 6500 is a system board and should be inserted into a system slot only.***

The Peripheral Slots may contain simple boards, intelligent slaves, or PCI bus masters. The "3U CompactPCI Backplane Example" figure on the following page illustrates a typical 3U CompactPCI backplane connector topology.

Other topologies besides the linear arrangement illustrated in the figure are allowed by CompactPCI. However, the specification and all backplane simulations have assumed a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing.



3U 64-Bit CompactPCI Form Factor



ZT6500F03-02

3U CompactPCI Backplane Example

Robust Connector

The CompactPCI connector is a shielded, 2 mm-pitch, 7-row connector as issued by AMP, Framatome, and ERNI as the 2 mm, Hard Metric (2 mm HM) connector for telecommunication and backplane applications (IEC 917 and IEC 1076-4-101). Features of this connector include:

- Pin and socket interconnect mechanism
- Multi-vendor support
- Coding Mechanism providing positive keying
- Staggered make-break pin populations for optional hot-swap capability
- Rear pin option for through-the-backplane I/O applications
- High density PCI capability
- High ground/signal ratio
- Shield for EMI/RFI protection
- Expandability for end user applications

CompactPCI is defined as a 7 column by 47 row array of pins divided logically into two groups corresponding to the physical connector implementation. See "ZT 6500

Specifics" in the "CompactPCI Pin Definitions" section later in this chapter for information about important differences between the *CompactPCI Specification, Rev. 2.1* and the ZT 6500 implementation.

The CompactPCI connector utilizes guide lugs located on the board connector to ensure correct polarized mating. Proper mating is further enhanced by the use of coding keys for 3.3 V or 5 V operation, with or without Hot-Swap capability, to prevent incorrect installation of boards.

Coding keys prevent inadvertent installation of a 5 V board in a 3.3 V system. The "Coding Key Color Assignments" table below illustrates the color coding that relates to different physical keys for the backplane connector and adapter board.

Coding Key Color Assignments

Operating Voltage V(I/O)	Color Reference
3.3 V	Cadmium Yellow
5 V	Brilliant Blue

CompactPCI BACKPLANE ARCHITECTURE

CompactPCI defines a backplane environment that allows up to eight boards. One slot, the System Slot, provides the clocking, arbitration, configuration, and interrupt processing for the other 7 slots. Fewer slots may be provided in a CompactPCI backplane, but the following sections assume that a maximum configuration is employed.

Backplanes must provide separate power planes for 3.3 V, 5 V, and ground.

Clock Routing

The System Slot drives five buffered clocks via CLK0-CLK4 (pins J1:D6, J2:A1, J2:A2, J2:B2, and J2:A3). Board slots receive their specific clock using the CLK pin (D6).

Signaling Environment

Each CompactPCI backplane provides for either a 5 V or 3.3 V signaling environment. PCI allows for two types of buffer interfaces for interboard connection. 5 V signaling will generally be used for early systems. A gradual shift to 3.3 V will occur as the semiconductor industry shifts to the lower power interface for speed and power dissipation reasons. The V(I/O) power pins on the connector are used to power the buffers on the peripheral boards, allowing a card to be designed to work in either interface.

CompactPCI allows for this dual interface scheme by providing a unique coding plug for either system. The CompactPCI backplane may be either a fixed signaling environment

backplane (e.g., 5 V only) or may be configurable. In any case, when configured for 5 V operation, the 5 V coding plug (Brilliant Blue) must be used, and when configured for 3.3 V operation, the 3.3 V coding plug (Cadmium Yellow) must be installed in the backplane.

With the above mechanism, boards that have the coding plug matching the backplane can be inserted. The opposite technology board is likewise inhibited from being inserted. Boards that can be either 3.3 V or 5 V do not require a coding plug and therefore can be inserted in either system.

IDSEL Assignment

The PCI signal IDSEL is used to provide unique access to each slot for configuration purposes. By connecting one of the address lines AD31 through AD25 to each board's IDSEL pin (J1:B9), a unique address for each board is provided during configuration cycles. The "System to Logical Slot Signal Assignments" table (see page 23) illustrates the assignment of address lines to each board's IDSEL pin.

PCI devices on a System slot CPU board can be selected using lower ADxx lines in the range of AD11 to AD24. There are two PCI peripherals on board the ZT 6500 (the memory cache controller and the system I/O controller) that use AD16 and AD17, respectively, for their IDSEL signals.

REQ#/GNT# Assignment

The System Slot interfaces to seven pairs of REQx#/GNTx# pins called REQ0#-REQ6# and GNT0#-GNT6#. Each board slot interfaces to one pair of REQx#/GNTx# signals using pins called REQ# (J1:A6) and GNT# (J1:E5). The "System to Logical Slot Signal Assignments" table (see page 23) lists the assignment of request/grant signals to each board's REQ# and GNT# pins.

If a System Slot board cannot support the full complement of REQ#/GNT# signals, CompactPCI backplane slots must be configurable to support arbitration. In this manner, boards using REQ#/GNT# signals may be located in any given slot as required by the application.

Note: The system board uses the pins labeled REQ# and GNT# as REQ0# and GNT0#, respectively. CLK1 and CLK0 are correct in the "System to Logical Slot Signal Assignments" table , although they seem reversed (see following page). This was done to facilitate trace routing and maintain equal trace lengths to minimize skew.

The ZT 6500 can support only five REQ#/GNT# pairs. Cuttable traces CT22 through CT25 allow the user to configure the slots that provide REQ#/GNT# (either the first or last five slots in an eight slot backplane). See Appendix A for the cuttable trace options.

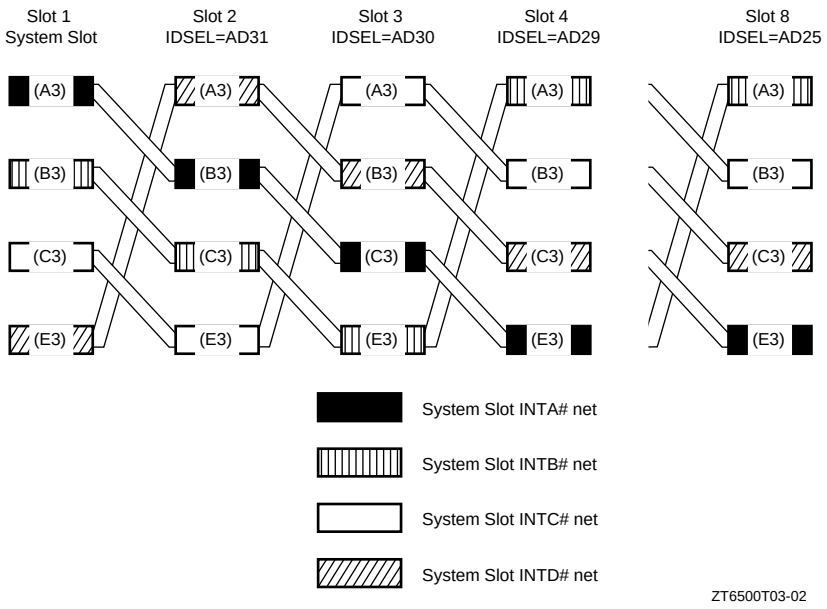
PCI Interrupt Binding

Interrupt binding of the BIOS setup program requires backplane assignments from the System Slot interrupt pins INTA#-INTD# to the logical board slot interrupts as defined in the "System To Logical Slot Interrupt Assignments" table below.

Backplane assignments rotate through logical board slots to provide a unique PCI interrupt to each board for the first four PCI connectors (assuming that each board drives just its INTA signal). Rotating interrupt assignments allows multiple PCI peripherals that drive only INTA# in order to utilize a different interrupt on the System Slot CPU without the need to share an interrupt with another PCI interface. Since multi-function PCI devices are allowed to drive more than one interrupt, shared interrupts may be required even within the first four board slots. In addition, the rotating pattern repeats itself after slot four, which also requires the sharing of an interrupt for slots that are four connectors apart (slots 2 and 6 for example).

Although PCI software device drivers are designed to allow sharing of interrupt signals, sharing an interrupt with another device can affect interrupt latency and is generally avoided where possible.

See the topic "Legacy IDE Interrupt Support" below for interrupt support for legacy IDE devices.



System To Logical Slot Interrupt Assignments

System to Logical Slot Signal Assignments

Signal	Pin	Signal	Pin
System Slot (△), Connector 1		**Peripheral Slot (○), Connector 2**	
CLK1 (1)	A26	CLK	D6
AD31	E6	IDSEL (3)	B9
REQ0#	A6	REQ#	A6
GNT0#	E5	GNT#	E5
System Slot (△), Connector 1		**Peripheral Slot (○), Connector 3**	
CLK1 (1)	A26	CLK	D6
AD30	A7	IDSEL (3)	B9
REQ1#	C26	REQ#	A6
GNT1#	D26	GNT#	E5
System Slot (△), Connector 1		**Peripheral Slot (○), Connector 4**	
CLK0 (1)	D6	CLK	D6
AD29	B7	IDSEL (3)	B9
REQ2#	E26	REQ#	A6
GNT2#	D27	GNT#	E5
System Slot (△), Connector 1		**Peripheral Slot (○), Connector 5**	
CLK0 (1)	D6	CLK	D6
AD28	C7	IDSEL (3)	B9
REQ3#	E27	REQ#	A6
GNT3#	C28	GNT#	E5
System Slot (△), Connector 1		**Peripheral Slot (○), Connector 6**	
CLK2	A27	CLK	D6
AD27	E7	IDSEL (3)	B9
REQ4#	D28	REQ#	A6
GNT4#	E28	GNT#	E5
System Slot (△), Connector 1		**Peripheral Slot (○), Connector 7**	
CLK3	B27	CLK	D6
AD26	A8	IDSEL (3)	B9
REQ5# (2)	D40	REQ#	A6
GNT5# (2)	E40	GNT#	E5
System Slot (△), Connector 1		**Peripheral Slot (○), Connector 8**	
CLK4	A28	CLK	D6
AD25	D8	IDSEL (3)	B9
REQ6# (2)	D42	REQ#	A6
GNT6# (2)	E42	GNT#	E5

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Notes:

(1) CLK0 and CLK1 are reversed to facilitate trace routing and maintain equal trace lengths to minimize skew.

(2) System Slot boards that do not support seven REQ#/GNT# signals must provide a mechanism to connect any of the Peripheral Slots 2-8 that may need arbitration service depending on the board installed.

(3) The IDSEL signal at each slot must be connected with minimal trace length at the slot that is intended. For example, at logical slot 6, IDSEL must be connected to AD27 with minimal trace length.

CompactPCI Signal Additions

CompactPCI utilizes PCI signals as defined by the *PCI Local Bus Specification* with some additional signals. These additional signals do not affect the PCI signals but rather enhance system operation by providing push-button reset, power supply status, System Slot identification, and legacy IDE interrupt support features.

Push-Button Reset (PRST#)

PRST# is an active low true TTL signal generated by a switch closure or an open-collector driver from any board in the system. It is the responsibility of all boards receiving PRST# to debounce it as required. The system board terminates PRST# with a pullup resistor. PRST# might be used in a CompactPCI system to reset the System Slot board which in turn would reset the rest of the system using the PCI RST# signal. This is implemented on the ZT 6500 as cuttable trace option CT21. See Appendix A for more information.

Power Supply Status (DEG#, FAL#)

Two low true TTL power supply status signals are available on backplanes utilizing modular power supplies implementing the optional DEG# and FAL# signals. The system board terminates both signals with a pullup resistor. These are implemented as cuttable trace options CT19 and CT20 on the ZT 6500. They are monitored through the on-board Digital I/O ASIC. See Appendix A and Chapter 11 for more information.

System Slot Identification (SYSEN#)

This pin is grounded on the backplane at the System Slot for the board to identify installation into the System Slot. This pin is tied to V(I/O) on the backplane for the remaining slots.

Legacy IDE Interrupt Support

Two additional non-PCI interrupts are defined for IDE adapters. Both a primary and secondary ISA interrupt, designated **INTP-** and **INTS-** respectively, are available for use by the CPU. The CPU routes the INTP- (pin D4) and INTS (pin E4) on board to interrupt requests IR14 and IR15, respectively. These signals are active high TTL level signals and do not have the requirement of meeting the PCI electrical buffer characteristics. INTP- and INTS- are provided to ease the transition from Compatibility Mode to Native Mode PCI IDE operation.

Compatibility Mode forces the IDE controller to be I/O mapped at the PC-AT location (1F0h-1F7h and 3F6h-3F7h) as well as forcing the use of IR14 and IR15 for hard disk interrupts.

Native Mode operation allows the IDE controller to be mapped at any location and also allows any interrupt that is available to be used for the hard disk interface.

These are implemented on the ZT 6500 as cuttable trace options CT10 and CT11. See Appendix A and Chapter 4 for more information.

CompactPCI PIN DEFINITION

The pinout for the CompactPCI connector is shown in the "CompactPCI Connector Pinout" table at the end of this chapter. The pin locations are shown in the "CompactPCI Connector Pin Locations" figure, also at the end of this chapter. The 32-bit PCI signals are defined by rows 1-25 on connector **J1** (corresponding to the **keyed** section of J6 on the ZT 6500—see "ZT 6500 Specifics" below). On peripheral boards, one connector can be used to implement a 32-bit board. Rows 12-14 on connector J1 are used for connector keying.

Rows 1-3 and 15-17 on connector **J2** (corresponding to the **non-keyed** section of J6 on the ZT 6500—see "ZT 6500 Specifics" below) are used on the System Slot board for adapter slot clocks and REQ#/GNT# pairs. Thus, System Slot boards use both the J1 and J2 connectors. The rest of the pins on connector J2 are used to support 64-bit CompactPCI or as user I/O.

Note: The number of System Slot signals utilized on connector J2 rows 1-3 and 15-17 depends on the total number of slots implemented for any given CompactPCI system.

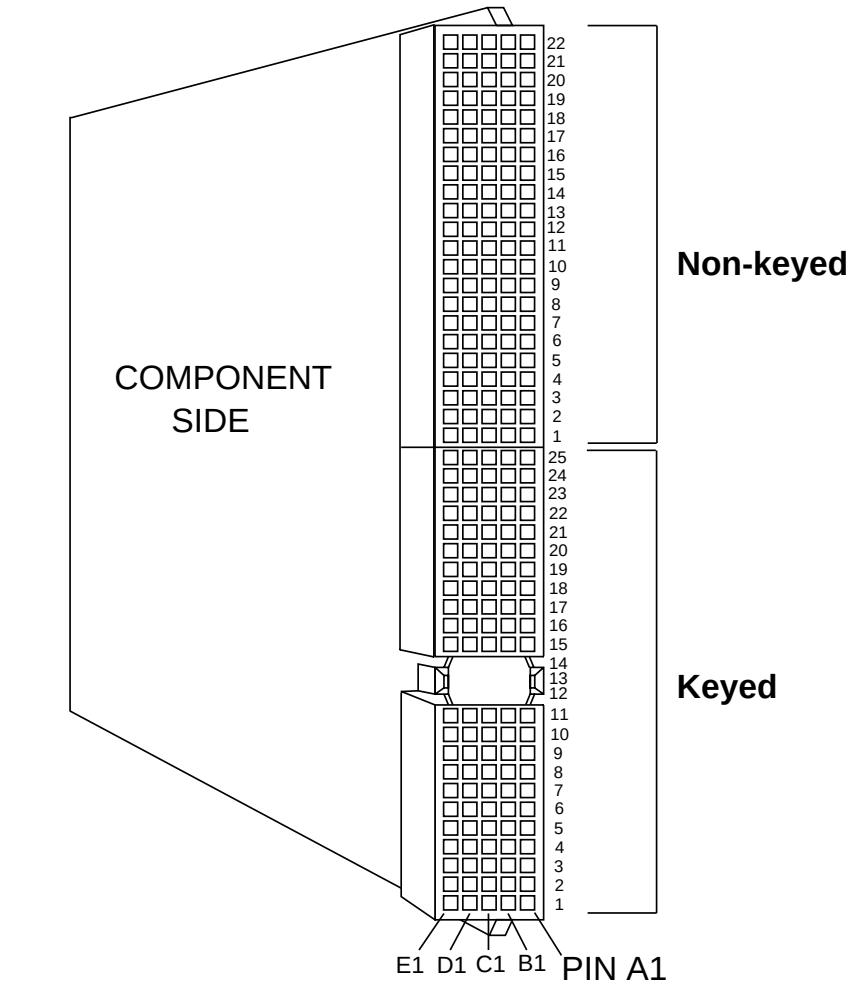
ZT 6500 Specifics

The CompactPCI bus connectors implemented on the ZT 6500 are numbered differently than they appear in the *CompactPCI Specification, Rev. 2.1*. See the table below.

ZT 6500		*CompactPCI Specification, Rev. 2.1*
J6 keyed	corresponds to	J1
J6 non-keyed	corresponds to	J2

In addition, on the ZT 6500—which is a 32-bit System Slot board—the unused 64-bit PCI pins on J6's non-keyed section are no-connects. See J6 in Appendix B for the pin assignments specific to the ZT 6500.

All CompactPCI connectors provide pins for +5 V, +3.3 V, +12 V and -12 V operating power. Additional power pins labeled +V(I/O) provide power for Universal boards utilizing I/O buffers driving backplane signals that can operate from +5 V or +3.3 V. On these boards, the PCI component's I/O buffers must be powered from V(I/O), not from +5 V or +3.3 V power pins. **The ZT 6500 ties the V(I/O) pins to +5 V; therefore, the ZT 6500 can only be used in +5 V backplane environments (Brilliant Blue keying)**.



ZT6500FB-03

CompactPCI Connector Pin Locations

CompactPCI Connector Pinout

22	**GND**	RSV	RSV	RSV	RSV	RSV	**GND**	**P2 / J2 CONNECTOR**
21	**GND**	RSV	**GND**	RSV	RSV	RSV	**GND**	
20	**GND**	RSV	RSV	RSV	**GND**	RSV	**GND**	
19	**GND**	RSV	**GND**	RSV	RSV	RSV	**GND**	
18	**GND**	BRSVP2A18 (12)	BRSVP2B18 (12)	BRSVP2C18 (12)	**GND**	BRSVP2E18	**GND**	
17	**GND**	BRSVP2A17 (12)	**GND**	PRST# (3)	REQ6# (3)(8)	GNT6# (3)(8)	**GND**	
16	**GND**	BRSVP2A16 (12)	BRSVP2B16 (12)	DEG# (3)	**GND**	BRSVP2E16	**GND**	
15	**GND**	BRSVP2A15 (12)	**GND**	FAL# (3)	REQ5# (3)(8)	GNT5# (3)(8)	**GND**	
14	**GND**	AD(35)	AD(34)	AD(33)	**GND**	AD(32)	**GND**	
13	**GND**	AD(38)	**GND**	**V(I/O)** (2)	AD(37)	AD(36)	**GND**	
12	**GND**	AD(42)	AD(41)	AD(40)	**GND**	AD(39)	**GND**	
11	**GND**	AD(45)	**GND**	**V(I/O)** (2)	AD(44)	AD(43)	**GND**	
10	**GND**	AD(49)	AD(48)	AD(47)	**GND**	AD(46)	**GND**	
9	**GND**	AD(52)	**GND**	**V(I/O)** (2)	AD(51)	AD(50)	**GND**	
8	**GND**	AD(56)	AD(55)	AD(54)	**GND**	AD(53)	**GND**	
7	**GND**	AD(59)	**GND**	**V(I/O)** (2)	AD(58)	AD(57)	**GND**	
6	**GND**	AD(63)	AD(62)	AD(61)	**GND**	AD(60)	**GND**	
5	**GND**	C/BE(5)#	**GND**	**V(I/O)** (2)	C/BE(4)#	PAR64	**GND**	
4	**GND**	**V(I/O)** (2)	BRSV	C/BE(7)#	**GND**	C/BE(6)#	**GND**	
3 (3)	**GND**	**CLK4**	**GND**	GNT3#	REQ4#	GNT4#	**GND**	
2 (3)	**GND**	**CLK2**	**CLK3**	SYSEN# (4)	GNT2#	REQ3#	**GND**	
1 (3)	**GND**	**CLK1**	**GND**	REQ1#	GNT1#	REQ2#	**GND**	
25	**GND**	**5V**	REQ64#	BRSV	**3.3V**	**5V**	**GND**	**P1 / J1 CONNECTOR**
24	**GND**	AD(1)	**5V**	**V(I/O)** (2)	AD(0)	ACK64#	**GND**	
23	**GND**	**3.3V**	AD(4)	AD(3)	**5V**	AD(2)	**GND**	
22	**GND**	AD(7)	**GND**	**3.3V**	AD(6)	AD(5)	**GND**	
21	**GND**	**3.3V**	AD(9)	AD(8)	M66EN (5)	C/BE(0)#	**GND**	
20	**GND**	AD(12)	**GND**	**V(I/O)** (2)	AD(11)	AD(10)	**GND**	
19	**GND**	**3.3V**	AD(15)	AD(14)	**GND**	AD(13)	**GND**	
18	**GND**	SERR#	**GND**	**3.3V**	PAR	C/BE(1)#	**GND**	
17	**GND**	**3.3V**	**SDONE**	**SBO#**	**GND**	PERR#	**GND**	
16	**GND**	**DEVSEL#**	**GND**	**V(I/O)** (2)(6)	**STOP#**	**LOCK#**	**GND**	
15	**GND**	**3.3V**	**FRAME#**	**IRDY#**	**GND** (7)	**TRDY#**	**GND**	
12-14	**KEY AREA**							
11	**GND**	AD(18)	AD(17)	AD(16)	**GND**	C/BE(2)#	**GND**	
10	**GND**	AD(21)	**GND**	**3.3V**	AD(20)	AD(19)	**GND**	
9	**GND**	C/BE(3)#	IDSEL	AD(23)	**GND**	AD(22)	**GND**	
8	**GND**	AD(26)	**GND**	**V(I/O)**	AD(25)	AD(24)	**GND**	
7	**GND**	AD(30)	AD(29)	AD(28)	**GND**	AD(27)	**GND**	
6	**GND**	REQ#	**GND**	**3.3V**	**CLK**	AD(31)	**GND**	
5	**GND**	BRSVP1A5 (12)	BRSVP1B5 (12)	RST#	**GND**	GNT#	**GND**	
4	**GND**	BRSVP1A4 (12)	**GND**	**V(I/O)**	INTP	INTS	**GND**	
3	**GND**	INTA#	INTB#	INTC#	**5V**	INTD#	**GND**	
2	**GND**	TCK	**5V**	TMS	TDO	TDI	**GND**	
1	**GND**	**5V**	**-12V**	TRST#	**+12V**	**5V**	**GND**	
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F** (9)	

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Notes:

The above is a generalized pinout for a 64-bit CPCI board and is identical to the "CompactPCI 64-Bit Connector Pin Assignments" table shown in the *CompactPCI Specification, Rev. 2.1.* See "ZT 6500 Specifics" in the "CompactPCI Pin Definitions" section of Chapter 3 for information about important differences between the *CompactPCI Specification, Rev. 2.1* and the ZT 6500 implementation.

1. This diagram defines the pinout from the front of the system chassis. Refer to the "System To Logical Slot Signal Assignments" table for pin assignment differences between the system and board slots. All pins are medium length (level 2), except C16 and D15, which are long (level 3) and short (level 1), respectively.

2. The V(I/O) signals are either 5 V or 3.3 V, depending on the system implementation.

3. Positions 1-3 of connector P2 (pins D17, D15, E17, E15, C15, C16 and C17) are only implemented on the system board. On Peripheral boards these signals are no connects.

4. Connector P2 pin C2 is grounded at the System Slot only. Remaining slots leave C2 unconnected. Boards that use this signal (e.g. CPU boards that may be used in the system slot or peripheral slot) must provide a local pull-up to V(I/O). System Slot only boards should tie this pin directly into the ground plane.

5. Connector P1 pin D21 (M66EN) is defined as GND for 33 MHz backplanes. Use of this signal in 66 MHz systems will be as a bused signal to all slots.

6. Connector P1 pin C16 (long, level 3) is used for early power to hot-swap capable boards for controlling the buffer logic.

7. Connector P1 pin D15 (short, level 1) is used as BD_SEL* for hot-swap capable boards.

8. System Slot boards must provide a mechanism to connect any of the Peripheral Slots 2-8 that may need arbitration service depending on the board installed.

9. Observation: Some manufacturers of top shields utilize every other ground pin while some use every ground pin.

10. CompactPCI connector pin numbering is intentionally different from the connector manufacturers pin numbering. This was done to maintain consistency with many other existing Eurocard specifications.

11. P1 and P2 connector tail lengths are defined to be "short" tail connectors with 4.5 mm tails.

12. BRSVPxxx signals map to PCI reserved signals per "The CompactPCI-to-PCI Reserved Signal Mapping" table. Bus segments must bus these signals even though the PCI specification defines these pins as no-connects.

CHAPTER 4. INTERRUPT CONTROLLER

The ZT 6500 includes two Intel-compatible 8259 cascaded interrupt controllers that provide a programmable interface between interrupt-generating peripherals and the CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device.

The major features of the interrupt architecture are listed below.

- 15 individually maskable interrupts
- Jumperless configuration
- Level-triggered or edge-triggered recognition
- Fixed or rotating priorities
- PCI Interrupt support
- PCI Extended Mode register support

The interrupt architecture is illustrated in the "Interrupt Architecture" figure on the following page. The ZT 6500 supports the Extended Mode register, which allows individual programming of low-level triggered or active high-edge triggered interrupts.

INTERRUPT SOURCES

The interrupt sources are summarized below.

PCI Interrupts

The CompactPCI bus interrupts have been assigned to IRQ9, IRQ10, IRQ11 and IRQ12 on the ZT 6500 PIC. These interrupts are automatically configured by the BIOS. The CompactPCI bus defines these four interrupts as INTA, INTB, INTC and INTD. These interrupts are all active low, level-triggered interrupts.

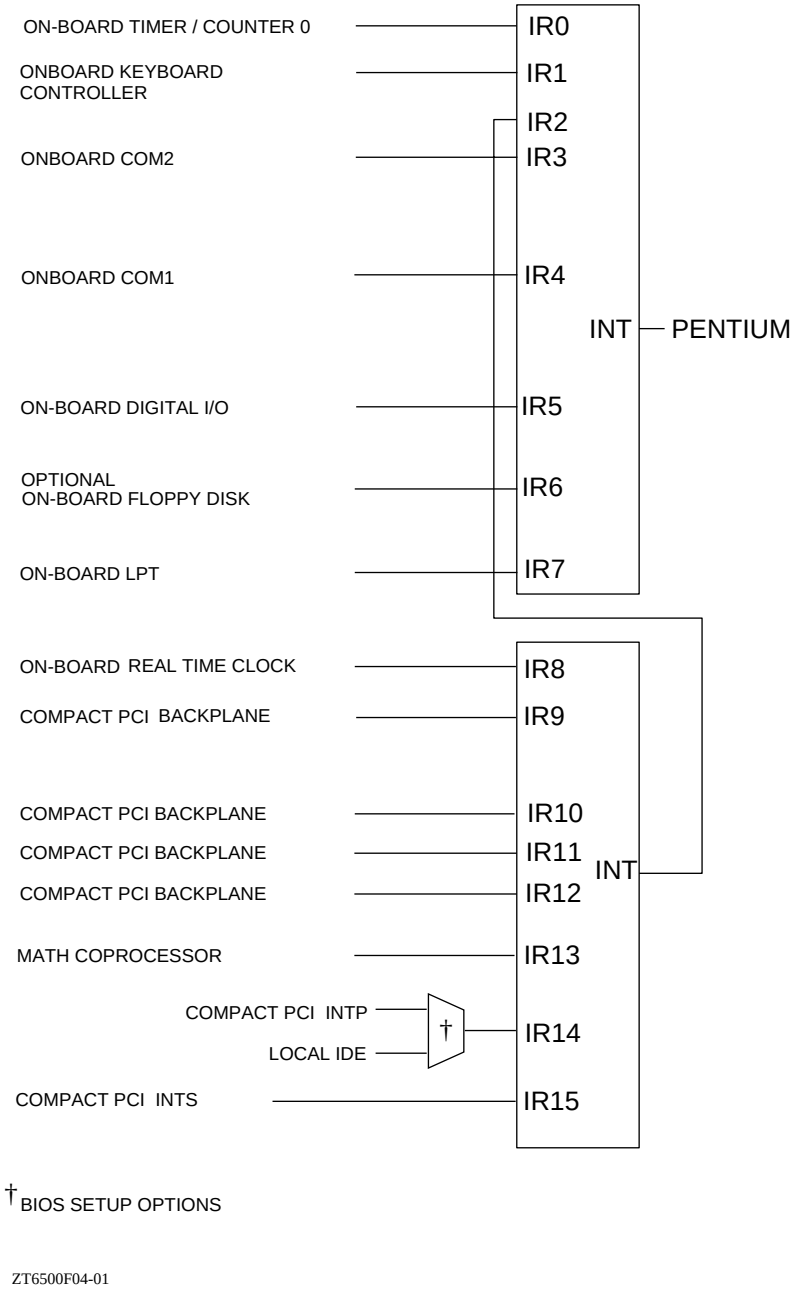
On-Board Interrupts

On-board interrupt sources include the keyboard controller, serial ports (COM1, COM2), parallel printer port, real-time clock, timer/counters, Math coprocessor, IDE controller, floppy disk, and digital I/O.

Legacy IDE Interrupts

Two interrupts (**INTP-**, **INTS-**) have been defined by the CompactPCI specification for supporting legacy IDE devices. These have been mapped to IRQ14 (primary) and

IRQ15 (secondary). The BIOS setup page allows IRQ14 to be switched between "on-board" and "PCI" IDE sources. This should be set to PCI unless the board has been modified for on-board IDE (a special factory option).



Interrupt Architecture

PROGRAMMABLE REGISTERS

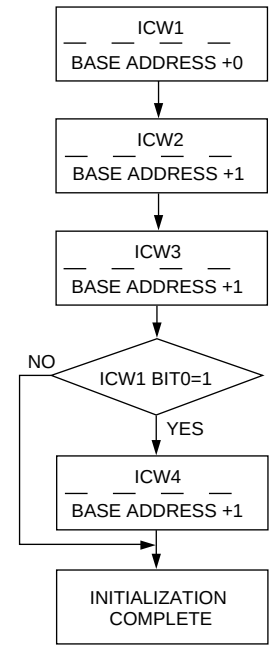
Each interrupt controller includes four initialization registers, three control registers, and three status registers. The I/O port addressing for the interrupt controllers is given in the following table. The base address of the master interrupt controller is 20h and the base address of the slave interrupt controller is A0h.

Interrupt Controller Register Addressing

Address	Register	Operation
Base+0h	IRR, ISR, IPR	Read
Base+0h	ICW1	Write
Base+0h	OCW2, OCW3	Write
Base+1h	OCW1	Read/Write
Base+1h	ICW2, ICW3, ICW4	Write

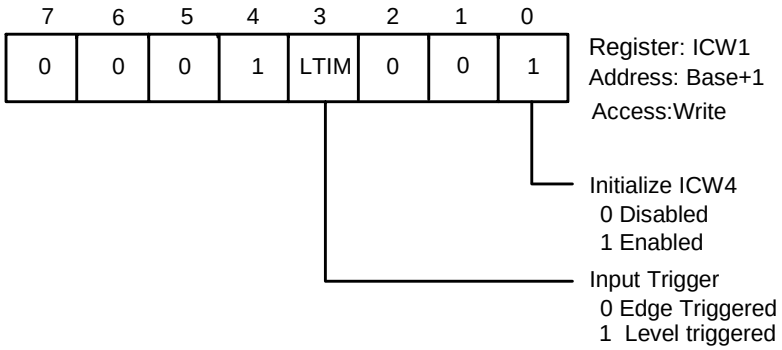
Initialization Registers (ICW1-ICW4)

Each interrupt controller must be initialized before it is used. Initialization consists of writing two, three, or four initialization commands. The programming sequence for these registers is given in the "Interrupt Initialization Programming" figure below. ICW1, ICW2, and ICW3 must be programmed during each initialization sequence. ICW4 may or may not be programmed, as required by the application.



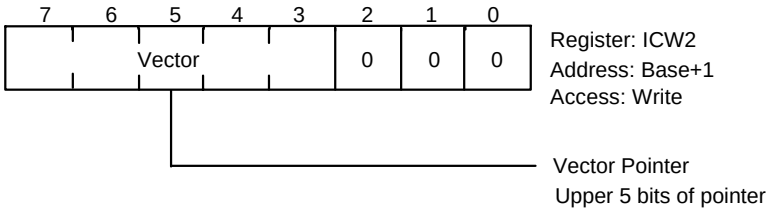
Interrupt Initialization Programming

Initialization Register ICW1



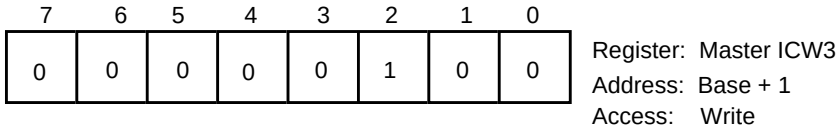
Initialization Register ICW1

Initialization Register ICW2

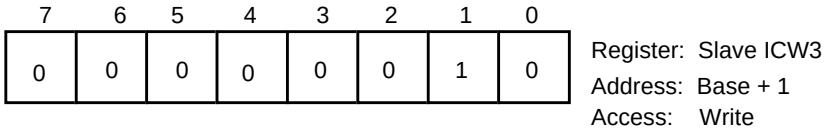


Initialization Register ICW2

Initialization Register ICW3

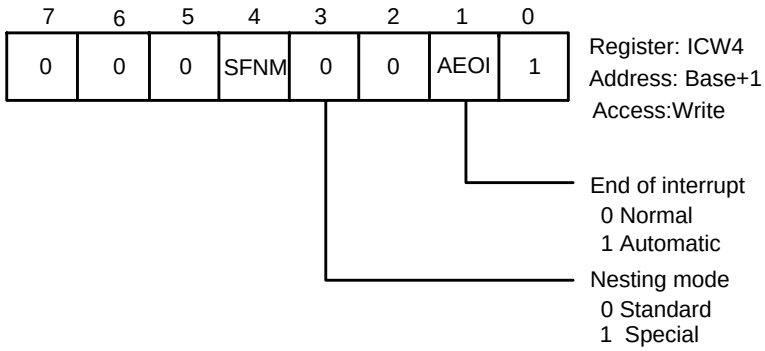


Master Initialization Register ICW3



Slave Initialization Register ICW3

Initialization Register ICW4

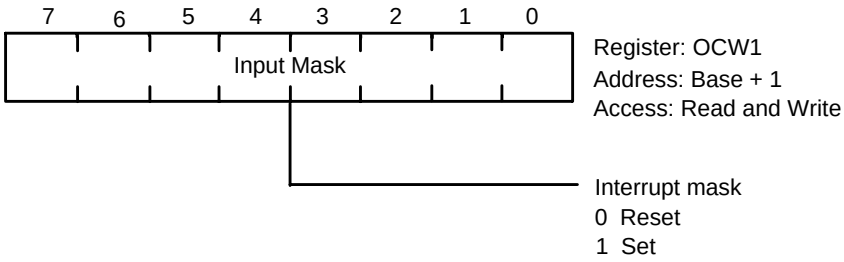


Initialization Register ICW4

Operational Registers (OCW1-OCW3)

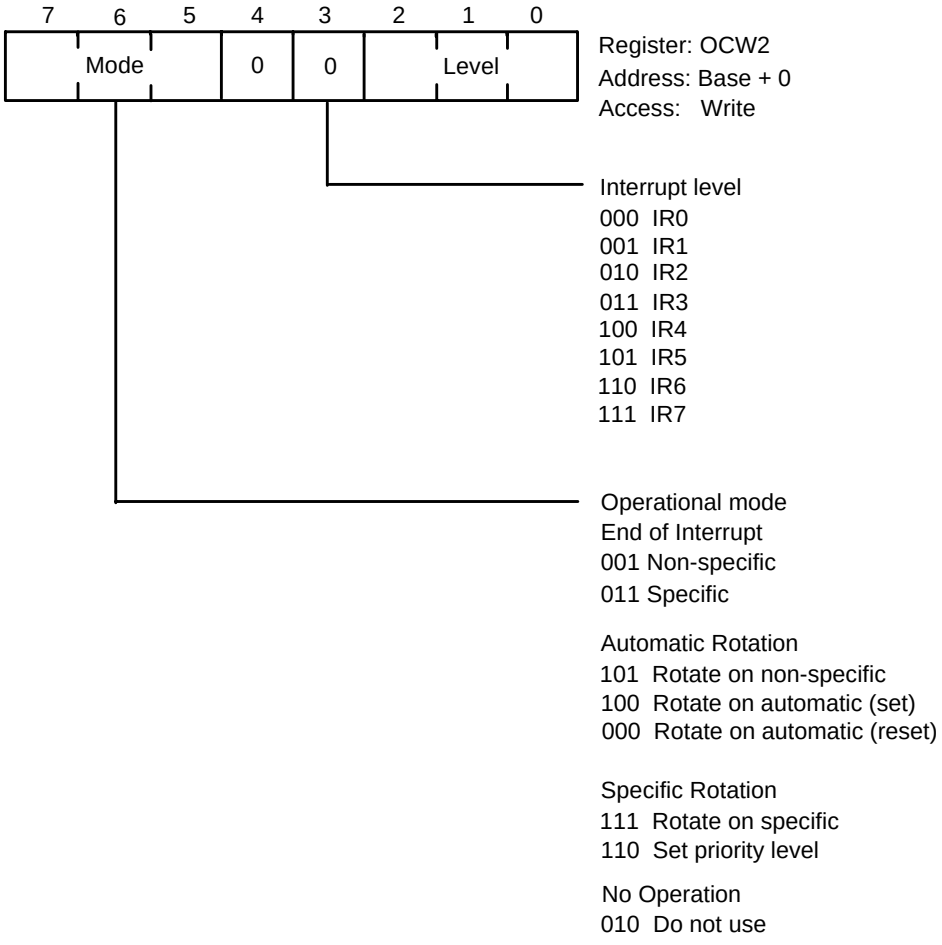
The operation of each interrupt controller is managed by three 8-bit operational registers. These registers are programmed in any sequence for things such as enabling and disabling interrupt requests and changing interrupt priorities. Illustrations of the three operational registers appear in the following topics.

Operational Register OCW1



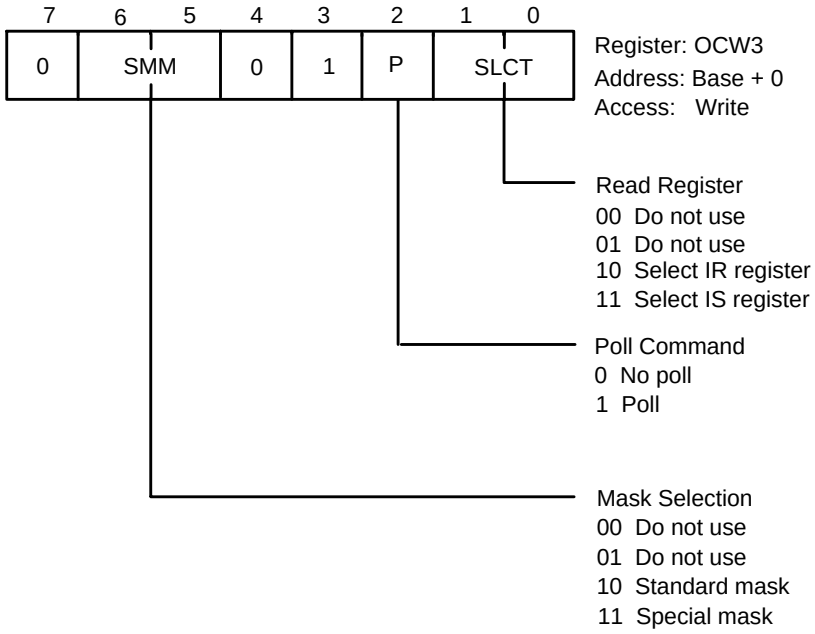
Operational Register OCW1

Operational Register OCW2



Operational Register OCW2

Operational Register OCW3

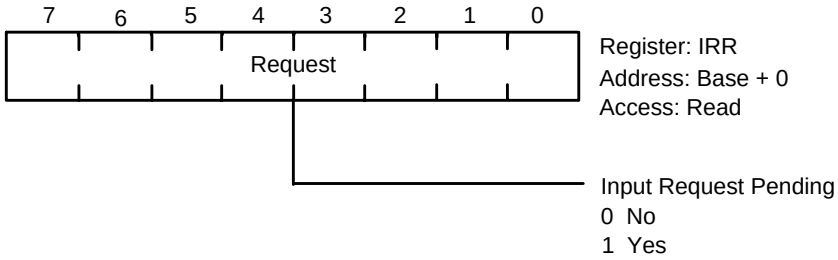


Operational Register OCW3

Status Registers (IRR, ISR, IPR)

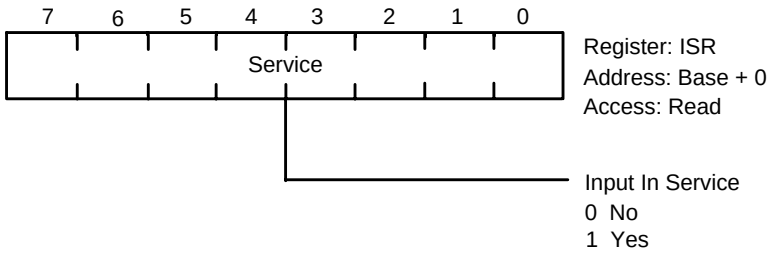
Each interrupt controller includes three status registers. A status register is selected by programming the first three bits of OCW3.

Status Register IRR



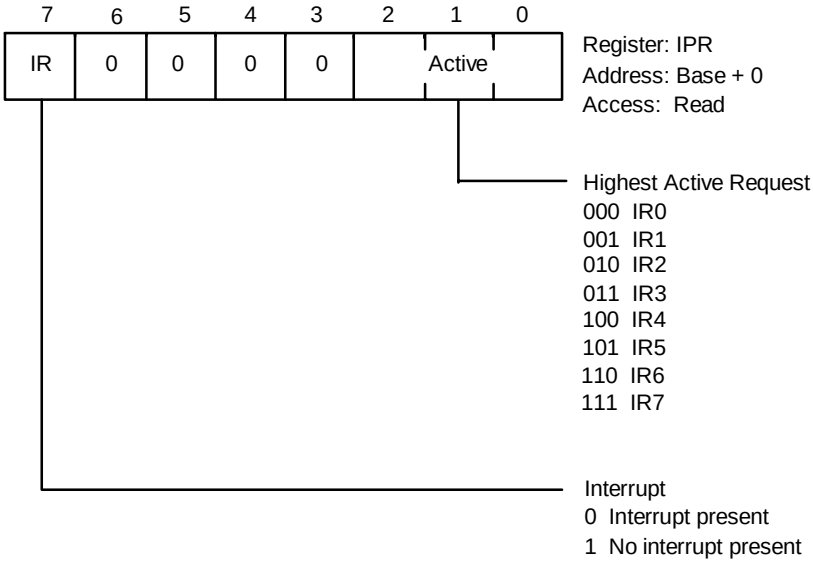
Status Register IRR

Status Register ISR



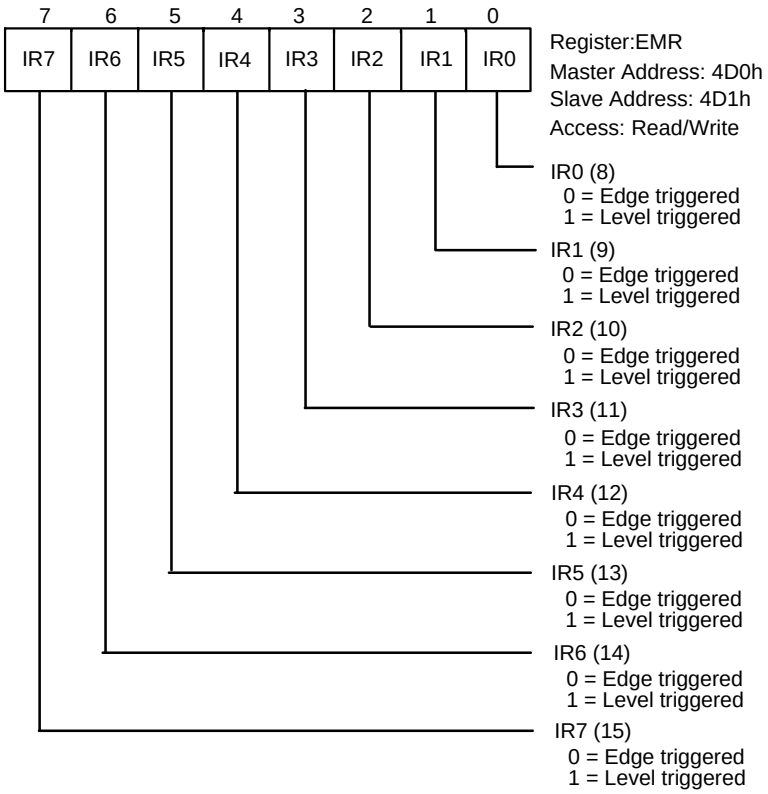
Status Register ISR

Status Register IPR



Status Register IPR

Extended Mode Register



Extended Mode Register

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the interrupt inputs. Refer to the Intel 'Peripherals' data book for more information on the 8259 interrupt controller operating modes.

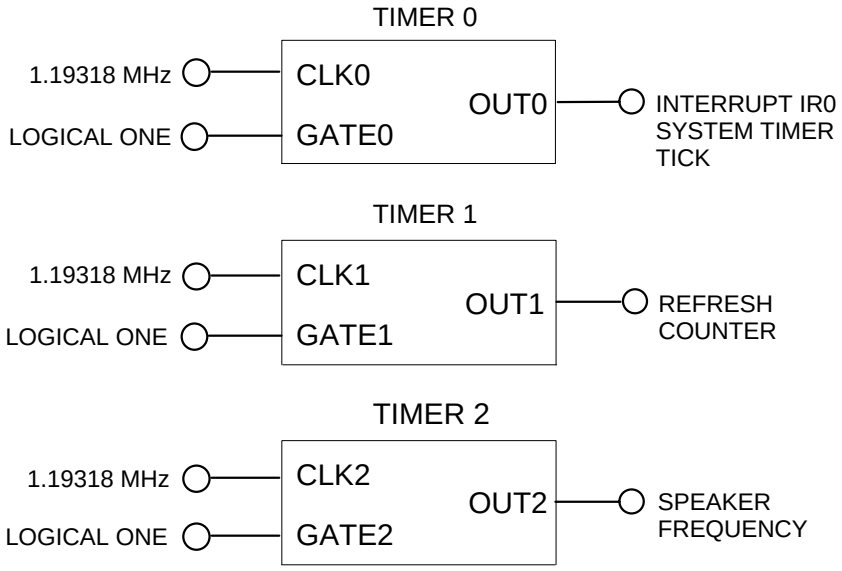
CHAPTER 5. COUNTER/TIMERS

The ZT 6500 includes one Intel-compatible 8254 device with a total of three programmable counter/timers. The counter/timers are useful for software timing loops, timed interrupts, and periodic interrupts. The major features of the counter/timers are listed below.

- Three 16-bit counter/timers
- Six programmable operating modes
- Binary and BCD counting
- Interrupt and polled operation

The counter/timer architecture is illustrated in the "Counter/Timer Architecture" figure below. In some cases, not all counter/timers are available for application development. In an MS DOS system, for example, counter/timer 0 generates a periodic system interrupt and should not be programmed by the application. Please refer to the selected operating system manual for more information.

The six programmable operating modes are summarized in the "Counter/Timer Operating Modes" table on the following page.



Counter/Timer Architecture

Counter/Timer Operating Modes

Mode	Counter/Timer Output Operation
0	Transitions after programmed count expires. Gate tied high to enable counting
1	Transitions after programmed count expires. Gate tied high to enable counting
2	Periodic single pulse after programmed count expires. Gate tied high to enable counting
3	Square wave with frequency equal to programmed count. Gate tied high to enable counting
4	Single pulse after programmed count expires. Gate tied high to enable counting
5	Single pulse after programmed count expires. Gate tied high to enable counting

PROGRAMMABLE REGISTERS

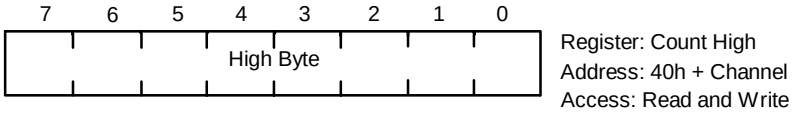
The counter/timers are accessed through four I/O addresses as shown in the following table. Each counter/timer occupies an I/O port address through which the preset count values are written and both the count and status information is read. The Control register occupies the remaining I/O port address, which services all three counter/timers.

Counter/Timer Register Addressing

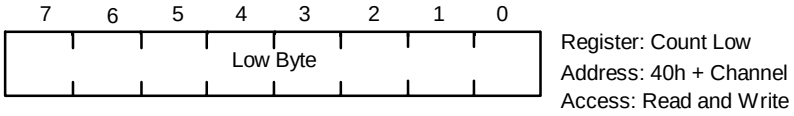
Address	Register	Operation
0040h	Channel 0 Count	Read/Write
0040h	Channel 0 Status	Read
0041h	Channel 1 Count	Read/Write
0041h	Channel 1 Status	Read
0042h	Channel 2 Count	Read/Write
0042h	Channel 2 Status	Read
0043h	Control	Write

Count Registers and Count Latch

Each counter/timer has a 16-bit Count Register and 16-bit Count Latch Register. The Count Register is programmed with the initial count and is updated according to the mode in which the counter/timer is programmed. The Count Latch Register is used to read the current count. The Access bits in the General Control Register define the method for accessing the 16-bit Count and Count Latch Registers (low byte, high byte, low byte followed by high byte).



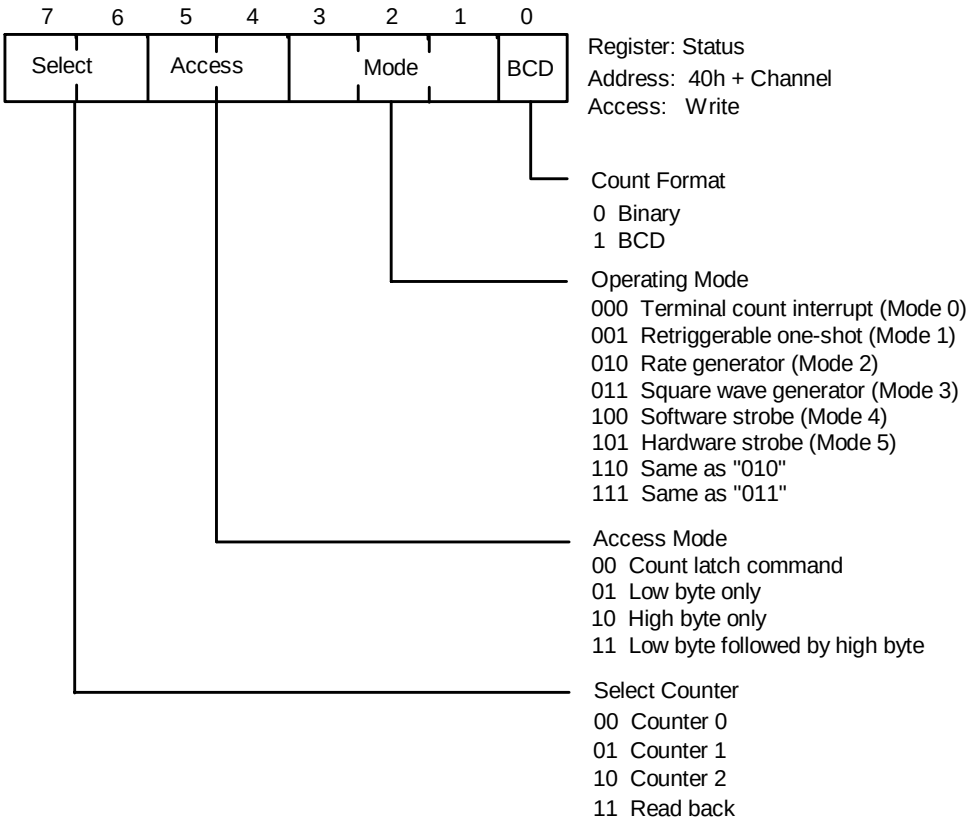
Count Register High Byte



Count Register Low Byte

Status Register

Each counter/timer has a Status Register. The Status Register must be read using the multiple latch command specified in the Multiple Latch Control Register (shown later in this chapter).

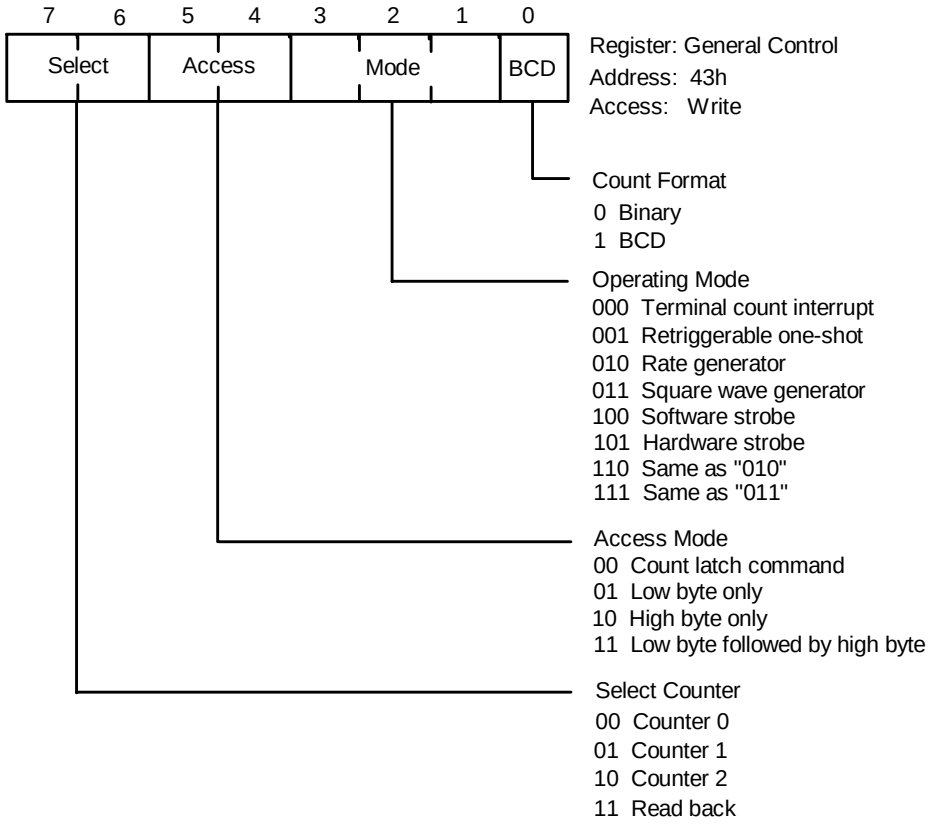


Counter/Timer Status Register

Control Register

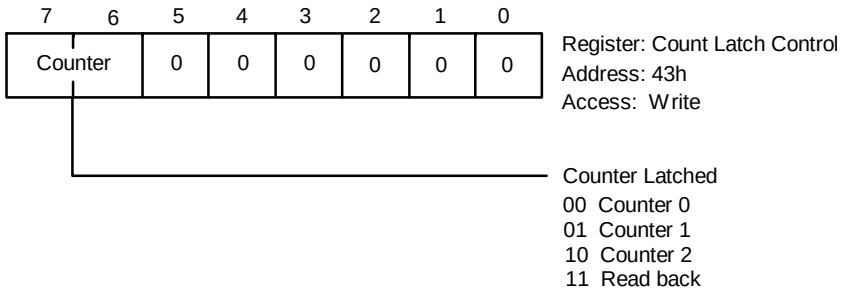
The Control register is used to initialize the counter/timers and to select the method of reading the count and status information. The Control register is best described by dividing it into three formats as illustrated in the following figures.

General Control Register



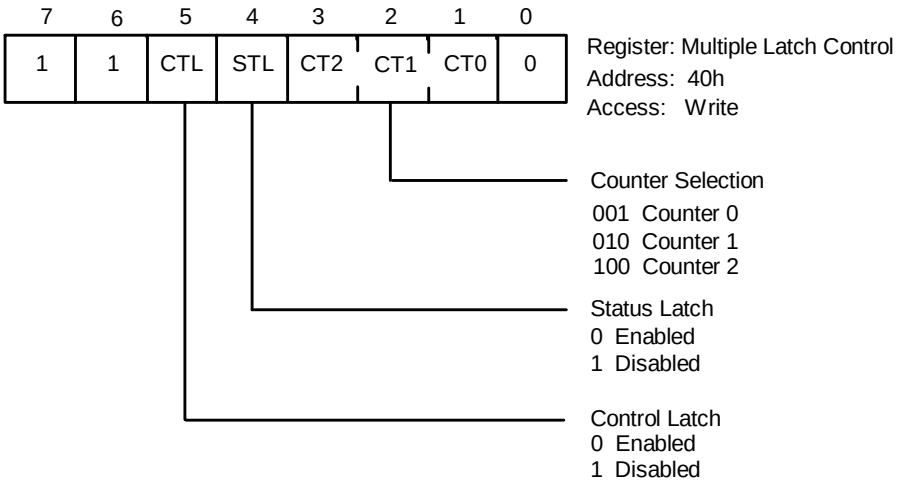
General Control Register

Count Latch Control Register



Count Latch Control Register

Multiple Latch Control Register



Multiple Latch Control Register

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the counter/timers. Refer to the Intel 'Peripherals' data book for more information on the 8254 counter/timer operating modes.

CHAPTER 6. DMA CONTROLLER

This chapter provides an overview of ZT 6500 DMA architecture and DMA controller operation. Descriptions of DMA controller programmable registers are also included.

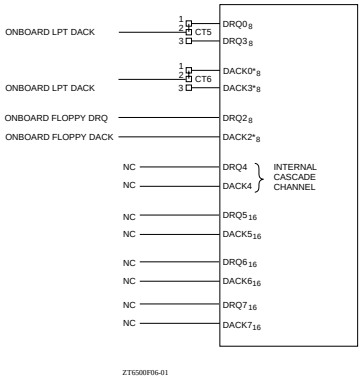
ZT 6500 SPECIFICS

The ZT 6500 includes two cascaded, Intel-compatible, 8237 Direct Memory Access controllers that provide a programmable interface for direct transfers between peripherals and main memory. The DMA controllers used on the ZT 6500 are supersets of the 8237 device, supporting 32-bit memory accesses, higher speed transfers, and the PCI protocol. Features of the DMA controllers include:

- 8237 Compatible/superset
- Seven DMA Channel support
- 32-bit memory addressing
- Compatible, TYPE A, TYPE B, TYPE F transfer rates
- Fixed or rotating priorities
- PCI Bus mastering

The DMA architecture is illustrated in the "DMA Architecture" figure below.

The on-board IEEE 1234 Parallel Port can be configured to use DMA channel 0 or 3 (cuttable trace option) for data transfers. The Parallel Port must be configured for ECP mode to use DMA. The optional floppy drive is configured to use DMA channel 2.



DMA Architecture

PROGRAMMABLE REGISTERS

Each DMA controller is managed through the 16 I/O port addresses shown in the "Slave DMA I/O Port Addressing" table below. Page registers extend the 16-bit DMA address to the full 24-bit address space available on the ZT 6500. I/O port addressing for the DMA page registers is given in the "DMA Page I/O Port Addressing" and "DMA Extended Page (A24-31) I/O Port Addressing" tables on the following page.

The topics that follow illustrate the DMA controller programmable registers.

Slave DMA I/O Port Addressing

Address			
Slave	**Master**	**Register**	**Operation**
0	C0	Channel 0 Base/Current Address	Write
		Channel 0 Current Address	Read
1	C2	Channel 0 Base/Current Count	Write
		Channel 0 Current Count	Read
2	C4	Channel 1 Base/Current Address	Write
		Channel 1 Current Address	Read
3	C6	Channel 1 Base/Current Count	Write
		Channel 1 Current Count	Read
4	C8	Channel 2 Base/Current Address	Write
		Channel 2 Current Address	Read
5	CA	Channel 2 Base/Current Count	Write
		Channel 2 Current Count	Read
6	CC	Channel 3 Base/Current Address	Write
		Channel 3 Current Address	Read
7	CE	Channel 3 Base/Current Count	Write
		Channel 3 Current Count	Read
8	D0	Status	Read
		Command	Write
9	D2	Write Request	Write
A	D4	Write Single Mask	Write
B	D6	Write Mode	Write
C	D8	Clear Byte Pointer	Write
D	DA	Clear Master	Write
E	DC	Clear Mask	Write
F	DE	Write Mask	Write

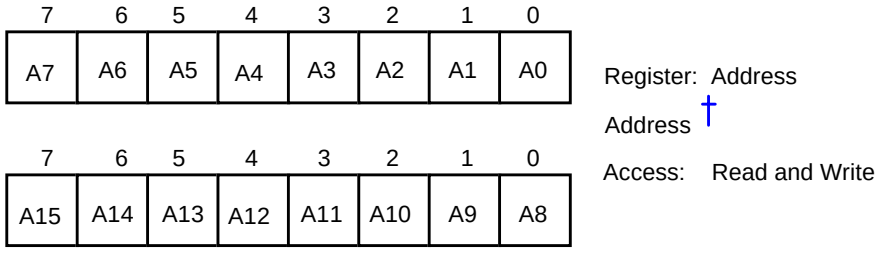
DMA Page I/O Port Addressing

Address	Register	Operation
87h	Channel 0 A16-23 Address	Read/Write
83h	Channel 1 A16-23 Address	Read/Write
81h	Channel 2 A16-23 Address	Read/Write
82h	Channel 3 A16-23 Address	Read/Write
8Bh	Channel 5 A16-23 Address	Read/Write
89h	Channel 6 A16-23 Address	Read/Write
8Ah	Channel 7 A16-23 Address	Read/Write

DMA Extended Page (A24-31) I/O Port Addressing

Address	Register	Operation
487h	Channel 0 A24-31 Address	Read/Write
483h	Channel 1 A24-31 Address	Read/Write
481h	Channel 2 A24-31 Address	Read/Write
481h	Channel 3 A24-31 Address	Read/Write
48Bh	Channel 5 A24-31 Address	Read/Write
489h	Channel 6 A24-31 Address	Read/Write
48Ah	Channel 7 A24-31 Address	Read/Write

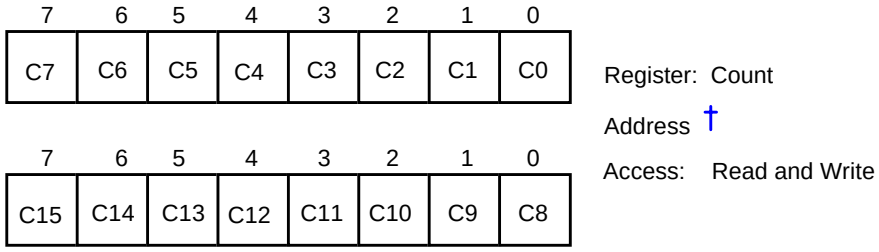
Address Register



Address Register

† See the "Slave DMA I/O Port Addressing" table

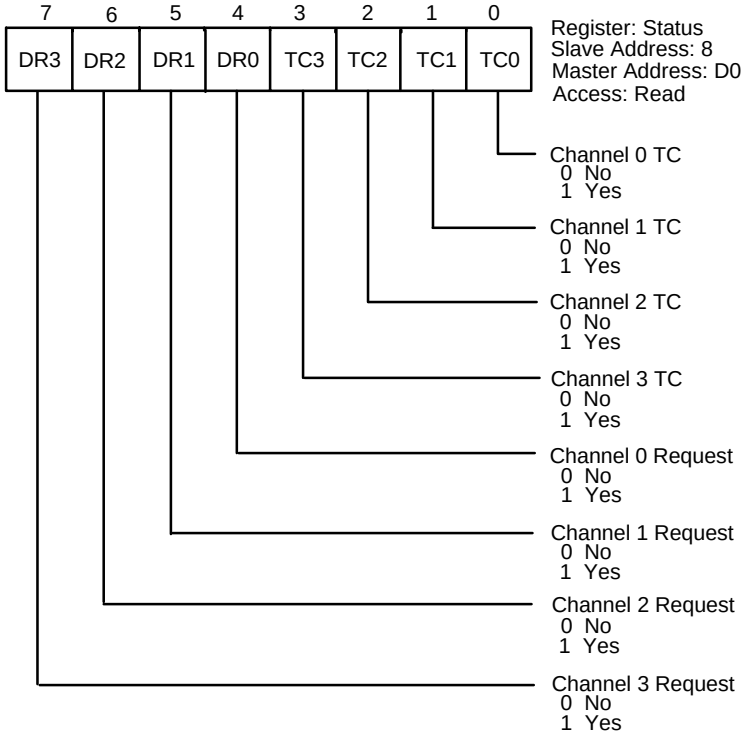
Count Register



Count Register

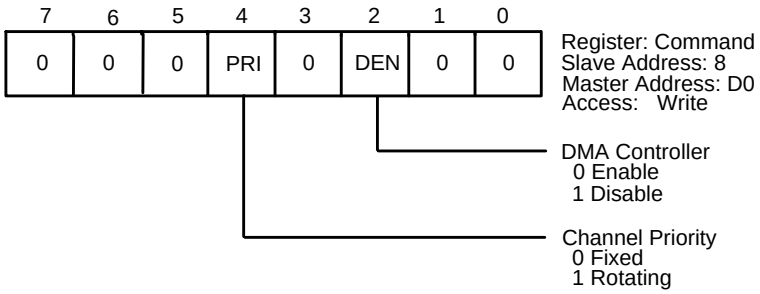
† See the "Slave DMA I/O Port Addressing" table

Status Register



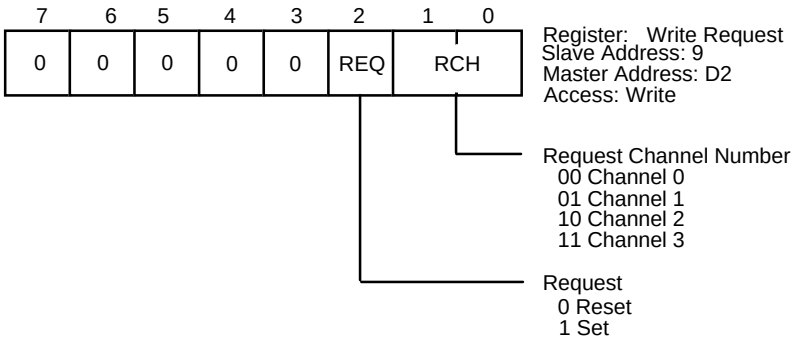
DMA Controller Status Register

Command Register



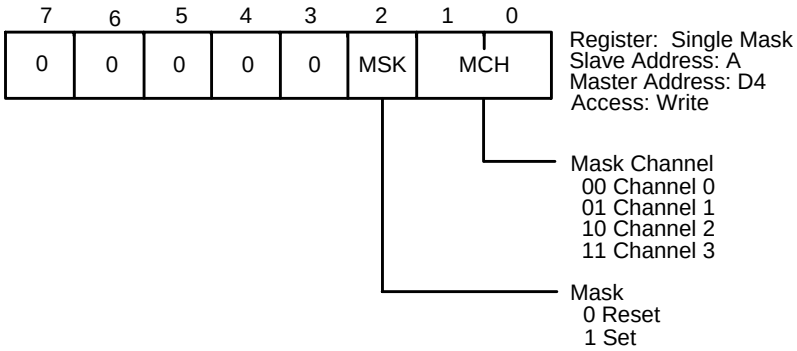
Command Register

Write Request Register



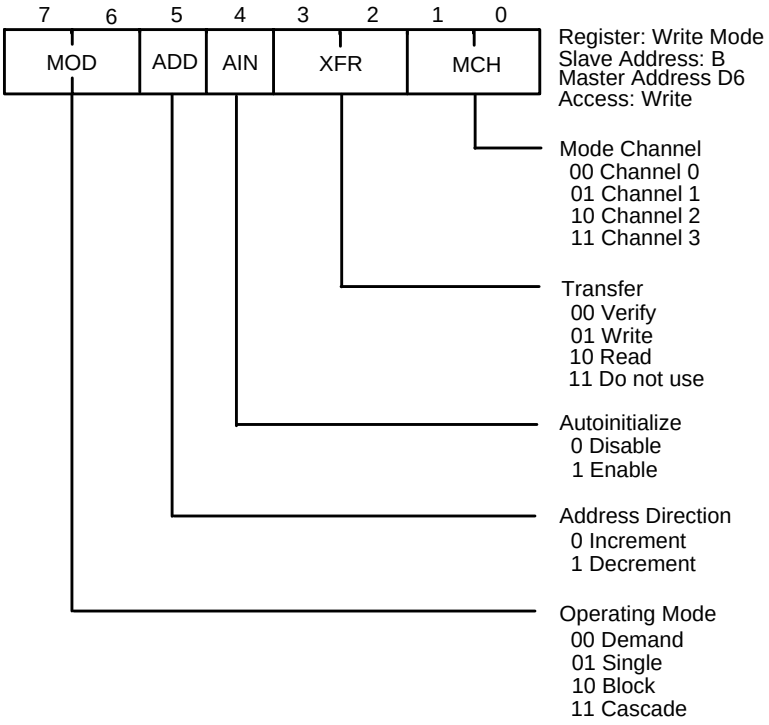
Write Request Register

Write Single Mask Register



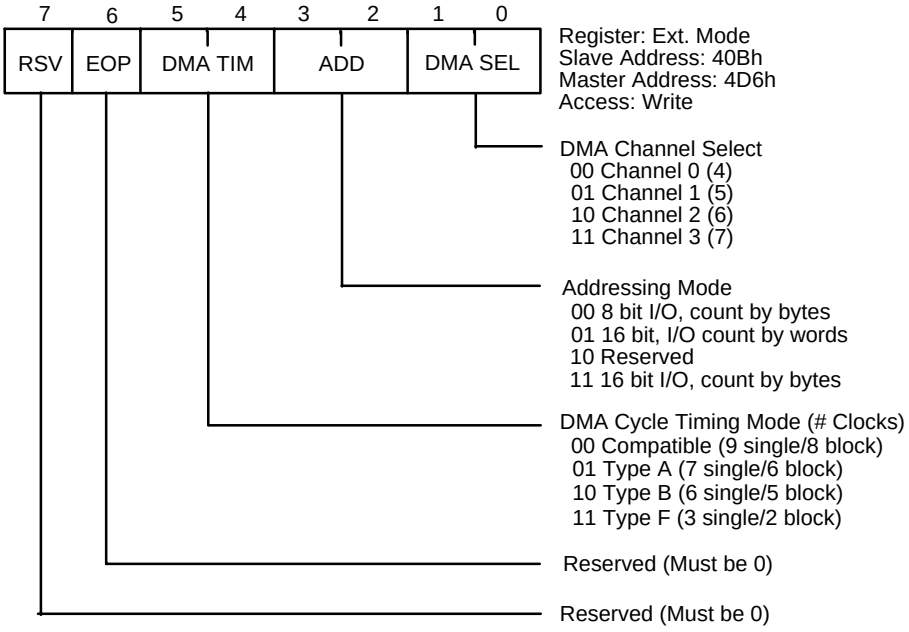
Write Single Mask Register

Write Mode Register



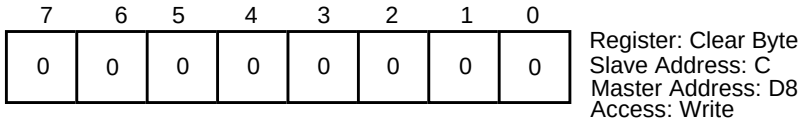
Write Mode Register

DMA Extended Mode Register



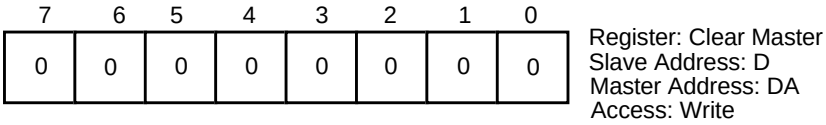
DMA Extended Mode Register

Clear Byte Register



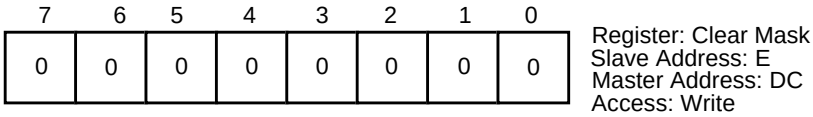
Clear Byte Register

Clear Master Register



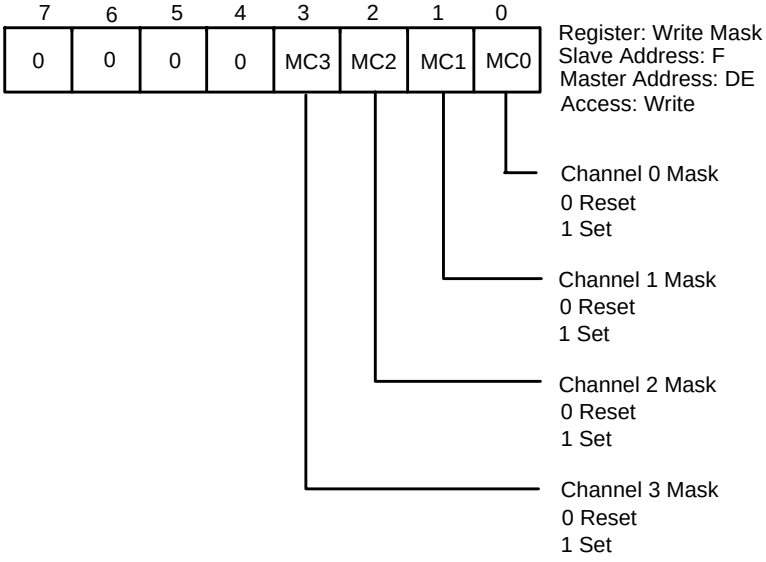
Clear Master Register

Clear Mask Register



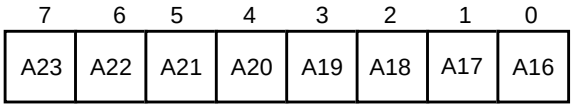
Clear Mask Register

Write Mask Register



Write Mask Register

DMA Page Register

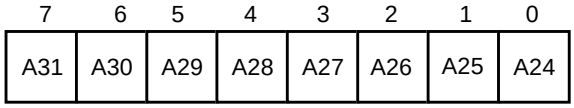


Register: DMA Page
Address †
Access: Read and Write

DMA Page Register

† See the "DMA Page I/O Port Addressingtable.

DMA Extended Page Register



Register: DMA Extended Page
Address †
Access: Read and Write

DMA Extended Page Register

† See the "DMA Extended Page (A24-31) I/O Port Addressingtable.

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the interrupt inputs. Refer to the Intel Peripherals data book for more information on the 8237 DMA controller operating modes.

CHAPTER 7. REAL-TIME CLOCK

The ZT 6500 includes one Motorola-compatible 146818 real-time clock. The real-time clock provides clock and 100-year calendar information in addition to 242 bytes of CMOS setup static RAM. These functions are battery backed for continuous operation even in the absence of system power. The RAM is used by the operating system BIOS to store configuration information. The major features of the real-time clock are listed below.

- Timekeeping to a 1 second resolution
- 50 bytes of CMOS setup RAM
- Leap year compensation
- Daylight Savings Time compensation
- Periodic, Alarm, and Update Ended interrupts
- Battery backed

PROGRAMMABLE REGISTERS

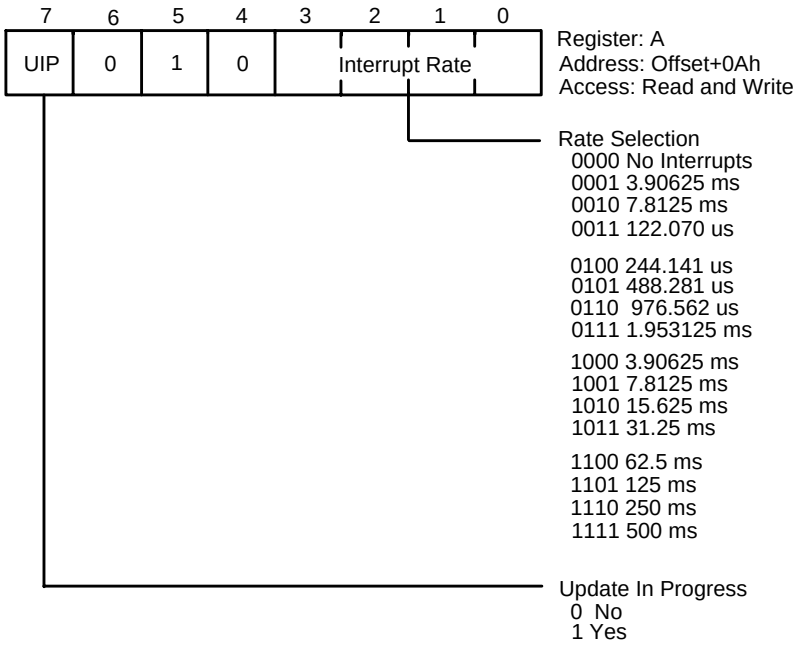
The real-time clock includes 64 register locations. These registers are accessed through I/O port locations 70h and 71h. A real-time clock register is accessed by first writing the offset address of the register to I/O port location 70h. Data is then transferred to or from the register through I/O port location 71h. This sequence must be repeated to read the same register a second time. The I/O port addressing for the real-time clock is given in the "Real-Time Clock Register Addressing" table below.

The topics that follow illustrate the programmable registers for the real-time clock.

Real-Time Clock Register Addressing

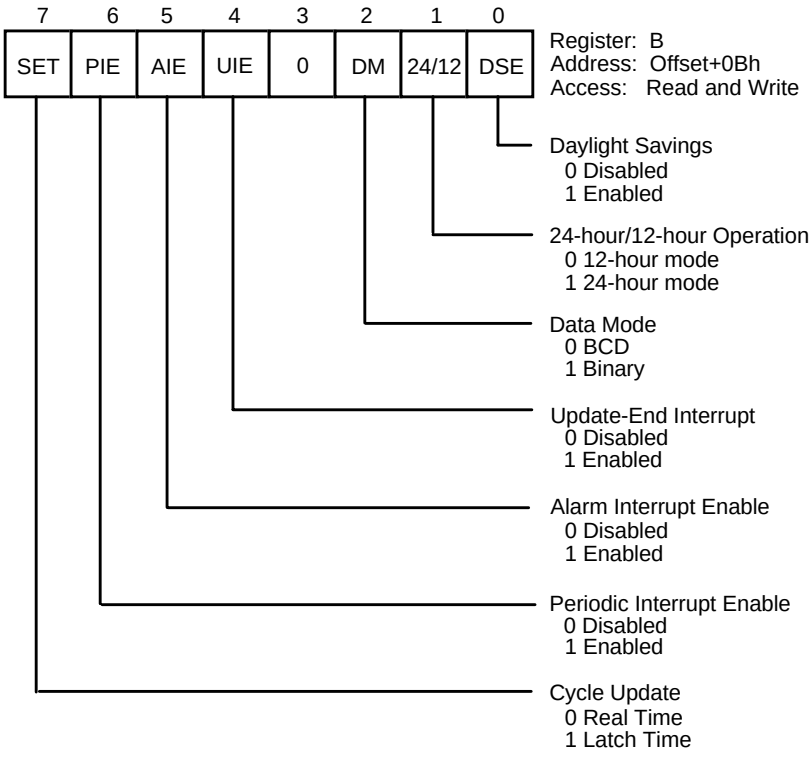
Address Offset	Function	Range
0h	Time-Seconds	0-59
1h	Alarm-Seconds	0-59
2h	Time-Minutes	0-59
3h	Alarm-Minutes	0-59
4h	Time-Hours (12 hour mode)	1-12
4h	Time-Hours (24 hour mode)	0-23
5h	Alarm-Hours	0-23
6h	Day of Week	1-7
7h	Date of Month	1-31
8h	Month	1-12
9h	Year	0-99
Ah-Dh	Register A-D	——
Eh-3Fh	General Purpose	——

Register A



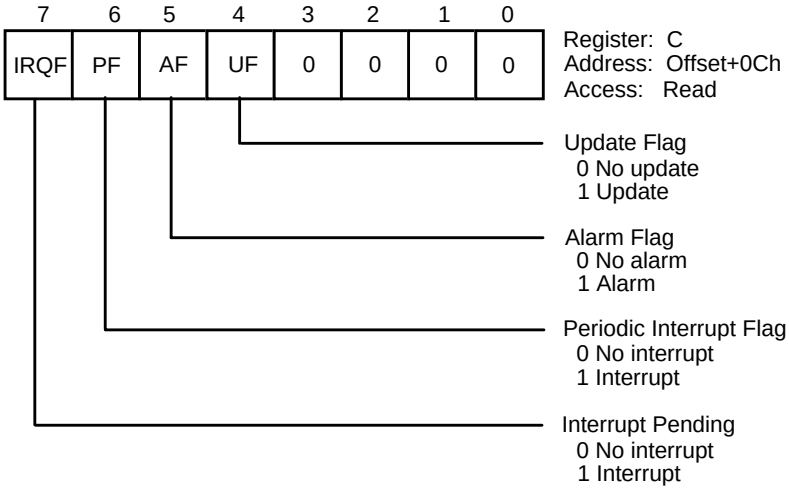
Real Time Clock Register A

Register B



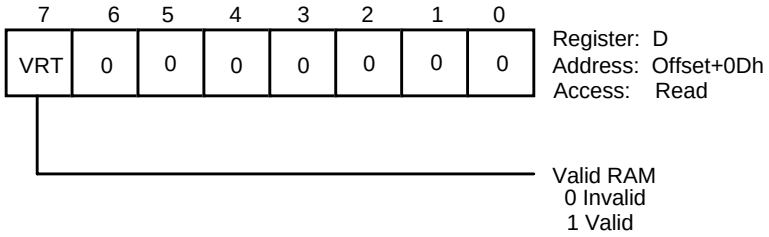
Real Time Clock Register B

Register C



Real Time Clock Register C

Register D



Real Time Clock Register D

ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87303 data book for more information on the real-time clock operating modes.

CHAPTER 8. SERIAL CONTROLLER

This chapter discusses operation of the two ZT 6500 serial ports. Each channel is compatible with the industry standard 16550 serial port, including support for a 16 byte FIFO for read and write operations.

ZT 6500 SPECIFICS

The ZT 6500 includes two serial ports that are compatible with the industry standard 16550. The interface for each serial port is implemented with 5 V charge pump technology to eliminate the need for a ±12 V supply. The serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud. Both channels are supplied as DTE configured devices through the multi-I/O connector, J1. The ZT 90206 cable assembly allows each channel to be interfaced directly to 9-pin D-Shell serial devices, as used in PC applications.

The major features of each serial port are listed below.

- Two RS-232 channels
- 16550 compatible
- Drivers do not require ±12 V
- Baud rates up to 115.2 Kbaud
- Polled and interrupt operation
- Loopback diagnostics

Details for the two serial ports on the ZT 6500 are discussed in the following topics.

Address Mapping

The address mapping for the PC standard architecture and the ZT 6500 is shown below.

Serial Channel	PC Port Address	ZT 6500 Port Address
COM1	3F8-3FF	3F8-3FF
COM2	2F8-2FF	2F8-2FF

Interrupt Selection

The interrupt mapping for the PC standard architecture and the ZT 6500 is shown below.

Serial Channel	PC Interrupt	ZT 6500 Interrupt
COM1	IR4	IR4
COM2	IR3	IR3

Handshake Signals

The PC architecture includes Transmit Data (TXD), Receive Data (RXD), Request To Send (RTS), Clear To Send (CTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Data Carrier Detect (DCD).

Serial Channel Interface

The serial ports are configured as DTE and are available through the 80-pin Multi-I/O connector (J1) The optional ZT 90206 cable converts the serial port interface to standard 9-pin D-shell connectors. The J1 connector pin assignments are given in the "J1 Multi-I/O Connector Pinout" table in Appendix B.

PROGRAMMABLE REGISTERS

There are six registers for initializing and controlling each serial channel. The "Serial Controller Register Addressing" table below shows the I/O port addressing for the COM port registers. The topics that follow illustrate the 16-bit divisor latch, baud rate divisors, and the six programmable registers for each serial channel.

Serial Controller Register Addressing

COM 1 Address	COM 2 Address	Register	Operation
03F8h (DIV=0)	02F8h (DIV=0)	Receive Buffer	Read
03F8h (DIV=0)	02F8h (DIV=0)	Transmit Buffer	Write
03F8h (DIV=1)	02F8h (DIV=1)	Divisor Latch LSB	Read/Write
03F9h (DIV=0)	02F9h (DIV=0)	Interrupt Control	Read/Write
03F9h (DIV=1)	02F9h (DIV=1)	Divisor Latch MSB	Read/Write
03FAh	02FAh	Interrupt Status	Read
03FBh	02FBh	Line Control	Read/Write
03FCh	02FCh	Modem Control	Read/Write
03FDh	02FDh	Line Status	Read
03FEh	02FEh	Modem Status	Read
03FFh	02FFh	Reserved	

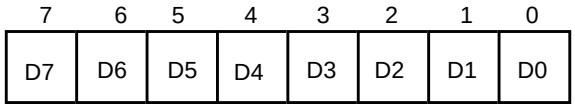
Baud Rate Divisors

The "Divisor Latch LSB" and "Divisor Latch MSB" figures that follow illustrate the 16-bit divisor latch. The "Baud Rate Divisors" table below lists the divisors for popular baud rates. It also includes the percent error based on the difference between the exact divisor for a specified baud rate and the divisor obtainable with a 16-bit integer format. To guarantee proper operation, the percentage error should never be greater than four.

Baud Rate Divisors Table

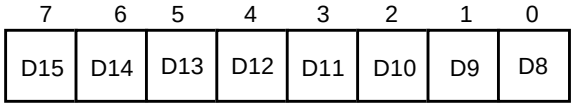
Baud Rate	Divisor (dec/hex)	Percent Error
50	2304/1440h	0
75	1536/960h	0
150	768/480h	0
300	384/240h	0
600	192/120h	0
1200	96/60h	0
1800	64/40h	0
2000	58/3Ah	0.69
2400	48/30h	0
3600	32/20h	0
4800	24/18h	0
7200	16/10h	0
9600	12/Ch	0
19200	6/6h	0
38400	3/3h	0
56000	2/2h	2.86
57600	2/2h	0
115200	1/1h	0

Divisor Latch LSB and MSB



Register: Divisor Latch LSB
Address: 2F8/3F8h DIV=1
Access: Read and Write

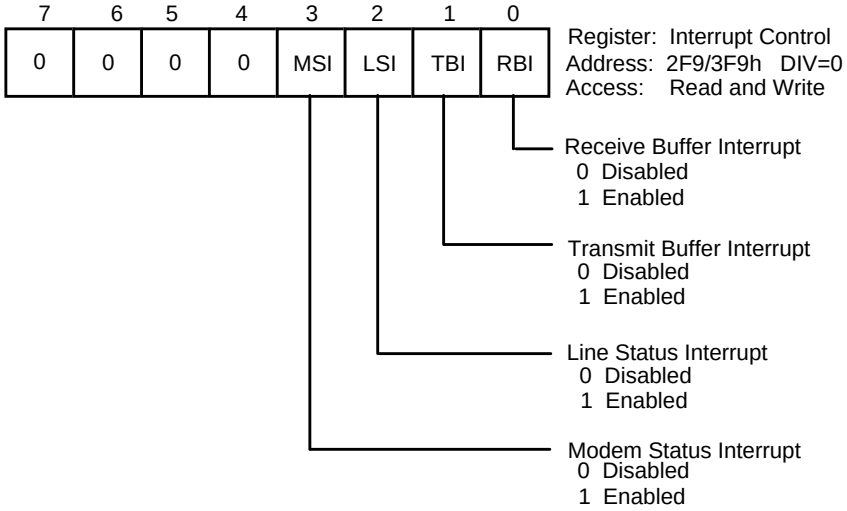
Divisor Latch LSB



Register: Divisor Latch MSB
Address: 2F9/3F9h DIV=1
Access: Read and Write

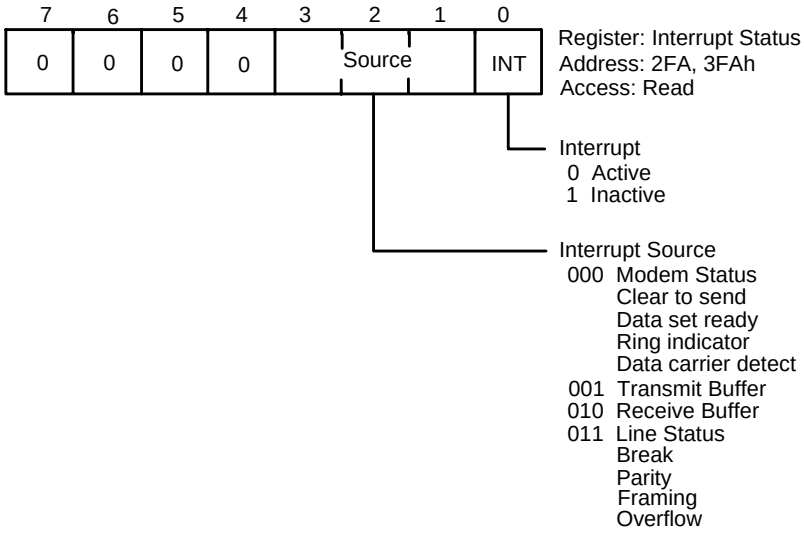
Divisor Latch MSB

Interrupt Control Register



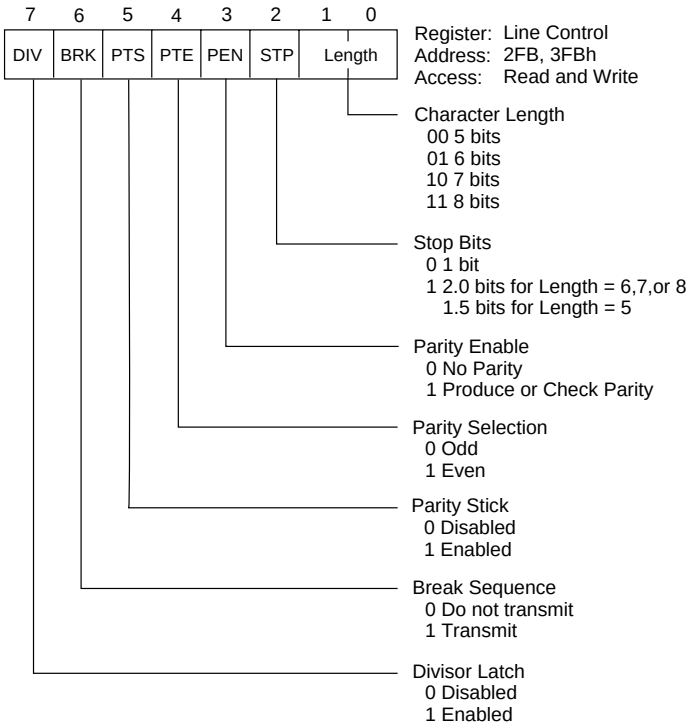
Interrupt Control Register

Interrupt Status Register



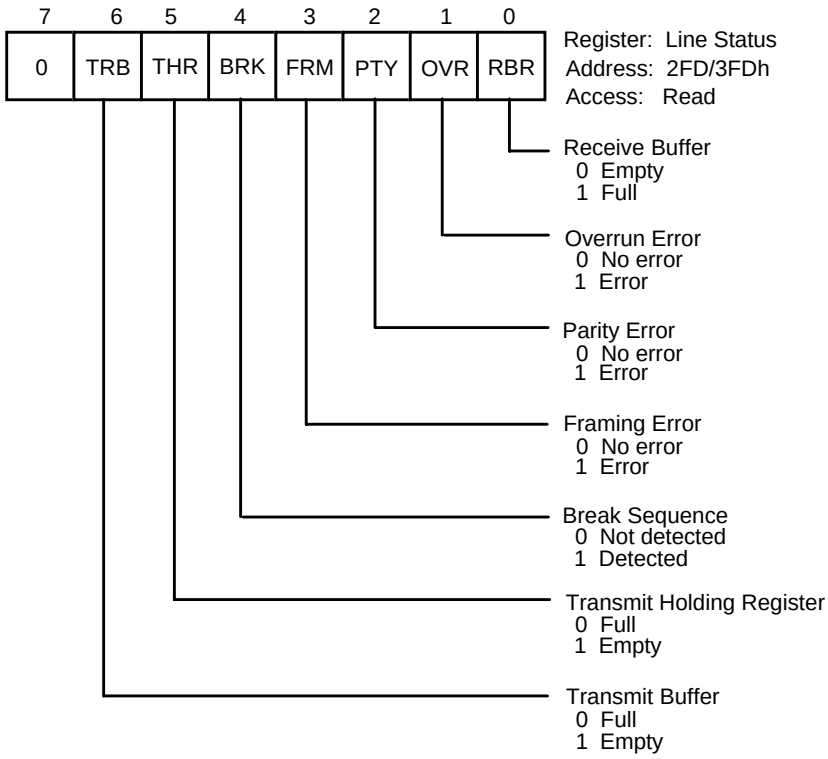
Interrupt Status Register

Line Control Register



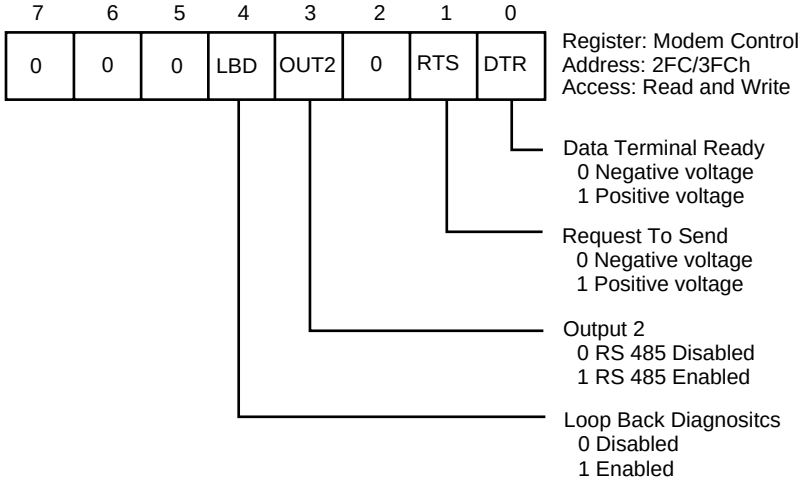
Line Control Register

Line Status Register



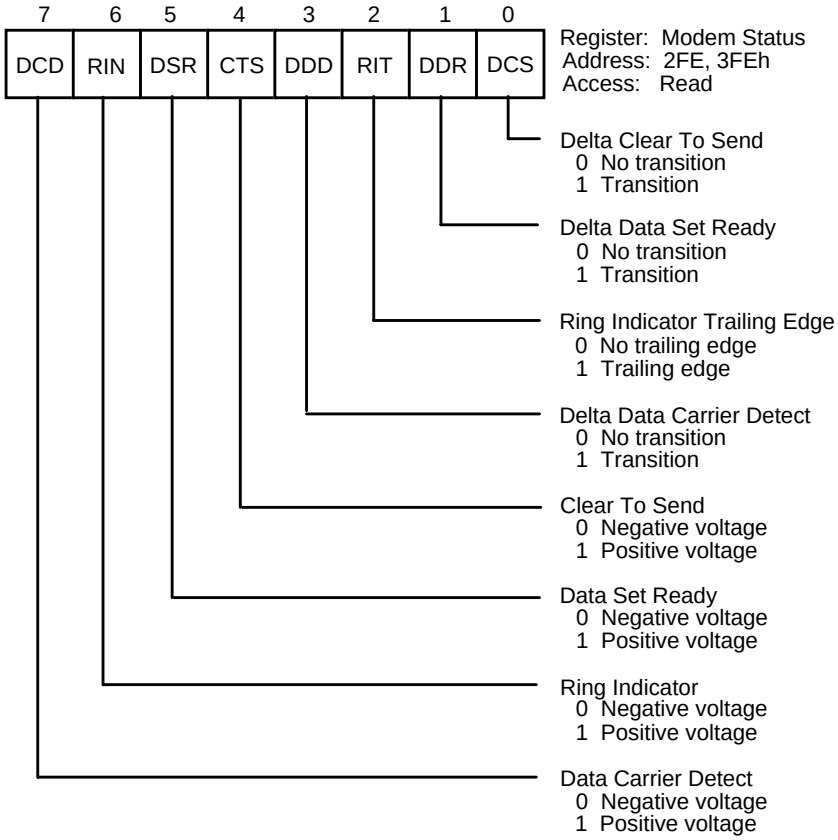
Line Status Register

Modem Control Register



Modem Control Register

Modem Status Register



Modem Status Register

ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87C303 data book for more information on the serial controller operating modes.

CHAPTER 9. IEEE-1284 PARALLEL PORT INTERFACE

The ZT 6500 supports an IEEE-1284 compatible printer port interface, available through the Multi-I/O connector (J1).

The printer port can be configured in compatibility, extended, EPP, or ECP modes through the BIOS SETUP Utility Screen (discussed in the section "ZT 6500 Setup" in Chapter 2).

The ZT 90206 cable assembly allows the on-board LPT1 channel to interface directly to 25-pin D-Shell parallel port devices, as used in PC applications.

PARALLEL PORT CONFIGURATION OPTIONS

The different modes for the printer port are described below. Details for the parallel port on the ZT 6500 are discussed in the following topics.

Parallel Port Mode	Description	Max. Data Rate
Compatibility (Default)	Unidirectional data configuration. The original PC-AT Mode. Also known as "nibble mode" because the four status bits in the cable are used for feedback from devices such as tape back-up units (when restoring data from a tape). Software based protocol.	50-150 kbps
Extended	Bi-directional data transfer capability. Similar to Compatibility mode, but allows 8-bit data in both directions. Faster for interfaces needing to supply data to the computer (e.g., scanners, tape back-up). Software based protocol.	50-150 kbps
EPP	Enhanced Parallel Port. Hardware based handshaking of the data transfers provide single I/O instruction data transfers in read and write operations. Register superset of compatibility/extended modes.	500 Kbps-2 Mbps
ECP	IEEE-1284 Extended Capability Port. Similar to EPP, but register set is strictly defined. Adds FIFOs for read/write operations. ECP devices require IEEE-1284 compliant cabling and buffers. The ZT 6500 supplies compliant buffers - cabling is available from other sources.	500 Kbps-2 Mbps

ADDRESS MAPPING

The address mapping for the PC standard architecture and the ZT 6500 is shown below.

Parallel Port	PC Port Address	ZT 6500 Port Address
LPT1	3BC (typically)	378-37F—Compatibility, Extended, EPP Modes 378-37A, 778-77A—ECP Mode

INTERRUPT SELECTION

The interrupt mapping for the PC standard architecture and the ZT 6500 is shown below.

Parallel Port	PC Interrupt	ZT 6500 Interrupt
LPT1	IR5 or IR7	IR7

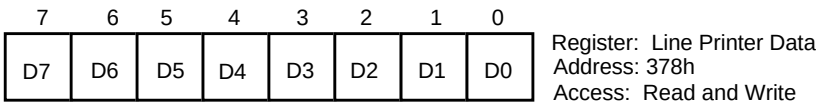
DMA SELECTION

DMA may be configured for ECP mode in software. DMA channel 0 is dedicated for ECP support and may be used by application software. The BIOS does not use DMA for any data transfers. Applications needing DMA support must configure the parallel port with appropriate initialization code.

PROGRAMMABLE REGISTERS

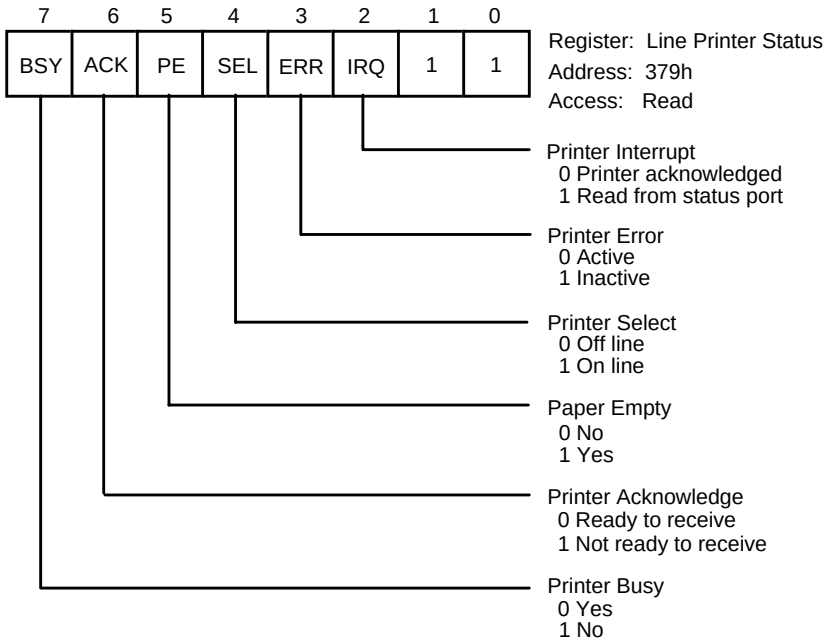
The following topics illustrate the programmable registers for the compatibility/extended mode parallel port interface. For EPP and ECP information, consult the National Semiconductor PC87303 data sheet (National LIT# 112904-001)

Line Printer Data Register



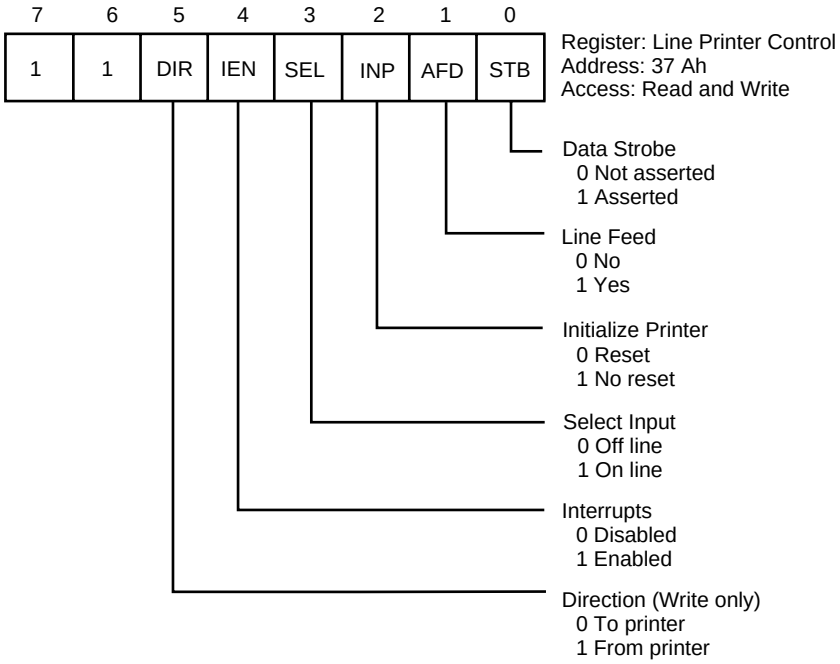
Line Printer Data Register

Line Printer Status Register



Line Printer Status Register

Line Printer Control Register



Line Printer Control Register

ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87303 data book (National LIT# 112904-001) for more information on the parallel controller operating modes. An excellent tutorial of IEEE-1284 can be obtained from FarPoint Communications (805) 726-4420. The IEEE-1284 specification can be obtained from the IEEE Standards Office at (800) 678-4333, ask for document number DS02709.

CHAPTER 10. OPTIONAL FLOPPY DISK INTERFACE

The ZT 6500 can be ordered with an optional floppy disk drive (option -F1). Included with the drive is a special three slot frontplate that includes an opening for the floppy drive (to the left of the CPU - solder side) along with a mounting plate for attaching the floppy to the ZT 6500. In addition, connector J4 on the solder side of the board is loaded for access to the floppy signals.

This chapter provides an overview of the optional Floppy Disk Controller. It includes a product definition, a list of product features, as well as register drawings and descriptions.

FEATURES OF THE OPTIONAL FLOPPY DISK INTERFACE

- 360K, 720K, 1.2 Mbyte, and 1.44 Mbyte floppy disk drive support
- IBM-PC®/AT®/MCA®/EISA® compatible register set
- 3½" floppy disk drive support
- Integrated 3½" slimline floppy disk drive (1 slot usage)

INTERRUPTS

The Floppy Disk Controller (FDC) communicates status to the host processor via interrupt IRQ6.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller supports all DOS-compatible floppy disk drives through a 1-millimeter 26-pin connector. Data rates of 250 Kbytes, 300 Kbytes, 500 Kbytes, and 1 Mbps are supported through program control. An on-board 16-byte FIFO provides increased bus-latency tolerance. The FDC is fully compatible with the IBM-AT, IBM-PS/2®, and EISA architectures.

POWER REQUIREMENTS

Power required by the optional floppy depends upon the type of drive loaded on the controller. Consult Appendix B, "Specifications," for details. Only +5 V is required for the floppy drive.

DMA MODE SELECTION

The optional floppy drive is configured to use DMA channel 2.

DATA TRANSFERS

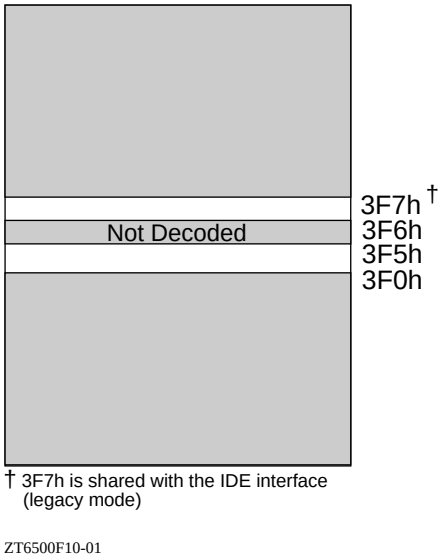
The floppy disk controller supports both polled and DMA-driven data transfers. Standard MS-DOS uses DMA, by default, for moving data back and forth between the host CPU's memory and the floppy disk controller. The DMA transfer is driven by the DMA controller on board the CPU board. The BIOS software is responsible for managing the low-level hardware in DOS systems. All transfers are 8 bits wide.

Memory

The floppy interface does not occupy or decode any memory address space.

I/O

The floppy interface I/O address range 3F0h-3F7h, with the exception of 3F6h. Port 3F7h is shared with the hard disk interface. The I/O map is shown below.



I/O Map

FLOPPY DISK CONTROLLER REGISTERS

The Floppy Disk Controller (FDC) interface is composed of eight registers. The table below defines the I/O address for all of the FDC registers.

Floppy Disk Controller I/O Registers

I/O Port Address	I/O Read Function	I/O Write Function
3F0h	Status Register A	—
3F1h	Status Register B	Status Register B
3F2h	Digital Output Register	Digital Output Register
3F3h	Tape Drive Register	Tape Drive Register
3F4h	Main Status Register	Data Rate Select Register
3F5h	Data	Data
3F6h	Reserved	Reserved
3F7h	Digital Input Register (Bit 7 only driven)	Configuration Control Register

FLOPPY DISK CONTROLLER DESCRIPTION

The optional floppy interface is software compatible with the DP8477, 765A, and N82077. The interface has 100% hardware register compatibility for PC/ATs and PS/2s. The 16-byte FIFO with programmable thresholds is extremely useful in systems with a large amount of bus latency.

Perpendicular Recording Mode

Perpendicular Recording Mode allows direct interface to perpendicular recording floppy drives that use the Toshiba format. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme then packs in more data bits for the same area.

The floppy interface with perpendicular recording drives can, at a minimum, read standard 3½" floppies as well as read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive. A single command puts the floppy interface into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires the 1 Mbits/s data rate. At this data rate, the FIFO eases the host interface bottleneck.

Status Register A (SRA)

3F0h Default

This register is read-only and monitors the state of the interrupt pin and several disk interface pins. This register is part of the PS/2 register set.

7	6	5	4	3	2	1	0
INT PENDING	DRV2*	STEP	TRK0*	HDSEL	INDX*	WP*	DIR

Status Register A

The **INT PENDING** bit is used by software to monitor the state of the floppy controller INTERRUPT pin. As a read-only register, no default value is associated with a reset other than that some drive bits change with a reset. The **INT PENDING**, **STEP**, **HDSEL**, and **DIR** bits are low after reset.

Status Register B (SRB)

3F1h Default

This register is read-only and monitors the state of several disk interface pins. This register is part of the PS/2 register set.

7	6	5	4	3	2	1	0
1	1	DRIVE SEL0	WRDATA TOGGLE	RDDATA TOGGLE	WE	MOT EN1	MOT EN0

Status Register B

As the only drive input, **RDDATA TOGGLE**'s level always reflects the level as seen on the cable.

The two **TOGGLE** bits do not read back the state of their respective pins directly. Instead, the pins drive a flip-flop which produces a wider and more reliably read pulse. **Bits 6 and 7** are undefined and always return a 1.

After any reset, the activity on the **TOGGLE** pins is cleared. **Drive select** and **motor** bits are cleared by the RESET pin and not by software resets.

Digital Output Register (DOR)

3F2h Default

The Digital Output Register contains the drive select and motor enable bits, a reset bit, and a DMAGATE* bit. This register is used in both PC/AT and PS/2 designs. The interface is shipped with the IDENT pin in PS/2 configuration.

7	6	5	4	3	2	1	0
MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMA GATE*	RESET	DRIVE SEL1	DRIVE SEL0

Digital Output Register

Bits 4-7, the **MOT ENx** bits, directly control their respective motor enable pins (ME0-3). A 1 means the pin is active. **Bits 0 and 1,** the **DRIVE SELx** bits, are decoded to provide four drive select lines; only one may be active at a time. These signals are active low on the interface. Standard programming practice is to set both MOT ENx and DRIVE SELx bits at the same time. The "Drive Activation Values" table below lists a set of DOR values to activate the drive select and motor enable for each drive.

Bit 3, the **DMAGATE*** bit, is not enabled on the FDC. DMAGATE* has no effect upon the INT and DRQ pins, and they are always active.

Bit 2, the **RESET*** bit, clears the basic core of the FDC and the FIFO circuits. Once set, it remains set until you clear it. This bit is set by a chip reset and the FDC is held in a reset state until you clear this bit. The RESET* bit has no effect upon this register. The RESET* pin clears this register.

Drive Activation Values

Drive	DOR Value
0	1Ch
1	2Dh
2	4Eh
3	8Fh

Tape Drive Register (TDR)

3F3h Default

This register allows you to assign tape support to a particular drive during initialization. Any future reference to that drive number automatically invokes tape support. This register is cleared by a hardware reset; software resets have no effect. Bits 2-7 are part of the "enhanced" tape drive register and are made available only when the EREG EN bit is set; otherwise, the bits are not driven.

7	6	5	4	3	2	1	0
MEDID1	MEDID0	DRVID1	DRVID0	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0

Tape Drive Register

Bits 2 through 7 are not writeable and remain three-stated if read when EREG EN is not set. **Bits 4 through 7** are not writeable, but return the states of the DRVID0, DRVID1, MEDID0, and MEDID1 pins when EREG EN is set.

The EREG EN bit is part of the COMMAND SET.

Bits 0 and 1, the **TAPESEL0** and **TAPESEL1** bits, allow you to select which drive is to be configured for tape drive support, as shown in the "Tape Drive Register Selection" table below. The Tape Select bits are hardware RESET to 0, making Drive 0 not available for tape support. Drive 0 is reserved for the floppy boot drive on reset.

Bits 2 and 3, the **BOOTSEL0** and **BOOTSEL1** bits, are not reset by software resets and are decoded as shown in the "Boot Drive Selection Options" table below. These bits allow for reconfiguring the boot-up drive and are reset only by a hardware reset. A drive can be enabled by remapping the internal DS0 and ME0 nodes to one of the other drive select and motor enable lines. Once a non-default value for BOOTSEL1 and BOOTSEL0 is selected, all programmable bits are virtual designations of drives; it is the user's responsibility to know the mapping scheme in the following table.

Tape Drive Register Selection

TAPESEL1	TAPESEL0	Drive Selected
0	0	None
0	1	1
1	0	2
1	1	3

Boot Drive Selection Options

BOOTSEL1	BOOTSEL 0	Mapping:
0	0	DS0 –> FDS0, ME0 –> FDME0 DS1 –> FDS1, ME1 –> FDME1 DS2 –> FDS2, ME2 –> FDME2
0	1	DS0 –> FDS1, ME0 –> FDME1 DS1 –> FDS0, ME1 –> FDME0 DS2 –> FDS2, ME2 –> FDME2
1	0	DS0 –> FDS2, ME0 –> FDME2 DS1 –> FDS1, ME1 –> FDME1 DS2 –> FDS0, ME2 –> FDME0
1	1	Reserved

Datarate Select Register (DSR)

3F4h Default

This register is included for compatibility and is write-only. Changing the data rate changes the timings of the drive control signals. Therefore, to avoid violating drive timings when changing data rates, choose a drive timing such that its fastest data rate will not violate the timing.

7	6	5	4	3	2	1	0
S/W RESET	POWER DOWN	PDOSC	PRE-COMP 2	PRE-COMP 1	PRE-COMP 0	DRATE SEL1	DRATE SEL0

Datarate Select Register

Bit 7, S/W RESET, behaves the same as DOR RESET except that this reset is self-clearing.

Bit 6, POWER DOWN, deactivates the internal clocks and shuts off the oscillator. Disk control pins are put in an inactive state. All input signals must be held in a valid state (D.C. level 1 or 0). POWER DOWN is exited by activating one of the reset functions.

Bit 5, the **PDOSC** bit, is used to implement crystal oscillator power management. The internal oscillator in the floppy controller can be programmed to be powered either on or off via PDOSC. This capability is independent of the chip's power-down state. Auto

power-down mode and power-down via the POWER DOWN bit have no effect over the power state of the oscillator.

In the default state the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a 1, the oscillator is shut off. Hardware reset clears this bit to 0. Neither of the software resets has any effect on this bit. Note that PDOSC should be set high only when the part is in the power-down state; otherwise, the part will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized.

Bits 2-4, PRECOMP 0-2, adjust the WRDATA output to the disk to compensate for magnetic media phenomena known as "bit shifting." The data patterns that are susceptible to bit shifting are well understood and the floppy controller compensates the data pattern as it is written to the disk. The amount of precompensation is dependent upon the drive and media, but in most cases the default value is acceptable.

The floppy controller starts precompensating the data pattern on Track 0. The CONFIGURE command can change the track on which precompensating starts. The "Precompensation Delays" table lists the precompensation values that can be selected, and the "Default Precompensation Delays" table on the following page lists the default precompensation values. The default value is selected if the three bits are zeros.

Bits 0 and 1, DRATESEL 0-1, select one of the four data rates as listed in the "Data Rates" table on the following page. The default value is 250 Kbps upon a chip reset. Other resets do not affect the DRATE or PRECOMP bits.

Precompensation Delays

PRECOMP BITS 432	Precompensation Delay
111	0.00 ns—DISABLED
001	41.67 ns
010	83.34 ns
011	125.00 ns
100	166.67 ns
101	208.33 ns
110	250.00 ns
000	DEFAULT

Default Precompensation Delays

Data Rate	Precompensation Delays
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
200 Kbps	125 ns

Data Rates

DRATESEL 1	DRATESEL 0	DATARATE
1	1	1 Mbps
0	0	500 Kbps
0	1	300 Kbps
1	0	250 Kbps

Main Status Register (MSR)

3F4h Default

The Main Status Register is a read-only register used to control command input and result output for all commands.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	DRV 3 BUSY	DRV 2 BUSY	DRV 1 BUSY	DRV 0 BUSY

Main Status Register

RQM—Indicates the host can transfer data if set to logical 1. No access is permitted if set to logical 0.

DIO—Indicates the direction of a data transfer once RQM is set. A 1 indicates a read is required and 0 indicates a write is required.

NON-DMA—This mode is selected in the SPECIFY command and will be set to 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

COMMAND BUSY—This bit is set to 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the

result phase. If there is no result phase (SEEK, RECALIBRATE commands), this bit is returned to 0 after the last command byte.

DRV x BUSY—These bits are set to 1 when a drive is in the seek portion of a command, including implied and overlapped seeks, and recalibrates.

Data (FIFO)

3F5h Default

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register (shown on the previous page).

The FIFO defaults to PC/AT compatible mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is it allows the system a larger DMA latency without causing a disk error. The two "FIFO Service Delay" tables below give several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold\#} \times \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5 \text{ microseconds} = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the floppy controller enters the command execution phase, it clears the FIFO of any data to ensure invalid data is not transferred.

An overrun or underrun terminates the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

FIFO Service Delay—1 Mbps Data Rate

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs

FIFO Service Delay—500 Kbps Data Rate

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

Digital Input Register (DIR)

3F7h Default

This register senses the state of the DSKCHG input and is read-only.

7	6	5	4	3	2	1	0
DSK CHG	—	—	—	—	—	—	—

Digital Input Register

Bit 7 , DSKCHG, monitors the pin of the same name and reflects the opposite value seen on the disk cable. **Bits 0-6** are not driven by the floppy controller.

Configuration Control Register (CCR)

3F7h Default

This register sets the data rate and is write only. In the PC/AT it is named the DSR.

7	6	5	4	3	2	1	0
—	—	—	—	—	—	DRATE SEL1	DRATE SEL0

Configuration Control Register

Refer to the "Data Rates" table in the "Datarate Select Register" section of this chapter for values.

Unused bits should be set to 0.

RESET

As discussed in the following topics, the FDC has three sources of reset: the RESET pin; a reset generated via a bit in the DOR; and a reset generated via a bit in the DSR. All resets take the FDC out of the power down state.

On entering the reset state, all operations are terminated and the FDC enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the CONFIGURE command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

RESET Pin

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset

These two resets are functionally the same. The DSR Reset is included to maintain compatibility. Both reset the floppy controller core, which affects drive status information and the FIFO circuits. The DSR Reset clears itself automatically, while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. You must manually clear this reset bit in the DOR to exit the reset state.

DMA TRANSFERS

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK*.

COMMAND SET/DESCRIPTIONS

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see if the first byte is a valid command and if valid, proceeds with the command. Refer to the National Semiconductor PC87303 (National Lit #112904-001) data sheet for details on the COMMAND SET.

CHAPTER 11. SYSTEM REGISTERS

A system register is used to control and monitor a variety of functions on the ZT 6500. The system register is read/write capable. Normally, only the system BIOS uses this register, but it is documented here for application use as needed. Take care when modifying the contents of this register: the system BIOS may be relying on the state of the bits under its control.

SYSTEM REGISTER DEFINITION

The System register can be accessed at I/O port 78 (see the "System Register" illustration on the following page).

Bits 0 - 2 are used by the BIOS for controlling accesses to the on-board FLASH memory. These bits should not be modified.

Bit 3 is used for arming the watchdog timer. See the "Watchdog Timer Operation" section in Chapter 12 for more information on using this bit.

ASIC SYSTEM REGISTER DEFINITIONS

In addition to the System register, the ZT 6500 uses several ports of the on-board Digital I/O ASIC for monitoring and controlling other board functions. These registers are mapped to I/O ports E3h, E4h, and E5h. Descriptions of these registers are given below. For more information on how the Digital I/O ASIC works, see the "Functional Description" section in Chapter 13.

ASIC System Register 0 (Port E3h)

This register is illustrated in the "ASIC System Register 0" figure on the following page.

Bit 0: On-board LED. (See Chapter 14 for more information)

Bit 1: Tachometer Input. This bit can be used to monitor a fan/sink with a tachometer input. This input is connected to J3 pin 2. The factory installed fan/sink does not contain a tachometer output. See the "Tachometer Monitoring" section in Chapter 15 for more information on using this feature.

Bit 2: Reserved. (Optional On-board IDE LED)

Bit 3 - **Bit 7:Board Revision.** This port reads the status of CT12-CT16 to determine the current board revision. Revision 0 = 1Fh.

ASIC System Register 1 (Port E4h)

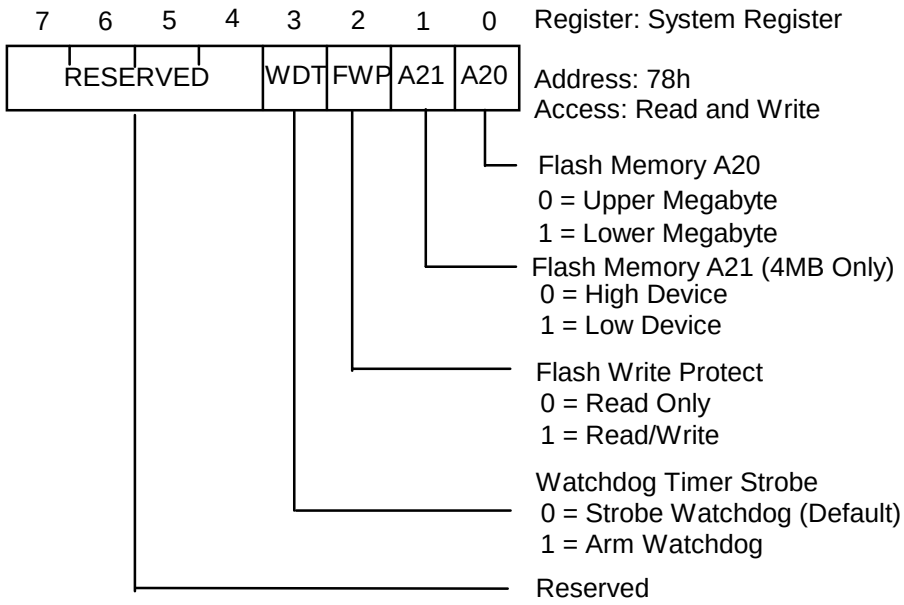
This register is illustrated in the "ASIC System Register 1" figure on the following page.

Bit 0 - Bit 1: Power Supply DEG, FAL#. These bits monitor the DEG# and FAL# signals. These bits are enabled by cuttable traces CT19 and CT20

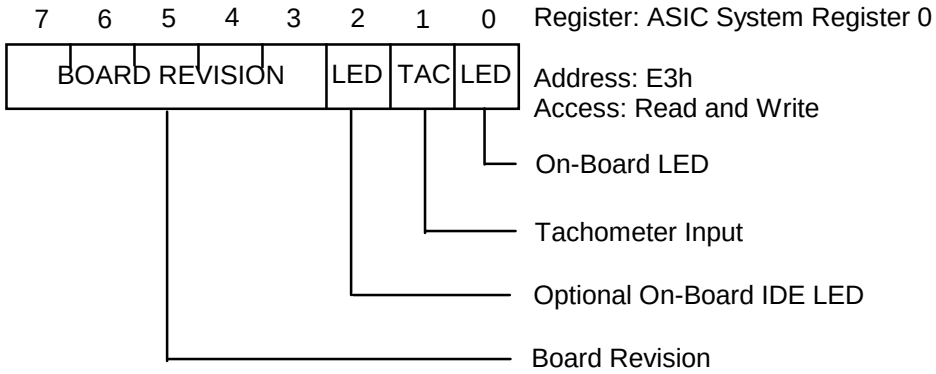
Bit 2 - Bit 7: Reserved. These bits are reserved for future use.

ASIC System Register 2 (Port E5h)

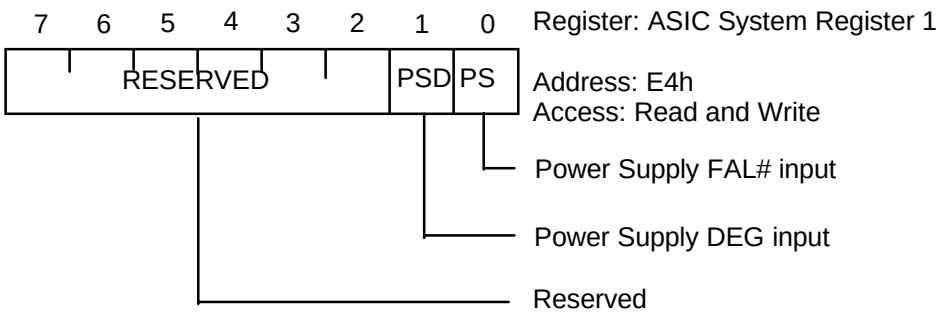
This register is reserved for future use.



System Register



ASIC System Register 0



ASIC System Register 1

CHAPTER 12. WATCHDOG TIMER

The primary function of the watchdog timer is to monitor ZT 6500 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are listed below.

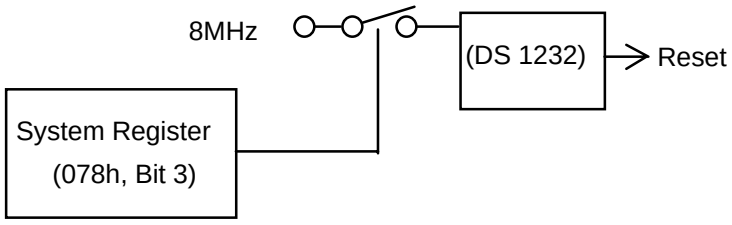
- Single-stage
- Enabled and disabled through software control
- Armed and strobed through software control

WATCHDOG TIMER OPERATION

The watchdog timer architecture is illustrated in the "Watchdog Timer Architecture" figure before. The watchdog timer is implemented in the Dallas Semiconductor DS1232 system monitor.

After power on or reset, the watchdog function is disabled, meaning that the watchdog is continually being strobed by an 8 MHz signal. Bit 3 of the System Register (078h) must be programmed with a logical one to enable the watchdog timer to begin operation. If the watchdog is allowed to expire, a reset is generated. To strobe the watchdog, Bit 3 of the System Register (078h) must be written with a logical 0 and then a logical 1.

The watchdog timeout period is fixed at 500 ms minimum and 2000 ms maximum. Software must strobe the watchdog timer within 500 ms to guarantee that the system is not reset.



Watchdog Timer Architecture

ADDITIONAL INFORMATION

Refer to the Dallas Semiconductor DS1232 data sheet for more information on the watchdog timer and the associated operating modes.

CHAPTER 13. PARALLEL I/O

The ZT 6500 includes six 8-bit parallel ports for a total of 48 I/O signals. Three of the parallel ports are available to the application through frontplane connector J1. The remaining three parallel ports are dedicated to controlling and monitoring local operations (see the "ASIC System Register Definitions" section in Chapter 11). The general operation of the six parallel ports is explained in this chapter. The specific features managed by the dedicated ports are explained in Chapter 11, "System Registers."

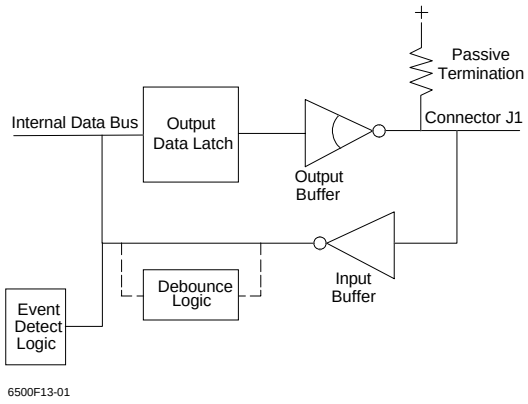
Each of the parallel I/O signals is configured as an input or an output with readback under software control. The major features of the parallel I/O are listed below.

- 12 mA sink current
- Software programmable input debounce
- Stable outputs during power up and reset
- Continuous data transfer rates up to 1 Mbyte/second
- Software programmable event sense interrupt generation

FUNCTIONAL DESCRIPTION

The parallel I/O signals are supported through the 16C50A, a custom ASIC device designed by Ziatech. Refer to Appendix C for tips on preventing latchup from the CMOS parts in the 16C50A.

A functional diagram of each I/O signal is illustrated in the following figure. The diagram includes an output latch, an output buffer, and an input buffer. These functional blocks are described in the following topics.



Parallel Port Functional Diagram

Output Latch

The output latch stores the data present on the internal data bus during a write operation to the parallel port. The data is latched until altered by another parallel port write, until a system reset, or until the power is turned off. The output latch is initialized with a logical 0 during power on and system reset.

Output Buffer

The output buffer isolates the output latch from connector J1. The output buffer is an inverting open-collector device with 12 mA of sink current and glitch-free operation during power cycles. The inversion means that a logical 0 written to the parallel port appears as a TTL high at connector J1, and a logical 1 written to the parallel port appears as a TTL low at connector J1.

The open collector feature permits each parallel I/O signal to be software configured as an input. To use a parallel port signal as an input, a logical 0 must first be written to the output latch. This causes the output buffer to become an open-collector gate and prevents contention with the input signal. The passive termination ranges from 25k Ω minimum to 120k Ω maximum. Applications needing a predictable rise time should provide additional termination.

Input Buffer

The input buffer is enabled during read operations to transfer the data from connector J1 to the internal data bus. If the parallel port bit is configured as input, the data read is the data driven by an external device.

The input buffer is an inverting device. This means that data read from the parallel port as a logical 0 is a TTL high at connector J1, and data read from the parallel port as a logical 1 is a TTL low at connector J1.

Debounce Control Logic

The debounce control logic is a new feature of the 16C50A digital ASIC. This feature eliminates the need for external logic or extensive software to remove unstable input signals to the digital ASIC. The internal circuitry of the digital ASIC automatically filters out glitches that can occur in received signals.

For example, if the digital ASIC is programmed for an 8 ms period, the incoming signal must be stable for the entire 8 ms period, with no glitches, before it is recognized by the digital ASIC.

The debounce control logic is controlled on the 16C50A by registers E0h, E1h, E2h, and E3h in register bank 2. An 8 MHz clock is used by the 16C50A for a timing reference, thus allowing the debounce circuit to be programmed for a debounce delay of 4 µs, 64 µs, 1 ms, or 8 ms.

Upon initialization of the debounce circuitry, be sure to delay at least the programmed debounce time before reading any of the input ports or the external event signals. This guarantees that the input data is valid prior to being used by the software.

Event Sense Detection Logic

The 16C50A contains event sense logic that allows the detection of either positive or negative events. The event input edge is controlled on a nibble basis by software. The event bits are enabled on an individual basis. Registers E0-E6h in register bank 1 are used to control and monitor the event sense logic.

To use the event inputs:

1. Determine which events are to be enabled and what polarity is to be detected, high to low (negative) or low to high (positive) transitions.

2 Set each port to the desired polarity.

3. Enable each of the event inputs to be detected.

All I/O and external event inputs are reset to negative events, and disabled after a Reset signal has occurred.

PROGRAMMABLE REGISTERS

The 16C50A supports standard and enhanced operating modes. The ZT 6500 BIOS configures the 16C50A for enhanced operating mode. There are three register banks (listed below) used for controlling the 16C50A. These register banks are selected by programming bits 6 and 7 of I/O port E7h with a "00" for bank 0, a "01" for bank 1, and a "10" for bank 2. The six 8-bit ports are allocated as follows.

Enhanced Bank 0 I/O Port Addressing

Enhanced Bank 1 I/O Port Addressing

Enhanced Bank 2 I/O Port Addressing

- The three I/O ports at E0h, E1h, and E2h are available through connector J1 (refer to Appendix B for the J1 connector pin assignments.
- The three I/O ports at E3h, E4h, and E5h are dedicated to managing functions local to the ZT 6500. Refer to Chapter 11, "System Registers," for additional information.

Enhanced Bank 0 I/O Port Addressing

Select this register bank by programming bits 6 and 7 of I/O port E7h with a "00".

Address	Register	Read Operation	Write Operation
00E0h	Port 0 Data	DIG0-DIG7	DIG0-DIG7
00E1h	Port 1 Data	DIG8-DIG15	DIG8-DIG15
00E2h	Port 2 Data	DIG16-DIG23	DIG16-DIG23
00E3h	Port 3 Data (System Register 0)	—	—
00E4h	Port 4 Data (System Register 1)	—	—
00E5h	Port 5 Data (System Register 2)	—	—
00E6h	Reserved	—	—
00E7h	Write Inhibit/Bank Address	Status	Control

Enhanced Bank 1 I/O Port Addressing

Select this register bank by programming bits 6 and 7 of I/O port E7h with a "01".

Address	Register	Read Operation	Write Operation
00E0h	Port 0 Event Sense	Status	Control
00E1h	Port 1 Event Sense	Status	Control
00E2h	Port 2 Event Sense	Status	Control
00E3h	Port 3 Event Sense	Status	Control
00E4h	Port 4 Event Sense	Status	Control
00E5h	Port 5 Event Sense	Status	Control
00E6h	Event Sense Manage	Status	Control
00E7h	Bank Address	Status	Control

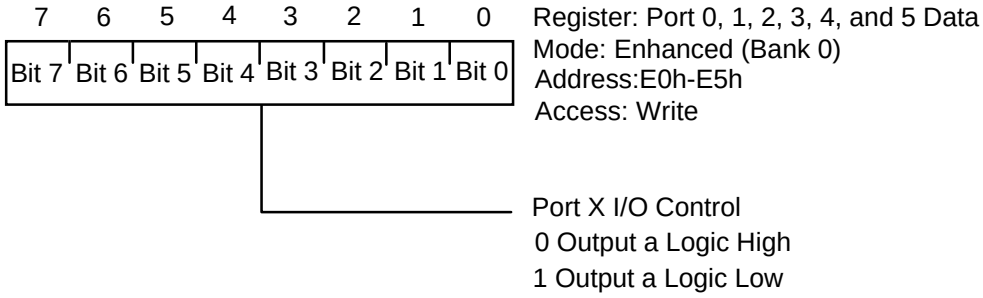
Enhanced Bank 2 I/O Port Addressing

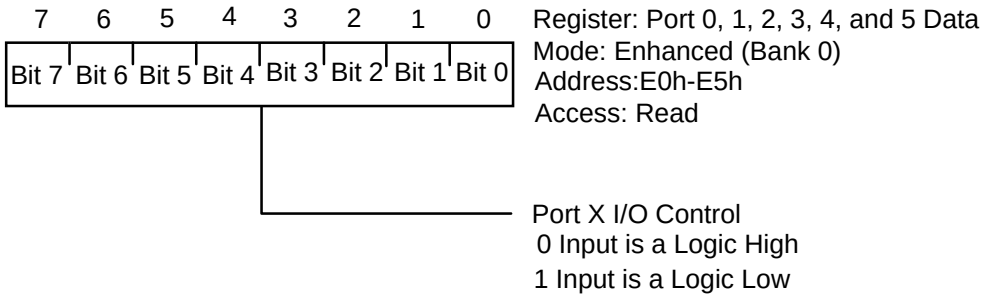
Select this register bank by programming bits 6 and 7 of I/O port E7h with a "10".

Address	Register	Read Operation	Write Operation
00E0h	Debounce Configure	Status	Control
00E1h	Debounce Duration	Status	Control
00E2h	Debounce Duration	Status	Control
00E3h	Debounce Clock	—	Control
00E4h	Reserved	—	—
00E5h	Reserved	—	—
00E6h	Reserved	—	—
00E7h	Bank Address	Status	Control

Port Data Registers

The six I/O ports assign the least significant I/O line to the least significant data line (D0). Each bit is changed or monitored by writing or reading the individual I/O port. On a power up or reset, the ports are reset to 0, forcing the outputs to be set high.





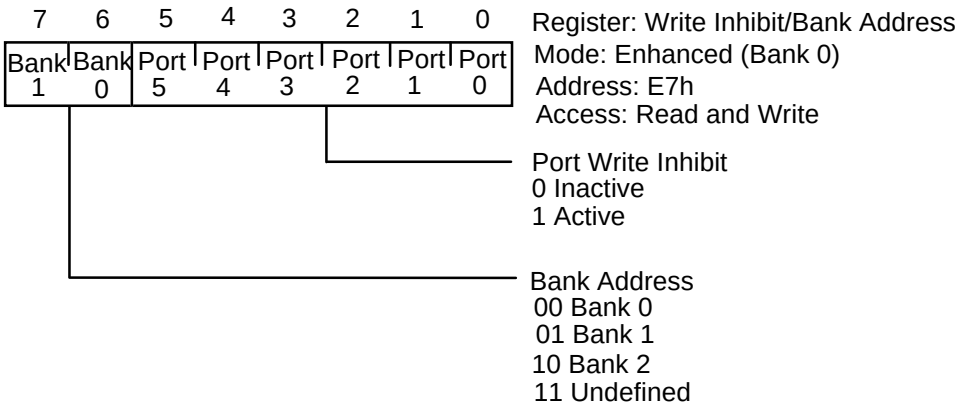
Note: To set a particular port and bit as an input, write a logic 0 to that port and bit.

Port Data Registers

Write Inhibit / Bank Address Register

The mask register is used to mask the ability to write data to the six output ports. Power-up default has the register unmasked to allow writes to the output ports. Writing the mask register bits D0-5 with a 1 masks I/O ports 0-5, respectively, while a read returns the status of the mask register.

Bits 7 and 6 of the register select which bank of registers is selected. A logic 00 selects bank 0, a 01 selects bank 1, and 10 selects bank 2, respectively. A logic 11 is an invalid state and should never be written to the Mask Register.

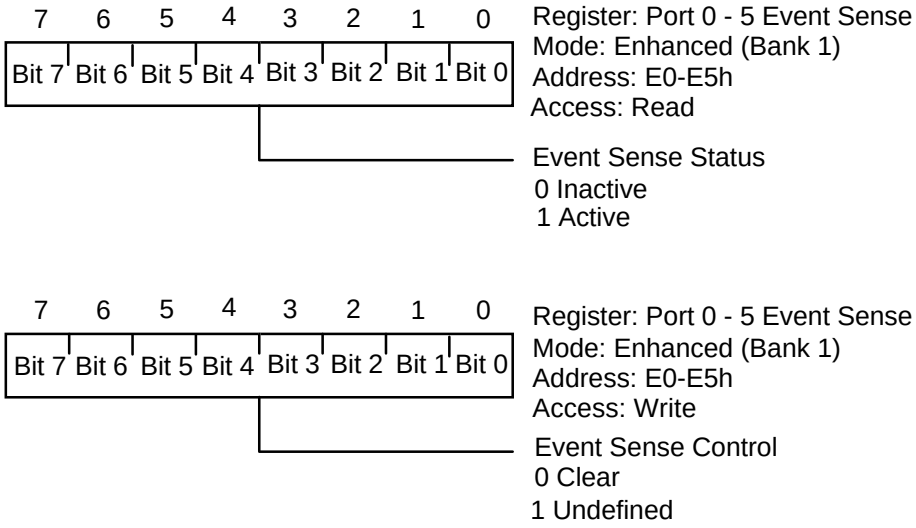


Write Inhibit / Bank Address Register

Port Event Sense Register

Reading the event sense status of each port gets the status of each I/O port sense line. Writing to the event sense status of each port with the corresponding bit equal to 0 clears that particular sense line.

When writing ports 0 - 5, each data bit written with a logic 0 clears its corresponding event sense flip-flop. Each data bit of ports 0 - 5 must be written with a 1 to re-enable the corresponding event sense input after it is cleared. Reading ports 0 - 5 returns the event sense flip-flop status.



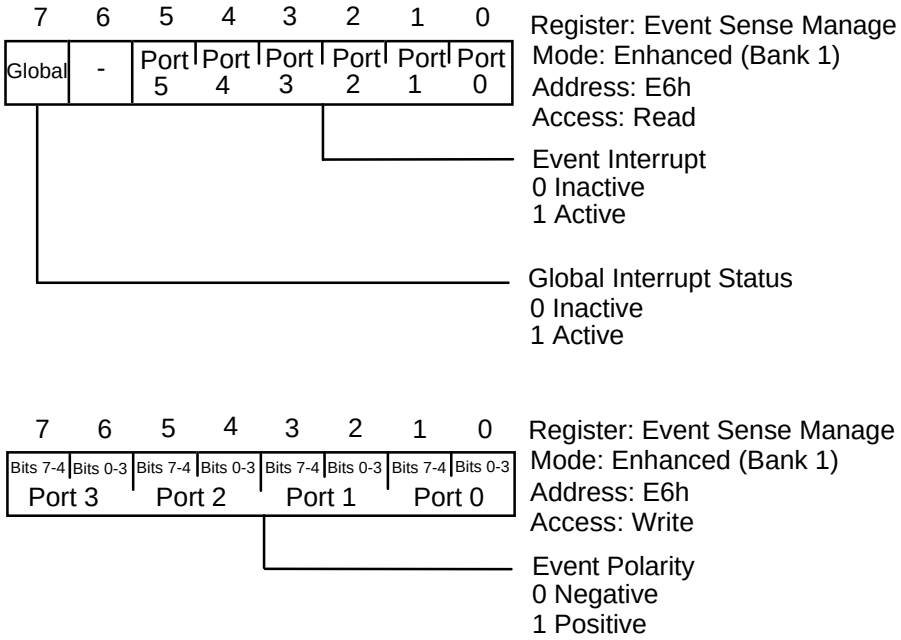
Port Event Sense Register

Event Sense Manage Register

A write to this register controls the polarity of the Sense Event for I/O ports 0 - 3. Each bit represents a nibble (4 bits) of the port. A logic 0 senses negative events, while a 1 senses positive events. The polarity of the event sense logic must be set prior to enabling the event input logic.

A read from this register returns the event status on I/O ports 0 - 5 and the status of the interrupt pin.

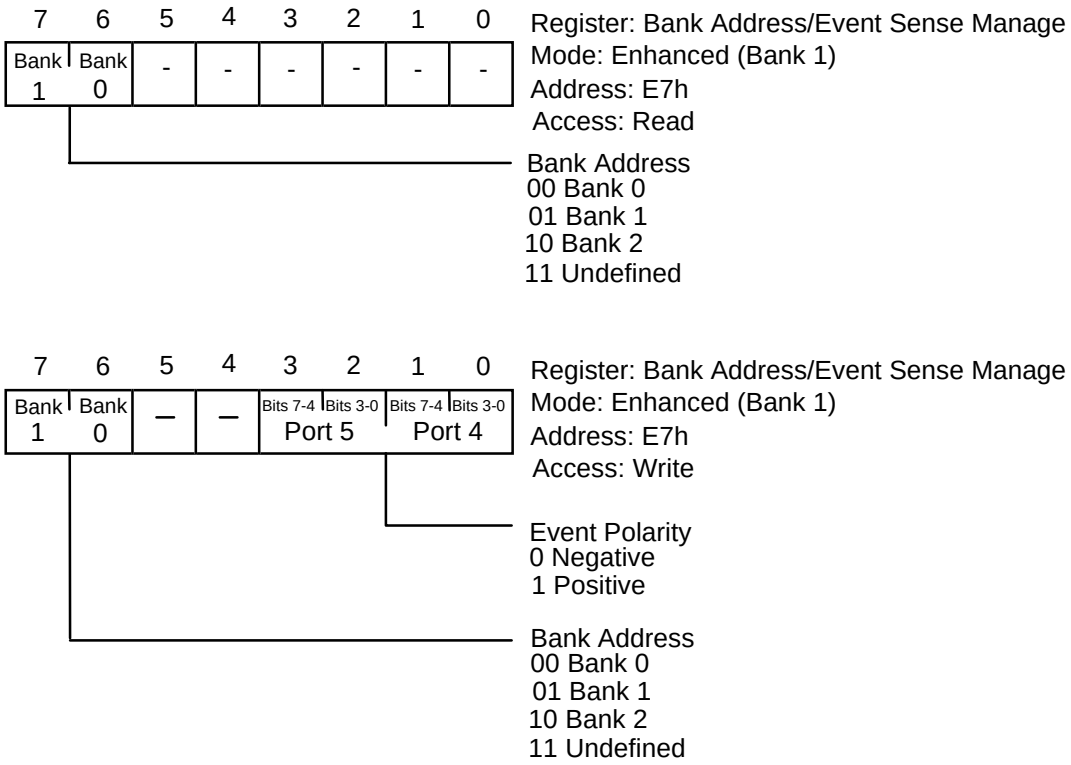
Bit 7, the global interrupt pin, indicates an event sense was detected on any of the six ports (1=interrupt is asserted).



Event Sense Manage Register

Bank Address Register

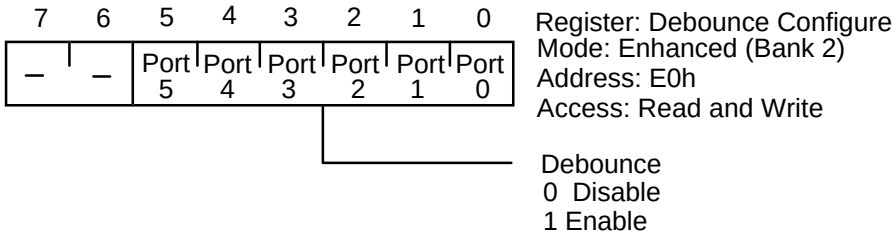
This register controls the polarity of the Sense Event for I/O ports 4 and 5. A 0 senses negative events, while a 1 senses positive events. Bits 6 and 7 select an individual bank. A read from this register returns only the bank status information.



Bank Address Register

Debounce Configure Register

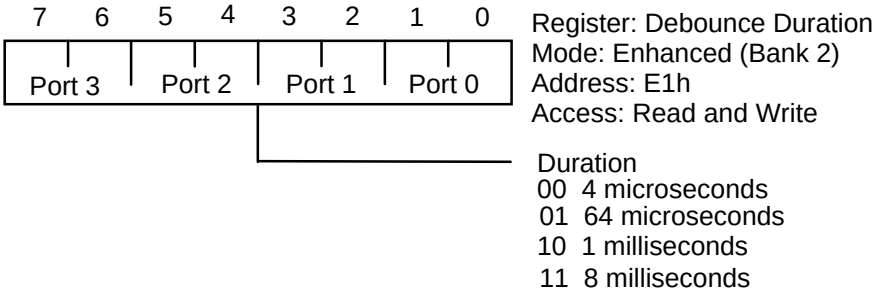
This register controls whether each individual port is passed through the debounce logic. A logic 0 disables the debounce logic, and a logic 1 enables the debounce logic.



Debounce Configure Register

Debounce Duration Register (Ports 0-3)

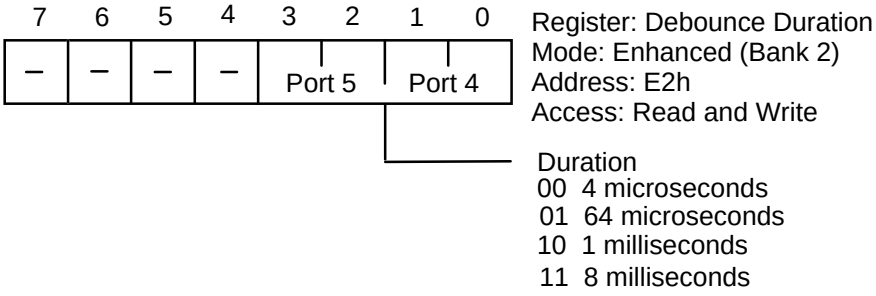
This register controls the duration required by each input signal before it is recognized for ports 0 - 3. The debounce times available are 4 µs, 64 µs, 1 ms, and 8 ms. A debounce value of 00 sets 4 µs, 01 sets 64 µs, 10 sets 1 ms, and 11 sets 8 ms. This register controls ports 0 - 3. The default value is 00 for a 4 µs debounce period.



Debounce Duration Register (Ports 0-3)

Debounce Duration Register (Ports 4-5)

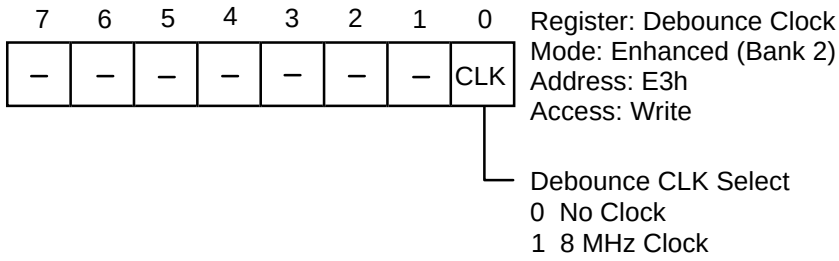
This register controls the duration required by each input signal before it is recognized for ports 4 and 5. The debounce times available are 4 µs, 64 µs, 1 ms, and 8 ms. A debounce value of 00 sets 4 µs, 01 sets 64 µs, 10 sets 1 ms, and 11 sets 8 ms. This register controls ports 4 and 5. The default value is 00 for a 4 µs debounce period.



Debounce Duration Register (Ports 4-5)

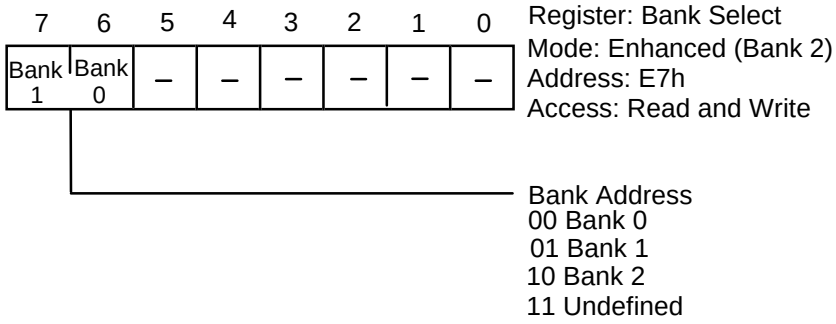
Debounce Clock Register

This bit must be set to a 1 to use the debounce feature. The default value is 0. A read from this port is undefined.



Debounce Clock Register

Bank Select Register



Bank Select Register

CHAPTER 14. PROGRAMMABLE LED

The ZT 6500 includes two Light-Emitting Diodes (LEDs). A green LED for the optional IDE disk drive (not loaded) is mounted next to jumper W3. A red general purpose LED is located next to the frontplane pushbutton reset. The red LED is software programmable through the Digital I/O ASIC (I/O port E3, bit 0). Writing a logical 0 to the LED bit turns the LED off and writing a logical 1 to the LED bit turns the LED on. The LED is turned off after a power cycle or a reset.

The LED bit is in the same register as several system level functions. It is important to preserve the state of the other bits in this register when modifying the LED status. The following code demonstrates the mechanism for modifying the LED bit:

```
;  set LED ON
cli                     ; clear interrupts
in     al, E3h          ; read current state
or     al, 01h          ; set LED bit
out    E3h, al          ; output new value for register
sti                     ; re-enable interrupts

;  set LED OFF
cli                     ; clear interrupts
in     al, E3h          ; read current state
and  al, FEh            ; clear LED bit
out    E3h, al          ; output new value for register
sti                     ; re-enable interrupts
```

CHAPTER 15. THERMAL CONSIDERATIONS

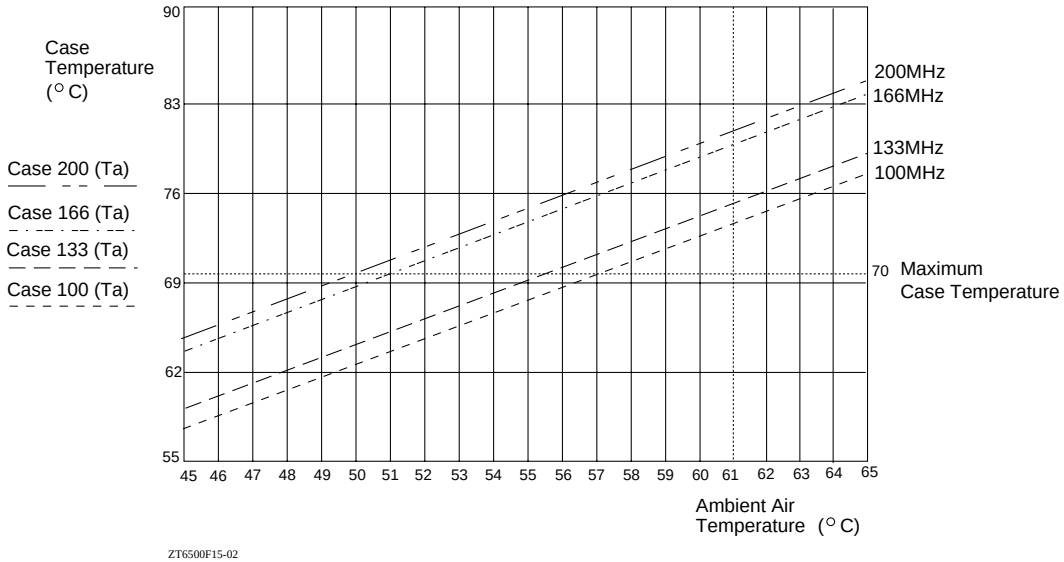
The ZT 6500 comes from the factory with an integrated fan/heatsink for cooling the processor. This fan/sink allows a maximum ambient air temperature between 51º C and 59º C, depending on the speed of the Pentium processor (70º C maximum case temperature).

The "Pentium Processor(s) Maximum Ambient Temperature" table below lists the **maximum** ambient temperatures for the various processor options.

Pentium Processors Maximum Ambient Temperatures

Processor Speed (MHz)	Max. Ambient Temperature (°C)
100	57.0
133	55.5
166	51.0
200	50.0

The "Ambient Air Temperature Vs. Pentium Processor Case Temperature" figure below shows the **relationship** between ambient temperature and case temperature (when operated with the integrated fan/heatsink) for the various processor options sold with the ZT 6500.

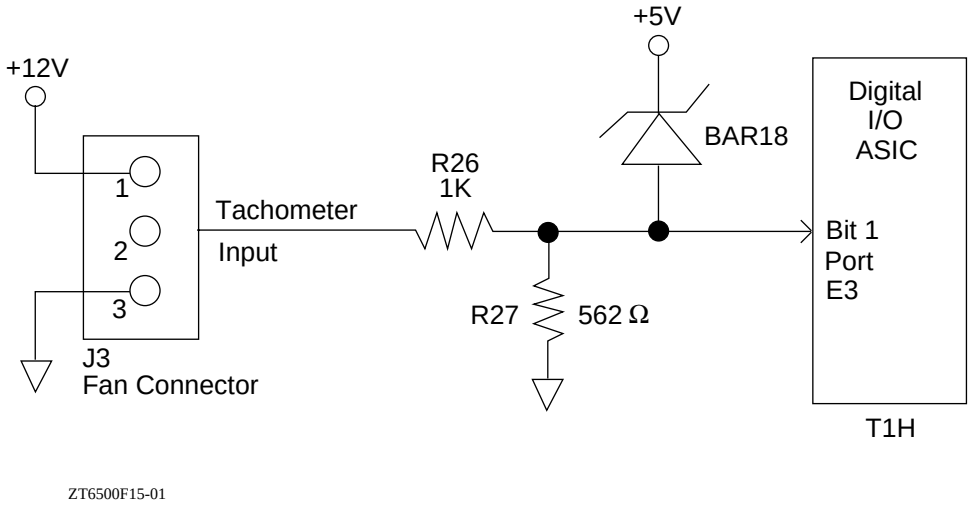


Ambient Air Temperature Vs. Pentium Processor Case Temperature

TACHOMETER MONITORING

The ZT 6500 has optional circuitry on board for monitoring a fan with a tachometer output. The tachometer input is connected to J3 pin 2. The input circuitry, shown in the "Tachometer Monitoring Input Circuitry" figure below, contains a two resistor voltage divider (R26, R27) and a protection diode (D6) to allow for a +12V tachometer signal. The tachometer signal connects to the Digital I/O ASIC bit 1 at I/O port E3h. Since this input is directly connected to the tachometer, user-written software is necessary to determine if the fan is working properly. Most fan tachometers have an output rate of approximately 100 Hz; this input therefore changes states approximately every 5 ms.

Note: The factory installed fan/sink does not have a tachometer output.



Tachometer Monitoring Input Circuitry

CHAPTER 16. FLASH MEMORY

The ZT 6500 comes with 2 or 4 Mbytes of on-board Flash memory. This memory is partitioned into two areas, one for the system BIOS, and the other for a non-volatile solid state disk. The system BIOS occupies 128 Kbytes. The rest is used for solid state disk. The solid state disk can be accessed at the P: drive and its size configured using the BIOS setup page. This solid state disk can be used to boot DOS and other user programs. Data can also be logged to this drive. However, since it is a Flash memory it has a limited write cycle life (approximately 100,000 cycles).

The Flash disk is mapped in upper memory at 1 Gbyte to 1 Gbyte+1 Mbyte. The system register (see Chapter 11) is used to control write accesses and page to 1 Mbyte portions. Access to the Flash disk is transparent to the user and handled by STD.SYS. The Flash disk is readable and writable in the same manner as magnetic media; thus it can be treated similar to a hard disk.

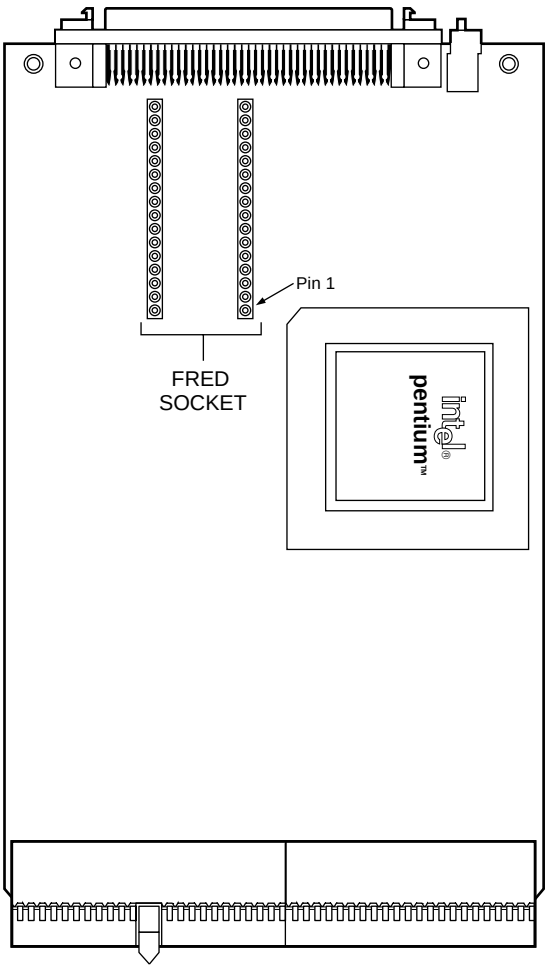
The BIOS portion of the Flash memory is mapped as a 128 Kbyte block in lower memory at E0000h to FFFFFh (896 K to 1 Mbyte). The BIOS can be re-Flashed for BIOS updates or if it becomes corrupted by using the FLASH.EXE utility available from Ziatech.

FRED

If for some reason the ZT 6500's BIOS does get corrupted, a Flash Recovery Emergency Device (FRED) socket has been provided on board. This 32-pin socket can be used with an EPROM that has been programmed with the BIOS to allow the board to boot. This EPROM can be ordered from Ziatech (order part number ZT 95195).

To boot from the FRED socket, first remove jumper W7, then insert the EPROM into the FRED socket. Make sure the device is correctly oriented and pin 1 is nearest the Pentium. See the "FRED Socket Location" figure on the following page for the location and orientation of the FRED socket

After powering the board, the on-board FLASH should be reprogrammed with the BIOS by using the FLASH.EXE utility (see the next section for detailed instructions). After Flashing the BIOS, turn off power, remove the EPROM, and reinsert jumper W7.



FRED Socket Location

FLASH UTILITY PROGRAM

FLASH.EXE is a utility program that comes with the Programmers toolkit. It allows the user to quickly and conveniently modify the BIOS in the on-board Flash memory. This eliminates the need for a PROM programmer and prevents the user from having to remove boards and chips from the system.

To reprogram the BIOS on the ZT 6500, use the following syntax at a DOS prompt:

```
FLASH  /b  95195-0.XXX
```

where 95195-0.XXX is the BIOS image for the ZT 6500. See the *Ziatech Industrial Computer System Manual for BIOS Version 4* for more information on the Flash utility.

APPENDIX A. BOARD CONFIGURATION

The ZT 6500 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS SETUP mechanism. Some options cannot be software controlled and are configured with jumpers or cuttable traces. Jumper options are made by installing and removing shorting receptacles. Cuttable trace options are made by installing and removing surface mount 0 Ω resistors.

This appendix covers SETUP options, jumper options, and cuttable trace options. It also provides an illustration showing the locations of jumpers and cuttable traces on the ZT 6500.

BIOS SETUP OPTIONS

The ZT 6500 has several features that can be configured with the BIOS SETUP program. The SETUP program is executed during the boot sequence when the key "**s**" is typed. In DOS systems, SETUP may be executed by running the SETUP.COM program from the command line.

For setup procedures and configuration of the ZT 6500, see the section "ZT 6500 Setup" in Chapter 2.

JUMPER OPTIONS AND LOCATIONS

The ZT 6500 includes seven jumpers labeled W1-W7. They are located next to the battery.

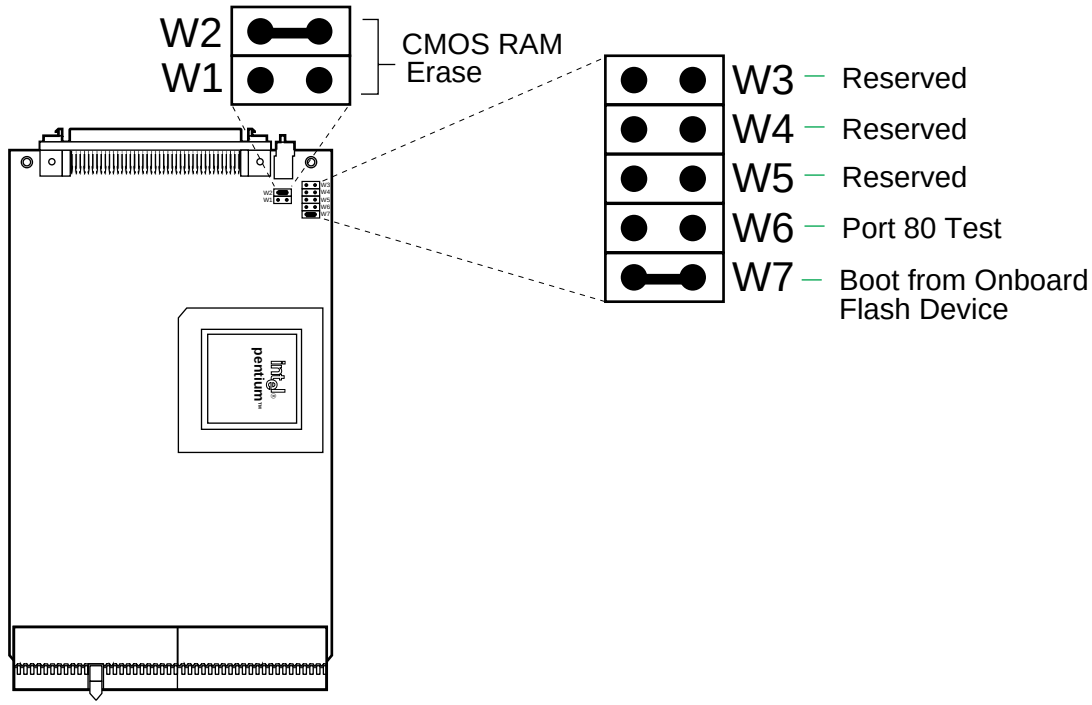
The "DOS Factory Default Jumper Configuration" figure on the following page illustrates the factory default jumper configuration for ZT 6500 boards purchased in a DOS system. The "Customer Jumper Configuration" illustration, also on the following page, provides a blank jumper layout; use this figure to document your jumper configuration if it differs from the factory default.

JUMPER CROSS-REFERENCE TABLE

The following table divides the jumper options into functional groups.

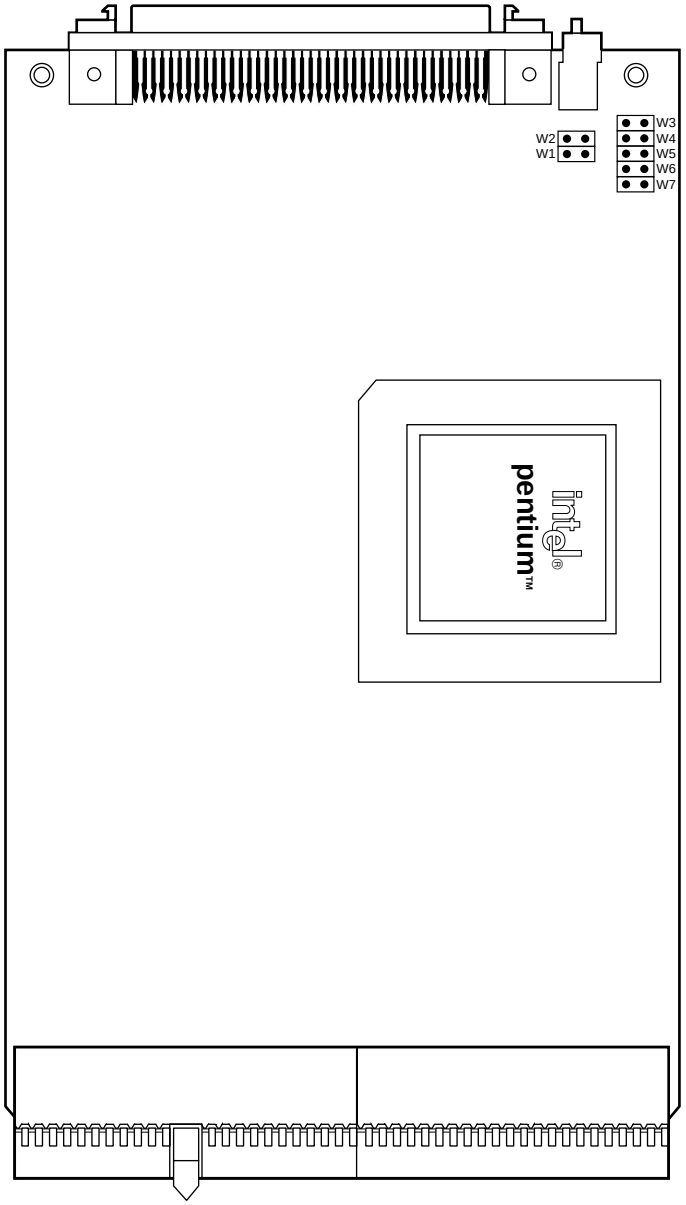
Jumper Cross Reference

Function	Jumpers
CMOS RAM Erase	W1,W2
Boot From On-Board Flash Device	W7
Reserved	W3-W5
Port 80 Test	W6



ZT6500FA-01

DOS Factory Default Jumper Configuration



ZT6500FA-02

Customer Jumper Configuration

JUMPER DESCRIPTIONS

The following topics list the jumpers in numerical order and provide a detailed description of each jumper. A dagger (†) indicates the default jumper configuration. Click on the green jumper number at the top of the topic for an illustration showing jumper locations.

W1, W2 (CMOS RAM Erase)

Remove the contents of the battery backed CMOS configuration RAM with these jumpers. The CMOS RAM is erased by turning off the power and moving the W2 shorting jumper to position W1 and back to W2 again.

	W1	W2	CMOS Configuration RAM
†	OUT	IN	Normal operation
	IN	OUT	Erase

W3-W5 (Reserved)

These jumpers must be left uninstalled.

W6 (Port 80 Test)

W6 allows the on-board Digital I/O ASIC to be re-mapped to decode at I/O port 80h instead of E0h. This is useful for debug purposes. The BIOS uses port 80 to output post codes during initialization of the various subsystems. The port 80 codes may be monitored on bits 0-7 of the Digital I/O output on connector J1 (pins 52-59).

	W6	Port 80 test
	IN	Test mode—DIO mapped at 80h
†	OUT	Normal mode—DIO mapped at E0-E7h

W7(Boot From On-Board Flash Device)

W7 enables the ZT 6500 to begin program execution from the local Flash device or an alternate boot image loaded in the socket at T5H. Select the alternate boot operation if the local Flash device is corrupted and the ZT 6500 fails to boot properly. W7must be removed when booting from a device in socket T5H.

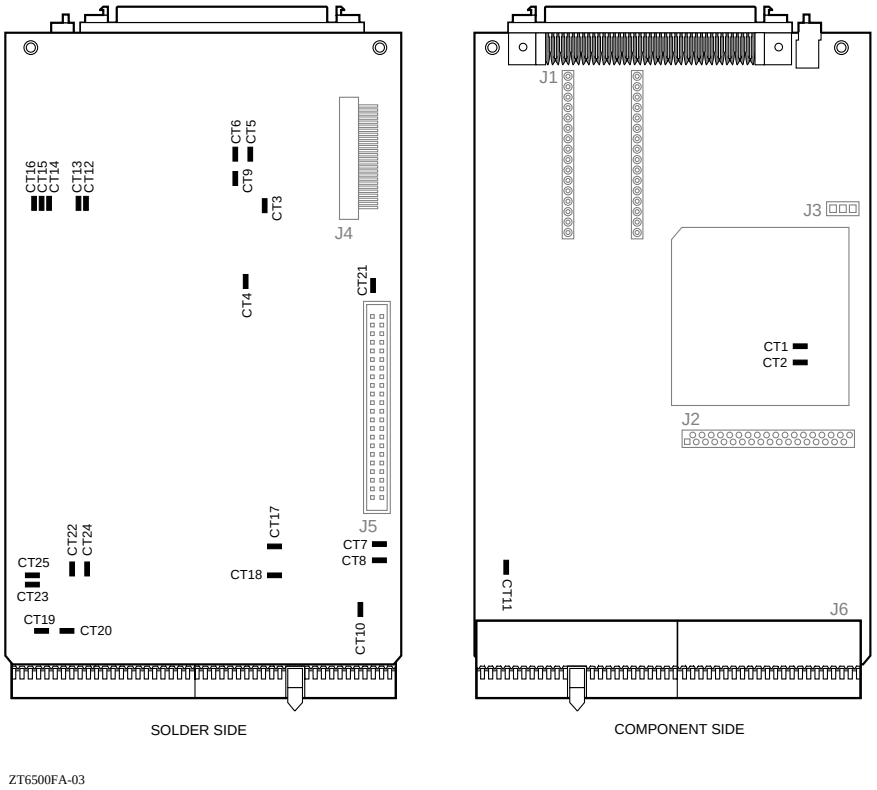
	W7	Boot Source
†	IN	Local Flash memory
	OUT	Alternate boot image in socket at T5H

† Factory default configuration

CUTTABLE TRACE OPTIONS AND LOCATIONS

The ZT 6500 contains several cuttable traces (zero ohm shorting resistors) that allow the user to configure other board options. The "Cuttable Trace Locations" figure below shows the placement of the ZT 6500 cuttable traces. The "Cuttable Trace Definitions" table on the following page provides a quick cross-reference for the ZT 6500 cuttable trace descriptions that follow. There are two types of cuttable traces on the ZT 6500: single option and double option. **Single option cuttable traces** are implemented using two 0603 surface mount pads. A zero ohm shorting resistor is then soldered between these pads to make the connection. **Double option cuttable traces** (CT5, CT6, CT9, CT22, CT23, CT24, CT25) are implemented using three 0603 surface mount pads. The zero ohm shorting resistor is then placed between one set of pads, depending on the chosen option.

Note: Cuttable trace modifications should be performed by a qualified technician only. These modifications require a technician who is familiar with surface mount soldering techniques. The product warranty is voided if the board is damaged by customer modifications. If you do not have access to a qualified technician, contact Ziatech Technical Support. For large production orders, Ziatech can also set up “specials” that are pre-configured at the factory. Contact Ziatech for more information.



Cuttable Trace Locations

Cuttable Trace Definitions

CT#	DEFAULT	DESCRIPTION
CT1, CT2		CPU Bus Fraction
CT3, CT4	OUT	Reserved
CT5	1-2†	LPT DMA 0
	2-3	LPT DMA 3
CT6	1-2†	LPT DMA 0
	2-3	LPT DMA 3
CT7, CT8	‡	Clock Frequency Select
CT9	1-2†	5V Flash Prog. Voltage
	2-3	12V Flash Prog. Voltage
CT10	IN	IRQS Support
CT11	IN	IRQP Support
CT12	IN	Board Rev. Bit 0
CT13	IN	Board Rev. Bit 1
CT14	IN	Board Rev. Bit 2
CT15	IN	Board Rev. Bit 3
CT16	IN	Board Rev. Bit 4
CT17, CT18	OUT	Reserved
CT19	OUT	P.S. Fail
CT20	OUT	P.S. Degrade
CT21	OUT	B.P. PRST-
CT22	1-2	GNT0 to Slot 2
	2-3†	GNT0 to Slot 7
CT23	1-2†	GNT1 to Slot 3
	2-3	GNT1 to Slot 8
CT24	1-2	REQ0 to Slot 2
	2-3†	REQ0 to Slot 7
CT25	1-2	REQ1 to Slot 3
	2-3†	REQ1 to Slot 8

† Factory default configuration

‡ Configured at the factory according to the board option ordered

CT1, CT2, CT7, CT8 (CPU Bus Fraction)

These cuttable traces can be used to control the CPU/PCI bus frequency for different speed processors as shown in the following table.

	Speed (MHz)		Cuttable Traces			
CPU	**CPU Bus**	**PCI Bus**	**CT1**	**CT2**	**CT7**	**CT8**
90	60	30	Out	Out	Out	In
100	66	33	Out	Out	In	Out
120	60	30	Out	In	Out	In
133	66	33	Out	In	In	Out
150	60	30	In	In	Out	In
166	66	33	In	In	In	Out
200	66	33	In	Out	In	Out

CPU Speed Multiplier Settings

CT1 and CT2 are used to set the multiplication factor of the internal CPU clock.

CPU Frequency Multiplier	CT1	CT2
1.5X	Out	Out
2.0X	Out	In
2.5X	In	In
3.0X	In	Out

Bus Frequency Settings

CT7 and CT8 are used to set the CPU and PCI bus frequency. The PCI bus frequency is always one-half of the CPU bus frequency.

Bus Frequency CPU/PCI (MHz)	CT7	CT8
50/25	In	In
60/30	Out	In
66/33	In	Out
n/a	Out	Out

CT3, CT4, CT17, CT18 (Reserved)

These cuttable traces are reserved for factory use only.

CT5, CT6 (LPT DMA)

CT5 and CT6 configure the LPT port (in extended modes) to use DMA channel 0 or channel 3.

CT9 (Flash Programming Voltage)

Programming voltage for on-board Flash memory. This is set at the factory depending on the type of Flash device loaded and should not be modified. Allows support of both 5 V and 12 V devices.

CT10 (IRQS Enable)

CT10 enables the IRQS signal on the CompactPCI backplane. See Chapter 4 for more discussion on this option.

CT11 (IRQP Enable)

CT11 enables the IRQP signal on the CompactPCI backplane. See Chapter 4 for more discussion on this option.

CT12-CT16 (Board Revision ID)

These cuttable traces are set at the factory depending on the current board revision and should not be modified.

CT19 (FAL# Monitor Enable)

Allows the power supply FAL# signal to be monitored by the Digital I/O ASIC. See Chapter 11.

CT20 (DEGRADE Monitor Enable)

Allows the power supply DEGRADE- signal to be monitored by the Digital I/O ASIC. See Chapter 11.

CT21 (PBRST- Enable)

Connects the optional CompactPCI backplane reset (PBRST-) to the on-board reset logic. This option allows the CPU to be reset from any device on the CompactPCI backplane.

CT22-CT25 (Bus Master Slot Selection)

These cuttable traces are used to select which CompactPCI slots can be bus masters. The ZT 6500's arbiter only supports five REQ/GNT pairs (bus master slots). These cuttable traces must be configured in pairs with the same options. CT22/CT24 should be configured as one pair and CT23/CT25 should be configured as another pair. The factory default sets slots 3, 4, 5, 6, and 7 as bus master slots and slots 2 and 8 as non-bus master slots. See Chapter 3 for more information.

CT22	CT24	Bus Slot	Master
1-2	1-2	Slot 2	
2-3†	2-3†	Slot 7	

CT23	CT25	Bus Slot	Master
1-2†	1-2†	Slot 3	
2-3	2-3	Slot 8	

† Factory default configuration

APPENDIX B. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 6500. It also includes illustrations of the board dimensions, the connector pinouts, and cables commonly used with the ZT 6500.

ELECTRICAL AND ENVIRONMENTAL

The following topics list electrical and environmental specifications, including absolute maximum ratings, DC operating characteristics, and battery backup characteristics.

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 6500 at these maximums. See the "DC Operating Characteristics" section in this appendix for operating conditions.

- Supply Voltage, Vcc: 0 to 7 V
- Supply Voltage, AUX +: 0 to 12.6 V (required for 4 Mbyte Flash programming and fan/heatsink only; 2 Mbyte Flash operation does not require +12 V)
- Supply Voltage, AUX -: Not used
- Storage Temperature: -40° to +85° Celsius
- Non-Condensing Relative Humidity: <95% at 40° Celsius

Operating Temperature

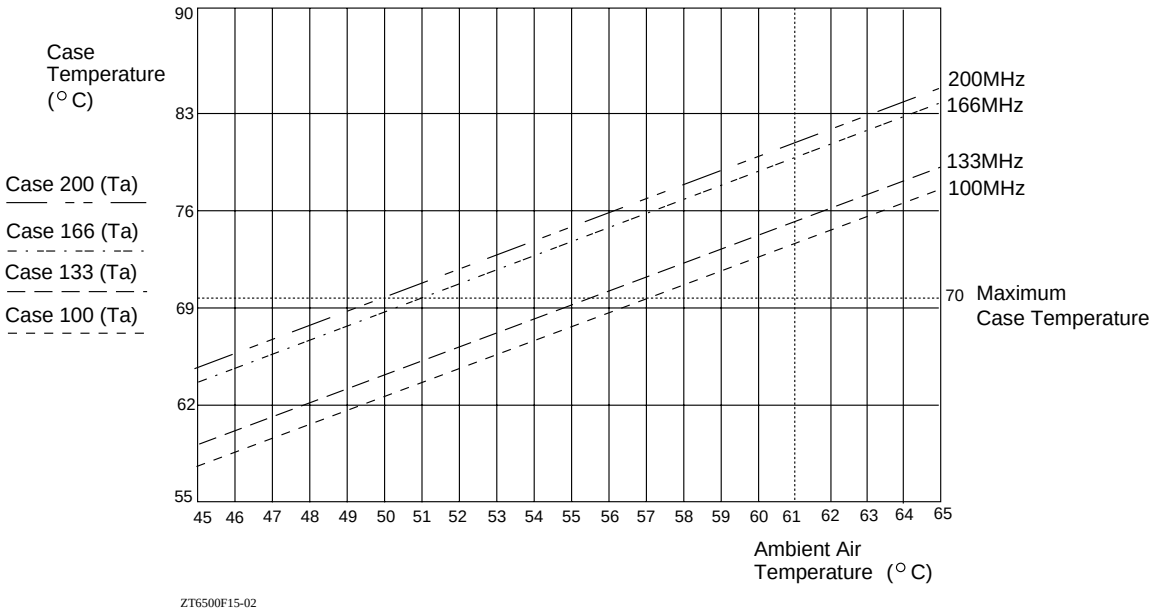
For proper operation of the ZT 6500, the Pentium processor case temperature must remain below 70° Celsius. An integrated fan/heatsink is provided with the processor to help maintain this requirement.

The "Pentium Processor(s) Maximum Ambient Temperature" table below lists the **maximum** ambient temperatures for the various processor options.

Pentium Processors Maximum Ambient Temperatures

Processor Speed (MHz)	Max. Ambient Temperature (°C)
100	57.0
133	55.5
166	51.0
200	50.0

The "Ambient Air Temperature Vs. Pentium Processor Case Temperature" figure below shows the **relationship** between ambient temperature and case temperature (when operated with the integrated fan/heatsink) for the various processor options sold with the ZT 6500.



Ambient Air Temperature Vs. Pentium Processor Case Temperature

DC Operating Characteristics

- Supply Voltage, Vcc: 4.75 to 5.25 V
- Supply Voltage, AUX +: 11.4 to 12.6 V (for 4 Mbyte Flash programming)
- Supply Voltage, AUX -: Not used
- Supply Current, Icc:

  Pentium-100: 1.7 A typ., 2.4 max.

  Pentium-133: 1.9 A typ., 2.6 A max.

  Pentium-166: 2.2 A typ., 3.0 A max.

  Pentium-200: 2.9A typ., 3.7 A max.

  (Numbers assume 8 Mbytes of DRAM and 2 Mbytes of Flash)

  (Each additional 8 Mbytes adds 0.2 A typ., 0.3 A max.)
- Supply Current, AUX + (12 V):

  4 Mbyte Flash Option: 0.010 A typ., 0.015 A max.

  Fan/Heatsink: 120 mA typ., 200 mA max.

DC/DC Voltage Settings

The on-board DC/DC converter supports Intel processors that use STD (standard voltage) or VRE (reduced and shifted voltage). The board is configured from the factory to the correct voltage for the loaded processor.

Processor Voltage	**R1 (Ω)**	**R13 (Ω)**
STD (3.3 V)	0	0
VRE (3.5 V)	470	470

Battery Backup Characteristics

- Battery Voltage: 3 V
- Battery Capacity: 255 mAH

- Real-Time Clock Requirements: 4 µA max. (Vbat = 3 V, Vcc=0 V)
- Real-time clock data retention:

  56250 Hours/ 6.4 years min. (in the absence of power)

  9.6 years min. (with Vcc power applied 8 hours per day)
- Electrochemical Construction: Poly-carbonmonofluoride

MECHANICAL

The following topics list mechanical specifications, including card dimensions and weight, connectors, and cables.

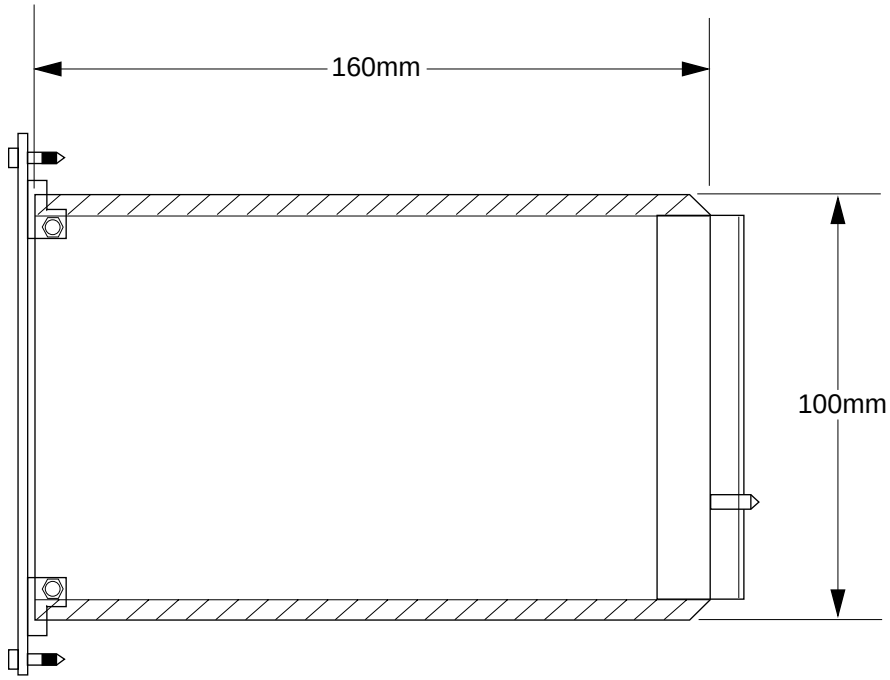
Card Dimensions and Weight

The ZT 6500 meets the CompactPCI Bus Specification for all mechanical parameters. In a CompactPCI cage with 0.8 inch spacing, the ZT 6500 requires two card slots with the integrated fan/heatsink. An additional card slot is required for the optional floppy interface (F1 option).

Mechanical dimensions are shown in the "Board Dimensions" illustration and are outlined below.

- Board Length: 160 mm
- Board Width: 100 mm
- Board Thickness: 0.158 ±0.018 cm (0.062 ±0.007 inches)
- Board Weight: 232.5 grams (8.2 ounces) without heatsink/fan

  246.6 grams (8.7 ounces) with heatsink/fan



Board Dimensions

Connectors

As shown in the "Connector Locations" illustration below, the ZT 6500 includes several connectors for interfacing to various peripherals. The main connector, J1, uses a breakout cable (ZT 90206) to transition from the 80-pin frontplane connector to standard PC compatible connectors.

Connector Assignments

J1 Multi-I/O connector (two RS-232 serial ports, LPT port, keyboard, digital I/O, speaker)

J2 Cache connector, for optional cache module. Contact Ziatech for more information.

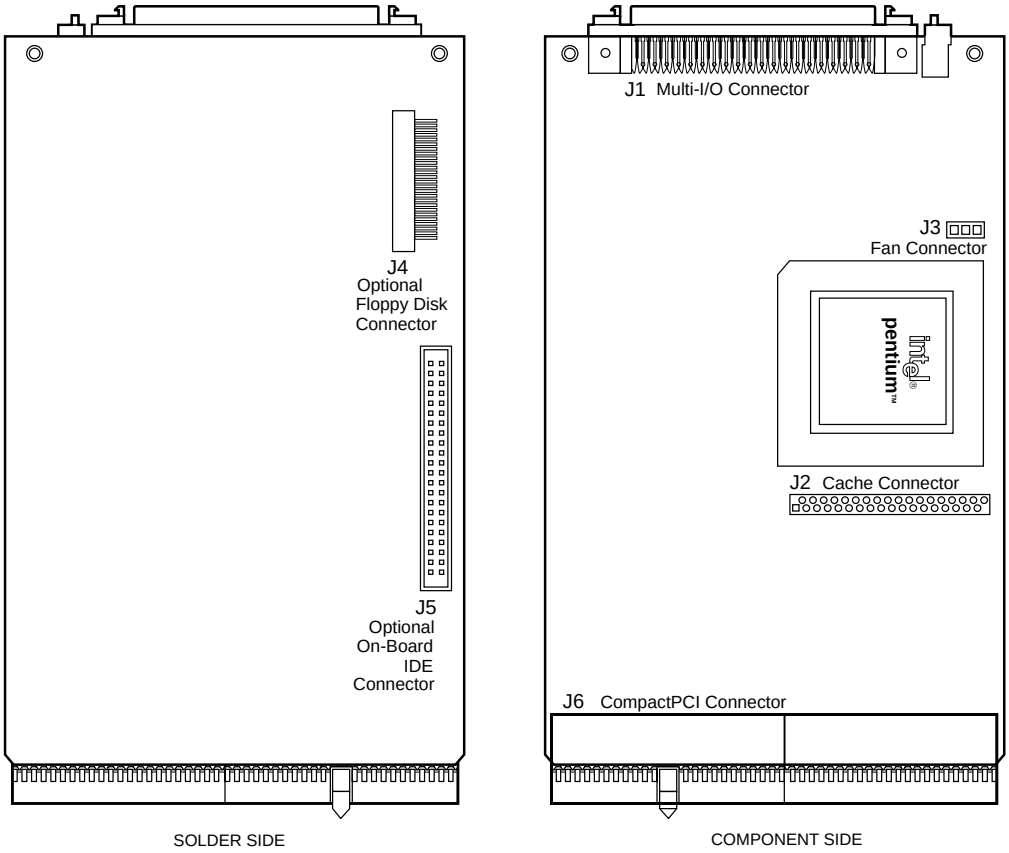
J3 Fan connector for integrated fan/heatsink.

J4 Optional floppy diskette connector.

J5 Optional on-board IDE connector.

J6 CompactPCI connector

Note: See "ZT 6500 Specifics" in the "CompactPCI Pin Definitions" section of Chapter 3 for information about important differences between the *CompactPCI Specification, Rev. 2.1* and the ZT 6500 implementation.



ZT6500FB-02

Connector Locations

J1 (Multi-I/O Connector)

J1 is a multi-I/O connector that provides a high density connection to the following interfaces:

- COM1
- COM2
- Local Keyboard
- LPT1
- Digital I/O
- Speaker

See the "J1 Multi I/O Connector Pinout" table below for pin definitions.

Ziatech offers the ZT 90206 transition cable that breaks out these signals into standard D-SHELL 0.1" connector interfaces. This cable is documented at the end of this appendix.

J1 Multi I/O Connector Pinout

	Description	Type	Signal	Pin #	Pin #	Signal	Type	Description	
COM 1	COM1 DCD	In	DCD	1	41	COM2 DCD	In	DCD	COM 2
	COM1 DSR	In	DSR	2	42	COM2 DSR	In	DSR	
	COM1 RXD	In	RxD	3	43	COM2 RXD	In	RxD	
	COM1 RTS	Out	RTS	4	44	COM2 RTS	Out	RTS	
	COM1 TxD	Out	TxD	5	45	COM2 TxD	Out	TxD	
	COM1 CTS	In	CTS	6	46	COM2 CTS	In	CTS	
	COM1 DTR	Out	DTR	7	47	COM2 DTR	Out	DTR	
	COM1 RINGIN	In	RIN	8	48	COM2 RINGIN	In	RIN	
	Ground	------	GND	9	49	Ground	------	GND	
	+5V (Fused)	------	VCC	10	50	+5V (Fused)	------	VCC	
IEEE 1284 PORT	STB*	Out	Data strobe	11	51	GND	------	Ground	DIGITAL I/O
	AFD*	Out	Autofeed	12	52	DIG0	In/Out	Digital I/O Bit0	
	PD0	In/Out	Data bit 0	13	53	DIG1	In/Out	Digital I/O Bit1	
	ERR*	In	Error	14	54	DIG2	In/Out	Digital I/O Bit2	
	PD1	In/Out	Data bit 1	15	55	DIG3	In/Out	Digital I/O Bit3	
	INIT*	Out	Initialize	16	56	DIG4	In/Out	Digital I/O Bit4	
	PD2	In/Out	Data bit 2	17	57	DIG5	In/Out	Digital I/O Bit5	
	SLIN*	Out	Select to printer	18	58	DIG6	In/Out	Digital I/O Bit6	
	PD3	In/Out	Data bit 3	19	59	DIG7	In/Out	Digital I/O Bit7	
	GND	------	Ground	20	60	VCC	------	+5V (fused)	
	PD4	In/Out	Data bit 4	21	61	DIG8	In/Out	Digital I/O Bit8	
	GND	------	Ground	22	62	DIG9	In/Out	Digital I/O Bit9	
	PD5	In/Out	Data bit 5	23	63	DIG10	In/Out	Digital I/O Bit10	
	GND	------	Ground	24	64	DIG11	In/Out	Digital I/O Bit11	
	PD6	In/Out	Data bit 6	25	65	DIG12	In/Out	Digital I/O Bit12	
	GND	------	Ground	26	66	DIG13	In/Out	Digital I/O Bit13	
	PD7	In/Out	Data bit 7	27	67	DIG14	In/Out	Digital I/O Bit14	
	GND	------	Ground	28	68	DIG15	In/Out	Digital I/O Bit15	
	ACK*	In	Acknowledge	29	69	GND	------	Ground	
	GND	------	Ground	30	70	DIG16	In/Out	Digital I/O Bit16	
	BUSY	In	Printer busy	31	71	DIG17	In/Out	Digital I/O Bit17	
	GND	------	Ground	32	72	DIG18	In/Out	Digital I/O Bit18	
	PE	In	Paper error	33	73	DIG19	In/Out	Digital I/O Bit19	
	GND	------	Ground	34	74	DIG20	In/Out	Digital I/O Bit20	
	SLCT	In	Select from printer	35	75	DIG21	In/Out	Digital I/O Bit21	
					76	DIG22	In/Out	Digital I/O Bit22	
					77	DIG23	In/Out	Digital I/O Bit23	
					78	VCC	------	+5V (fused)	
KEY	+5V (Fused)	------	VCC	36					
	Keyboard Clock	In/Out	KCLK	37					
	Ground	------	GND	38					
	Keyboard Data	In/Out	KDAT	39					
					79	FPSPK	Out	Speaker control	SPK
-	Pin 40	In	RSVD	40	80	VCC	------	+5V (Fused)	

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J2 (Cache Connector)

J2 is a 36-pin location for an optional L2 cache module. Contact Ziatech for availability.

J3 (Fan Connector)

J3 is a 3-pin vertical male header with 0.1 inch contact spacing for supplying power to the fan/heatsink. +12 V is used to power the fan. Pin 2 is an optional Tachometer input from fans so equipped.

The factory supplied fan/heatsink has its leads soldered directly to the board. However, a connector can be used in this location if desired. The following connectors are recommended:

- MOLEX 39-27-0031 (3-pin polar male—solder to board)
- MOLEX 39-01-0033 (3-pin polar female—for fan signals)

See the "J3 Fan Connector Pinout" table below for pin definitions.

J3 Fan Connector Pinout

Pin #	Signal	Type	Description
1	+12V	Power	+12V For fan
2	TACH IN	In	Tach Input (Option)
3	GND	Ground	Ground

J4 (Floppy Disk Connector)

J4 is a surface mount connector location for the optional floppy disk controller interface. This interface is provided for development systems and can be ordered as option F1. See the "J4 Floppy Disk Connector Pinout" table for pin definitions.

J4 Floppy Interface Connector Pinout

Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
1	VCC	——	+5V	14	STEP*	Out	Step
2	INDEX*	In	Index	15	GND	——	GND
3	VCC	——	+5V	16	WDATA*	Out	Write Data
4	DRSEL0*	Out	Drive Select 0	17	GND	——	GND
5	VCC	——	+5V	18	WGATE*	Out	Write Gate
6	DSKCHG*	In	Disk Change	19	GND	——	GND
7	DRSEL1*	Out	Drive Select 1	20	TRK0*	In	Track 0
8	READY*	n/c	Ready	21	GND	——	GND
9	DENSTAT	In	Density Status (Media Sense)	22	WP*	In	Write Protect
10	MOTON*	Out	Motor Enable	23	GND	——	GND
11	DENSEL	Out	Density Select	24	RDATA*	In	Read Data
12	DIR*	Out	Direction	25	GND	——	GND
13	GND	——	GND	26	HDSEL*	Out	Head Select

For more information on specific signals, see the National PC87303 data sheet.

J5 (On-Board IDE Hard Disk Connector)

J5 is a 44-pin surface mount connector location to provide a local Integrated Drive Electronics (IDE) hard disk interface. The ZT 6500 can have, as a special option, a local IDE drive. This option is useful for single board computer operation (no backplane). See the "J5 On-Board IDE Hard Disk Connector Pinout" table below for pin definitions.

J5 On-Board IDE Hard Disk Connector Pinout

Pin #	Signal	Type	Description	Pin #	Signal	Type	Description
1	RESET*	Out	Reset	23	IOWR*	Out	I/O Write Strobe
2	GND	——	Ground	24	GND	——	Ground
3	D7	In/Out	Data Bit 7	25	IORD*	Out	I/O Read Strobe
4	D8	In/Out	Data Bit 8	26	GND	——	Ground
5	D6	In/Out	Data Bit 6	27	RSVD	——	Reserved (IORDY)
6	D9	In/Out	Data Bit 9	28	ALE	Out	Address Latch En.
7	D5	In/Out	Data Bit 5	29	RSVD	——	Reserved
8	D10	In/Out	Data Bit 10	30	GND	——	Ground
9	D4	In/Out	Data Bit 4	31	IRQ	In	Interrupt Request
10	D11	In/Out	Data Bit 11	32	IOCS16*	In	16-bit I/O handshake
11	D3	In/Out	Data Bit 3	33	A1	Out	Address Bit 1
12	D12	In/Out	Data Bit 12	34	PDIAG	——	Inter-drive diagnostics
13	D2	In/Out	Data Bit 2	35	A0	Out	Address Bit 0
14	D13	In/Out	Data Bit 13	36	A2	Out	Address Bit 2
15	D1	In/Out	Data Bit 1	37	CS0*	Out	Chip Select (1F0h-1FFh)
16	D14	In/Out	Data Bit 14	38	CS1*	Out	Chip Select (3F6h)
17	D0	In/Out	Data Bit 0	39	ACT*	In	Active/Slave present
18	D15	In/Out	Data Bit 15	40	GND	——	Ground
19	GND	——		41	VCC	——	+5V - Drive Logic
20	KEY	——	Cable Key	42	VCC	——	+5V - Drive Motor
21	RSVD	——	Reserved	43	GND	——	Ground
22	GND	——	Ground	44	XT/AT	Out	Drive Mode = AT

J6 (CompactPCI Connector)

J6 consists of two connectors: one with a key area, and the other without a key area. Each connector is a 110-pin 2mm x 2mm right-angle female CompactPCI connector.

For pin definitions, see the two "J6 CompactPCI Connector Pinouts" (**"keyed"**and **"non-keyed")** below. The pinouts are followed by the "CompactPCI Connector Pin Locations" figure showing pin placement.

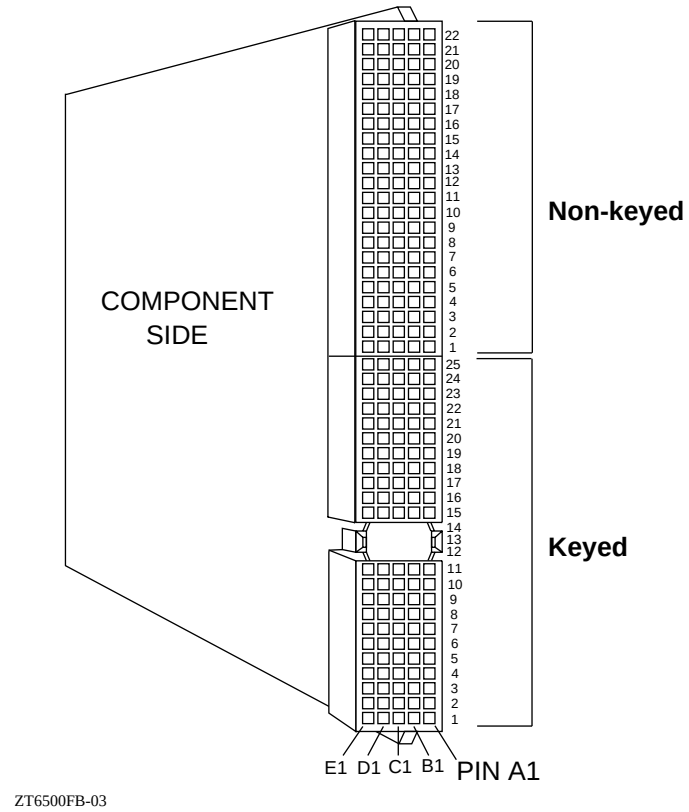
Note: See "ZT 6500 Specifics" in the "CompactPCI Pin Definitions" section of Chapter 3 for information about important differences between the *CompactPCI Specification, Rev. 2.1* and the ZT 6500 implementation.

J6 CompactPCI Connector Pinout: Keyed

Pin#	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	BRSV	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)(2)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN(5)	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)(2)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)(2),(6)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14							
13				KEY AREA			
12							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5(12)	BRSVP1B5(12)	RST#	GND	GNT#	GND
4	GND	BRSVP1A4(12)	GND	V(I/O)	NC	NC	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND
Pin#	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

J6 CompactPCI Connector Pinout: Non-keyed

Pin#	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	NC	NC	NC	NC	GND
20	GND	NC	NC	NC	NC	NC	GND
19	GND	NC	NC	NC	NC	NC	GND
18	GND	NC	NC	NC	NC	NC	GND
17	GND	NC	GND	PRST#	REQ#6	GNT6#	GND
16	GND	NC	NC	DEG#	GND	NC	GND
15	GND	NC	GND	FAL#	REQ#5	GNT5#	GND
14	GND	NC	NC	NC	NC	NC	GND
13	GND	NC	NC	NC	NC	NC	GND
12	GND	NC	NC	NC	NC	NC	GND
11	GND	NC	NC	NC	NC	NC	GND
10	GND	NC	NC	NC	NC	NC	GND
9	GND	NC	NC	NC	NC	NC	GND
8	GND	NC	NC	NC	NC	NC	GND
7	GND	NC	NC	NC	NC	NC	GND
6	GND	NC	NC	NC	NC	NC	GND
5	GND	NC	NC	NC	NC	NC	GND
4	GND	NC	NC	NC	NC	NC	GND
3	GND	CLK4	GND	GNT3#	REQ#4	GNT4#	GND
2	GND	CLK2	CLK3	GND	GNT2#	REQ#3	GND
1	GND	CLK1	GND	REQ#1	GNT1#	REQ#2	GND
Pin#	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

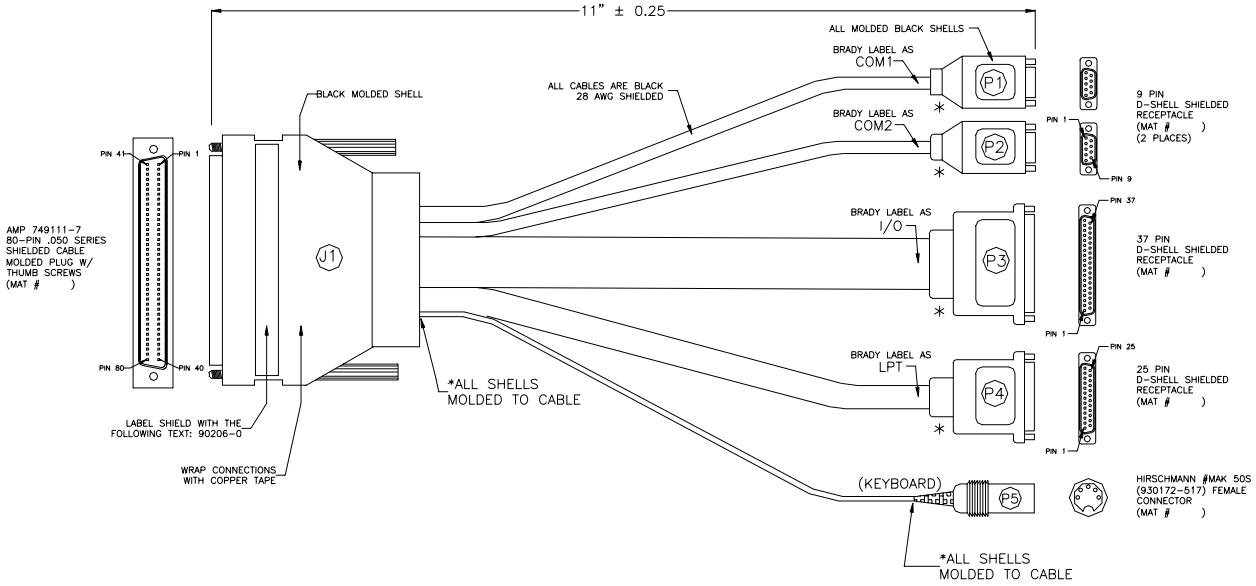


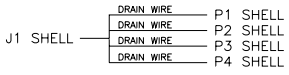
CompactPCI Connector Pin Locations

Cables

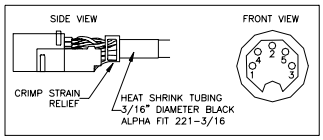
The following cable is available from Ziatech Corporation. A drawing is included here as reference for those who wish to make their own cables:

ZT 90206 Multi-I/O cable (supports keyboard, COM1, COM2, LPT1, and Digital I/O)





KEYBOARD CONNECTOR DETAIL



J1 - P1 (COM1)	J1 - P4 (LPT)		J1 - P5 (KYBRD)	J1 - P2 (COM2)	J1 - P3 (DIG I/O)	
1 - 1	11 - 1	24 - 20	36 - 5	41 - 1	51 - 1	66 - 16
2 - 6	12 - 14	25 - 8	37 - 1	42 - 6	52 - 2	67 - 17
3 - 2	13 - 2	26 - 21	38 - 4, SHIELD	43 - 2	53 - 3	68 - 18
4 - 7	14 - 15	27 - 9	39 - 2	44 - 7	54 - 4	69 - 19
5 - 3	15 - 3	28 - 22	40 - NC	45 - 3	55 - 5	70 - 20
6 - 8	16 - 16	29 - 10	NC - 3	46 - 8	56 - 6	71 - 21
7 - 4	17 - 4	30 - 23		47 - 4	57 - 7	72 - 22
8 - 9	18 - 17	31 - 11		48 - 9	58 - 8	73 - 23
9 - 5	19 - 5	32 - 24		49 - 5	59 - 9	74 - 24
10 - NC(+5)	20 - 18	33 - 12		50 - NC(+5)	60 - 10	75 - 25
	21 - 6	34 - 25			61 - 11	76 - 26
	22 - 19	35 - 13			62 - 12	77 - 27
	23 - 7				63 - 13	78 - 28
					64 - 14	79 - 29
					65 - 15	80 - 30
					31-37 NC	

ZT 90206 Rev. 0 Multi-I/O Cable

APPENDIX C. PIA SYSTEM SETUP CONSIDERATIONS

The 16C50A Parallel Interface Adapter (PIA) device used on the ZT 6500 is designed by Ziatech to offer bidirectional I/O signals with or without event sense capability. This device features low power, high speed, wide temperature operation achievable only by utilizing CMOS technology.

Although CMOS technology offers many advantages, you must observe a few cautions when interfacing to any CMOS parts.

CMOS inputs and outputs can exhibit latchup characteristics. These inherent characteristics of any CMOS technology can result in the formation of a Silicon-Controlled Rectifier (SCR) that appears between Vcc and ground when voltages greater than Vcc or less than ground are applied to inputs or outputs. When this happens, Vcc is effectively shorted to ground. The only way to remove the latchup condition is to shut off the power supply. If a large current is allowed to flow through the chip, its operating temperature may increase, it may exhibit intermittent operation, or it may be damaged.

CMOS inputs must be protected from slow rising signals and inductive coupling on their inputs. Failure to do so will allow a potentially large current to flow through the chip, damaging the chip.

The purpose of this appendix is to illustrate precautions you should take to prevent latchup conditions and protect inputs.

PREVENTING SYSTEM LATCHUP

The most common causes of latchup are:

- Input signals applied before the input circuitry is powered, resulting in a signal to power supply sequence mismatch
- Input signals greater than Vcc or less than ground, resulting in a signal level mismatch

Each of these conditions is covered in the following topics.

Power Supply Sequence Mismatch

A common application is to interface to a 24-position ZT 2226, Opto 22, or equivalent I/O module rack. Vcc and ground are provided from the ZT 6500 through connector J1 with Vcc protected by a 1 A fuse. In this application (illustrated in Figure 1 on the following page), no power supply sequence mismatch exists because the power supplying the input circuitry within the PIA is applied before or at the same time as the power supplying the external signals. Proper system operation will result.

However, if a power source other than that supplying the PIA is used to power the external signals, then a power sequence mismatch could occur, resulting in a latchup

condition. An external power source might be required if the external circuitry requires more than the 1 A supplied by the cable or if a custom interface is being designed (see Figure 2 on the following page for an example).

One solution is to switch the external signals' power supply with an output that is controlled by the computer. In this manner, if the computer is off, so is the external power supply. This solution is illustrated in Figure 3 on the following page.

A simpler solution is to power the relay controlling the external power supply directly from Vcc and ground supplied by the interface cable.

Another solution is to utilize the same switch to control the computer's power supply and the external signals' power supply, as illustrated in Figure 4 on the following page. This is an acceptable solution for power supply sequence mismatches as long as the computer supply ramps up faster than the external power supply. This ensures the PIA input circuitry is powered before the external signal circuitry.

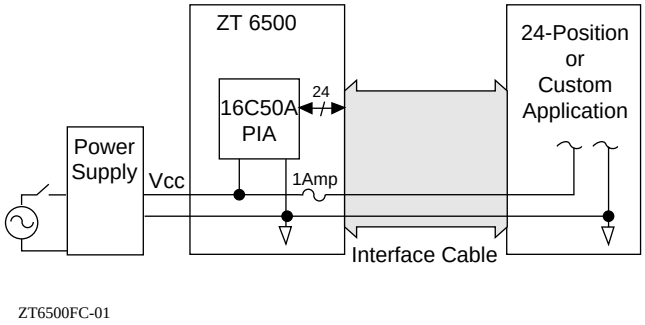


Figure 1. I/O Rack Vcc and Ground Supplied Via Interface Cable

Correct Power Supply Sequence, Signal Level Matched

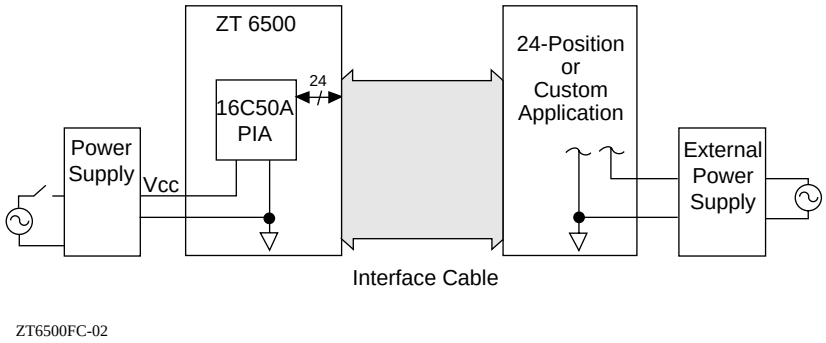


Figure 2. I/O Rack Vcc and Ground Supplied Externally

Potential Power Supply Sequence Mismatch, Signal Level Mismatch

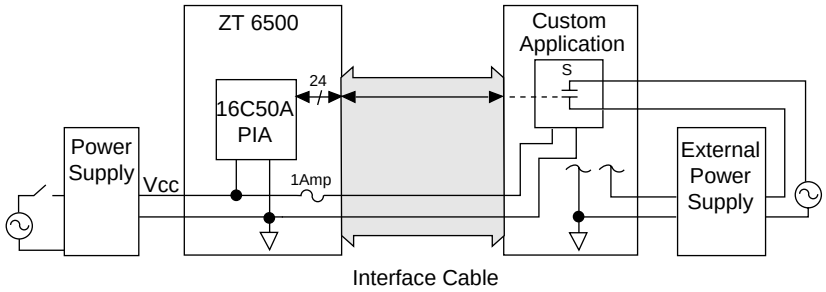


Figure 3. Computer-Switched External Power Supply

Correct Power Supply Sequence, Potential Signal Level Mismatch

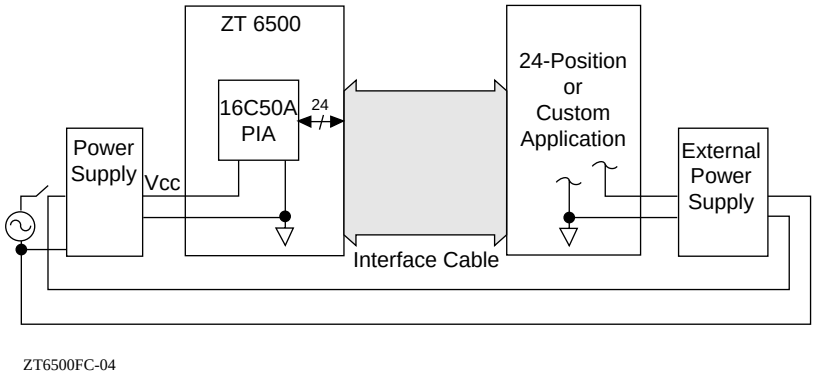


Figure 4. Computer & Ext. Power Supply w/ Common Switch

Correct Power Supply Sequence, Potential Signal Level Mismatch

Signal Level Mismatch

Power supplying the external signal in Figure 1 (see previous page) is always relative to the PIA input circuitry power because power is provided over the interface cable. Signal level mismatches will not occur and proper system operation will result. However, if separate power supplies are used, there are two predominant causes of signal level mismatches.

The first (assuming no sequencing problems) occurs when the two supplies are not referenced to each other, as illustrated in Figures 2, 3, and 4. This results in signals that may be higher than Vcc or lower than ground, potentially causing SCR latchup. All that is generally needed is to reference one supply to the other, typically by connecting a common ground. The most convenient way of connecting a common ground is to use the interface cable. Figures 5, 6, and 7 below illustrate correct ground connections.

The second cause of mismatch occurs when the two power supplies are referenced to each other but the Vcc difference between the two power supplies exceeds 0.5 V. This results in signals that could be greater than Vcc, causing SCR latchup. This is easily remedied by adjusting the external power supply voltage to be within 0.5 V of the computer power supply voltage.

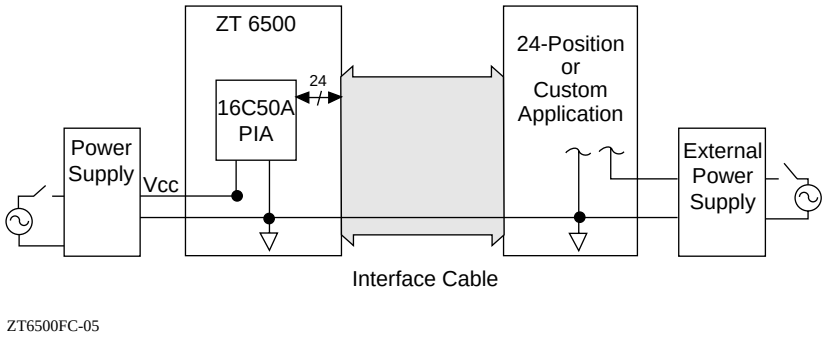


Figure 5. I/O Rack Vcc Supplied Externally, Common Ground

Potential Power Supply Seq. Mismatch, Correct Signal Level Match

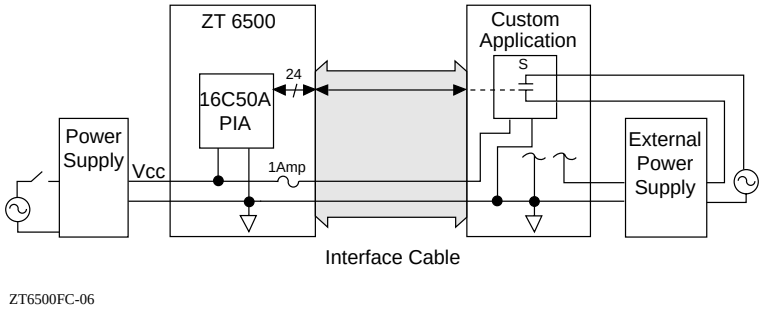


Figure 6. Computer-Switched External PS, Common Ground

Correct Power Supply Sequence, Correct Signal Level Match

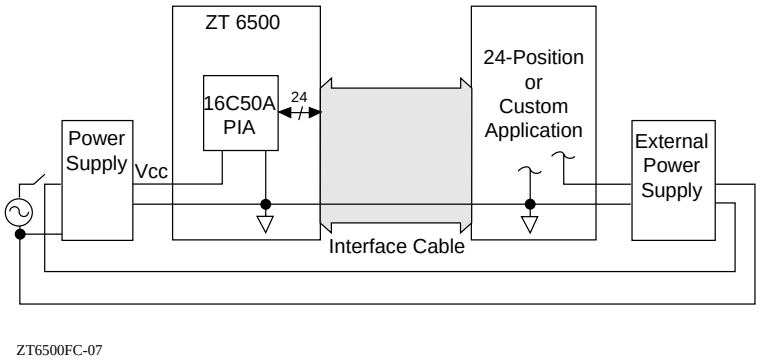


Figure 7. Computer & External PS w/ Common Switch & Ground

Correct Power Supply Sequence, Correct Signal Level Match

PROTECTING CMOS INPUTS

The most common causes of damaged inputs are:

- Slow rise times, resulting in a ground bounce within the chip
- Inductive coupling on I/O lines causing noise to be coupled into the chip, resulting in intermittent operation

Each of these conditions is covered in the following topics.

Rise Times

Slow rise times on a CMOS input can easily cause the transistor to bounce between Vil and Vih. When this oscillation occurs, the operating current goes up, resulting in "ground bounce." Ground bounce can cause internal latchup or can cause other system components to malfunction. A pullup termination resistor is used to increase the rise time.

Input rise times must be kept to less than 50 ns. Given a maximum chip capacitance of 10 pF, a 5k Ω resistor is the largest that could be used without additional cabling. As cabling is added, the capacitance goes up, resulting in the use of a smaller pullup resistor until the maximum sink current of the output is achieved.

If the 16C50A PIA device is driving the output, its maximum sink current at a Vol of .4 V is 12 mA. This gives a lower limit of 420 ohms for the pullup resistor, allowing a maximum cabling capacitance of 110 pF. Note that while the input feature of the PIA may not be used by your application (PIA used as an output only), the input circuitry remains in parallel; therefore, the output rise time is still a critical parameter that the input still sees. The output rise time must not exceed 50 ns.

Be wary of using low pass filters to remove electrical noise. The resulting capacitance is typically too large to meet the 50 ns rise time requirement.

Typically, optical isolators are used to help remove electrical noise while providing for different grounds. Separate grounds are achieved through the use of an additional power supply for the optocoupler rather than using the computer's power supply. If the computer's power supply powers the optocouplers, electrical isolation is defeated. An example of one such circuit is illustrated in Figure 8 below. The circuit can be altered to allow for design considerations.

Assuming a Vil of 1 V maximum for the 16C50A PIA, the HP Dual Optocoupler must have a Vol of less than or equal to 1 V over the operating temperature. Using a TTL-compatible optocoupler gives a Vol of .6 V maximum with rise and fall times (50 ns and 10 ns, respectively) that are easily compatible with the PIA, given a 1k ohm pullup.

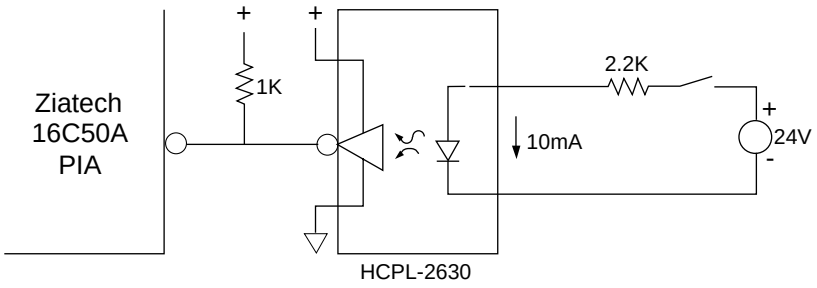


Figure 8. PIA-to-Optocoupler Interface Example

Inductive Coupling

Inductive coupling on I/O lines can cause noise to be coupled into the chip, resulting in intermittent operation. This situation occurs when the PIA I/O signals are routed with other signals within a wire bundle. One way to filter inductively coupled noise, or any noise for that matter, within a system with the same ground (not using optocouplers) is illustrated in Figure 9 on the following page.

In the above circuit, the Texas Instruments 74S1053 Schottky diode clamps limit a transient to ±1 V above +5 V or below ground. The ferrite bead has a 50 ohm impedance at the frequency of interest. As the diodes begin to clamp and current flows through them, the voltage across the LCA05 5 V bidirectional TransZorbs® increases, causing them to conduct and allowing the majority of energy to flow through them instead of through the diode clamps. The 39 pF capacitor, in conjunction with the ferrite bead, forms an additional low pass filter, and is entirely optional. The 1k ohm pullup ensures adequate rise time on the signal. The fuse acts as additional insurance against catastrophic events that might destroy the TransZorb and diode clamps.

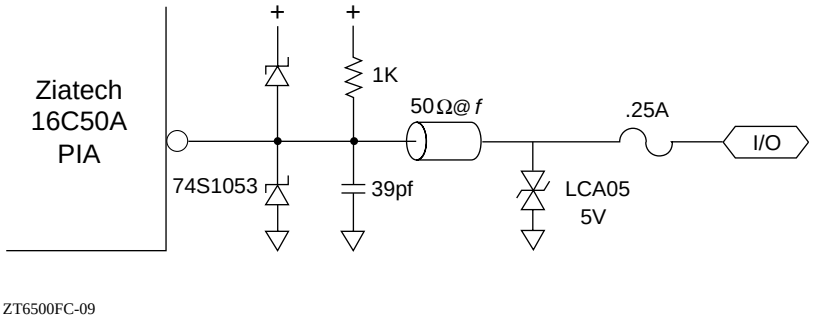


Figure 9. PIA-to-Filter Interface Example

ADDITIONAL INFORMATION

You can find additional design information in the *Advanced CMOS Logic Designer's Handbook,* published by Texas Instruments.

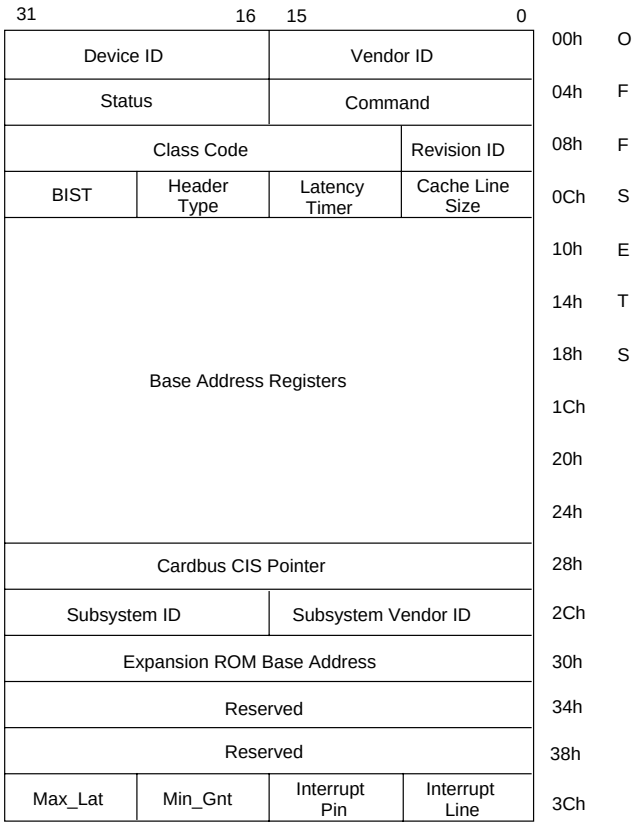
APPENDIX D. PCI CONFIGURATION SPACE MAP

All PCI compliant devices contain a PCI configuration header. The generic layout of the header is shown in the "PCI Configuration Header" diagram below.

Additionally, a device may contain unique configuration registers (at location > 40h). For the ZT 6500, these are shown in the "ZT 6500 On-Board Device PCI Bus Mapping" table below. Details for each device's configuration space can be found in the respective manufacturer's data manuals. For more information on the PCI chipset implemented on the ZT 6500, refer to the *Aladdin™ M1461/M1449 3.3-Volt Pentium Chip Set Preliminary Data Sheet, Rev. D*, or contact **ALI® Pacific Technology Group** at (408) 764-0644.

ZT 6500 On-Board Device PCI Bus Mapping

Bus # (hex)	Dev # (hex)	Fcn # (hex)	Vendor ID	Device ID	Description
00	00	00	10B9	1461	Aladdin M1461 Memory Controller
00	01	00	10B9	1449	Aladdin M1449 PCI-to-ISA Bridge



PCI Configuration Header

APPENDIX E. CUSTOMER SUPPORT

This appendix offers technical assistance information for this product, and also the necessary information should you need to return a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_Support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information is available at Ziatech's website, located at http://www.ziatech.com.

Corporate Headquarters

1050 Southwood Drive

San Luis Obispo, CA 93401 USA

Tel (805) 541-0488

FAX (805) 541-5088

REVISION HISTORY

Revision 0 - 2/17/96

Revision 0 is the first production release of the board.

Revision 0.1 - 7/26/96

There are no functional changes between Revision 0 and Revision 0.1. Modifications made to the Revision 0.1 product include:

Cache connector is loaded on standard product.

Revision 0.2 - 6/11/97

There are no functional changes between Revision 0.1 and Revision 0.2. Modifications made to the Revision 0.2 product include:

1. Changed DC/DC trim resistor values (562 Ω to 470 Ω) for VRE voltage settings.

2. Corrected a problem involving digital I/O corruption during floppy DMA writes.

RELIABILITY

Ziatech has taken extra care in the design of the ZT 6500 in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each ZT 6500 has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Returned Material Authorization (RMA) number. The following information is needed to expedite the shipment of a replacement to you:

1. Your company name and address for invoice
2. Shipping address and phone number
3. Product I.D. number
4. If possible, the name of a technically qualified individual at your company familiar with the mode of failure on the board

If the unit is out of warranty, service is available at a predesignated service charge. Contact Ziatech for pricing and please supply a purchase order number for invoicing the repair.

Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it. ***Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!*** Mark the RMA number clearly on the outside of the box before returning.

ZIATECH WARRANTY

Ziatech provides a five-year limited warranty to its customers with a special extended warranty option. Ziatech also has an explicit policy regarding the use of Ziatech products in life support systems. These topics are covered in the following sections.

Five-Year Limited Warranty

Products manufactured by Ziatech Corporation are covered from the date of purchase by a five-year warranty against defects in materials, workmanship, and published specifications applicable to the date of manufacture. During the warranty period, Ziatech will repair or replace, solely at its option, defective units provided they are

returned at customer expense to an authorized Ziatech repair facility. Products which have been subjected to misuse, abuse, neglect, alteration, or unauthorized repair, determined at the sole discretion of Ziatech, whether by accident or otherwise, are excluded from warranty. The warranty on fans and disk drives is limited to two years and the warranty on flat panel displays is limited to nine months from date of purchase. Other products and accessories not manufactured by Ziatech are limited to the warranty provided by the original manufacturer. Consumable items (fuses, batteries, etc.) and software are not covered by this warranty.

Ziatech Corporation warrants that for a period of ninety (90) days from the date of purchase; the media on which software is furnished will be free of defects in materials and workmanship under normal use; and the software contains the features described in the Ziatech price list. Otherwise, the software is provided "AS IS". This limited warranty extends only to Customer as the original licensee. Customer's exclusive remedy and Ziatech's entire liability under this limited warranty will be, at Ziatech's option, to repair or replace the software, or refund the license fee paid therefore.

Ziatech may offer, where applicable and available, replacement products; otherwise, repairs requiring components, assemblies, and other purchased materials may be limited by market availability.

Ziatech assumes no liability resulting from changes to government regulations affecting use of materials, equipment, safety, and methods of repair. Ziatech may, at its discretion, offer replacement products.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY FOR FITNESS OF PURPOSE, MERCHANTABILITY, OR FREEDOM FROM INFRINGEMENT OR THE LIKE, AND ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATIONS, OR SAMPLE.

Ziatech neither assumes nor authorizes any person to assume for it any other liability. The liability of Ziatech under this warranty agreement is limited to a refund of the purchase price. In no event shall Ziatech be liable for loss of profits, use, incidental, consequential, or other damage, under this agreement.

Life Support Policy

Ziatech products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Ziatech Corporation. As used herein:

1. Life support devices or systems are devices or systems which support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, affect its safety, or limit its effectiveness.

TRADEMARKS

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OS/2 and PC/AT are registered trademarks of International Business Machines, Inc.

QNX is a registered trademark of Quantum Software Systems Ltd.

UNIX is a registered trademark of AT&T Bell Laboratories.

VRTX32 is a registered trademark of Ready Systems, Inc.

Windows and Windows NT are trademarks and MS-DOS is a registered trademark of Microsoft Corporation.

APPENDIX F. AGENCY APPROVALS

This appendix presents agency approval and certification information for the ZT 6500 Single Board Computer with Pentium processor.

CE CERTIFICATION

This product was tested as a component in the following system:

†
- ZT 6200-08WF0-B 3U CompactPCI 8-slot card cage
- ZT 6500 3U Single Board Computer with Pentium processor
- ZT 6650-A.2 3U CompactPCI Fast Ethernet Interface
- ZT 6631 3U CompactPCI Super VGA Interface
- ZT 6640 3U CompactPCI Enhanced IDE Controller
- ZT 90206-0 Multi I/O Cable

† Please note that the enclosure used was the ZT 6200-08WF0, Revision B, which is unplated.

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