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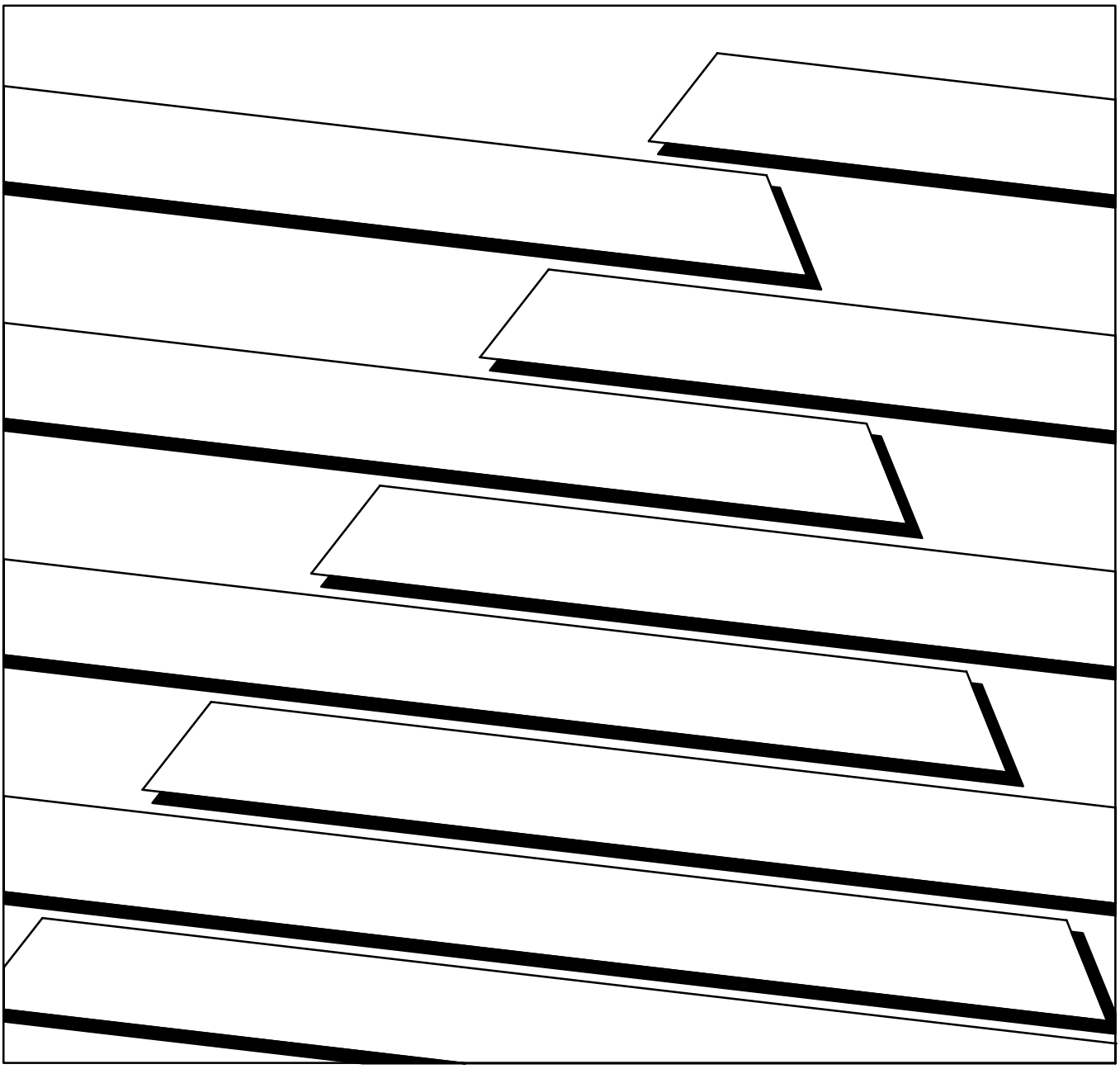
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Mini-PLC-2/02, -2/16, -2/17 Processor (cat. no. 1772-LZ, -LZP, -LX, -LXP, -LW, -LWP)

User Manual



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Important User Information

Because of the variety of uses for this product and because of the differences between solid state products and electromechanical products, those responsible for applying and using this product must satisfy themselves as to the acceptability of each application and use of this product. For more information, refer to publication SGI-1.1 (Safety Guidelines For The Application, Installation and Maintenance of Solid State Control).

The illustrations, charts, and layout examples shown in this manual are intended solely to illustrate the text of this manual. Because of the many variables and requirements associated with any particular installation, Allen-Bradley Company cannot assume responsibility or liability for actual use based upon the illustrative uses and applications.

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Throughout this manual we make notes to alert you to possible injury to people or damage to equipment under specific circumstances.



ATTENTION: Identifies information about practices or circumstances that can lead to personal injury or death, property damage or economic loss.

Attention helps you:

- Identify a hazard
- Avoid the hazard
- recognize the consequences

Important: Identifies information that is critical for successful application and understanding of the product.

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Summary of Changes

Summary of Changes

This release of the publication contains updated information:

For this updated information:	See:
revised conventions	chapter 1
clarified ATTENTION statement about using 1770-XZ batteries	chapter 3
revised illustrations showing the new chassis (1771-A1B, -A2B, -A3B, -A3B1, and -A4B)	chapter 3 chapter 4 chapter 5 chapter 10
minor corrections to the structure for 2-slot addressing	chapter 7 appendix E
added information about adding Branch Start and Branch End instructions while programming on line	chapter 9
corrected last counter address information for counter instructions	chapter 11
minor corrections to Limit Test examples	chapter 12
added more information about output alarms and output limits	chapter 16
minor correction to FIFO ladder diagram examples	chapter 15 appendix E
added warning about using Jump instructions; corrections to programming examples	chapter 17
corrections to programming examples	chapter 18
added warning about using selectable timed interrupt routines	chapter 22
minor revisions to programming examples	chapter 25
clarified the Important statement about illegal opcodes	chapter 26
new format	all chapters and appendices

To help you find new information in this publication, we have included change bars as shows to the left of this paragraph.

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Chapter 1

Using This Manual

Chapter Objectives

Read this chapter before you use your processor.

Important: This manual is for the series D Mini-PLC-2/02, Mini-PLC-2/16 and Mini-PLC-2/17 processors. See the Series Changes on page 3-2 for the differences with other processor series.

Differences

This manual describes the Mini-PLC-2/02, Mini-PLC-2/16 and Mini-PLC-2/17 processors. Unless stated otherwise, assume the features or instructions are common to all the processors.

Feature	Mini-PLC-2/02	Mini-PLC-2/16	Mini-PLC-2/17
Size of memory (words)	2K	4K	7.75K
Size of EEPROM backup (words)	4K	4K	8K
Data table expansion (words)	1920	3968	7808
EAF instructions (up to 12 digits)	Add Subtract Multiply Divide	Add Subtract Multiply Divide	Add Subtract Multiply Divide
EAF instructions	Square Root BCD to Binary Binary to BCD FIFO Load FIFO Unload Log_{10} Sin X Cos X 10^x	Square Root BCD to Binary Binary to BCD FIFO Load FIFO Unload Log_{10} Sin X Cos X 10^x	Square Root BCD to Binary Binary to BCD FIFO Load FIFO Unload Log_{10} Sin X Cos X 10^x
Additional EAF instructions	none	none	Log_e $y^{+/-x}$ $e^{+/-x}$ Reciprocal of x Averaging Standard Deviation PID Wall Clock/Calendar

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What's this User Manual Contains

This manual is divided into eight sections (Table 1.A):

Table 1.A
Sections of the Mini-PLC-2/02, Mini-PLC-2/16, and Mini-PLC-2/17 Processor User Manual

Information Sections	What's Covered	In Chapters
Overview	how to use this manual; fundamentals of programmable controllers	1-2
Hardware	the processor's hardware features; how to assemble, install, start, maintain, and troubleshoot the processor	3
Basic instruction set	how to use basic instructions common to all PLC-2 family processors	4-13
Advanced instruction set	how to use advanced instructions unique to some the processors	14-22
Programming procedures and troubleshooting	how to use special programming techniques and follow a troubleshooting guide so you can minimize production down time	23-26
Specifications, comparison chart, number systems, and glossary	specifications; PLC-2 family comparison chart; explanation of number systems; and list of processor terms used in this manual	Appendices A-D
Quick reference	selected tables in this manual	Appendix E

This manual is procedure oriented. It tells you how to program and operate your Mini-PLC-2/02, Mini-PLC-2/16, and Mini-PLC-2/17 processor. If you need to learn more about these processors, contact your local Allen-Bradley representative or distributor.

Vocabulary

To make this manual easier to read and understand, we refer to the:

We Refer to the:	As the:
Mini-PLC-2/02, Mini-PLC-2/16, and Mini-PLC-2/17 Processors	processors
Electrically Erasable Programmable Read Only Memory	EEPROM
Programmable Read Only Memory	PROM
Execute Auxiliary Function	EAF
Complementary Metal Oxide Semi-conductor Random Access Memory	CMOS RAM
Industrial Terminal (cat. no. 1770-T3)	1770-T3 terminal

A glossary at the back of this manual clarifies technical terms.

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Conventions

A word equals 16 bits; a byte equals 8 bits (1/2 of a word).

Words in [ ] denote a key name or symbol. Words in < > denote information that you must provide - for example, an address value.

All word addresses are displayed in the octal numbering system. Therefore, references to base 8 are not displayed.

Word values are displayed in:

- decimal (0-9) for timers, counters, and mathematics



- hexadecimal values (0-9, A-F) for Get and Put instructions

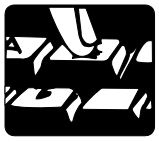
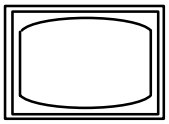


Important: Numbers 0-9 are displayed the same in decimal and hexadecimal.

- octal byte values for examine on and output energize instructions



Keystroke directions are divided into two columns:

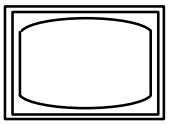
-  tells you what key or keys to press
-  tells you the processor's action

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Figure 1.1 shows the keystrokes to produce a display.

Figure 1.1
Illustration Showing Keystroke Conventions





Start by positioning your cursor on the words SEQUENCER INPUT. Use the arrow keys to move the cursor.

DISPLAY

The word display appears in the lower left hand corner of the screen.

0

```
                    BINARY DATA MONITOR
                    SEQUENCER OUTPUT

COUNTER ADDR:  200          STEP:  001          SEQUENCER LENGTH:  006
                            FILE:  400- 413

OUTPUT ADDR:  110                       201
DATA:  00000000 00000000    00000000 00000000

MASK ADDR:  070                         071
DATA:  00000000 00000000    00000000 00000000

STEP        WORD 1          WORD 2
001  00000000 00000000  00000000 00000000
002  00000000 00000000  00000000 00000000
003  00000000 00000000  00000000 00000000
004  00000000 00000000  00000000 00000000
005  00000000 00000000  00000000 00000000
006  00000000 00000000  00000000 00000000

DATA:  00000000 00000000
```

Related Publications

The publication index, publication SD 499, lists all available publications to further inform you about products related to the Mini-PLC-2/02, Mini-PLC-2/16, and Mini-PLC-2/17 processors. Consult your local Allen-Bradley distributor or sales engineer for information regarding this publication or any needed information.

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Chapter 2

Fundamentals of a Programmable Controller

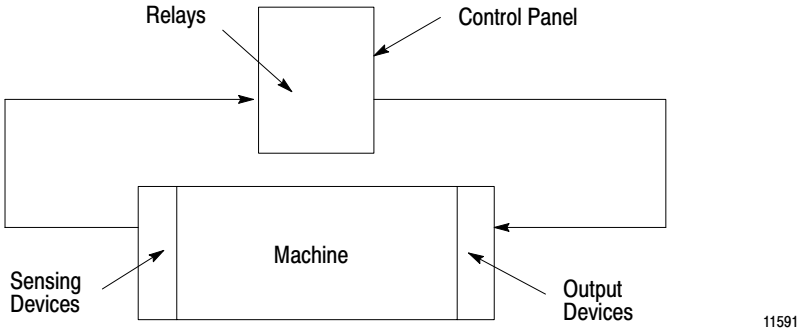
Chapter Objectives

In this chapter, you review general fundamentals common to our programmable controllers. This chapter:

- describes what a programmable controller does
- describe the functions of a programmable controller
- describes the four major sections of a programmable controller
- gives an example of a simple program

Traditional Controls

You are probably familiar with the traditional methods of machine control.



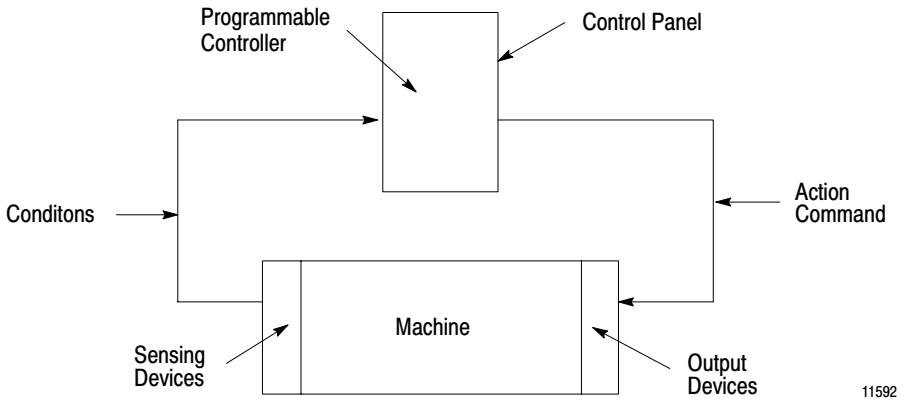
Sensing devices located on the machine detect changes in the machine's condition. For instance, a part arriving at a work station contacts and closes a limit switch, the sensing device. As a result, an electrical circuit is completed and a signal is sent to the control panel.

At the control panel, the electrical signal enters a bank of relays or other devices, such as solid state modules. Circuits within the control panel open or close causing additional electrical signals to be sent to output devices at the machine. For example, a relay energized by the limit switch closed by the arriving part may complete another circuit energizing the output device, a clamp, which secures the part at the work station.

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Programmable Systems

Systems run by programmable controllers operate in much the same way. Programmable controllers can perform many of the functions of traditional controls. Input sensing devices report machine conditions; output devices respond to commands.



Wiring between the machine and the controller provides electrical paths from the sensing devices to the controller and from the controller to the output devices.

However, instead of wiring relays together to produce a desired response, you simply tell your programmable controller how you want it to respond.

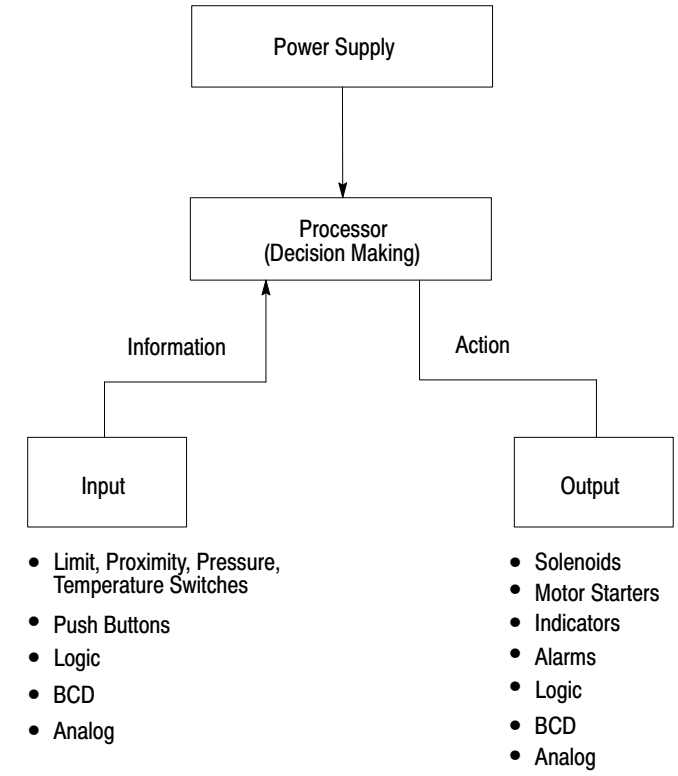
A program tells your programmable controller what you want it to do. A program is nothing more than a set of instructions you give the programmable controller telling it how to react to certain conditions within the machine.

The Four Major Sections

A typical programmable controller system usually consists of four major sections:

- processor
- input modules
- output modules
- power supply

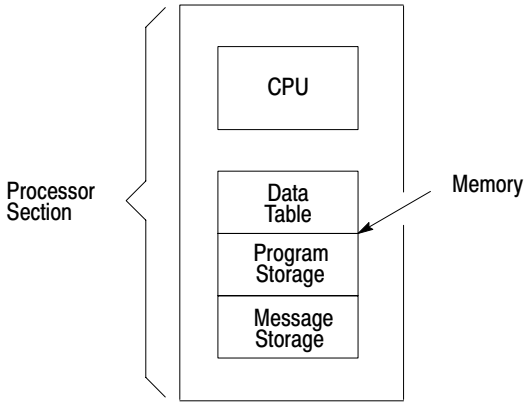
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Processor

The first section of a programmable controller is the processor. The processor might be called the “brains” of the programmable controller. It is divided into halves:

- central processing unit
- memory



Central Processing Unit

The Central Processor Unit (CPU) makes decisions about what the processor does according to the program you write.

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Memory

Memory serves three functions:

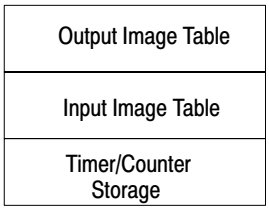
- stores information in the data table that the CPU may need
- stores sets of instructions called a program
- stores messages

Data Table

The area of memory where data is controlled and used, is called the data table. The data table is divided into several smaller sections according to the type of information to be remembered. These smaller sections are called:

- output image table
- input image table
- timer/counter storage

Data Table



This memory area:	Serves this purpose:
output image tables	The output image table controls the on or off status of the output devices wired to the output module's terminals. If an output image table bit is ON (1), its corresponding output device is ON (energized). If a bit is OFF (0), its corresponding output device is OFF (de-energized). Output image table bits are controlled by the user's program.
input image tables	The input image table duplicates the on or off status of the input devices. If an input device is ON (closed), its corresponding input image table bit is ON (1). If an input image table bit is OFF (open), its corresponding input image table bit is OFF (0). Input image table bits are monitored by the user's program.
timer/counter storage	Timer and Counter instructions are output instructions. They provide many of the capabilities available with timing relays and solid-state timing and counting devices. Usually conditioned by examine instructions, they keep track of timed intervals or counted events according to the logic of the rung.

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I/O Image Tables

The input image table reflects the status of the input terminals. The output image table reflects the status of bits controlled by the program.

Each image table is divided into a number of smaller units called bits. A bit is the smallest unit of memory. A bit is a tiny electronic circuit that the processor can turn on or off. Bits in the image table are associated with a particular I/O terminal in the input or output section.

When the processor detects a voltage at an input terminal, it records that information by turning the corresponding bit on. Likewise, when the processor detects no voltage at an input terminal, it records that information by turning the corresponding bit off. If, while executing your program, the CPU decides that a particular output terminal should be turned on or off, it records that decision by turning the corresponding bit on or off. In other words, each bit in the I/O image tables corresponds to the on or off status of an I/O terminal.

When people who work with personal computers talk about turning a bit on, they use the term “set.” For example - “The processor sets the bit” means “turns it on.” On the other hand, we use the term “reset” when we talk about turning the bit off - for example, “The processor reset the bit.”

Picture memory as a page that has been divided into many blocks. Each block represents one bit. Since each bit is either on or off, we could show the state of each bit by writing “on” or “off” in each block. However, there is an easier way. We can agree that the numeral one (1) means on and that the numeral zero (0) means off. We can show the status of each bit by writing 1 or 0 into the appropriate block. For example, you might hear expressions like, “The CPU responded by writing a one into the bit when the limit switch closed.” Of course, the processor didn’t really write a one into memory: it simply set the bit by turning it on.

When the I/O device is:	The bit status is said to be:
on	on 1 set
off	off 0 reset

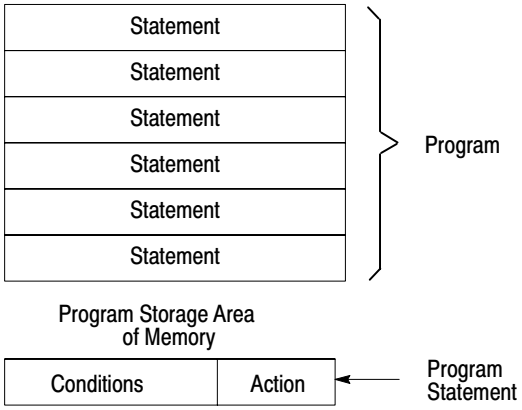
If you heard the expression, “The processor wrote a zero into that bit location.” What actually happened? If you said the processor merely reset the bit by turning it off, you’re right.

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Program Storage

Program storage takes up the largest portion of memory. This is where the user's program is stored. Each program is made up of a set of statements. Each statement does two things:

- It describes an action to be taken. For instance, it might say, "Energize motor starter number one."
- It describes the conditions that must exist in order for the action to take place.



For example, you may want this action to take place: "Whenever a certain limit switch closes." So your condition could be: "If limit switch number two is closed,..." The action would be: "energize motor starter number one." Therefore, when limit switch number two at the machine closes, the programmable controller energizes the motor starter. If limit switch number two does not close, the programmable controller does not energize the motor starter. Thus, when limit switch number two opens, the programmable controller de-energizes the motor starter because that action is implied in the statement.

A program is made up of a number of similar statements. Typically, there is one statement for each output device on the machine. Each statement lists the conditions that must be met and then, states the action to be taken.

Each condition is represented by a specific instruction; therefore, each action is represented by a specific instruction. These instructions tell the processor to do something with the information stored in the data table.Some instructions tell the processor to read what's written in the image table. When the processor is instructed to read from an image table, it examines a specific bit to see if a certain I/O device is on or off.

Other instructions tell the processor to write information into the image table. When the processor is instructed to write into the output image table, it writes a one or a zero into a specific bit. The corresponding output device will turn on or off as a result.

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Message Storage
The third area of memory, message storage, begins after the end statement in the user's program. Two alphanumeric characters can be stored in a word. Messages are entered into memory from either a 1770-T3 terminal or a peripheral device.

Messages are displayed on a 1770-T3 terminal or a peripheral device each time a message is required. The messages are activated through program control by programming specific instructions in the ladder diagram program.

Input Modules

The input modules of a programmable controller have four functions:

- termination
- indication
- conditioning
- isolation

Termination
The input provides terminals for the field wiring coming from the sensing devices on the machine.

Indication
The input of most modules also provides a visual indication of the state of each input terminal with LED indicators. The indicator is on when there is a voltage applied to it terminal. The indicator is off when there is no voltage applied to its terminal. Since the indicator reveals the status of its terminal, it's usually called an input status indicator.

Input indicators are only associated with terminals used for wiring sensing devices to the input section. The terminal that's used to provide a ground for the sensing circuits has no indicator.

Conditioning
Another function of input modules is signal conditioning. Voltage levels used at the machine are usually not compatible with the voltage levels used within the programmable controller. The input modules receives the electrical signal from the machine and converts it to a voltage level compatible with the programmable controller's circuitry.

Isolation
The input isolates the machine circuitry from the programmable controller's circuitry. Isolation helps protect the programmable controller's circuitry from unwanted and dangerous voltage levels that may occur occasionally at the machine or in the plant's wiring system.

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Output Modules

The output modules of a programmable controller have four functions:

- termination
- indication
- conditioning
- isolation

Termination

The output provides terminals for the field wiring going to the output devices on the machine.

Indication

The output of most modules provides a visual indication of the selected state of each output device with LED indicators. The output status indicator is on when the output device is energized. A common term applied to either input status indicators or output status indicators is I/O status indicators. I/O stands for either input or output.

In older modules, when power is present at the output terminals, the status indicators are ON. In high density modules, power may not be present at the output terminals for the status indicator to be ON.

Conditioning

The output conditions the programmable controller's signals for the machine. That is, it converts the low-level dc voltages of the programmable controller to the type of electrical power used by the output devices at the machine.

Isolation

The output isolates the circuitry of the programmable controller from unwanted and dangerous voltages that occasionally occur at the machine or the plant's wiring system. Some situations require additional external protection.

Power Supply

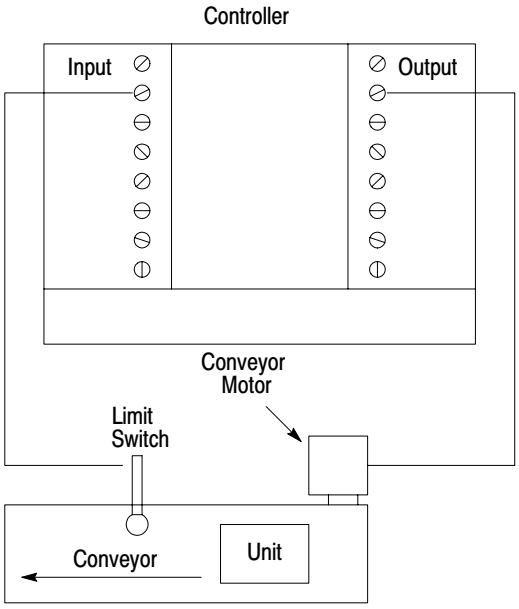
The power supply provides low-level dc voltage for the electronic circuitry of the processor, its input and output modules. It converts line voltages to the lower logic voltages required by the processor and its input and output modules.

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Control Sequence

Let's look at a simple example to see the sequence of events that take place in controlling a machine with a programmable controller (Figure 2.1). Suppose you are making a part. The motor driven conveyor carries a unit to the work area. The limit switch detects wen the part arrives at the work area. when that happens, we want the conveyor to stop so you can work on the part.

Figure 2.1
A Simplified Example of a Machine with a Programmable Controller



Notice how the limit switch and motor are wired to the programmable controller. The limit switch, wired to terminal 02, is normally-closed. The arriving part will open the switch. Therefore, the program statement controlling the conveyor motor must read: "If there is voltage at input terminal 02 (limit switch), then energize output terminal 02 (conveyer motor)." The conveyor motor is wired to output terminal 02.

Important: Figure 2.1 is for demonstration purposes only. We do not show the associated wiring, a motor starter, or an emergency stop button.

Since the limit switch is wired normally-closed, the conveyor motor runs until the arriving part opens the switch. At that time, the condition for energizing the motor is not longer met. Therefore, the motor is de-energized.

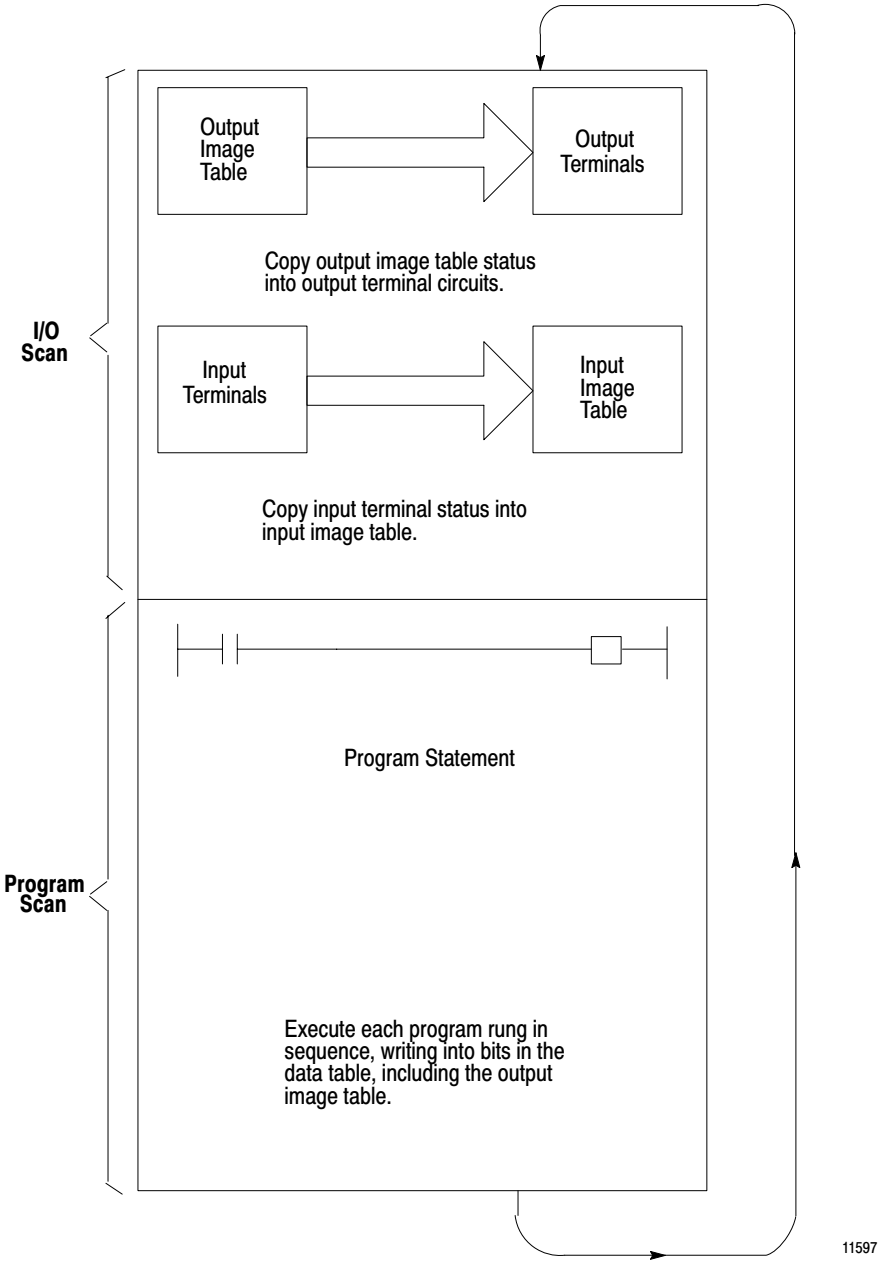
When the condition is met, we say it is true. When the condition is not met, we say it is false. There may be more than one condition which must be met before an action is executed. When all the conditions are met, the action is executed and we say the statement is true. When one or more of the conditions are false, the action is not executed and we say the statement is false.

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Scan Sequence

On power up, the processor begins the scan sequence (Figure 2.2) with a program pre-scan. This pre-scan is completed as if the entire program lies within an active MCR zone. Next the processor completes the I/O scan. During the I/O scan, data from input modules is transferred to the input image table. Data from output image table is transferred to the output modules.

Figure 2.2
Scan Sequence



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Next, the processor scans the program. It does this statement by statement. Each statement is scanned in this way:

1. For each input instruction, the processor checks, or "reads," the image table to see if the condition has been met.
2. If the set of conditions has been met, the CPU writes a 1 into the bit location in the output image table corresponding to the output terminal to be energized. On the other hand, if the set of conditions has not been met, the processor writes a 0 into the bit location, indicating that the output terminal should not be energized.

Here is a simple explanation of the program. If input 02 is on, then turn on output 02. If input 02 is off, then turn off output 02. The program could be written this way:

If (condition)	**Then** (action)
Input bit 02 is on	Turn output bit 02 on

In this example, the processor reads a 1 at input bit location 02 and knows that the condition has been met. The processor then carries out the action instruction by writing a 1 into output bit location 02.

If there were more statements in the program, the processor would continue in this same manner scanning each statement and executing each instruction until it reached the end of the program. Statement by statement, the processor would write a 0 or a 1 into an output bit as directed by the program. Then, the processor would read specific image table bits to see if the proper set of conditions were met. After reading and executing all program statements, the processor scans the output image table and energizes or de-energizes output terminals. The processor then goes to the input modules to update the input image table.

Now the entire process is repeated. In fact, it's repeated over and over again, many times a minute. Each time, the processor sets or resets output bits. Next, the processor senses the status of the input terminals. Finally, the processor scans the program and orders each output terminal on or off according to the state of its corresponding bit in the output image table.

When forcing is attempted, the processor's I/O scan slows down to do the forcing (see chapter 19). When forcing is terminated, the processor automatically switches back to the faster I/O scan mode.

When this example begins, the processor is energizing output terminal 02 because output bit 02 is on.

When the part is conveyed to the work station, it turns the limit switch off. When the limit switch is off, there is no voltage at input terminal 02. The processor scans the input image table, senses no voltage, and responds by writing a zero into bit 02 in the input image table.

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The processor scans the program. Our program states that if (conditions) input bit 02 is on, turn on output 02. If input bit 02 is off then output bit 02 is off. Since the alter condition is not true, the processor turns off output bit 02.

When the processor next scans the output image table, it sees the zero in output bit 02 and responds by de-energizing output terminal 02. The action causes the conveyor to stop.

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Chapter 3

Hardware Features

Chapter Objectives

This chapter is a summary of the Mini-PLC-2/02, -2/16, and -2/17 processors. In this chapter, you will read about:

- major features
- processor features
- series changes
- special features
- optional equipment

Major Features

A complete processor system consists of the following major components:

- a processor
- I/O chassis
- power supply
- as many as 16 I/O modules
- industrial terminal (cat. no. 1770-T3)[1]

Processor Features

This manual incorporates the features and instructions of three processors: Mini-PLC-2/02, -2/16, and -2/17. Unless stated otherwise, assume that the features or instructions are common to all processors.

- memory and data table
- memory protection above word address 177_8
- self-contained 120/220V AC power supply in cat. nos. 1772-LWP and 1772-LXP; cat. no. 1772-LZP supplies an additional 4A to the backplane for I/O
- mode select key switch
- diagnostic indicators
- I/O capacity: 128 for Mini-PLC-2/02
  256 for Mini-PLC-2/16
  512 for Mini-PLC-2/17
- 1/2-, 1-, or 2-slot addressing

1 Series C of the T3 terminal gives you the additional features required to take full advantage of all of the processor functions described. See Industrial Terminal section of this chapter.

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- basic instruction set:
  - relay-like instructions
  - up to 488 timers and counters in the processors
  - program control instructions
  - data manipulation and comparison
  - three-digit math (add, subtract, multiply, and divide)
- advanced instruction set:
  - jump instructions and subroutine programming
  - block transfer instructions
  - data-transfer file instructions
  - sequencer instructions
  - bit shift register instructions (bit shifts)
  - EAF functions: 6-digit add, subtract, multiply and divide, square root, Binary/BCD conversions, FIFO Load and Unload, log10, sine, cosine, 10x
  - The Mini-PLC-2/17 can perform these additional EAF functions: loge, y+/- x and e+/- x, reciprocal of x, averaging, standard deviation, PID, clock and calendar

Series Changes

The additional features of the various series of the processors are outlined in Table 3.A.

Important: The processor features described in the previous section apply to all series except where noted in Table 3.A.

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Table 3.A
Additional Features of Mini-PLC-2 Processors

	AA Batt	12.5msec/ K Scan	1/2AA Batt	Key Switch	Last State	1/2-Slot Addr	Bit Shift	7.5msec/ K Scan	Memory
Mini-PLC-2/02									
Series A		X	X	X	X	X	X		1K
Series D			X	X	X	X	X	X	2K
Mini-PLC-2/16									
Series A	X	X							3K
Series B Rev A or B		X	X	X					3K
Series B Rev C or later		X	X	X		X	X		3K
Series C		X	X	X	X	X	X		3K
Series D			X	X	X	X	X	X	4K
Mini-PLC-2/17									
Series A	X	X							6K
Series B Rev A or B		X	X	X		X	X		6K
Series B Rev C or later		X	X	X		X	X		6K
Series C		X	X	X	X	X	X		6K
Series D			X	X	X	X	X		7.75K

Special Features

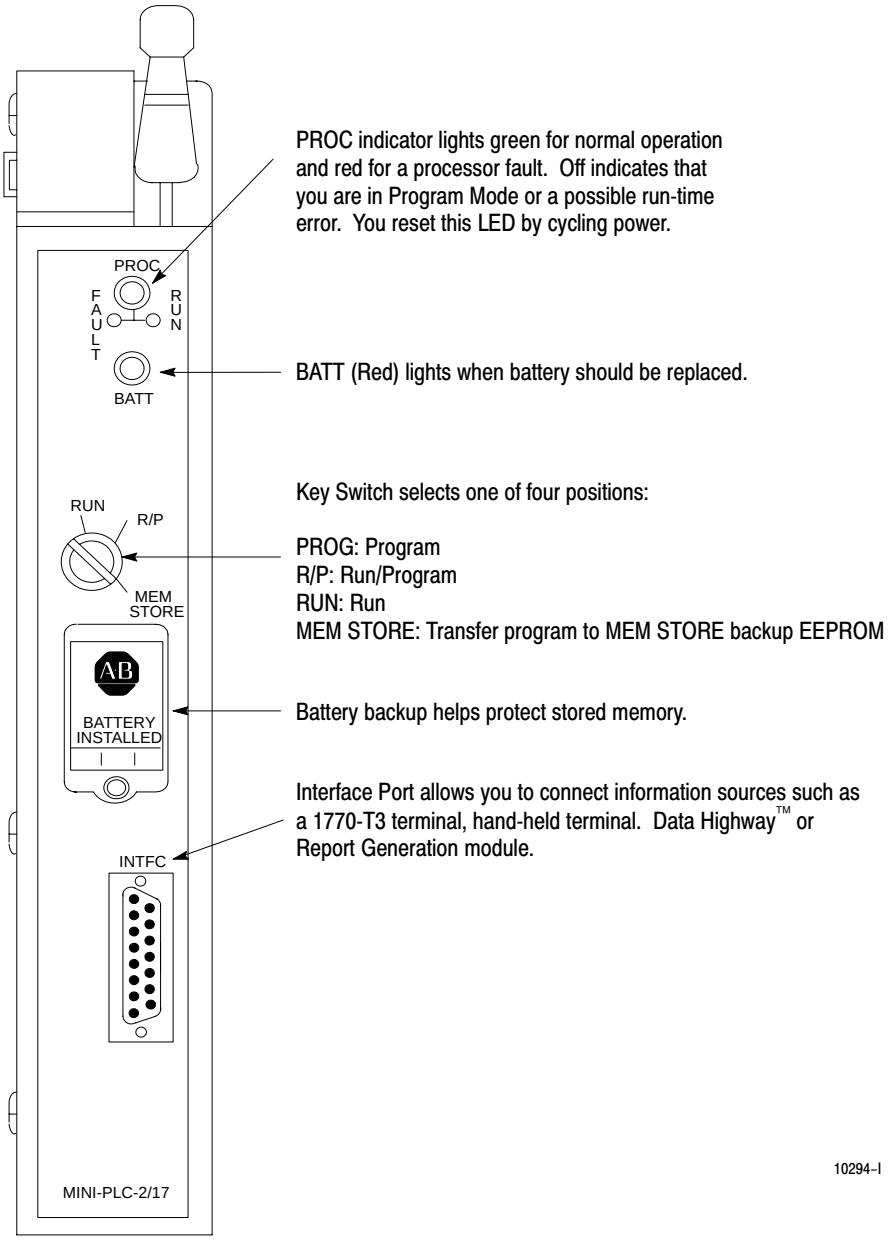
- on-line data change
- on-line programming
- selectable timed interrupt enables recurring subroutine
- self-contained lithium battery for memory
- full I/O forcing when using 2-slot addressing — I/O forcing only on rack 1 addresses when using 1-slot or 1/2-slot addressing and a series B 1770-T3 terminal, or earlier. The series C 1770-T3 terminal allows full I/O forcing when using 2-slot, 1-slot or1/2-slot addressing.
- data highway interface
- report generation

Processors

The front panels of the processors are nearly identical. The only visual difference between them is the catalog number across the bottom of the processor (Mini-PLC-2/02, Mini-PLC-2/16, or Mini-PLC-2/17).

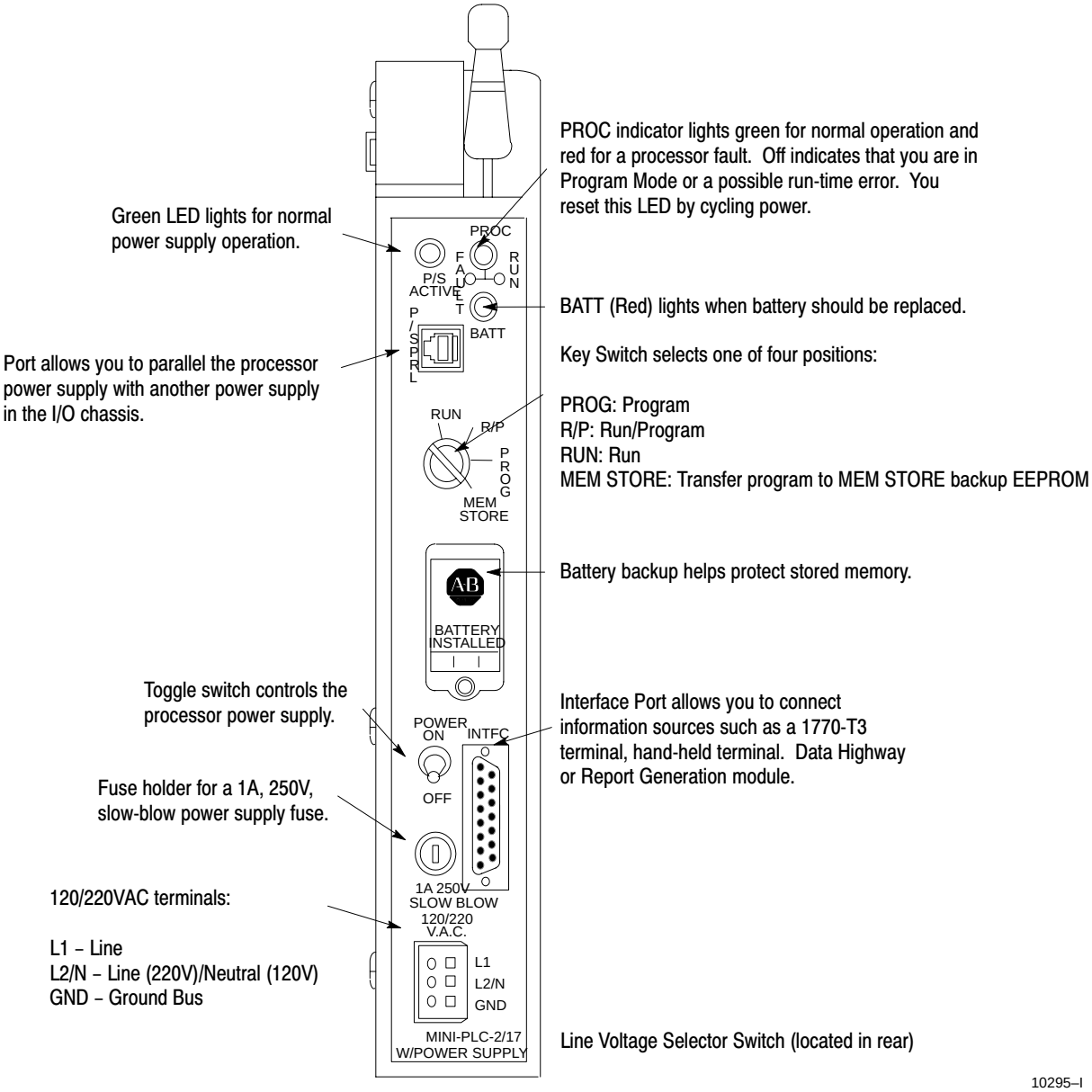
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Figure 3.1
Without a Power Supply



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Figure 3.2
With a Power Supply



Mode Select Key Switch

You can place the processor in any one of three modes of operation or program the EEPROM with the key switch located on the front of the processor.

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PROG – You can enter and edit your program from the 1770-T3 industrial terminal. User program and I/O are not scanned when the switch is in this position and outputs are disabled. You cannot change to another mode of operation with the 1770-T3 terminal when the switch is in this position.

R/P – When your key switch is in this position, the processor can be programmed for any one of three modes of operation.

- Run/Program – Change your key switch from PROG through R/P to RUN and back to R/P or, using the 1770-T3 terminal, press the key sequence SEARCH 590. In this mode, your program is continuously scanned and executed. You can:

  - make on-line changes to the data table
  - force instructions
  - make on-line programming changes
  - select remote mode of operation

- Remote Program – Change your key switch from PROG to RP or, using a 1770-T3 terminal, press the key sequence SEARCH 592. In this mode:

  - you can enter and edit a program.

  - the processor stops scanning and executing its stored program and waits for commands from the programmer.

- Remote Test – Use this mode to test your program.

Using a 1770-T3 terminal, press the key sequence SEARCH 591.

1. program is executed
2. inputs are scanned
3. outputs are disabled

RUN – The processor scans and executes your program. You cannot change to another mode of operation with the 1770-T3 terminal when the switch is in this position nor can you alter the program or change any data.

MEM STORE – The processor will load your program to be backed up by EEPROM when you switch to this position, then to PROG, then back to the MEM STORE position within one second.

Battery Backup

Memory contents may be lost when the processor loses power. A battery in the processor guards against loss of data. The battery holder accepts a AA lithium battery (cat. no. 1770-XZ).

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ATTENTION: Use only an Allen-Bradley authorized 1770-XZ 3.6V "1/2AA" size (Tadiran TL 2150 Type 1/2AA/s lithium thionyl chloride battery with pressure contacts. Using an unauthorized battery could result in sub-standard performance of your processor.

See chapter 4 for details about battery installation and disposal.

INTFC (socket)

The 15 pin socket, labeled INTFC, provides communication between the processor and the programming terminal (1770-T3 or 1784-T50), the 1770-RG report generation module, the 1770-T11 hand held terminal, the 1772-KG interface module or 1771-KA communications interface module.

Processor Module and:	Through:	Catalog Number:
Industrial Terminal (cat. no. 1770-T3)	PLC-2 Program Panel Interconnect Cable	1772-TC
Industrial Terminal (cat. no. 1784-T50)	PLC-2 Program Panel Interconnect Cable	1772-TC or 1784-CP2
Data Highway Communication Modules	Data Highway/Processor Cables	1771-CN, -CO, or -CR
PLC-2 Family Report Generation Module (cat. no. 1770-RG)	PLC-2 Program Panel Interconnect Cable	1772-TC (with external ground wire only)

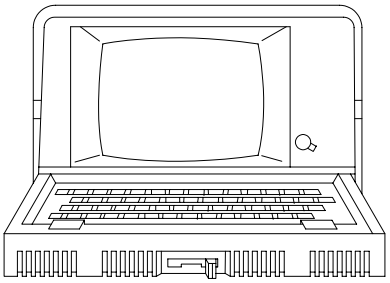
The 1784-T50 also requires PLC-2 6200 programming software (cat. nos. 6201-PLC2, 6203-PLC2, 6211-PLC2, or 6213-PLC2).

Optional Equipment

Industrial Terminal

Use a 1770-T3 terminal (Figure 3.3) to program your processor. With this 1770-T3 terminal you can enter, edit, test, and troubleshoot your program.

Figure 3.3
An Industrial Terminal System



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We recommend that you use a series C, revision C or later 1770-T3 terminal; earlier versions do not provide full functionality. You can use a 1770-T1 or 1770-T2 industrial terminal to program the processors; however, only instructions supported by these terminals can be programmed.

ATTENTION: Programs entered using a 1770-T3 Industrial Terminal must not be edited with either a 1770-T1 or a 1770-T2 industrial terminal. Such editing could result in unexpected operation with possible damage to equipment and injury to personnel.

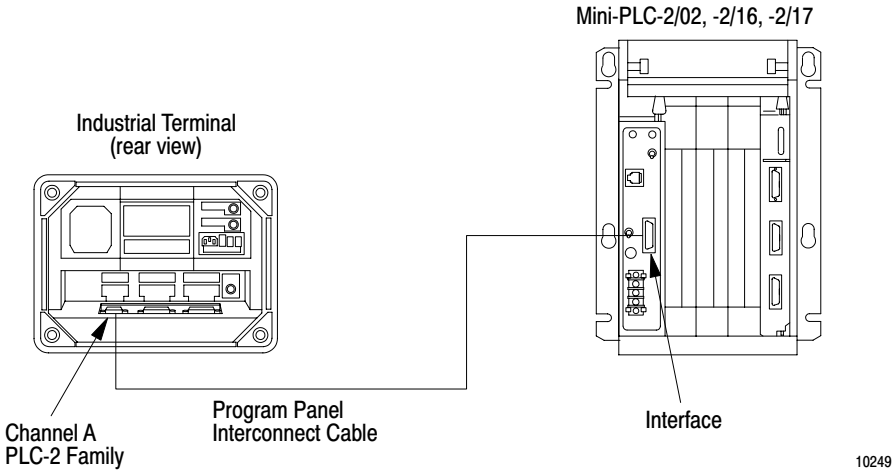
When using 1-slot or 1/2-slot addressing, use a series C 1770-T3 terminal to obtain full compatibility with the processor. With this series terminal, you can perform the following operations in rack 1, 2, 3 or 4.

- immediate I/O
- block transfer
- full forcing

Installing the 1770-T3 Terminal

Before you start to program your processor make sure all of your peripheral equipment is installed properly. Follow these basic instructions to connect the 1770-T3 terminal to the processor (Figure 3.4).

Figure 3.4
The Connections Between an Industrial Terminal and a Processor



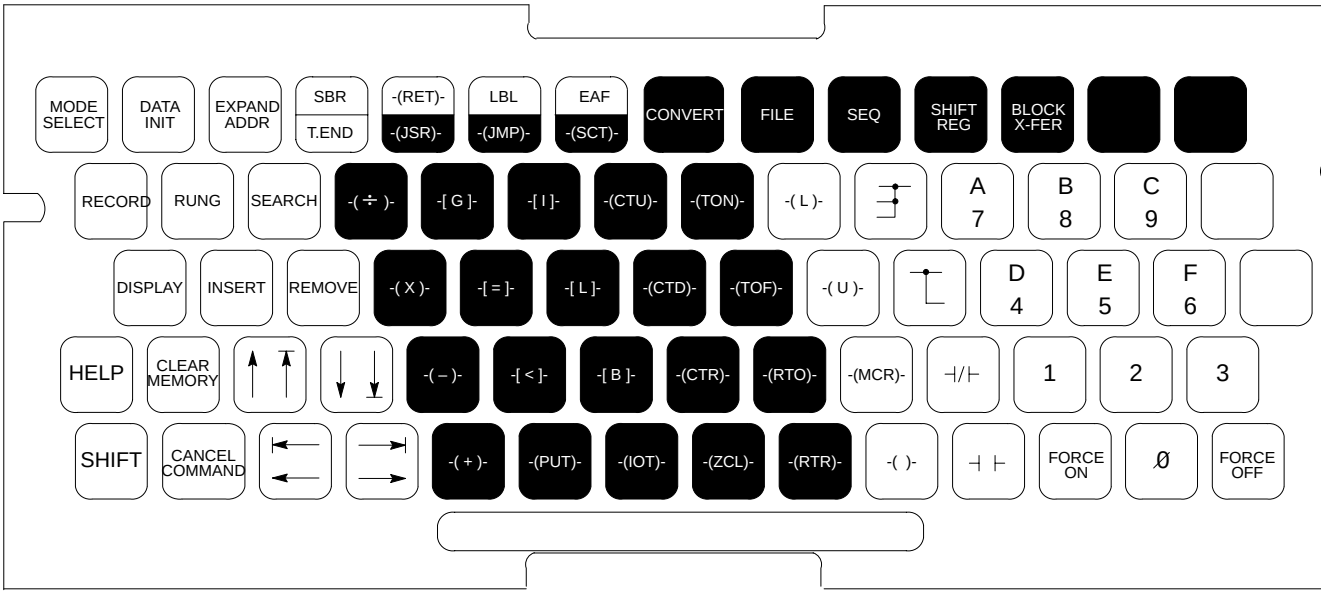
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1. Connect one end of the PLC-2 Program Panel Interconnect Cable (cat. no. 1772-TC) to CHANNEL A at the rear of the industrial terminal.

2. Connect the other end of the cable to the socket labeled INTFC at the front of the processor.

3. Place the PLC-2 Family Keytop Overlay (cat. no. 1770-KFA) (Figure 3.5) onto the keyboard.

Figure 3.5
A PLC-2 Family Keytop Overlay



4. Plug the ac power cord of the terminal into the ac power source.

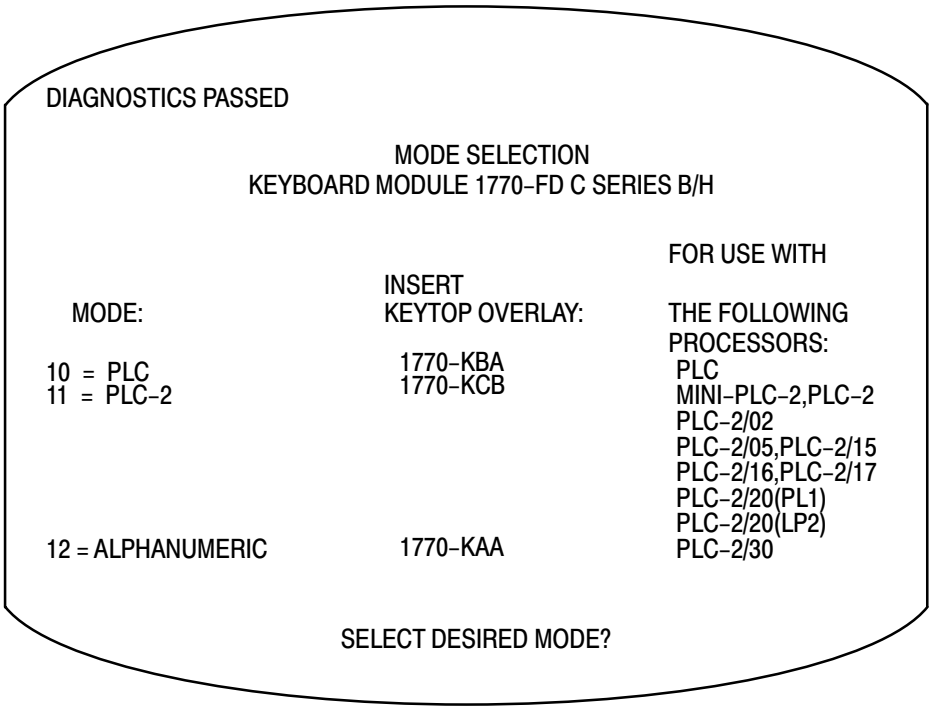
5. If using a 1772-LWP, -LXP, or -LZP processor, plug the power cord into the ac power source.

6. Turn the power switch on the front of the industrial terminal to the ON position.

7. Turn the power switch of the 1772-LWP, -LXP, -LZP processor to the ON position.

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8. After a short while the following display appears.



9. Select the PLC-2 mode by pressing [1] [1] on the 1771-T3 terminal.

Industrial Terminal Keyboard

The detachable keyboard houses PROMs, a sealed touchpad, and a keytop overlay.

There are three keytop overlays:

- PLC-2 family processor — for use with any PLC-2 family processor.
- PLC processor — for use with any PLC family processor.
- Alphanumeric — for alphanumeric characters and graphic characters generation.

Key Symbols — There are no numbered keys greater than 9. To display numbers greater than 9 press the individual keys. For example:

To display:	10	234
Press individually:	[1][0]	[2][3][4]

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Some keys have two symbols occupying one key (Figure 3.5). To display the top section of each key, press your shift key before the desired symbol. For example:

To display:	7	A
Press individually:	7	[Shift] A

Data Monitor Functions — You can display on a CRT and print directly to a data terminal – binary, hexadecimal, and ASCII data monitor functions with the keystrokes in Table 21.B.

Data Cartridge Recorder

The data cartridge recorder is a portable recorder that loads programs into and records the memories of the programmable controllers. Be sure switch no. 8 of the backplane switch group is OFF (disable memory protect) to load a program from a cartridge. See the Data Cartridge Recorder User Manual, publication 1770-6.5.4, for details.



ATTENTION: You must ensure that the addressing mode stored on the data cartridge and the current addressing mode selected for the rack are the same prior to uploading a data cartridge. Failure to do so would result in unpredictable machine operation. The series C, revision C 1770-T3 terminal prompts you in choosing the proper addressing mode.

Report Generation Module

The report generation module (cat. no. 1770-RG) provides bi-directional communication for report generation between the processor and an EIA RS-232-C peripheral device. The module allows you to store, delete, edit, report, and display messages in the processor memory.

Power Supply Modules

The following table lists the power supplies we recommend. If you are going to parallel a power supply and a 1772-LWP, -LXP, or -LZP processor, use either a 1771-P3 or 1771-P4 power supply.

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This Power Supply:	Receives Power from:	And Supplies this Power to the Chassis:
1771-P3	an external 120V ac power source	+5V dc
1771-P4		
1771-P5	an external 24V dc power source	
1771-P7	an external 120V or 220V ac power source	

ATTENTION: Do not parallel a 1771-P5 power supply and a 1772-LWP, -LXP, or -LZP processor because of power-up and power-down timing differences.

Paralleling Cable

Use the 1771-CT paralleling cable to connect the 1771-P3 and 1771-P4 power supplies in parallel with the 1772-LZP, -LXP, or -LWP processor.

EEPROM

The 1785-MJ EEPROM provides 8K backup; the 1772-MJ EEPROM provides 4K backup. Both EEPROMs are non-volatile and are physically interchangeable.

- You can use the 1772-MJ with the PLC-2/02 and -2/16 processors. You can also use it with a PLC-2/17 processor if your program END statement address is not greater than 4095 and you have no stored messages.
- If your PLC-2/17 processor END statement is greater than 4095, then, you must use the 1785-MJ for backup memory.

Important: You can use the 1785-MJ with the PLC-2/02 or -2/16 processors but you won't use its full capacity.

ATTENTION: You must ensure that the addressing mode stored on the EEPROM and the current addressing mode for the selected rack are the same prior to uploading the EEPROM. Failure to do so may result in unpredictable machine operation.

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Transferring a Program into the EEPROM (Burning the EEPROM)

1. Put the processor in the remote program or program mode of operation.

2. Place the keyswitch into the MEM STORE position, then to PROG, and then back to MEM STORE within one second until the green PROC RUN indicator turns ON. This indicator turns OFF after a few seconds. If the PROC RUN indicator does not turn green (or if it turns red), the program was not stored.

Important: Be careful not to touch any of the keys on the industrial terminal keyboard at any time during the EEPROM burn. If any key is pressed during the burn, the terminal will exhibit temporary communications problems and must be re-initialized to the PLC-2 programming mode. Press [1] [1] to re-initialize the terminal **after the EEPROM burn is complete.**

Important: Do not leave the keyswitch in the MEM STORE position after the burn is complete. The terminal will display program mode, but ladder programming operations will be extremely slow.

Transferring a Program into the Processor from EEPROM

1. Turn off power to the processor.

2. Set switch 6 of the switch assembly group on the I/O chassis backplane to the OFF position. This allows the processor to unconditionally load its memory with EEPROM contents on power up.

3. Turn on power to the processor.

Program transfer and execution begin immediately.

See the EEPROM Memory Module Product Data, publication 1772-2.22 for details. See Table 4.D for further information about setting switch 6.

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Chapter 4

Installing Your Programmable Controller

Chapter Objectives

This chapter discusses the location and methods of installing your processor. When you have finished, you should be able to:

- determine where to locate your processor system
- install your processor system

Related Hardware

Table 4.A lists the hardware needed to install your processor system.

Table 4.A
Hardware for Your Processor System

Allen-Bradley Hardware	Catalog Number
I/O chassis	1771-A1B, -A2B, -A3B, -A3B1, -A4B
I/O modules	1771 product line
Industrial terminal	1770-T3 series C
Power supplies	1771-P3, -P4, -P5, -P7
Emergency stop	800 product line switches
Master control relay	700 product line
Disconnects	1494 product line
Suppression devices	599-K04, 700-N24, 1401-N10

The quantity of the hardware you need depends on your application. Consult your local Allen-Bradley sales engineer or distributor for more information concerning these items.

In addition to our hardware, we recommend:

- a metal enclosure to protect your processor from electromagnetic interference (EMI) noise and airborne contaminants
- enclosure backpanel
- power supplies for I/O devices
- 6.35 mm (0.25 inch) bolts
- power cable for ac input power
- electrical tape or shrink tubing
- tie wraps for wires

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Planning Your Processor System

A well-planned layout is essential for the installation of your processor. You should consider the following factors:

- location
- environment
- mechanical protection
- conductor categories
- raceway layout
- power distribution
- surge suppression

Location

Determining the proper location should be your primary concern. We specify:

This Characteristic:	Should Meet this Specification:
Operating temperature	0 to 60°C (32 to 140°F)
Storage temperature	-40 to 85°C (-40 to 185°F)
Relative humidity	5 to 95% (without condensation)

Environment

Separate the processor system from other equipment and plant walls to allow for convection cooling. Convection cooling draws a vertical column of air upward over the processor. Cooling air must not exceed 60°C (140°F) at any point immediately below the processor. If the air temperature does exceed 60°C, install:

- fans inside the enclosure to bring in filtered air or recirculate internal air, or
- air conditioning/heat exchangers

Follow these guidelines when installing your processor system:

- Allow six vertical inches above and below all processor components, including other processors.
- Allow four horizontal inches on the sides of each processor component. When you use more than one processor in the same area, allow six horizontal inches between each processor.
- Allow two inches (vertical and horizontal) between the processor and the wiring duct or terminal strips.
- Mount the I/O chassis horizontally to allow convection cooling.

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Mechanical Protection

You provide the enclosure for your processor system. This enclosure is the primary means of protecting your processor system from atmospheric contaminants such as oil, moisture, dust, corrosive materials, or other harmful substances. We suggest that you use an enclosure that conforms to the National Electrical Manufacturer's Association standard (NEMA Standard Publication No. ICS 6).

Mount the enclosure in a position that lets you fully open the doors. You need easy access to the processor's wiring and related components.

When choosing the enclosure size, allow extra space for isolation transformers, fusing, disconnect switch, master control relay and terminal strips. Your processor requires a minimum of eight inches of space from the rear of the chassis to the innermost front surface of the enclosure.

Conductor Categories

When planning your raceway layout, classify into the following categories all wires and cables connecting your processor system. See the documentation for each specific I/O module for its individual classification.

Category-1 Conductors

Category-1 conductors are, in general, high-power conductors that are, therefore, more tolerant of electrical noise than category 2 conductors and may also generate more noise. They include:

- **ac power lines**
- **high-power ac I/O lines** — They connect to ac I/O modules that are rated for high power and high noise immunity.
- **high-power dc I/O lines** — They connect to dc I/O modules that are rated for high power or have input circuits with long time-constant filters for high noise rejection. They typically connect to devices such as:
  - hard-contact switches
  - relays
  - solenoids

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Category-2 Conductors

Category-2 conductors are, in general, low-power conductors that are, therefore, less tolerant of noise than category-1 conductors and should also generate less noise. They include:

- **serial communication cables** — They connect between processors or to remote I/O adapter modules, programming terminals, computers, or data terminals.
- **low-power dc I/O lines** — They connect to dc I/O modules that are rated for low power and have input circuits with short time-constant filters to detect short pulses. They typically connect to devices such as:
  - proximity switches
  - photo-electric sensors
  - TTL devices
  - encoders
  - motion-control devices
  - analog devices
- **low-power ac-dc I/O lines** — They connect to I/O modules that are rated for low power such as low-power contact-output modules.

Category-3 Conductors

Category-3 conductors interconnect the processor components within an enclosure. Processor cables include:

- processor power cables — provide backplane power to processor components
- local I/O interconnect cables — connect to local I/O adapter modules
- processor-peripheral cables — connect processors to their communication interface modules

Raceway Layout Guidelines

The following are general guidelines for routing wires and cables for your processor system. These guidelines apply to wire and cable routing both inside and outside of the enclosure. Follow these guidelines to guard against coupling noise from one category conductor to another.

- All category-1 conductors can be routed with machine power conductors of up to 600V ac (feeding up to 100 hp devices) if this does not violate local codes. Article 300-3 of the National Electrical Code requires that all conductors (ac and/or dc) in the same raceway must be insulated for the highest voltage applied to any one of the conductors in the raceway.

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- All category-2 conductors must be properly shielded, where applicable, and routed in a separate raceway.
- If a category-2 conductor must cross power feed lines, it should do so at right angles.
- Route category-2 conductors at least 1 foot from 120V ac power lines, 2 feet from 240V ac power lines, and 3 feet from 480V ac power lines.
- Route category-2 conductors at least 3 feet from any electric motors, transformers, rectifiers, generators, arc welders, induction furnaces, or sources of microwave radiation.
- If a category-2 conductor is in a metal raceway or conduit, that raceway or conduit must be well grounded along its entire length.
- All category-3 conductors should be routed external to all raceways or in a raceway separate from any category-1 or category-2 conductors.

Power Distribution

In many applications, you can connect the processor power supply directly to the secondary of a transformer (Figure 4.1 and Figure 4.2). The transformer can provide dc isolation from other equipment not connected to that transformer secondary. Connect the transformer primary to the ac source; connect the high side of the transformer secondary to the L1 terminal of the power supply; connect the low side of the transformer secondary to the neutral (common) terminal of the power supply.

Sizing the Transformer

Note that the external-transformer rating (in VA) of each supply is 2.5 times its input power requirements (in Watts). This is necessary because, converting ac to dc draws power only from the peak of the ac voltage wave-form.

If the transformer's rating is too small, it will clip the peak of the sine wave. When the input voltage is still above the lower voltage limit, the power supply will sense this clipped wave form as a low voltage and shut down the processor prematurely. If the transformer is too large, it will not provide as much isolation as a transformer of proper size because a larger noise spike on the primary can pass through to the secondary.

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To determine the required rating of the transformer, add the external-transformer rating for the power supply and all other power requirements (input circuits, output circuits). The power requirements must take into consideration the surge currents of devices controlled by the processor. Choose a transformer with the closest standard transformer rating above the calculated requirements.

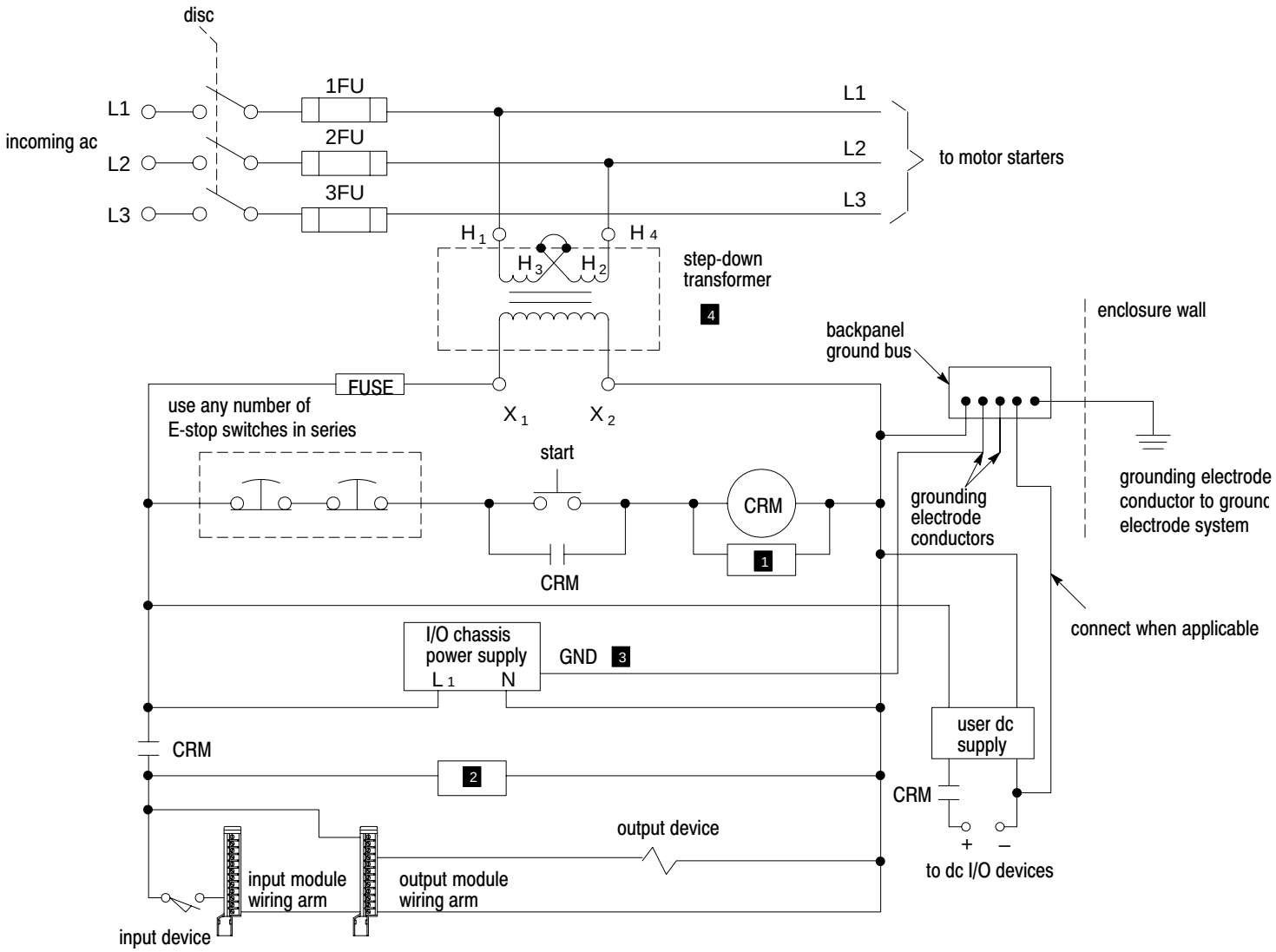
For example, the external-transformer rating of a 1771-P4S power supply is 150VA. A 150VA transformer could be used if a 1771-P4S power supply were the only load. A 500VA transformer should be used if there were 350VA of load in addition to that of the 1771-P4S power supply.

Undervoltage Shutdown

Each power supply is designed to generate a shutdown signal if the ac line voltage drops below its lower voltage limit. A shutdown in that situation is necessary to ensure that only valid data is stored in memory. The controller resumes operation when the line voltage reaches the lower voltage limit again.

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Figure 4.1
Grounded ac Power-Distribution System with Master Control Relay



1 To minimize EMI generation, you should connect a suppression network: for 120V ac, use Allen-Bradley cat. no. 700-N24; for 220/240V ac, use cat. no. 599-KA04.

2 To minimize EMI generation, you should connect a suppression network: for 120V ac, use Allen-Bradley cat. no. 700-N24; for 220/240V ac, use cat. no. 599-KA04.

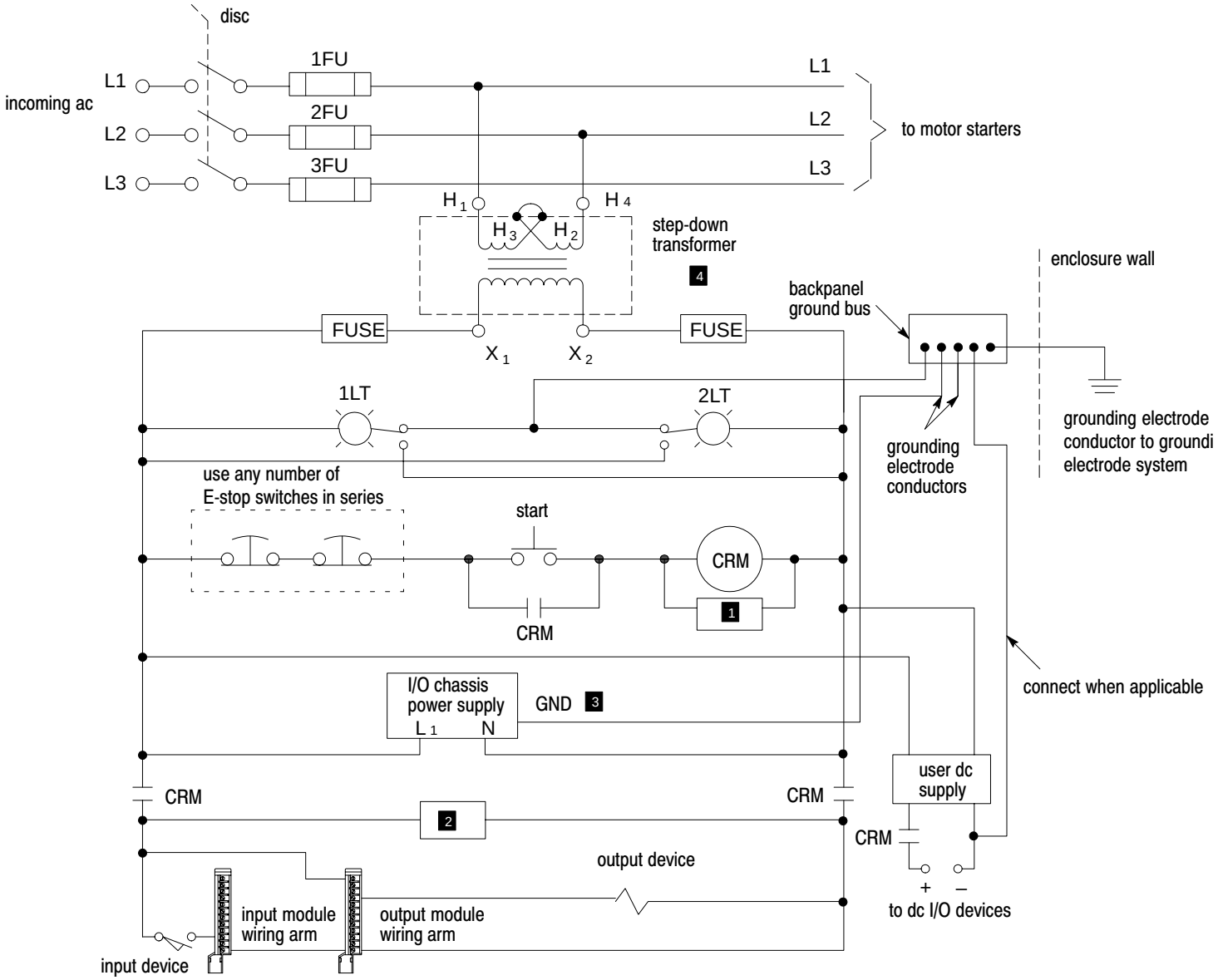
3 For a power supply with a groundable chassis, this represents connection to the chassis only. For a power supply without a groundable chassis, this represents connection to both the chassis and the GND terminal.

4 In many applications, a second transformer provides power to the input circuits and power supplies for isolation from the output circuits.

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Figure 4.2
Ungrounded ac Power-Distribution System with Master Control Relay



1 To minimize EMI generation, you should connect a suppression network: for 120V ac, use Allen-Bradley cat. no. 700-N24; for 220/240V ac, use cat. no. 599-KA04.

2 To minimize EMI generation, you should connect a suppression network: for 120V ac, use Allen-Bradley cat. no. 700-N24; for 220/240V ac, use cat. no. 599-KA04.

3 For a power supply with a groundable chassis, this represents connection to the chassis only. For a power supply without a groundable chassis, this represents connection to both the chassis and the GND terminal.

4 In many applications, a second transformer provides power to the input circuits and power supplies for isolation from the output circuits.

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Second Transformer

Allen-Bradley power supplies have circuits which suppress electromagnetic interference from other equipment. However, it is useful to isolate output circuits from power supplies and input circuits to guard against output transients from being induced into inputs and power supplies. Therefore, in many applications, power is provided to the input circuits and power supplies through a second transformer as in Figure 4.3. In some applications, a special kind of transformer is used for the second transformer.

Isolation Transformer

For installations near particularly excessive electrical noise generators, an isolation transformer (for the second transformer) will provide further suppression of electromagnetic interference from other equipment. The output devices being controlled should draw power from the same ac source as the isolation transformer, but not from the secondary of the isolation transformer (Figure 4.3).

Constant-Voltage Transformer

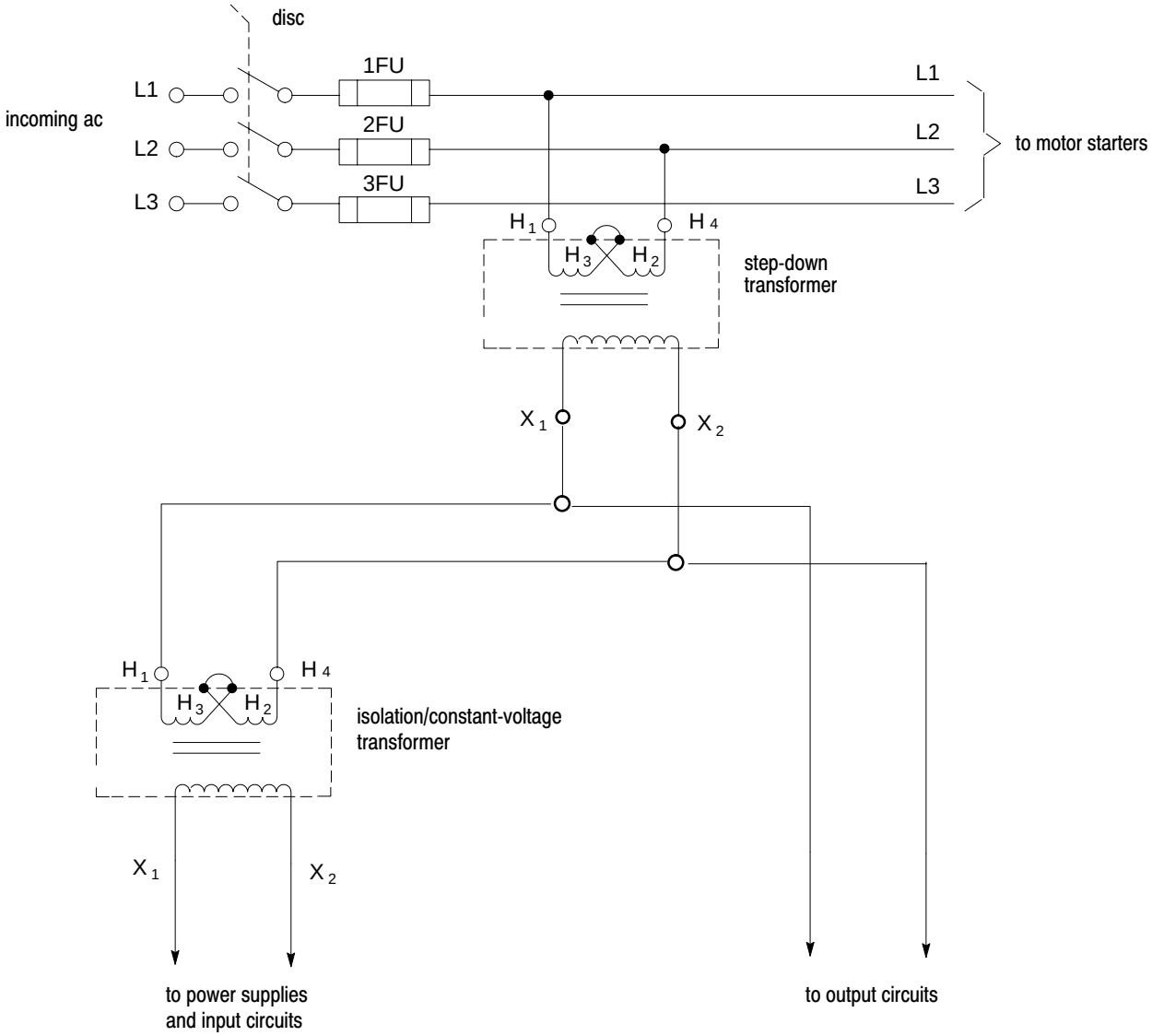
In applications where the ac power source is especially “soft” and subject to unusual variations, a constant-voltage transformer can stabilize the ac power source to the controller, thereby minimizing shutdowns. However, the constant-voltage transformer must provide a sinusoidal output.

If the controller power supply receives its ac power through a constant-voltage transformer, the input devices connected to the I/O chassis must also receive their ac power through the same constant-voltage transformer. If the inputs receive their ac power through another transformer, the ac source voltage could go low enough that erroneous input data enters memory while the constant-voltage transformer prevents the power supply from shutting down the controller.

The output devices being controlled should draw power from the same ac source as the constant-voltage transformer, but not from the secondary of the constant-voltage transformer (Figure 4.3).

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Figure 4.3
Power Supplies and Input Circuits Receiving Power through a Separate Transformer



Ground Connection

When bringing ac power into the enclosure, do not connect its raceway through an equipment-grounding conductor to the ground bus on the back-panel. The raceway should be grounded elsewhere. Connecting the raceway to the ground bus would cause a ground loop.

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Ground loops may introduce objectionable ground currents causing faulty operation of the programmable controller. If multiple grounding connections cause faulty operation, refer to Article 250-21 of the National Electrical Code for recommended methods of reducing the objectionable ground current.

When ac power is supplied as a separately derived system through an isolation/step-down transformer, you can connect it as a grounded ac system or an ungrounded ac system. For a grounded ac system, connect one side of the transformer secondary to the ground bus as in Figure 4.1. For an ungrounded ac system, connect one side of each test switch for the ground-fault-detector lights to the ground bus as in Figure 4.2.

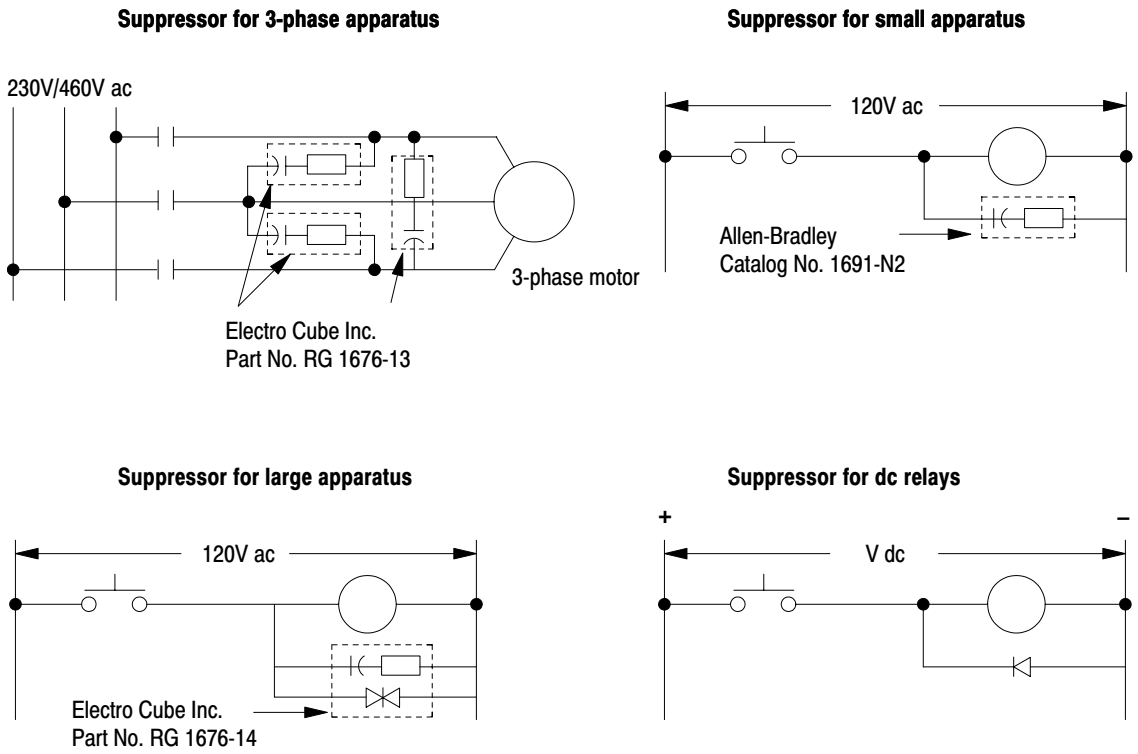
Surge Suppression

EMI can be generated whenever inductive loads such as relays, solenoids, motor starters, or motors are operated by “hard contacts” such as pushbutton or selector switches. The wiring and grounding practices described previously guard the processor system against the effects of EMI. However, in some cases it may be necessary to use suppression networks to suppress EMI at its source. Inductive loads controlled only by solid-state output devices alone do not cause comparable EMI generation. However, inductive loads on ac output modules that are in series or parallel with hard contacts require suppression networks to protect the module output circuits as well as to suppress EMI.

Connect suppression networks at the inductive loads. If you connect them at the switching devices, the wires connecting the switching devices to the inductive loads will act as antennas to radiate EMI. Figure 4.4 shows typical suppression circuitry for different types of loads. Allen-Bradley bulletin 700 relays and bulletin 509 and 709 motor starters have surge suppressors available as an option. Table 4.B lists these Allen-Bradley products and their suppressors.

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Figure 4.4
Typical Suppression Networks



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Table 4.B
Allen-Bradley Suppressors

Allen-Bradley Equipment	Suppressor Catalog Number
Motor Starter Bulletin 509	599-K04[1]
Relay Bulletin 700 Type N or P	700-N24[2]
Motor Starter Bulletin 709	1401-N10[1]
Miscellaneous	700-N24[3]

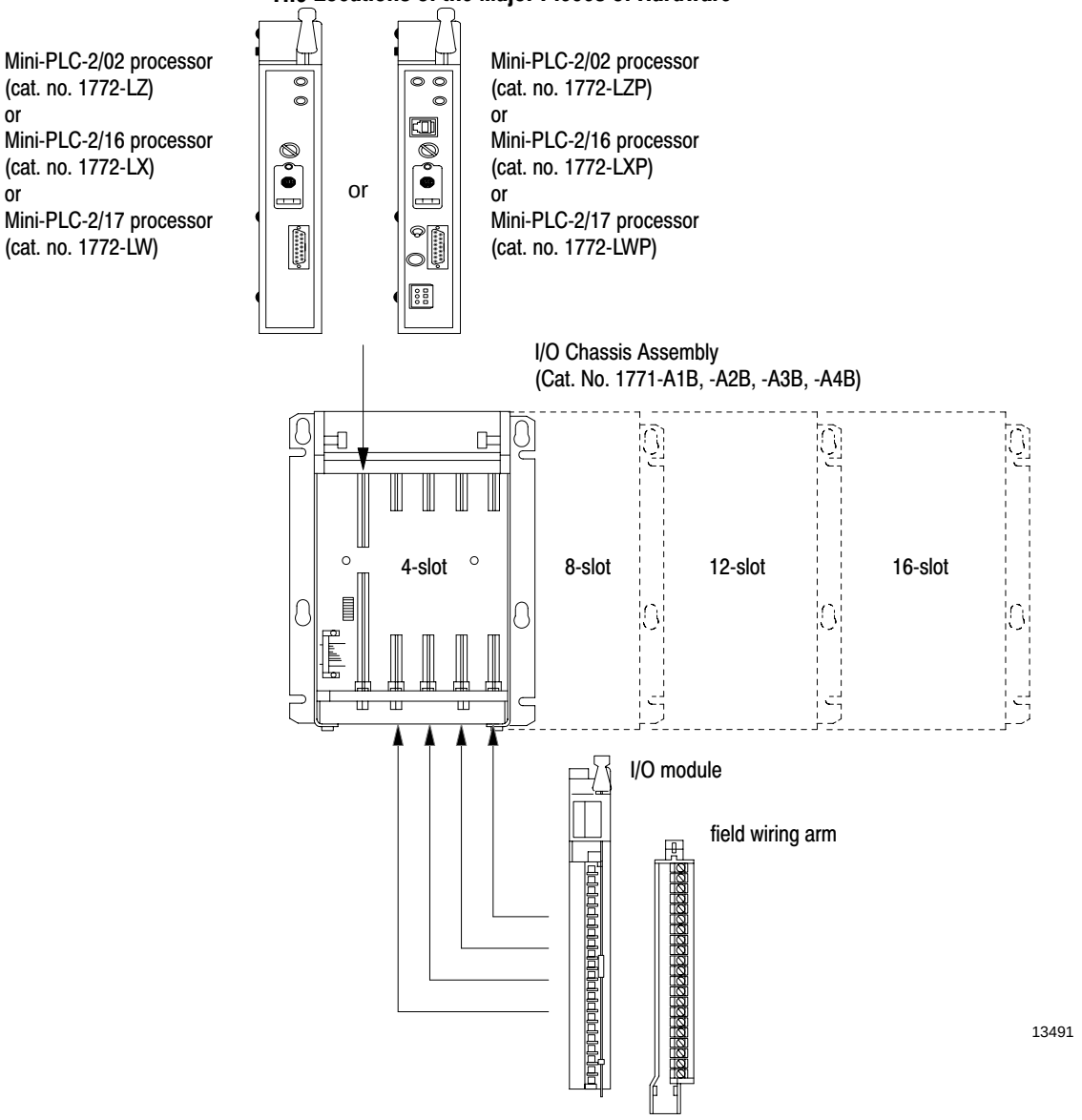
[1] For starters with 120V ac coils.
[2] Maximum coil voltage 150V ac or dc.
[3] The Bulletin 700-N24 is a universal surge suppressor. It can be used on electromagnetic devices with the limitation of 35 sealed VA, 150V.

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How to Install Your Processor

This section provides general installation guidelines. The input and output devices that control your manufacturing operations determine the specifics of your installation. Figure 4.5 shows the location of your major pieces of hardware.

Figure 4.5
The Locations of the Major Pieces of Hardware



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Installing your processor involves twelve steps. Perform these steps in order.

1. Mounting the backpanel (page 4-14)
2. Mounting and grounding components on the backpanel (page 4-15)
3. Setting the switches within the switch group assembly (page 4-22)
4. Installing keying bands and field wiring arms (page 4-24)
5. Installing I/O modules (page 4-26)
6. Installing backup battery (page 4-28)
7. Installing the EEPROM memory module (page 4-29)
8. Installing the processor (page 4-31)
9. Installing the power supply (page 4-31)
10. Wiring field wiring arms (page 4-32)
11. Connecting power to the processor or power supply (page 4-37)
12. Connecting the industrial terminal (page 4-42)

Electrostatic Discharge

Electrostatic discharge can damage integrated circuits or semiconductors in this processor if you touch backplane connector pins. Avoid electrostatic damage by observing the following precautions:

- Touch a grounded object to discharge yourself before handling the processor.
- Do not touch the backplane connector or connector pins.
- When not in use, keep the module in its static-shield bag.



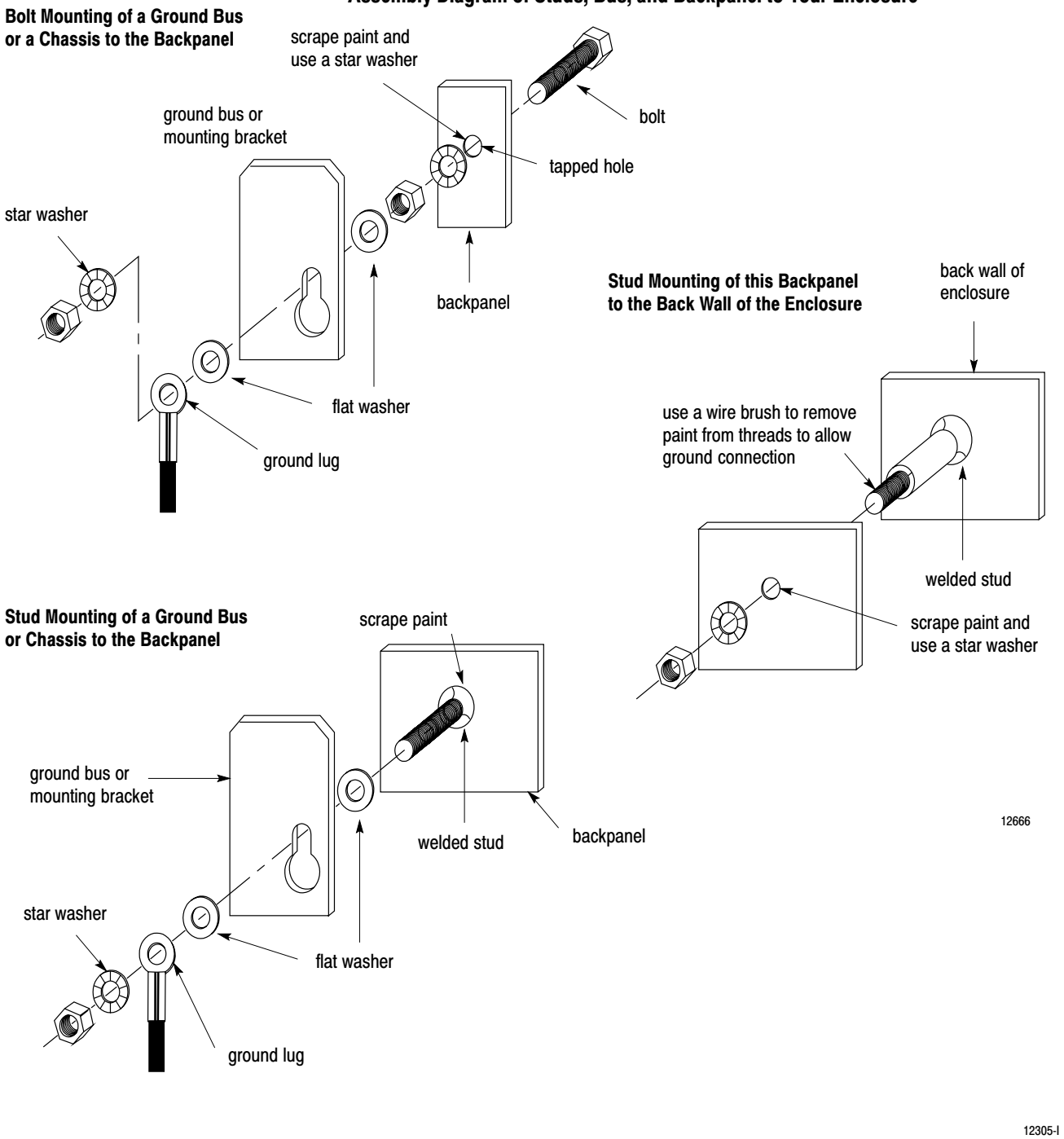
ATTENTION: Electrostatic discharge can degrade performance or damage the processor. Handle as stated above. Failure to observe this caution may cause damage to the processor.

Step 1 – Mounting the Backpanel

- Stud mounting of a backpanel to the back wall of an enclosure
- Bolt mounting of an I/O chassis or ground bus to the backpanel
- Stud mounting of an I/O chassis or ground bus to the backpanel

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Figure 4.6
Assembly Diagram of Studs, Bus, and Backpanel to Your Enclosure



Step 2 – Mounting and Grounding Components on the Backpanel

Use 6.35 mm (0.25 in.) bolts to mount the I/O chassis on the enclosure backpanel. For component spacing and dimensions see Figure 4.7 and Figure 4.8.

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Figure 4.7
Programmable Controller Components Must Not be Spaced Less Than These Minimums

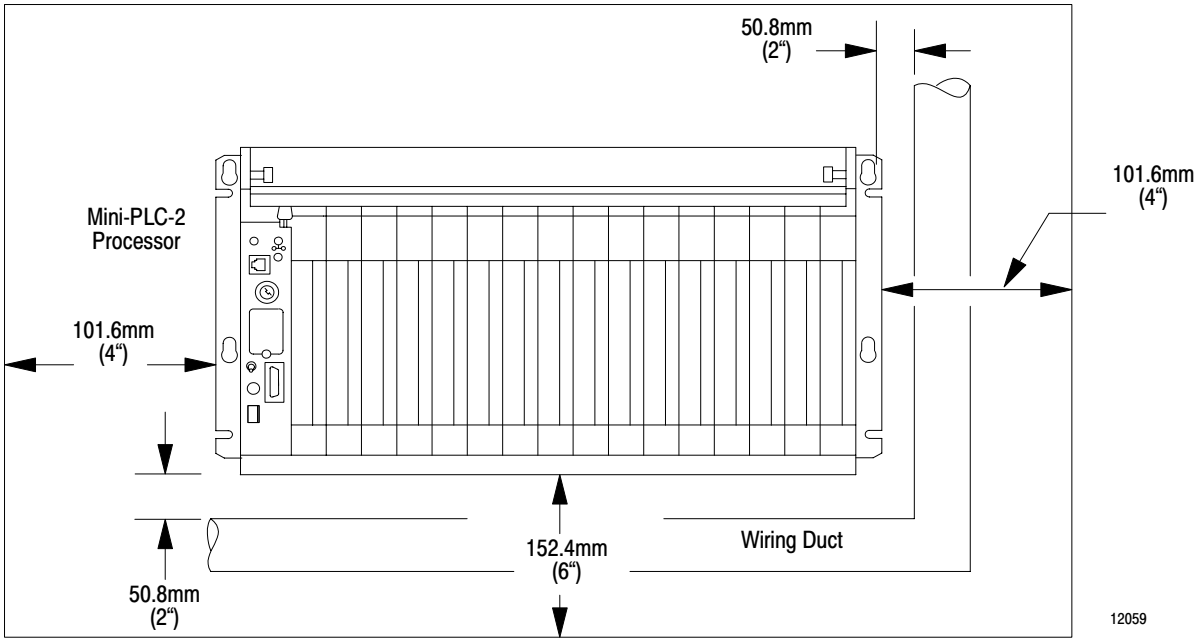
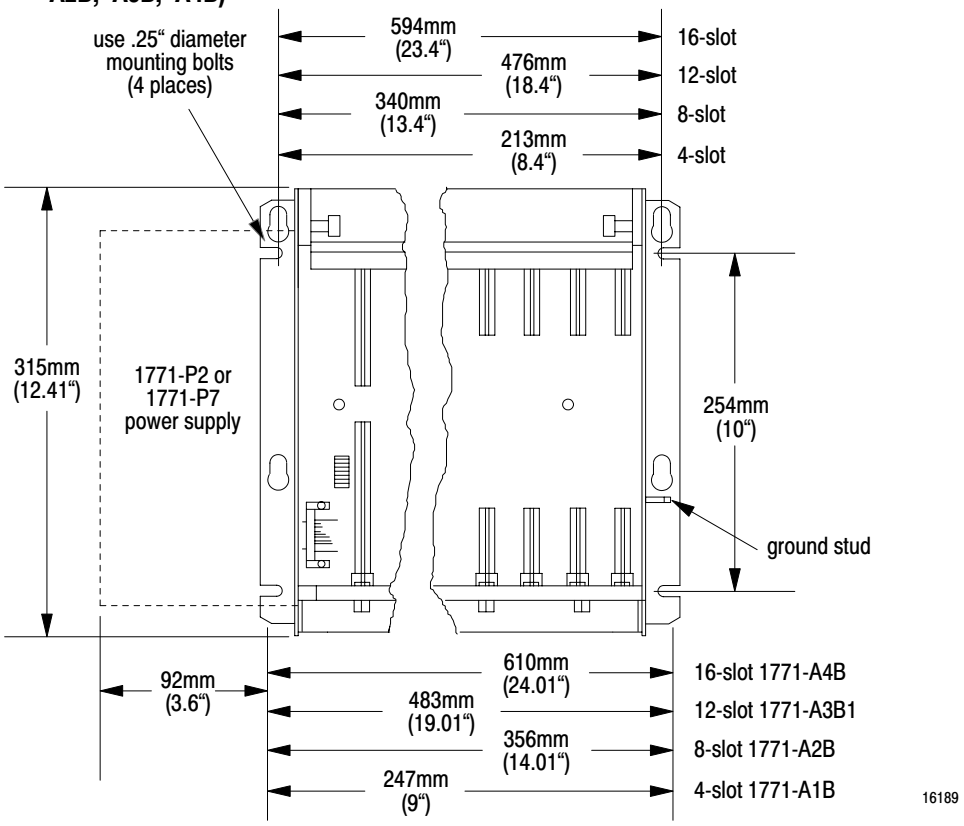


Figure 4.8
You Need These Dimensions to Mount an I/O Chassis (cat.no. 1771-A1B, -A2B, -A3B, -A4B)



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Before grounding your processor system, consult the following sources of information:

- National Electrical Code, published by the National Fire Protection Association of Boston, Massachusetts
- local codes and ordinances

Mounting Processor Components

After planning your layout, you can begin mounting the chassis. In mounting each chassis:

- Make sure each chassis lies flat. If the I/O chassis does not lie flat, shim it with washers so that the chassis is not warped, when the nuts are tightened. Warping an I/O chassis could damage the backplane and cause poor connections.
- Make good electrical connections between each I/O chassis, the backpanel, and the enclosure
- Remove paint or other nonconductive finish from studs and the backpanel so that good electrical contact is made at each bolt or stud.

After you have established all layouts, you can begin mounting and properly grounding each chassis.

Grounding is important for safety in electrical installations. With solid-state controls, proper grounding (including elimination of ground loops) has an added value of helping reduce the effects of electrostatic and electromagnetic interference. Providing a low-impedance path to earth-ground potential will reduce the chances of EMI causing your processor system to malfunction.

An authoritative source for safety grounding requirements is the National Electrical Code. Article 250 of the code provides such data as the size and types of conductors and methods of safely grounding electrical components. As defined in the code, a grounding path must be permanent and continuous, and must be able to safely conduct ground-fault currents that may occur in the system to ground with minimum impedance. Also, the connections to a grounding conductor must be a permanent nature. Local codes and ordinances dictate which grounding method is permissible.

Figure 4.8 showed mounting assembly details for stud-mounting of a chassis or ground bus to a backpanel, bolt-mounting of a chassis or ground bus to a backpanel, and stud-mounting of a backpanel to the back wall of the enclosure. You can mount the chassis with either bolts or welded studs.

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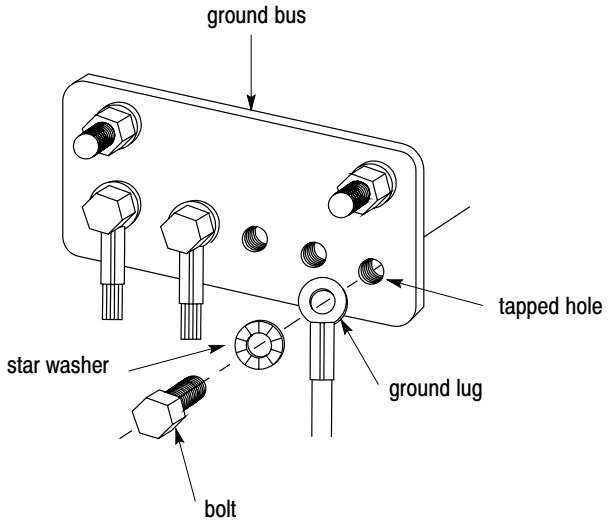
If the mounting brackets of a chassis do not lay flat before the nuts are tightened, use additional washers as shims so that the chassis will not be warped by tightening the nuts. Warping a chassis could damage the backplane and cause poor connections.

Make good electrical connection between each chassis, the backpanel, and the enclosure through each mounting bolt or stud. Wherever contact is made, remove paint or other non-conductive finish from around studs or tapped holes so that good electrical contact is made at each bolt or stud.

Equipment Ground Conductor

In addition to the connection through each bolt or stud, use either 1-inch copper braid or 8 AWG copper wire to connect between each chassis, the enclosure, and a central ground but mounted on the backpanel. Figure 4.9 and Figure 4.10 show ground-bus connection details. Figure 4.11 shows enclosure-wall ground connection details. Use a steel enclosure to guard against EMI. If the enclosure door has a viewing window, it should be a laminated screen or a conductive optical substrate to block EMI. Do not rely on the hinge for electrical contact between the door and the enclosure; install a bonding wire.

Figure 4.9
Ground Bus Connection Details



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Figure 4.10
Ground Bus Connections

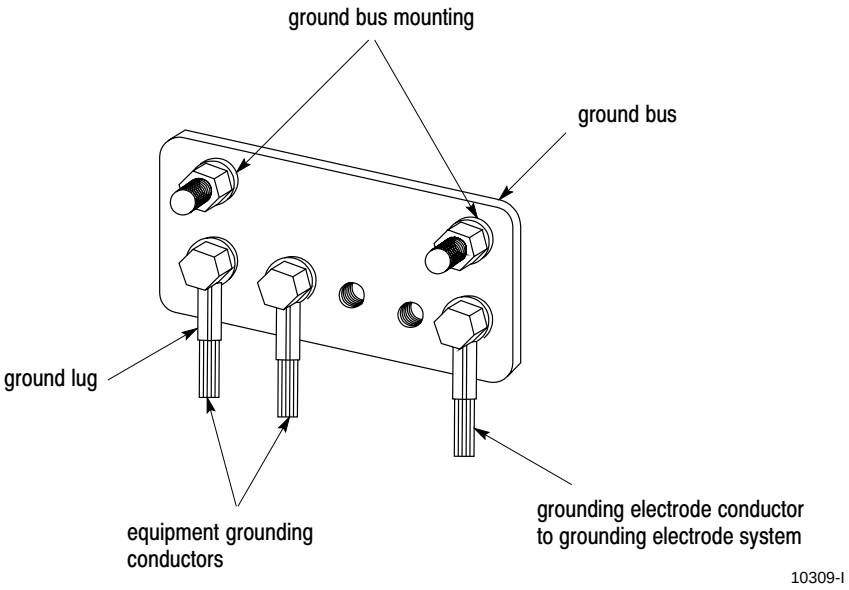
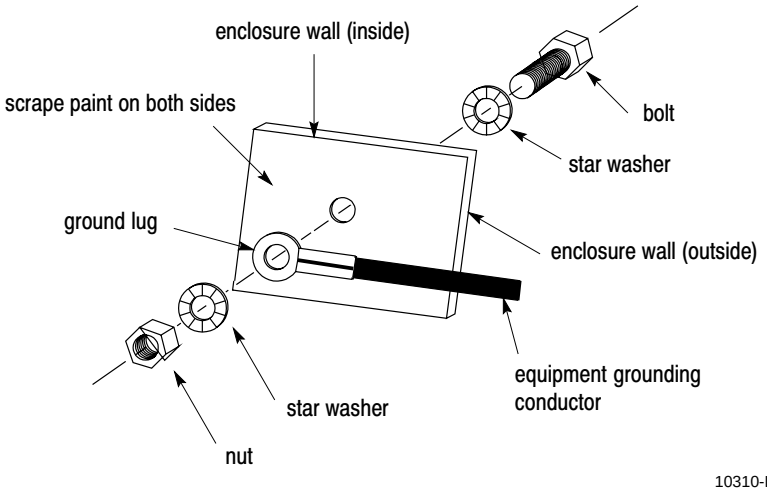


Figure 4.11
Details of Ground Connection at Enclosure Wall



Connect an equipment grounding conductor directly from each chassis to an individual bolt on the ground bus (Figure 4.12). For those chassis with a ground stud, use the ground stud for this connection. For those chassis with no ground stud, use a mounting bolt.

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If the power supply has its own groundable chassis, do not connect the GND terminal of the power supply. However, when you connect power to a power supply without a groundable chassis of its own (such as an ac-input power-supply module), you must also use 12 AWG copper wire to connect its GND terminal to the ground stud or mounting bolt connected to the ground bus (Figure 4.12).

Do not lay one ground lug directly on top of the other; this type of connection can become loose due to compression op f the metal lugs. Sandwich the first lug between a star washer and a nut with a captured star washer. After tightening the nut, sandwich the second lug between the first nut and a second nut with a captive star washer (Figure 4.12).

Grounding-Electrode Conductor

Connect the ground bus to the grounding-electrode system through a grounding-electrode conductor. The grounding-electrode system is at earth-ground potential and is the central ground for all electrical equipment and ac power within any facility. Use 8 AWG copper wire minimum for the grounding-electrode conductor to guard against EMI. The National Electrical Code specifies safety requirements for the grounding-electrode conductor.

Shielded Cables

Certain connections require shielded cables to help reduce the effects of electrical noise coupling. Ground each shield at one end only. A shield grounded at both ends forms a ground loop which could cause faulty processor operation.

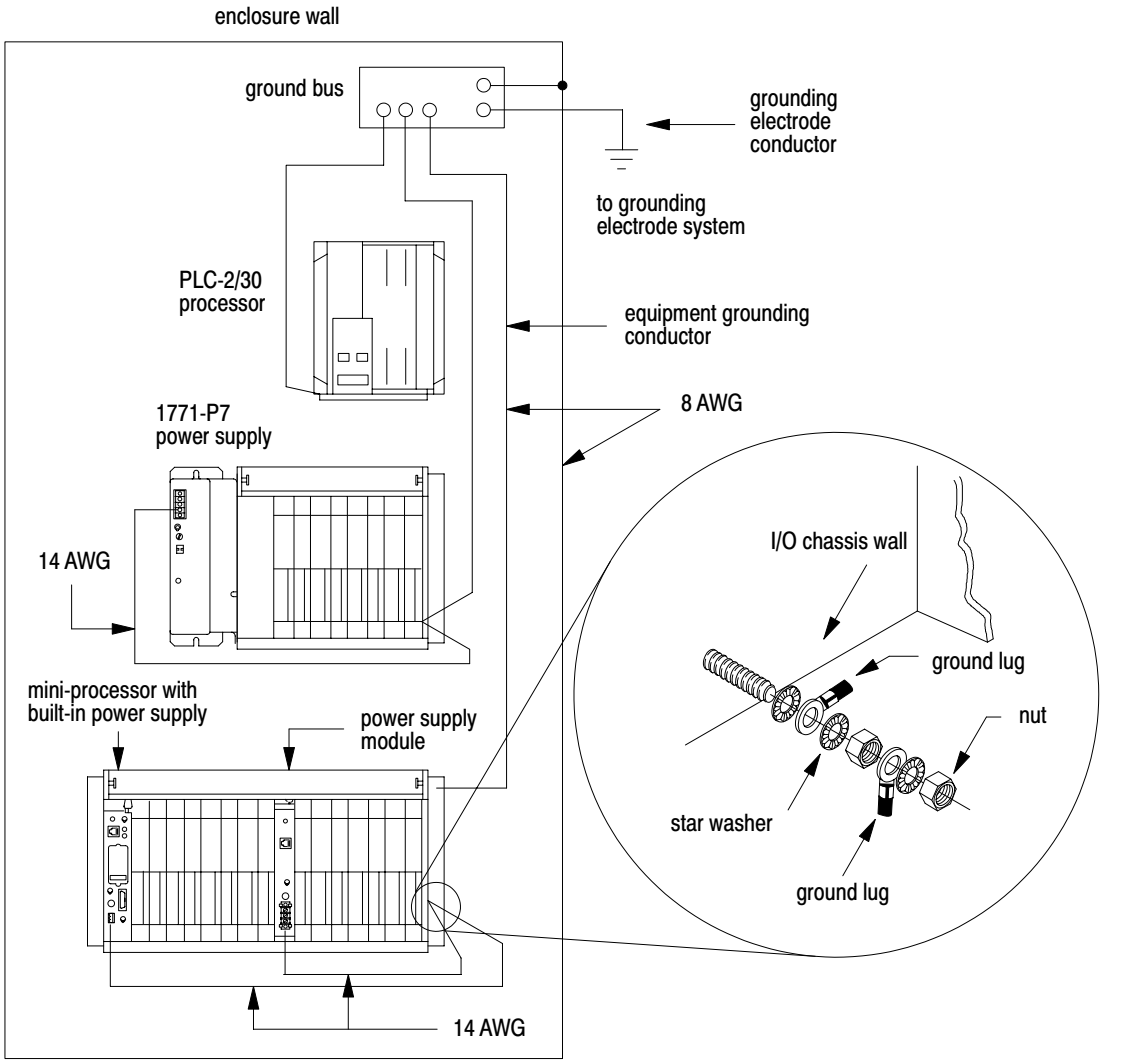
Ground each shield at the end specified in the appropriate publication for the product.

Avoid breaking shields at junction boxes. Many type of connectors for shielded conductors are available from various manufacturers. If you do break a shield at a junction box:

- Connect only category-2 conductors in the junction box.
- Do not strip the shield back any further than necessary to make a connection
- Connect the shields of the two cable segments to ensure continuity along the entire length of the cable.

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Figure 4.12
Grounding Configuration (Typical)



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Step 3 – Setting the Switches within the Switch Group Assembly

Figure 4.13
Locating Switch Group Assembly on the Backplane of an I/O Chassis

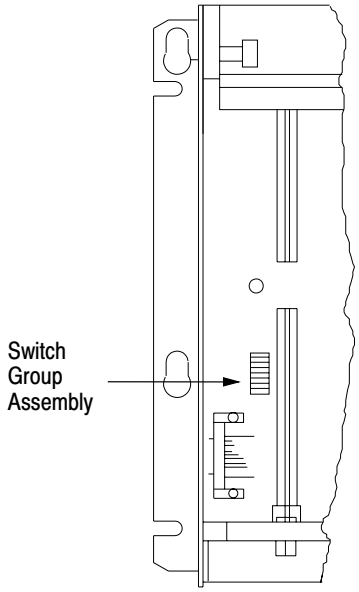


Table 4.C and Table 4.D explain how each switch is used by the processor. Switches 2 and 3 are not used. Use a ball-point pen to set each switch. Do not use a pencil because the tip can break off and jam the switch.

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Table 4.C
Set Switches 1, 4, 5 and 8

If you want:	Then set:	And
Outputs to remain in their last state when a fault (red LED in ON) is detected [1]	Switch 1 ON	--
Outputs to de-energize when a fault (red LED is ON) is detected [1]	Switch 1 OFF	--
2-slot addressing [2]	Switch 4 OFF	Switch 5 OFF
1-slot addressing [3]	Switch 4 OFF	Switch 5 ON
1/2-slot addressing [4]	Switch 4 ON	Switch 5 ON
RAM memory protect disabled	Switch 8 OFF	--
RAM memory protect enabled [5]	Switch 8 ON	

[1] Last state switch only on PLC-2/16 and -2/17 series C or later, and PLC-2/02 series A or later.

[2] When using 2-slot addressing and 8-pt. I/O modules: a 16-slot chassis equals one rack which can address 128 I/O. See chapters 5 and 7.

[3] When using 1-slot addressing and 16-pt. I/O modules: a 16-slot chassis equals two racks which can address 256 I/O. See chapters 5 and 7.

[4] When using 1/2-slot addressing and 16-pt. I/O modules: a 16-slot chassis can address four racks which equals 512 I/O. See chapters 5 and 7.

[5] When memory protect is enabled, you can only change the status and value of the bits in the first 128 words (word addresses up to 177_8) of the data table.

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Table 4.D
Set Switches 6 and 7

If	And	Then
Without and EEPROM installed in your processor		
Switch 6 is OFF	Switch 7 may be either ON or OFF	With a battery installed and a program stored in RAM memory, your processor powers-up in the mode identified by the position of the mode select switch. If the mode select switch is in the RP position, the processor will power-up in the remote program mode. Without a battery installed and without a program stored in RAM memory, your processor powers-up in the program mode or remote program mode (depending on the keyswitch position) and a `PROCESSOR MEMORY INVALID` message appears on the 1770-T3 terminal.
Switch 6 is ON	Switch 7 may be either ON or OFF	If the mode select switch is in RP position with valid memory, the processor powers up in the same mode (run/program, remote test or remote test or remote program) that it powered down in. If the switch is not in the R/P position, then the power up mode is determined by the position of the switch (run or program).
If	**And**	**Then**
With an EEPROM installed in your processor		
Switch 6 is OFF	Switch 7 may be either ON or OFF	Contents of the EEPROM memory module area transferred to RAM memory whether or not RAM memory is valid. If switch 6 is OFF, your processor powers-up in the mode selected by the keyswitch. 2
Switch 6 is ON	Switch 7 is ON	Contents of the EEPROM memory module are not transferred to RAM memory is RAM memory is valid. 1 Contents of the EEPROM memory module are transferred to RAM memory if RAM memory is not valid. 2
Switch 6 is ON	Switch 7 is OFF	With a battery installed and a program stored in RAM memory, your processor powers-up in the mode identified by the position of the mode select switch. 1 Contents of the EEPROM memory module are not transferred to RAM memory. Without a battery installed and without a program stored in RAM memory, your processor powers-up in the program mode and a `PROCESSOR MEMORY INVALID` message appears on the 1770-T3 terminal.

1 If the mode select switch is in the RP position, then the processor powers-up in the last programmed mode or operation, i.e. Run/Program, Remote Test, Remote Program.

2 If the mode select switch is in the RP position, then the processor powers-up running (RUN/PROG mode). We recommend that you put the mode select switch in the PROG position so that the processor will power-up in the program mode.

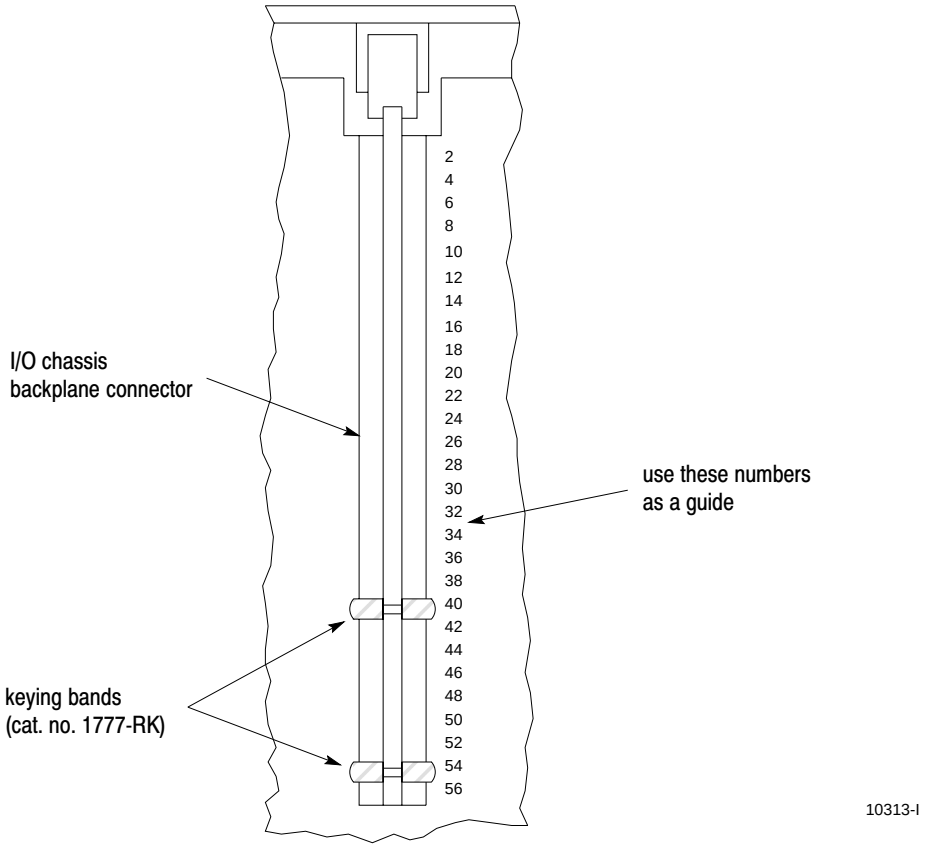
Step 4 – Installing Keying Bands and Field Wiring Arms

We ship plastic keying bands with each I/O chassis. With your fingers, insert two keying bands in the top backplane connectors of the I/O chassis. For the processor, place one keying band in the leftmost slot (Figure 4.14) between pins:

- 46 and 48
- 54 and 56

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Figure 4.14
Place the Keying Bands on the Backplane of the I/O Chassis



Use the numbers to the right of the backplane socket as a guide when positioning the keying bands.

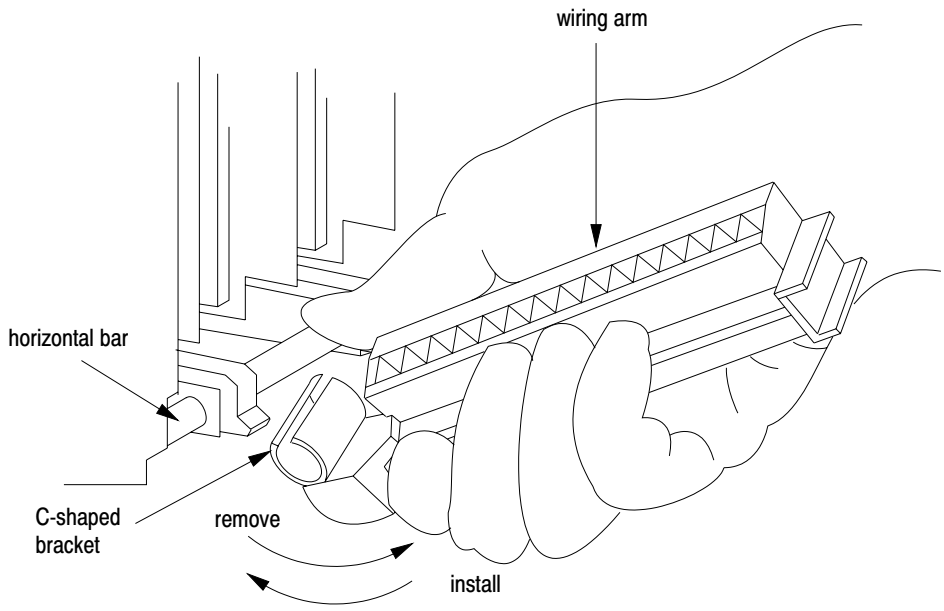
See the installation instructions for the keying position of each I/O module. Do not place any I/O modules in the left-most slot. Your processor goes there.

ATTENTION: If keying bands (in general) are not installed, a module inserted into a wrong slot could be damaged by improper voltages connected through the wiring arm. Short circuits on the I/O module can result from misalignment if keying bands are not installed.

Snap each field wiring arm onto the lower horizontal bar of the I/O chassis (Figure 4.15). When I/O modules are in place, the field wiring arm pivots and connects to the module.

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Figure 4.15
Snap the Field Wiring Arm onto the I/O Chassis

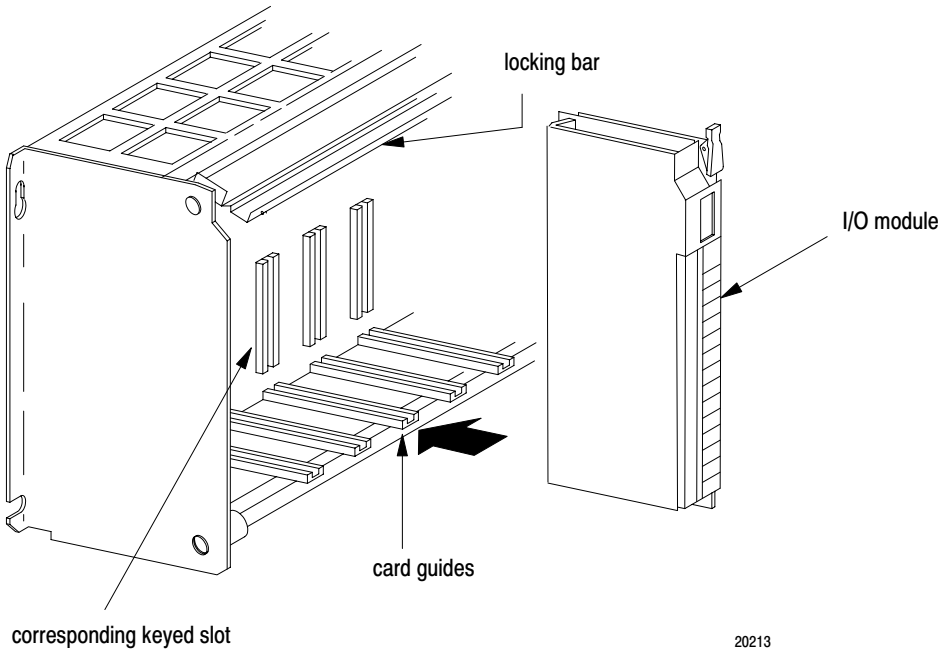


Step 5 – Installing I/O Modules

Insert each I/O module into its properly keyed slot by sliding it onto the plastic tracks of the I/O chassis (Figure 4.16). Snap the module locking latch over the I/O module.

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Figure 4.16
Place Each I/O Module into its Corresponding Keyed Slot in the I/O Chassis



ATTENTION: Do not force and I/O module into a backplane connector. Forcing an I/O module can damage the backplane connector or the I/O module.

Calculate the total current requirement for all installed modules to ensure that the sum does not exceed the limit of the I/O chassis' power supply. The 1772-LWP, -LXP, and -LZP processor provides 4A to power the I/O modules. If you need additional power, you can choose either a 1771-P3 or 177-P4 power supply module to parallel to the 1772-LWP, -LXP, -LZP:

Catalog Number	Input Voltage	Current to the Backplane
1771-P3	120V ac	3A
1771-P4	120V ac	8A
1771-P5	24V ac	8A
1771-P7	120/220V ac	16A

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ATTENTION: We recommend that you use the following series of modules when using slot-mounted power supplies:

- Isolated ac (120V) Output Module (1711-OD) series C
- Isolated ac (220V) Output Module (1771-OR) series B
- Contact Output Module (1771-OYL, -OZL, or -OW)

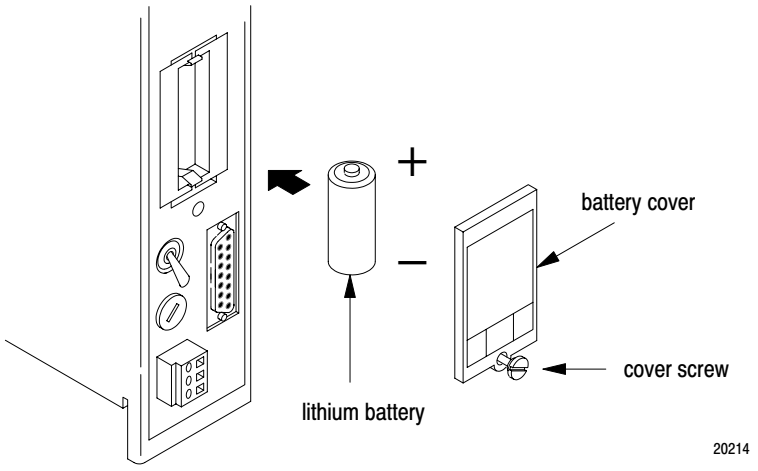
These modules are compatible with the "soft-start" feature of slot-mounted power supplies. Outputs of certain discrete modules may momentarily change operating state during power-up or power-down period, which may cause damage to equipment and injure personnel.

Updates to the latest series modules are available for the 1771-OD series A or B, 1771-OR series A, and 1771-OY series A. The 1771-OZ series A or B must be replaced by the 1771-OYL, 177-OZL, or 1771-OW.

Step 6 – Backup Battery

We recommend that you replace the internal lithium battery every year. Leave the processor turned on when you replace the battery. If you turn off the processor and replace the battery, you may lose the CMOS RAM memory.

1. Remove the screw that secures the slotted battery cover.
2. Remove the battery cover from the processor.
3. Replace the battery in the battery holder. The positive (+) end of the battery should contact the positive (+) end of the battery holder. The negative (–) end of the battery should contact the negative (–) end of the battery holder.



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4. Replace the battery cover.

5. Tighten the screw.

How to Dispose of the Battery

Batteries should be collected for disposal in a manner to prevent short circuiting, compacting, or destruction of case integrity and hermetic seal.



ATTENTION: Do not incinerate or dispose of lithium batteries in general trash collection. Explosion or violent rupture is possible.

For disposal, batteries must be packaged and shipped, in accordance with transportation regulations, to a proper disposal site. The U.S. Department of Transportation authorizes shipment of "lithium batteries for disposal" by motor vehicle only in regulation 173.1015 of CFR49 (effective Jan. 5, 1983). For additional detailed information, contact:

U. S. Department of Transportation
Research and Special Programs Administration
400 Seventh Street, S.W.
Washington, D.C. 20590

Although the United States Environmental Protection Agency at this time has no regulations specific to lithium batteries, the material contained in the battery may be considered toxic, reactive, or corrosive. The person disposing of the material is responsible for any hazard created in doing so. State and local regulations may exist regarding the disposal of these materials.

Step 7 – Installing the EEPROM Memory Module

If you have a processor with a power supply, start at step 1. If you have a processor without a power supply, turn off power to the chassis and start at step 5.

1. Move the POWER switch to the off position.

2. Turn off the incoming power source to the processor and chassis

3. Unplug the power cable

4. Lift the latch of the I/O chassis that holds your processor.

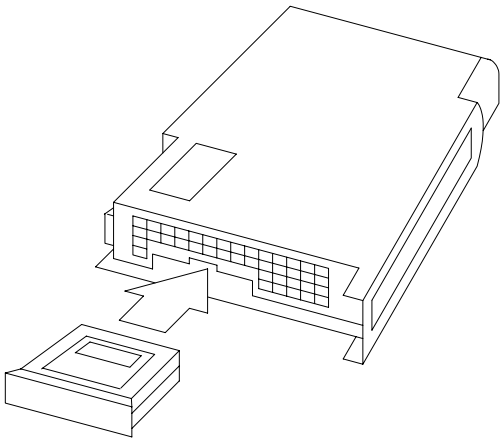
5. Slide the processor out of the I/O chassis.

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6. Place the processor on a clean flat surface with the bottom of the module facing you.

7. Position the EEPROM memory module in the memory module slot with its label facing upward. Insert and press firmly for proper connection (Figure 4.17).

Figure 4.17
Inserting the EEPROM Memory Module into the Processor



10316-I

8. Slide the processor into the I/O chassis.

9. Secure the I/O chassis latches.

10. Connect the power cable.

11. Apply power to the processor

How to Remove the EEPROM

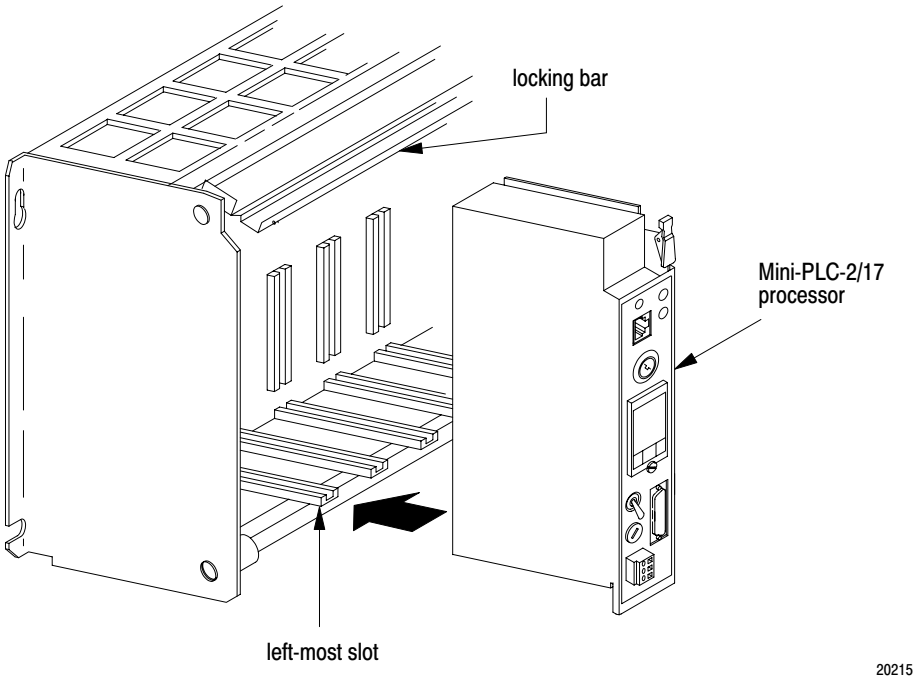
Repeat steps 1 through 4 from the previous procedure, then insert a coin into the slot so that it engages the lip on the EEPROM memory module. Carefully rotate the coin upward to start removing the EEPROM memory module from its slot. Grasp and remove the EEPROM memory module.

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Step 8 – Installing the Processor

Slide your processor into the leftmost slot of the I/O chassis (Figure 4.18)

Figure 4.18
Place the Processor in the Left-Most Slot of the I/O Chassis



ATTENTION: Do not place your processor in the I/O chassis without keying bands. Short circuits can result from misalignment.

Step 9 – Installing the Power Supply

Skip this step if you have a processor with a power supply and do not need additional current for your I/O modules. If you need additional current, use an ac powered supply because we recommend that you use the same input voltage source for two paralleled power supplies

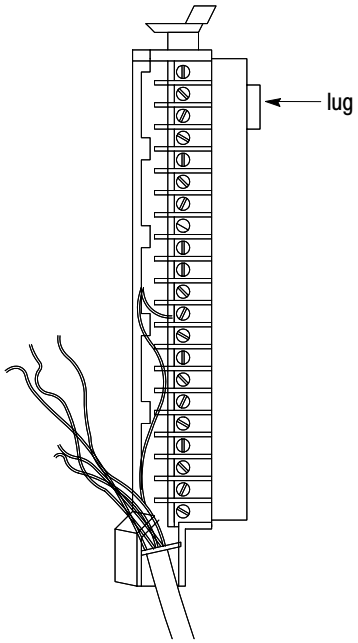
ATTENTION: Do not parallel a 1771-P5 power supply and a processor with a power supply because of power-up and power-down timing difference.

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Step 10 – Connecting to the Field Wiring Arms

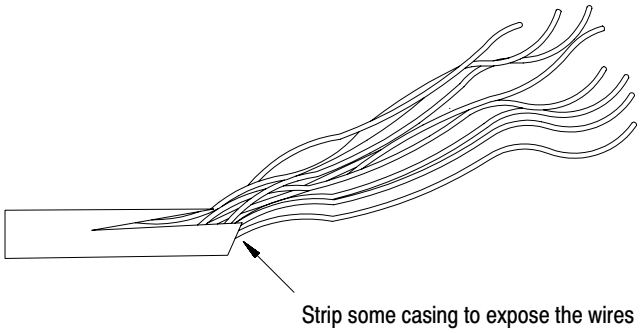
Your I/O devices connect to the I/O module's field wiring arm. Every I/O module must be properly wired and every I/O connection must be made at the proper field wiring arm terminal. Refer to the specific I/O module publication for connection diagrams. We recommend using copper wire for these connections.

1. Grasp the lug and open the terminal cover to the right.



2. Measure the wire distance from your I/O devices to the field wiring arm terminals. This distance determines the length of wire you need for your application.

3. Strip some of the outer jacket from the end of the cable that connects to the field wiring arm.

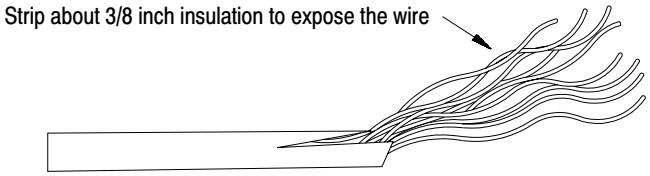


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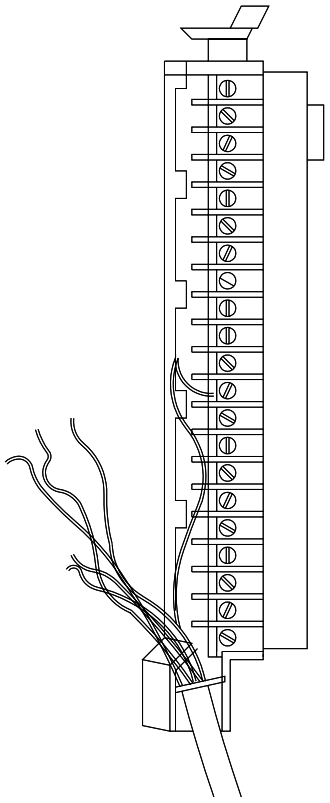
For a single-conductor wire or multi-conductor cable, perform the following steps. For a multi-conductor shielded cable, proceed to the next section (page 4-34).

Single-Conductor Wire or Multi-Conductor Cable

1. Strip about 3/8 inch insulation to expose the end of the wire



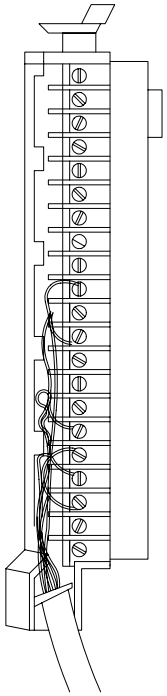
2. Loosen a terminal screw and place the wire under the pressure plate of the terminal.



3. Secure the terminal screw.

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4. Repeat steps 2 and 3 until you wire the appropriate I/O devices to the field wiring arm.



5. Connect the drain wire to ground.

6. Gather all wires and neatly bundle them using tie wraps.

7. Label all wires with a 5-digit I/O address code at each wire connection. Chapter 7 describes I/O addressing.

Multi-Conductor Shielded Cable

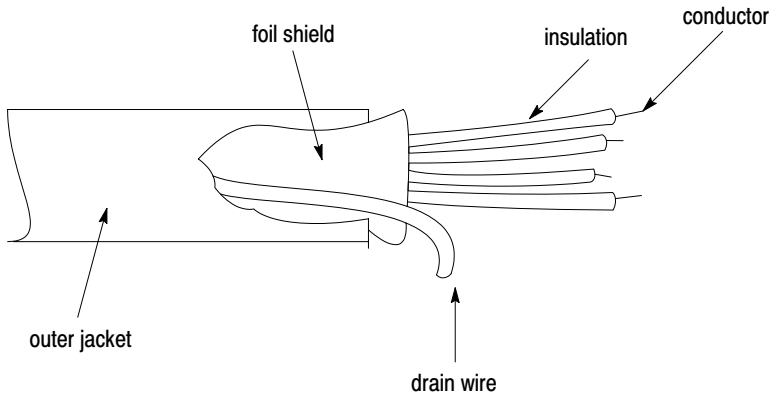
Intelligent and low-voltage dc discrete I/O modules require shielded cables that help to reduce the effects of electrical noise coupling. Ground a shield at one end only as specified in the appropriate publication for the product. A shield grounded at both ends may form a ground loop that can introduce objectionable ground currents resulting in faulty operation of the programmable controller.

Avoid breaking shields at junction boxes. If you do break a shield at a junction box, make sure that the junction box contains only low-level conductors. Also, do not strip the shield back any farther than necessary to make a connection.

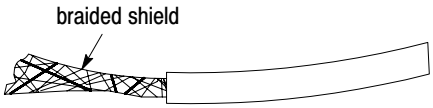
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Multi-conductor shielded cable is Belden type 8761. It consists of twisted pairs of conductor wires wrapped in two layers of shielding. Our wiring procedure shows one pair of conductor wires. The required number of I/O terminals determines the number of conductor wires needed within the cable for your application. Figure 4.19 shows each component making up this cable.

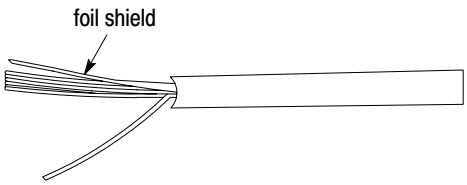
Figure 4.19
A Multi-Conductor Cable Contains these Component



1. Cut the braided shield.

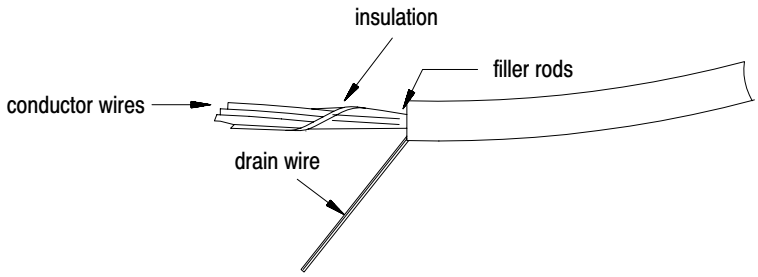


2. Remove the foil shield

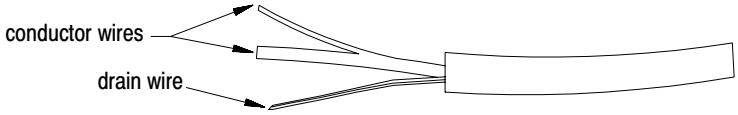


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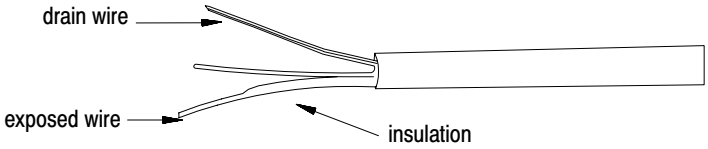
3. Cut the insulation and filler cords.



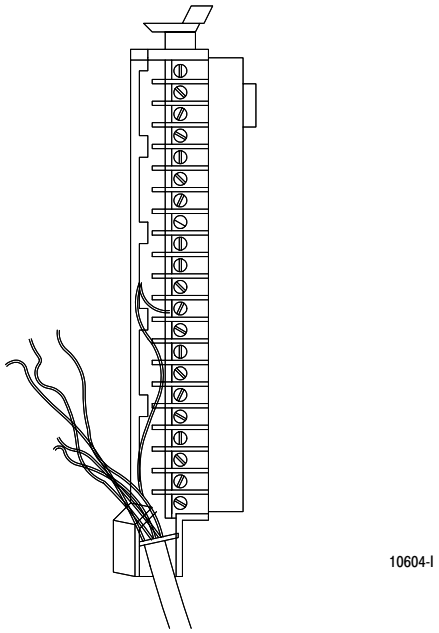
4. Fold the drain wire back to separate it from the conductor wire.



5. Strip about 3/8 inch insulation to expose the end of the wire.



6. Loosen a terminal screw and place the wire under the pressure plate of the terminal screw.



7. Secure the terminal screw.

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8. Repeat steps 6 and 7 until you wire the appropriate I/O devices to the field wiring arm.

9. Connect the drain wire to ground.

10. Gather all of your wires and neatly bundle them using tie wraps.

11. Label all of your wires with a 5-digit I/O address code at each wire connection. Chapter 7 describes I/O addressing.

12. Make sure that the field wiring arm pivots freely from vertical to horizontal.

13. Replace the field wiring arm's terminal cover.

14. Write terminal numbers on the labels next to the terminal's status indicator and on the terminal cover. These notes aid you during system start-up (chapter 5) and troubleshooting (Chapter 6).

If your application uses many shielded cables connected to one I/O chassis, then:

- provide a ground bus to connect the shielded wires
- solder several drain wires together at a field wiring arm so you route only one drain

Step 11 – Connecting Power to the Processor or Power Supply

When ac power is supplied as a separately derived system through an isolation or step-down transformer, you can connect the transformer either as a grounded or an ungrounded ac system.

If you want to connect:	Then:
a grounded ac system	connect one side of the transformer secondary to the ground bus (Figure 4.1)
an ungrounded ac system	connect one side of each test switch for the ground-fault detector lights to the ground bus (Figure 4.2)

Power supplies are designed to give an ac undervoltage signal that shuts the processor down when ac line voltage drops below a specific value (Table 4.E). Power supplies give an ac OK signal that turns the processor on when the line voltage rises above a specific value (Table 4.E). This shutdown feature helps keep invalid data out of memory.

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Table 4.E
Processor Operate and Shutdown Voltages

If the line voltage	On this system		The processor should
	120V	220V	
drops below	92V	184V	shutdown
increases to	97V	194V	start to operate

You provide the appropriate power cable to connect a processor with a power supply (1771-P3, -P4, -P5 power supplies) to its terminal strip. A processor without a power supply receives its power from the backplane of the I/O chassis.

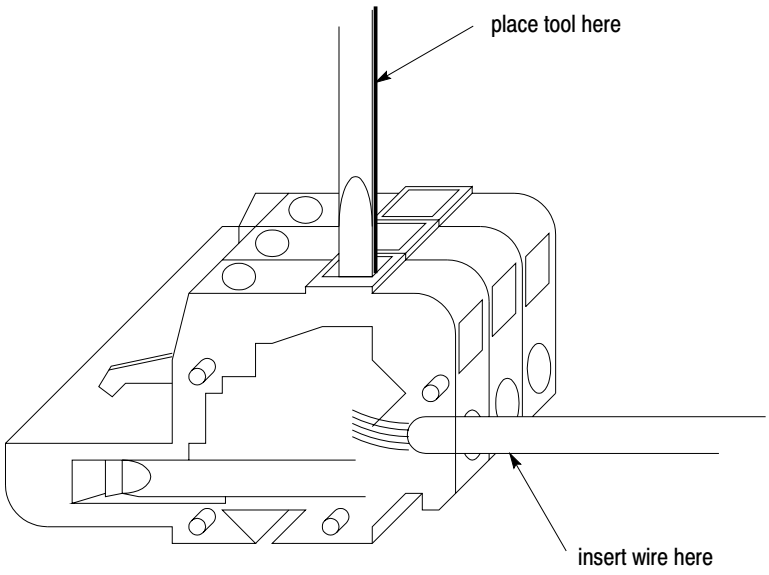
To connect the wires to the processor power plug or power supply terminal strip, do the following:

Connecting the Processor

1. Strip 3/32 inch insulation from the end of the wire.
2. Insert screwdriver (tip should be no greater than 3/32 inch wide) into the square opening.
3. Press down with the screwdriver. Figure 4.20 shows a top view of the power plug.
4. Insert the wire into the round opening on the front of the plug.
5. Remove screwdriver.

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Figure 4.20
Top View of the ac Power Plug



Connecting a Power Supply

To connect the wires to the 1771-P3, -P4, or -P5 power supplies do the following:

1. Strip 3/8 inch insulation from the end of the wire. Figure 4.21 shows an ac powered 1771-P3 or -P4 power supply. Figure 4.22 shows a dc powered 1771-P5 power supply.

2. Loosen each terminal screw and place the appropriate wire under it (Figure 4.21).

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Figure 4.21
Connect Your Power Cable to the ac Power Supply's Terminal Strip

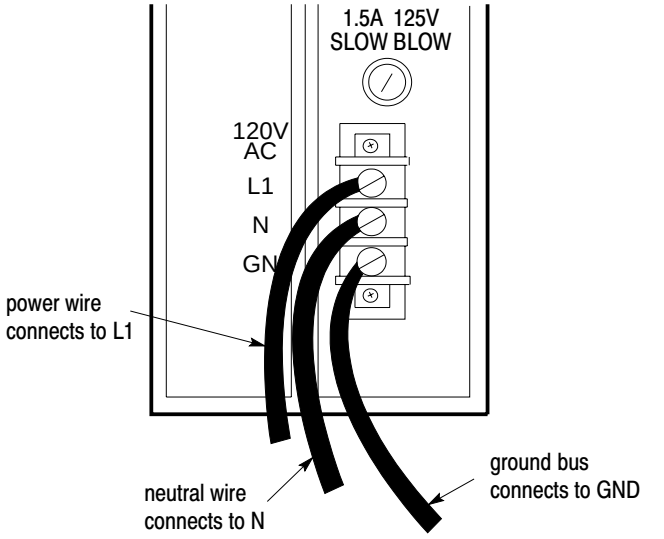
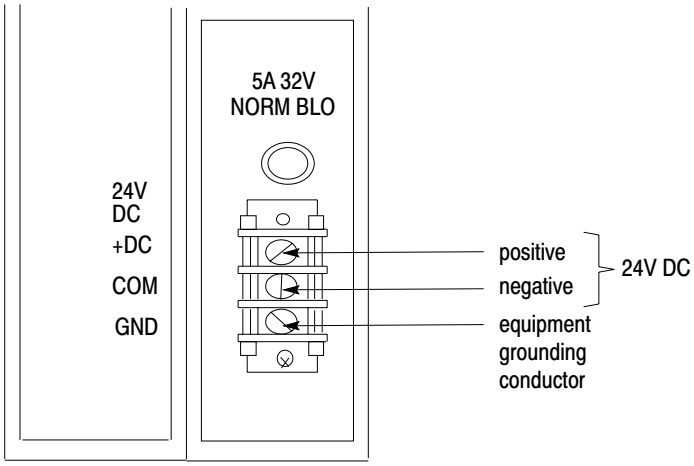


Figure 4.22
Connect Your Power Cable to the dc Power Supply's Terminal Strip



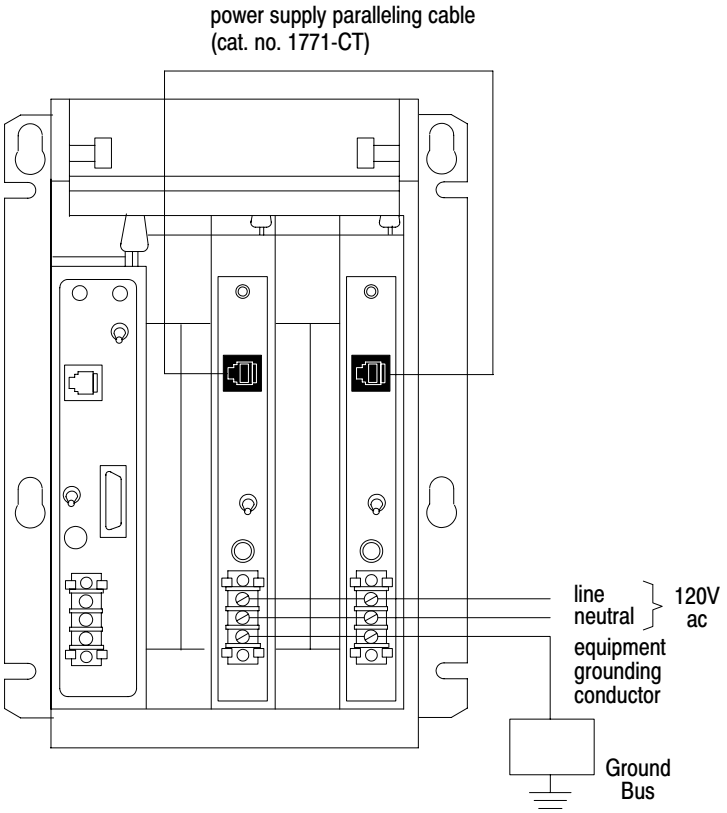
Connecting More Than One Power Supply

When you use two power supplies (Figure 4.23) connect the:

- paralleling cable between each power supply
- incoming power source to that terminal strips of the power supplies

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Figure 4.23
Connecting More Than One Power Supply



When wiring a 1771-P3 module, connect GND to the ground stud. No. 14 AWG is recommended.

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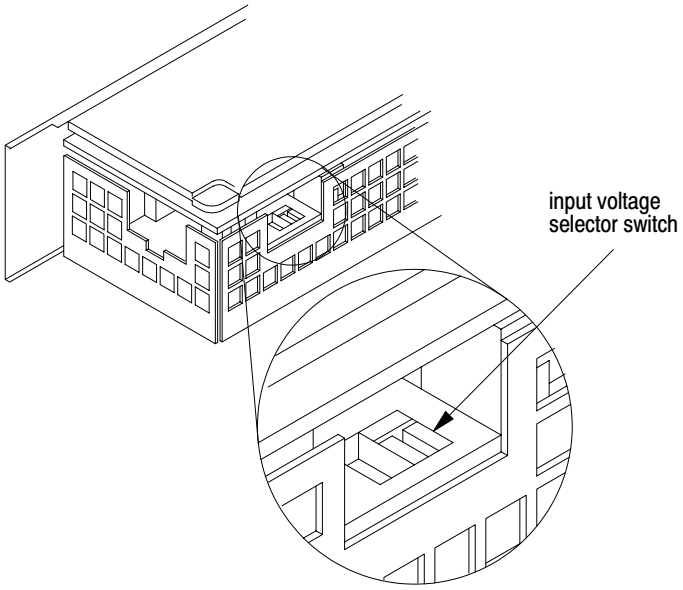
To easily remove your I/O modules that are between the two power supplies, place the paralleling cable across the top of the I/O chassis (Figure 4.23).

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Setting the Input Voltage Selector Switch

The processors can operate on 120 or 220 V ac. Select the required operating voltage by setting the Input Voltage Selector Switch at the rear of the processor (Figure 4.24). The processor is shipped set for 120V operation.

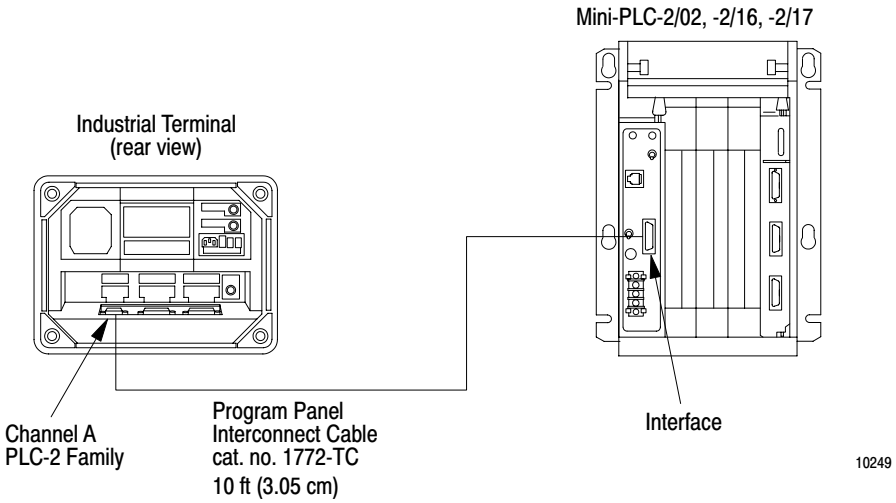
Figure 4.24
Location of the Input Voltage Selector Switch



Step 12 – Connecting the Industrial Terminal

To connect your 1770-T3 terminal to the processor refer to Figure 4.25.

Figure 4.25
The Connections between an Industrial Terminal and a Processor



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1. Turn the power switch on the front of the 1770-T3 terminal to the OFF position.
2. Plug the ac power cord into the 1770-T3 terminal.
3. If using a processor with a power supply, plug the ac power cord into the ac power source.
4. Connect one end of the 1772-TC Interconnect Cable to CHANNEL A at the back of the industrial terminal.
5. Connect the other end of the interconnect cable to the socket labeled INTFC at the front of the processor.
6. Place the PLC-2 family keytop overlay onto the keyboard.
7. Turn the power switch on the front of the 1770-T3 terminal to the ON position.
8. Turn the power switch of the processor to the ON position.
9. Press the keys [1] [1] on the industrial terminal keyboard.

Master Control Relay

In cases where unexpected machine motion could damage equipment or injure personnel, you should provide a hard-wired master control relay for emergency power shutdown. Allen-Bradley suggests you include several emergency stop switches in the master control relay circuit. When any of the emergency stop switches is opened, power to the input and output devices is removed. Power is still supplied to the system power supply so that the processor continues operation even though all of its input and output devices are powered down.



ATTENTION: Emergency stop switches can be monitored but should not be controlled by your program. Any emergency stop switch must turn off all input and output devices by removing power to the master control relay. Otherwise, it is your responsibility to provide the master control relay and emergency stop switches. You must make certain that emergency stoop switches are wired in series and are located to provide quick and easy access to the operator or maintenance personnel.

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Chapter 5

Starting Your Processor

Chapter Objectives

This chapter covers the initial start-up of your processor system. It explains how to:

- document the processor
- check the operation of your processor before supplying power
- understand hardware addressing
- start the processor system
- test the input and output devices

Verify Your System's Addresses

Verify your I/O devices' and field wiring arms' wire numbers using the Connection Diagram Addressing Worksheet (Figure 5.1).

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Figure 5.1
Connection Diagram Addressing Worksheet

ALLEN-BRADLEY
A ROCKWELL INTERNATIONAL COMPANY

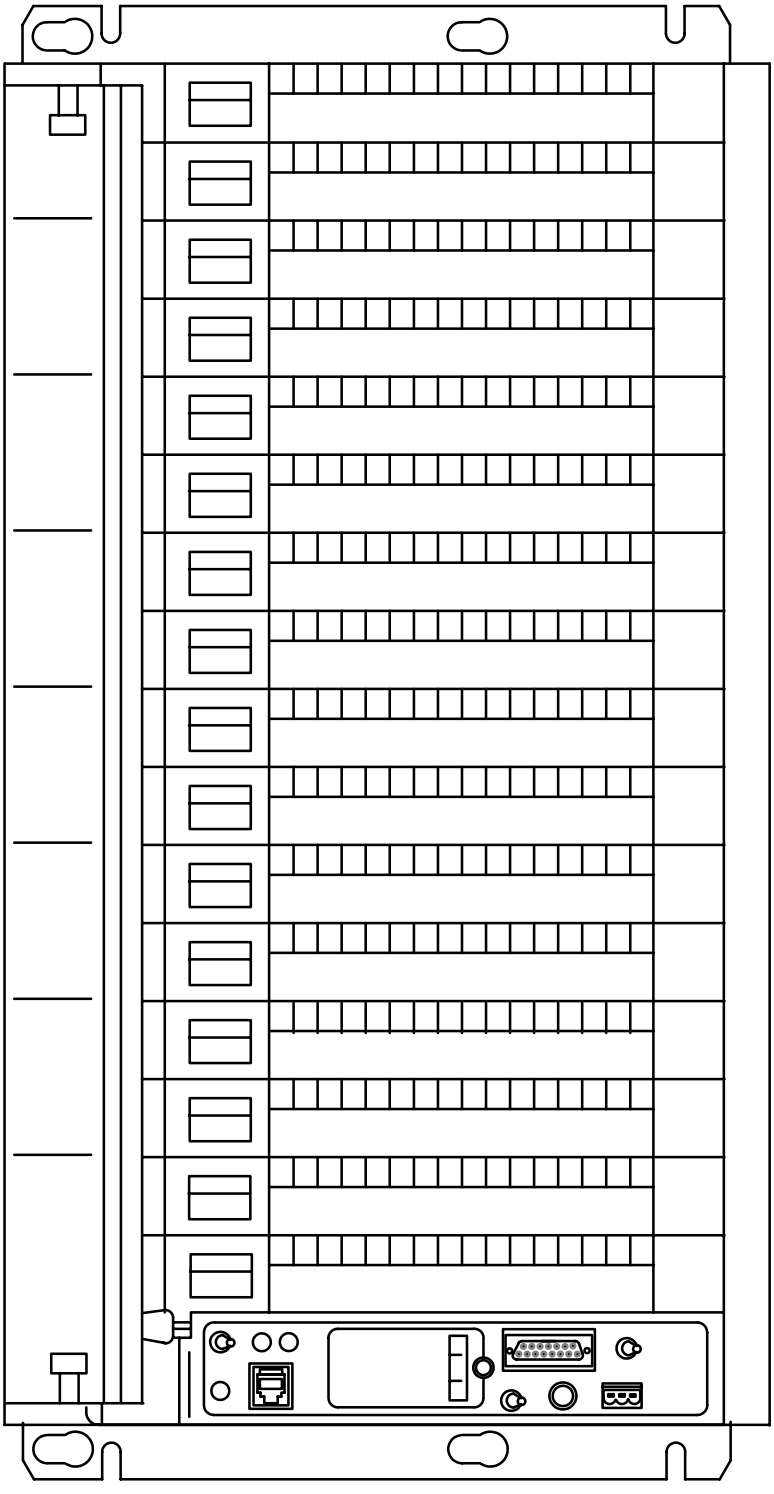
Bulletin 1771 I/O chassis
CONNECTION DIAGRAM ADDRESSING WORKSHEET
(16-point modules)

PAGE ____ OF ____

DATE ____

DESIGNER ____

PROJECT NAME ____

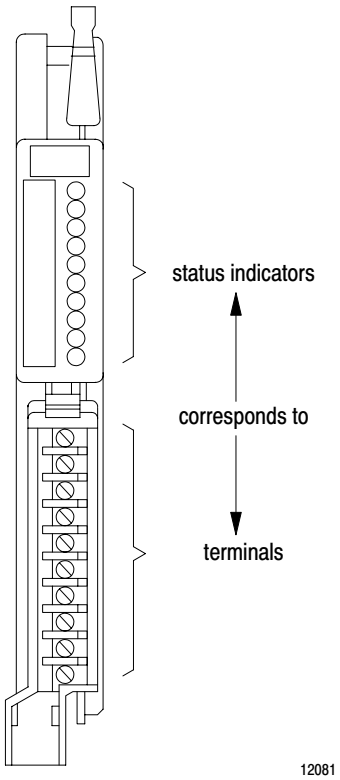


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Status Indicators for I/O Modules

Most I/O modules have status indicators on the front panel. Each indicator corresponds to a terminal on the I/O module's field wiring arm (Figure 5.2). When status indicators on input modules light, power is present at the input terminal. When status indicators on 8-point output modules light, power is present at the output terminal. When status indicators on 16- and 32-point output modules light, logic to turn on the indicator is true; this does not mean that power is present at the output terminals.

Figure 5.2
Status Indicators



Status indicators help isolate the source of a fault in your hardware. A hardware fault can originate from:

- improper I/O device operation
- wiring error
- loss of external power to the I/O module
- loss of power/signal from the I/O device

The user manual or installation instructions for each I/O module explains the operation of the module's status indicators.

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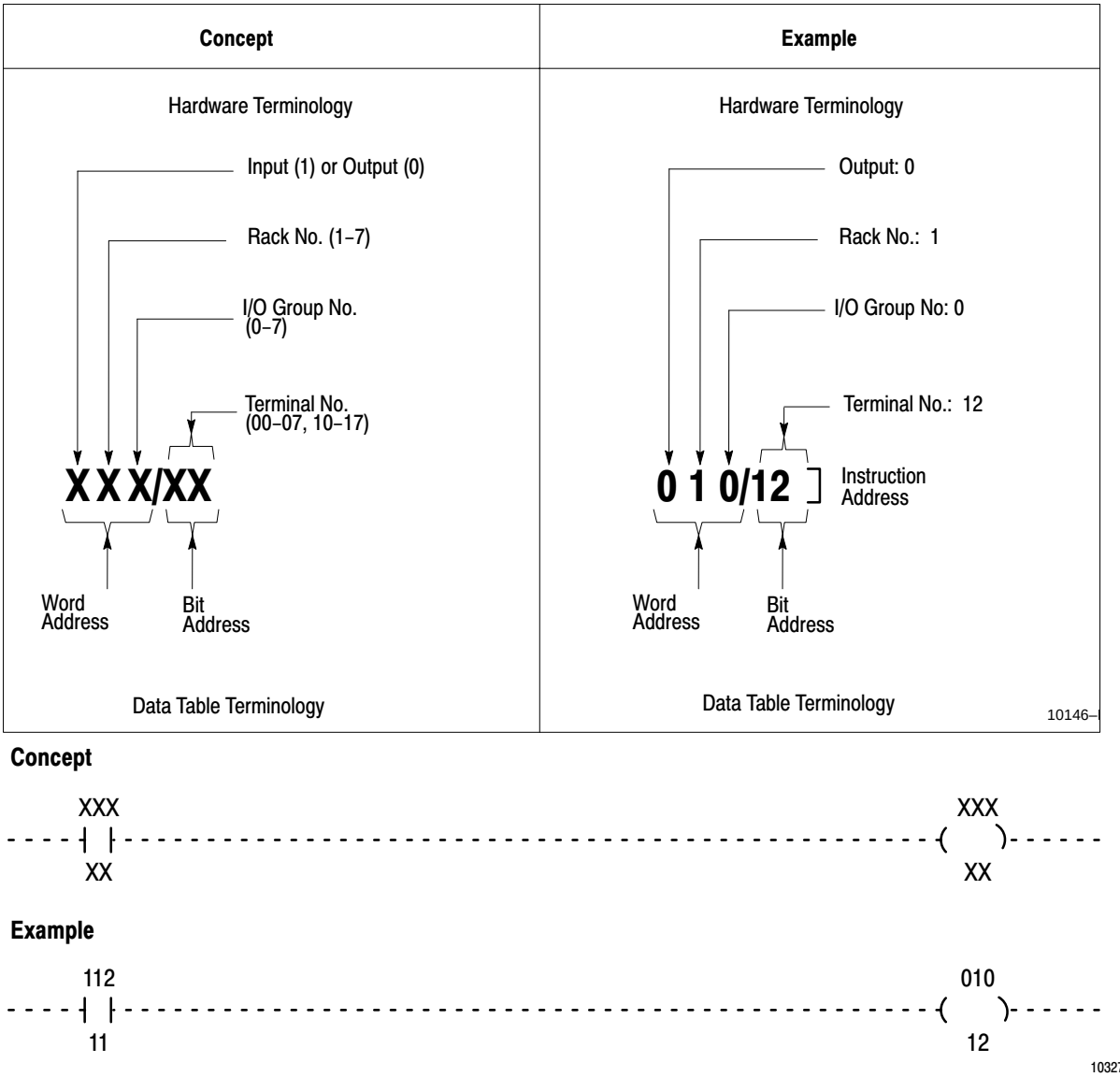
Addressing Your Hardware

You must properly address your hardware so that it relates to your ladder diagram program.

In the ladder diagram program, the input or output instruction address is associated with a particular I/O module terminal and is identified by a 5-digit address (Figure 5.3).

Addressing links a hardware terminal to a data table location (input), and links a data table location to a terminal (output).

Figure 5.3
Hardware/Data Table Addressing Relationships



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In Figure 5.3, reading from left to right, the:

- first number denotes the type of module:
  - 0 output
  - 1 input
- second number denotes the I/O rack:
  - In 2-slot addressing, the rack number is always 1.
  - In 1-slot addressing, the rack number is either 1 or 2.
  - In 1/2-slot addressing the rack number may be 1, 2, 3, or 4.
- third number denotes an I/O group (0 to 7).
- fourth and fifth numbers denote a terminal:
  - In 2-slot addressing, 00 through 07 for the left slot of the I/O group, 10 through 17 for the right slot of the I/O group.
  - In 1-slot addressing, 00 through 17 for each I/O group (slot).
  - In 1/2-slot addressing, 00 through 17 for the upper half of each I/O module (one group) and 00 through 17 for the lower half of each module (another group).

2-Slot Addressing

The processor addresses two I/O module slots as one I/O group.

Each physical 2-slot I/O group is represented by a word in the input image table and a word in the output image table. Each input terminal corresponds to a bit in the input image table word and each output terminal corresponds to a bit in the output image table word.

The maximum number of bits available for one 2-slot I/O group is 32: 16 bits in the input image table word and 16 bits in the output image table word. The type of discrete I/O module you install, either 8-point (standard density) or 16-point (high-density, used in complementary mode) determines the number of bits in the words that are used.

You select 2-slot addressing by setting switches 4 and 5 of the I/O chassis backplane switch assembly:

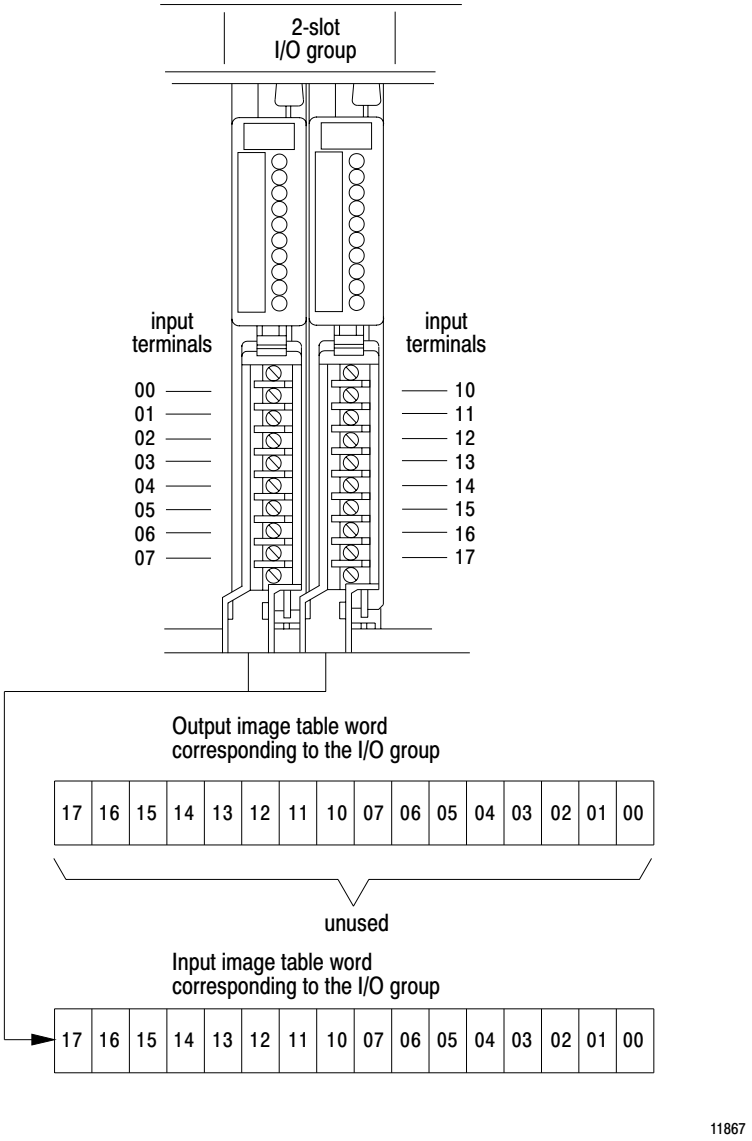
- Switch 4 to the OFF position
- Switch 5 to the OFF position

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Using 8-Point I/O Modules

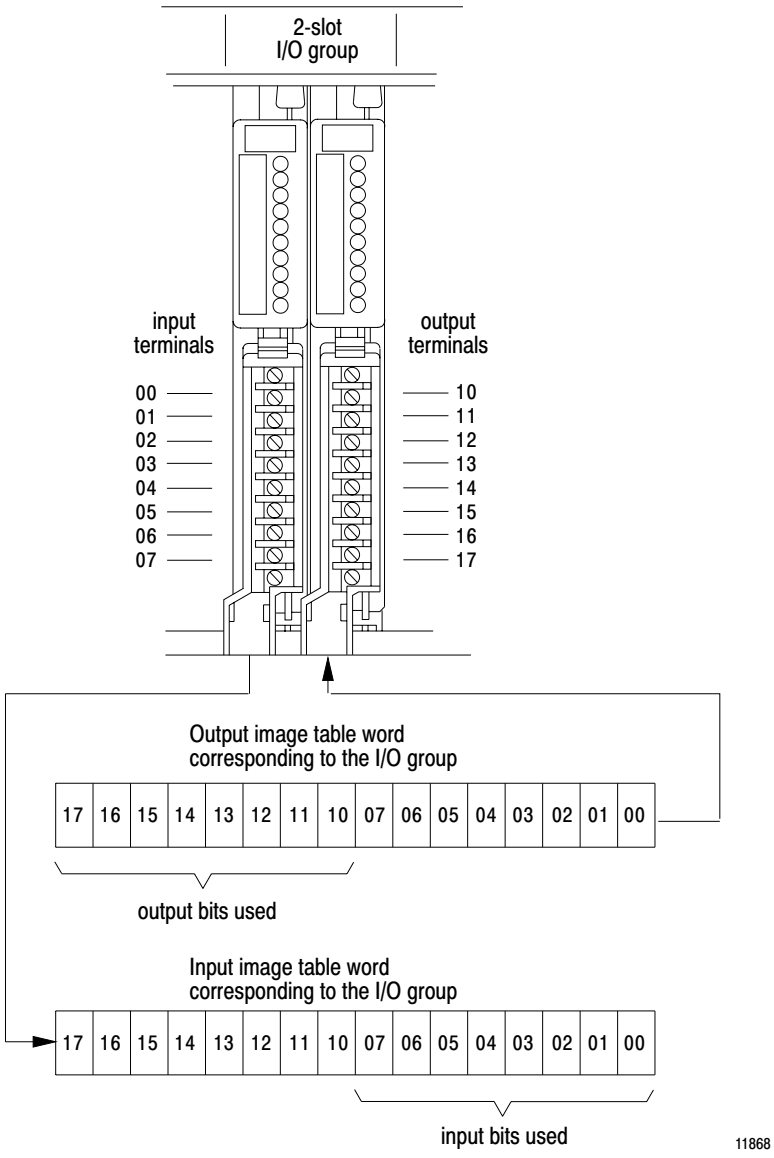
I/O modules generally provide eight input terminals or eight output terminals. Figure 5.4 illustrates the 2-slot I/O group concept with two 8-point input modules. Figure 5.5 illustrates the 2-slot I/O group concept with an 8-point input and an 8-point output module.

Figure 5.4
Illustration of 2-Slot Addressing with Two 8-Point Input Modules



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Figure 5.5
Illustration of 2-Slot Addressing with 8-point Input and Output Modules



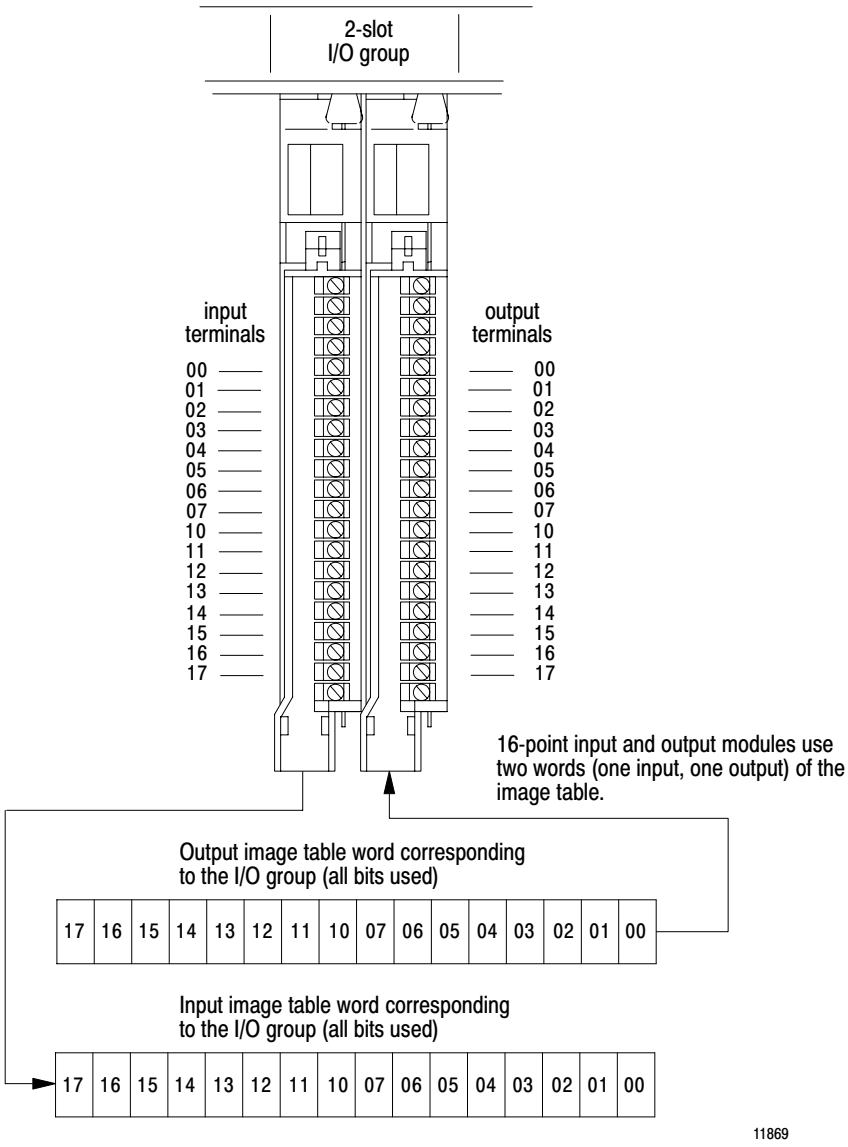
Using 16-Point I/O Modules

High-density (16-point) I/O modules provide 16 input terminals or 16 output terminals. 16-point I/O modules use a full word in the input or output image table.

Important: 16-point modules may only be used in a complimentary fashion in 2-slot addressing mode. Two 16-point modules, one input and one output, can be used in a 2-slot I/O group (Figure 5.6).

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Figure 5.6
Illustration of 2-Slot Addressing with 16-Point Input and Output Modules



Because these modules use a full word in the image table, the only type of module you can use in a 2-slot I/O group with a 16-point module is one that performs the opposite (complementary) function; an input module complements an output module and vice-versa.

You can use an 8-point module with a 16-point module in a 2-slot group; however, it too must perform the opposite function. Eight bits in the I/O image table are unused.

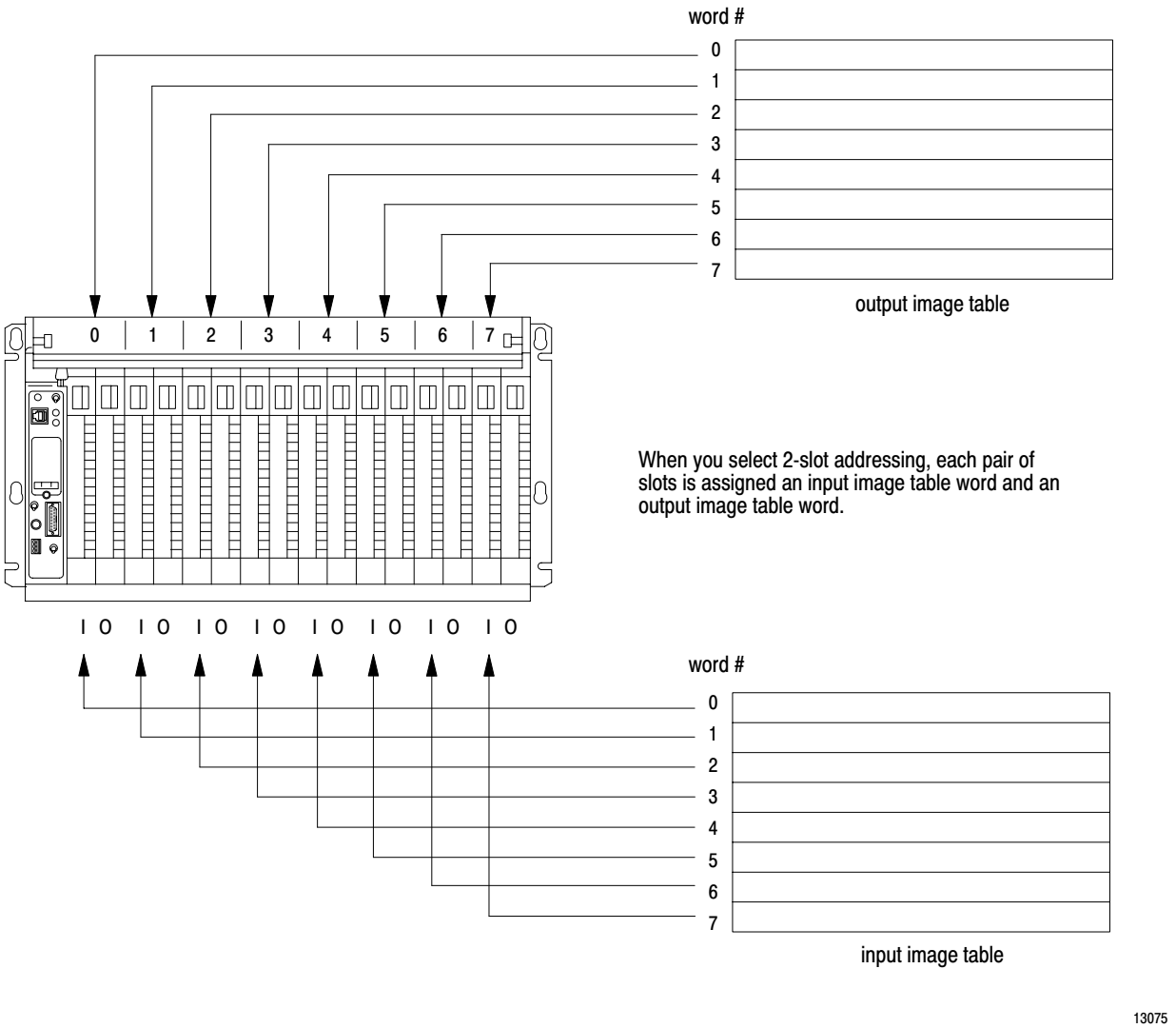
Important: 32-point modules will not work in 2-slot addressing mode.

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Assigning I/O Rack Numbers

When you select 2-slot addressing, each pair of slots (one I/O group) is assigned to the corresponding pair of words in the input and output image tables. You assign one I/O rack number to eight I/O groups (Figure 5.7).

Figure 5.7
I/O Image Table and Corresponding Hardware for One Assigned Rack Number for 2-Slot Addressing



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1-Slot Addressing

The processor addresses one I/O module slot as one I/O group.

Each 1-slot I/O group is represented by a word in the input image table and a word in the output image table. You have 16 input bits and 16 output bits available for each slot. This lets you use any mix of 8- and 16-point I/O modules in the I/O chassis in any order. 32-point modules must be used in complementary arrangements.

Important: For full compatibility with 1-slot addressing you must use the series C, revision A (or later) 1770-T3 industrial terminal.

You select 1-slot addressing by setting switches 4 and 5 of the I/O chassis backplane switch assembly:

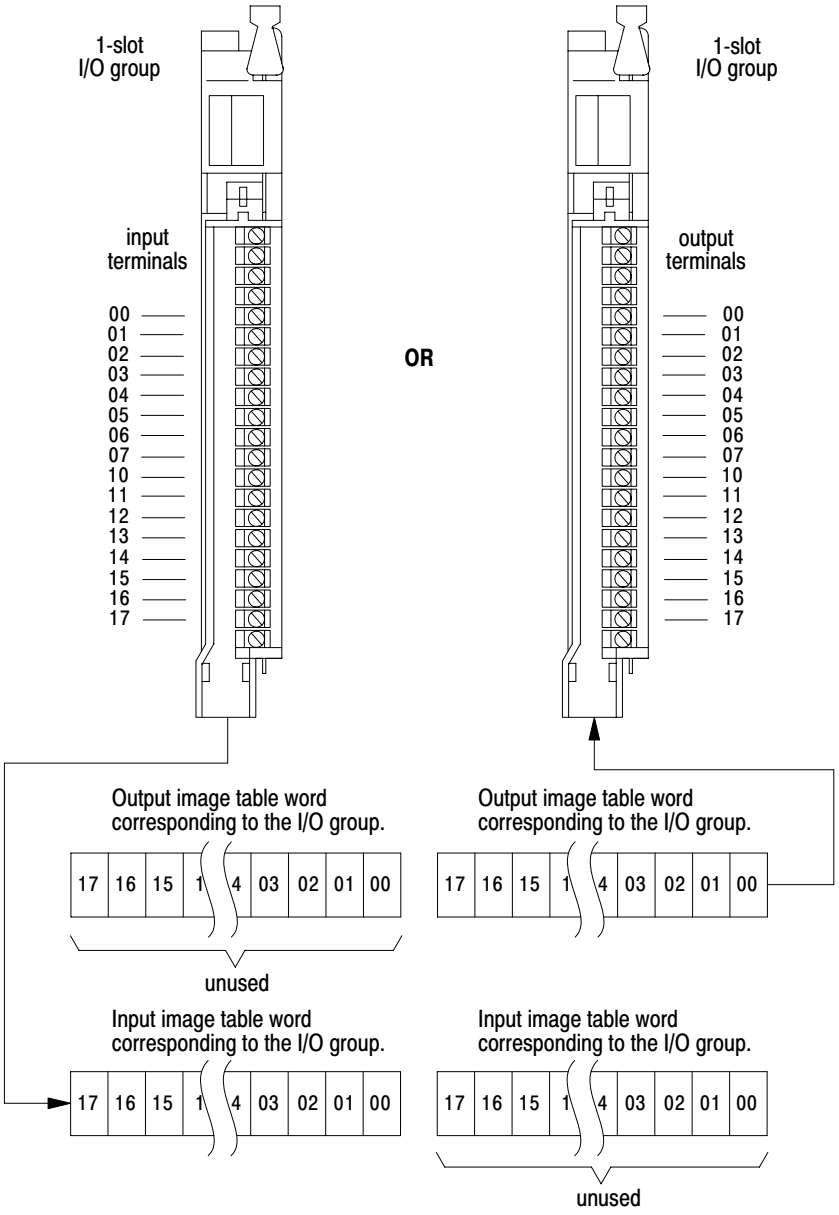
- Switch 4 to the OFF position
- Switch 5 to the ON position

The physical address of each I/O group (1-slot) corresponds to an input and an output image table word. The type of module you install (either 8-point or 16-point I/O) determines the number of bits in these words that are used.

Figure 5.8 (on the next page) illustrates the 1-slot I/O group concept with one 16-point I/O module. This module group uses an entire word of the image table. You can use an 8-point I/O module with 1-slot addressing, but the module uses only 8 bits of the I/O image table word (8 bits in the I/O image table are unused).

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Figure 5.8
Illustration of 1-Slot Addressing with 16-Point I/O Modules



The corresponding opposite image table word is not used when 16-point modules are used.

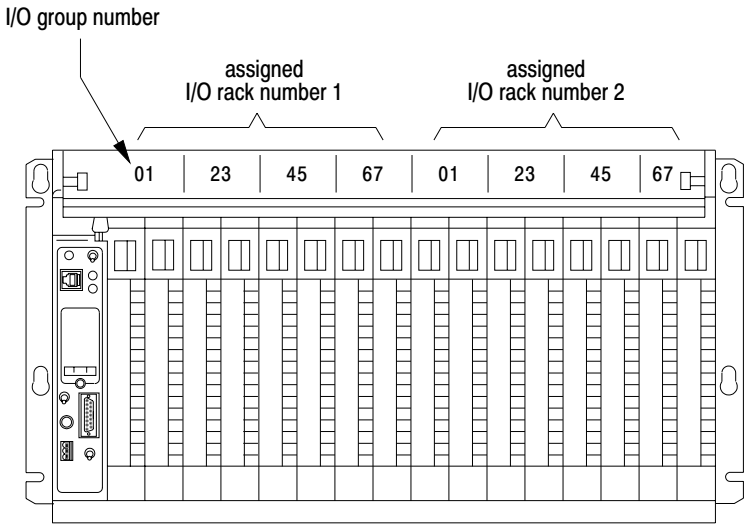
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Assigning I/O Rack Numbers

When you select 1-slot addressing, each slot is an I/O group. You still assign one I/O rack number to eight I/O groups; therefore, in a 16-slot I/O chassis you now have two I/O racks (Figure 5.9).

Figure 5.9
Assigning I/O Rack Numbers with 1-Slot Addressing



1771-A4B I/O chassis using 1-slot addressing.

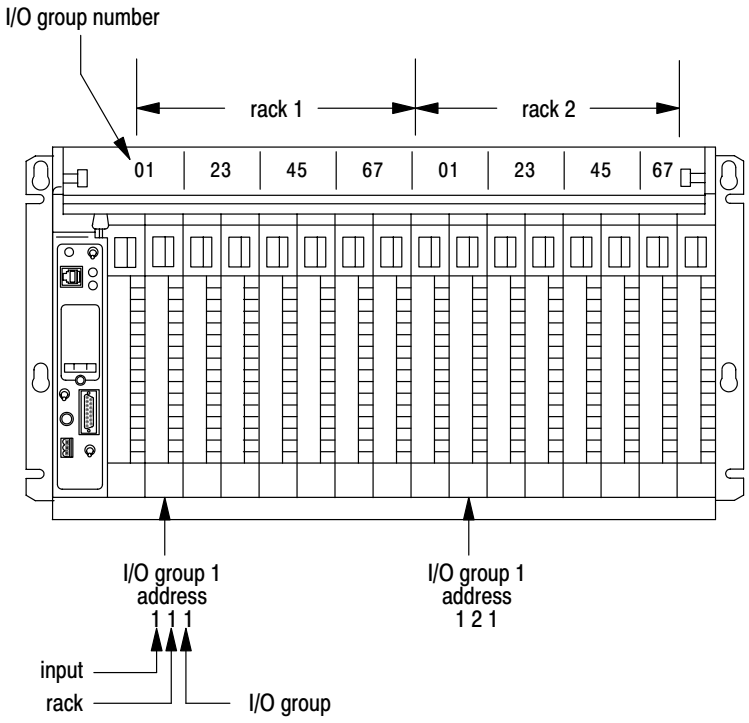
13077

In Figure 5.3, we showed how the 5-digit input or output instruction is associated with a particular I/O module terminal. With two I/O racks you use the instruction address to identify which rack you are communicating with.

Figure 5.10 illustrates addressing two modules, each in the same I/O group number but in different assigned racks of a single I/O chassis.

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Figure 5.10
Example of 1-Slot Addressing



Using 32-Point I/O Modules

32-point I/O modules provide 32 input or 32 output terminals. 32-point I/O modules use two full words in the input or output image table. In 1-slot addressing mode, 32-point modules must be placed in a complimentary fashion; a 32-point input module must be next to any output module and vice versa.

If 32-point modules are not placed in a complimentary fashion when in 1-slot addressing mode, the PROC RUN LED indicator will continuously blink green and the processor will not operate.

Important: When addressing a block transfer module, it must be addressed by the lowest group number that it occupies and at slot 0. For example: a 2-slot block transfer module in rack 1, groups 2 and 3 (slots 3 and 4) would be addressed (by rack-group-slot) at location 120.

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1/2-Slot Addressing

When you select 1/2-slot addressing, the processor addresses one-half of an I/O module slot as one I/O group. The physical address of each I/O slot corresponds to two input and two output image table words. The type of module you install (8, 16 or 32 I/O points) determines the number of bits in these words that are used.

With 1/2-slot addressing, since 32 input bits and 32 output bits are set aside in the processor's image table for each slot (16 input image table bits and 16 output image table bits times 2 groups per slot = 32 of each), you may use any mix of I/O modules (8, 16 or 32 point) in the I/O chassis.

You select 1/2-slot addressing by setting switches 4 and 5 of the I/O chassis backplane switch assembly:

- Switch 4 to the ON position
- Switch 5 to the ON position

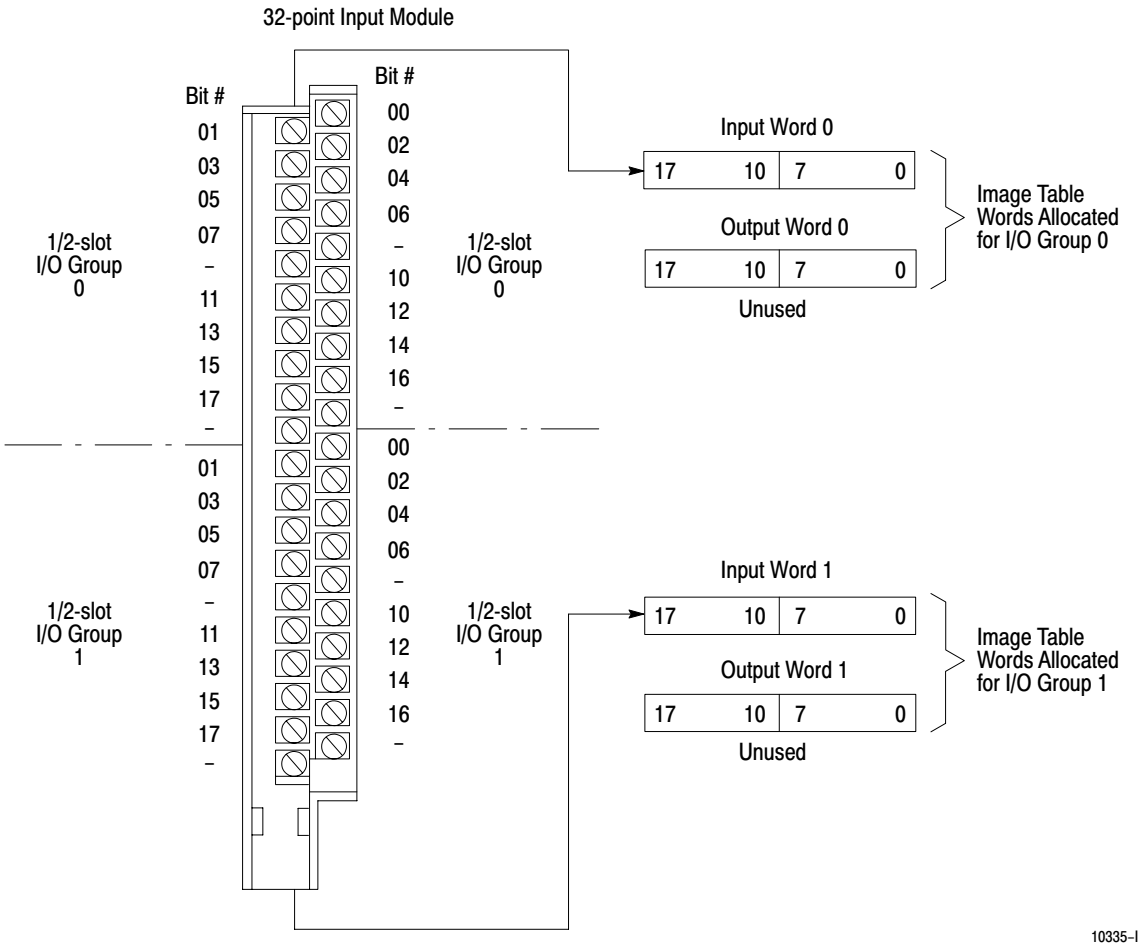
Figure 5.11 illustrates the 1/2-slot addressing concept with a 32-point I/O module. A 32-point I/O module (two 1/2-slot I/O groups) uses two input or two output words of the image table. I/O group applies to the upper 16 points; I/O group 1 applies to the lower 16 points.

You can use 8-point and 16-point I/O modules with 1/2-slot addressing but the rest of the bits are unused. They may be addressed through either I/O module group.

Important: For full compatibility with 1/2-slot addressing you must use a series C, revision B (or later) 1770-T3 industrial terminal.

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Figure 5.11
Illustration of 1/2-Slot Addressing Using a 32-Point I/O Module

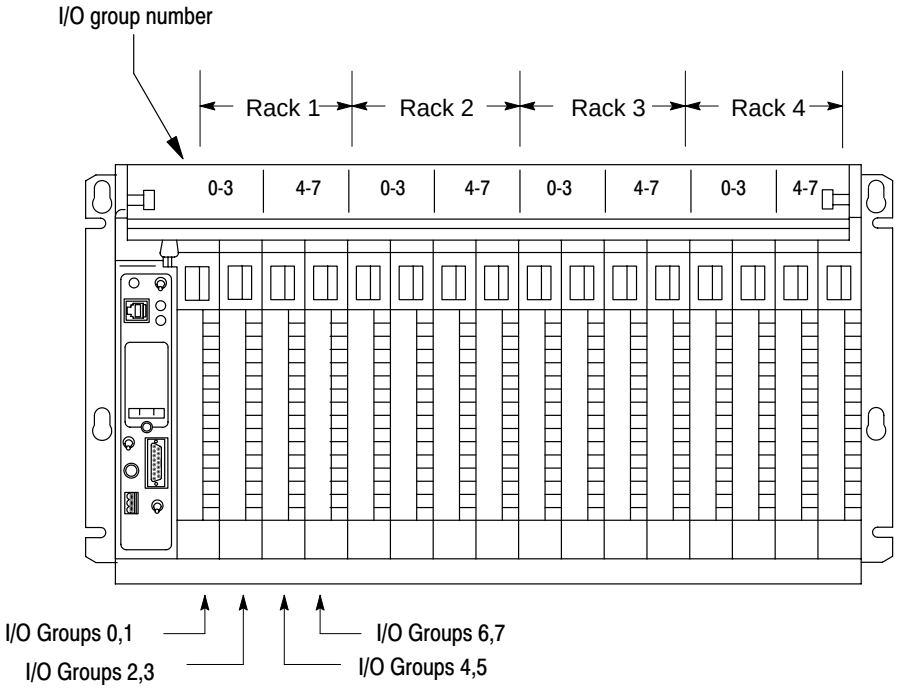


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Assigning I/O Rack Numbers

When you select 1/2-slot addressing, each slot corresponds to two I/O groups. You still assign one rack number to eight groups; however, with 1/2-slot addressing this requires only four slots. Thus, in a 16-slot chassis, you now can have four I/O racks (Figure 5.12).

Figure 5.12
Assigning I/O Rack Numbers with 1/2-Slot Addressing



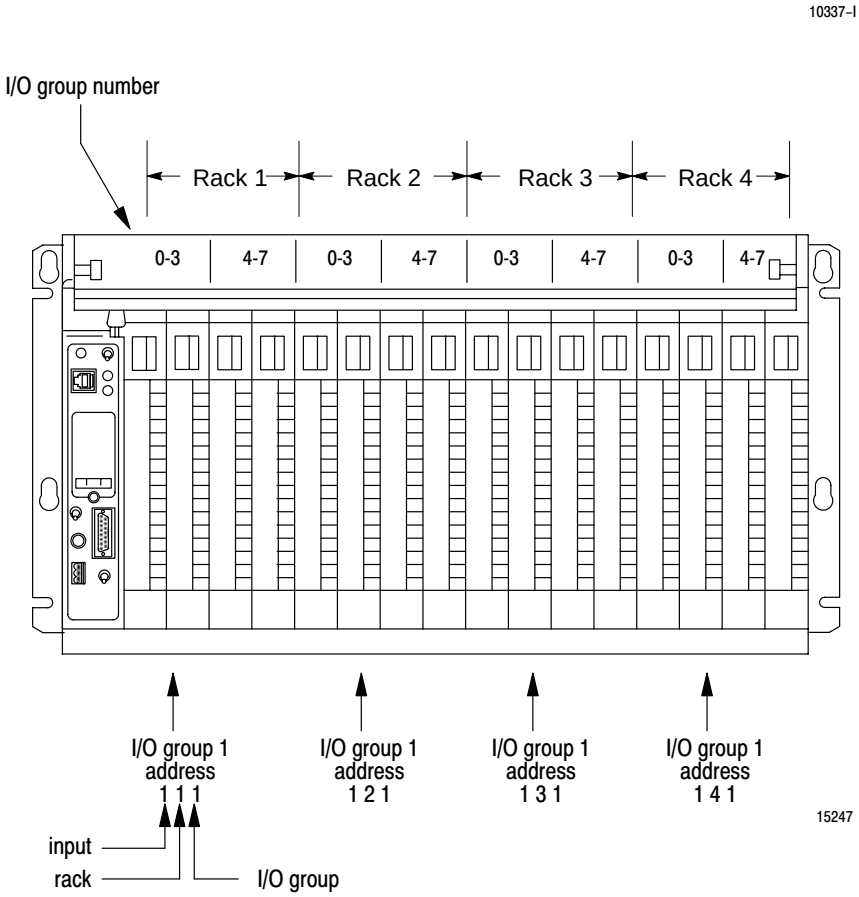
1771-A4B I/O Chassis using 1/2-slot addressing

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Figure 5.13 illustrates addressing 4 modules, each with the same I/O group number, but in the four different racks of a single I/O chassis.

Figure 5.13
Group Address of a Module in Four Different Racks



Important: When addressing a block transfer module, it must be addressed by the lowest group number that it occupies and at slot 0. For example: a 1-slot block transfer module in rack 1, groups 2 and 3 (slot 2) would be addressed (by rack-group-slot) at location 120. Be aware that this module is occupying group 2, slots 0 and 1, and group 3, slots 0 and 1.

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Before You Supply AC Power



ATTENTION: Unexpected machine motion during system start-up can damage equipment and injure personnel.

Disconnect any device that might cause machine motion to occur when it is energized.

Before you supply ac power to your processor do the following:

1. Measure the ac line voltage and make sure it corresponds to the system power supply. Verify the L1, L2 and Chassis Gnd connections
(L1 = ac high, L2 = ac return).

2. Check the wiring of:

   - main disconnect switch or circuit breaker
   - master control relay
   - emergency stop switches

3. Check the power cable connections. Make sure plugs are securely held in their sockets.

4. Check the location and chassis positioning of each I/O module. All I/O chassis latches must be snapped down. All field wiring arms must be connected with their corresponding I/O modules.

5. Disconnect all motors to ensure that no power-driven machine can start when you first apply power to the processor. Alternatively, disconnect the output device at its terminal strip.

6. Test each output point and input point of each module in accordance with the suggestions of the following sections.

Testing Output Devices

There are four ways to test output devices, using:

- a pushbutton (you supply the pushbutton)
- force functions (through the industrial terminal). (See chapter 26.)
- using the 1771-SIM switch/indicator module
- bit monitor/manipulation (SEARCH 53). (See chapter 25.)

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Using Pushbuttons

ATTENTION: Use only trained personnel to conduct this test. Have a trained person at appropriate emergency stop switches to de-energize output devices that could cause hazardous operation.

To use a pushbutton to test your output devices, do the following:

1. Connect a normally-open/momentary-close pushbutton switch as an input device to an input module.
2. Connect the industrial terminal to your processor. (See chapter 4.)
3. Select the RUN mode of operation.
4. Use an examine-on address corresponding to the address of the pushbutton. Use an energize address corresponding to the output device being tested. For example, enter a rung similar to this one:



ATTENTION: Test only one rung at a time. Do not program multiple rungs; unpredictable machine operation can occur.

5. Close the pushbutton switch and see if the input and output address instructions are intensified
6. If the output instruction is not intensified, verify your test setup and the input address.
7. Make sure that the output module's status indicator lights. If the indicator lights, repeat the setup procedure for another output device.
8. If the indicator does not light, check the following:

   - power source for the output device
   - I/O chassis power supply
   - connections to the field wiring arm
   - address of the output I/O module (rack, group, slot, terminal)
   - examine-on address of the pushbutton switch

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Using the 1771-SIM Module

The Switch/Indicator module is compatible with any 1771 I/O chassis. It has 8 switches to simulate 8 inputs and it has 8 LED's to indicate when an addressed output is active. It requires no external power. See publication 1771-2.106 for more information.

Testing Input Devices

ATTENTION: Use only trained personnel to conduct this test. Have a trained person at appropriate emergency stop switches to de-energize output devices that could cause hazardous operation.

To test your input devices, do the following:

ATTENTION: Do not reach into a machine to actuate a switch since unexpected machine motion can occur. Use a wooden stick or other nonconductive device to guard against electrical shock. Failure to observe this warning may injure personnel.

1. Connect the industrial terminal to your processor (see chapter 4).
2. Select the TEST mode of operation.
3. Use an examine-on address corresponding to your input device address. Use an energize-output address that is an internal storage bit. For example, enter a rung similar to this one:



4. Manually turn on one input device and observe that the input instruction is intensified and the input module's status indicator lights. If both do, repeat this procedure for another input device. Continue until all devices are tested.

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5. If the instruction does not intensify, then:

- repeat the test procedure
- check your input module
- call your Allen-Bradley sales engineer or distributor

6. If the indicator does not light, check:

- power source for the input device
- wiring from the input device
- connection to the field wiring arm's terminal
- input device
- verify the address of the input device
- input terminal

Using The 1771-SIM

The Switch/Indicator module is compatible with any 1771 I/O chassis. It has 8 switches to simulate 8 inputs and it has 8 LED's to indicate when an addressed output is active. It requires no external power. See publication 1771-2.106 for more information.

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Chapter 6

Maintaining and Troubleshooting Your Processor

Chapter Objectives

This chapter describes techniques of maintaining and troubleshooting your processor. When you have finished, you should be:

- aware of items requiring maintenance
- able to troubleshoot your processor.

General

The processor is designed to minimize the need for maintenance and troubleshooting procedures. Troubleshooting does not usually require special test equipment or programming techniques. Instead, status and diagnostic indicators on the processor help isolate the source of a fault.

Preventive Maintenance

The processor is an electrical system comprised of printed circuit boards that are vulnerable to dirt and dust. We make every effort to limit processor exposure to dust, dirt, and soot.

You should periodically inspect terminal-strip connections, plugs, sockets, and connections for tightness. Loose connections may result in permanent damage to the components.



ATTENTION: Remove system power before inspecting connections in the system. Otherwise, you could damage equipment and injure personnel.

Troubleshooting

Use a systematic approach when troubleshooting the processor to resolve a malfunction. Some problems could result in extended periods of down time if they were solved on an interim basis.

Generally, the problem sources can be grouped into three areas: hardware, processor, and programming.

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The most likely source of a problem is your hardware. This includes the wiring, I/O devices, I/O power source, and system power. You should be able to trace the source of the problem if you observe I/O device behavior and processor indicators.

The following sections deal with troubleshooting problems as they relate to your processor components. Observe all attentions. One general warning to observe is:



ATTENTION: When cycling or removing line power, always use the main disconnect switch. Never use the ac line fuse to cycle or remove line power; contact with ac can injure personnel.

Troubleshooting with an Industrial Terminal

The industrial terminal indicates whether an input or output bit is on or off. You can verify this status with the program to see if it is operating the way it should, when it should. If not, test inputs, outputs, and machine motion to isolate and repair the trouble.

Processor Front Panel Indicators

There are three front panel indicators located on the processor. These should always be the first check points when troubleshooting (Table 6.F).

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Table 6.F
The PROC Indicating LED Will Help You Troubleshoot Your Processor

If the PROC indicator	And the processor	You should
Green	is in the Run mode operating normally • program is executing • outputs are enabled. is in MEM STORE mode and EEPROM memory module is being programmed. The indicator will be ON for a few seconds and then then turn OFF.	No action required
Blinking Green	has an I/O configuration error • there is an illegal backplane switch combination (i.e., switch 4 is ON, switch 5 is OFF) • the I/O is not in complementary fashion (32-pt. I/O only).	Check the switch settings and module placement.
Red	has a possible hardware failure • program is not executing • if switch 1 of the switch group assembly if OFF, outputs are disabled data lines on the I/O chassis could be shorted to ground	Cycle power. If the problem still persists, call your A-B representative.
Off	is operating normally in Program or Remote Test mode is operating in Run mode, it has a memory or program error	Change the processor to Program mode, correct problem and cycle power. If problem still persists, call your A-B representative.

Watchdog Timer

The watchdog timer monitors the operation of the processor hardware. If something goes wrong with the hardware (electronic circuit failure within the processor), the watchdog timer times out after 250 milliseconds and a processor fault (red PROC indicator light) occurs. You then must recycle power to clear the fault. If repeated faults occur, return your processor for repair.

Processor Faults and Run-Time Errors

For information on run-time errors, see chapter 26.

Processor Removal

If the Processor is the suspected source of a fault, replace it.

Fuses

A fuse in the processor has no visual indicator. When a fuse is blown, the processor appears dead (since there is no power) and no indicators are lighted.

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Chapter 7

Memory Organization

Chapter Objectives

This chapter discusses:

- hardware and its relationship to your program
- memory and its components

This chapter provides detailed concepts of the memory's organization and its structure. Understanding these concepts aids you in programming your processor.

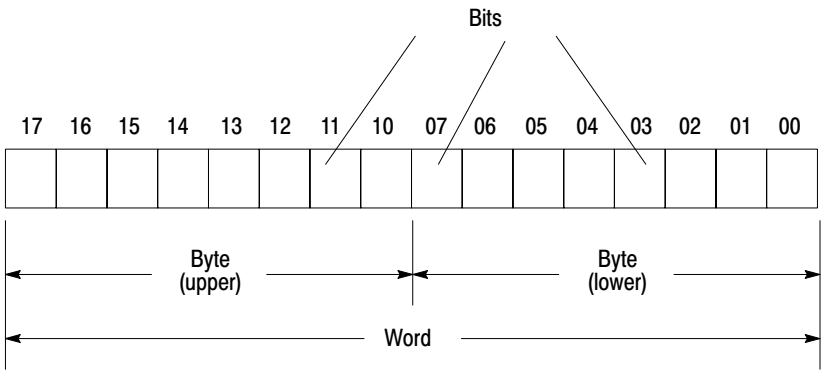
Introduction

Before we explain memory organization and its structure, read the following definitions:

Bit - the smallest unit of information that memory is capable of retaining

Byte - a group of 8 consecutive bits ($00\text{-}07_{08}$ or $10\text{-}17_{08}$)

Word - a group of 16 consecutive bits ($00\text{-}17_{08}$)



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In the program, the input or output instruction address is associated with a specific I/O terminal. See chapter 5 for more information.

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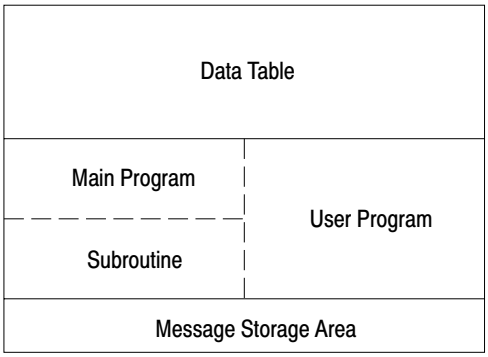
Memory Areas

Memory is divided into three major areas: data table, user program, and message storage area. These areas store input status, output status, and program instructions and messages.

Data Table

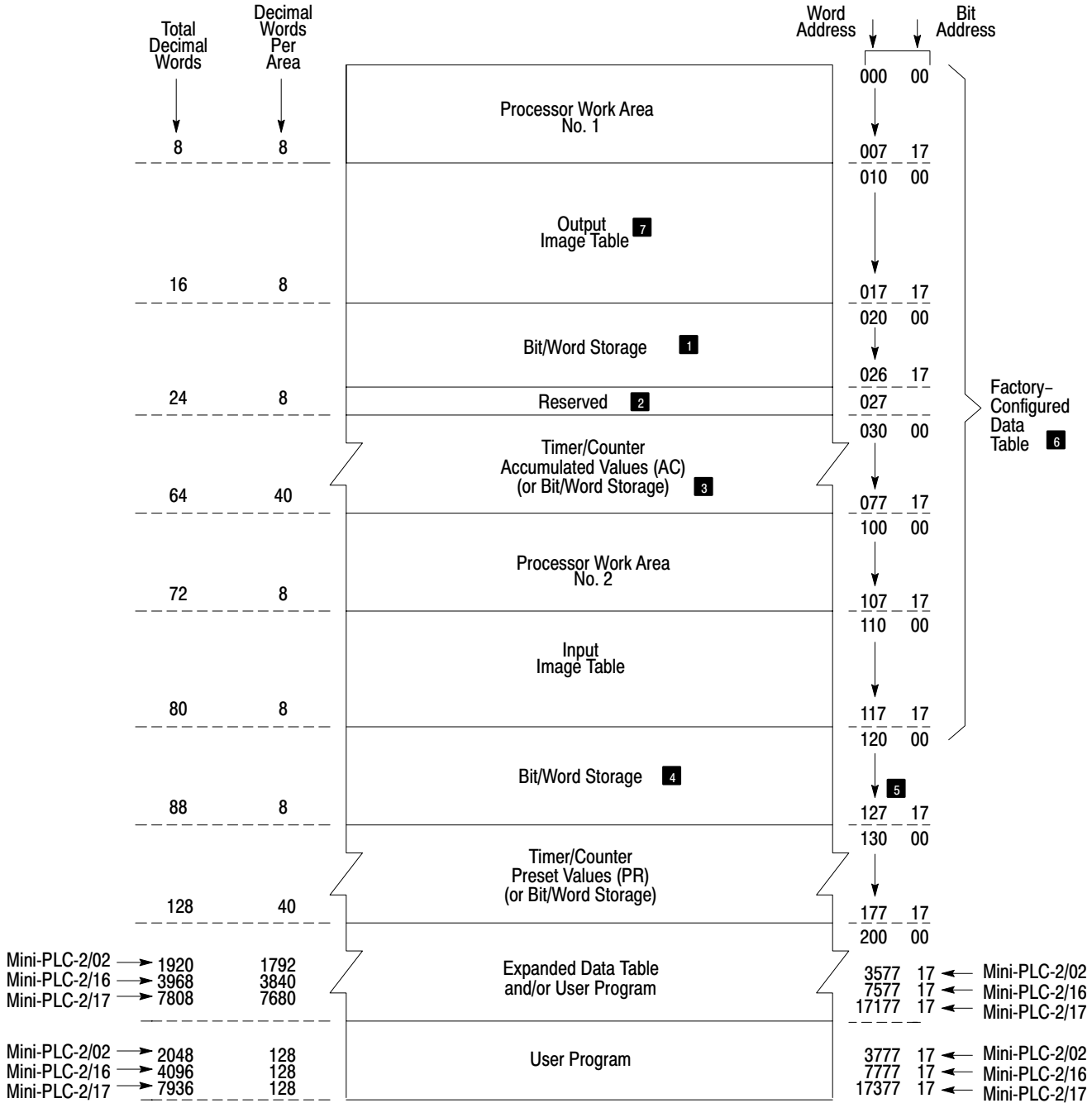
The first part of memory is the data table (Figure 7.1). The processors are factory configured for 128 words. Figure 7.2 shows memory structure with a factory configured data table. The specific concepts throughout this publication refer to a factory configured data table.

Figure 7.1
Simplified Memory Structure



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Figure 7.2
Data Table Factory Configured for 2-Slot Addressing

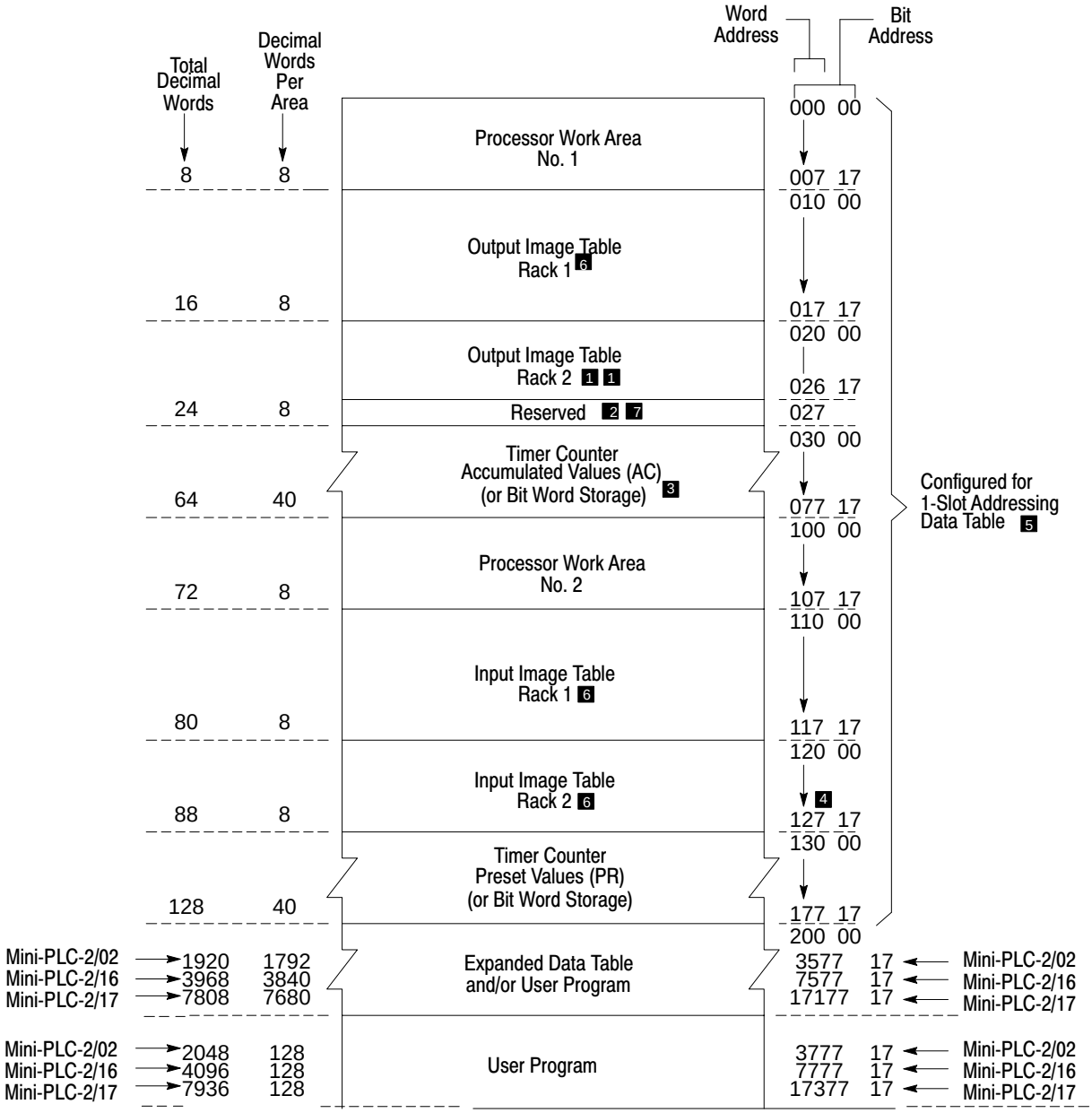


1 May not be used for accumulated values.
2 Not available for bit/word storage. Bits in this word are used by the processor.
3 Unused timer/counter memory words can reduce data table size and increase user program area.
4 May not be used for preset values.
5 Do not use word 127 for block transfer data storage.
6 Can be decreased to 48 words.
7 Do not use for bit/word storage.

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Figure 7.3
Data Table Configured for 1-Slot Addressing



1 May not be used for accumulated values.
2 Not available for bit/word storage. Bits in this word are used by the processor.
3 Unused timer/counter memory words can reduce data table size and increase user program area.
4 Do not use word 127 for block transfer data storage.
5 Can be decreased to 48 words.
6 Used with 1-slot addressing.
7 You cannot put an output or block transfer module in rack 2, I/O group 7 when using 1-slot addressing. You can put an input module in rack 2, I/O group 7.

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Figure 7.4
Data Table Configured for 1/2-Slot Addressing



1 May not be used for accumulated values.
2 Not available for bit/word storage. Bits in this word are used by the processor.
3 Unused timer/counter memory words can reduce data table size and increase user program area.
4 Do not use word 127 for block transfer data storage.
5 Can be decreased to 48 words.
6 You cannot put an output or block transfer module in rack 2, I/O Group 7 when using 1/2-slot addressing. You can put an input module in rack 2, I/O group 7.

10350–I

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Data Table Areas

The following areas make up the data table. They are:

- processor work area no. 1
- output image table
- bit/word storage (020-027)
- timer/counter accumulated values and internal storage
- processor work area no. 2
- input image table
- bit/word storage (120-127)
- timer/counter preset values and internal storage

Chapter 2 describes the input and output image tables. The following sections describe the remaining areas.

Processor Work Areas

There are two processor work areas. They are located at addresses 000 00 to 007 17 and 100 00 to 107 17. The processor uses these 16 words for its internal control functions. You cannot address these data table words.

Bit/Word Storage

There are two bit/word storage areas (providing you are not using 1-slot addressing). They are located at addresses 020-026 and 120-127.

Diagnostic Word: Word 027

Bits in word 027 are used by the processor for internal control functions.

This Bit:	Stores this Information:
00	(Battery low) – set when the battery is low.
01	(EEPROM) – set indicates that EEPROM transferred at power-up. This bit is always reset (0) when the processor powers down
02	(STI too long) – set indicates subroutine execution time plus program transition time exceed service time.
03	Reserved.
04	
05	
06	
07	Reserved for Data Highway – set when the processor is connected to the line and actively communicating with the Data Highway.
10-15	Used in Report Generation for message request bits
16	Report Generation Busy bit
17	Report Generation Done bit

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Adjusting the Data Table

You can adjust the size of a data table at any time during programming or editing. Using the 1770-T3 terminal, you can expand the data table in steps of two words from 48 words to 256 words and then in steps of 128 words to 1,920 words for a Mini-PLC-2/02, 3,968 words for a Mini-PLC-2/16 or 7,808 words for a Mini-PLC-2/17.

You can expand the data table to accommodate the full I/O capacity of the processor. Expanding the data table provides more timer/counters or up to 488 timers/counters maximum and space for files (see chapter 11). Expanding the data table reduces the size of the user program and memory storage area. You should allow sufficient room for both data table and user program.

To use the data table to its fullest capacity, remember the following:

- The processor initially reserves the first 128 words in the memory for the data table.
- You can adjust the data table size in two word increments to 256 words. Then, you can increase the data table size in blocks of 128 words.
- When the data table is set to 256 words, you can program up to 104 timer/counter instructions.
- If a block transfer instruction in your program addresses a module in rack 2 and you have a 1770-T3 series A or B terminal, you cannot decrease the size of the data table but you can increase it. You can use the two GET method for performing block transfers in rack 2 (see chapter 18).

Expanding the Data Table Between 48 and 128 Words

To expand your data table to any size between 48 and 128 words, do this:

SEARCH The word SEARCH appears in the lower left hand corner of the screen.

50 **DATA TABLE CONFIGURATION**

NUMBER OF 128–WORD D. T. BLOCKS	01
NUMBER OF INPUT/OUTPUT RACKS	2
NUMBER OF T/C (if available)	040
DATA TABLE SIZE	0128

This illustration shows a factory-configured data table. The numbers shown are default values. Numbers must be replaced by user-entered values.

Enter the number of timer/counters equivalent to the size of the data table (Table 7.A).

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Table 7.A
The Data Table Sizes Between 48 and 256 Words

Number of Timers and Counters	Data Table Size	Number of Timers and Counters	Data Table Size	Number of Timers and Counters	Data Table Size
000	0048				
001	0050	036	0120	071	0190
002	0052	037	0122	072	0192
003	0054	038	0124	073	0193
004	0056	039	0126	074	0196
005	0058	040	0128	075	0198
006	0060	041	0130	076	0200
007	0062	042	0132	077	0202
008	0064	043	0134	078	0204
009	0068	044	0136	079	0206
010		045	0138	080	0208
011	0070	046	0140	081	0210
012	0072	047	0142	082	0212
013	0074	048	0144	0873	0214
014	0076	049	0146	084	0216
015	0078	050	0148	085	0218
016	0080	051	0150	086	0220
017	0082	052	0152	087	0222
018	0084	053	0154	088	0224
019	0086	054	0156	089	0026
020	0088	055	0158	090	0228
021	0090	056	0160	091	0230
022	0092	057	0162	092	0232
023	0094	058	0164	093	0234
024	0096	059	0166	094	0236
025	0098	060	0168	095	0238
026	0100	061	0170	096	0240
027	0102	062	0172	097	0242
028	0104	063	0174	098	0244
029	0106	064	0176	099	0246
030	0108	065	0178	100	0248
031	0110	066	0180	101	0250
032	0112	067	0182	102	0252
033	0114	068	0184	103	0254
034	0116	069	0186	104	0256
035	0118	070	0188		

For 92 words, enter 022.

022 **DATA TABLE CONFIGURATION**

NUMBER OF 128–WORD D. T. BLOCKS	01
NUMBER OF INPUT/OUTPUT RACKS	2
NUMBER OF T/C (if available)	022
DATA TABLE SIZE	0092

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Three things happen to the display.

- The cursor returns to the NUMBER OF 128–WORD D.T. BLOCKS.
- NUMBER OF T/C changes to 022.
- DATA TABLE SIZE becomes 92.

Expanding the Data Table Between 130 and 256 Words

To expand your data table to any size between 130 and 256 words, do this:

02

DATA TABLE CONFIGURATION

NUMBER OF 128–WORD D. T. BLOCKS	01
NUMBER OF INPUT/OUTPUT RACKS	2
NUMBER OF T/C (if available)	104
DATA TABLE SIZE	0258

Three things happen to the data table configuration:

- The cursor jumps to the Number of T/C.
- Number of T/C changes to 104.
- Data table size becomes 256.

Enter the number of timer/counters equivalent to the desired size of the data table (Table 7.A).

065

DATA TABLE CONFIGURATION

NUMBER OF 128–WORD D. T. BLOCKS	021
NUMBER OF INPUT/OUTPUT RACKS	2
NUMBER OF T/C (if available)	165
DATA TABLE SIZE	0178

Three things happen to the data table configuration:

- The cursor returns to the NUMBER OF 128–WORD D.T. BLOCKS.
- NUMBER OF T/C changes to 065.
- DATA TABLE SIZE becomes 178.

If you want to increase the data table size to 256 words, press 02 and then CANCEL COMMAND.

If you want to increase the data table size beyond 256 words, remember the data table increases in steps of 128 words. See Table 7.B.

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Table 7.B
The Data Table Sizes Between 384 and 7,808 words

Enter	Data Table Size	Enter	Data Table Size
The Mini-PLC-2/02 has this number of data table blocks.			
3	384	10	1280
4	512	11	1408
5	640	12	1536
6	768	13	1664
7	896	14	1792
8	1024	15	1920
9	1152		
The Mini-PLC-2/16 has this additional number of data table blocks.			
16	2048	24	3072
17	2176	25	3200
18	2304	26	3328
19	2432	27	3456
20	2560	28	3584
21	2688	29	3712
22	2816	30	3840
23	2944	31	3968
32	4096	47	6016
33	4229	48	6144
34	4352	49	6272
35	4480	50	6400
36	4608	51	6528
37	4736	52	6656
38	4864	53	6784
39	4992	54	6912
40	5120	55	7040
41	5248	56	7168
42	5376	57	7296
43	5504	58	7424
44	5632	59	7552
45	5760	60	7680
46	5888	61	7808

After you have adjusted the data table, press CANCEL COMMAND and we will continue.

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User Program

The second major part of memory is the user program (Figure 7.1). It is divided into two areas:

This Area:	Stores this:
main program	The program is a group of ladder diagram instructions that control an application that guides the processor. These instructions can examine or change the status of bits in the memory of the processor. The status of these bits determines the operation of your output devices. When you write a program, you specify the things you want done in your application and the conditions that must be met before those things should be done.
subroutine area	This area stores small programs that are periodically accessed. The subroutine area is not scanned unless you program the processor to jump to this area (which is located in the memory between the main program and the message store areas). This area acts as the end of program statement for the main program.

The user program area begins at the end of the data table.

Message Storage

The third major part of memory is the message storage area (Figure 7.1). You are able to print messages in hard copy. You can store up to 70 messages using the 1770-T3 terminal, or 198 messages using the 1770-RG module and an RS-232-C device.

Message storage follows the end statement of your program and is limited by the number of unused words remaining in memory. Each word stores two alphanumeric characters. A character is any alpha or numerical figure (this includes blank spaces).

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Examining the Memory

If you want to examine the memory layout:

SEARCH The word SEARCH appears in the lower left hand corner of the screen.

54

Memory Layout Display

Mini-PLC-2/16

Data Table Size 128 words
User Program Area 0001 words
User Message Area 0000 words
Unused Memory Available 3967 words

Mini-PLC-2/17

Data Table Size 128 words
User Program Area 0001 words
User Message Area 0000 words
Unused Memory Available 7807 words

Mini-PLC-2/02

Data Table Size 128 words
User Program Area 0001 words
User Message Area 0000 words
Unused Memory Available 1919 words

This illustrates the memory layout display for a 128 word data table.

Even if there are no messages or programs in the memory, the END statement is there and it requires one word. Adding the number of words in the four areas equals the memory size (decimal).

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Chapter 8

Scan Theory

Chapter Objectives

In this chapter you will read about:

- scan function
- scan time

Scan Function

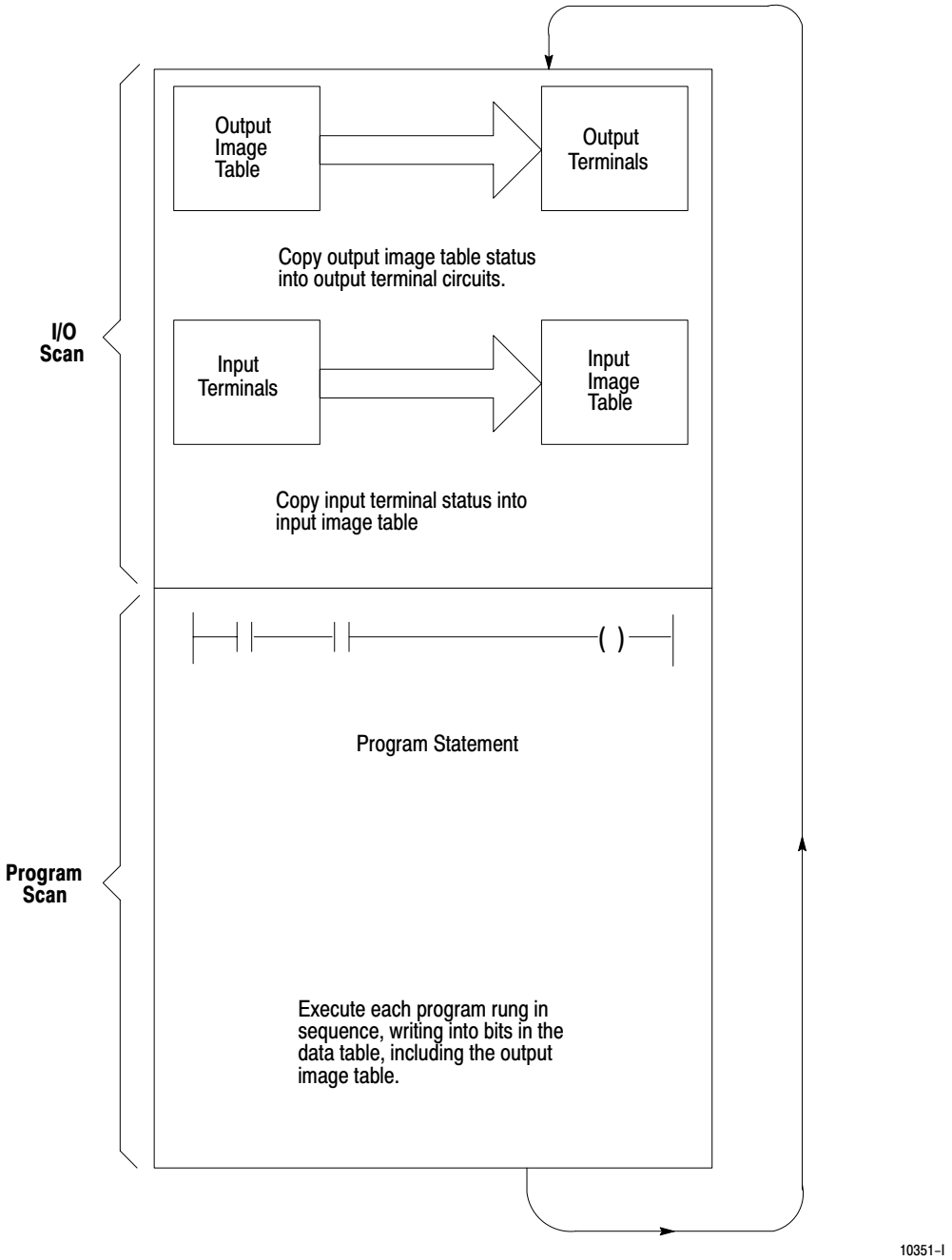
The processor controls the status of output devices or instructions in accordance with program logic. Every instruction in your program requires execution time. These times vary greatly depending upon the instruction, the amount of data to be operated on, and whether the instruction is true or false.

As a review from chapter 2, there are two types of scans (Figure 8.1):

- I/O scan
- Program scan

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Figure 8.1
The Processor Scans With This Sequence



Upon power-up, the processor begins the scan sequence with a program pre-scan. The processor then proceeds with the I/O scan. Data from output image table is written to the output modules. Data from the input modules is read into the input image table.

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Next, the processor scans the program statement by statement:

1. For each condition, the processor checks, or “reads,” the image table to see if the condition has been met.
2. If the set of conditions has been met, the processor writes a one into the bit location in the output image table corresponding to the output terminal to be energized. On the other hand, if the set of conditions has not been met, the processor writes a zero into that bit location, indicating that the output terminal should not be energized.

Important: When your processor is in the Remote Test mode, all outputs are held off. When your processor is in the Run/Program mode, all outputs are controlled by the user program.

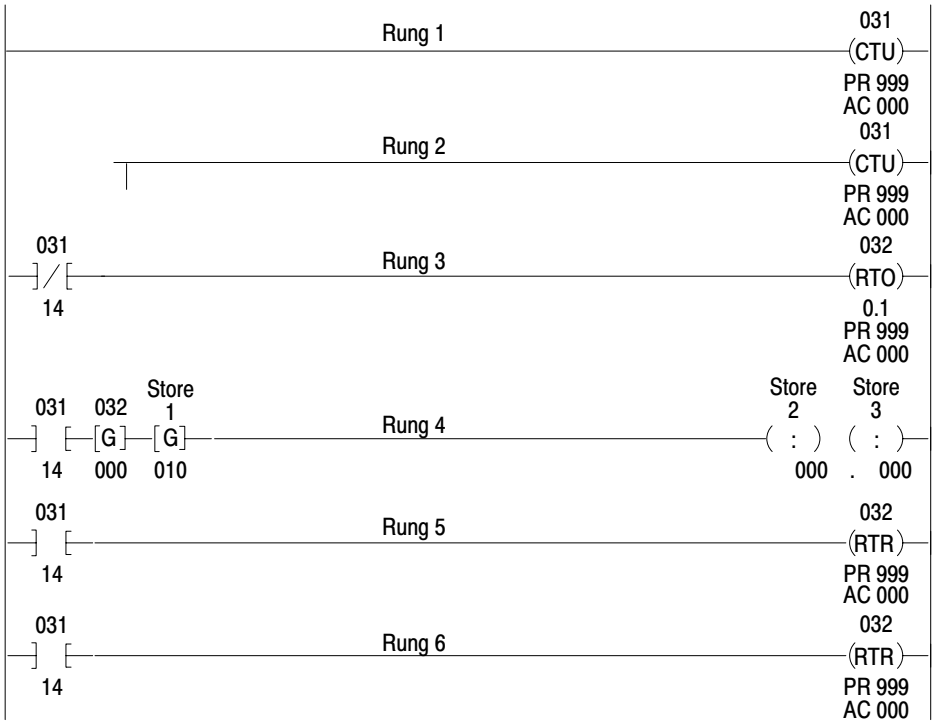
Average Scan Time

Average scan time is the average amount of time it takes the processor to monitor and update input and outputs, and to execute instructions in the program. The scan is performed serially; first the I/O image table is updated, other parts of the data table are not scanned, then the user program is scanned.

There are two ways to measure average scan time:

- Append the rungs in Figure 8.2 to your program.

Figure 8.2
Average Scan Time



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- Add the execution values for each instruction by using Table 8.A. The sum of these values added to the I/O scan time is the average scan time.

Table 8.A
These Are the Approximate Execution Time Per Scan (in average microseconds) and Words Per Scan for Each Instruction

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average μ sec.	False average μ sec.	
These instructions are features of the Mini-PLC-2/02, Mini-PLC-2/16, and Mini-PLC-2/17				
Examine On	–[ ]–	7 [10]	6 [10]	1 [1]
Examine Off	–[/]–	5 [10]	5 [10]	1 [1]
Output Energize	–( )–	8 [10]	8 [10]	1 [1]
Output Latch	–(L)–	7 [10]	6 [10]	1 [1]
Output Unlatch	–(U)–	7 [10]	6 [10]	1 [1]
Get	–[G]–	15 [10]	–	1 [1]
Put	–(PUT)–	12 [10]	7	1 [1]
Equal	–(=)–	12 [10]	13 [10]	1 [1]
Less Than	–(<)–	14 [10]	13 [10]	1 [1]
Get Byte	–]B[–	11 [10]	–	1 [1]
Limit Test	–]L[–	13 [10]	14 [10]	1 [1]
Counter Reset	–(CTR)–	19	6	1
Retentive Timer Reset	–(RTR)–	19	6	1
Timer On-Delay	–(TON)–	51	36	1
Retentive Timer On-Delay	–(RTO)–	52	33	1
Timer Off-Delay	–(CTD)–	55	39	1
Up Counter	–(CTU)–	38	30	1
Down Counter	–(CTD)–	36	31	1

[1] add 1 word per instruction when its address is 400_8 or greater
[2] add 2 words per instruction when its address is 400_8 or greater
[3] 1 word
[4] 999 words
[5] 1 bit
[6] 999 bits
[7] with 2 data values
[8] with 10 data values
[9] with 50 data values
[10] add 8 μs per instruction when its address is 400_8 or greater
[11] add 16 μs per instruction when its address is 400_8 or greater

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Table 8.A (continued)
These Are the Approximate Execution Time Per Scan (in average microseconds) and Words Per Scan for Each Instruction

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average µ sec.	False average µ sec.	
Add	-(+)-	29 [10]	9 [10]	1 [1]
Subtract	-(-)-	32 [10]	8 [10]	1 [1]
Multiply	-(x)-(x)-	201 [11]	18 [11]	2 [2]
Divide	-(:)-(:)-	184 [9]	20 [11]	2 [2]
Add	EAF 01	247	30	3
Subtract	EAF 02	252	30	3
Multiply	EAF 03	915	30	3
Divide	EAF 04	1442	30	3
Square Root	EAF 05	1007	30	3
BCD to Binary	EAF 13	228	31	3
Binary to BCD	EAF 14	192	31	3
FIFO Load	EAF 28	409 [3]	116	3
		8051 [4]	116	
FIFO Unload	EAF 29	377 [3]	117	3
		8051 [4]	117	
Bit Shift Left		222 [5]	55	5
		534 [6]	55	
Bit Shift Right		234 [5]	56	5
		482 [6]	55	
Examine Off Bit Shift	EAF 18	58	18	3
Examine On Bit Shift	EAF 19	60	18	3
Set Bit Shift	EAF 16	61	20	3
Reset Bit Shift	EAF 17	61	20	3
Log 10	EAF 30	807	30	3
Sin X	EAF 35	538	30	3
Cos X	EAF 36	538	30	3

[1] add 1 word per instruction when its address is 400_8 or greater
[2] add 2 words per instruction when its address is 400_8 or greater
[3] 1 word
[4] 999 words
[5] 1 bit
[6] 999 bits
[7] with 2 data values
[8] with 10 data values
[9] with 50 data values
[10] add 8 µs per instruction when its address is 400_8 or greater
[11] add 16 µs per instruction when its address is 400_8 or greater

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Table 8.A (continued)
These Are the Approximate Execution Time Per Scan (in average microseconds) and Words Per Scan for Each Instruction

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average μ sec.	False average μ sec.	
10x	EAF 37	685	30	3
Master Control Reset	–(MCR)–	7	7	1
Zone Control Last State	–(ZCL)–	12	8	1
Branch Start		8	6	1
Branch End		8	10	1
End, Temporary End	T. END	11	8	1
Subroutine Area	SBR	*	13	1
Immediate Input Update	–[I]–	62	–	1
Immediate Output Update	–(IOT)–	67	9	1
Label	LBL	17	–	1
Return	–(RET)–	*	0	1
Jump to Subroutine	–(JSR)–	*	9	1
Jump	–(JMP)–	34	10	1
Block Transfer Read		54	52	2
Block Transfer Write		54	52	2
Sequencer Output	SEQ 0	343	72	5
Sequence input	SEQ 1	418	36	5
Sequencer Load	SEQ 2	283	69	4
File-To-File Move	FILE 10	291	60	5
Word-To-File Move	FILE 11	153	49	4
File-To-Word Move	FILE 12	153	49	4

* = combined execution time – 79 μs

1 add 1 word per instruction when its address is 400_8 or greater
2 add 2 words per instruction when its address is 400_8 or greater
3 1 word
4 999 words
5 1 bit
6 999 bits
7 with 2 data values
8 with 10 data values
9 with 50 data values
10 add 8 μs per instruction when its address is 400_8 or greater
11 add 16 μs per instruction when its address is 400_8 or greater

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Table 8.A (continued)
These Are the Approximate Execution Time Per Scan (in average microseconds) and Words Per Scan for Each Instruction

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average μ sec.	False average μ sec.	
These EAF instructions are features of the Mini-PLC-2/17 only.				
Set Clock	EAF 10	217	30	3
Set Date	EAF 11	225	30	3
Set Leap Year and Day of Week	EAF 12	167	31	3
Read Clock	EAF 15	203	30	3
Read Date	EAF 16	205	30	3
Read Leap Year and Day of Week	EAF 17	138	31	3
PID	EAF 27	2450 (typical) 3500 (max.)	118	3
Log_e	EAF 31	1727	30	3
Powers of e ($e^{+/-x}$)	EAF 32	2071	30	3
Powers of Y ($y^{+/-x}$)	EAF 33	1500	30	3
Reciprocal (1/x)	EAF 34	1620	30	3
Average (3-digit	EAF 06	2463 [7]	101	3
		6787 [8]	101	
		2784 [9]		
		2103 [7]	98	
Average (6-digit)	EAF 06	3374 [8]	98	3
		10038 [9]	98	
Standard Deviation (3-digit)	EAF 07	4260 [7]	119	3
		34430 [8]	119	
Standard Deviation (6-digit)	EAF 07	162384 [9]	119	3
		13532 [7]	101	
		23322 [8]	101	
		70746 [9]	101	

[1] add 1 word per instruction when its address is 400_8 or greater
[2] add 2 words per instruction when its address is 400_8 or greater
[3] 1 word
[4] 999 words
[5] 1 bit
[6] 999 bits
[7] with 2 data values
[8] with 10 data values
[9] with 50 data values
[10] add 8 μs per instruction when its address is 400_8 or greater
[11] add 16 μs per instruction when its address is 400_8 or greater

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Here is an explanation of the rungs in Figure 8.2:

Rung 1 - The count increments its accumulated value each time this rung is true.

Rung 2 - This rung enables the counter to increment on the next scan. If we did not have this rung, the counter would always be true and it would not increment. Remember: Counters increment only on false to true transitions.

Rung 3 - The timer times in tenths of seconds when we are counting. This value is displayed on the industrial terminal screen.

Rung 4 - The average scan time is displayed beneath store 2 and store 3 in milliseconds. Replace store 1 using Editing a Get Instruction in a Completed Rung, chapter 12. Replace store 2 and store 3 instructions. Refer to three-digit math in chapter 13.

Rung 5 - The counter overflow bit is re-setting the timer.

Rung 6 - The counter overflow bit is resetting the counter.

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Chapter 9

Relay-Like Instructions

Chapter Objectives

This chapter describes the relay-like instructions. This chapter shows how to:

- define the conditions needed before the action takes place
- enter, edit or remove relay-like instructions

Programming Logic

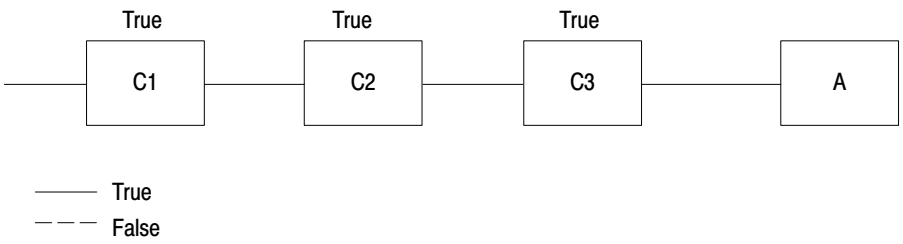
A program is a list of instructions that the processor executes. These instructions can examine or change the status of bits in the data table of the processor. The status of these bits can determine the operation of other instructions.

The program you specifies the order of things you want done in your application and the conditions that must be met before those things are done. For example, if you want a solenoid energized when a limit switch is closed, you specify:

Condition: if limit switch is closed
Action: energize solenoid

Programming logic differs from relay logic in an important way. Programming logic is only concerned with whether or not conditions have been met. These conditions may be open or closed input or output devices. We must have a continuous or unbroken path or true logic conditions for an action to be taken. The number of conditions is not important. There can be none, one, or many conditions preceding an output action.

Perhaps an example might make this clearer:



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Here, a **series** of conditions (C2, C2, C3) must be true before action A is performed.

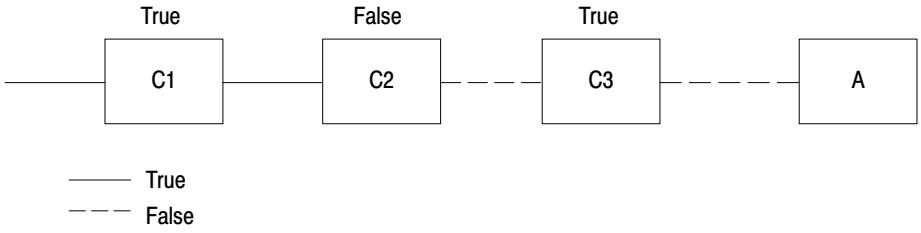
C1 = Input switch 1. When the switch is on, this condition is true. This switch turns on a conveyer belt.

C2 = Input sensor 1. When the sensor is off, this condition is true. This sensor detects if the temperature in the factory is below 40°C.

C3 = Input sensor 2. When the sensor is on, this condition is true. This sensor detects the presence of a part of the conveyer belt.

A = The part will be drilled. The path of conditions is continuous, that is, all conditions are true.

When C1, C2, and C3 are true, then a continuous path is made to a particular action. In this case, the continuous path causes the part to be drilled. When the path of conditions is continuous, we say that the rung is true. When the path of conditions is not continuous, we say the rung is false.



Here the path of conditions is not continuous because condition 2 is false. Therefore, the action A is not performed. We say the rung is false.

Set vs. Reset

As a review, if the device goes on, then we say the corresponding bit in data table is set to a 1. If the device goes off, we say the corresponding bit in data table is reset to a 0. (From this point on, set means the on-condition or 1. Reset means the off-condition or 0.)

If the device is:	Then a bit in memory is
on	set
off	reset

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Addresses

The processor scans the status of inputs and controls output devices. It does not go to the input or output terminals to see if outputs are on or off. Rather, it checks the status of the input and output devices by scanning corresponding bits in the input and output image area of the data table. The processor uses addresses to refer to words and bits in the data table.

For addressing purposes, I/O modules in a given I/O rack are organized into “module groups.” Thus, the module group number of an individual I/O module depends only on the I/O slot the module occupies. The first module group in any I/O chassis is always module group 0. Module groups can be easily identified by module group labels on the latches on top of the I/O chassis.

Each input and output bit has a five-digit address. If you need a bit address with more than 5 digits, use the EXPAND ADDR key. Press this key and then enter the address.

Word addresses, unlike bit address, do not require the EXPAND ADDR key. Instead, use leading zeros when necessary.

Any time a digit you are entering is not within the proper limits, the message `DIGIT OUT OF RANGE` is displayed. The cursor remains in the same position until you enter a valid digit.

Bit Examining

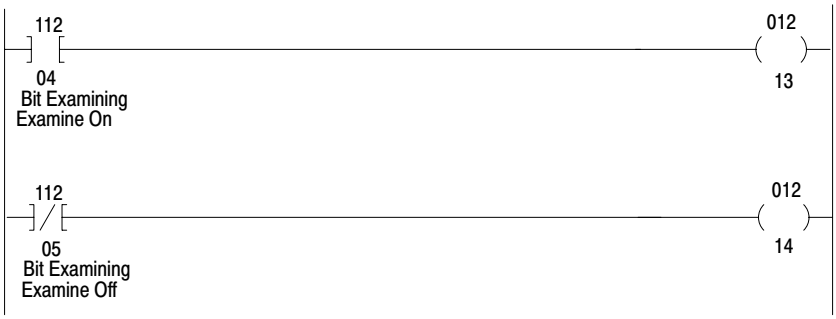
You can use seven programming instructions to write a program. These instructions are divided into three categories: bit examining, bit controlling, and branch instructions.

These instructions examine the status of bits in any data table area except processor work areas. When an examine on or examine off instruction is given an address in the I/O image table, the instruction can indirectly examine the status of a corresponding I/O device. If the image table bit is on, the condition is true. The I/O device and the I/O image table bit have the same address.

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Examine On and Examine Off

The Examine On (–] [–) and Examine Off (–]/[–) instructions tell the processor to examine a bit at a specified data table location.



This Instruction:	Becomes:	When the Corresponding Bit Is:
EXAMINE ON	true	set
	false	reset
EXAMINE OFF	true	reset
	false	set

Keystrokes

Enter an Examine On or Examine Off instruction by performing the following steps.

1. Press either –] [– or –]/[– as required.
2. Enter <bit address>.

Removing the Examine On or Examine Off Instruction

Remove an Examine On or a Examine Off instruction by performing the following steps.

1. Position the cursor over the Examine On or Examine Off instruction you want to remove.
2. Press [Remove] –] [– or –]/[–.

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Editing a Partially Completed or a Completed Rung

Edit an Examine On or Examine Off by performing the following steps. If you are editing a completed rung, proceed to step 1. If you are editing a partially completed rung, enter the next instruction and proceed to step 1.

1. Position the cursor over the Examine On or Examine Off instruction you want to edit.
2. Press either –] [– or –]/[– any other appropriate instruction key.
3. Enter <address>.

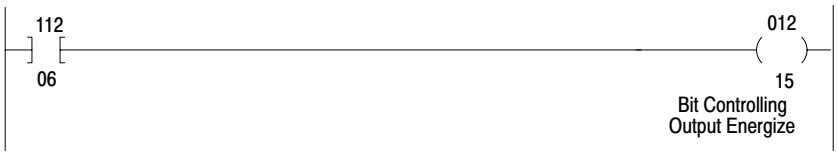
Bit Controlling

Output instructions are programmed at the end of the ladder-diagram rungs. Only one output instruction can be programmed on each rung and it is executed only if the instructions preceding it are true.

These instructions are used to set memory bits ON or OFF in any area of the data table, excluding processor work areas. They should not be assigned input image table addresses because input image table words are reset by the I/O scan.

Output Energize

The Output Energize instruction tells the processor to set or reset a specified data table bit.



It controls a specific bit based on the rung condition. When the rung condition is:

True - Output Energize sets a specified bit.
False - Output Energize resets a specified bit.

Keystrokes

Enter an Output Energize instruction by performing the following steps.

1. Press –( )–.
2. Enter <address>.

Removing an Output Energize Instruction

The only way to remove an Output Energize instructions is to remove the entire rung. See chapter 24.

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Editing in a Completed Rung

Edit the Output Energize instruction by performing the following steps. However, you cannot remove an output instruction.

1. Position the cursor over the Output Energize instruction you want to change.
2. Press –( )– or any other appropriate output instruction key.
3. Enter <address>.

Output Latch/Unlatch

The Output Latch –(L)– instruction tells the processor to latch and set a specified data table bit when the rung is true. It is usually paired with an unlatch instruction.



The Output Unlatch –(U)– instruction tells the processor to unlatch and reset a specific data table bit. It is usually paired with a latch instruction.



Important: The conditions for the Output Unlatch instruction must be different from the conditions that precede the Output Latch instruction.

These are retentive instructions. Retentive means that when the rung condition goes false, the latched bit remains set and the unlatched bit remains reset until changed by the program.

These instructions control a specific bit based on the rung condition. When its rung conditions are:

True - Output Latch sets a specified bit.
True - Output Unlatch resets a specified bit.
False - No action is taken.

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Keystrokes

Enter an Output Latch or Unlatch instruction by performing the following steps.

1. Press either –(L)– or –(U)– as required.
2. Enter <address>.

Important: You can initially condition the latch or unlatch instruction to on or off by positioning the cursor over the Output Latch or Output Unlatch instruction and pressing 1 or 0, respectively.

Editing in a Completed Rung

Edit an Output Latch or Unlatch instruction by performing the following steps.

1. Position the cursor over the Output Latch or Unlatch instruction you want to change.
2. Press either –(L)– or –(U)– or any other output instruction type as required.
3. Enter <address>.

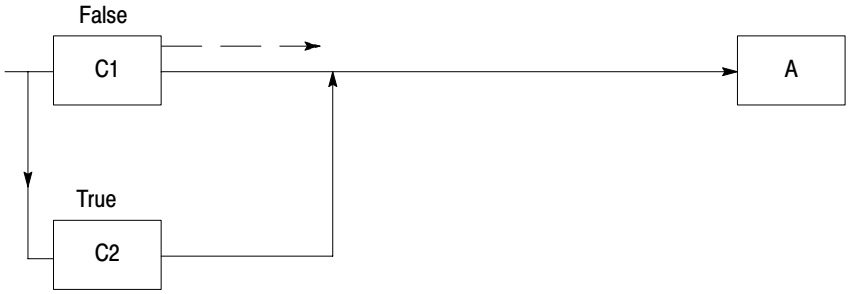
Important: If power is lost, all latch bits remain in their last state. When power is restored, all outputs connected to latch bits are energized immediately.

If power is lost but the processor battery back-up is maintained, all latched bits retain their state before power was lost. When power is off, outputs associated with the latched bits are off. When power is restored, all outputs connected to latched bits are energized immediately (provided the processor comes up in the Run/Program or Run mode).

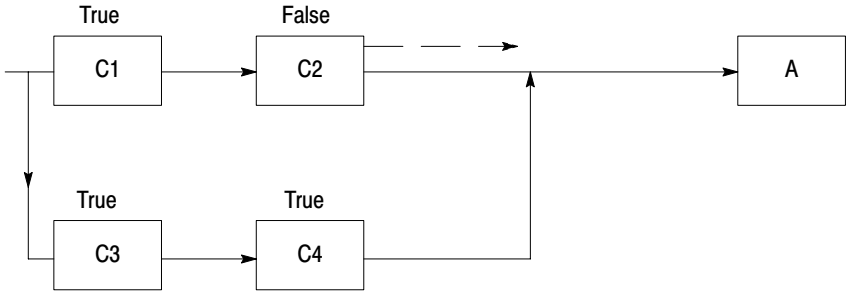
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Branching Instructions

Use branching instructions when you want several parallel sets of conditions to make an output action possible. A program with branching says, “If this set of conditions is true, or if that set of conditions is true, perform the following action.” Branching allows two or more paths to reach the same output destination.



Here two conditions are parallel. As long as one of the conditions (C1 or C2) is true, a continuous path to the action exists. Therefore, the action is performed.



Here are two sets of parallel conditions. If either set of conditions are true, the action is performed.



This illustration shows a program rung with branching, as it would appear by the 1770-T3 terminal display. You create a branch by using two different branch instructions. These are the Branch Start and Branch End instructions.

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Branch Start/End

A Branch Start instruction begins each parallel logic branch of a rung. It allows more than one combination of input conditions to energize an output device. It is programmed before the first instruction of each parallel branch.

A Branch End instruction completes a set of parallel branches.

Keystrokes

Enter a Branch Start or Branch End instruction by pressing either: ⊤ or ∃.

Important: You must begin each rung of parallel conditions with a Branch Start instruction.

Removing a Branch Start or Branch End Instruction

Remove a Branch Start or Branch End instruction or change an instruction type by performing the following steps.

1. Position the cursor over either the Branch Start or Branch End instruction.
2. Press [Remove] ⊤ or ∃

Inserting a Branch Instruction in a Completed Rung

Insert a Branch Start or Branch End instruction or change an instruction type by performing the following steps.

1. Position the cursor over the instruction immediately preceding the position you want to insert a Branch Start instruction.
2. Press [Insert] ⊤ .

Important: Once you press the Branch Start instruction, the statement `BRANCH END OMITTED` appears in the lower lefthand corner of the screen. It stays there until you enter a Branch End instruction.

3. Insert the conditioning instructions for this rung.
4. You must begin each set of parallel conditions or rung with a Branch Start instruction.
5. Complete the set of parallel conditions by pressing [Insert] ⊤.

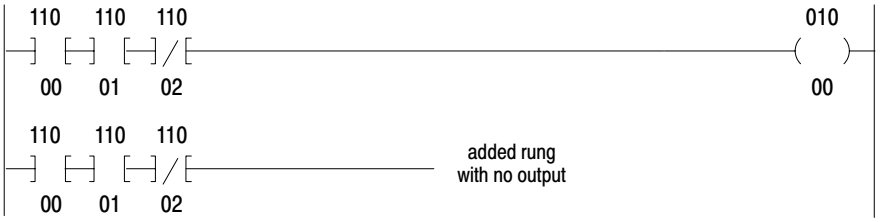
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Important: Once you press the Branch End instruction, the statement `BRANCH END OMITTED` disappears.

While inserting a Branch Start instruction to an existing rung during online programming, the actual output status (on or off) may not be the logically expected state of the rung. This condition exists until you enter the Branch End instruction and complete the rung.

To avoid this condition, do the following:

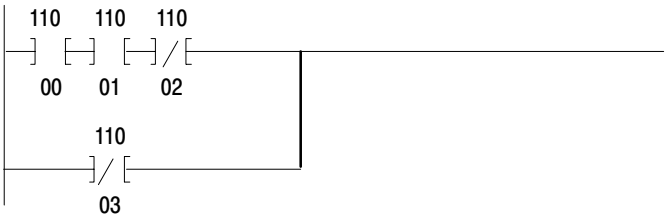
1. Immediately below the rung to be changed, create a new rung with the same input logic (duplicate the rung), but do not put the output in yet.



2. Move the cursor to the point where you want to change the logic and insert the Branch Start instruction.

3. Insert the desired parallel logic.

4. Insert the Branch End instruction.



5. Insert the output instruction



6. Delete the original rung

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Nesting

The following rung shows a nested branch.

Creating nested branches is not possible because the Branch End instruction completes a branch group. But the above rung shows a single branch group with two branch end instruction. Above, the Examine On instruction with the address 11012 is actually a branch group within a branch group.

The following rung achieves the same result and avoids nested branching:



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Chapter 10

Program Control Instructions

Chapter Objectives

This chapter describes these program control instructions:

- output override
- immediate I/O update

Introduction

Some applications need programming techniques designed to override a group of non-retentive outputs or update I/O ahead of the usual I/O scan time. The program control instructions satisfy this need.

The output override, or zone type instructions, operate similarly to a hardwired master control relay in that they affect a group of outputs in the user program. But these instructions are **not** a substitute for a hardwired master control relay, which provides emergency I/O power shutdown.

The following table illustrates specific instructions for these categories:

Output Override	Immediate Update I/O
Master Control Reset	Immediate Input Update
Zone Control Last State	Immediate Output Update

Output Override Instructions

Master Control Reset and Zone Control Last State



ATTENTION: Do not place a LABEL instruction in an MCR or ZCL zone. When jumping over a start fence, the processor will execute the program from the label to the end fence as if the start fence had been true. The start fence may have been false, so that all outputs within the zone are controlled by the output override instruction (i.e. OFF for MCR or last state for ZCL instructions).

Failure to observe this warning could cause unexpected operation with possible damage to equipment and/or injury to personnel.

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A Master Control Reset (MCR) establishes a zone in the user program in which all non-retentive outputs are turned off simultaneously.

Important: Retentive instructions (-(U)-, -(L)-, -(RTO)-) should not be placed within an MCR zone, because the MCR zone maintains retentive instructions in the last active state when the start fence goes false.



ATTENTION: A programmable controller should not be operated without a hard-wired master control relay and emergency stop switches to provide emergency I/O power shutdown. Emergency stop switches can be monitored but should not be controlled by the user program. These devices should be wired as described in chapter 4. The purpose of the devices is to guard against damage to equipment and/or injury to personnel.

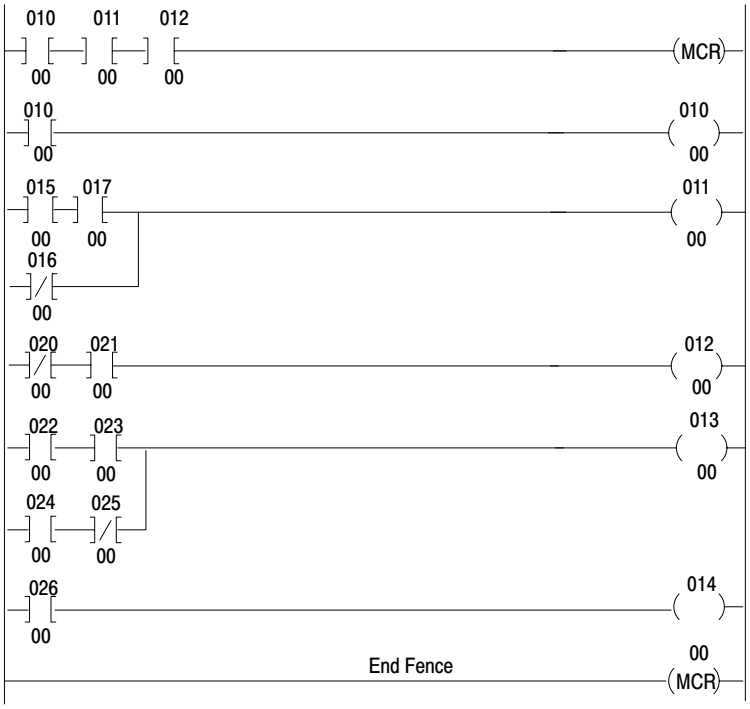
A Zone Control Last State (ZCL) instruction allows control of one or a group of outputs in more than one manner in the same program. It establishes a zone in the user program which controls the same outputs, through separate rungs, at different times.

To override a group of output devices, you must use two MCR (Figure 10.1) or ZCL (Figure 10.2) instructions: one each to begin the zone and one each to end the zone. The start fence is always programmed with a set of input conditions. The end fence must be programmed unconditionally.

When the input conditions of the start fence of an MCR zone are false, nonretentive outputs are turned off and held off. When the input conditions of the start fence of a ZCL zone are false, all outputs within the zone are left in their last state. The end fence must be programmed unconditionally.

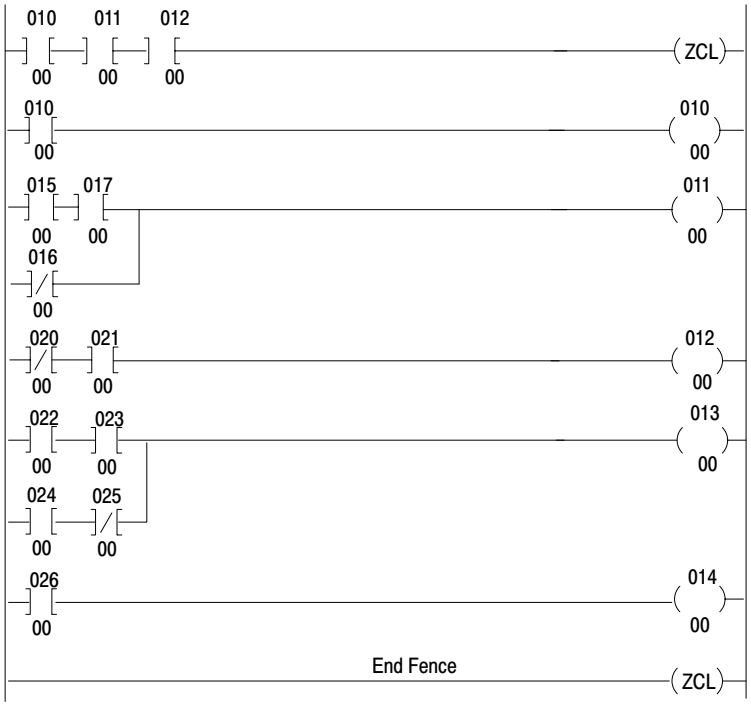
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Figure 10.1
Master Control Reset



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Figure 10.2
Zone Control Reset



If the start fence becomes:

True - Each rung condition controls their output instruction.
False - All output instructions within the zone are left in their last state.

ATTENTION: MCR or ZCL zones must not overlap or nest. Each zone must be separate and complete. Overlapping MCR or ZCL zones could result in unpredictable machine operation with possible damage to equipment and/or injury to personnel.

Keystrokes
Enter an MCR or ZCL instruction by performing the following steps.

1. Press either -(MCR)- or -(ZCL)-.

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Editing in a Completed Rung
Edit these instructions by performing the following steps:

1. Position the cursor over the MCR or ZCL instruction you want to change.
2. Press either -(MCR)- or -(ZCL)- or any other appropriate instruction type key.
3. Enter any parameters that may be required by a new instruction.

Immediate I/O Update Instructions

Immediate I/O update instructions interrupt the program scan to update I/O data before the normal I/O update sequence. Use these instructions where I/O modules interface with I/O devices that operate in a shorter time period than the processor scan.

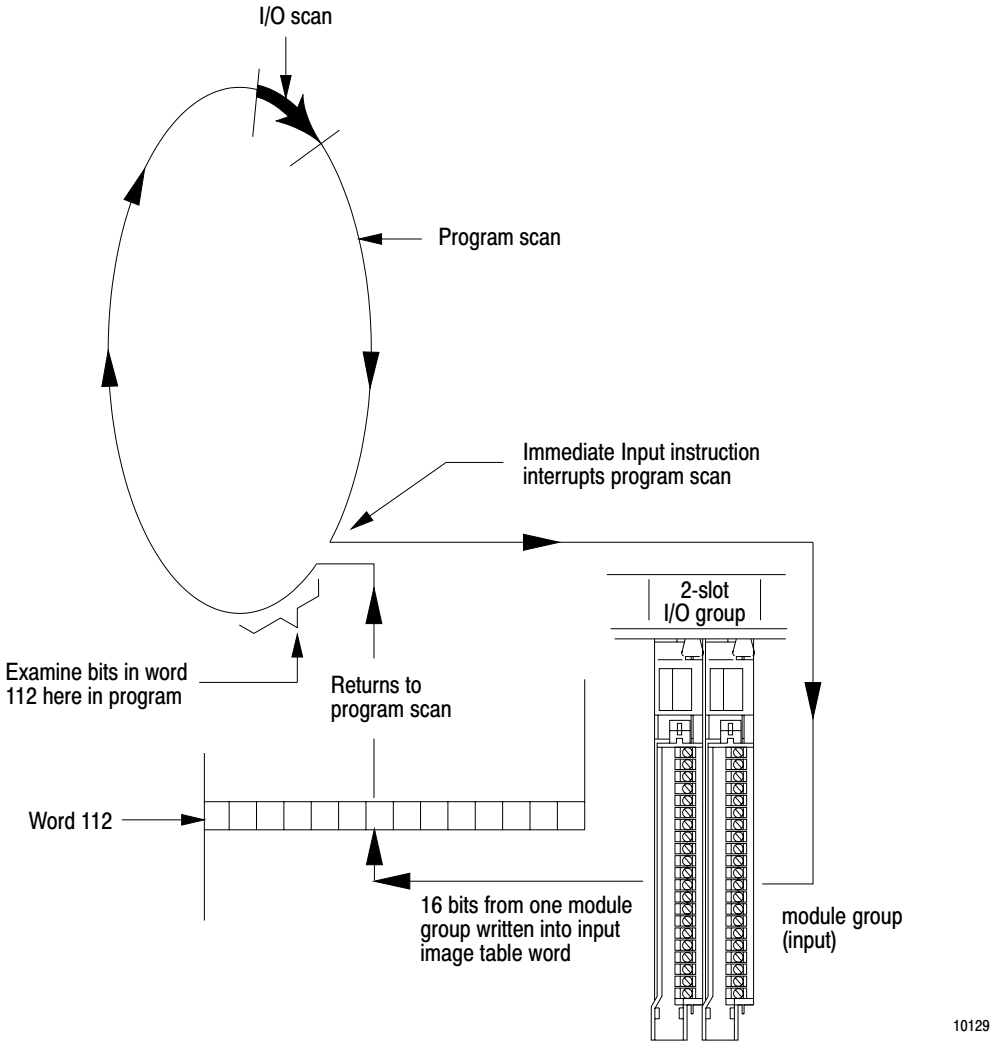
Important: You can have as many as 8 Immediate Input and 8 Immediate Output instructions per rack.

Immediate Input/Immediate Output Update

An Immediate Input Update instruction interrupts the program scan to update input image table with data from the corresponding module group. The image table is updated before the normal I/O scan and executed each program scan (Figure 10.3). This instruction is always considered logic true and execution takes place whether or not other rung conditions allow logic continuity.

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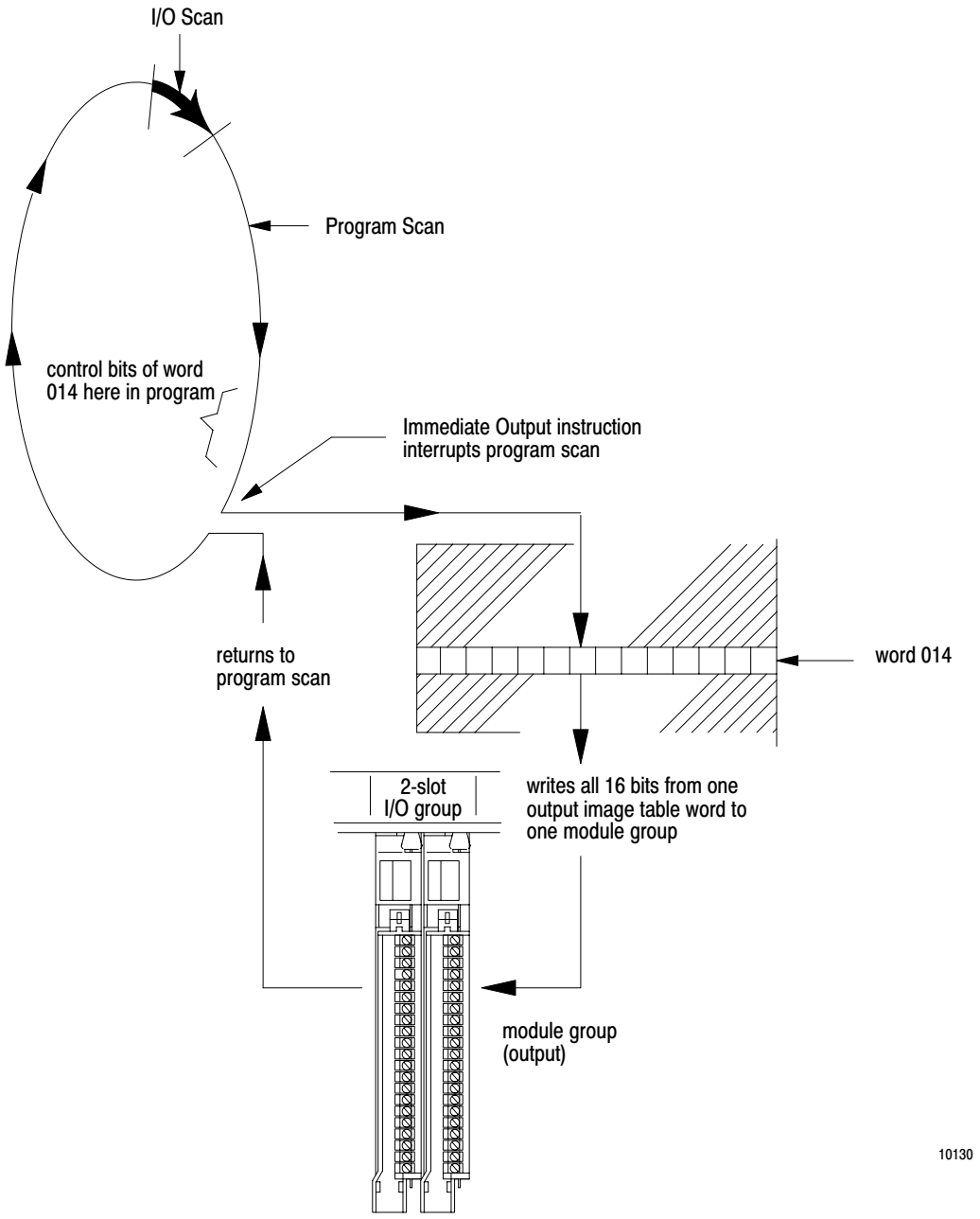
Figure 10.3
Immediate Input Instruction



An Immediate Output Update instruction interrupts the program scan to update the module group with data from corresponding output image table word address (Figure 10.4). The image table is updated before the normal I/O scan and executed each program scan when the rung is true. It can be programmed unconditionally. This instruction immediately transfers output data from the selected 16-bit word in the output image table without waiting for the normal I/O scan.

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Figure 10.4
Immediate Output Instruction



Keystrokes

Enter an Immediate Input or Immediate Output instruction by performing the following steps.

1. Press either -[I]- or -[IOT]-.

2. Enter <address>.

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Removing an Immediate Output Instruction

The only way to remove an Immediate Output Update instruction is to remove the entire rung. See chapter 11.

Removing an Immediate Input Instruction

Remove an Immediate Input Update instruction by performing the following steps.

1. Position the cursor over the Immediate Input Update instruction you want to remove.

2. Press [REMOVE]-[I]-.

Editing a Partially Completed Rung or a Completed Rung

Edit an Immediate Input or Immediate Output instruction by performing the following steps.

If you are editing a completed rung, proceed to step 1. If you are editing a partially completed rung, enter the next instruction and proceed to step 1.

1. Position the cursor over the Immediate Input or Immediate Output Update instruction you want to change.

2. Press -(I)-, -[IOT]-, or any other appropriate instruction type key.

3. Enter <address>.

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Chapter 11

Timers and Counters

Chapter Objectives

This chapter describes two instructions that keep track of timed intervals or counted events:

- timers
- counters

Introduction

Timer and counter instructions are output instructions internal to the processor. They provide many of the capabilities available with timing relays and solid state timing/counting devices. Usually conditioned by examine instructions, timers and counters keep track of timed intervals or counted events according to the logic continuity of the rung.

You can program up to 488 internal **timers** and the last timer address is 1677. The number of **counters** are limited only by the processor's memory. The last counter address for each is listed below:

This Processor	Has This Last Timer/Counter Address:
Mini-PLC-2/02	3477
Mini-PLC-2/16	7477
Mini-PLC-2/17	17077

Each timer or counter instruction has two 3-digit values. Each value requires one word of data table memory. These 3-digit values are:

Accumulated Value (AC)

Storage begins at word address 030 in 2-slot and 1-slot addressing modes and 050 in 1/2-slot addressing mode. The address of the AC value word is the address of the timer or counter.

The AC value always starts at 000. Use status bit 15 of the AC word to control outputs.

Function:		
	Timers	number of elapsed timed intervals
	Counters	number of counted events
	Both	upper 4 bits of accumulated word (14-17) are the status bits.

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Preset Value (PR)

Storage begins at an address 100 words greater than its corresponding AC value.

Function:	Timers	number of elapsed timed intervals
	Counters	number of counted events
	Both	when the accumulated value equals the preset value, AC = PR, a status bit is set and can be examined to turn an output device on or off.

Timer Instructions

A timer counts the elapsed time-base intervals and stores this count in the accumulated value word. Timers can be anywhere in the data table. The third digit from the right in the address must be an even number. Timer instructions have three time bases: 1.0 second, 0.1 second, or 0.01 second.

Two bits in the accumulated value word are status bits:

- Bit 15 is the timed (done) bit. It is set when the timer has timed out (AC = PR). The setting or resetting depends on the type of timer instruction.
- Bit 17 is the enable bit. It is set when rung conditions are true and is reset when rung conditions are false.

There are four types of timer instructions available:

- timer on-delay
- timer off-delay
- retentive timer on-delay
- retentive timer reset

Timer On Delay

The Timer On Delay instruction is programmed as an output instruction.



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When the timer on delay rung condition becomes:

True

- Timer cycle begins.
- Timer increments its AC value.
- Bit 15 is set when AC=PR and the timer stops timing.
- Bit 17 is set.

False

- Accumulated value resets to 000.
- Bits 15 and 17 are reset.

The accumulated value and status bits are also reset when the Mode Select Switch is turned from the PROG position to RUN/PROGRAM or RUN.

Timer Off Delay

The Timer Off Delay instruction is programmed as an output instruction.



When the timer off delay rung condition becomes:

True

- Bit 15 is set.
- Bit 17 is set.
- Accumulated value resets to 000.

False

- Timer cycle begins.
- Timer increments its AC value.
- Bit 15 resets when the AC=PR and the timer stops timing.
- Bit 17 is reset.

Keystrokes

Enter a Timer On or a Timer Off Delay instruction by performing the following steps.

1. Press either -(TON)- or -(TOF)-.
2. Enter <address>.

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3. Enter <time base>.

For This Time Base:	Press:
1.0	[1] [0]
0.1	[0] [1]
0.01	[0] [0]

4. Enter <preset value>.

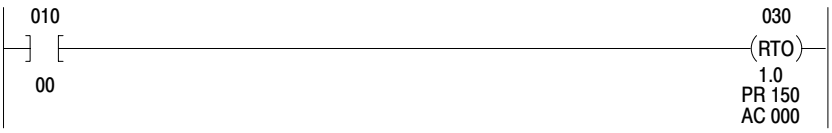
Editing in a Completed Rung

Edit the Timer On or Timer Off Delay instruction by performing the following steps.

1. Position the cursor over the Timer On or Timer Off Delay instruction you want to change.
2. Press -(TON)-, -(TOF)-, or any other appropriate instruction type.
3. Enter <address>.
4. Enter <time base>.
5. Enter <preset value>.

Retentive Timer On

The Retentive Timer On accumulates the amount of time that the preconditions of its rung are true. It controls one or more outputs (by means of other rungs) after the total accumulated time is equal to the preset time. Whenever the rung is false, the accumulated time is retained. If the outputs have been energized, they remain on. The accumulated time and energized outputs are retained if power is removed from the processor. A separate rung, containing a retentive timer reset instruction must be programmed in order to reset the accumulated time to zero and turn off the outputs.



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When the rung condition becomes:

True

- Timer begins counting time-base intervals.
- Bit 15 is set when AC=PR and the timer stops timing.
- Bit 17 is set.

False

- Accumulated value is retained.
- Bit 15 - no action is taken.
- Bit 17 is reset.

Important: The RTO instruction retains its AC value when the:

- Rung condition turns false.
- Processor changes to remote/program mode.
- Power outage occurs and memory backup is maintained.

Retentive Timer Reset

The Retentive Timer Reset instruction resets the accumulated value and timed bit of the retentive timer to zero. This instruction is given the same word address as its corresponding RTO instruction. When the rung conditions go true, the RTR instruction resets the AC value and resets the status bits to zero.



When the rung condition becomes:

True

- RTR instruction resets the accumulated value of the RTO instruction.
- Bits 15 and 17 are reset.

False

- No action is taken.

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Keystrokes

Enter a Retentive Timer On or a Retentive Timer Reset instruction by performing the following steps.

1. Press either –(RTO)– or –(RTR)–.
2. Enter <address>.

Perform steps 3, 4 and 5 for a Retentive Timer On instruction only.

3. Enter <time base>.
4. Enter <preset value>.
5. Enter <accumulated value>.

Editing in a Completed Rung

Edit a Retentive Timer On or a Retentive Timer Reset instruction by performing the following steps.

1. Position the cursor over the Retentive Timer or Retentive Timer Reset you are going to change.
2. Press -(RTO)-, -(RTR)-, or any other appropriate instruction type key.
3. Enter <address>.

Important: Do not perform steps 4 and 5 for a Retentive Timer Reset instruction.

4. Enter <time base> if appropriate.
5. Enter <preset value>.

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Counter Instructions

A counter counts the number of events that occur and stores this count in its accumulated value word. Counters can be located anywhere in the data table. An event is defined as a false-to-true transition. Counter instructions have no time base.. The last counter address for each is listed below:

This Processor	Has This Last Timer/Counter Address:
Mini-PLC-2/02	3477
Mini-PLC-2/16	7477
Mini-PLC-2/17	17077

The upper four bits in the accumulated value (AC) word are status bits:

This Bit:	Contains This Information:
14	Overflow/underflow bit. It is set when the AC value of the CTU instruction exceeds 999 or when the AC value of the CTD instruction falls below 000.
15	Count complete bit. it is set when the AC value $\geq$ PR value.
16	Enable bit for CTD instruction. It is set when the rung condition is true.
17	Enable bit for CTU instruction. It is set when the rung condition is true.

There are three types of counter instructions available with the controller:

- up counter
- down counter
- counter reset

Up Counter

An Up Counter instruction increments its accumulated value for each false-to-true transition of the rung condition. The rung condition must go from true to false and back to true before the next count is registered.



When the rung condition becomes:

True

- Accumulated value increments by 1.
- Bit 14 is set if the AC > 999.
- Bit 15 is set when AC $\geq$ PR. Incrementing the accumulated value continues after the preset value is reached.
- Bit 17 is set and stays set until the rung goes false.

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False

- Accumulated value is retained.
- Bit 14 - no action is taken.
- Bit 15 - no action is taken.
- Bit 17 is reset.

The Up Counter instruction retains its AC value when:

- You change the mode to program or remote program.
- The rung condition turns false.
- A power outage occurs and memory backup is maintained.

Important: Bit 14 of the accumulated value word is set when the accumulated value either overflows or underflows. When a down counter preset is 000, the underflow bit 14 will not be set when the count goes below 0.

Down Counter

The Down Counter instruction subtracts one from its accumulated value for each false to true transition of its rung conditions. A count is only added on a false to true transition, so rung conditions must go from true to false and back to true before the next count is registered.



When the rung condition becomes:

True

- Accumulated value decrements by 1.
- Bit 14 is set when AC < 000.
- Bit 15 is reset when AC < PR; counting continues.
- Bit 16 is set and stays set until the rung goes false.

False

- Accumulated value is retained.
- Bit 14 - no action is taken.
- Bit 15 - no action is taken.
- Bit 16 is reset.

The Down Counter instruction retains its AC value when:

- You change the mode to program or remote program.
- The rung condition turns false.
- A power outage occurs and memory backup is maintained.

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Important: When a down counter preset is 000, the underflow bit 14 will not be set when the count goes below 0 and the count complete bit 15 will not be reset when AC < PR.

Counter Reset

The Counter Reset instruction resets the up counter or down counter instructions accumulated value and status bits to 0. When used alone, the Down Counter's accumulated value may need to be "reset" in the program to its original value (usually a value other than 000).



When the rung condition becomes:

True

- Accumulated value of the specified counter is reset to 000.
- Status bits (14,15,16,17) are reset.

False

- No action is taken.

Keystrokes

Enter an Up Counter, Down Counter or Counter Reset instruction by performing the following steps.

1. Press -(CTU)-, -(CTD)-, or -(CTR)-.

2. Enter <address>.

Important: Do not perform steps 3 and 4 for a Counter Reset instruction.

3. Enter <preset value>.

4. Enter <accumulated value>.

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Editing in a Completed Rung

You edit an Up Counter, a Down Counter, or a Counter Reset instruction by performing the following steps.

1. Position the cursor over the Up Counter, Down Counter or Counter Reset you want to change.

2. Press either -(CTU)-, -(CTD)-, -(CTR)-, or any other appropriate instruction type.

3. Enter <address>.

Important: Do not perform steps 4 and 5 for a Counter Reset instruction.

4. Enter <preset value> if appropriate.

5. Enter <accumulated value>.

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Chapter 12

Data Manipulation and Comparison Instructions

Chapter Objectives

In this chapter, you will read about two types of instructions used to transfer and compare data and how to use these instructions to perform operations of data that is stored in the data table. These types of instructions are:

- transfer instructions
- compare instructions

Get

A Get instruction accesses all 16 bits of one word in the data table. It displays a three digit hexadecimal value of the lower 12 bits (bits 0 – 13) of the chosen word.

The Get instruction is programmed in the condition area of the ladder diagram rung and it can be located at the beginning of a rung or with one or more conditions preceding it.

A Get instruction always accesses the word which it addresses. It is not a "condition" that determines rung logic continuity and it is always true and intensified.



In a selectable timed interrupt, the Get instruction is the first instruction in the subroutine area. See chapter 22 for more information.

ATTENTION: Use the Get instruction in the subroutine area carefully because unintended subroutine execution can cause unexpected machine operation.

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Put

A Put instruction receives all 16 bits of data from the immediately preceding Get instruction and stores the data at the specified data table word location. Use with a Get instruction to form a data transfer rung.

This instruction is programmed in the output side of the ladder diagram rung. This instruction can have the same address as other instructions in the program. It must be immediately preceded by a Get instruction.



When rung conditions become:

True

- A Get instruction transfers data to the Put instruction.
- The lower 12 bits are displayed in hexadecimal beneath the Put instruction.
- Bits 14-17 are transferred but not displayed.

False

- Because the Put instruction is retentive, any change in Get instruction data does not change Put instruction data.

Keystrokes

Enter a Get or Put instruction by performing the following steps.

1. Press -[G]- or -(PUT)-.

2. Enter <address>.

Important: Step 3 is not needed for a Put instruction.

3. Enter <data> if appropriate.

Removing a GET instruction

Remove a GET instruction by performing the following steps.

1. Position the cursor over the Get instruction you are going to remove.

2. Press [REMOVE] -[G]-.

Removing a PUT instruction

The only way you can remove a Put instruction is to remove the whole rung. See chapter 24.

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Editing a Get Instruction on a Partially Completed Rung

1. Enter the next instruction.
2. Position the cursor over the GET instruction.
3. Press -[G]- or any other appropriate instruction type key.
4. Enter <address>.
5. Enter <data> if appropriate.

Editing a Get or Put Instruction in a Completed Rung

1. Position the cursor over the GET or PUT instruction.
2. Press -[G]-, -(PUT)-, or any other appropriate instruction type key.
3. Enter <address>.

Important: Step 4 is not needed for a PUT instruction.

4. Enter <data> if appropriate.

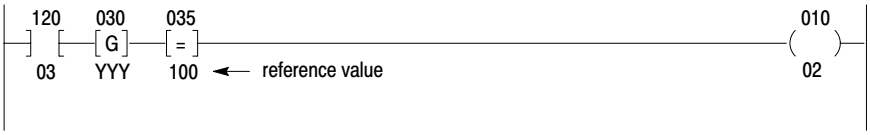
Compare Instructions

There are four compare instructions:

- Equal To
- Less Than
- Get Byte
- Limit Test

Equal To

An Equal To comparison is made with the Get and Equal To instructions. The Get value is the changing variable and is compared to the reference value of the Equal To instruction for an equal to condition. When the Get value equals the Equal To value, the comparison is true and logic continuity is established. It determines the rung condition. A Get/Equal To compares only the lower 12 bits to the immediately preceding Get instruction.



When YYY equals 100, the Get/Equal To comparison is true and 010/02 is energized.

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If the rung condition becomes:

True If there is equality.
False If there is no equality.

Keystrokes

Enter an Equal To instruction by performing the following steps.

1. Press -[=]-.
2. Enter <address>.
3. Enter <reference value> if appropriate.

Removing an Equal To Instruction

Remove an Equal To instruction by performing the following steps.

1. Position the cursor over the Equal To instruction you are going to remove.
2. Press [Remove] -[=]-.

Editing a Completed Rung

Edit an Equal To instruction by performing the following steps.

1. Position the cursor over the Equal To instruction.
2. Press -[=]- or any other appropriate instruction type key.
3. Enter <address>.
4. Enter <reference value> if appropriate.

Less Than

The Less Than instruction compares the data in your specified address with the data stored at another address in memory. It determines the rung condition. A Less Than instruction compares only the lower 12 bits to the immediately preceding Get instruction.

It is programmed after the Get instruction in the condition side of the ladder diagram rung.



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When YYY is less than 654, the Get/Less Than comparison is true and 010/02 is energized.

The rung condition becomes:

True	If the get value is less than the reference value stored in the Less Than instruction.
False	If the get value is equal to or greater than the less than value.

Keystrokes

Enter a Less Than instruction by performing the following steps.

1. Press -[<]-.
2. Enter <address>.
3. Enter <reference value>.

Removing the Less Than Instruction

Remove a Less Than instruction by performing the following steps.

1. Position the cursor over the Less Than instruction.
2. Press [REMOVE] -[<]-.

Editing a Completed Rung

You can edit a Less Than instruction by performing the following steps.

1. Position the cursor over the Less Than instruction.
2. Press -[<]- or any other appropriate data comparison instruction.
3. Enter <address>.
4. Enter <reference value> if applicable.

Limit Test

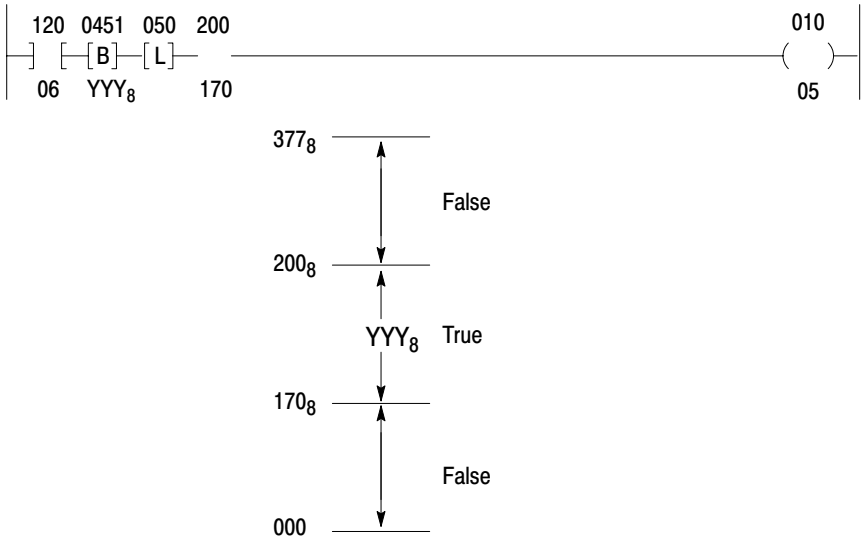
The Limit Test checks to see if an octal value of a byte is between two reference limit values that are also octal.

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- Programmed with a Get Byte instruction located in the condition area of the ladder diagram.
- Do not place compare instructions between the Get Byte and Limit Test instruction.
- The Get Byte and Limit Test instructions work only with octal values (ranging from 000 to 377).

There are two cases for comparison:

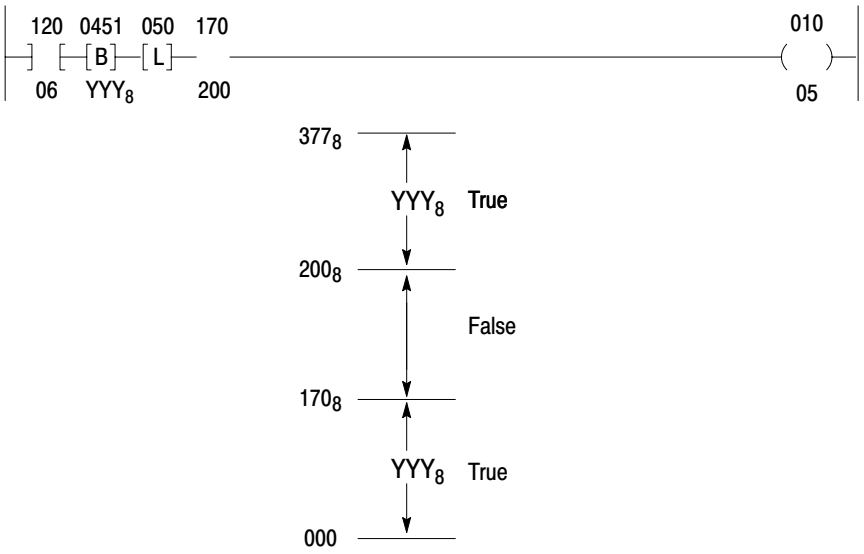
Case 1. Lower Limit ≤≤YYY ≤≤Upper Limit



If YYY is equal to or greater than 170 and equal to or less than 200, the comparison is true and logic continuity is established. If YYY is less than 170 or greater than 200, the comparison is false and logic continuity is not established.

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Case 2. Lower Limit ≥ YYY ≥ Upper Limit



If YYY is equal to or less than 200 and equal to or greater than 170, the comparison is false and logic continuity is not established. If YYY_8 is greater than 200 or less than 170, the comparison is true and logic continuity is established.

Keystrokes

Enter a Limit Test instruction by performing the following steps.

1. Press -[L]-.
2. Enter <address>.
3. Enter <upper limit>.
4. Enter <lower limit>.

Editing a Completed Rung

Edit the Limit Test comparison by performing the following steps.

1. Positions the cursor over the limit instruction you are going to edit.
2. Press -[L]-.
3. Enter <address>.
4. Enter <upper limit>.
5. Enter <lower limit>.

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Operations Involving Transfer and Comparison Instructions

You can perform four operations involving transfer and comparison instructions.

- equal to or less than
- greater than
- equal to or greater than
- get byte/put

Equal To or Less Than

The Equal To/Less Than comparison is made using the Get, Less Than, Equal To, and branching instructions. The Get value is the changing value. The Less Than and Equal To instructions are assigned a reference value. When the Get value is either less than or equal to the value at Less Than and Equal To instructions, the comparison is true and logic continuity is established.



If YYY is equal to or less than 237 the Get/Less Than or Equal To comparison is true an 010/02 is energized.

Important: Only one Get instruction is required for a parallel comparison. The Less Than and Equal To instructions are programmed in parallel branches.

Keystrokes

Enter an Equal To or Less Than comparison by performing the following steps.

1. Press -[G]-.
2. Enter <address>.
3. Enter <reference value>.
4. Press [↳]
5. Press -[<]-.
6. Enter <address>.
7. Enter <reference value>.
8. Press [↳].

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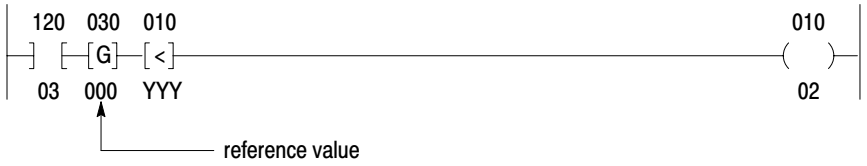
9. Press -[=]-.
10. Enter the same address as that entered for the Less Than instruction.
11. Enter <reference value>.
12. Press [ ]
13. Press -( )-.
14. Enter <address>.

Editing the Operation

See the editing for the Get, Less Than, Equal To, and branching instructions.

Greater Than

A Greater Than comparison is also made with the Get/Less Than pair of instructions. This time the Get instruction BCD value is the reference and the Less Than instruction BCD value is the changing value. The Less Than value is compared with to the Get value for a greater than condition. When the Less Than value is greater than the Get value, the comparison is true and logic continuity is established.



If YYY is greater than 100 the Get/Greater Than comparison is true and 010/02 is energized.

Keystrokes

Enter a Greater Than comparison by performing the following steps.

1. Press -[G]-.
2. Enter <address>.
3. Enter <reference value>.
4. Press -[<]-.
5. Enter <address>.
6. Enter <reference value>.

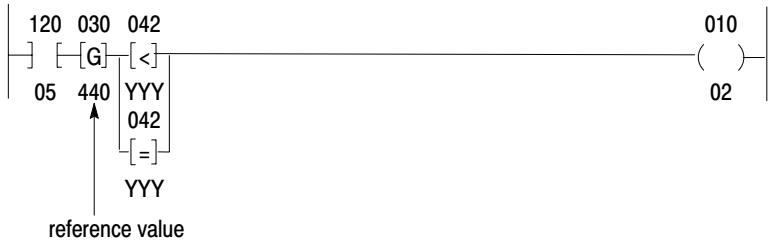
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Editing the Operation

See the editing for the Get and Less Than instructions

Equal To or Greater Than

This comparison is made using the Get, Less Than, Equal To, and branching instructions. The Get value is assigned a reference value. The Less Than and Equal To values are changing and are compared to the Get value. When the Less Than and Equal To values are greater than or equal to the Get value, the comparison is true and logic continuity is established.



If YYY is equal to or greater than 440 the Get/Equal To or Greater Than comparison is true and 010/02 is energized.

Keystrokes

Enter an Equal To or Greater Than comparison by performing the following steps.

1. Press -[G]-.
2. Enter <address>.
3. Enter <reference value>.
4. Press [ ].
5. Press -[=]-.
6. Enter <address>.
7. Enter <reference value>.
8. Press [ ].
9. Press -[<]-.
10. Enter <address>.
11. Enter <reference value>.
12. Press [ ].
13. Press -( )-.
14. Enter <address>.

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Editing the Operation

See the editing Get, Less Than, Equal To, and branching instructions.

Get Byte

The Get Byte instruction addresses either the upper or lower byte of a data table word. A 1 is entered after the word address for the upper byte; a 0 is entered for the lower byte.

The Get Byte instruction accesses 1 byte (instead of word) from one address in the data table. The data is displayed in octal format.

- The Get Byte instruction can be programmed with a Limit Test instruction located in the condition area of the ladder diagram rung.
- Do not place compare instructions between the Get Byte and Limit Test instructions.
- Use with a Put instruction to transfer either the upper or lower byte to the upper or lower byte of the Put instruction address.

Keystrokes

Enter a Get Byte instruction by performing the following steps.

1. Press -[B]-.
2. Enter <address>.
3. Enter <byte designation>.

Editing the Operation

Edit the Get Byte instruction by performing the following steps.

1. Position the cursor over -[B]-.
2. Press -[B]-.
3. Enter <address>.
4. Enter <byte designation>.

Get Byte/Put

The Get Byte instruction can be programmed either at the beginning of the rung or with one or more condition instructions preceding it. Condition instructions, however, should not be programmed after a Get Byte instruction. When one or more condition instructions precede the Get Byte instruction, they determine whether the rung is true or false.

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The Get Byte instruction addresses either the upper or lower byte of a data table word. A 1 is entered after the word address for an upper byte; a 0 is entered for the lower byte.

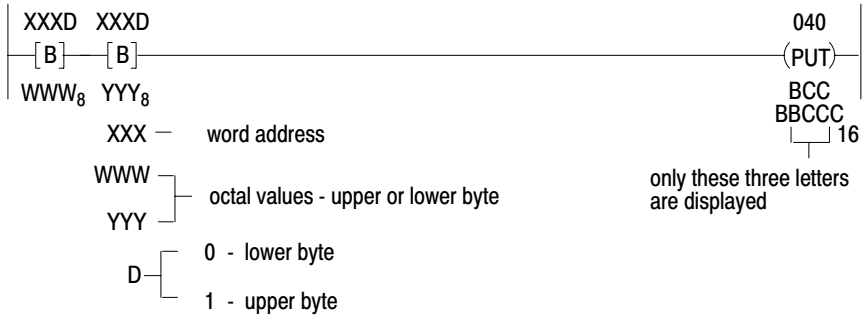
There are two ways to perform a Get Byte/Put instruction.

Case 1. One Get Byte



The Get Byte instruction is programmed in the condition area of the ladder rung. It tells the processor to make a duplicate of all 8 bits in the addressed byte. When the rung containing the Get Byte/Put instructions goes true, the data is transferred to both the upper and lower byte of the word address of the Put instruction.

Case 2. Two Get Bytes



Two Get Byte instructions are programmed in the condition area of the ladder rung. It tells the processor to make a duplicate of all 8 bits in each addressed byte. When the rung containing the Get Byte/Put instructions goes true, the data from the first get byte is transferred into the upper byte of the addressed Put instruction. Also, the data from the second get byte is transferred into the lower byte of the addressed Put instruction.

Keystrokes

Enter a Get Byte/Put instruction by performing the following steps.

1. Press -[B]-.
2. Enter <address>.
3. Enter <byte designation>.

Important: Repeat steps 1, 2 and 3 when using two Get Byte instructions.

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4. Press -(PUT)-.
5. Enter <address>.

Editing the Operation

Edit a Get Byte/Put instruction by performing the following steps.

1. Position the cursor over -[B]-.
2. Press -[B]-.
3. Enter <address>.
4. Enter <byte designation>.

Important: Repeat steps 2, 3 and 4 when using two Get Byte instructions.

5. Press -(PUT)-.
6. Enter <address>.

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Chapter 13

Three-Digit Math Instructions

Chapter Objectives

This chapter explains the three-digit math instructions.

Three-Digit Math

Your processor can perform four operations using three-digit math:

- addition
- subtraction
- multiplication
- division

These operations are not signed functions.

Addition

Reports the sum of two values from the two Get instructions immediately preceding the addition instruction. Programmed in the output position of the ladder diagram rung. The sum is stored in the add instruction word address.



When the sum exceeds 999, the overflow bit (bit 14) in the add instruction word is set. When the processor is operating in the Run/Program, Run, or Test mode, the overflow condition is displayed on the industrial terminal screen as a “1” preceding the sum.

If an overflow value (four digits) is used for subsequent comparisons or other arithmetic operations, inaccurate results could occur.



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Subtraction

Reports the difference between two Get values immediately preceding the subtraction instruction. The second get word value is subtracted from the first get word value. Programmed in the output position of the ladder diagram rung. The difference is stored in the subtract instruction word address.



When the difference is a negative number, the underflow bit (bit 16) in the subtract instruction word is set. When your processor is in the Run, Test or Run/Program mode, the negative sign is displayed on the industrial terminal screen preceding the difference.



Important: Use only positive values. If you use a negative BCD value for subsequent operation, inaccurate results could occur.

Multiplication

Reports the product of two values stored in the Get instruction words immediately preceding the multiply instruction. Programmed in the output position of the ladder diagram. The product is stored in two multiplication instruction words. The first word contains the most significant digit and the second word contains the least significant digit. If the product is less than six digits, leading zeros appear in the product.

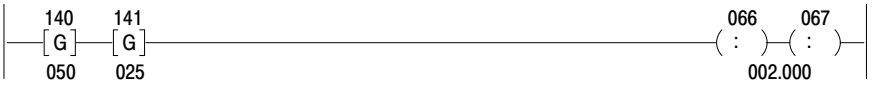


Important: Use consecutive word addresses for the two addresses of the multiply instruction.

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Division

Reports the quotient of two values stored in the two Get instructions immediately preceding division instruction. Programmed in the output position of the ladder diagram rung. The quotient is stored in two divide instruction words. The first word contains the most significant word and the second word contains the least significant digit.



Important: Use consecutive word addresses for the two addresses of the divide instruction. Quotient is expressed as a decimal, accurate to 3 decimal places. Any remaining data is rounded. Division by zero (including 0/0) gives the result of 999.999. This result differs from the PLC-2/20 and PLC-2/30 controllers where 0/0 = 1.000.



Entering a Three-Digit Math Instruction

Enter a three digit math operation by performing the following keystrokes.

1. Start the rung. Press -[G]-.
2. Enter <address>.
3. Enter <data> if appropriate.
4. Press -[G]-.
5. Enter <address>.
6. Enter <data> if appropriate.
7. Close the rung by pressing the appropriate math instruction key (Table 13.A).

Table 13.A
Three Digit Math Functions

Addition	-(+)-
Subtraction	-(-)-
Multiplication	-(x)-
Division	-(÷)-

8. Enter <address(es)>.

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Editing a Completed Rung

Edit a three-digit math operation by performing the following steps.

1. See chapter 12 and follow the editing procedure for a Get instruction.
2. Position the cursor over the math function.
3. Press the appropriate instruction key.
4. Enter <address(es)>.

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Chapter 14

EAF Math Instructions

Chapter Objectives

This chapter describes the EAF (Execute Auxiliary Function) math instructions. Table 14.A lists these instructions.

Table 14.A
EAF Function Numbers

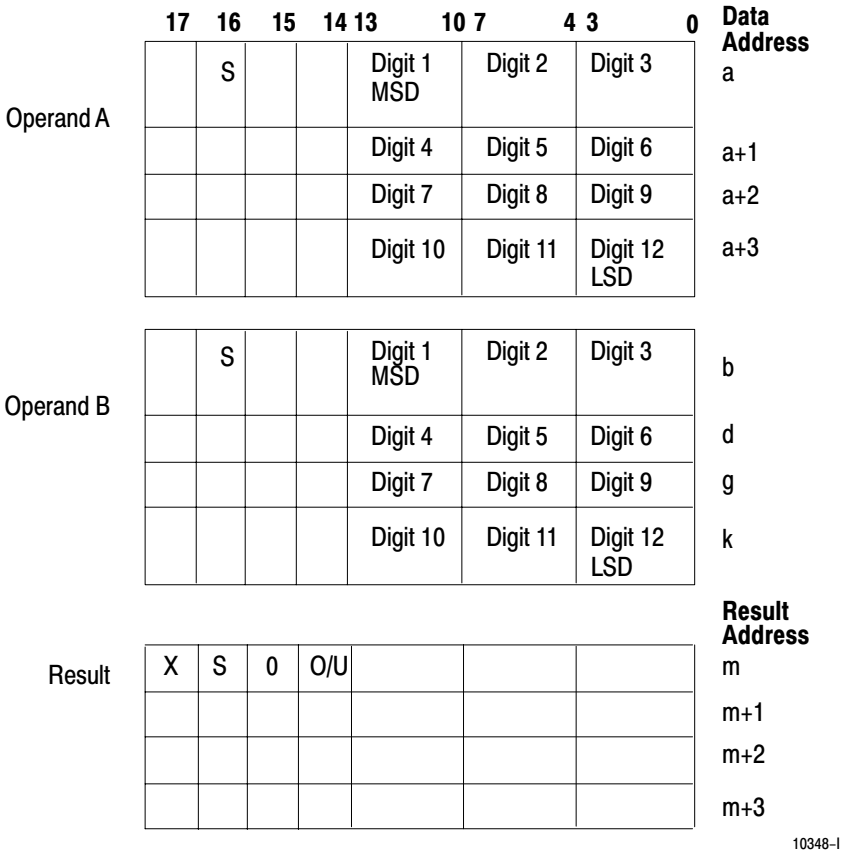
If you want to perform an operation of this type	Use this function number
The Mini-PLC-2/02, Mini-PLC-2/16, and Mini-PLC-2/17 can perform these functions.	
Addition	(01)
Subtraction	(02)
Multiplication	(03)
Division	(04)
Square Root	(05)
BCD to Binary	(13)
Binary to BCD	(14)
10^x	(37)
The Mini-PLC-2/17 can perform these additional functions.	
Y to the X ($y^{+/-x}$)	(33)
Powers of e ($e^{+/-x}$)	(32)
Reciprocal (1/x)	(34)

Two Operand EAFs

When a processor executes an EAF, it uses the data table format shown in Figure 14.1. Operands A and B represent the numbers you manipulate.

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Figure 14.1
EAF Two Operand Word and Digit Format in the Data Table



The Operands and the Result words have the format xxx xxx . xxx xxx. Only the Addition and Subtraction EAFs use all 12 digits. All other EAFs use 6 digits maximum, located anywhere within the 12 available digits. Legal formats are:

123456.	12.3456
12345.6	1.23456
1234.56	.123456
123.456	

Enter the operands from the keyboard of your 1770-T3 terminal or through ladder diagram instructions.

Operand A (which is the data address of the EAF instruction) can be placed in any legal address in the data table. However, you must select four consecutive addresses.

Important: Operand A does not need to be shown in the EAF rung.

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Operand B can have as many as 4 data table words. They must be in the same rung as the EAF. Conditioning statements are not permitted between these Gets and the EAF. This operand can use as many as 4 Gets, and their addresses do not have to be consecutive. See the data addresses of Operand B in Figure 14.1 (b, d, g, and k).

To enter the number ABC use only one Get or one data table word. If there is only one Get, the value is placed immediately to the left of the decimal point.

```
——[G]——                    xxx ABC . xxx xxx
+/– ABC
```

To enter the number ABC DEF use two Gets or two data table words.

```
——[G]——[G]——               ABC DEF . xxx xxx
+/– ABC   DEF
```

To enter the number ABC DEF . GHI use three GETs or three data table words.

```
——[G]——[G]——[G]——          ABC DEF . GHI xxx
+/– ABC   DEF   GHI
```

To enter the number ABC DEF . GHI JKL use four GETs or four data table words.

```
——[G]——[G]——[G]——[G]——  ABC DEF . GHI JKL
+/– ABC   DEF   GHI   JKL
```

The numbers have a fixed decimal point that is implied but not displayed.

The Result word can be placed in any legal location in the data table. The Result Address of the EAF points to the first result word. However, you must select four consecutive locations. Its word format is similar to the operands except there are 3 status bits.

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Bits 14-17 of the result word are reserved for status bits:

This Bit:	Stores this:
14	overflow/underflow 1 indicates overflow/underflow 0 result is in range
15	zero indicator 1 zero result 0 non-zero result
16	sign bit 1 negative (-) 0 positive (+)
17	not used

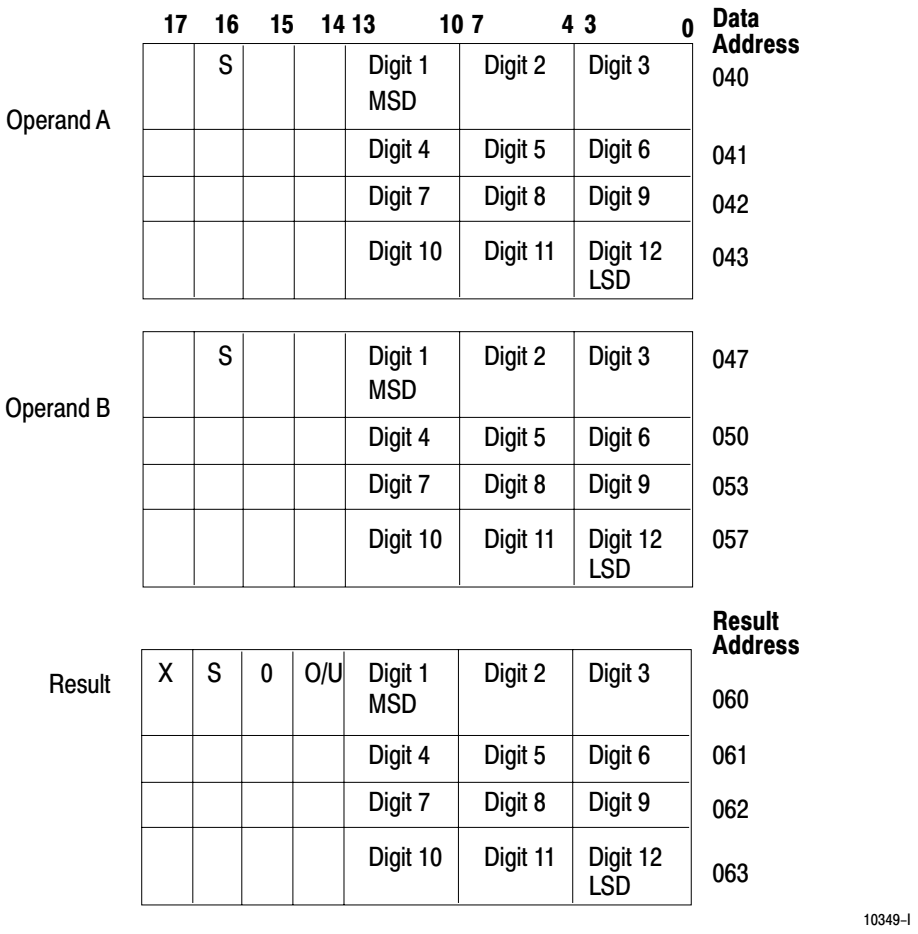
Data Table Format After Address Entry

If you select a data address of 040 for operand A, the EAF establishes a data table format with four consecutive words as shown in Figure 14.2. You can locate the result word anywhere in your data table. However, four consecutive word addresses must be available. If you select an address of 060 for the result, the EAF automatically reserves 061, 062 and 063.

Be careful not to select data and result addresses so that they overlap.

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Figure 14.2
EAF Word Format in the Data Table After Address Entry



Entry and Display of Input and Result Values

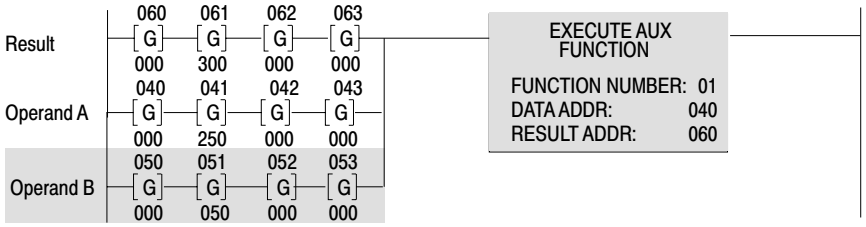
You can monitor the values in the Operands and Result words by entering the instructions shown in Figure 14.3. This figure shows one method for monitoring input and result values of an EAF instruction.

The shaded portion is called a primary ladder diagram. It contains Operand B and an EAF block. You can have as many as 4 Gets in this rung to select Operand B and they need not be consecutive data table addresses. Any rung conditions must be at the beginning of the rung. Nothing except a Branch End can be between the Gets and the EAF.

Operand A must have four consecutive data table word addresses. They can be stored anywhere in your data table.

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Figure 14.3
EAF Input and Result Rung



Keystrokes
Enter an EAF input and result rung (like Figure 14.3) be performing the following steps.

1. Press ⊤.
2. Enter Result and Operand branches.
3. Enter the values for Operands A and B. You can enter these values from the keyboard of your 1770-T3 terminal or through ladder diagram functions.
4. Complete the parallel branches.
5. Press [Shift] [EAF].
6. Enter the appropriate function number (Table 14.A).
7. Enter the data and result addresses for the EAF instruction.

ATTENTION: Do not enter data in hexadecimal. Enter all data in BCD. Failure to observe this warning could cause unwanted machine motion and may injure personnel.

Addition and Subtraction

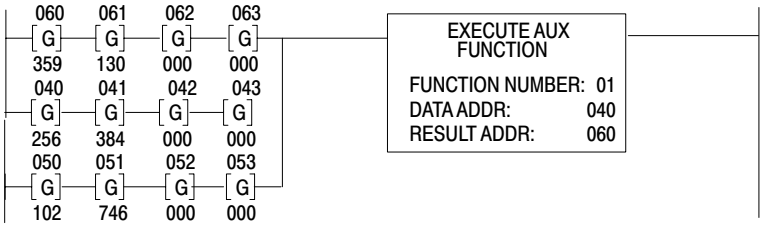
This EAF adds (or subtracts) two numbers. Word formats for addition or subtraction are the same. The only difference between the two EAFs is their function number: addition is 01 and subtraction is 02.

(+/– xxx xxx . xxx xxx) +/– (+/– xxx xxx . xxx xxx) = +/– yyy yyy . yyy yyy
or
(+/– Operand A) +/– (+/– Operand B) = +/– Result

Enter a rung like that shown in Figure 14.4

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Figure 14.4
EAF Addition Function Input and Display Rungs



Enter values for operands A and B. Entry of Operand A = 256384 and Operand B = 102746 produces the Result 359130 for addition (Figure 14.4) or 153638 for subtraction. Figure 14.5 shows how the words are stored in the data table.

Figure 14.5
EAF Addition Format in the Data Table After Execution

	17	16	15	14	13 10	7 4	3 0	Data Address
Operand A		0			2	5	6	040
					3	8	4	041
					0	0	0	042
					0	0	0	043
Operand B		0			1	0	2	050
					7	4	6	051
					0	0	0	052
					0	0	0	053
								Result Address
Result	X	0	0	0	3	5	9	060
					1	3	0	061
					0	0	0	062
					0	0	0	063

10350–I

Error Message

If the result has more than 12 digits, bit 14 is set (1) indicating overflow. Underflow does not exist for either addition or subtraction.

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Multiplication and Division

This EAF multiplies (or divides) two numbers. Word formats for multiplication and division are the same. The only difference between the two EAFs is their function numbers: multiplication is 03 and division is 04. Both of these functions limit calculations to six digits per operand, stored anywhere within the 12 available digits.

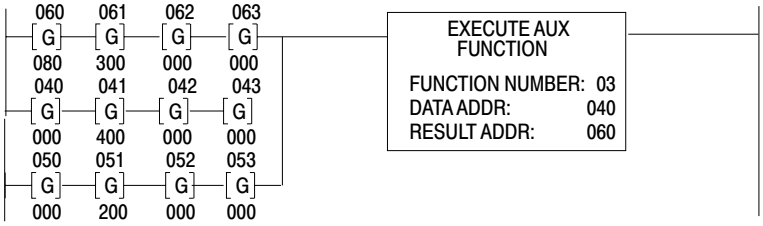
(+/– xxx xxx . xxx xxx) x or / (+/– xxx xxx . xxx xxx)= +/– yyy yyy . yyy yyy

or

(+/– Operand A) x or / (+/– Operand B) = +/– Result

Enter an EAF rung like that shown in Figure 14.6.

Figure 14.6
EAF Multiplication Input and Result Display Rungs

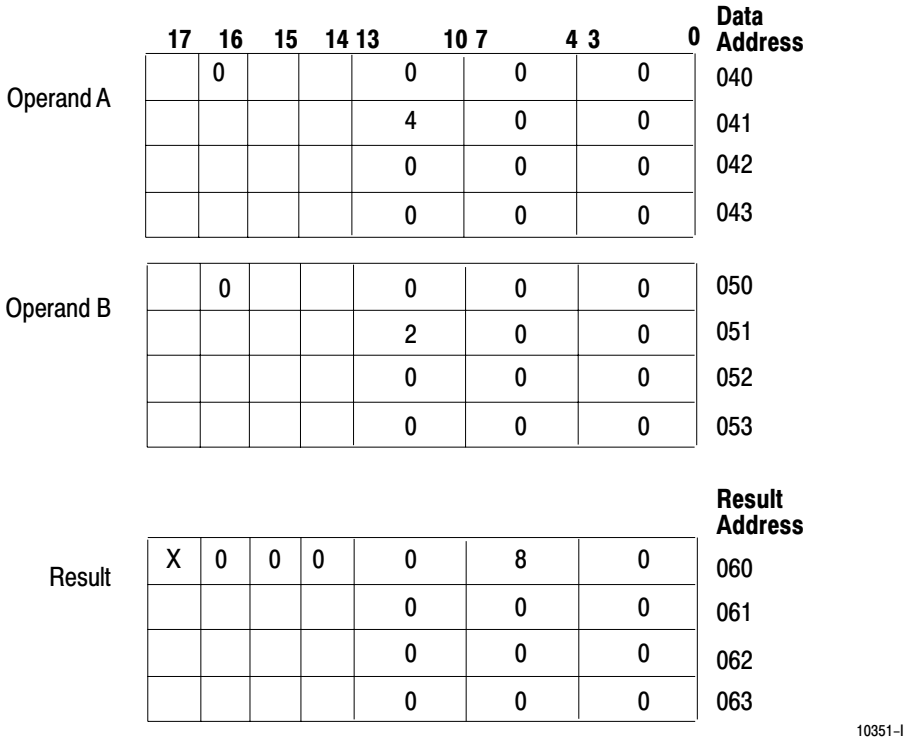


Enter the values for Operands A and B. The quotient of the Division EAF is expressed as a decimal. The first 5 most significant digits are accurate. Division by zero (including 0/0) gives the result of 999.999 and the overflow bit is set. This result differs from the PLC-2/20 and PLC-2/30 processors where 0/0 = 1.000.

Entry of Operand A = 000 400 000 000 and Operand B = 000 200 000 000 produces the result 080 000 000 000 for multiplication (Figure 14.6) or 000 002 . 000 000 for division. Figure 14.7 shows how the words are stored in the data table.

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Figure 14.7
EAF Multiplication Format in the Data Table After Execution



Y to the X

This EAF instruction is a feature of the Mini-PLC-2/17 processor only and finds the value of the equation $y^{+/-x} = r$. The Operand and Result words have the format:

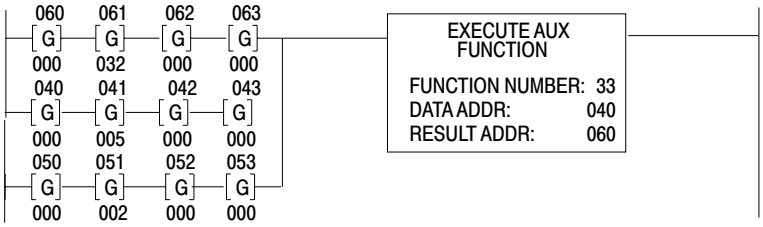
y = input base (positive only)
x = exponent (+/–)
r = resultant number (positive only)

yyy yyy . yyy yyy$^{+/-}$xxx xxx . xxx xxx = rrr rrr . rrr rrr

Enter an EAF rung like that shown in Figure 14.8.

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Figure 14.8
EAF Power Function Input and Display Rungs



Enter the values for the base and the exponent. Entry of y = 2 in word 050 and x = 5 in word 041 produces the result 32. Figure 14.9 shows how the words are stored in the data table. If a result has numbers beyond 12 digits, the result is truncated.

Figure 14.9
EAF Power of Y Format in the Data Table After Execution

	17	16	15	14	13	10	7	4	3	0	Data Address
Operand A		0			0	0		0			040
					0	0		5			041
		0			0	0		0			042
		0			0	0		0			043
Operand B		0			0	0		0			050
					0	0		2			051
					0	0		0			052
					0	0		0			053
											Result Address
Result	X	0	0	0	0	0		0			060
					0	3		2			061
					0	0		0			062
					0	0		0			063

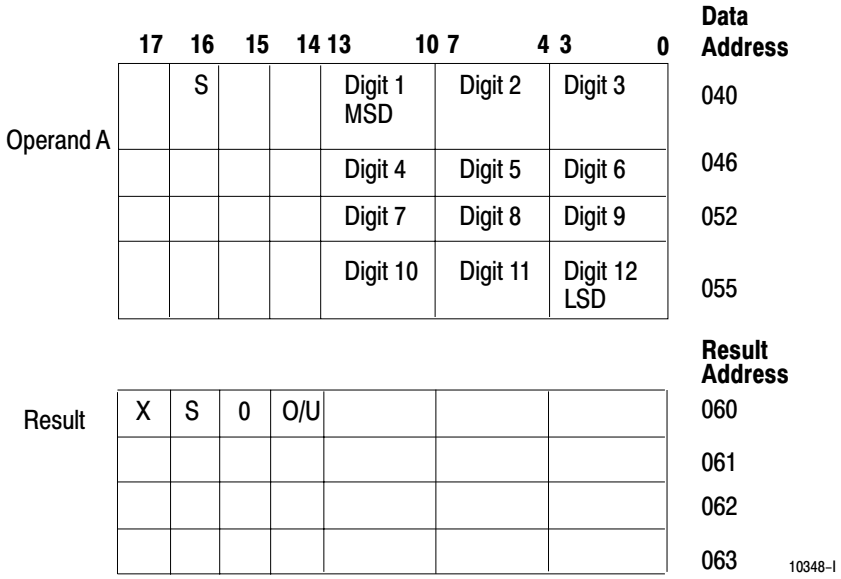
10352–I

One Operand EAFs

When a processor executes an EAF, it uses the data table format shown in Figure 14.10. The Operand represents a number you are going to manipulate.

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Figure 14.10
EAF One Operand Word and Digit Format in the Data Table



The Operand and the Result words have the format xxx xxx . xxx xxx. You can enter them from the keyboard of your 1770-T3 terminal or through ladder diagram instructions.

If you select a data address (inside the EAF) other than 010 for the Operand, you can locate the data anywhere in your data table. However, you must select four consecutive data table addresses (Figure 14.11).

If you choose to use the default address (010) as the data address of the EAF instruction, the processor seeks its data (operand) from the Get instructions in the rung. Address 010 will not be altered or used by this instruction. The Get instructions must be located in the rung immediately before the EAF instruction. You may select up to four data table addresses but they do not need to be consecutive addresses (Figure 14.10).

To enter the number ABC use only one Get or one data table word.

Important: If there is only one GET, the value is placed immediately to the left of the decimal point.

```
——[G]——                    xxx ABC . xxx xxx
+/– ABC
```

To enter the number ABC DEF use two Gets or two data table words.

```
——[G]——[G]——               ABC DEF . xxx xxx
+/– ABC   DEF
```


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To enter the number ABC DEF . GHI use three Gets or three data table words.

```
——[G]——[G]——[G]——          ABC DEF . GHI xxx
+/– ABC   DEF   GHI
```

To enter the number ABC DEF . GHI JKL use four Gets or four data table words.

```
——[G]——[G]——[G]——[G]——  ABC DEF . GHI JKL
+/– ABC   DEF   GHI   JKL
```

The numbers have a fixed decimal point that is implied but not displayed.

The Result word can be placed in any legal location in the data table. However, you must select four consecutive locations. Its word format is similar to the operand except that there are three status bits. Bits 14 to 16 of the Result word are reserved for status bits. These bits have the following meanings:

Bits 14-17 of the result word are reserved for status bits:

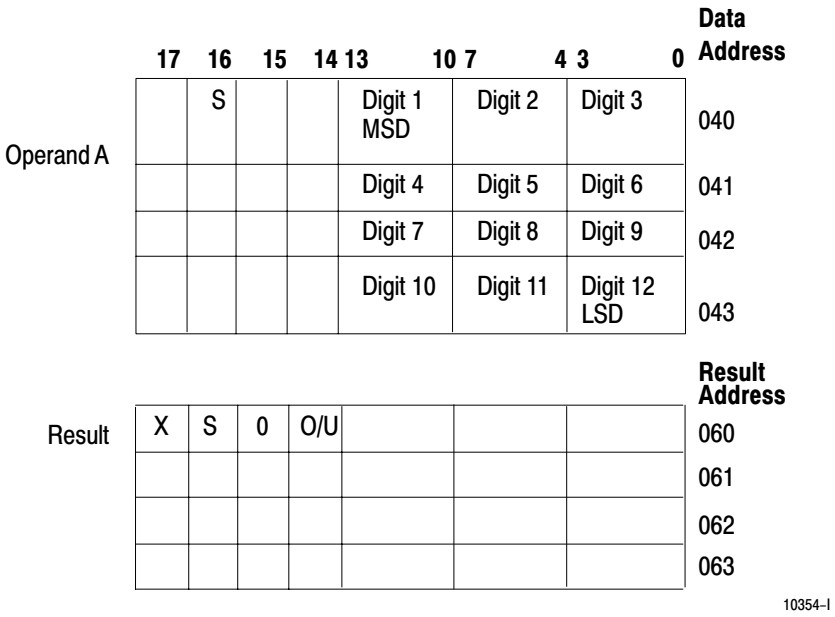
This Bit:	Stores this:
14	overflow/underflow **10 to the X** 1 you entered a number larger than 5.999 999 and the result indicates 999 999 0 result is in range **Reciprocal** 1 you tried to find the reciprocal of zero and the result indicates zero 0 result is in range
15	zero indicator 1 zero result 0 non-zero result
16	sign bit 1 negative (-) 0 positive (+)
17	not used

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Data Table Format After Address Entry

Be careful not to select data and result addresses so that they overlap.

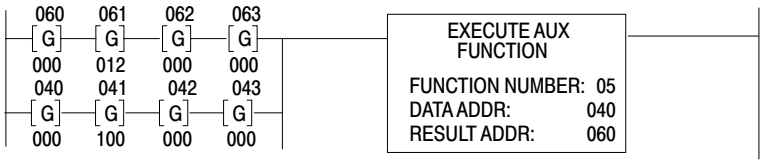
Figure 14.11
EAF Word Format in the Data Table After Address Entry



Entry and Display of Input and Result Values

Figure 14.12 shows one method for displaying input values and the result of an EAF. The first branch contains the Result. The second branch contains the Operand. The addresses of the Operand do not have to be consecutive if you use data address of 010.

Figure 14.12
EAF Input and Result Rung



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Keystrokes
Enter a one operand EAF (like Figure 14.12) by performing the following steps.

1. Press ⊤.
2. Enter result and data branch.
3. Enter the values for the Operand.
4. Complete the parallel branches.
5. Press [Shift] [EAF].
6. Enter the appropriate function number (Table 14.A).
7. Enter the data and result addresses of the EAF instruction.



ATTENTION: Do not enter data in hexadecimal. Enter all data in BCD. Failure to observe this warning could cause unwanted machine motion and may injure personnel.

Exponential and Square Root

The Exponential EAF instruction is a feature of the Mini-PLC-2/17 processor only.

Word formats for Exponential and Square Root functions are the same. The function number for the exponential function is 32 and the square root is 05. The operand and result are accurate to 6 decimal places for each function.

The exponential function finds the value of $e^{+/-x} = y$ (where e is approximately equal to 2.71828). The Operand and Result words have the format:

x = exponent of e
y = resultant number

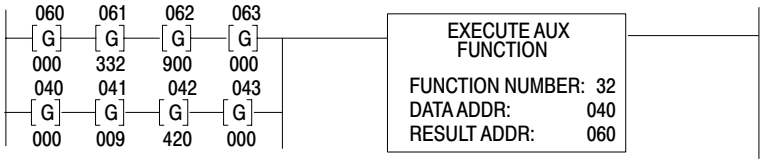
$$e^{+/-xxx\ xxx\ .\ xxx\ xxx} = yyy\ yyy\ .\ yyy\ yyy$$

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Exponential

Enter an exponential function EAF rung like that shown in Figure 14.13.

Figure 14.13
EAF Exponential Function Input and Display Rung



Enter values for the operand. You can enter these values from the keyboard of your 1770-T3 terminal or through ladder diagram functions. Entry of an operand (exponent of e) of 9.42 yields an exponential function value of 012 332 . 900 000. Figure 14.14 shows how it is stored in the data table.

Figure 14.14
EAF Exponential Format in the Data Table After Execution

	17	16	15	14	13 ... 10	7 ... 4	3 ... 0	Data Address
Operand A		0			0	0	0	040
					0	0	9	041
					4	2	0	042
					0	0	0	043

								Result Address
Result	X	0	0		0	1	2	060
					3	3	2	061
					9	0	0	062
					0	0	0	063

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Square Root

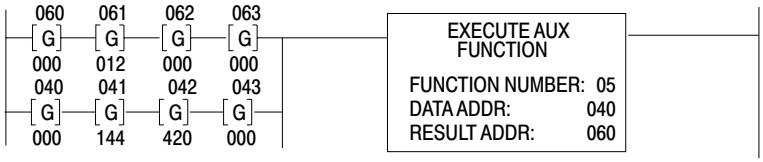
This function finds the value of $+x^{1/2}= y$. The Operand and Result words have the format:

$$+ xxx\ xxx\ .\ xxx\ xxx^{1/2}= + yyy\ yyy\ .\ yyy\ yyy$$

If you want to find the square root of a negative number, this function ignores the minus sign and finds the square root of the absolute value of the number.

Enter an EAF square root function like that shown in Figure 14.15.

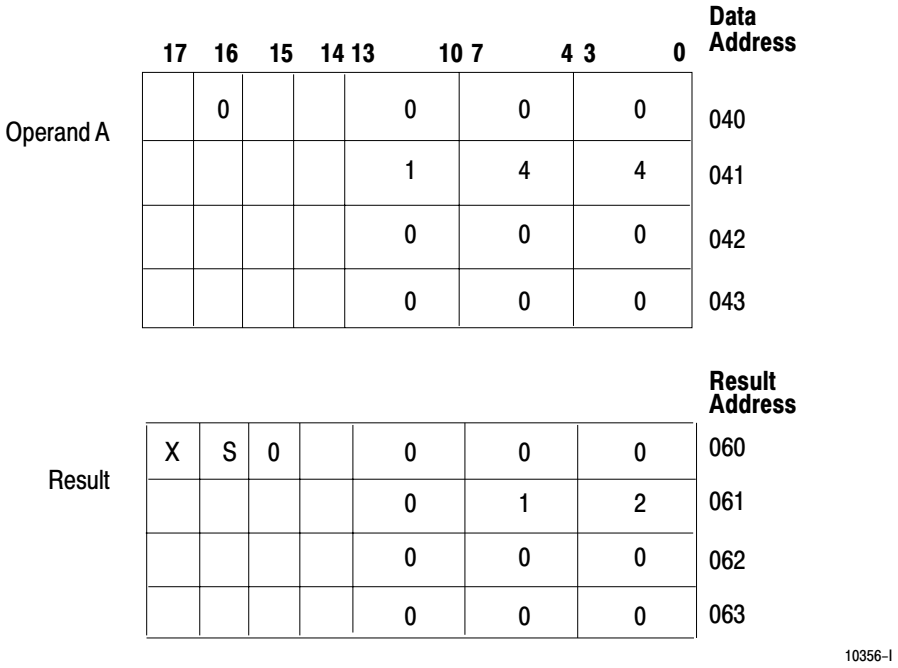
Figure 14.15
EAF Square Root Function Input and Display Rung



Enter the value for the Operand. You can enter this value from the keyboard of your 1770-T3 terminal or through ladder diagram functions. Entry of operand 144 produces the number 12. Figure 14.16 shows how the operand and the result are stored.

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Figure 14.16
EAF Square Root Format in the Data Table After Execution



10 to the X

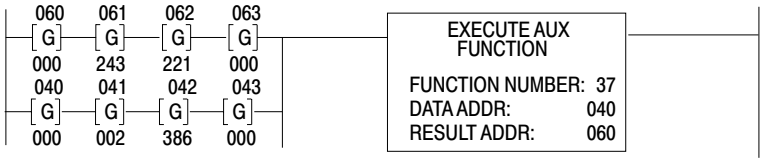
The 10 to the x function finds the value of $10^x = y$. The Operand and Result words have the format:

x = exponent of 10 (maximum value = 5.999 999)
y = resultant number (maximum of 6 digits)

$$10^{+/-x\ .\ xxx\ xxx} = yyy\ yyy\ .\ yyy\ yyy$$

Enter an EAF rung like that shown in Figure 14.17.

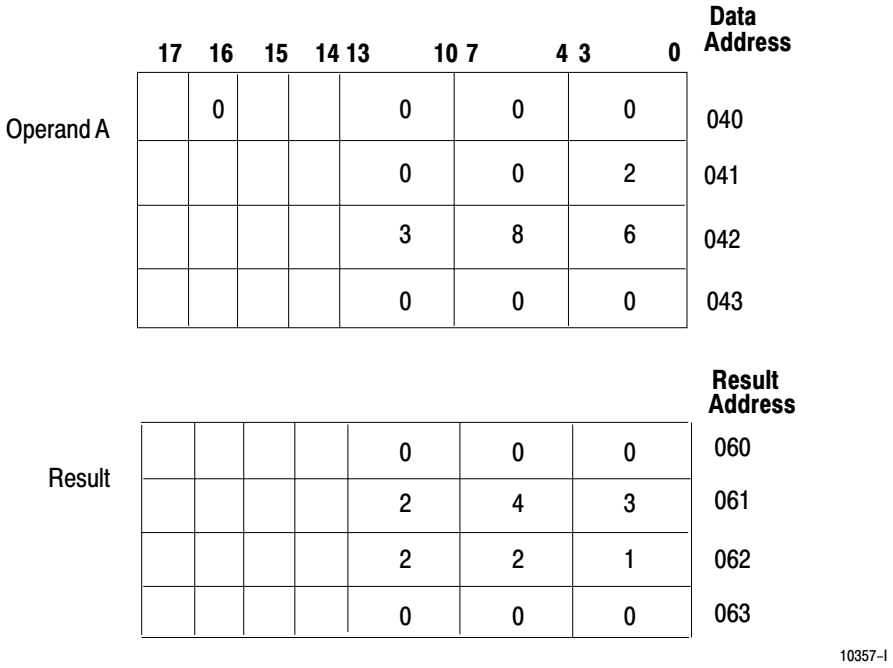
Figure 14.17
EAF Power of 10 Function Input and Display Rung



Enter values for the operand. You can enter these values from the keyboard of your 1770-T3 terminal or through ladder diagram functions. Entry of an operand (exponent of 10) of 000 002 . 386 000 yields an exponential value of 000 243 . 221 000. Figure 14.18 shows how it is stored in the data table.

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Figure 14.18
EAF Power of 10 Format in the Data Table After Execution



Reciprocal

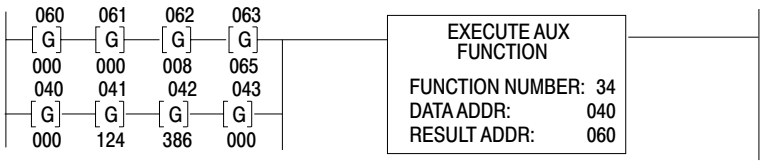
The Reciprocal EAF instruction is a feature of the Mini-PLC-2/17 processor only.

This EAF function finds the reciprocal of a number. The Operand and Result words have the format:

1/ +/–xxx xxx . xxx xxx = +/–yyy yyy . yyy yyy

Enter an EAF rung like that shown in Figure 14.19.

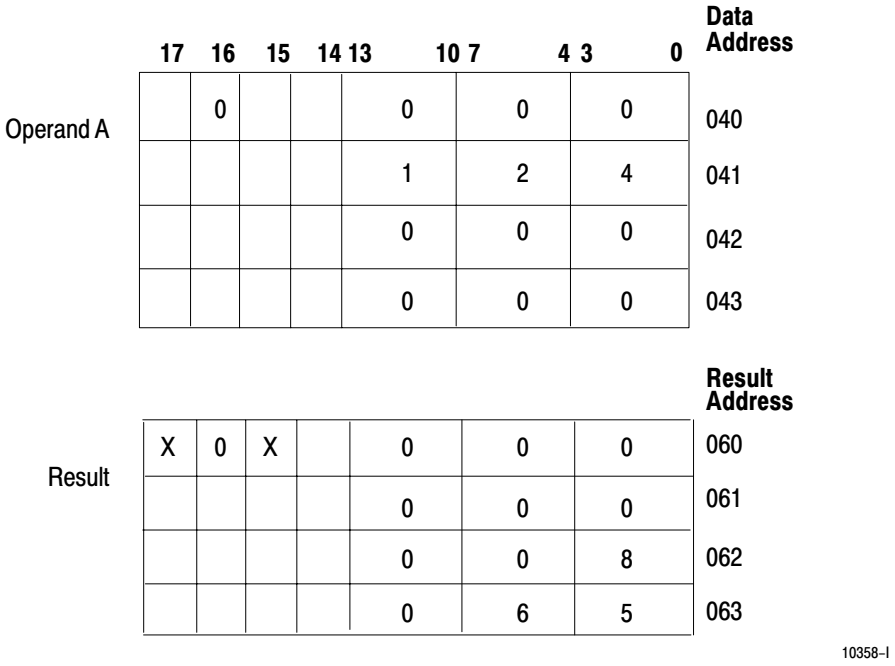
Figure 14.19
EAF Reciprocal Function Input and Display Rung



Enter the value for the operand. Entry of operand 124 yields as its reciprocal value 0.008065. Figure 14.20 shows how it is stored in the data table.

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Figure 14.20
EAF Reciprocal Format in the Data Table After Execution



BCD to Binary

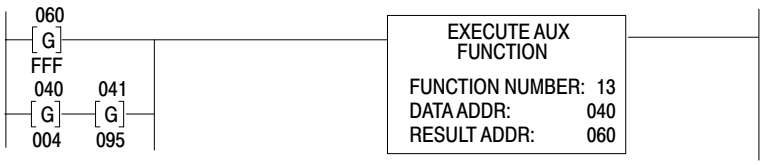
The BCD to Binary conversion function converts a BCD Conversion number into a binary number. Its function number is 13 and the conversion takes the form:

0xx xxx = y yyy

Important: When the result is displayed using a Get instruction, only the first 12 bits can be seen. Use a SEARCH 53 to look at all 16 bits.

Enter an EAF rung like that in Figure 14.21

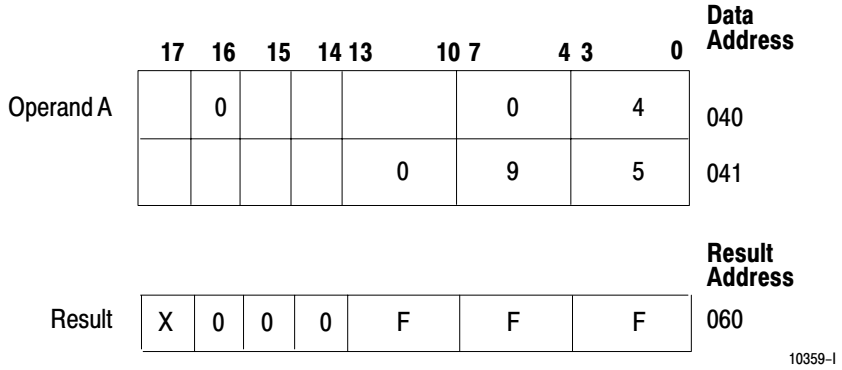
Figure 14.21
EAF BCD to Binary Conversion Function Input and Display Rung



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Enter the BCD number. Entry of the BCD number 004 095 produces the hexadecimal number FFF. If the Operand is greater than +32 767, the result 7FFFh is stored in the data table. However, you will see only FFF below the instruction. You must use a SEARCH 53 to see the entire word. If the Operand is more negative than –32 767, 8001 is displayed at the result address. All negative values are stored as two's complement. Figure 14.22 shows how the result is stored in the data table.

Figure 14.22
EAF BCD to Binary Conversion Format in the Data Table After Execution



Bit 16 of the first data address word is the sign bit of the BCD number. Bit 17 of the result address is the sign bit of the binary number. Bits 14-16 of the Result Address word are used if the operand is greater than 4095.

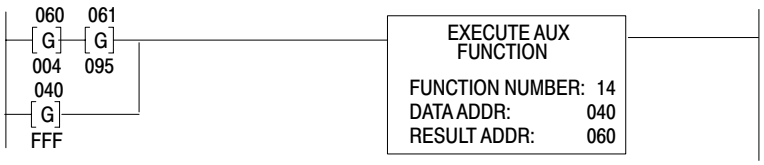
Binary to BCD

The BCD to Binary EAF function converts a Binary number into a BCD number. Its function number is 14 and the conversion takes the form:

x xxx = 0yy yyy

Enter an EAF rung like that in Figure 14.23

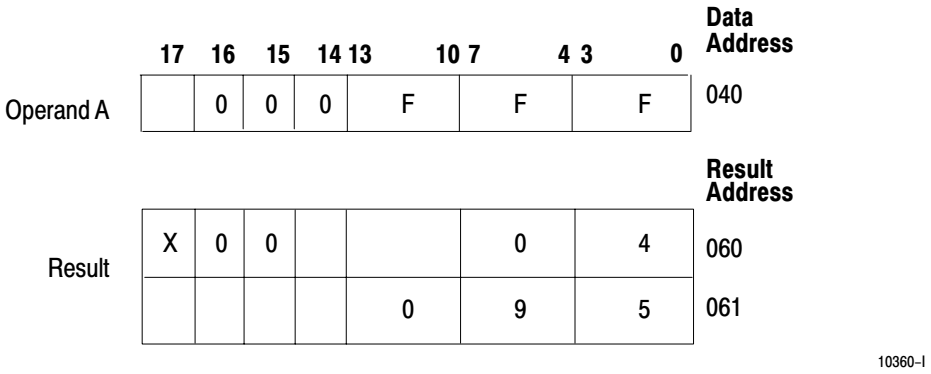
Figure 14.23
EAF Binary to BCD Conversion Function Input and Display Rung



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Enter a Binary number. Entry of the binary number FFF produces the BCD number 004 095. If you enter 7FFF (use SEARCH 53 and set the bits), 32 767 is displayed. All negative values are stored as two's complement. Figure 14.24 shows how the result is stored in the data table. Bit 16 of the first Result Address word is the sign bit of the BCD number.

Figure 14.24
EAF Binary to BCD Conversion Format in the Data Table After Execution



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Chapter 15

EAF Logarithmic, Trigonometric, and FIFO Instructions

Chapter Objectives

This chapter describes the Logarithmic, Trigonometric, and FIFO Load, and FIFO Unload EAF instructions.

Table 15.A
EAF Function Numbers

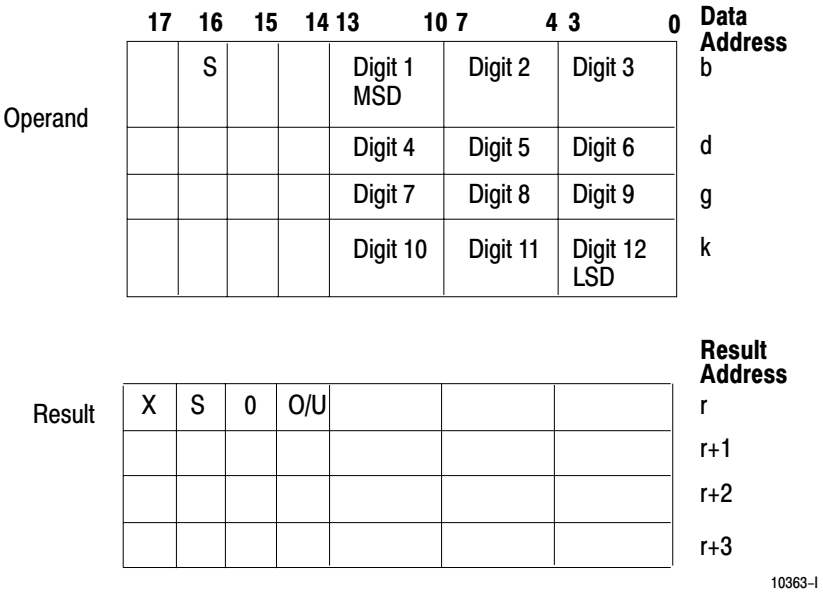
If you want to perform an operation of this type	Use this function number
The Mini-PLC-2/02, Mini-PLC-2/16 and Mini-PLC-2/17 can perform these functions	
FIFO Load	(28)
FIFO Unload	(29)
Log_{10}	(30)
Sin x	(35)
Cos x	(36)
The Mini-PLC-2/17 can perform these additional functions.	
Log_e	(31)

One Operand EAFs

When a processor executes an EAF, it uses the data table format shown in Figure 15.1. The Operand represents the number you manipulate.

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Figure 15.1
EAF One Operand Word and Digit Format in the Data Table



The Operand and the Result words have the format xxx xxx . xxx xxx. You can enter them from the keyboard of your 1770-T3 terminal or through ladder diagram instructions.

If you select a data address (inside the EAF) other than 010 for the Operand, you can locate the data anywhere in your data table. However, you must select four consecutive data table addresses (Figure 15.2).

If you choose to enter the default address (010) as the Data Address inside the EAF instruction, the processor seeks its data from the Get instructions in the Operand rung. Address 010 will not be altered or used by this instruction. The Get instruction must be located in the rung immediately before the EAF instruction. You may select up to four data table addresses (Figure 15.2). You can locate the Result word anywhere in your program. However, you must select four consecutive addresses for the result. If you select an address of 060 for the Result, the EAF automatically reserves the next three higher addresses.

To enter the number ABC use only one Get or one data table word.

Important: If there is only one Get, the value is placed immediately to the left of the decimal point.

——[G]——
+/– ABC

xxx ABC . xxx xxx

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To enter the number ABC DEF use two Gets or two data table words.

```
——[G]——[G]——                ABC DEF . xxx xxx
+/– ABC   DEF
```

To enter the number ABC DEF . GHI use three Gets or three data table words.

```
——[G]——[G]——[G]——            ABC DEF . GHI xxx
+/– ABC   DEF   GHI
```

To enter the number ABC DEF . GHI JKL use four Gets or four data table words.

```
——[G]——[G]——[G]——[G]——  ABC DEF . GHI JKL
+/– ABC   DEF   GHI   JKL
```

The numbers have a fixed decimal point that is implied but not displayed.

The Result word can be placed in any legal location in the data table. However, you must select four consecutive address locations. The Result word format is similar to the Operand format except that there are three status bits.

Bits 14-17 of the result word are reserved for status bits:

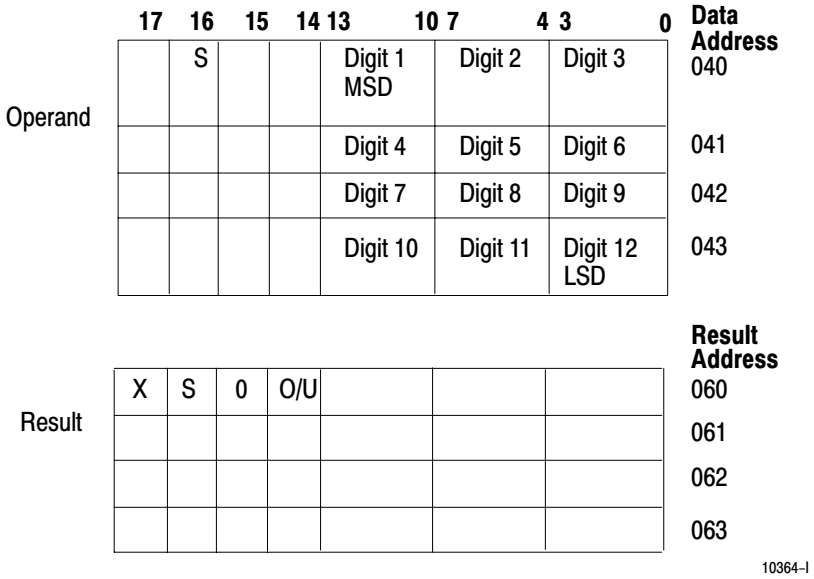
This Bit:	Stores this:
14	overflow/underflow 1 you entered a number that is out of range 0 result is in range **Log_{10} and Log_e** 1 you tried to find the log of zero and the result indicates zero; or you tried to fin the log of a negative number and the result indicates 999 999 . 999 999 0 result is in range
15	zero indicator 1 zero result 0 non-zero result
16	sign bit 1 negative (-) 0 positive (+)
17	not used

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Data Table Format After Address Entry

Be careful not to select operand (data) and result addresses so that they overlap.

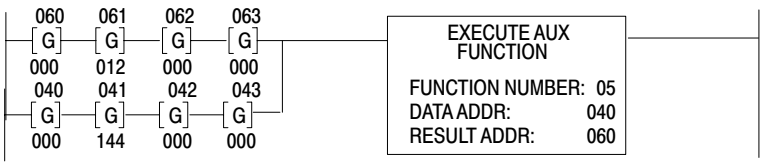
Figure 15.2
EAF Word Format in the Data Table After Address Entry



Entry and Display of Input and Result Values

Figure 15.3 shows one method for displaying operand (data) values and the result values of an EAF, not using the default address (010) as the Data Address inside the EAF instruction. The first branch contains the Result. The second branch contains the Operand. Addresses of the Operand do not have to be consecutive (if the Data Address in the instruction is 010).

Figure 15.3
EAF Operand and Result Rung



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Keystrokes
Enter an EAF input and result rung (like Figure 15.3) by performing the following steps.

1. Press ⊤.
2. Enter the **result** branch with its four Gets. Press ⊤ and enter the **operand** with its four Gets.
3. Enter the values for the Operand.
4. Complete the parallel branches.
5. Press [Shift] [EAF].
6. Enter the appropriate function number (Table 15.A).
7. Enter the data and result addresses.

ATTENTION: Do not enter data in hexadecimal. Enter all data in BCD. Failure to observe this warning could cause unwanted machine motion and may injure personnel.

Log to Base 10 or Log to Base e

The EAF log instruction is a feature of the Mini-PLC-2/17 processor only.

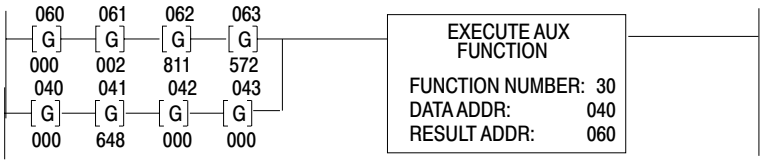
Word formats for $\log_{10}$ or the $\log_e$ are the same. The only difference between the two EAFs is their function number: $\log_{10}$ is 30 and the $\log_e$ is 31.

$\log_{10}$ xxx xxx . xxx xxx = 000 00y . yyy yyy

$\log_e$ xxx xxx . xxx xxx = 000 0yy . yyy yyy

Enter an EAF rung like that in Figure 15.4

Figure 15.4
EAF Log to Base 10 Function, Operand and Result Rung



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Enter the value for the operand. Entry of operand (base 10) = 648 produces the result 2.811572. Figure 15.5 shows how the result is stored in the data table.

Figure 15.5
EAF Log to Base 10 Format in the Data Table After Execution

Operand

17	16	15	14	13 10	7 4	3 0	Data Address
X	S	0	O/U	0	0	0	040
				6	4	8	041
				0	0	0	042
				0	0	0	043

Result

							Result Address
X	S	0	O/U	0	0	0	060
				0	0	2	061
				8	1	1	062
				5	7	2	063

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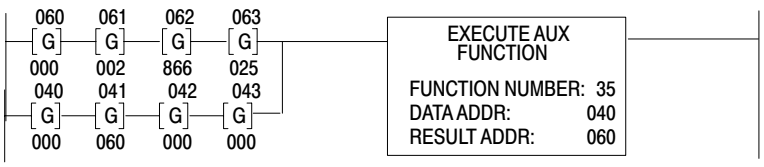
Sine and Cosine

This EAF trigonometric function finds the sine (or cosine) of an angle. The angle operand (data) is in degrees. Word formats for sine and cosine are the same. The only difference between the two EAFs is their function numbers: sine is 35 and cosine is 36. Both functions operate based on 6-digit operands.

sine +/–xxx xxx . xxx xxx = +/–yyy yyy . yyy yyy

Enter an EAF rung like that shown in Figure 15.6

Figure 15.6
EAF Sine Function, Operand and Result Rung

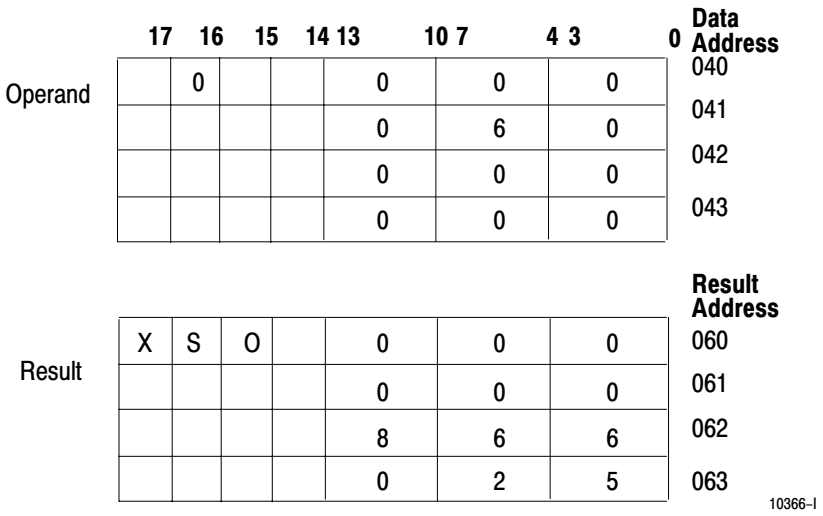


Enter the value of the angle in degrees (operand rung). Enter the angle from the keyboard of your 1770-T3 terminal or through ladder diagram instructions. Entry of the angle 060 in word 041 produces the result

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0.866025 for the sine function and and 0.500 for the cosine function. Figure 15.7 shows how it is stored in the data table.

Figure 15.7
EAF Sine Function Format After Execution



FIFO Load and FIFO Unload

The FIFO Load and FIFO Unload are output instructions that can be used together to construct an asynchronous word shift register. Length of the FIFO can be a maximum 999 words long.

- Upon a false-to-true transition of the FIFO Load rung, the contents of the Input Word is transferred into the File as long as the input word is non-zero.
- Upon a false-to-true transition of the FIFO Unload rung, the word at the top of the file (highest file address) is transferred out of the File to an Output Word.

Important: Only non-zero values can be loaded.

Use the full and empty flags in your ladder program to assure that the data being loaded/unloaded to/from the file is not lost or invalid.

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Bits 14-17 of the result word are reserved for status bits:

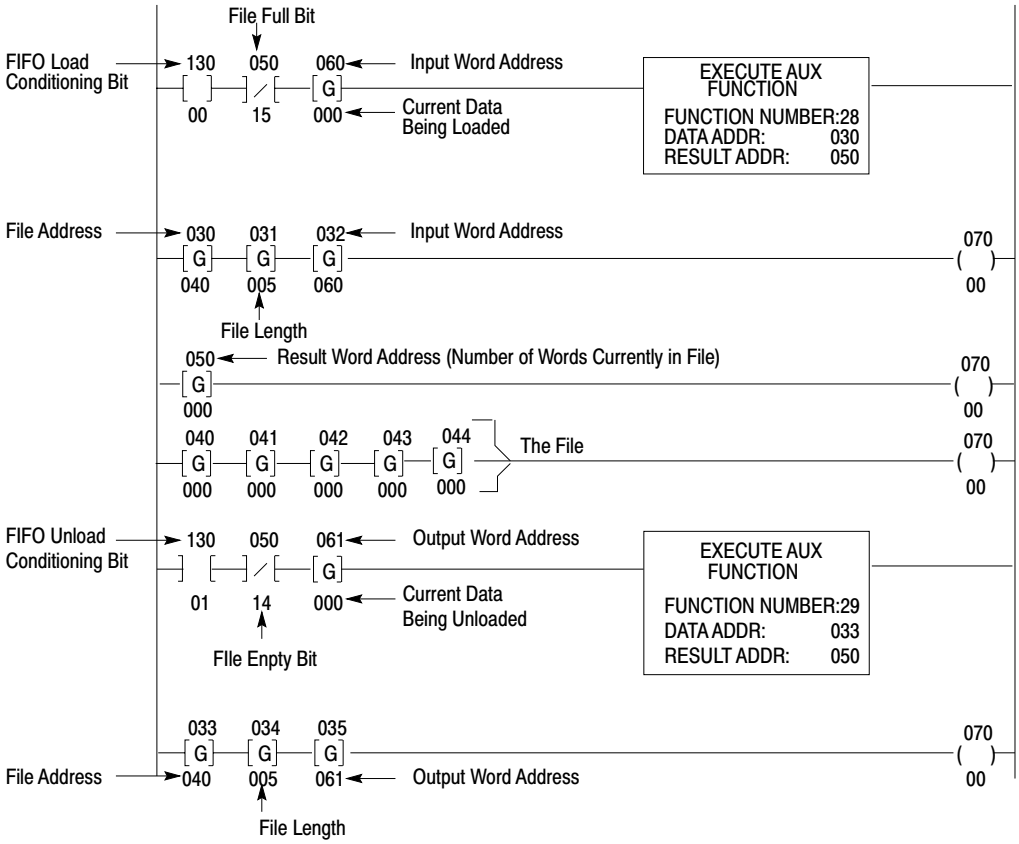
This Bit:	Stores this:
14	file empty indicator 1 file is empty 0 file has data You cannot unload data from an empty file. If the FIFO file is empty, there is no data to unload. Use this bit to condition a FIFO Unload.
15	file full indicator 1 file is full 0 file has data You cannot load data after the FIFO file is full. If you attempt to load any data it will be lost. As soon as you unload the first word, the bit resets (0). Use this bit to condition a FIFO Load. Data transfers with a false to true (0 to 1) transition of the EAF rung. You can monitor this transition with bits 16 or 17.
16	unload enabled 1 FIFO is enabled 0 FIFO is not enabled
17	load enabled 1 FIFO is enabled 0 FIFO is not enabled

Important: The FIFO Load and FIFO Unload instructions must have the same File Address, Result Address and File Length. Data is loaded into and unloaded from the same addressed file.

You can enter a ladder diagram for executing FIFO Loads and FIFO Unloads by entering a ladder diagram like that in Figure 15.8. This figure identifies all words and certain bits used in FIFO Load and FIFO Unload. Rungs 2, 3, 4 and 6 are included as display rungs and are not necessary for proper FIFO operation.

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Figure 15.8
FIFO Load and FIFO Unload Ladder Diagram



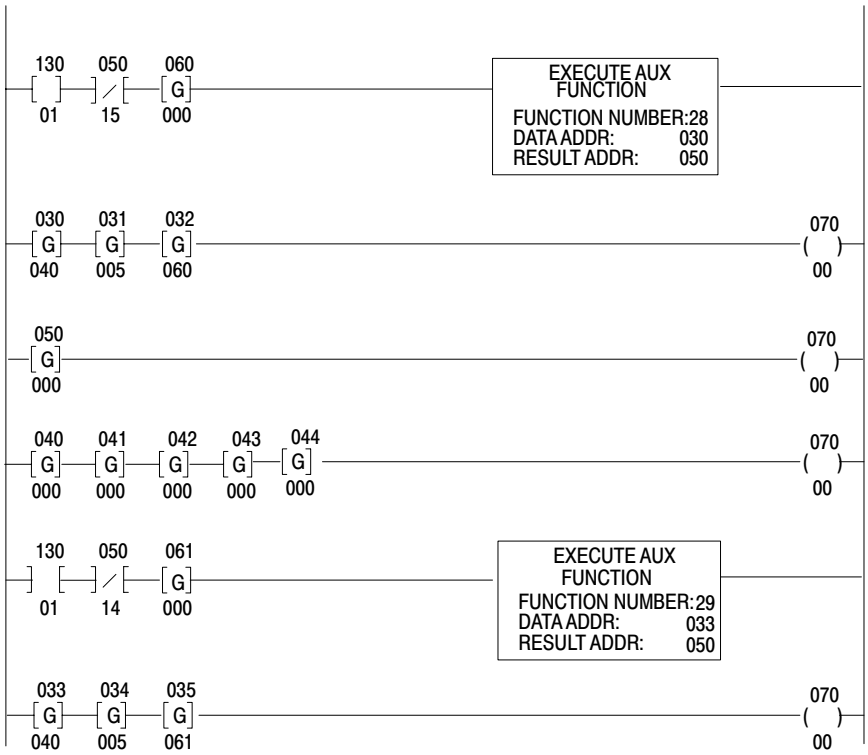
Important: Read chapter 19 and become familiar with the concepts introduced in this chapter before attempting FIFO instructions.

Figure 15.9 shows data (111) in the Input Word 060 ready to be loaded into the File. Toggle the precondition bit 13000 from false to true (0 to 1). Each time data is entered into the file, it is placed in the highest available address in the file. Observe that transferring data from the Input Word to the File does not destroy the data in the Input Word. Also, the Result Word (050) increments by 1 each time a transfer is performed. The Result Word indicates the number of words in your file at any given time. You can monitor the Result Word for this information.

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FIFO Load

Figure 15.9
First Data Is Ready to Be Loaded



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Figure 15.10 shows how the first data is stored in the data table before the FIFO Load is energized.

Figure 15.10
First Data Stored in the Data Table

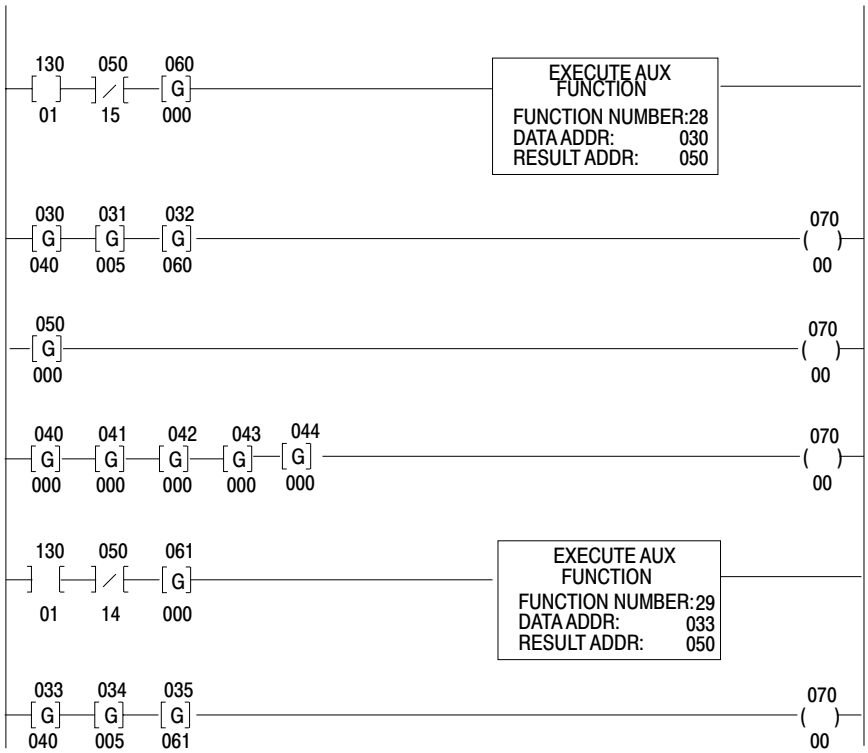
	17 10	07 00
030	0	4 0
031	0	0 5
032	0	6 0
033	0	4 0
034	0	0 5
035	0	6 1
040	0	0 0
041	0	0 0
042	0	0 0
043	0	0 0
044	0	0 0
050	0	0 0
060	1	1 1
061	0	0 0
130		0 0

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Figure 15.11 shows a full file. Inspect word 050 (Figure 15.12), you will find that bit 15 is set (1) indicating the file is full. Bit 17 follows the condition of the rung. Bit 17 is set (1) if the FIFO Load rung is true. Bit 17 is reset (0) if the rung is false.

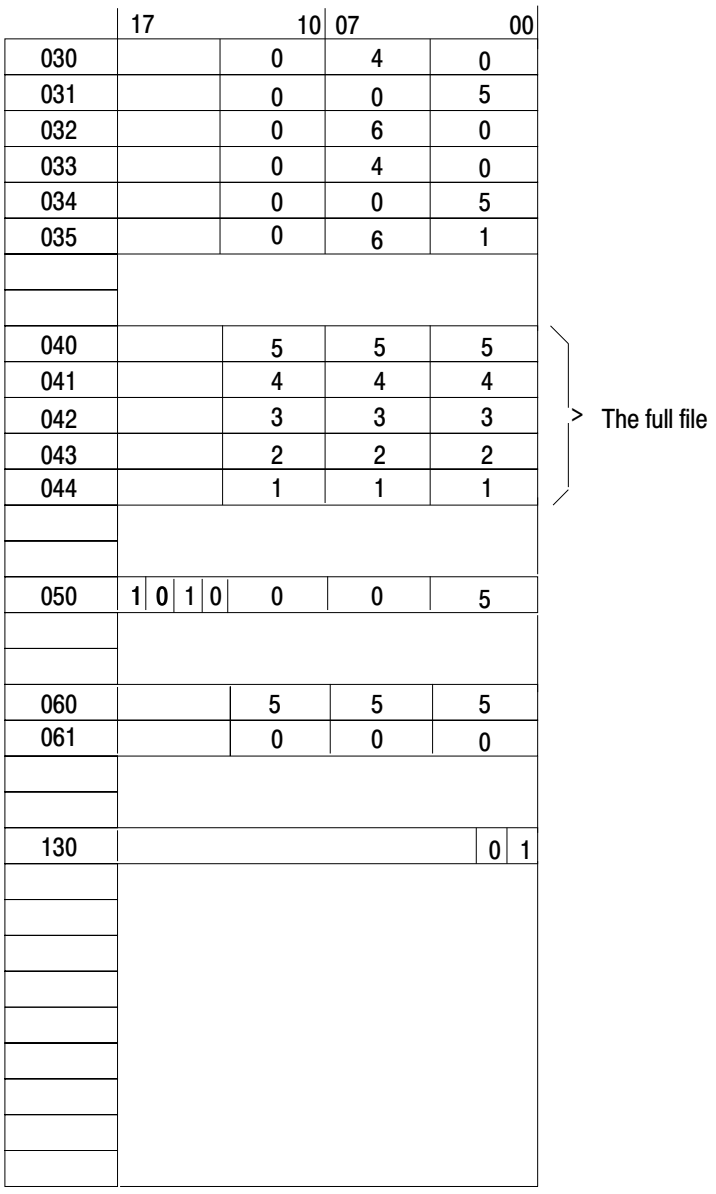
Figure 15.11
This Is a Full File of Five Words



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Figure 15.12 shows how a full file is stored in the data table.

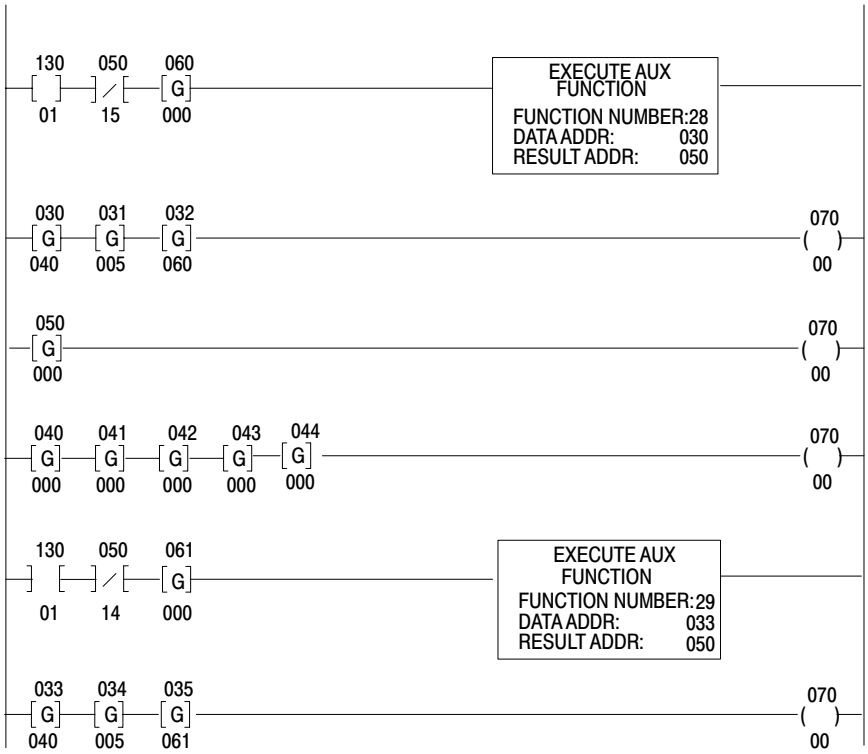
Figure 15.12
This Is a Full File Stored in the Data Table



If you want to load zero as valid FIFO data, insert zeros in the Input Word. Do a SEARCH 53, enter the address of the input word, and set any one of the upper four bits on. Set bit 15 since this is the designated “zero” bit for EAF instructions. Then, when you load the data into the file, the file will accept “zero” as valid FIFO data (Figure 15.13).

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Figure 15.13
Zero as Valid FIFO Data



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Figure 15.14 shows how zero is stored in the file as valid FIFO data.

Figure 15.14
Zero Stored in the Data Table

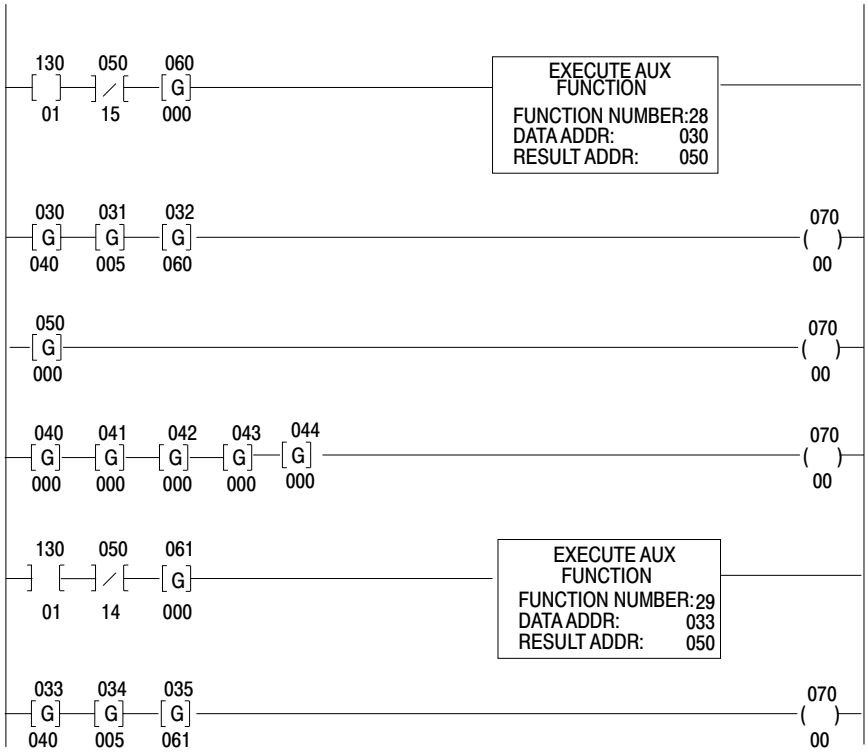
	17 10	07 00		
030	0	4	0	
031	0	0	5	
032	0	6	0	
033	0	4	0	
034	0	0	5	
035	0	6	1	
040	0 0 0 0	4	4	4	
041	0 0 1 0	0	0	0	← Zero is a valid number
042	0 0 0 0	3	3	3	
043	0 0 0 0	2	2	2	
044	0 0 0 0	1	1	1	
050	1 0 1 0	0	0	5	
060		4	4	4	
061		0	0	0	
130			0	1	

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If you want to keep zero as valid FIFO data, leave the bit set and it will progress through the file as any other word would. However, if you want to get rid of zero, you could reset the bit with ladder logic. The Result Word will not reflect the change until the next data is transferred into or out of the file. The zeros are then over-written. Valid data moves up to take the place of the zeros when either a FIFO Load or Unload executes (Figure 15.15).

Figure 15.15
Zero Has Been Eliminated

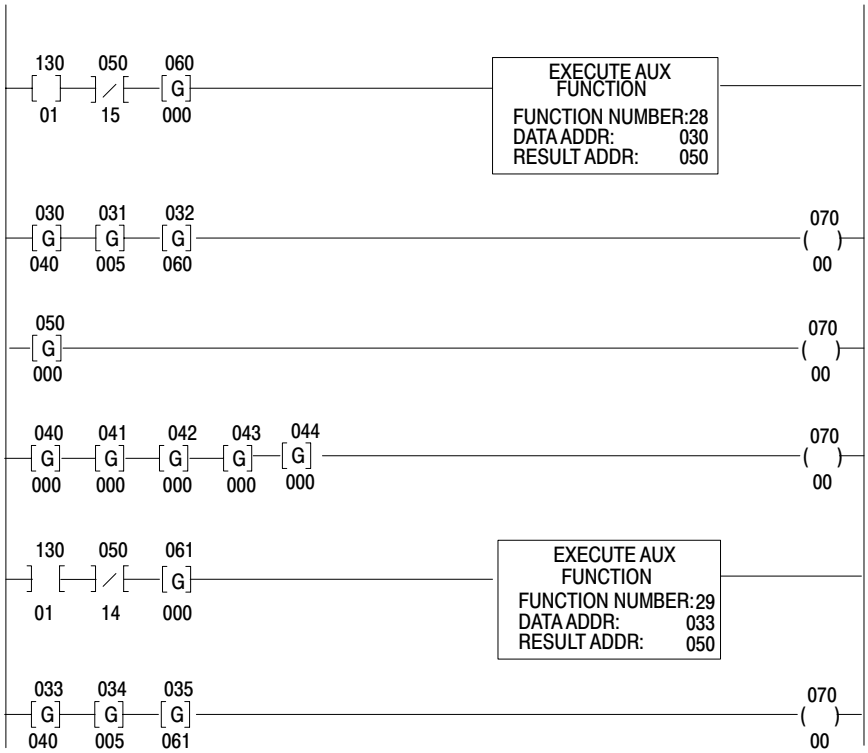


FIFO Unload

Figure 15.16 shows data unloaded from the file into the Output Word. Bit 16 of the output word follows the condition of the FIFO Unload rung. Bit 16 is set (1) if the rung is true. Bit 16 is reset (0) if the rung is false. Observe that 111 was the first data in the file and it is the first data out or first in – first out (FIFO). Also, the Result Word has decremented by one. It now shows four indicating that there are now four words in the file.

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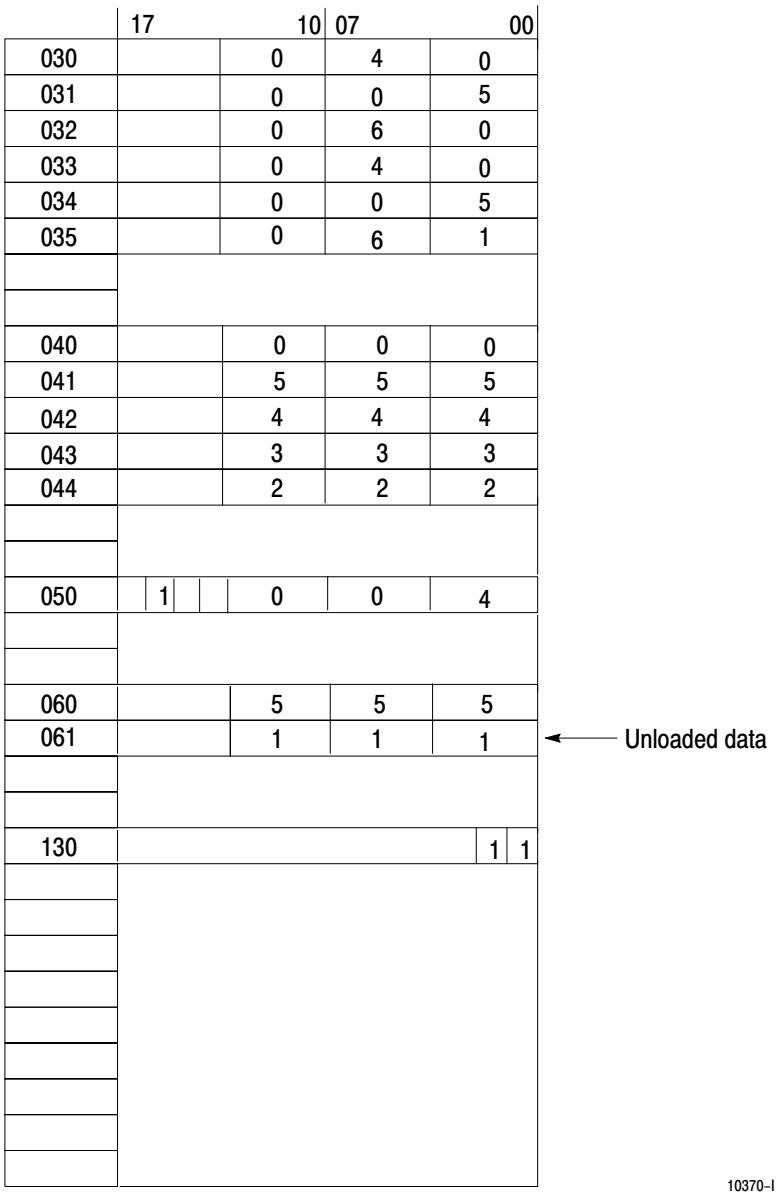
Figure 15.16
First Data Has Been Unloaded



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Figure 15.17 shows how the first unloaded data is stored in the data table.

Figure 15.17
Unloaded Data Stored in the Data Table



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Chapter 16

EAF Process Control Instructions

Chapter Objectives

This chapter describes the EAF Process Control instructions, which are a feature of the Mini-PLC-2/17 processor only.

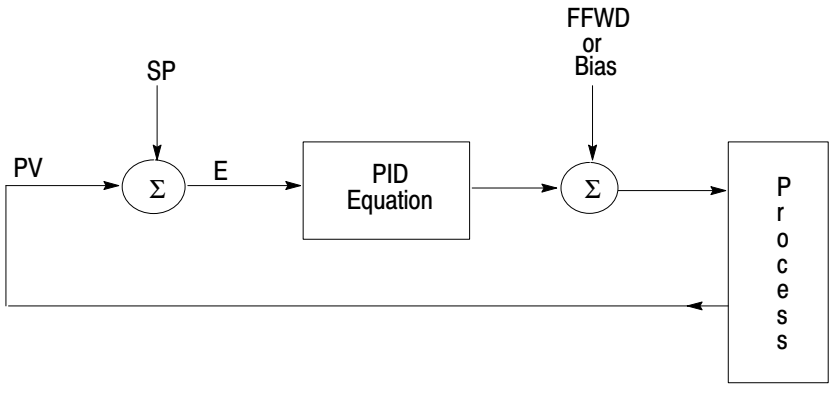
Table 16.A
EAF Function Numbers

If you want to perform an operation of this type	Use this function number
Only the Mini-PLC-2/17 can perform these functions	
PID	(06)
Averaging	(07)
Standard Deviation	(27)
Set Clock	(10)
Set Date	(11)
Set Leap Year and Day of the Week	(12)
Read Clock	(15)
Read Date	(16)
Read Leap Year and Day of the Week	(17)

PID Control

The PID EAF instruction lets the Mini-PLC-2/17 processor control regulating process loops for such quantities as pressure, temperature, flow rate, or fluid level (Figure 16.1). You configure your PID control instructions by selecting the desired features.

Figure 16.1
Closed Loop Control



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PID Features

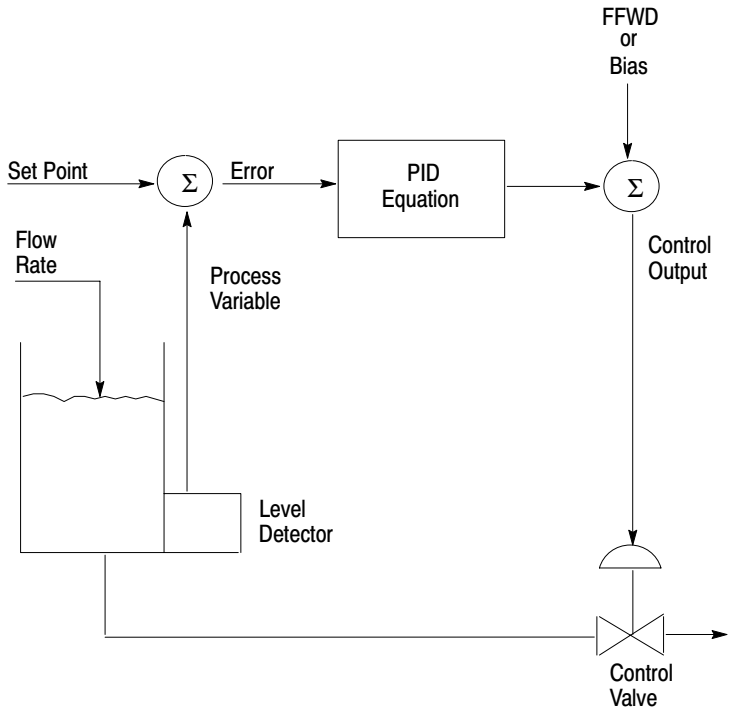
The PID EAF instruction provides the following features:

- Selectable dependent or independent gain PID equations
- Manual to automatic mode with bumpless transfer
- Derivative term calculates from PV or error
- Process variable and setpoint scaled to engineering units
- Output alarms
- Output limiting with anti-reset windup
- Zero crossing dead band
- Feedforward or output biasing
- Direct or reverse control action

Concepts

PID Closed Loop Control (Figure 16.2) holds a physical quantity such as pressure, temperature, or flow rate at a desired value (set point).

Figure 16.2
Loop Control With A PID Controller



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This is accomplished by evaluating the PID equation whose output goes to a control device. An additional value may be added to the control output either as a bias to decrease offset when using proportional control, or as a feedforward control value. The result of the calculation tends to drive the quantity that you are trying to control towards the desired value (set point).

The PID Equation = Proportional Term + Integral Term + Derivative Term + Bias Term

Select either of two equations: the Dependent Gains equation or the Independent Gains equation. Select the equation with which you are most familiar. There is no difference in the control capabilities; you can achieve comparable control with either equation. In the Dependent Gains equation, a change in the proportional term affects the integral and derivative terms. In the Independent Gains equation, you adjust the proportional, integral and the derivative terms independently.

Dependent Gains

The Dependent Gains equation is an interactive algorithm that contains variables dependent upon the controller gain. When you adjust your controller gain (K_C), you also change your integral and derivative terms.

$$CO = K_C \quad E + \frac{1}{Ti}\int_0^t Edt + T_D\frac{[E-E(n-1)]}{dt} \qquad + Bias$$

or, if derivation of PV is selected:

$$CO = K_C \quad E + \frac{1}{Ti}\int_0^t Edt + T_D\frac{[PV-PV(n-1)]}{dt} \qquad + Bias$$

where:

C	=	control output
K_C	=	controller gain constant (unitless)
Ti	=	integral time constant (minutes)
T_D	=	derivative time constant (minutes)
dt	=	time between samples (minutes)
Bias	=	feedforward or output bias
E	=	error equal to (PV – SP) or (SP – PV)
E(n-1)	=	error from last sample
PV	=	process variable
PV(n-1)	=	process variable from last sample

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Independent Gains

Using the independent gain equation you adjust the proportional, integral and derivative terms separately.

$$CO = K_P E + K_I \int_o^t Edt + \frac{KD[E - E(n-1)]}{dt} + Bias$$

or

$$CO = K_P E + K_I \int_o^t Edt + \frac{KD[PV - PV(n-1]}{dt} + Bias$$

where:

C=		control output
K_P	=	proportional gain constant (unitless)
K_I	=	integral gain constant (1/sec)
K_D	=	derivative gain constant (sec)
dt	=	time between samples
Bias	=	feedforward or output bias
E	=	error equal to (PV – SP) or (SP – PV)
E(n-1)	=	error from last sample
PV	=	process variable
PV(n-1)	=	process variable from last sample

You can convert dependent gain constants to independent gain constants by using the following formulas:

$K_P = K_C$

$K_I = K_C/(Ti(60 \text{ sec/min}))$

$K_D = K_C(TD)(60 \text{ sec/min})$

For more information about PID control, see the Fundamentals of Process Control Theory by Paul W. Murrill (Instrument Society of America).

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Loop Considerations

The number of PID loops, loop update time, and type of input and output modules are important considerations for using the PID instruction.

Consideration:	Description:
Number of PID loops	The number of PID loops that a Mini-PLC-2/17 processor can handle depends on the update time required by the loops. The longer the update time and the less sophisticated the loop control, the more loops can be controlled. Typically, when programmed in the selectable timed interrupt subroutine, the processor can control 16 loops which have a 100 ms loop update time. You can also program slower loops in the main ladder program. The PID instruction is a time-based calculation which can be triggered with timer done bits.
Loop update time	The PID instruction calculates a new control output (CO) whenever its rung changes from false to true. The PID instruction is a time-based calculation. Trigger the calculation with either timer done bits or a selectable timed interrupt subroutine to control its update time. In order for the PID instruction to operate predictably, the update time (term that you entered in word 14) must be equal to the rate at which the PID rung is toggled. The rung will be toggled at the timing value of the timer (preset x time base) or each time value of the STI. Deviation in toggle rate from the update time will degrade the accuracy of PID calculations. To get the accuracy suited to your process: • Program loops with fast response time in the selectable timed interrupt (STI) subroutine along with their corresponding block transfer instructions. • Program slower response loops in the main ladder program using timers to control the update time.

Programming

Block Transfer Instructions

Use block transfer instructions to transfer data between analog I/O modules and the PID instruction. Use a block transfer read instruction for input values, Process Variable (PV), and Tieback Use a block transfer write instruction for the Control Output (CO). Make each block transfer file address (Data File entry) the same address that you enter in the PID instruction respectively for the Process Variable, Tieback, and Control Output. Also, enter the module's location (rack, group, and module) in each block transfer instruction.

PID Instruction Input/Output Data Format

The PID instruction must access its PV (input) and deliver its output in a particular format:

- The series A and series B Mini-PLC-2/17 processor must use 12-bit binary format
- The series C (and later) Mini-PLC-2/17 processor lets you select 12-bit binary or 4-digit BCD.

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In both cases, PID data must be limited to a range of 0-4095. Set your analog input and output modules accordingly (by selection or by default in most analog modules).

The PID Output (resultant address) is always formatted in 12-bit binary, with a range of 0-4095. Scale your output module accordingly. If the module cannot be scaled to 0 to 4095 (for example, 1771-IR and -IX), the input range must be descaled (refer to the section on descaling inputs on page 16-23).

Tieback Input

Tieback is an optional input used only when a hardware automatic/manual station is connected. It allows the PID instruction to track the station for bumpless transfer from manual to automatic. If Tieback is not needed, program its Get instruction with a dummy address.

PID Control Block

The control block is 24 words long. You need the control block to enter parameters, their signs, and selected features. Use a File-to-File Move (File 10) and then a Hexadecimal Data Monitor (Display 1) to display and enter data into the control block. We recommend displaying only the first 17 words, since the last 7 words are reserved for use by the instruction. Set/reset status and sign bits of words 01 and 02 using a Binary Data Monitor (Display 0).

Each entry in the PID Control Block is displayed in 4-digit BCD. Parameters that must be entered directly into the control block (Set Output, Set Point, Feedforward, etc.) must be entered in this format only. For example, if the feedforward value is binary analog input, it must be converted to 4-digit BCD before being transferred into the PID Control Block.

The series D update added two new bits to Control Word 02: the Resume Control From Last State bit and the Bumpless Transfer With Proportional Controllers bit.

Resume Control from Last State

The Resume bit is located in the PID Control Block Word 02, Bit 10. When this bit is set, you can select a PID resume function to be performed when switching from Program to Run mode.

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Important: Do not set this bit when entering the PID instruction in Program mode. Since the PID instruction has not been executed yet, there is nothing to resume in Run mode. Set this bit only after the PID instruction has been executed in Run mode at least once**.**

Bumpless Transfer with Proportional Controllers

The Bumpless Transfer bit is located in the PID Control Block Word 02, Bit 11. This bit provides a bumpless transfer from manual mode to auto mode for loops that have no integral term (K_I=0).

When this bit is set, a Bias value is calculated and stored in the PID control file to account for the difference between the Proportional Term and the manually adjusted Control Output (CO). When you switch back to auto mode, this Bias value is added to the PID calculation to produce a CO value equal to the last manually adjusted CO value (thus achieving a bumpless transfer).

Important: In this mode, the range on the Feedforward is 0-FFFF (hexadecimal). The Feedforward/Bias Sign Bit (Word 02 Bit 02) is still valid.

Table 16.B, Table 16.C, Table 16.D and Table 16.E explain the functions of all of the words and bits in the PID Control Block.

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Table 16.B
Control Word 01 Bit Descriptions: Status Bits

00	–	Equation (Set by User) Independent Gain =0	Dependent Gain = 1
01	–	Mode (Set by User) Auto =)	Manual = 1
02	–	Control Action (Set by User) Direct (SP–PV) = 0	Reverse (PV–SP) = 1
03	–	Output Limiting (Set by User) No = 0	Yes = 1
04	–	Set Output (Set by User) Inhibited = 0	Enabled = 1
05	–	Cascade Bit (Set by User) 3 No = 0 Secondary Cascade Loop = 1	
06	–	Derivative Uses Error (set by User) 3 PV = 0	E = 1
07	–	Input Format (for Series C or later) Binary = 0 BCD = 1	
10	–	Dead Band (set by Instruction) 1 Out of DB = 0	Within DB = 1
11	–	Maximum Output Alarm (set by Instruction) 1 Within limit = 0	Above limit = 1
12	–	Minimum Output Alarm (Set by Instruction) 1 Within limit = 0	Below limit = 1
13	–	Set point Error (Set by Instruction) 1 In range = 0	Out of range = 1
14	–	Reserved 2	
15	–	Done bit (set by Instruction) 1 Not executed = 0 Executed = 1	
16	–	Reserved 2	
17	–	Enabled bit (set by Instruction) 1 Not enabled = 0	Enabled = 1

1 Do not change. Values are set by PID function.
2 Do not change Reserved bits.
3 Do not change while the processor is operating.

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Table 16.C
Control Word 02 Bit Descriptions: Status and SIgn Bits

00	–	K_Ix10 (Set by User) Do not move decimal = 0 Move decimal to right = 1
01	–	K_P/10 (Set by User) Do not move decimal = 0 Move decimal = 1
02	–	Feedforward/Bias Sign (Set by User) Pos = 0 Neg = 1
03	–	Maximum Scaling Sign (Set by User) Pos = 0 Neg = 1
04	–	Minimum Scaling Sign (Set by User) Pos = 0 Neg = 1
05	–	Set Point Sign (Set by User) Pos = 0 Neg = 1
06	–	Process Variable Sign (Set by Instruction) 1 Pos = 0 Neg = 1
07	–	Error Sign (Set by Instruction) 1 Pos = 0 Neg = 1
10	–	Resume Control From Last State 2 Disabled – on first scan, a new CO is calculated Enabled = on first scan, the accumulated integral value is back-calculated from the last CO value
11	–	Bumpless Transfer With Proportional Controllers 3 0 = no adjustment to Bias 1 = bumpless manual to auto mode by adjusting Bias

1 Do not change these values. They are set by the PID function.
2 This bit should only be set after the PID program has been run to obtain a valid last CO value
3 Do not change while the processor is operating.

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Table 16.D
Words 03 through 09

All range values are unitless unless noted otherwise.

Independent Gain Equation		**Dependent Gain Equation**
Range 0000-9999	Word 03 **Set Point – SP** 1	Range 0000-9999
Range 00.00-99.99	Word 04 **Proportional Gain**	Range 00.00-99.99
Term K_I Range Bit Set 0.000-9.999 Bit reset 0.000-9.999 Units rep/sec	Word 05 **Integral Gain**	Term 1/TI Range 00.00-99.99 Units rep/min
Term KD Range Bit set 00.01-99.99 Bit reset 000.1-999.9 Units – sec	Word 06 **Derivative Gain**	Term TD Range 00.00-99.99 Unites – min
Range 0000-4095 or 0000-FFFF 3	Word 07 **Feedforward – FFWD** 1	Range 0000-4095 or 0000-FFFF 3
Range 0000-9999	Word 08 **Maximum Scaling Value** 1 2	Range 0000-9999
Range 0000-9999	Word 09 **Minimum Scaling Value**	Range 0000-9999

1 Can be negative number by setting appropriate sign bits.
2 Do not change while processor is operating.
3 With word 02 Bit 11 set.

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Table 16.E
Words 10 through 24

Independent Gain Equation		Dependent Gain Equation
Range 0000-9999	Word 10 **Zero Crossing Dead Band**	Range 0000-9999 Units 0000-9999
Range 0000-100% Units Percent Range 0000-100% Unites Percent	Word 11 **Set Output Value** Word 12 **Maximum Control Output**	Range 0000-100% Units Percent Range 0000-100% Units Percent
Range 0000-100% Units Percent	Word 13 **Minimum Control Output**	Range 0000-100% Units Percent
Range 0000-99.99 Units sec	Word 14 **Loop Update Time**	Range 00.00-99.99 Units sec
Range 0000-9999	Word 15 **Process Variable – PV**	Range 0000-9999
Range 0000-9999	Word 16 **Error** [2]	Range 0000-9999
Range 0000-100% Units Percent	Word 17 **Control Output** [2]	Range 0000-100% Units Percent
	Words 18 through 24 Reserved [3]	

[1] Do not change while processor is operating.
[2] Do not change. These values are set by the PID function.
[3] Do not change Reserved bits.

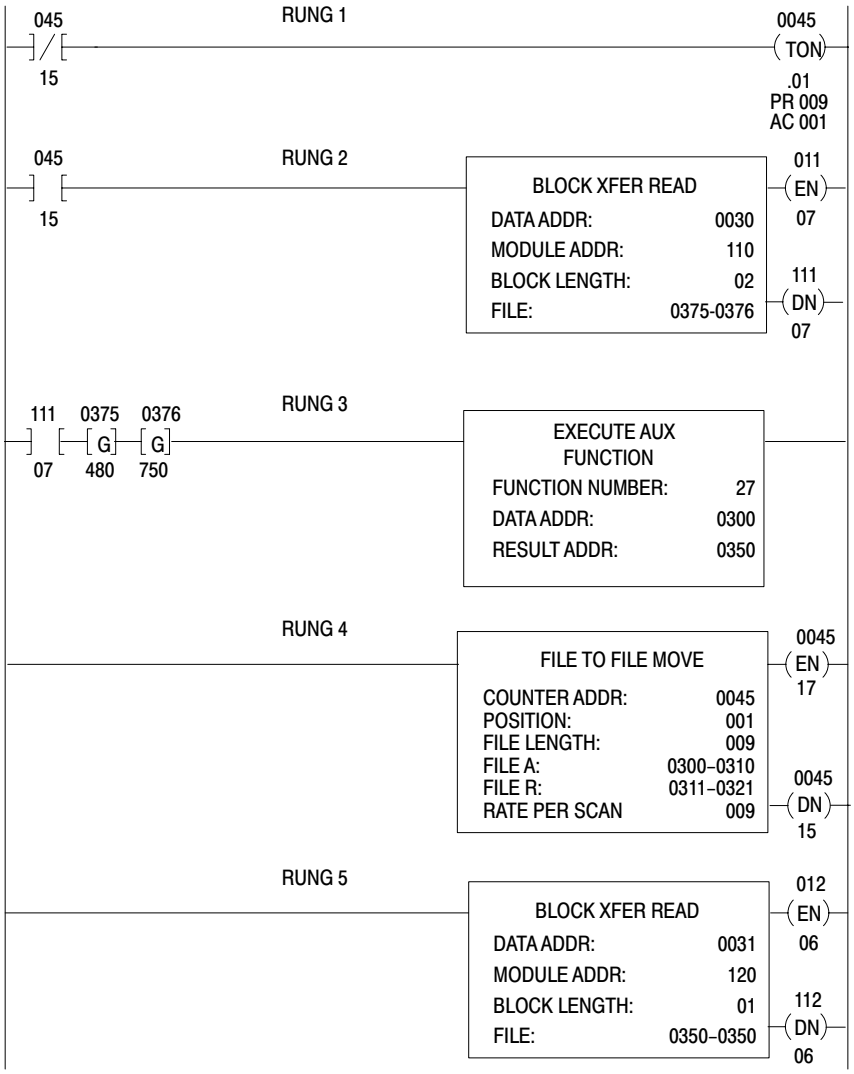
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Entry and Display of a PID Control Instruction

The following example programs show how to use the PID EAF. Figure 16.3 and the associated rung description give a detailed explanation of the basic sections of a PID program. We recommend that you study this example thoroughly before proceeding to the other example programs. The three programs that follow were programmed specifically for 1771-IF and 1771-OF modules.

Figure 16.3 shows how you can enter a ladder diagram in the main program and execute a PID function.

Figure 16.3
PID Ladder Diagram for Loops with a Minimum Update Time of 200ms



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Rung 1 This is a timing rung that toggles the block transfer. The timing value (preset x time base) must equal the loop update time of the PID instruction.

Rung 2 The Block Transfer Read instruction rung inputs the process variable (PV), tieback (TB) and feedforward/bias, if used.

Rung 3 The PID rung uses the block transfer done bit for conditioning and two GETs representing the tieback input and the process variable. The block transfer done bit gives the needed false-to-true transition to cause the PID instruction to calculate a new control output. Block transfer and PID calculation are then synchronized and each calculation is at the specified loop update time based on new data. Once you select an address for the Data Addr, the EAF automatically reserves the next 23 higher addresses for a total of 24 addresses (30 octal).

Important: The two Gets shown in the PID rung (Rung 3) are mandatory and must not be separated from the EAF by any other instruction.

The first Get contains data to be used as the tieback (TB) input. The second Get contains the process variable (PV) input to the PID calculation. The addresses of the two Gets do not have to be consecutive. You must enter both Gets, even if TB is never used.

The EAF block contains the function number, a Data address, and a Result address. The function number for the PID instruction is 27. The Data address points to the PID control block. The control block contains a list of parameters needed to solve the PID equation and select the PID control options. The Result address points to the location of the control output (CO) or output of the PID EAF.

Rung 4 This rung is a FIle-to-File Move used to display or input equation parameters and set sign and status bits. The rung is conditioned with a Branch End to ensure that the rung is never executed.

Rung 5 The Block Transfer Write is used to relay the control output to the final actuator. The File Address must be the same as the Result Address in the EAF Block of the PID rung.

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Entry and Display of a Selectable Timed Interrupt (STI) Controlled PID Function

Figure 16.4 shows you how to enter and display an STI to execute a controlled PID function. The program that follows is programmed specifically for 1771-IE, -IF, -OF, -IX and -IY modules. For the 1771-IFE, -IL and -IR modules, add the module initialization rungs in the main program (see Figure 16.5).

The processor executes 16 PID loops with an update time of 100 ms. Eight loops are executed each alternate scan (50 ms STI): the first 8 on scan 1, the second 8 on scan 2, the first 8 on scan 3, the second 8 on scan 4. Since the PID instruction needs a leading edge transition to execute (false-to-true), you must use the alternate scan method even if you use less than 8 loops.

The Immediate Output Update (IOT) instructions are required. Place them after each block transfer instruction. The IOT instructions cause the block transfer to be requested and completed immediately, instead of at the next program scan. The address of the IOT is the same as the address of the block transfer enable bit.

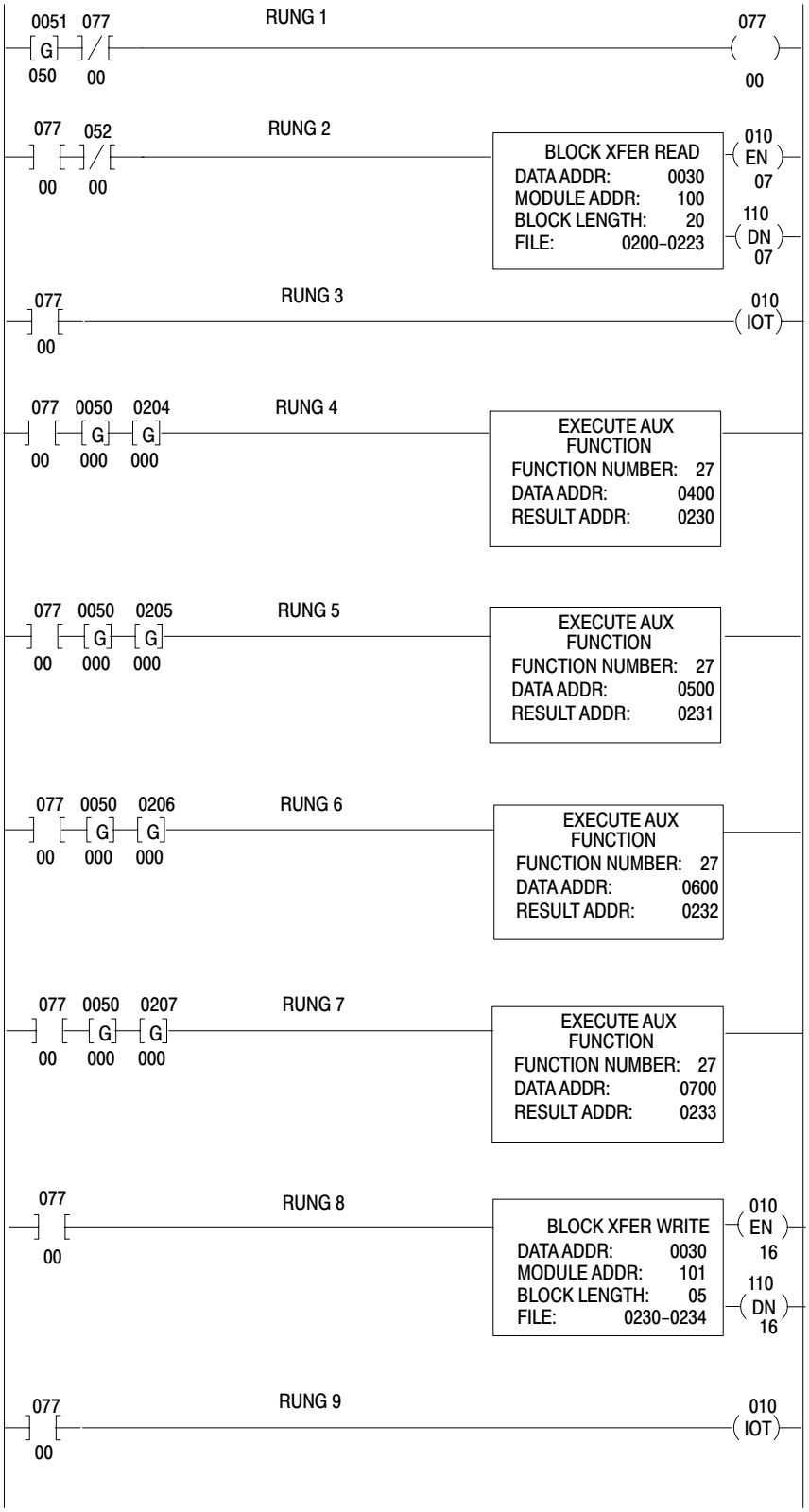
Observe there is no data buffering on the Block Transfer Read (BTR) instruction. The BTR done bit cannot be made to report predictably in the STI. Therefore, it can’t be used to buffer data.

If you want to program less than 16 loops, eliminate a PID EAF rung. However, once you have eliminated four EAF rungs, you must eliminate the associated Block Transfer Write (BTW) and IOT instructions.

Place an unconditionally false File-to-File instruction in the main program to display the configuration of the PID loops.

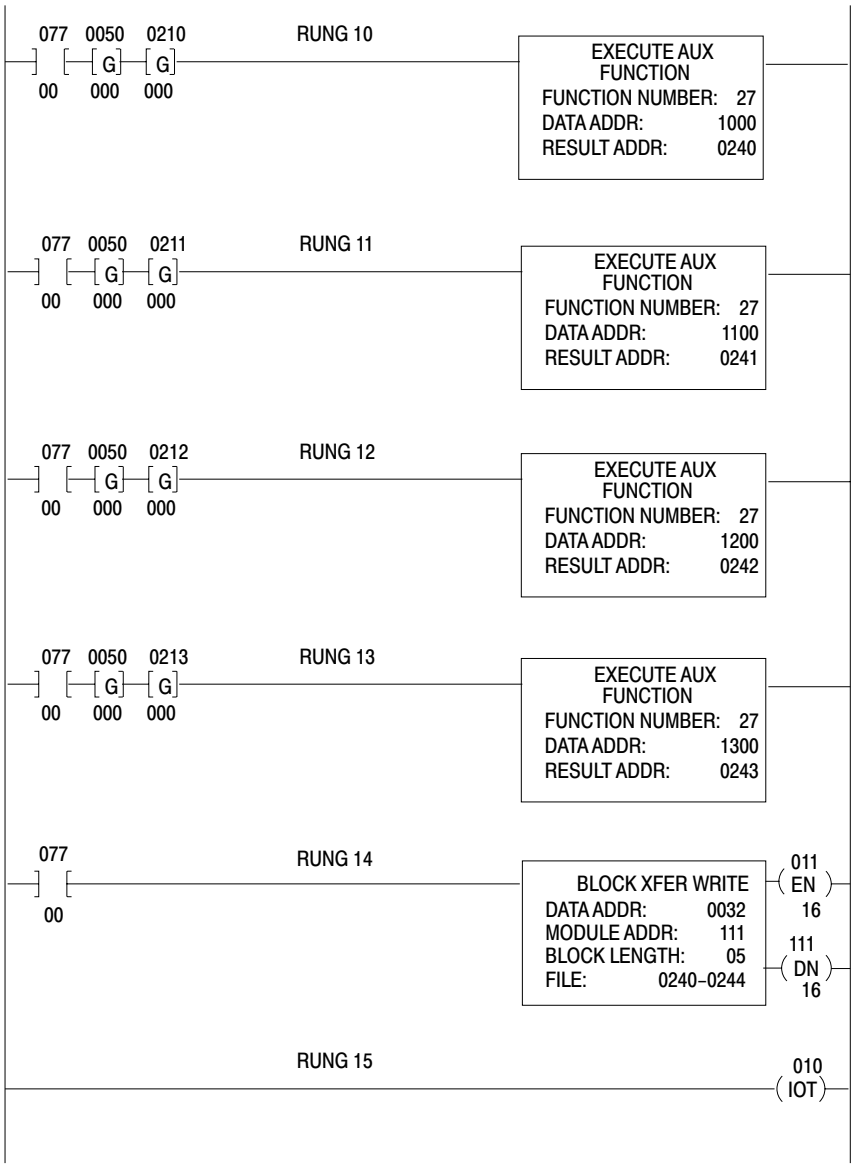
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Figure 16.4
Selectable Timed Interrupt Example (the first 4 PID instructions)



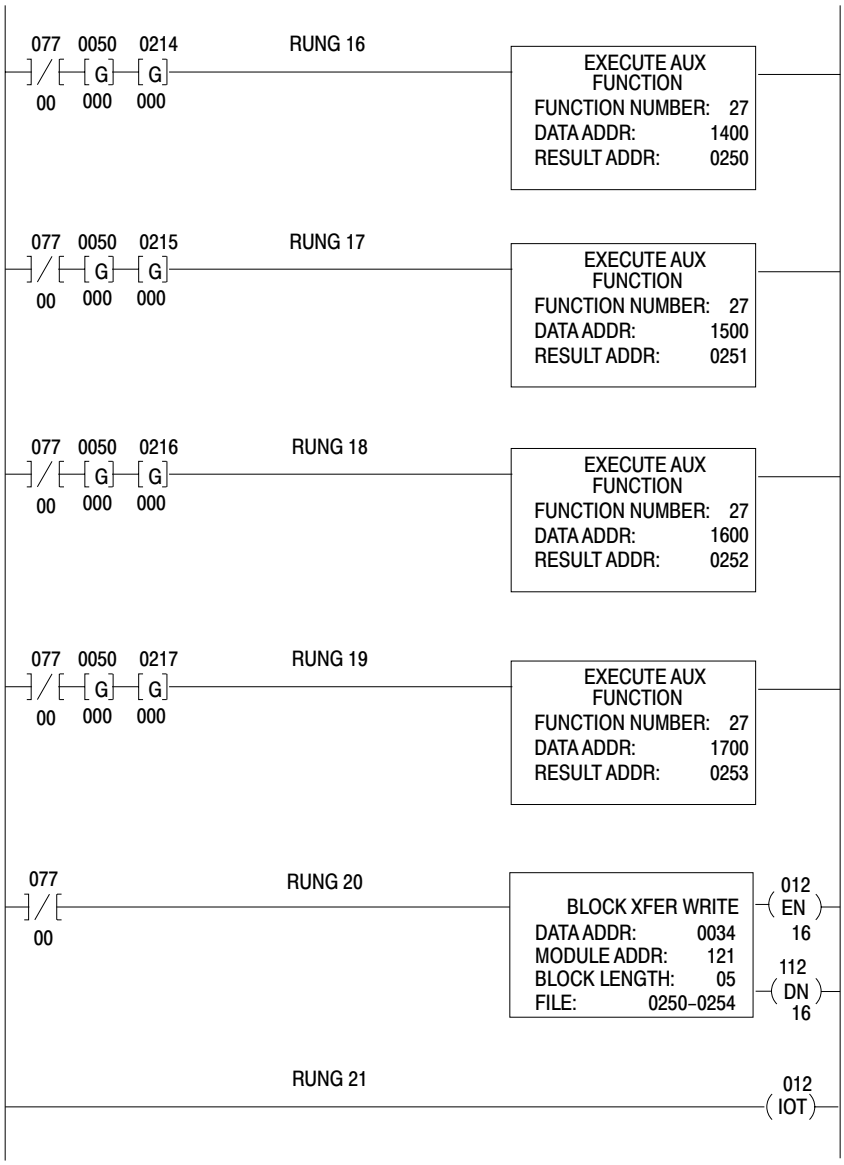
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Figure 16.4 (continued)
Selectable Timed Interrupt Example (the second 4 PID instructions)



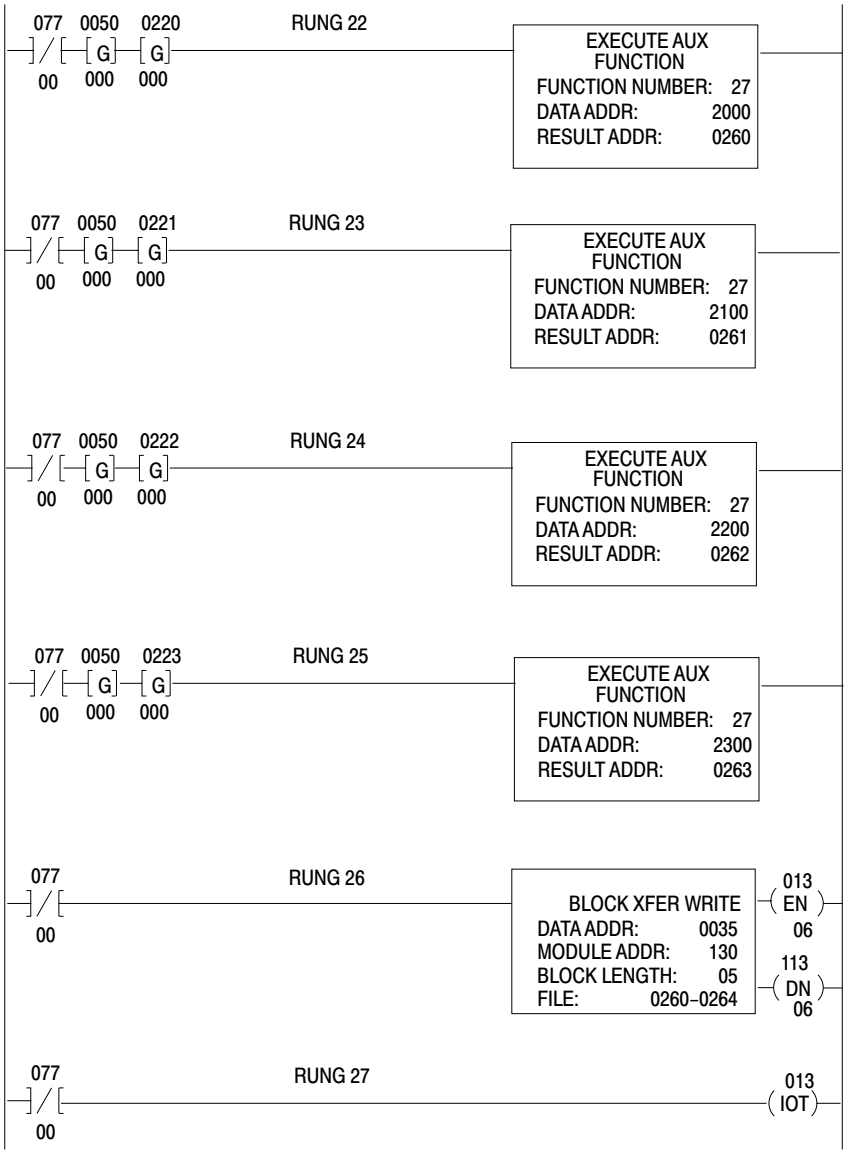
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Figure 16.4 (continued)
Selectable Timed Interrupt Example (the third 4 PID instructions)



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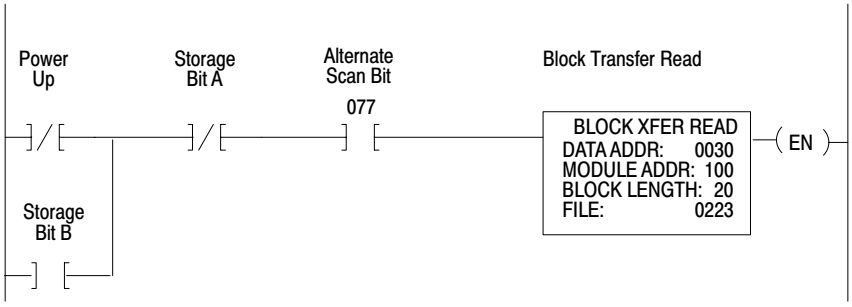
Figure 16.4 (continued)
Selectable Timed Interrupt Example (the fourth 4 PID instructions)



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If you are using an 1771-IFE, -IL, -IR or -IXE module, place all module configuration rungs except rung 2 in the main program. Place rung 2 in the subroutine. Figure 16.5 shows what the modified STI block transfer looks like. Please consult the module's user manual for specific Block Transfer programming requirements.

Figure 16.5
Initialization Rung



Rung 1 Program a Get instruction as the first instruction of the first rung to indicate that this is a selectable timed interrupt. The time base is specified by the value in the Get instruction, in this case, 50 ms.

Bit 077/00 enables the "alternate Scan" PID routines every other scan. It goes on for one scan and off for the next scan

Rung 2 The BTR instruction executes every other scan.

Rung 3 The Immediate Output Update forces completion of the BTR instruction.

Rungs 4 – 7 The first four PID instructions grouped with the first output module.

Rung 8 The BTW for the first 4 PID instructions. The PIDs and the BTW execute on the same scan.

Rung 9 IOT to force completion of the block transfer.

Rungs 10 – 15 The second four PID instructions grouped with the second output module block transfer write and the IOT instructions. The PIDs and the BTW execute on the same scan.

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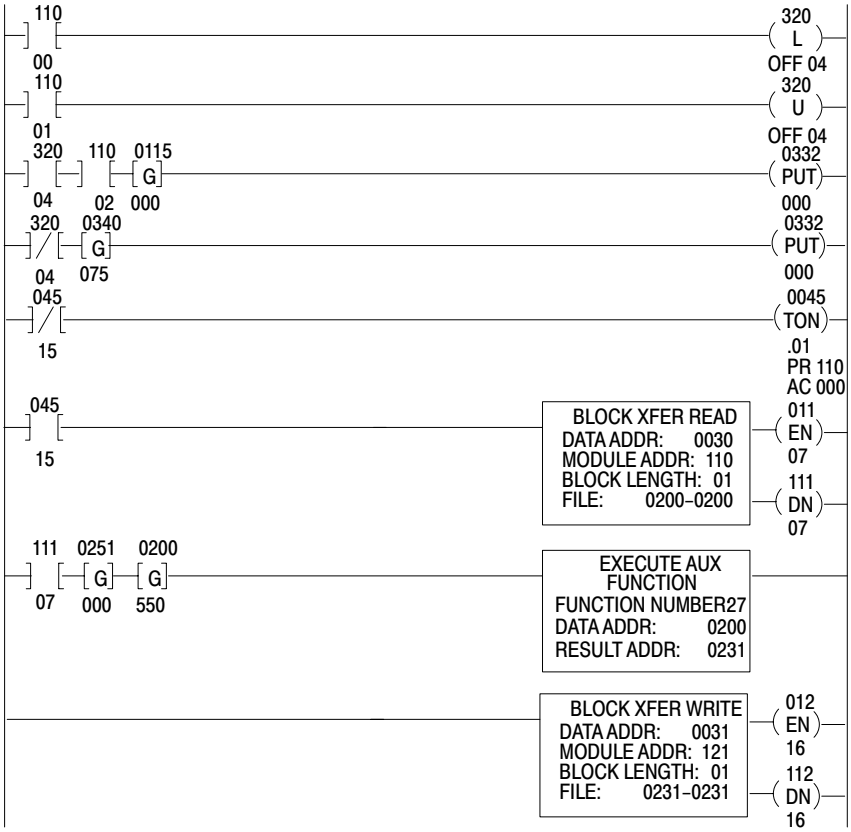
Rungs 16 – 21 An additional group of PID instructions would cause the STI to exceed its allowed limit (33 ms for a 50 ms interrupt). This is the first four of a second group of eight PID instructions. They execute on the opposite scan from the first group of eight PID instructions so that the timing limit is not exceeded.

Rungs 22 – 27 The second four PID instructions of the second group of PID instructions. They execute on the opposite scan from the first group of eight PID instructions.

Software Manual Control Station

Figure 16.6 shows how you can simulate a manual control station. Locate these rungs in the main program. This program will be used when the functionality of a hardware manual control station is desired but manual control separate from the controlling processor is not needed. It uses set output mode to write the manual override output value to the control device.

Figure 16.6
This Is a Simulated Manual Station



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This list identifies the function of the ladder diagram symbols.

110/00	Manual Push Button
110/01	Auto Push Button
110/02	Enter Push Button
320/04	Set-Output bit
332	PID Set-Output value
115/00	Manual Override Output Value
340	PID CO Value

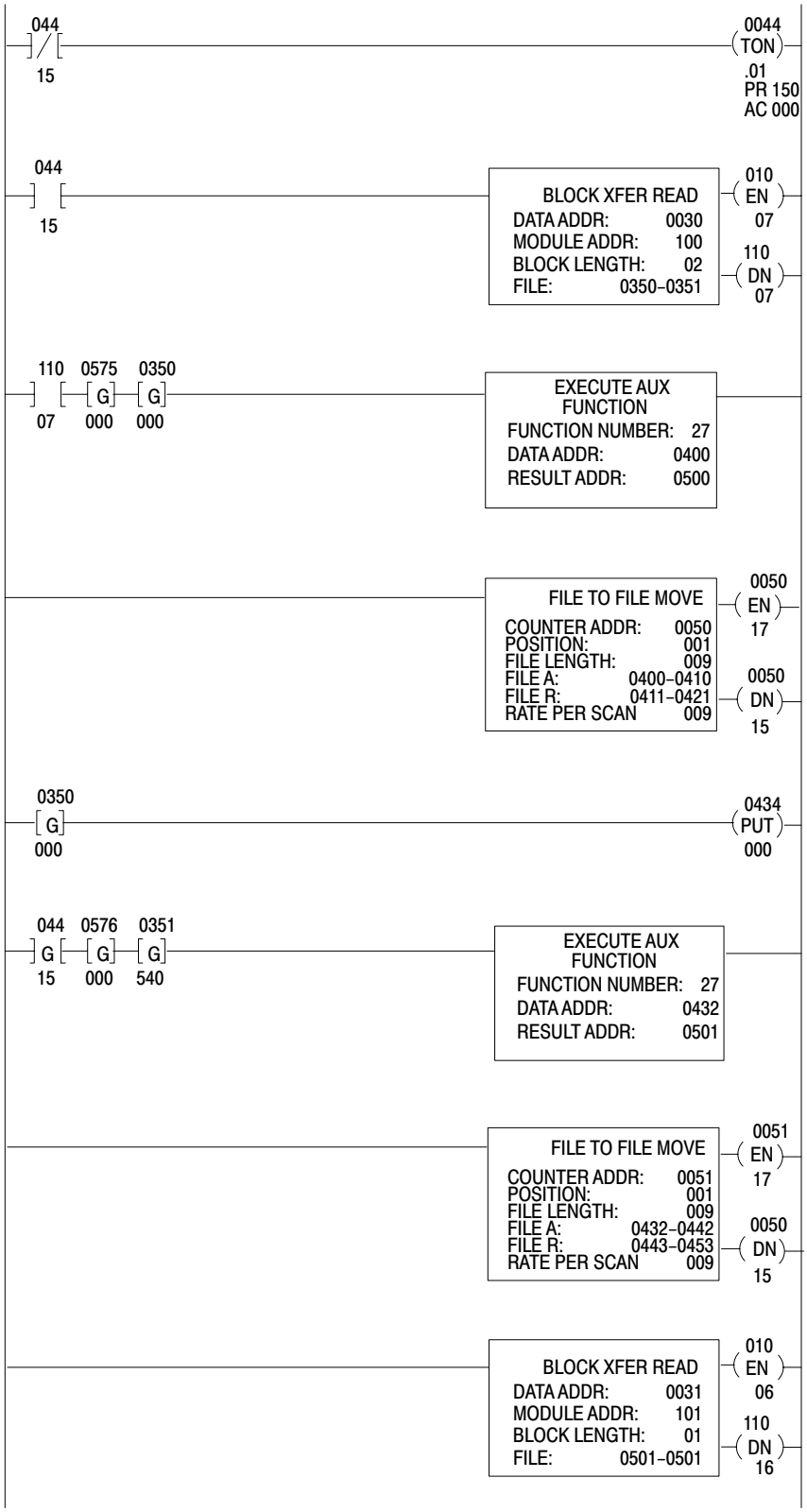
Cascading Loops

Figure 16.7 shows how you can cascade two loops by assigning the control output (CO) of one loop as the set point (SP) of the next loop. Locate these rungs in the main program. Set the cascade bit (word 01, bit 05) of the inner loop so that it will interpret the outer loops properly.

Setting the cascade bit forces the set point of the secondary loop to accept 0 to 4095 binary. This allows the output of the primary loop to be moved directly into the set point of the secondary loop.

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Figure 16.7
Cascaded Loops

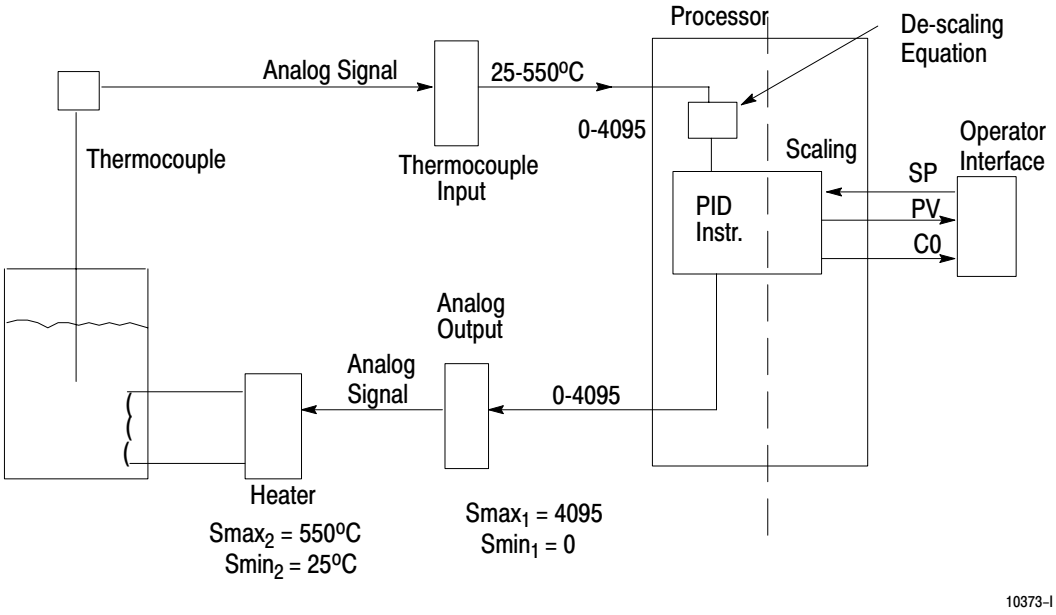


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De-Scaling Inputs

De-scaling is necessary to force the PID input range to 0 to 4095 when using an input module that does not return this range. A thermocouple input module is a good example. It returns a scaled temperature range, typically -300° to +1200° Fahrenheit. When specifying the input range for de-scaling, specify the maximum range that your process will actually see. For example, if your thermocouple input range is -300° to +1000° C but your process could only possibly experience 25° to +550° C, then use the latter range in the de-scaling equation. This improves the resolution for the PID instruction and results in better system control.

Figure 16.8
De-Scaling Inputs



Example: If measuring a full scale temperature range of 25° to 550° C, enter 25 for the minimum scaling value and 550 for the maximum scaling value.

$$M_2 = (M_1 - Smin_1)\frac{(Smax_2 - Smin_2)}{(Smax_1 - Smin_1)} + Smin_2$$

where:

M = Measured value
Smin = Minimum Scaling Value
Smax = Maximum Scaling Value

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Subscripts

1 = Units you are converting from
2 = Units you are converting to

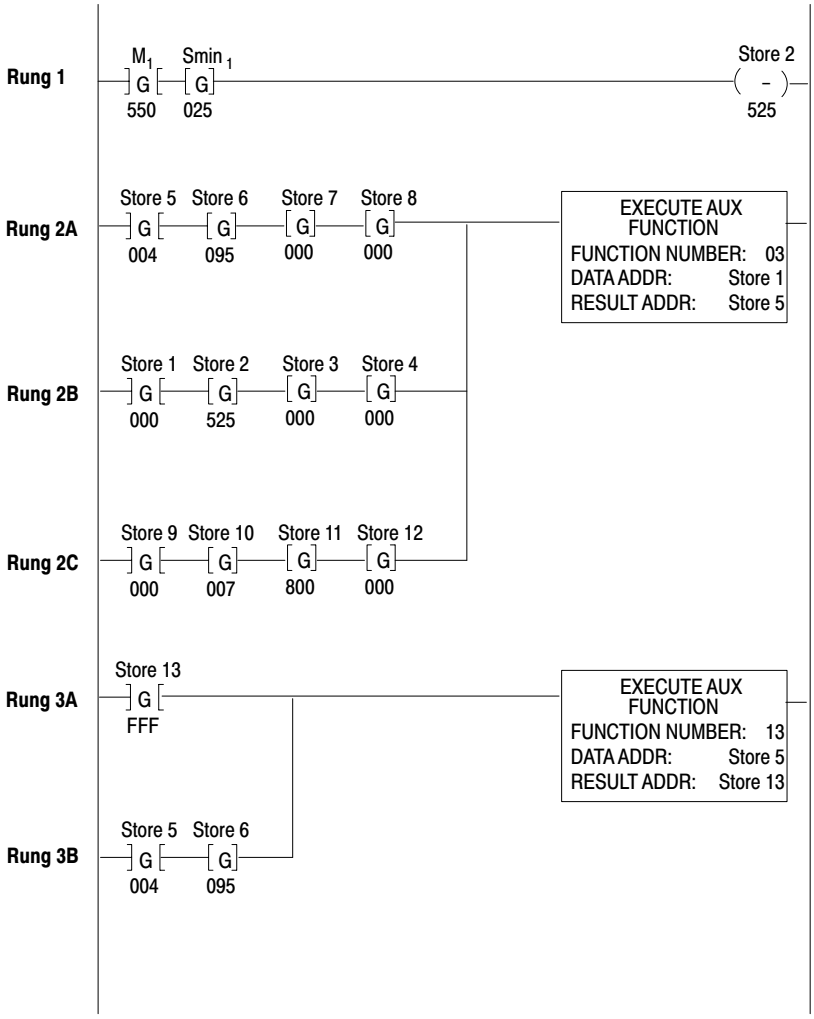
Since the converted range is always 0 to 4095, the equation simplifies to:

$$M_2 = 4095\frac{(M_1 - Smin_1)}{(Smax_1 - Smin_1)}$$

To simplify the actual programming, break the equation down into:

$$M_2 = K\,(M_1 - Smin_1),\ \text{where } K = \frac{4095}{Smax_1 - Smin_1}$$

For this example: $K = \frac{4095}{550-25}$, $K = 7.8$. So $K = 7.8$ is the constant for de-scaling this termperature range.



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The following ladder logic solution to the de-scaling equation assumes that $Smax_1$ and $Smin_1$ are between 0-999. For values less than 0 or greater than 999, additional math instructions would have to be programmed.

Rung 1 Subtraction of Smin1 from M1. In this case, the input is at maximum, 550° C.

Rung 2 This is the EAF math multiplication instruction necessary to handle the possible 4 digit BCD answer, in this case, 4095.

Rung 2A Display branch. Displays the product. The four locations must be stored consecutively starting with Store 5.

Example: Store 5 through Store 8 = 400 through 403.

Rung 2B Display of multiplier. You must allocate 4 consecutive words even though only one is used. The unused words must store zero.

Rung 2C Display of floating point multiplicand. Note implied decimal point between store 10 and 11. You must include this branch. The first two branches are for display only and can be omitted. Note that 12 words must be allocated to use this instruction.

Rung 3 BCD to Binary conversion. The 2 word value to be converted is in store 5 and 6, the answer is in store 13. Store 13 will be the PV for your PID instruction.

For systems requiring more than one de-scaled input, store this program in a subroutine and call it as many times as it is needed.

PID Glossary

Anti-Reset Windup
This is a feature that prevents the integral output term from becoming excessive when the output reaches a limit. When the sum of the PID and bias terms in the output reaches the limit, the instruction stops calculating until the error changes sign causing the output to come back in range.

Bumpless Transfer (Word 02, Bit 11)
The ability to switch from manual to auto mode without causing a sudden shift or “bump” in the Control Output. When this bit is set, the Bias Term is adjusted to provide a bumpless transfer when the Integral Gain is zero (i.e., when no integral control is used).

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Cascade (Word 01, Bit 05)
Set/reset this bit for cascading two loops. When the bit is set, the loop is the secondary (fast) loop of the cascade. When the bit is reset, the loop is the primary (slow) loop of the cascade or not part of a cascade configuration.

Control Action (Word 01, Bit 02)
Set/Reset this bit to change the control action for the PID calculation.

Direct Control	Bit Reset (0)	E = (SP – PV)
Reverse Control	Bit Set (1)	E = (PV – SP)

CO (Control Output) (EAF Result Address and Parameter File Word 17)
This is the result of the evaluation of the PID equation. It is expressed in two formats. In the EAF result address, it is a binary number (0-4095). In the parameter file (word 17), it is a percentage in BCD format (0-100). This number is converted to a signal that drives a control device such as a valve or heating element.

Control Output Tracking
It is desirable to make the CO equal to the output of the manual control station when in the manual mode. This allows a bumpless transfer between Manual and Auto modes. This is accomplished by feeding the output of the manual control station into the tieback (TB) input. The instruction sets the calculated CO equal to the TB input when in manual mode.

Dead Band (Word 10)
The adjustable deadband lets you select an error range above and below the setpoint over which no new output will be calculated as long as the Process Variable remains within this range. This lets you control how closely the process variable matches the setpoint without changing the output.

The Dead Band operates using the zero crossing principle. Zero Crossing Dead Band control allows the instruction to use the error for computational purposes as the process variable crosses into the Dead Band until it crosses the Set Point. Once it crosses the Set Point (error crosses zero and changes sign) and as long as it remains in the Dead Band, the instruction considers the error value zero for computational purposes.

Dead Band Status Bit (Bit 10 of word 01)
This bit is set/reset by the PID EAF instruction indicating whether the process variable is within or out of the Dead Band.

Reset (0)	Outside of the Dead Band
Set (1)	Within the Dead Band

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Derivative Gain Constant (Word 06)
When using the Independent Gain Equation, this is the derivative gain K_D (sec). When using the Dependent Gains equation, this is the derivative time constant T_D (min).

Derivative Uses Error (Word 01, Bit 06)
You can select whether the derivative term in either PID equation acts on changes in error or process variable. Consider selecting this feature if you want to accelerate the response to online changes to the setpoint.

Reset (0)	For normal response to set point changes, derivative acts on the change in PV
Set (1)	For a faster response to set point changes, set this bit to act on the change in Error

Done Bit (Word 01, Bit 15)
This bit is set/reset by the EAF instruction when new values have been calculated.

Reset (0)	New values not calculated
Set (1)	New values calculated

Enable Bit (Word 01, Bit 17)
This bit is set/reset by the EAF instruction to change the status of the PID rung.

Reset (0)	Rung is not enabled
Set (1)	Rung is enabled

Error (E) (Word 16)
The algebraic difference between PV and SP.

Error Sign (Word 02, Bit 07)
This bit is set/reset by the EAF instruction to indicate the polarity of the error.

Reset (0)	error is negative
Set (1)	error is positive

Equation (Word 01, Bit 00)
This bit is set/reset this bit to choose your PID equation.

Reset (0)	Independent Gain Equation
Set (1)	Dependent Gain Equation

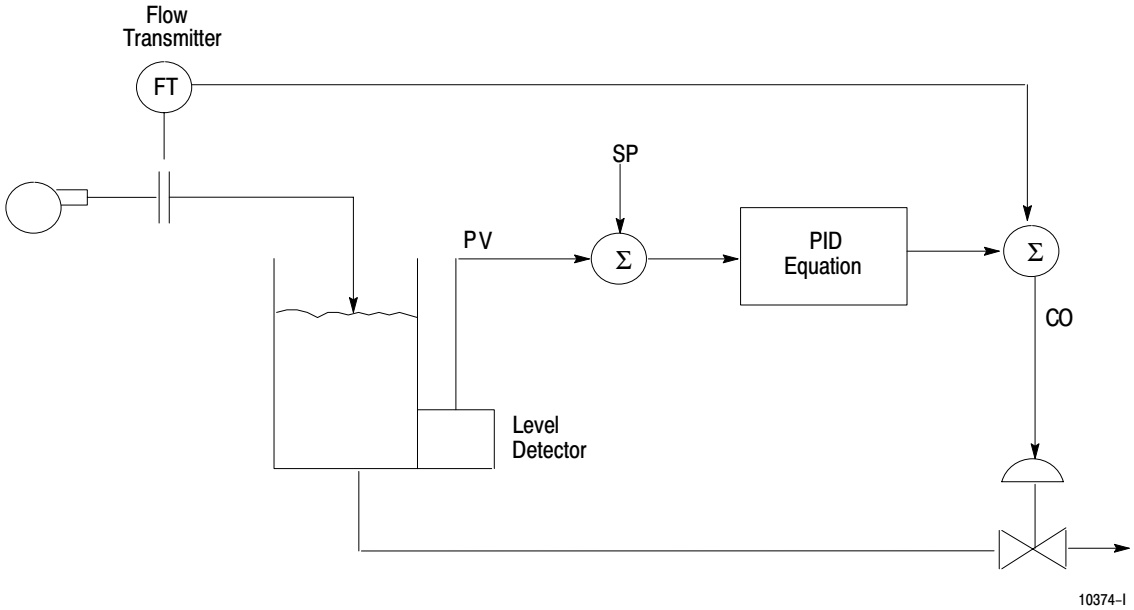
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Feedforward or Bias (Word 07)
This input is added to the calculated control output of the PID equation. It is used when a bias is needed or if feedforward control is desired. This value can be a storage constant or a calculated variable of process measurement.

Proportional only control will give a steady-state offset of the process variable from setpoint. A bias value can be added into the control output using this word to bring the process variable to the set point.

The feedforward value (Figure 16.9) represents a measured feed system disturbance fed into the PID equation. Its effect is to adjust the output before the disturbance has a chance to change the process variable, thereby reducing the impact of the disturbance on the system.

Figure 16.9
This Is an Example of Feedforward Control



Feedforward/Bias Sign Bit (Word 02, Bit 02)
Set/reset this bit to change the sign of the feedforward value.

Reset (0)	value is positive
Set (1)	value is negative

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Input Format Bit (Word 01, Bit 07)
Allows the Process Variable (PV) and Tieback (TB) to be input in Binary or BCD (series C or later).

Reset (0)	PV and TB are in Binary
Set (1)	PV and TB are in BCD

Integral Gain (Word 05)
When using the Independent Gain Equation, this value is the integral gain constant K_I (rep/sec). When using the Dependent Gains Equation, this value is equal to T_I (min/rep).

K_Ix10(Word 02, Bit 00)
When using the Independent Gains Equation. Set this bit to move the implied decimal point of K_I to the right (for example 0.10 converts to 1.00).

Reset (0)	decimal point not moved
Set (1)	decimal moved one place to the right

K_D/10 (Word 02, Bit 01)
When using the Independent Gains equation, set this bit to move the implied decimal point of K_D to the left (for example, 10.0 converts to 1.00). This improves the resolution of this term.

Reset (0)	decimal point not moved
Set (1)	decimal moved one place to the left

Manual Control Station
A manual control station is a hardware device used to control the output directly and override the PID instruction's output. The use of a manual control station is optional. Set Output mode allows the same features without this hardware device (See Set Output). When using a manual control station, feed the manually controlled output value into the PID instruction's tieback (TB) input. The PID instruction uses this value (0 to 4095) to calculate the integral term value required to achieve a bumpless transfer when switching from manual to automatic control.

Maximum Output Alarm (Word 01, Bit 11)
This bit is set by the EAF instruction whenever the computed Control Output goes above the limit set by Maximum Control Output (word 12).

Mode (Word 01, Bit 01)
Set/reset this bit to choose either Automatic or Manual mode. A hardwired auto/manual station would manipulate this bit.

Reset (0)	Automatic
Set (1)	Manual

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Maximum Control Output (Word 12)
This limits the maximum value of the Control Output. Defined as 0-100% of the 0-4095 Control Output range. This value works in conjunction with the Output Limiting feature and the Maximum Output Alarm.

Maximum Scaling Value (Word 08)
The scaling value which corresponds to the maximum setpoint and process variable in engineering units (such as PSI or oF).

Range	0000 to 9999, the decimal point is implied by the user.

Important: When Maximum Scaling Value = Minimum Scaling Value, scaling is not performed.

Maximum Scaling Sign (Word 02, Bit 03)
Set/Reset this bit to change the sign of Maximum Scaling Value (see Scaling).

Reset (0)	positive
Set (1)	negative

Minimum Control Output (Word 13)
This is the minimum allowable value of the Control Output. Enter the value as 0-100% of the 0-4095 Control Output range. This value works in conjunction with the Output Limiting feature and the Maximum Output Alarm.

Minimum Output Alarm (Word 01, Bit 12)
This bit is set whenever the calculated control output goes below the limit set by Minimum Control Output.

Minimum Scaling Value (Word 09)
The scaling value which corresponds to the minimum setpoint value and process variable (see Scaling).

Range	0000 to 9999, the decimal point is implied by the user.

Important: When Maximum Scaling Value = Minimum Scaling Value, scaling is not performed.

Minimum Scaling Sign (Word 02, Bit 04)
Set/Reset this bit to change the sign of Minimum Scaling Value.

Reset (0)	positive
Set (1)	negative

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Output Limiting (Word 01, Bit 03)
Set/Reset this bit to enable/inhibit output limiting.

Reset (0)	Output limiting inhibited
Set (1)	Output limiting enabled

Set the output limits as a percentage (0-100%) of control output. When the instruction detects that the output has reached either of these limits, the instruction sets an alarm bit in word 01 of the PID control block and prevents the output from exceeding either value.

Select maximum and minimum control output limits by setting the output limiting bit (bit 03 of word 01), and entering a maximum limit (word 12) and minimum limit (word 13). Limit values are a percentage (0-100%) of the control output (word 17). If you do not select limits, the instruction limits the range to 0-100%.

The difference between selecting output alarms and output limits is that you must set bit 03 of word 01 to enable limiting. Limit and alarm values are stored in the same words. Output alarms are always enabled. Output limiting is only enabled when word 01, bit 03 is set. Both output alarms and output limiting use the Maximum Control Output (word 12) and the Minimum Control Output (word 13) values to determine when action should be taken, such as set bits or limit the output.

Proportional Gain Constant (Word 04)
When using the Independent Gain Equation, this value is proportional gain (K_P) or controller gain (K_C) when using the Dependent Gain Equation.

PV (Process Variable) (Word 15)
This is the process measurement, scaled according to the minimum and maximum scaling values. It can be either BCD or Binary format.

Process Variable Sign Bit (Word 02, Bit 06)
This bit is set/reset by the EAF instruction to indicate the polarity of PV.

Reset (0)	PV = positive
Set (1)	PV = negative

Reserved (Word 1, Bit 14 and 16; Words 18-24)
These bits and words are used internally by the PID instruction and should **NEVER** be altered by the user.

Resume Control From Last State (Word 02, Bit 10)
This bit should be set when you want to keep the Control Output in last state (analog output module to hold the last output value). On the first program scan, the last stored value of the Control Output will then be used to back-calculate the accumulated integral value.

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Important: This bit should not be set until a valid Control Output value is calculated and stored at the Result Address (i.e., until the PID instruction has been executed at least once in Run mode).

Scaling
Input scaling lets you specify the engineering units for the set point and Dead Band values and to display the process variable and error values in the same engineering units. Select input scaling as follows:

- Enter the Maximum Scaling Value (word 02, bit 03) and Minimum Scaling Value (word 02, bit 04) in the PID control block. The Minimum Scaling Value corresponds to an analog value of zero for the lowest reading of the process variable and the Maximum Scaling Value corresponds to an analog value of 4095 for the highest reading. Set values to zero if you do not want input scaling. The unscaled range is 0-4095.

- Enter the Set Point (word 03) and Dead Band (word 10) in the same scaled engineering units. Read process variable and error in these units as well.

- The control output (word 17) is scaled to a percentage (0-100%) of the resultant range. For example, a value of 50 in this word represents a control output of 2047 (50% of 4095).

When you select scaling, the instruction scales the setpoint, Dead Band, process variable, and error. You must consider the effect on all these variables when you change scaling.



ATTENTION: Do not change scaling while the processor is in run mode. The processor could fault causing an undesirable process response resulting in possible damage to equipment and injury to personnel.

Set Output (Word 01, Bit 04)
Set/reset this bit to replace the calculated CO with the set output value word. When reset, a bumpless transfer back to standard automatic will occur if there is a number greater than zero in the integral gain. This bit functions only when the controller is in automatic (word 01, bit 01).

Reset (0)	Set Output inhibited
Set (1)	Set Output enabled

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Set Output will not override Output Limiting. The Control Output abides by the Output Limiting value. For example, if Output Limiting is enabled and the Minimum Output is 30% and the set output is set to 0% and enabled, the Control Output goes to 30%.

Set Output Value (Word 11)
When operating in the Set Output mode, this value is sent as the Control Output. The PID instruction uses the value in this word only when the Set Output bit is set. The Set Output value should be entered as 0-100% Control Output range.

Range	0000 – 0100 percent; positive integer value.

Sign Bit Word (Word 02)
This word contains the PID sign bits.

Set Point Error (Word 01, Bit 13)
This bit is set/reset by the EAF instruction when the Set Point (SP) has been set out of the Maximum or Minimum Scaling Value ranges.

Reset (0)	SP is in range
Set (1)	SP is out of range

Set Point Sign (Word 02, Bit 05)
Set/Reset this bit to change the sign of the Setpoint.

Reset (0)	SP is positive
Set (1)	SP is negative

SP (Set Point) (Word 03)
This is the desired value of the process variable. Enter it with the same engineering units as the Minimum Scaling Value and Maximum Scaling Value. Use the same implied decimal point.

Status Word (Word 01)
This word contains the PID Status Bits.

Tieback
The Manual Control Station output is brought into the PID instruction as tieback (TB). This allows a bumpless transfer from manual to automatic control.

The tieback input (output tracking) from a manual control station must also have the range of 0 to 4095. The instruction masks the upper four bits of this 16 bit value.

Also, see Control Output Tracking.

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Averaging and Standard Deviation Functions

These arithmetic functions have applications in various industries. You can use the average function for averaging thermocouple inputs or other process variables. You can use standard deviation and averaging for trend analysis and report generation.

Status Bits

Bits 14-17 of the most significant word of the result word are reserved for status bits:

This Bit:	Stores this:
14	not used
15	done bit 1 the instruction is done and the result is valid 0 the result is not valid
16	sign bit 1 negative (-) 0 positive (+)
17	enable bit 1 instruction started 0 instruction not started

Important: Bit 16 of the most significant word of each operand is reserved for the sign bit.

See chapter 14 for the word format used when a processor executes an EAF.

Difference Between Three-Digit and Six-Digit Functions

We provide two forms of these instructions (3-digit and 6-digit) for two types of users, one who will be block transferring 3-digit BCD data to his processor and one who needs up to 6 significant digits.

The 3-digit function must be enabled once for each value to be averaged. The 6-digit function is completed by enabling the function once.

Three-Digit Functions

The 3-digit averaging and standard deviation ladder diagrams are very similar with the following exceptions:

1. The averaging function number is 06 and standard deviation is 07.

2. The EAF rung (rung 4) of the averaging ladder diagram is a branched rung. The standard deviation ladder diagram is not branched.

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3. The first result word in the averaging EAF occurs in the second word after the beginning of the result word address. The first 4 words of the standard deviation result are reserved for internal processor functions.

Averaging

The averaging instruction determines the arithmetic average of a group of three digit BCD values. The maximum number of values you can average is 999 or is limited by the data table area available.

The Averaging instruction uses the formula:

$$y = \sum_{i=1}^{n} \frac{X_i}{n}$$

where

X_i = three digit signed BCD values
y = the average of the values
n = the number of values

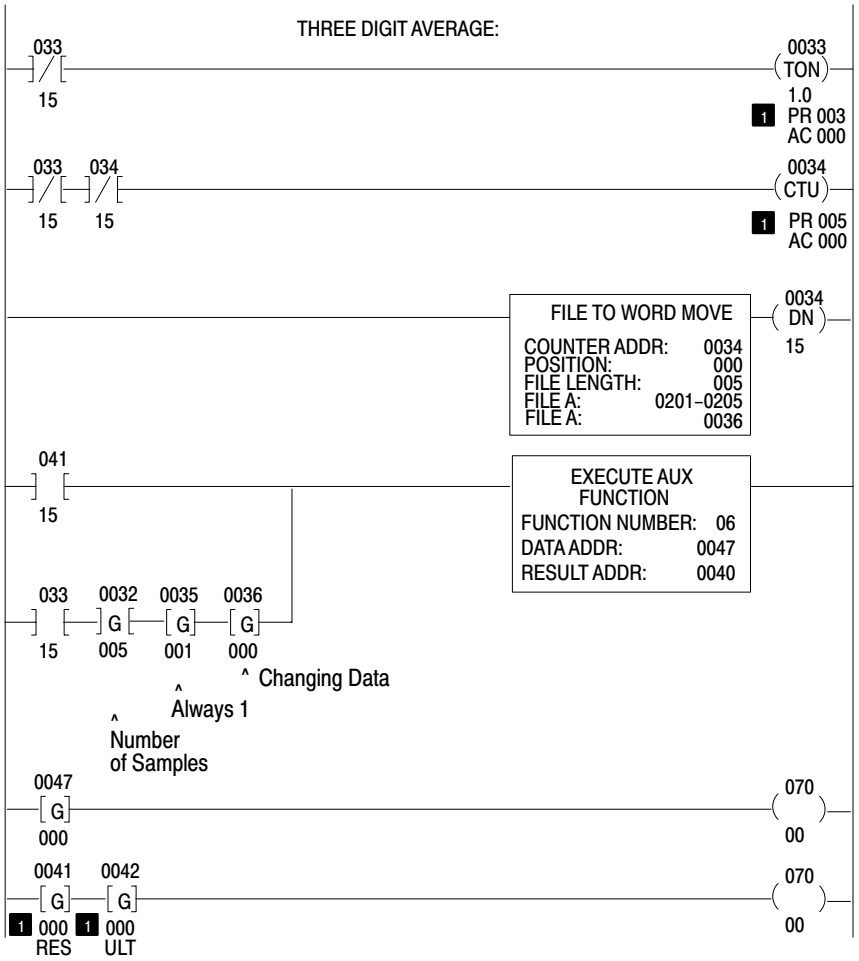
Entry and Display of Input and Result Values

Figure 16.12 shows one method you can use to enter values and display results of the 3 digit averaging. Although there are several techniques for accomplishing this, we chose Get instructions.

Be careful not to select data and result addresses so close together that they overlap.

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Figure 16.10
3-Digit Averaging Ladder Diagram



1 Indicates that these values need to be reset to zero in between calculations.

Entry and Display of Input and Result Values

Here is a description of the ladder diagram. This programming example averages five values and stops.

Rung 1 Contains a free-running timer (033) that allows a different value to be summed every 3 seconds. The pre-set of this timer can be as small as 10 milliseconds.

Rung 2 Increments counter 034 every 3 seconds to externally index the File-to-Word Move in rung 3 that moves each value into the average instruction. The preset of the counter must equal the length or number of samples to average in word 0032 in the EAF rung. The accumulated value of the counter must start at zero.

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Rung 3 This is an unconditional File-to-Word Move instruction containing the values you want to average. Addresses 201 through 205 are externally indexed by the counter 0034 and the position starting value must be zero (see rung 2).

Rung 4 This is the averaging EAF rung. The input conditions (second rung) must be programmed as shown.

Branch 1 The result word done bit 04115 (when set) stops the averaging calculation after all five values have been entered and their average calculated.

The positioning of the Get instructions cannot be altered from the example program

Branch 2 Bit 03315 is a timer done bit enabling the calculation. (Timer in rung 1)

Word 0032 is the the number of samples you want to average.

Word 0035 is the rate (or sum) per scan which **must always be 001**. The instruction will not be completed in one scan but must be executed once per value to be averaged.

Word 0036 is the result word of the File-to-Word move. It will contain a different value each time the instruction is enabled (every 3 seconds). The 3 Gets must be included in this rung. The first two can reside in any storage location; the third GET must correspond to the WORD ADDR(ess) from the File-to-Word Move in rung 3.

The DATA ADDR(ess) in the EAF average instruction (047) is used by the function to store the position of the word currently being summed. The result address (040) is the first of three consecutive words reserved for the result. The first word is used by the instruction; the second word contains the three most significant digits of the result; and the third word contains the three least significant digits of the result.

Rung 5 Word 047 points to the next value added to the calculation (present position). (Optional display rung.)

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Rung 6 This rung displays the result with a decimal point implied but not shown between the two words. Word 041 contains the 3 most significant digits and word (042) contains the 3 least significant digits. The values of these words are not valid until the done bit (04115) is ON. Word 040, the RESULT ADDR(ess) of the EAF instruction, is used for intermediate calculations and must not be manipulated by the user. (Optional display rung)

If you want to average a new set of values, you must reset to zero:

1. The accumulated value of the counter and the timer (034 and 033 in this example).

2. The data in the data address word, rung 5 (047 in this example).

3. The results in the result words (041 and 042 in this example).

Standard Deviation
The Standard Deviation instruction determines the standard deviation of a group of three digit values. The maximum number of values the instruction can handle is 999 or is limited by the data table area available. Standard deviation instruction uses the formula:

$$y = \left\{ \frac{\sum (x_i - x_{avg})^2}{n} \right\}^{1/2}$$

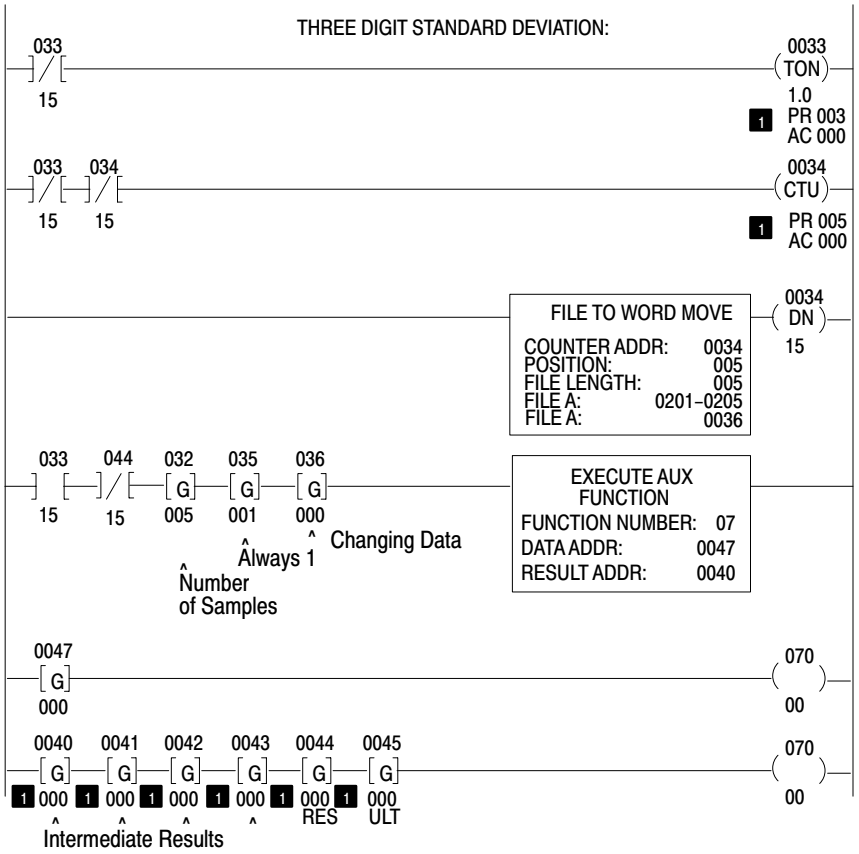
Where:

x_i = the group of values whose standard deviation you want to calculate
x_{avg} = the arithmetic average of the group of values
n = the number of values in the group

Entry and Display of Input and Result Values
Figure 16.13 shows one method you can use to enter values and display results of the 3 digit standard deviation. Although there are several techniques for accomplishing this, we chose Get instructions.

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Figure 16.11
3 Digit Standard Deviation Ladder Diagram



1 Indicates that these values need to be reset to zero in between calculations.

Here is a description of the ladder diagram. This programming example calculates the standard deviation of five values and stops.

Rung 1 Contains a free-running timer (033) that allows a different value to be summed every 3 seconds. The preset of this timer can be as small as 10 milliseconds.

Rung 2 The Timer Done Bit (03315) increments counter 034 every 3 seconds to externally index the File-to-Word Move in rung 3 that moves each value into the standard deviation instruction. The preset of the counter must equal the length or number of samples in word 032 in the EAF rung. The accumulated value of the counter must start at zero.

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Rung 3 This is an unconditional File-to-Word Move instruction containing the values for which you want to calculate the standard deviation. Addresses 201 through 205 are externally indexed by the counter 0034. The starting position must be one (see rung 2).

Rung 4 This is the EAF rung.

Bit 03315 a timer done bit enabling the calculation. (see rung 1)

Bit 04415 the result word done bit that stops the standard deviation calculation after all five values have been entered and their standard deviation calculated.

Word 0032 the calculation length or the number of samples for which you want to find the standard deviation (five in this example).

Word 0035 the rate per scan (must be 001).

Word 0036 the Output WORD ADDR(ess) of the File-to-Word Move instruction. It will contain a different value each time the instruction is enabled (every 3 seconds). The 3 Gets must be included. The first two can reside in any storage location; the third Get must correspond to the RESULT ADDR(ess) of the File-to-Word move in rung 3.

The Data Address, word 047, contains the current position for which the standard deviation is being calculated. The Result Address is the first of six consecutive words used for intermediate calculations and for storing the final result. The first 4 words (040-043) are reserved for intermediate calculations. Word 044 contains the 3 most significant digits of the result and word 045 contains the 3 least significant digits. There is an implied decimal point between the words (044 and 045).

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Rung 5 This is the Data Address of the EAF instruction. It points the next value added to the calculation (present position). This is an optional display rung.

Rung 6 This rung displays the result of the EAF instruction. Words 040 through 043 are used for internal calculations and must not be manipulated. Word 044 contains the 3 most significant digits (fifth word of the EAF result) and word 045 contains the 3 least significant digits (sixth word of the EAF result). There is an implied decimal point between these two words (044 and 045). This is an optional display rung.

If you want to calculate the standard deviation for a new set of values, you must reset to zero:

1. The accumulated value of the timer.
2. The data in the data address word, rung 5 (047 in this example).
3. The results in the result words, rung 6 (0044 and 0045 in this example).

The starting position of the File-to-Word Move must also be set to one. (The accumulated value of counter 034 in this example.)

Six-Digit Functions

Six-digit averaging and standard deviation ladder diagrams are very similar with the following exceptions:

1. The averaging function number is 06 and standard deviation is 07.
2. The first result word in 6-digit averaging occurs one word after the Result Address. The first eight words of the 6-digit standard deviation result are reserved for internal processor calculations, and thus the result occurs 9 decimal words after the Result Address.

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Averaging

The averaging instruction determines the arithmetic average of a group of six digit BCD values. The maximum number of values you can average is 999 or is limited by the data table area available. The Averaging instruction uses the formula:

$$y = \sum_{i=1}^{n} \frac{X_i}{n}$$

where:

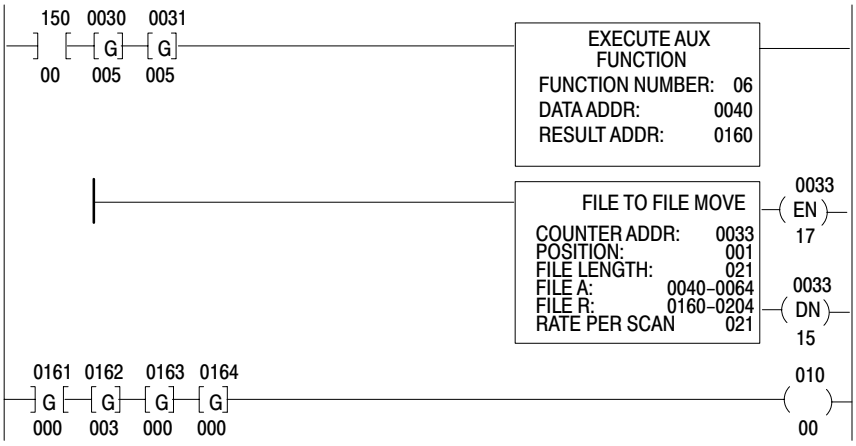
X_i = six digit signed BCD values
y = the average of the values
n = the number of values

Entry and Display of Input and Result Values

Figure 16.12 shows one method you can use to enter values and display results of the six digit averaging. Although there are several techniques for accomplishing this, we chose Get instructions.

Be careful not to select data and result addresses so that they overlap.

Figure 16.12
6-Digit Averaging Ladder Diagram



Here is a description of the ladder diagram. This programming example averages five values and stops.

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Rung 1 The EAF rung calculates an average upon a false-to-true transition of bit 15000. This bit must remain energized until the done bit (bit 16115 in this example) is energized.

Word 0030 the number of samples you want to average.

Word 0031 the number of samples to sum per scan (from 1 to the total number of samples).

The Data Address of the EAF (040) is reserved for the preset position. Each value to be averaged requires four consecutive data table words, beginning at word 041 in this example. The result address stores intermediate calculations in the first word (160) and the final result in words 161-163.

Rung 2 This rung is conditioned with a branch end to keep the File-to-File Move from becoming true. The data values to be averaged are in addresses 0041-0064. Each value uses 4 words (the format is xxx xxx . xxx xxx). The first word (0040) is reserved for present position value. (Optional display rung)

Rung 3 This rung displays the result of the EAF instruction. Word 0160 is an intermediate summation. You do not have to put this word in the rung. There is an implied decimal point between words 162 and 163. (Optional display rung)

If you want average a new set of values, you must do the following:

1. Zero the data in the data address or present position word (040 in this example).
2. Initiate a false to true transition of bit 15000.

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Standard Deviation

The Standard Deviation instruction determines the standard deviation of a group of six digit values. The maximum number of values the instruction can handle is 999 or is limited by the data table area available.

Standard deviation instruction uses the formula:

$$y = \left\{ \frac{\sum (x_i - x_{avg})^2}{n} \right\}^{1/2}$$

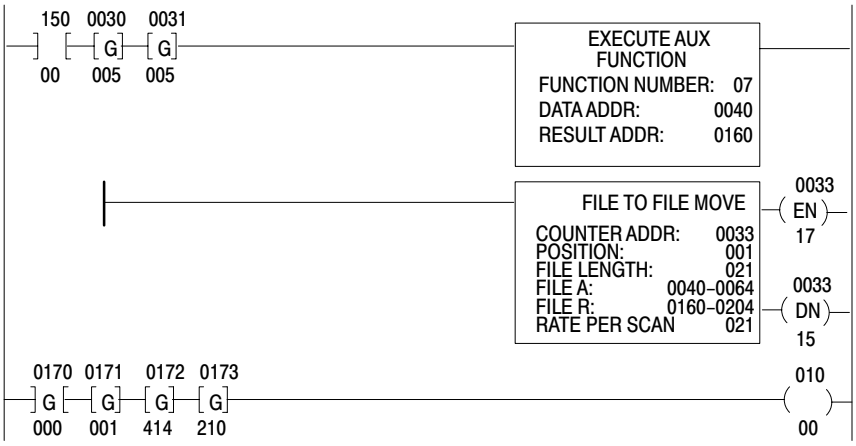
where:

x_i = the group of values whose standard deviation you want to calculate
x_{avg} = the arithmetic average of the group of values
n = the number of values in the group

Entry and Display of Input and Result Values

Figure 16.13 shows one method you can use to enter values and display results of the 6-digit standard deviation. Although there are several techniques for accomplishing this, we chose Get instructions.

Figure 16.13
6-Digit Standard Deviation Ladder Diagram



The first eight words after the result address are used for intermediate calculation. The standard deviation ladder diagram is the same as the ladder diagram for averaging with the exception already discussed. The result address stores intermediate calculations in the first 8 words (160-167) and the final result in the next 4 words (170-173, the implied decimal point is after word 171). The done bit is 17015.

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If you want to calculate the standard deviation of a new set of values, you must:

1. Reset to zero the data in the data address word (0040 in this example).
2. Reset to zero the data in the result words (0160-0173) in this example).
3. Initiate a false to true transition of bit 15000.

Wall Clock/Calendar

The EAF Wall Clock/Calendar function allows you to set time, date, leap year, and day of the week and read them for control and reporting purposes. Over the temperature range, the worst case clock accuracy will be +/– 10 minutes per month.

Entry and Display of Set and Read Values

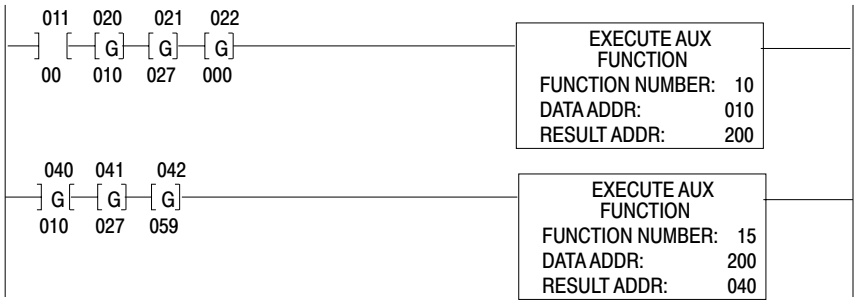
Figure 16.14 shows a method for inserting set and read values. Be careful not to select set and read addresses so close together that they overlap.

The first rung is the set rung. It contains Get instructions and an EAF block. You must use an Examine On for conditioning. Three addressed Gets contain set data. These Gets need not be consecutively addressed. However, they must be in the same rung as the EAF block and must immediately precede the EAF instruction. The data address in the EAF block must be 010 (the default value) or a run-time error results. (Word 010 is not altered by the instruction and can be used elsewhere in the program.) The result address is not used by the set instruction and can be any address.

The second rung is the read rung. It contains three consecutively addressed Get instructions and an EAF block. The data address is not used by the Read instruction and can be any address. The result address is chosen to put read data into three consecutively addressed data table words. It points to the first of the three addresses.

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Figure 16.14
EAF Set and Read Rung



Keystrokes
Enter an EAF (like Figure 16.14) by performing the following steps.

1. Enter the Examine On and Get instructions.

2. Press [Shift] [EAF].

3. Enter the appropriate function number (Table 16.A).

4. Enter the data and result addresses.

5. Enter the set values. The clock stops when you are setting any of the three functions.

Time

Time is displayed in military format. For example: 15:00 hours is 3:00pm.

0AA 0BB 0CC

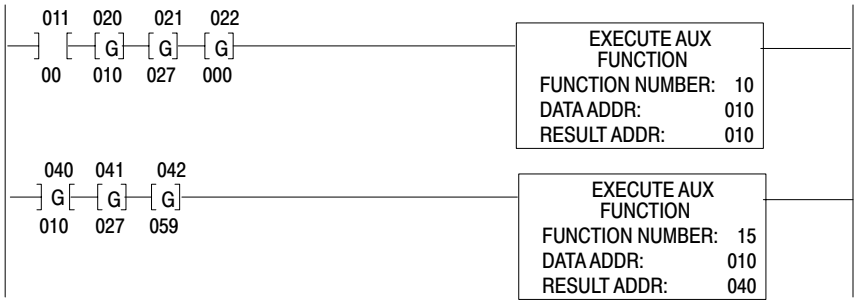
0AA = hours (00 – 23)
0BB = minutes (00 – 59)
0CC = seconds (00 – 59)

Word format for Set and Read Time functions is the same. The only difference between the two EAFs is their function number: Set Time is 10 and Read Time is 15.

Enter EAF rungs like those shown in Figure 16.15.

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Figure 16.15
Set and Read Time Input and Display Rungs



Enter the time and set the condition bit (01100) true. Then, start the clock by resetting the condition bit.

Dates

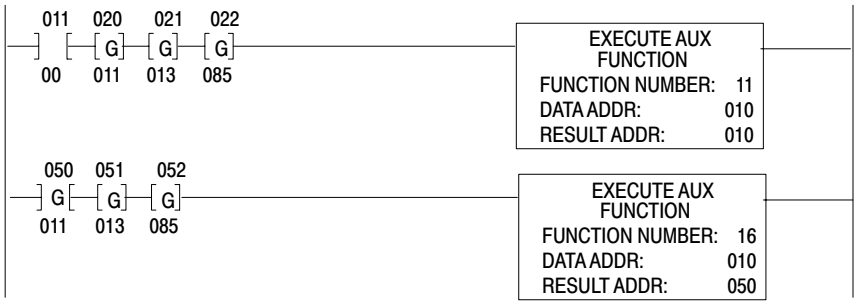
Dates are entered as numbers. For example:

- November is displayed as 011.
- The year 1994 is displayed as 094.

Word format for Set and Read Date functions are the same. The only difference between the two EAFs is their function number: Set Date is 11 and Read Date is 16.

Enter EAF rungs like those shown in Figure 16.16.

Figure 16.16
Set and Read Date Input and Display Rungs



Enter the date and set the condition bit (01100) true. Then, start the calendar by resetting the condition bit.

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Leap Year and the Day of the Week

Leap year is displayed as a number representing the number of years since the last leap year. For example:

```
–[GET]–[GET]–
00A      00B
```

In the first Get:

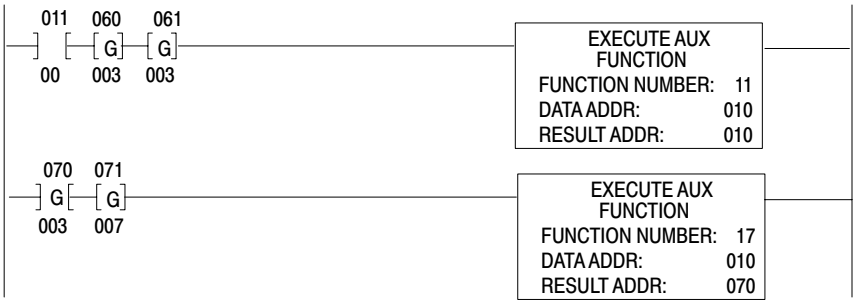
- 000 represents leap year
- 001 represents the first year since leap year
- 002 represents the second year since leap year
- 003 represents the third year since leap year

In the second Get, the day of the week is displayed as a number from 1-7. You may set this Get to any number from 1-7. It increments each day at midnight. After it increments to 7, it starts over again at 1.

Word format for set and read leap year and the day of the week functions are the same. The only difference between the two EAFs is their function number: set leap year and the day of the week is 12; read is 17.

Enter EAF rungs like those shown in Figure 16.17.

Figure 16.17
Set and Read Leap Year and the Day of the Week Input and Display Rungs



Enter the Leap Year and Day of the Week values and set the condition bit (01100) true. Then, set the leap year and day of the week by resetting the condition bit (01100).

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Chapter 17

Jump Instructions and Subroutine Programming

Chapter Objectives

This chapter describes the instructions you can use to selectively jump over portions of a program. The instructions are:

- Jump
- Jump to Subroutine
- Label
- Return

This chapter describes how jump instructions and subroutine programming direct the path of the program scan through the main program and the subroutine area.

Jump

A Jump instruction is an output instruction. It has an identification number from 00-07. When its rung is true, it instructs the processor to jump forward in the main program to the Label instruction having the same identification number. The main program executes from that point.



You can reduce scan time by selectively jumping over a portion of the program. Do not program in an area where the Jump instruction crosses the boundary between the main program and subroutine area, or vice-versa.

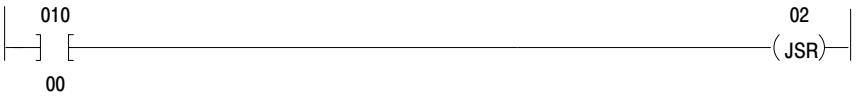
ATTENTION: Allowances should be made for conditions which could be created by the Jump instruction. Jumped program rungs are not scanned by the processor. Input conditions are not examined and outputs that are controlled by these rungs remain in their last state. Timers and counters cease to function. Critical rungs should be re-programmed outside of the jumped section in the program.

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Jump to Subroutine

The Jump to Subroutine instruction is an output instruction. It has an octal identification number from 00-07. When its rung is true, it instructs the processor to jump from the main program to the label instruction having the same number in the subroutine area. Subroutine execution begins at that point.

This instruction always causes the processor to cross the boundary from the main program to the subroutine area.



Label

The Label instruction is the target for both the Jump and Jump to Subroutine instructions. Label instructions are assigned octal identification numbers from 00-07. The label identification number must be the same as that of the Jump and/or Jump to Subroutine instruction with which it is used. A Label instruction can be defined only once, meaning that a label with a given identification number can only appear in one location. However, a Label instruction can be the target of jumps from more than one location.

The Label instruction is always logically true. Programmed as the first condition instruction in the rung. If conditions precede a Label instruction, they will be ignored by the processor during a jump operation. Do not program with a program control instruction.

Important: If conditions precede a Label instruction, they are ignored by the processor during a jump operation.





ATTENTION: Do not place a Label instruction in a ZCL or MCR zone. When jumping over a start fence, the processor executes the program from the label to the end fence as if the start fence had been true. The start fence may have been false intending that all outputs within the zone are controlled by the output override instruction (i.e. OFF for MCR or last state for ZCL instructions).

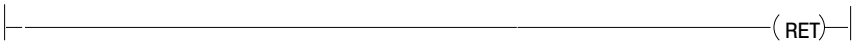
Failure to observe this warning could cause unexpected operation with possible damage to equipment and/or injury to personnel.

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Return

The Return instruction is an output instruction. It is used only in the subroutine area to terminate a subroutine or selectable timed interrupt and return the processor to the main program or, in the case of nested subroutines, return program execution to the preceding subroutine. It returns program execution to the instruction immediately following the Jump to Subroutine instruction that initiated the subroutine. Program execution continues from that point.

It is programmed as an output instruction without an identification number in the subroutine area. It is usually programmed unconditionally. Every subroutine must have a Return instruction.



Entering Jump Instructions

Enter one of the above instructions by performing the following steps.

1. Press -(JMP)-, -(SR)-, or [SHIFT] -(RET)-.

Important: Do not perform step 2 for a Return instruction.

2. Enter <octal identification number>.

Removing a Label Instruction
Remove the Label instruction by performing the following steps.

1. Position the cursor over the Label instruction you want to remove.
2. Press [Remove][Shift][LBL].

Editing Jump Instructions
Edit one of the above instructions by performing the following steps.

1. Position the cursor over the instruction you are going to edit.
2. Press [Remove]
3. Press -(JMP)-, -(JSR)-, or [SHIFT]-(RET)- or any other appropriate instruction type key.

Important: Do not perform step 3 for a Return instruction.

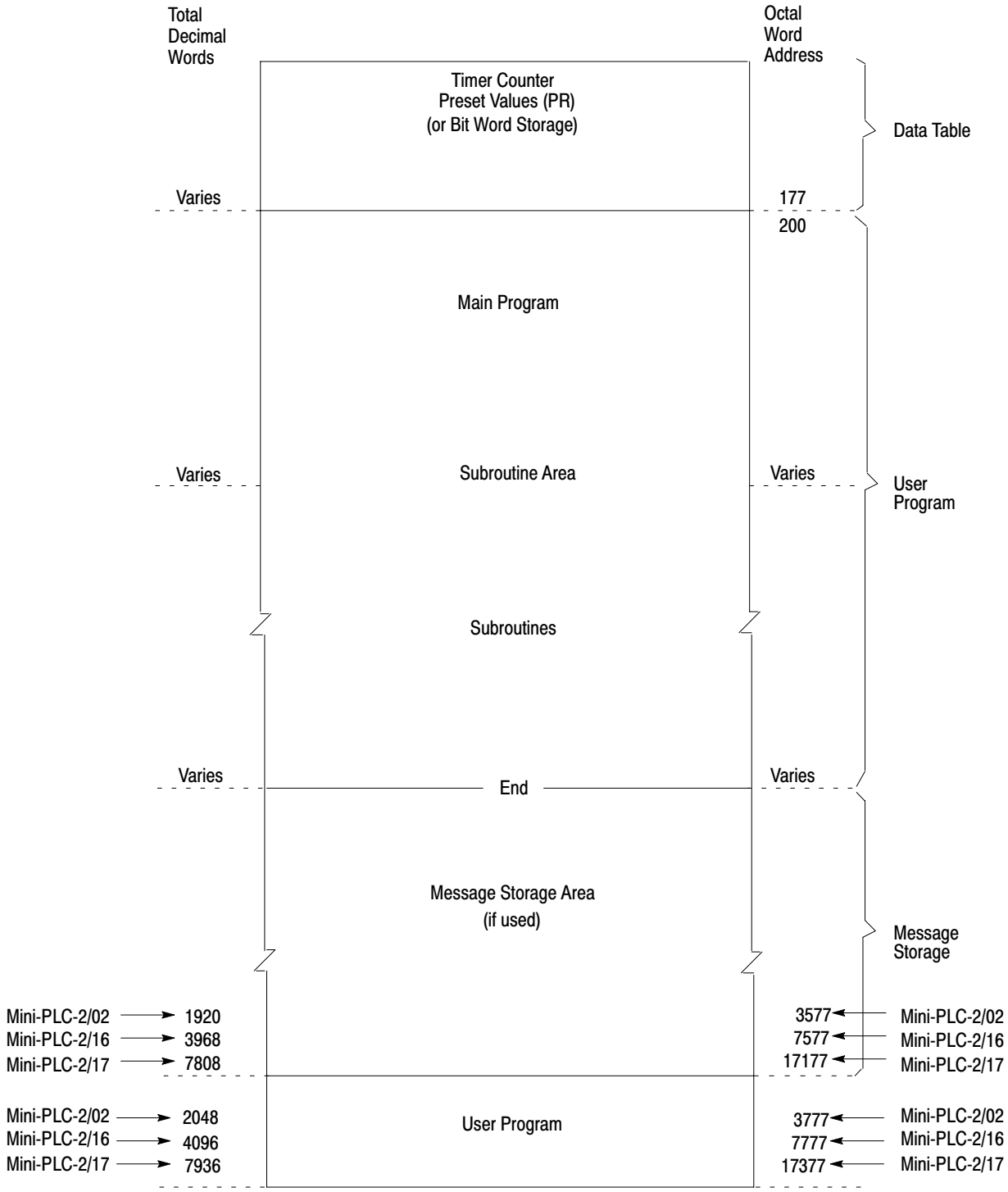
4. Enter <octal identification number>.

Subroutine Area Instruction

The subroutine area is located in the memory between the end of the main program and the beginning of the message store areas (Figure 17.1). The subroutine area allows you to store small programs you plan to access periodically. Subroutines are not scanned unless you program the processor to jump into this area.

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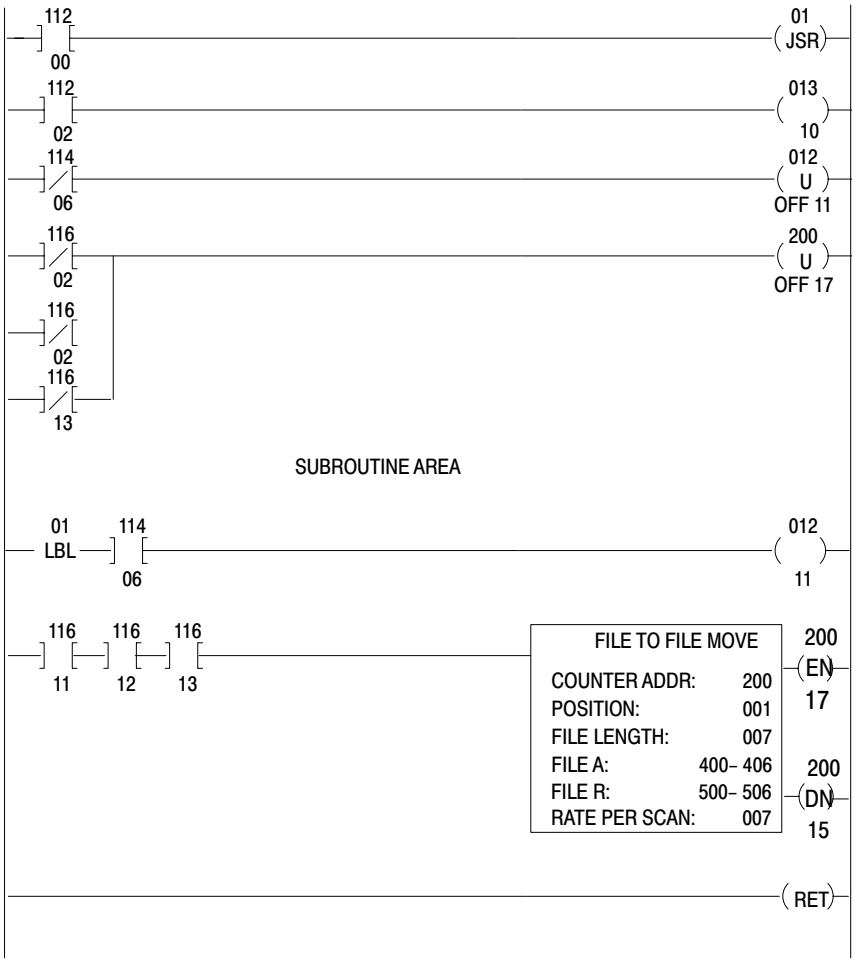
Figure 17.1
Subroutine Area



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You can program a maximum of 8 subroutines in the subroutine area. Each subroutine begins with a Label instruction and ends with a return instruction. The Return should be an unconditional rung. The subroutine area serves as the end of the main program and defines the beginning of the subroutine area (Figure 17.2).

Figure 17.2
Subroutine Programming Example



You can establish a subroutine area by performing the following steps.

1. Move the cursor down to the end of the main program.

2. Press [Shift] [SBR]

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The boundary marker subroutine area appears. A Subroutine Area instruction can only be programmed after the last instruction in the main program. The Subroutine Area instruction cannot be inserted between rungs in the main program. It requires 1 word of memory, it can be programmed only once, and it cannot be removed except by clearing the memory. You cannot nest subroutine programs by inserting a Jump To Subroutine instruction within the subroutine area, but it is possible to jump from one subroutine to another using a Jump instruction.

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Chapter 18

Block Transfer

Chapter Objectives

This chapter describes 3 types of block transfer:

- read
- write
- bi-directional

Block transfer is a combination of an instruction and support rungs used to transfer as many as 64 16-bit words of data in one scan from I/O modules to/from the data table. This transfer method is used by intelligent I/O modules such as the analog, PID, servo positioning, stepper positioning, ASCII, thermocouple, or encoder/counter modules.

Block transfer can be performed as a read, write, or bi-directional operation, depending on the I/O module you are using. An input module uses the read operation, an output module uses the write operations. During a read operation, data is read into the data table from the module. During a write operation, data is written to the output module from the data table.

Basic Operation

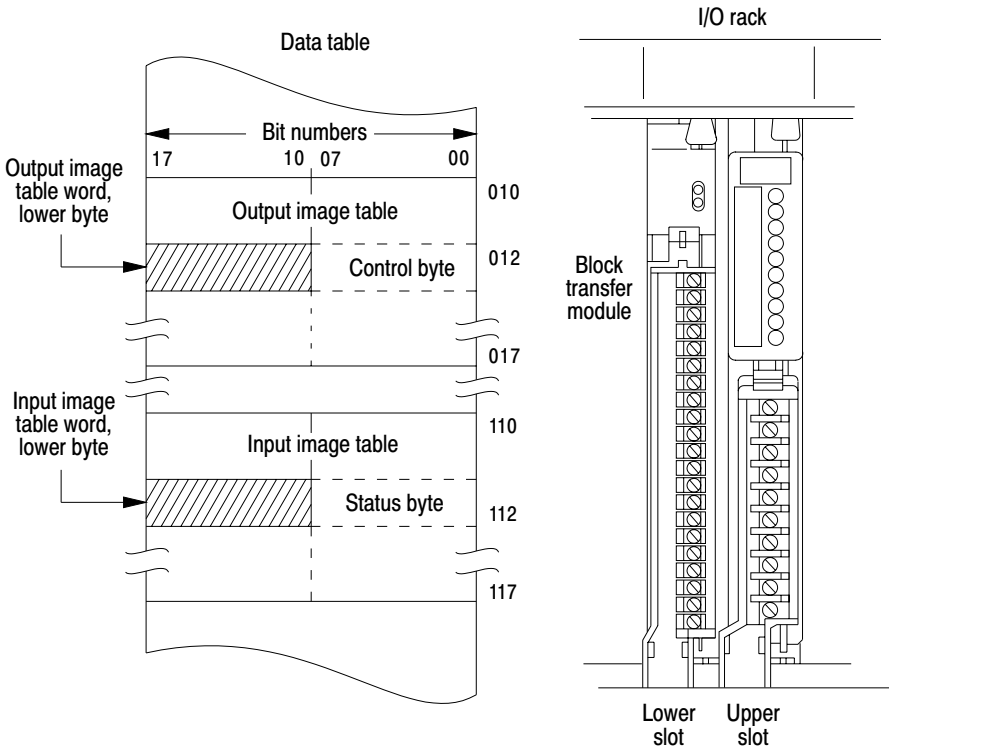
The processor uses two I/O image table bytes to communicate with block transfer modules. The byte corresponding to the module's address in the output image table (control byte) contains the read or write bit for initiating the transfer of data. The byte corresponding to the module's address in the input image table (status byte) is used to signal the completion of the transfer.

Important: Do not use word 127 for data storage. Block transfer requires the output image table byte and the corresponding input image table byte. Word **127** cannot be used since its corresponding image table byte, word **027**, contains the processor status bits.

Whether the upper or lower byte of the I/O image table word is used depends on the position of the module in the module group. When the module is in the left slot, the lower byte is used and vice versa (Figure 18.1).

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Figure 18.1
Image Table Byte Relationship versus Module Position

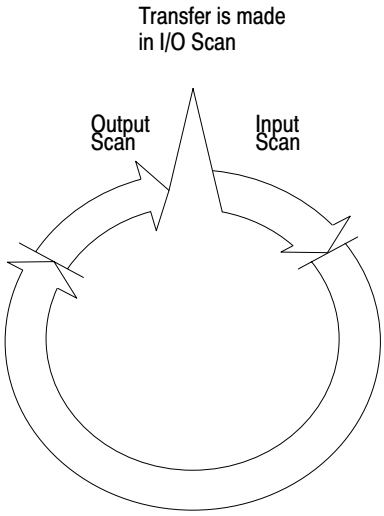


The block transfer read or write operation (Figure 18.2) is initiated in the program scan and completed in the I/O scan as follows:

- Program scan – When the rung goes true, the instruction is enabled. The number of words to be transferred and the read or write bit that controls the direction of transfer are set by a bit pattern in the control byte in the output image table.
- I/O scan – The processor requests a transfer by sending the output image table byte of data to the block transfer module during the scan of the output image table. The module signals the processor that it is ready to transfer. The processor then interrupts the I/O scan and scans the timer/counter accumulated area of the data table, looking for the address of the module that is ready to transfer.

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Figure 18.2
Block Transfer Timing Diagram



The module address is stored in the timer/counter accumulated area in the same manner as an accumulated value of a timer. The word address at which the module address is stored is called the data address of the instruction.

Once the module address is found, the processor locates the address of the file to which (or from which) the data is transferred. The file address is stored in BCD at an address 100_8 above the address containing the module address. This is done in the same manner that the processor locates the preset value of a timer/counter in a word address 100_8 above the accumulated value address. The analogy between block transfer and timer/counter data and addresses is shown in Table 18.A.

Table 18.A
Timer and Counter Block Transfer Analogy

Timer/Counter	Block Transfer
Address of Accumulated Value	Data Address of Instruction
Accumulated Value in BCD	Module Address in BCD
Address of Preset Value	100_8 Above Data Address
Preset Value of BCD	File Address in BCD

After locating the file address in the preset timer/counter area of the data table, the processor then duplicates and transfers the file data consecutively one word at a time until complete, starting at the selected file address.

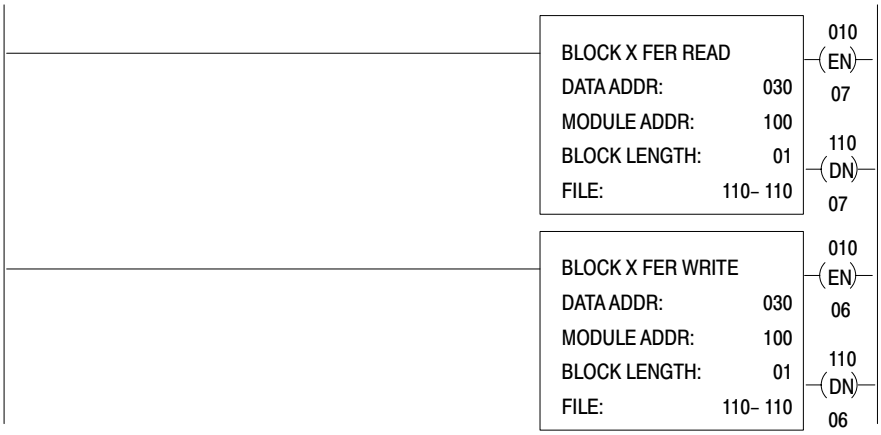
At the completion of the transfer, a done bit for the read or write operation is set in the status byte in the input image table as a signal that a valid transfer has been completed.

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Block Transfer Format

The format of a block transfer read and a block transfer write instruction with default values is shown in Figure 18.3.

Figure 18.3
Block Transfer Format



Numbers shown are default values. The number of default address digits initially displayed (3 or 4) depends on the size of the data table.

Here is an explanation of each value:

This Value:	Stores the:
Data Address	First possible address in the timer/counter accumulated value area of the data table
Module Address	RGS for R = rack, G = module, S = slot number
Block Length	Number of words to be transferred (enter 00 for default value or for 64 words)
File	Address of the first word of the file
Enable bit -(EN)-	Automatically entered from the module address Set on when the rung containing the instruction is true
Done bit -(DN)-	Automatically entered from the module address Remains on for 1 program scan following successful transfer

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Data Address

The data address stores the module address of the block transfer module. The data address must be assigned the first available address in the timer/counter accumulated area of the data table. This depends on the number of I/O racks being used (Table 18.B). When more than 1 block transfer module is used, consecutive data addresses must be assigned ahead of addresses for timer and counter instructions.

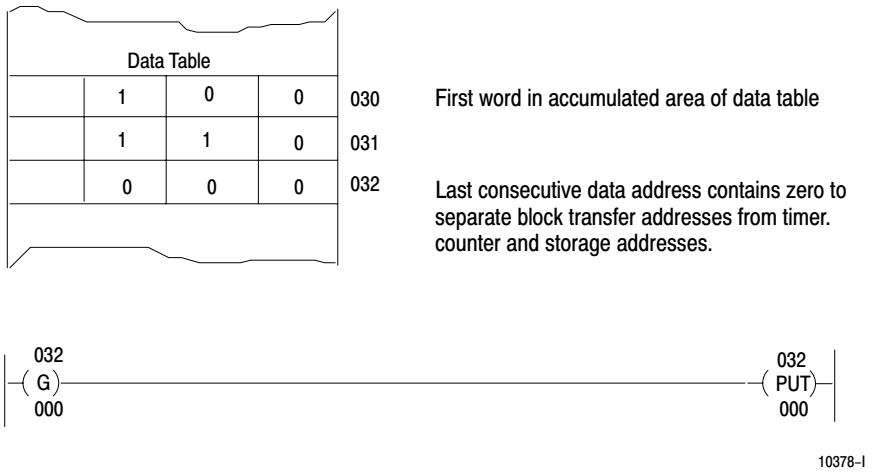
Table 18.B
Block Transfer Addressing

2-slot	030
1-slot	030
1/2-slot	050

Block transfer data addresses should be consecutive numbers (for example 030, 031, 032, etc.). A 1-word space or boundary should be left after the last block transfer data address. When the processor sees this boundary word, it will not search further for block transfer data. In addition, the processor is prevented from finding other BCD values that could, by chance, be in the same configuration as the rack, group and slot numbers found in block transfer data addresses.

The boundary word data bits can be set to zero manually with bit manipulation. Use [Search] [5][3] and insert zeros. Program a Get/Put transfer assigning Get and Put instructions to the address immediately following the last block transfer data address (Figure 18.4). The value of the Get instruction is set to 000 when programmed.

Figure 18.4
Defining the Data Address Area



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Module Address

The module address is stored in BCD with the first digit representing the rack number, the second digit the I/O group number and the third digit the slot number. When block transfer is performed, the processor searches the timer/counter accumulated area of the data table for a match of the module address. When a match is found, the processor looks 100_8 above that value to find the address of the block transfer data file.

Block Length

The block length is the number of words that the module will transfer. It depends on the type of module and the number of channels connected to it. The number of words requested by the instruction must be a valid number for the module: i.e. from 1 up to the maximum of 64. The maximum number depends on the type of module that is performing block transfer. The block length can also be set at the default value of the module (useful when programming bi-directional block transfers). For some modules, the default value allows the module to decide the number of words to be transferred. See the documentation for the module.

The block length heading of the instruction accepts any value from 00-63, whether or not valid for a particular module. Enter 00 for the default block length of 64.

The block length is stored in binary in the byte corresponding to the module's address in the output image table.

Equal Block Lengths
When the block lengths are set equal or when the default block length is specified by the programmer, the following considerations are applicable:

- Read and write instructions could and should be enabled in the same scan (separate but equal input conditions).
- Read and write instructions should be enabled in the same scan.
- Module decides which operation will be performed first when both instructions are enabled in the same scan.
- Alternate operation will be performed in a subsequent scan.
- Transferred data should not be operated upon until the done bit is set.

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Unequal Block Lengths
Consult the documentation for the block transfer module for programming guidelines when setting the block lengths to unequal values.



ATTENTION: When the block lengths of bi-directional block transfer instructions are set to unequal values, the rung containing the alternate instruction must not be enabled until the done bit of the first transfer is set. If they are enabled in the same scan, the number of words transferred may not be the number intended, invalid data could be operated upon in subsequent scans, or analog output devices could be controlled by invalid data. Unexpected and/or hazardous machine operation could occur. Damage to equipment and/or personal injury could result.

File Address

The file address is the first word of the file to which (or from which) the transfer is made. The file address is stored 100_8 words above the data address of the instruction. When the file address is entered into the instruction block, the industrial terminal computes and displays the ending address based on the block length.

When reserving an area for a block transfer file, an appropriate address must be selected to ensure that block transfer data does not write over assigned timer/counter accumulated and preset values. The file address cannot exceed address 3577 for a Mini-PLC-2/02, 7577 for a Mini-PLC-2/16, or 17177 for a Mini-PLC-2/17.

Enable/Done Bit

The read and write bits are the enable bits for block transfer modules. Either one (or both for a bi-directional transfer) is set on in the program scan when the rung containing the block transfer instruction is true.

The done bit is set on in the I/O scan that the words are transferred, provided that the transfer was initiated and successfully completed. The done bit remains on for only one scan.

A block transfer is requested in each program scan that the read and/or write bit remains on. The read and/or write bits are turned off when the rung containing the instruction goes false.

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Run-Time Errors

Misuse and/or inadvertent changes of instruction data can cause run-time errors when:

- The module address is given a non-existent I/O rack number.
- A read transfer overruns the file into a processor work area or into user program by an inadvertent change of the block length code.

Block Transfer Read

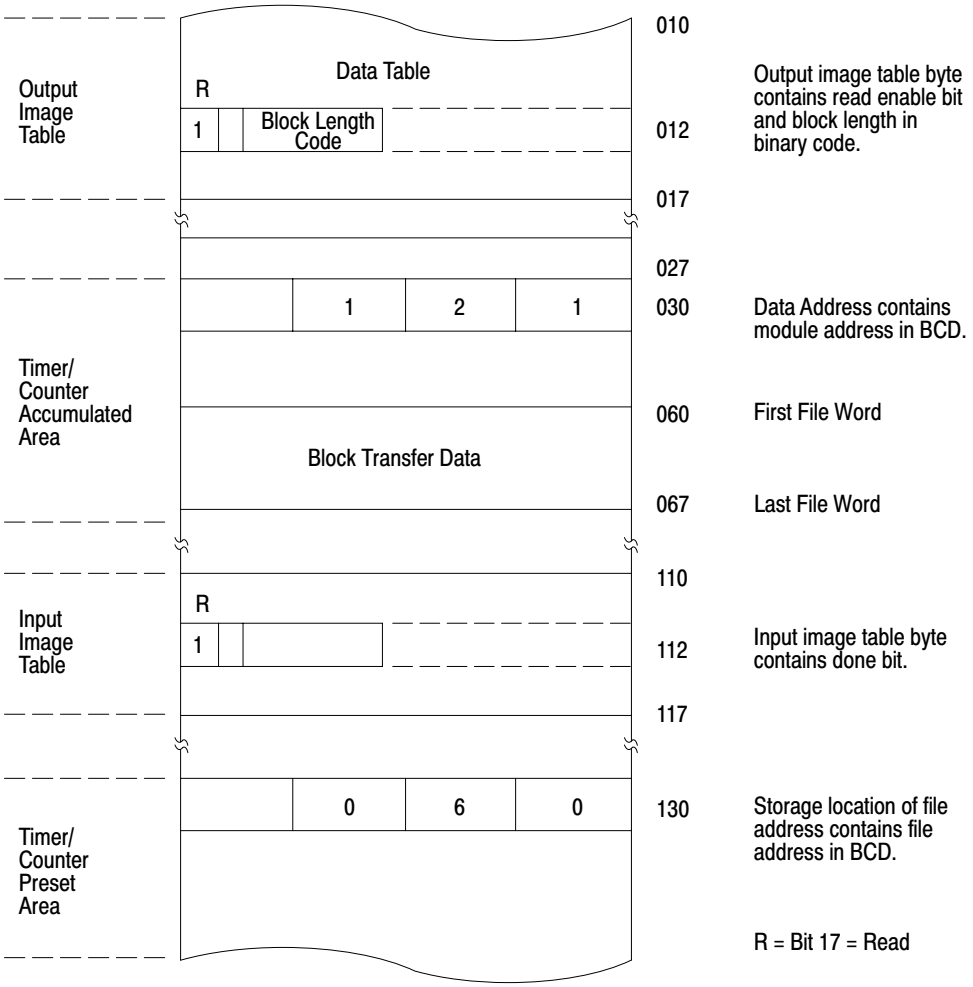
Block transfer reads data from an I/O module into the processor's input image table in one I/O scan.

- Programmed as an output instruction.
- Block length depends on the type of module you are using.
- Request for transfer is made in the program scan.
- I/O scan is interrupted for the transfer.
- Done bit remains on for one scan after a valid transfer.
- Instruction requires two words of the data table.

Figure 18.5 shows an example rung containing a block transfer read instruction and the data table areas used by the instruction.

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Figure 18.5
Data Table Locations for Block Transfer Read



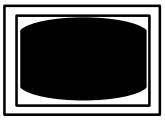
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Keystrokes

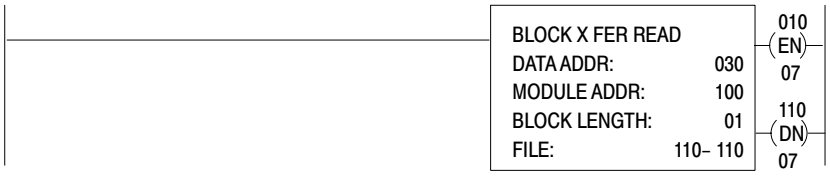
Enter a block transfer read (like this example) by performing the following steps.



BLOCK XFER 1



Block Transfer 0 appears in the lower left corner of the screen, above the processor's current programming mode.



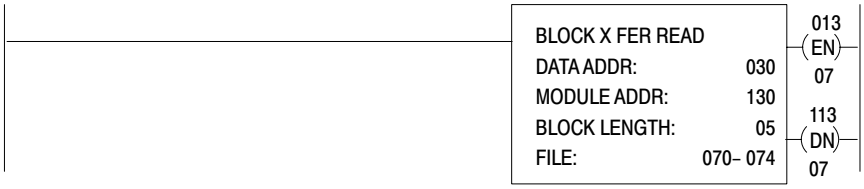
Note that the words BLOCK TRANSFER READ are flashing.

Insert the following values. The cursor moves automatically through the block transfer read instruction. The values are:

DATA ADDRESS	030
MODULE ADDRESS	130
BLOCK LENGTH	05
FILE	070-074

where the Data Address is the first possible timer/counter address; the Module Address is the rack, group, and slot number; the Block Length is the number of words to be transferred; and File is the address of the starting word to be transferred.

The instruction should look like this:



The Block Transfer enable bit is 01307; the done bit is 11307.

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Block Transfer Write

A block transfer writes data from the processor's output image table to an I/O module in one scan.

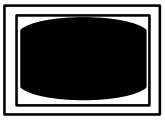
- Programmed as an output instruction.
- Block length depends on the type of module you are using.
- Request for transfer is made in the program scan.
- I/O scan is interrupted for the transfer.
- Done bit remains on for one scan after a valid transfer.
- Request requires two words of the data table.

Keystrokes

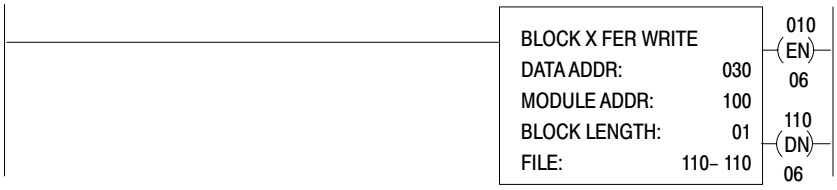
Enter a block transfer write (like this example) by performing the following steps.



BLOCK XFER 0



Block Transfer 0 appears in the lower left corner of the screen, above the processor's current programming mode.



Note that the words BLOCK TRANSFER WRITE are flashing.

Insert the following values. The cursor moves automatically through the block transfer write instruction. The values are:

DATA ADDRESS	031
MODULE ADDRESS	130
BLOCK LENGTH	05
FILE	060-064

The instruction should look like this:



The Block Transfer enable bit is 01006; the done bit is 11006.

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You can enter data directly into the block to be transferred. Position the cursor over the block transfer instruction and press [Display] [1]. See chapter 9.

Bi-Directional Block Transfer

Bi-directional block transfer is the sequential performance of both operations. The order of operation is generally determined by the module.

Two data addresses must be used. In this example they are 030 and 031. Both contain the module address. For bi-directional operation, each data address word also contains an enable bit:

- bit 16 for a Write operation (in 031)
- bit 17 for a Read operation (in 030)

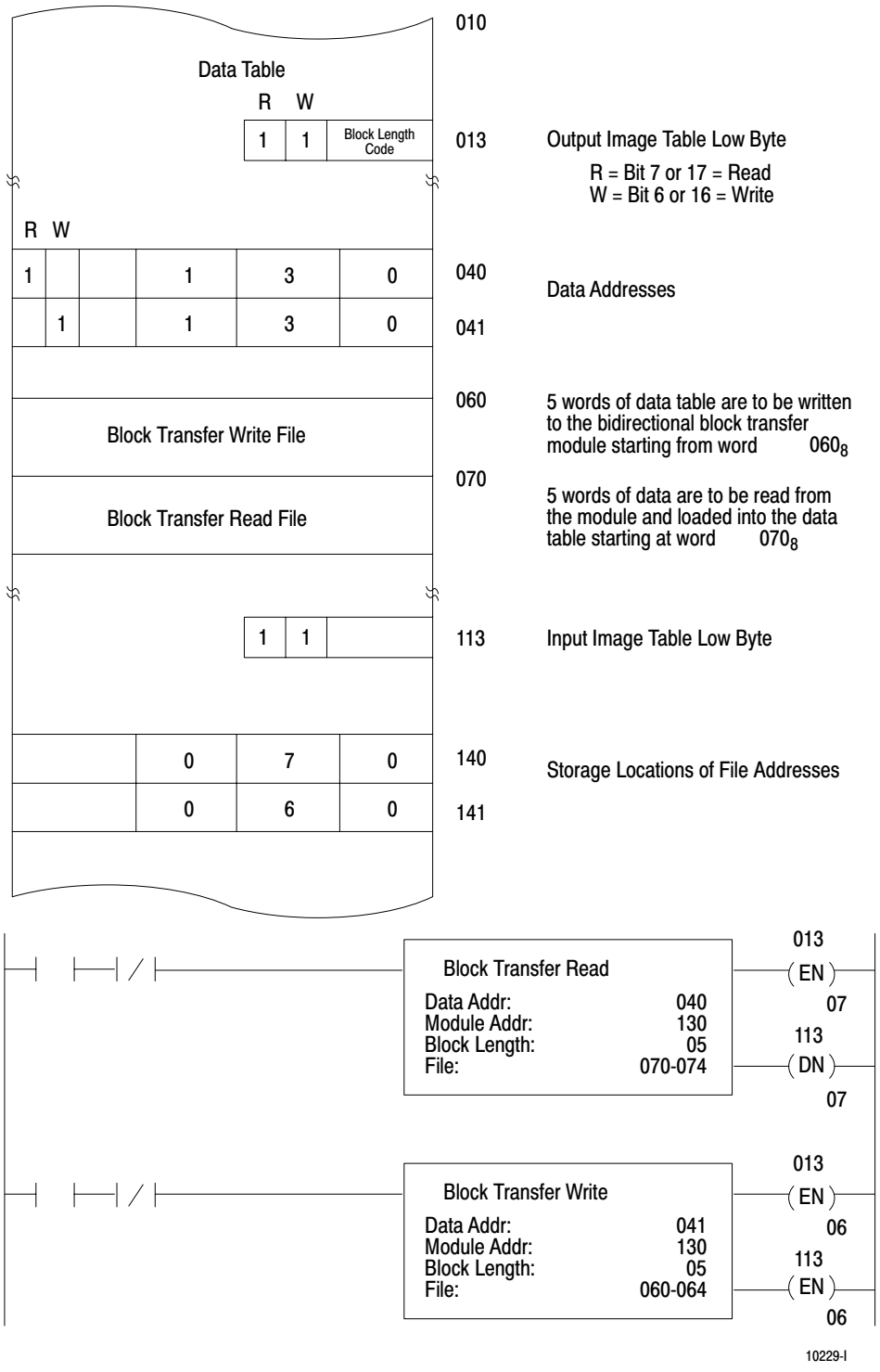
Important: These bits are automatically set by the Block Transfer Read and Write instructions.

When the processor searches the data addresses in the timer/counter accumulated area of the data table, it finds two consecutive data addresses both containing the same module address. The read bit and the write bit are set in two consecutive data addresses. When the processor finds a match of the module address and the read or write enable bit (read bit or write bit) for the desired direction of transfer, it then locates the file addresses to which (or from which) the data will be transferred.

Figure 18.6 shows an example bi-directional block transfer.

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Figure 18.6
Data Table Locations for Bi-Directional Transfer



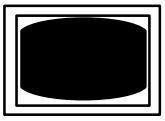
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Keystrokes

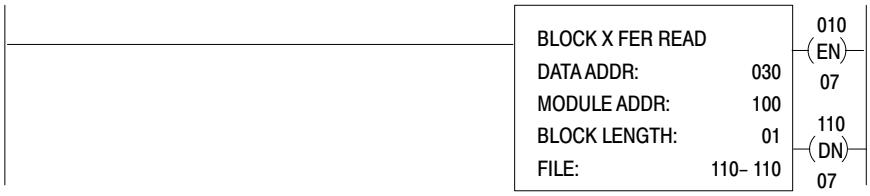
Enter a bi-directional block transfer (like this example) by performing the following steps.



BLOCK XFER 1



Block Transfer 0 appears in the lower left corner of the screen, above the processor's current programming mode.



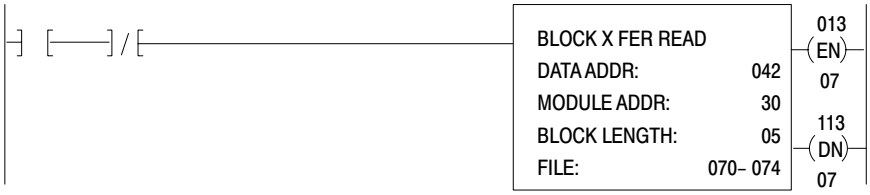
The Block Transfer enable bit is 01007; the done bit is 11007.

Note that the words BLOCK TRANSFER READ are flashing.

Insert the following values. The cursor will block automatically step through the block transfer write instruction. The values are:

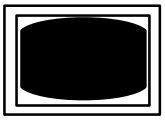
DATA ADDRESS	030
MODULE ADDRESS	142
BLOCK LENGTH	05
FILE	060-064

The write instruction should look like this:



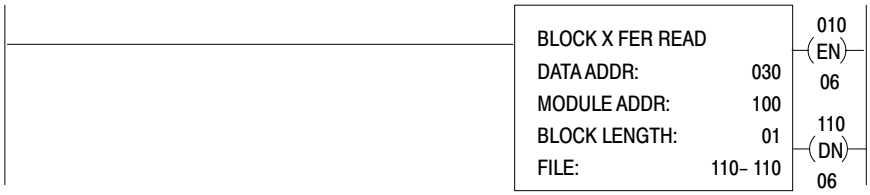
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BLOCK
XFER
0

Block Transfer 0 appears in the lower left corner of the screen, above the processor's current programming mode.

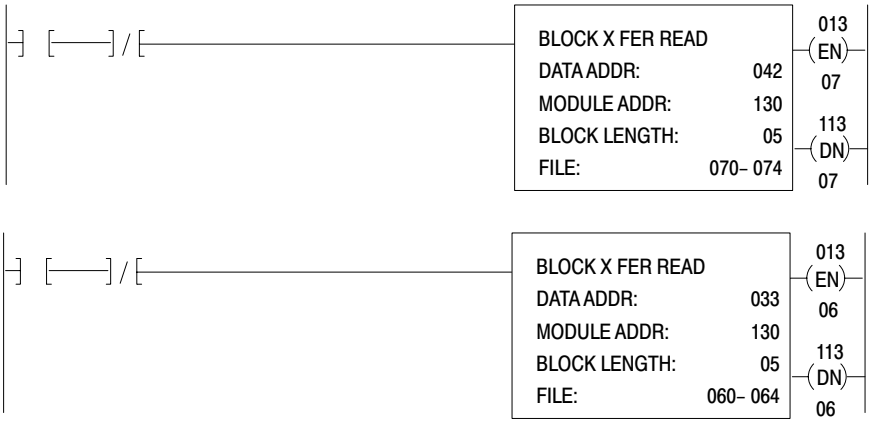


Note that the words BLOCK TRANSFER WRITE are flashing.

Insert the following values. The cursor will move automatically through the block transfer read instruction. The values are:

DATA ADDRESS	031
MODULE ADDRESS	142
BLOCK LENGTH	05
FILE	070-074

The read instruction should look like this:



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Multiple Reads of Different Block Lengths

Under certain conditions, you might want to transfer part of a file rather than the entire file. For example, a processor could be programmed to read the first two or three channels of an analog input module periodically but read all channels less frequently. To do this, use 2 or more Block Transfer Read instructions: one for each desired transfer length. The read instructions would have the same module address, data address, and file address but different block lengths. The size of the file would equal the largest transfer.

When two or more block transfer instructions have a common module address, program carefully to compensate for the following possible situations:

First - During any program scan, data in the output image table byte can be changed by each successive block transfer instruction having a common module address. The enable bit can be turned on or off according to the true or false condition of the rungs containing these instructions. The on or off status of the last rung governs whether the transfer occurs.

Second - The block length can be changed according to the block lengths of the enabled instructions. The block length of the last enabled block transfer instruction having a common module address governs the number of words transferred.



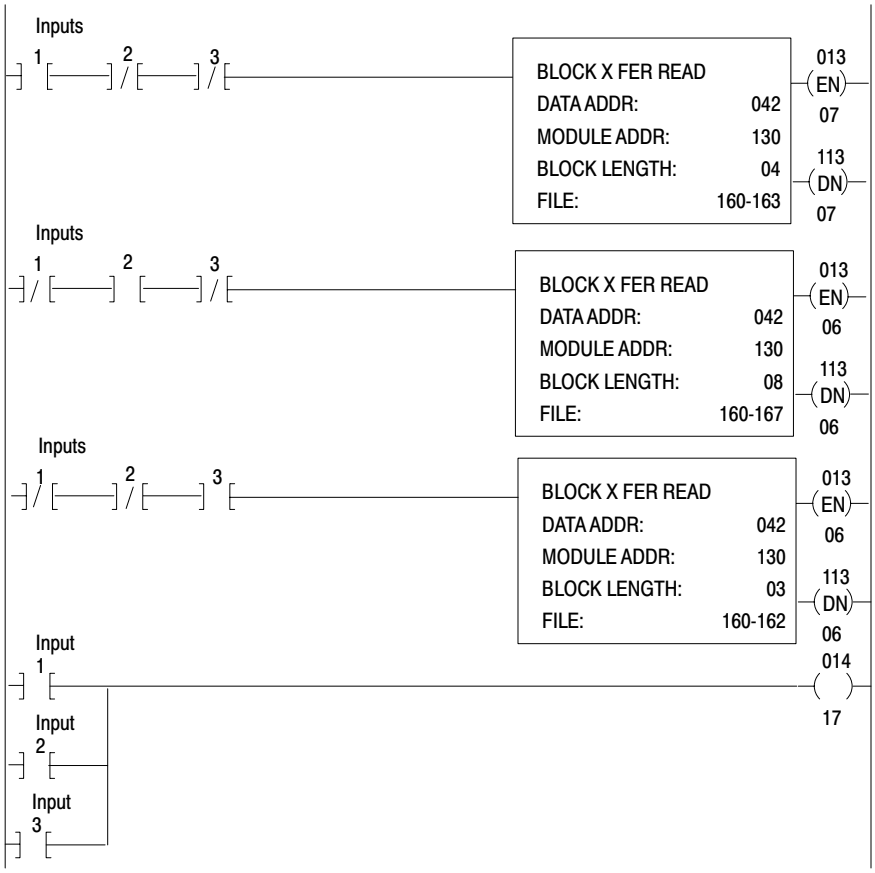
ATTENTION: When programming multiple writes (or reads) to the same module, it is possible that a desired transfer will not take place or the number of words transferred will not be the number programmed. Invalid data could be sent to a device (or could be operated upon in subsequent scans) resulting in unpredictable and/or hazardous machine operation.

The example in Figure 18.7 shows how multiple reads of different block lengths from one module can be programmed. When any one of the input switches is closed, the rung is enabled and the block length of the Block Transfer instruction is the same as the block length in that rung. The last rung sets (or energizes) the read bit of the block transfer instruction regardless of the previous changes in the status of the enable bit. The Examine Off instructions prevent more than one of the block transfer instructions from being energized in the same scan.

Important: The same discussion applies when programming multiple writes of different block lengths to one module.

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Figure 18.7
Programming Multiple Reads from One Module



Buffering Data

Buffer block transfer data so you can validate it before you use it. Data that is read from the block transfer module and transferred to data table locations must be buffered. Data that is written to the module need not be buffered because block transfer modules perform this function internally.

Buffer transferred data to ensure that both the transfer and the data are valid. As an example, readings from an open-circuited temperature sensor (invalid data) could have a valid transfer from an analog input module to the data table. Program the processor to examine data-valid and/or diagnostic bits contained in the transferred data to determine whether or not the data is valid. The block transfer done bit is set if the transfer is valid.

The data-valid and/or diagnostic bits differ for each block transfer module. Some modules set one or both for the entire file of words transferred, while others set a data-valid diagnostic bit in each word. See the documentation for the block transfer module to determine the correct usage of the data valid and/or diagnostic bit(s).

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One technique of buffering data is to store the transferred data in a temporary buffer file. If the data in the buffer is valid, it is immediately transferred to another file in the data table where it can be used. If invalid, it is not transferred but written over in the next transfer.

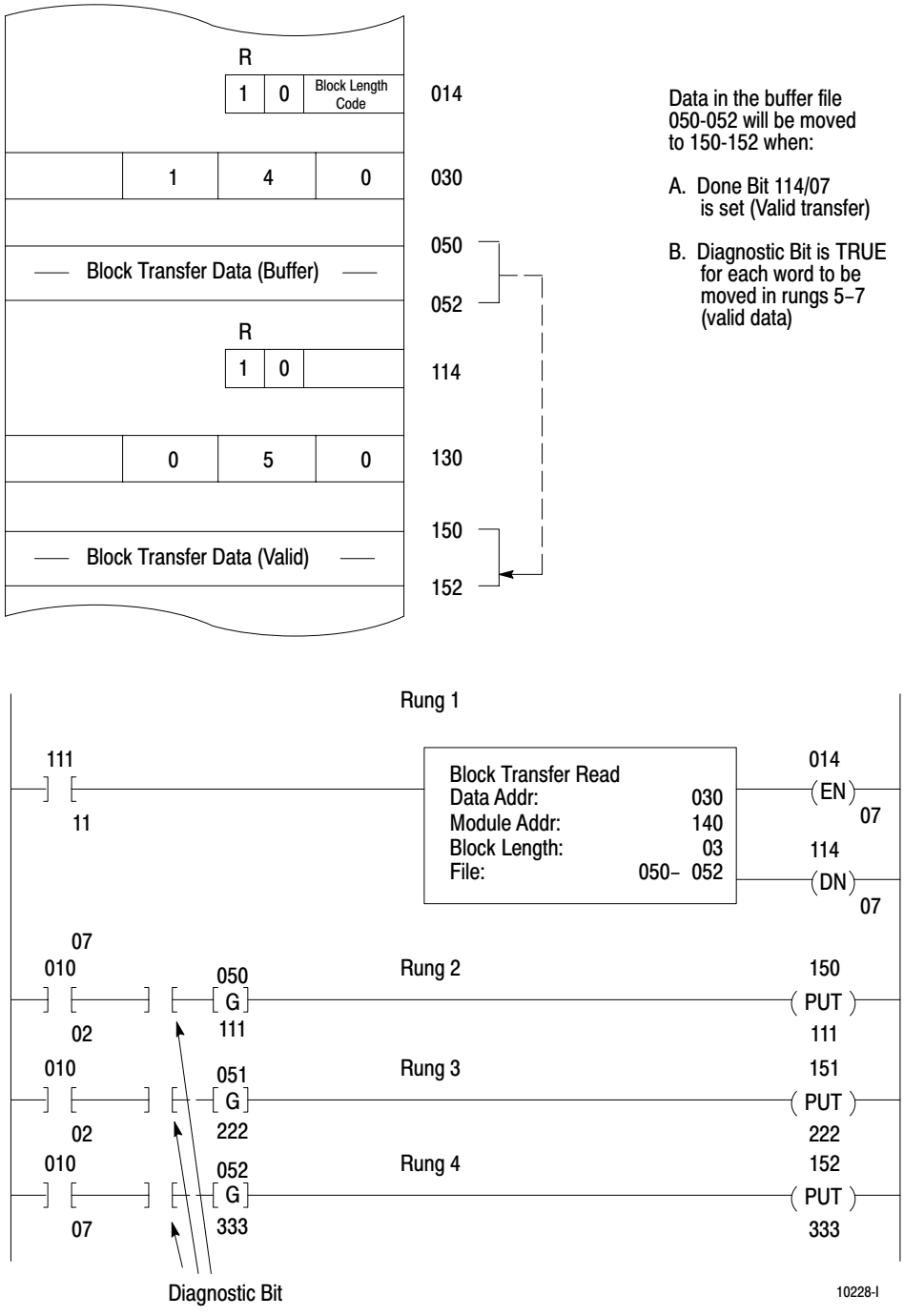
Another technique uses only one file. The technique prevents invalid data from being operated upon by preconditioning the rungs that would transfer data out of a file one word at a time. Diagnostic and/or data-valid bits are examined in these rungs.

Data can be moved from the buffer word-by-word using Get/Put transfers, or the entire file can be moved at once using a File-to-File Move instruction. The choice depends on the kinds of diagnostic and/or data-valid bits and the objectives of the user program. Generally, when one diagnostic bit is contained in each word, a get/put transfer is used. When one is set for the entire file, a File-to-File Move instruction is used. In either case, the diagnostic bits are examined as conditions for enabling the file move or word transfer.

The example in Figure 18.8 shows the memory map and ladder diagram rungs for buffering three words of data that are read from the block transfer module. The data is read and buffered in the following sequence:

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Figure 18.8
Buffering Data



1. When rung 1 is true, bit 014/07 (the block transfer enable bit) is turned on and block transfer is requested.

2. Block transfer is enabled during the program scan. The transfer is performed during an interruption of the next I/O scan. Data from the

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module is loaded into words 050-052. When block transfer is complete, done bit 114/07 is set in the input image table byte. This indicates the block transfer was successfully performed. The processor then continues with the I/O scan and program scan.

3. In rung 2, bit 114/07 is still on and a diagnostic bit is examined to ensure the data read from the module is valid. Assuming the data is valid, the diagnostic bit is on and the data is transferred from word 050 to 150. In rungs 3 and 4, the data in words 051 and 052 is transferred to words 151 and 152 if the appropriate diagnostic bits are on.

Two Get Method

If you are using a 1770-T1 or -T2 industrial terminal to program a processor and you want to perform block transfer, you must use the two Get method.

The Block Transfer rung must be programmed in a certain format (Figure 18.9). It consists of condition instructions that are optional, two Get instructions and an Output Energize instruction.

Figure 18.9
Block Transfer Rung



Here is an explanation of the optional conditions:

This Condition:	Examine the:
WYZ	First timer/counter address (accumulated area).
XYZ	Timer/counter address 100_8 higher than WYZ (preset area).
RGS	Location of the block transfer module (I/O rack, module group. and module slot. S is a zero for the left slot and a 1 for the right slot. For a 2-slot module, S is always zero.
ABC	Starting address where data in transferred to/from.
0RGST	Output energize initiates Block Transfer. 0 = output byte R = rack G = module group S = module slot T = 6 for write operation; 7 for read operation

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First Get Instruction

The first Get instruction (Figure 18.9) identifies the rack location of the block transfer module. The location must be stored in the first available address in the timer/counter accumulated value area of the data table, starting with 030. When more than one block transfer module is used, consecutive addresses must be assigned in this area.

As its "data," the first Get instruction stores the location of the block transfer module with the first digit as the rack number, the second as the I/O group number, and the third as the slot number. The processor searches the timer/counter accumulated area for a match of the module's rack, group, and slot number.

Important: Place a 2-slot module in a complete group. Do not overlap a module group when using 2-slot addressing.

Second Get Instruction

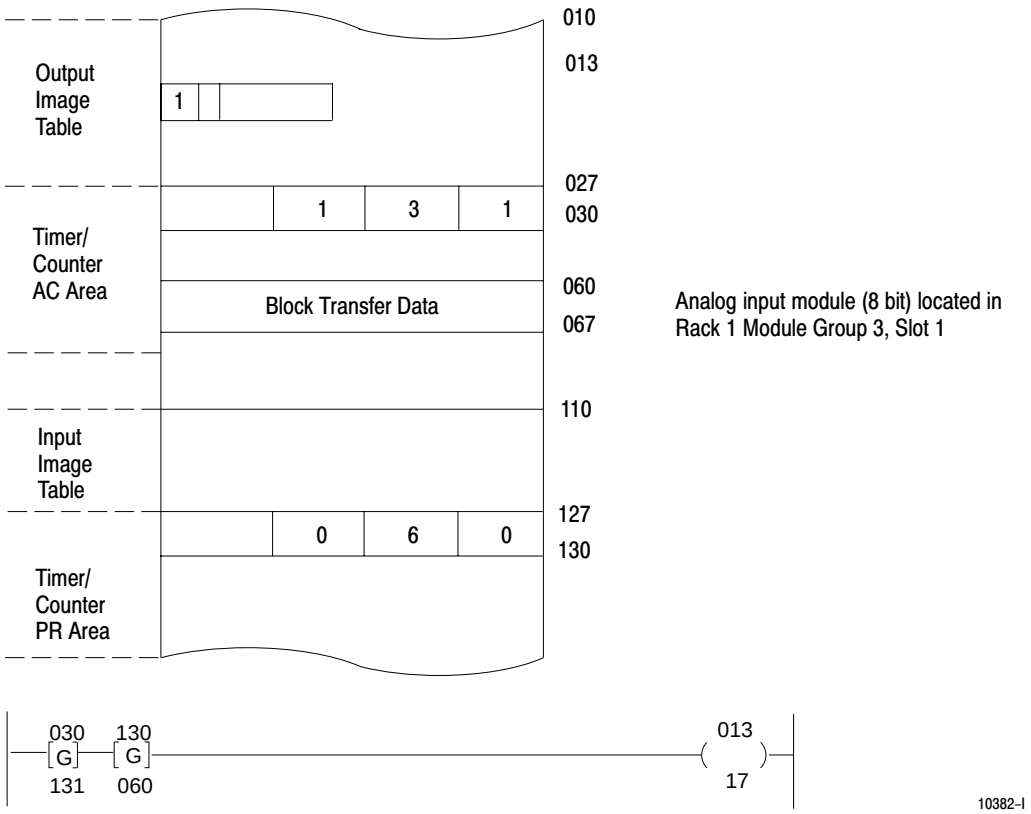
The second Get instruction (Figure 18.9) must be assigned an address in the timer/counter preset area of the data table, 100_8 words above the first Get address.

As its "data," the second Get instruction stores a data table address that designates the beginning of the file area reserved for block transfer data. During a read operation, data is loaded into consecutive word locations starting with the designated file address. During a write operation, data is sent to the module from consecutive word locations starting with the designated file address.

Important: When you reserve an area for block transfer data, select an appropriate address to ensure all block transfer data is located in one 100 word (octal) accumulated data storage area or preset area (Figure 18.10). If you select an address so the block transfer data cannot be located in a single 100 word (octal) area, the processor jumps 100_8 words to the next preset or accumulated area. If you have timers or counters in these areas, the block transfer writes over these values which may cause undesirable operation.

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Figure 18.10
Selecting Block Transfer Data Area



Output Energize Instruction

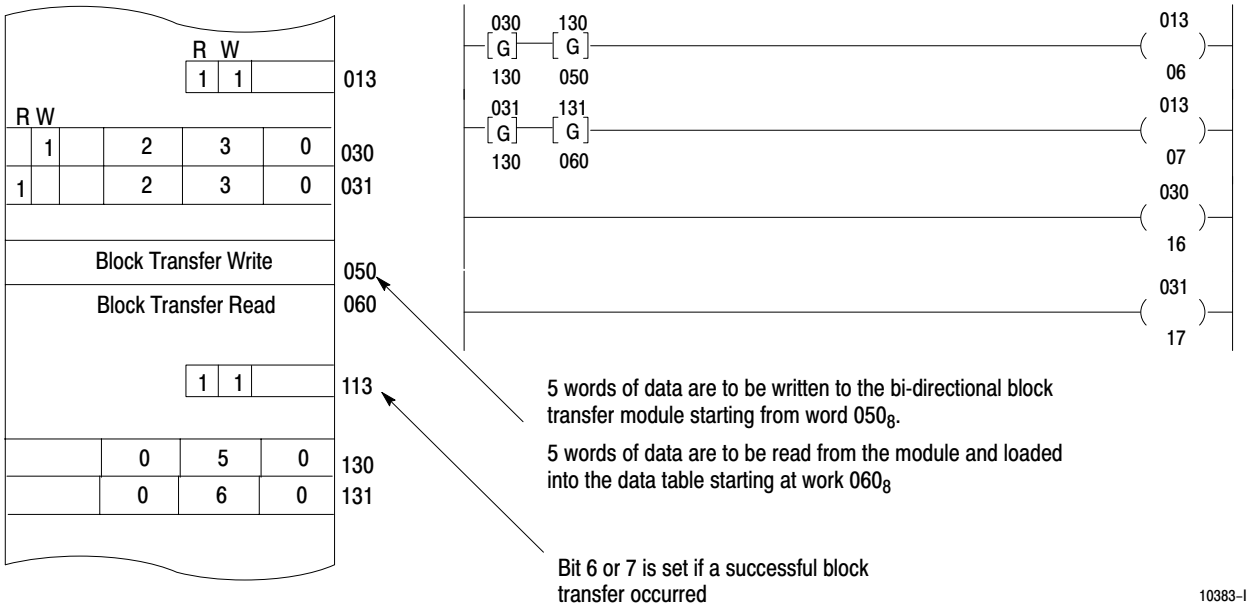
The Output Energize instruction (Figure 18.9) initiates the block transfer. It is given an address that indicates the module location and the type of block transfer operation. The first digit of the address is always 0 for output byte, even though an input or output block transfer module can be used. The next three digits identify the module location by rack, group, and slot. The last digit is either a 6 to enable a write or a 7 to enable a read. When the block transfer is successfully completed, the Read or Write done bit is set in the corresponding Input Image Table byte.

Bi-Directional Block Transfer

A bi-directional operation requires one rung for a read operation and one rung for a write operation. Consecutive addresses in the timer/counter area of the data table should be selected for the Get instructions (Figure 18.11). For example, the first Get instruction of both rungs should be assigned consecutive word addresses such as 030 and 031. Both will have the same “data” to identify the module location.

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Figure 18.11
Data Table Location for Bi-Directional Block Transfer



The second Get instruction of both rungs will be assigned addresses 100_8 words above the first Get instructions. As "data," they will store the starting address for block transfer data such as 050 and 060.

The Output Energize instruction is addressed for a write operation in rung 1 and a read operation in rung 2. To let the processor know whether a read or write operation is to be performed, bit 16 or 17 of the first Get instructions must be set On (Figure 18.11). This can be done by programming an Output Energize or Output Latch instruction unconditionally. For example, in Figure 18.11 bit 16 of word 030 is set on to indicate a write operation. Bit 17 of word 031 is set on to indicate a read operation.

Support Rungs

There are additional techniques that can be used to support the block transfer operation:

- Loading Zeros
- Setting the number of words to be transferred

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Of these support rungs, buffering data must be programmed to ensure the block transfer data is valid. Other techniques, such as an Immediate Output instruction or a scan monitor, can also be programmed. The IOT instruction requests a block transfer more than once per scan by assigning it the output word address corresponding to the module's location. Program the IOT rung immediately following the block transfer rung. A scan monitor monitors the number of scans that occurred between each block transfer operation. For programming information on the scan monitor, see the documentation for the block transfer module.

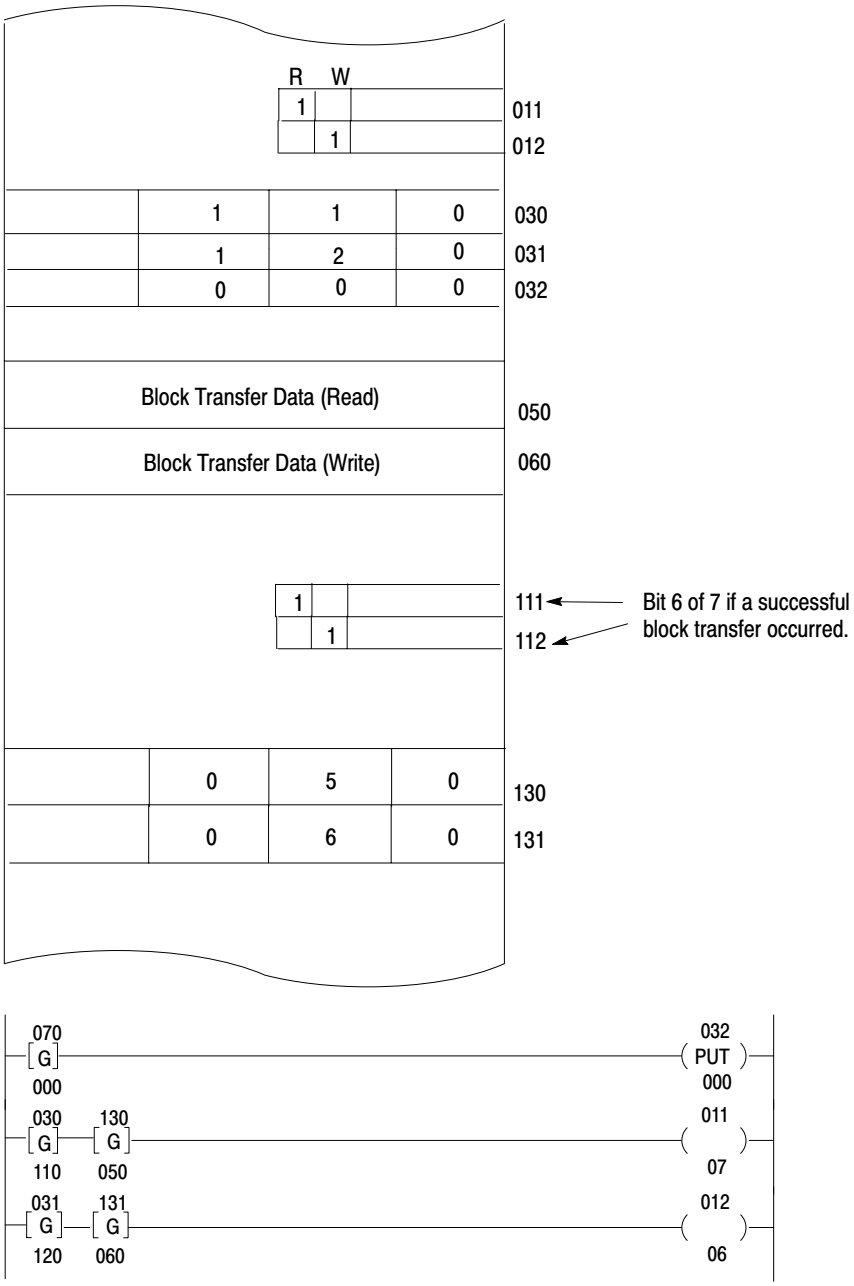
Also, if the number of words to be transferred or the location of block transfer data must change at different times, special programming techniques must be used.

Loading Zeros

One rung that can be programmed is a Get/Put transfer (Figure 18.12). It loads zeros into the timer/counter accumulated word, immediately following the last block transfer Get address that identifies the module location. The Get/Put transfer is programmed by selecting an unused storage word for the Get instruction and entering zeros for its BCD value. When a block transfer is requested, the processor starts at the first timer/counter address and searches the timer/counter area until it finds the module's rack, group, and slot number or timer/counter address with all zeros. By loading zeros into this consecutive Timer/Counter word following the last Block Transfer instruction, the processor will not search the remaining timer/counter area. In addition, the processor will not find another BCD value that may, by chance, be the same number as the rack, group or slot number.

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Figure 18.12
Loading Zeros



10384–I

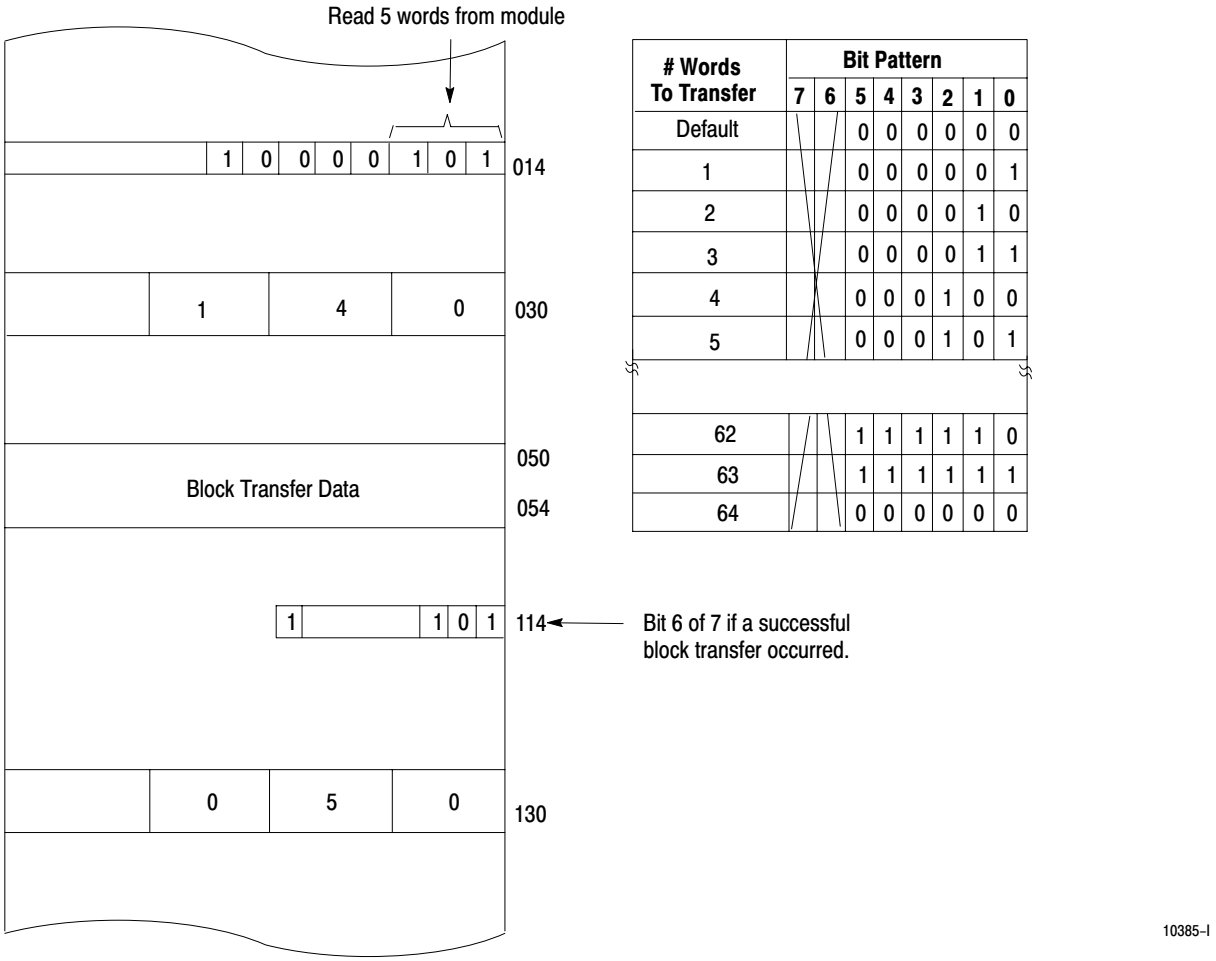
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Setting the Number of Words to Transfer

Each block transfer module has a default value that specifies the maximum number of words that can be transferred. Either the default value or some lesser value can be selected. For bi-directional block transfers, use the default value of the module. The default value varies from one kind of module to another, consult the appropriate module documentation for specifics.

When you what fewer words, set the number of words to be transferred by programming support rungs. The number of words is stored in the upper or lower Output Image Table byte that corresponds to the module's location in the I/O rack. The appropriate bits must be set On to specify a binary value that equals the number of words to transfer (Figure 18.13). These bits can be set On by programming unconditional Output Energize or Output Latch instructions.

Figure 18.13
Setting the Number of Transfer Words



# Words To Transfer	Bit Pattern							
	7	6	5	4	3	2	1	0
Default			0	0	0	0	0	0
1			0	0	0	0	0	1
2			0	0	0	0	1	0
3			0	0	0	0	1	1
4			0	0	0	1	0	0
5			0	0	0	1	0	1
62			1	1	1	1	1	0
63			1	1	1	1	1	1
64			0	0	0	0	0	0

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For example, 5 words can be transferred by setting bits 00 and 02 high unconditionally in output image table word 014. The binary equivalent of 5, as stated in the look-up table, is 000101.

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Chapter 19

Data Transfer File Instructions

Chapter Objectives

This chapter describes the data transfer file instructions:

- File-to-File Move
- Word-to-File Move
- File-to-Word Move

Figure 19.1
Types of File Instructions

Key Sequence	1770-T3 Display	Instruction Notes
FILE 10	FILE–TO–FILE MOVE COUNTER ADDR: 030 POSITION: 001 FILE LENGTH: 001 FILE A: 110– 110 FILE R: 110– 110 RATE PER SCAN: 001 030 (EN) 17 030 (DN) 15	Output Instruction Modes Complete, Distributed, and Incremental Counter is internally incremented by the instruction. Requires 5 words of user program.
FILE 11	WORD–TO–FILE MOVE COUNTER ADDR: 030 POSITION: 001 FILE LENGTH: 001 FILE A: 110 FILE R: 110– 110 030 (DN) 15	Output Instruction Counter must be externally indexed by user program. Data is transferred every scan that rung is true. Requires 4 words of user program
FILE 12	FILE–TO–WORD MOVE COUNTER ADDR: 030 POSITION: 001 FILE LENGTH: 001 FILE A: 110– 110 WORD ADDRESS: 010 030 (DN) 15	Same as word-to-file

A file is a group of consecutive data table words used to store information. A file can be between 1 and 999 words in length. The address of word 1 defines the address of the file. When displayed, the words of a file are designated consecutively by positions 001-999 according to the length of the file.

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The word address defines:

- the location in the data table to which or from which the data will be moved.
- this word address can be manipulated by ladder diagram logic

File-to-File Move Instruction

This instruction copies a source file and transfers it to the destination file address.

- It is programmed as an output instruction and requires 5 words of the user program area.
- The source file remains intact.
- The counter is incremented internally by the instruction.

Internally Indexed Counter

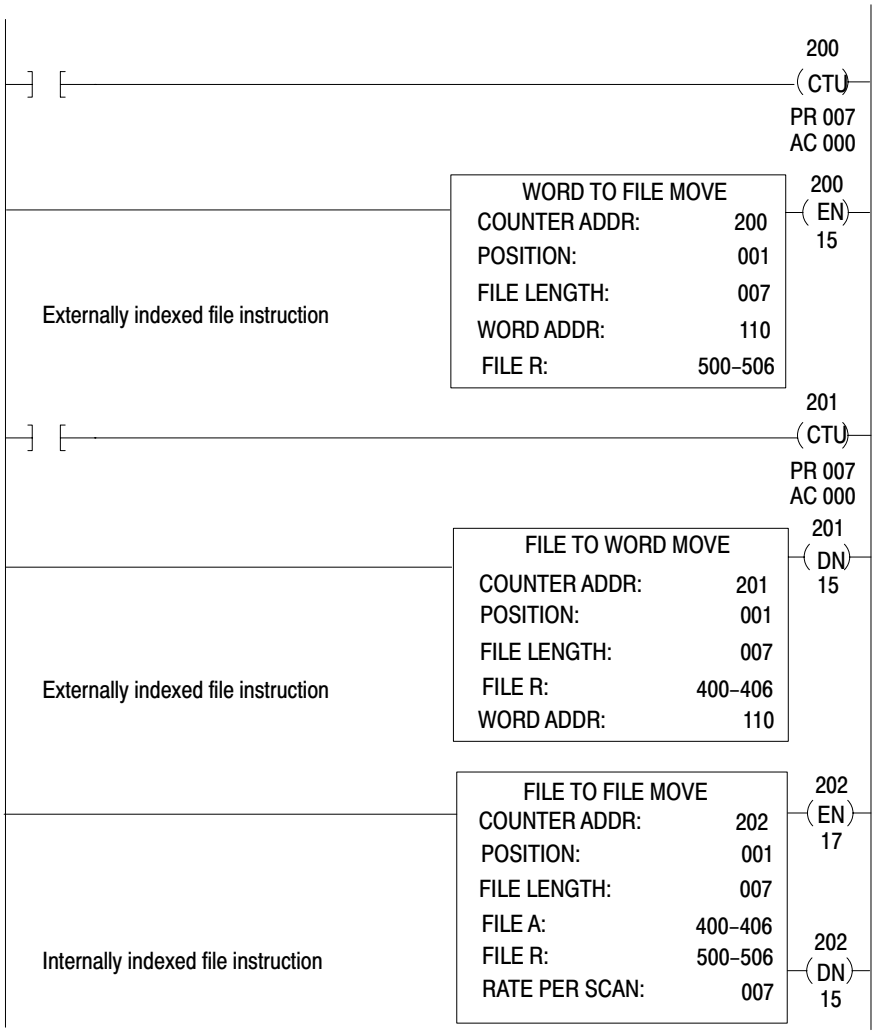
An internally indexed counter is incremented by the instruction itself. No outside control is required. You assign an address to the counter.

An internally indexed file instruction has a done bit (15) and an enable bit (17). These two bits are automatically entered from the counter address. The enable bit is set when the rung logic goes from a false to true transition; the done bit is set when the file instruction is completed.

When you look at Figure 19.2, notice that a value for rate per scan is needed. The rate per scan defines the number of words that are operated upon during one scan and is determined by the mode of operation.

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Figure 19.2
Types of Counter Indexing



Complete Mode of Operation

In the complete mode, the rate per scan is equal to the file length value and the entire file is operated upon in one scan.

For each false-to-true transition of the rung condition, the instruction is enabled and the accumulated value of the file counter is internally indexed from the first to the last word of the file. As the accumulated value points to each word, the operation defined by the file instruction is performed. After the instruction has operated on the last word, the done bit (bit 15) is set.

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When the rung condition goes false, both the done and enable bits are reset and the counter resets to position 001. If the rung was enabled for only one scan, the done bit would come on during that scan and remain set for one additional scan.

Distributed Complete Mode of Operation

In the distributed complete mode, the rate per scan is less than the file length value and the entire file is transferred over several program scans. For example, suppose you have a file that contains twelve words. If you assign the value of 004 for the rate per scan that means that the instruction executes four words per scan at a time. Therefore, the entire operation will be completed in three consecutive scans.

For each true rung condition, the instruction is enabled. The number of words equal to the rate per scan is operated upon during one scan. The process is repeated over a number of consecutive scans until the entire file has been transferred. Once the file instruction is enabled it remains enabled for the number of scans necessary to complete the operation, regardless of the rung condition.

At the time of completion, if the rung is true, the enable bit (bit 17) and the done bit (bit 15) are both set. If the rung is false, the enable bit is reset after the last group of words is operated upon. At the same time, the done bit is set and stays set for one scan. During the next scan the done bit is reset, and the counter is reset to position 001.

Incremental Mode of Operation

In the incremental mode, the rate per scan is equal to 0. This means that upon each false-to-true transition one word is operated upon per scan, then the counter increments to the next position. When the rung is true the enable bit (bit 17) is set. After the last word in the file has been operated upon, the done bit (bit 15) is set. When the rung goes false, the done and enable bits are reset (after the last word has been operated upon), and the counter is reset to position 001. If the rung remains true for more than one scan, the operation does not repeat. The operation only occurs in the scan in which the false-to-true transition occurs.

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Table 19.A
Modes of Operation

Mode of Operation	R = Rate Per Scan	Number of Words Operated Upon
Complete	R = File Length	Entire file per scan
Distributed complete	0<R< File Length	R words per scan
Incremental	R = 0	One word per rung transition



ATTENTION: The counter address for the File-to-File Move instruction should be reserved for that instruction only. Do not manipulate the counter accumulated or preset word. Changes to these values could result in unexpected machine operation with damage to equipment and/or injury to personnel.

When the rung becomes:

True — The data is transferred from the source file to the destination file at the specified rate per scan.
False — No action is taken.

Here is an explanation of each value:

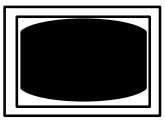
This Value:	Stores This:
Counter address	Address of the instruction's file position in the accumulated value area of the data table.
Position	Current word being operated upon (accumulated value of the counter).
File length	Number of words in file (preset value of the counter).
File A	Starting address of the source file.
File R	Starting address of the destination file.

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Keystrokes

Enter a File-to-File Move instruction by performing the following steps.





BLOCK XFER 0

Block Transfer 0 appears in the lower left corner of the screen, above the processor's current programming mode.

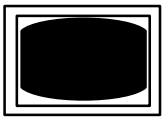
SEARCH

The word SEARCH appears in the lower left corner of the Industrial Terminal Screen.

592

Puts the processor in the remote mode.

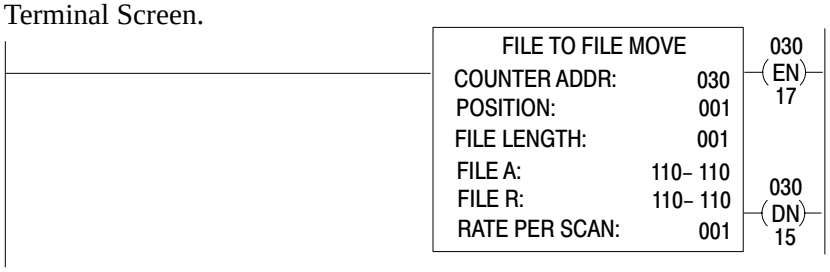




FILE

The word FILE appears in the lower left corner of the Industrial Terminal Screen.

10



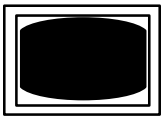
Notice that the cursor is now on the first digit of the counter address. Also, the display shows all default values.

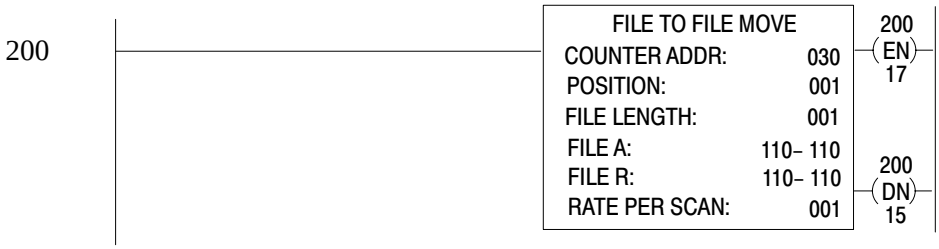
You must expand the data table to insert the following values. Follow the procedure in chapter 7. Then, your cursor will move automatically through the File-To-File Move instruction. The instructions values are:

COUNTER ADDR 200
POSITION 001
FILE LENGTH 007
FILE A 400
FILE R 500
RATE PER SCAN 007

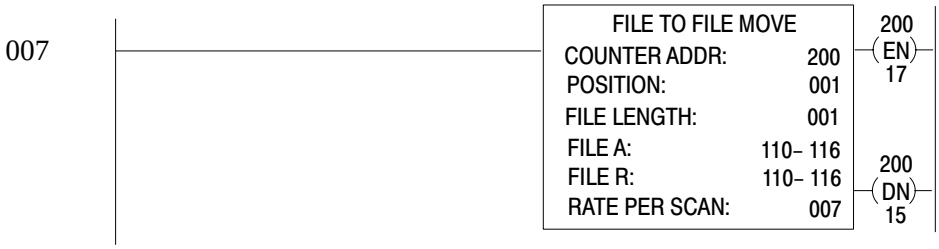
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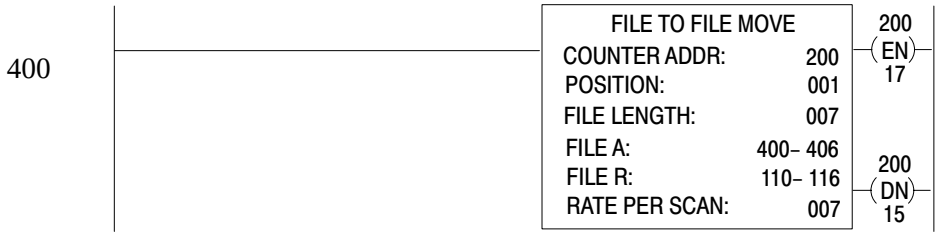




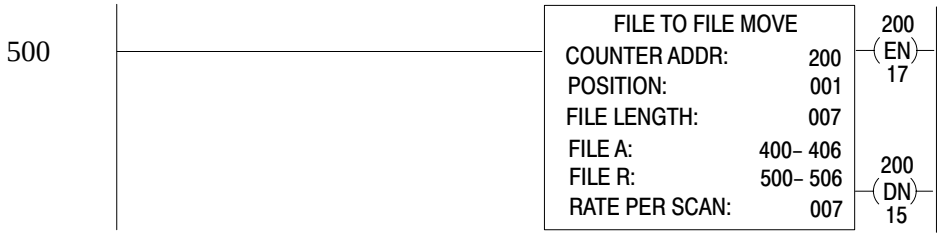
Now the cursor is on the first digit of the file length.



The cursor moved to the first digit of file A.

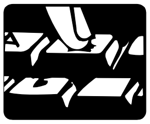


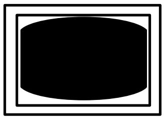
The cursor moved to the first digit of file R.



Finally, the cursor is on the first digit of the rate per scan.

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007

FILE TO FILE MOVE	
COUNTER ADDR:	200
POSITION:	001
FILE LENGTH:	007
FILE A:	400– 406
FILE R:	500– 506
RATE PER SCAN:	007

200 (EN) 17
200 (DN) 15

You can now proceed to add data to your file. Position your cursor on the words file to file move. Use the arrow keys to move your cursor. For this example, we will use the hexadecimal data monitor display.

The screen does not change.

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE
POSITION: 001

COUNTER ADDR: 200 FILE LENGTH: 007
FILE A: 400-406 FILE R: 500- 506

1

POSITION	FILE A DATA	FILE R DATA
001	0000	0000
002	0000	0000
003	0000	0000
004	0000	0000
005	0000	0000
006	0000	0000
007	0000	0000

DATA: 0000

We will now enter data in position 001 of file A.

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE
POSITION: 001

COUNTER ADDR: 200 FILE LENGTH: 007
FILE A: 400-406 FILE R: 500- 506

1257

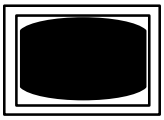
POSITION	FILE A DATA	FILE R DATA
001	0000	0000
002	0000	0000
003	0000	0000
004	0000	0000
005	0000	0000
006	0000	0000
007	0000	0000

DATA: 1257

This enters data into the command buffer.

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Important: If you made a mistake, you can correct it by moving the cursor left or right to the incorrect number and then pressing the correct number key.

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE

COUNTER ADDR: 200 POSITION: 001 FILE LENGTH: 007
FILE A: 400-406 FILE R: 500- 506

INSERT

POSITION	FILE A DATA	FILE R DATA
001	1257	0000
002	0000	0000
003	0000	0000
004	0000	0000
005	0000	0000
006	0000	0000
007	0000	0000

DATA: 1257

This information (1257) now appears in position 001 of file A. The command buffer at the bottom of the screen still displays 1257.

↓↓ Cursor down one line.

We will now add information to position 002.

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE

COUNTER ADDR: 200 POSITION: 001 FILE LENGTH: 007
FILE A: 400-406 FILE R: 500- 506

0721

POSITION	FILE A DATA	FILE R DATA
001	1257	0000
002	0000	0000
003	0000	0000
004	0000	0000
005	0000	0000
006	0000	0000
007	0000	0000

DATA: 0721

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE

COUNTER ADDR: 200 POSITION: 001 FILE LENGTH: 007
FILE A: 400-406 FILE R: 500- 506

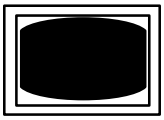
INSERT

POSITION	FILE A DATA	FILE R DATA
001	1257	0000
002	0721	0000
003	0000	0000
004	0000	0000
005	0000	0000
006	0000	0000
007	0000	0000

DATA: 0721

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Proceed by loading each position of file A with following data:

Position 003 0879
Position 004 0162
Position 005 1982
Position 006 9715
Position 007 5761

Important: You do not have to enter data in each position. You can skip position numbers.

All the data for file A is entered.

CANCEL COMMAND

The File-to-File Move instruction rung is displayed.

SEARCH

The word SEARCH appears in the lower left corner of the industrial terminal screen.

590

Puts the processor in the run/program mode.

DISPLAY

The word DISPLAY appears in the lower left corner of the industrial terminal screen.

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE

COUNTER ADDR: 200
FILE A: 400-406
POSITION: 001
FILE LENGTH: 007
FILE R: 500- 506

POSITION	FILE A DATA	FILE R DATA
001	1257	1257
002	0721	0721
003	0879	0879
004	0162	0162
005	1982	1982
006	9715	9715
007	5761	5761

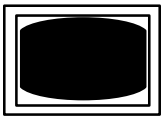
1

Notice that the data in file A transferred to file R.

Do not clear your processor memory. We will use this rung to edit the file.

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Editing in a Completed Rung

Edit a File-to-File Move instruction by performing the following steps in the hexadecimal data monitor display.

CANCEL COMMAND

The FILE TO FILE MOVE instruction rung is displayed.

SEARCH

The word SEARCH appears in the lower left corner of the industrial terminal screen.

592

Puts the processor in the run/program mode.

DISPLAY

The word DISPLAY appears in the lower left corner of the industrial terminal screen.

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE

COUNTER ADDR: 200
FILE A: 400-406

POSITION: 001

FILE LENGTH: 007
FILE R: 500- 506

POSITION	FILE A DATA	FILE R DATA
001	1257	1257
002	0721	0721
003	0879	0879
004	0162	0162
005	1982	1982
006	9715	9715
007	5761	5761

DATA: 1257

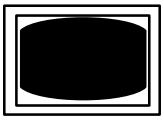
1

Notice the command buffer at the bottom of the screen. It is labeled DATA: 1257. This is also the same number in FILE A at POSITION 001.

Cursor down to POSITION 004.

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We will change the data in the command buffer from 0162 to 0281.

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE

COUNTER ADDR: 200 POSITION: 001 FILE LENGTH: 007
FILE A: 400-406 FILE R: 500- 506

0281

POSITION	FILE A DATA	FILE R DATA
001	1257	1257
002	0721	0721
003	0879	0879
004	0162	0162
005	1982	1982
006	9715	9715
007	5761	5761

DATA: 0281

HEXDECIMAL DATA MONITOR
FILE TO FILE MOVE

COUNTER ADDR: 200 POSITION: 001 FILE LENGTH: 007
FILE A: 400-406 FILE R: 500- 506

INSERT

POSITION	FILE A DATA	FILE R DATA
001	1257	1257
002	0721	0721
003	0879	0879
004	0162	0162
005	1982	1982
006	9715	9715
007	5761	5761

DATA: 0281

Notice that file R's DATA has not changed.

Now practice by changing POSITION 006 of file A to 7777.

Important: If you wanted to change the data in FILE R, follow the same procedure. To move your cursor over to file R, press [Insert] [→]. Then, follow the same procedure.

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Word-to-File Move Instruction

This instruction duplicates and transfers the data of a word from the data table to a specified word within your destination file. Here are some characteristics of a Word-to-File Move:

- Programmed as an output instruction; requires four words of the user program area.
- Your program must externally index the counter.

Externally Indexed Counter

An externally indexed counter must be controlled by a CTU/CTD instruction to index through the file values. A false-to-true transition is needed to increment the counter.

- The counter address identifies the file instruction's location in the timer/counter area of the data table and holds the accumulated value.
- The position value is the accumulated value of the counter. It points to the current position to be used/entered in the file.
- The counter's preset value represents the maximum number of words (length) in the file.
- File A is the starting address of the source file for a File-to-Word Move instruction.
- The word address is the source (input) word of a Word-to-File Move instruction. It is the destination (output) word of a File-to-Word Move instruction.
- File R is the destination file of a Word-to-File Move instruction.
- The Counter Reset instruction (CTR) resets the file (or the file's counter) once the file position is the same as the file length on the counter instruction (or the accumulated value is equal to the preset value).

An externally indexed file instruction has a done bit. The done bit (15) is automatically entered as part of the instruction. The address of the done bit is automatically changed to match the counter address. It is set when the operation is complete and remains set as long as the rung condition is true.

When a Word-to-File Move instruction rung goes:

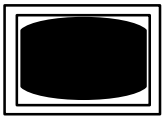
True	Data from the word address is transferred to the destination file.
False	No action is taken.

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Keystrokes

Enter a Word-File Move instruction by performing the following steps.

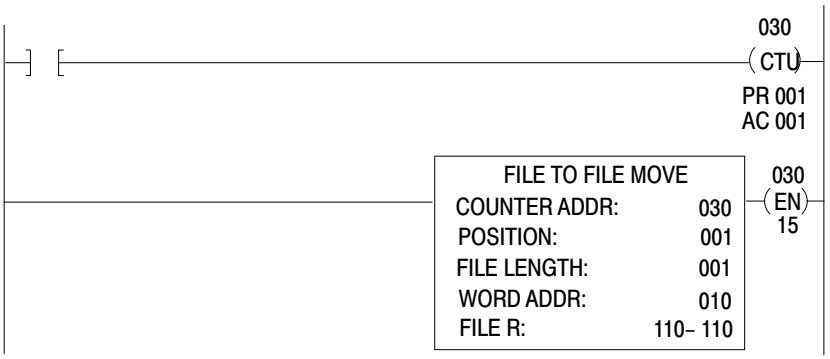




First, enter a conditioned rung with a CTU instruction for 030.

FILE

11



The word FILE appears in the lower left corner of the industrial terminal screen.

Here is an explanation of each value:

This Value:	Stores This:
Counter address	Address of the instruction's file position in the accumulated value area of the data table.
Position	Current word being operated upon (accumulated value of the counter).
File Length	Number of words in file (preset value of the counter).
File R	Starting address of the destination file.
Word Address	Address of source input word into the file.

File-to-Word Move Instruction

This instruction duplicates and transfers the data of a word within your source file to a specified word elsewhere in the data table. Here are some characteristics of a File-to-Word Move instruction:

- Programmed as an output instruction; requires four words of the user program area.
- Your program must externally index the counter. The explanation of external indexing is the same for the File-to-Word Move instruction as the Word-to-File Move.

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When the rung becomes:

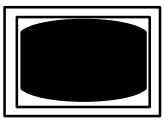
True	The data of a word is transferred from File A to a designated (output) word address.
False	No action is taken.

ATTENTION: The counter address for the Word-to-File Move and the File-to-Word Move instructions should be used only for the intended instruction and the corresponding instructions which manipulate the accumulated value. Do not inadvertently manipulate the preset or accumulated word. Changes to these values could result in unexpected machine operation with damage to equipment and/or injury to personnel.

Keystrokes

Enter a File-to-Word Move instruction by performing the following steps.

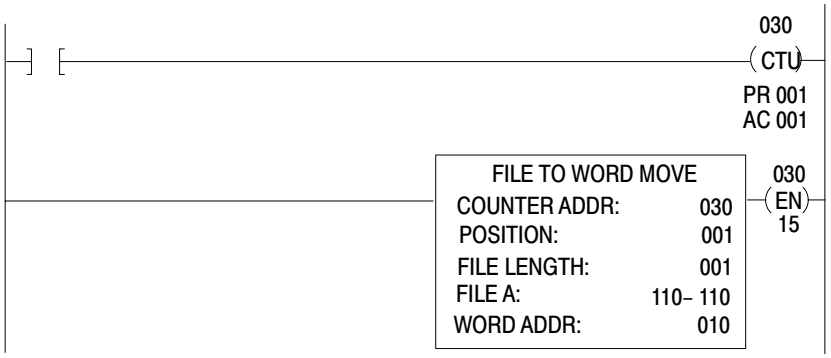




First, enter a conditioned rung with a CTU instruction for 030.

FILE

12



The word FILE appears in the lower left corner of the industrial terminal screen.

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Here is an explanation of each value:

This Value:	Stores This:
Counter address	Address of the instruction's file position in the accumulated value area of the data table.
Position	Current word being operated upon (accumulated value of the counter).
File Length	Number of words in file (preset value of the counter).
File A	Starting address of the source file.
Word Address	Address of the destination (output) word outside of the file.

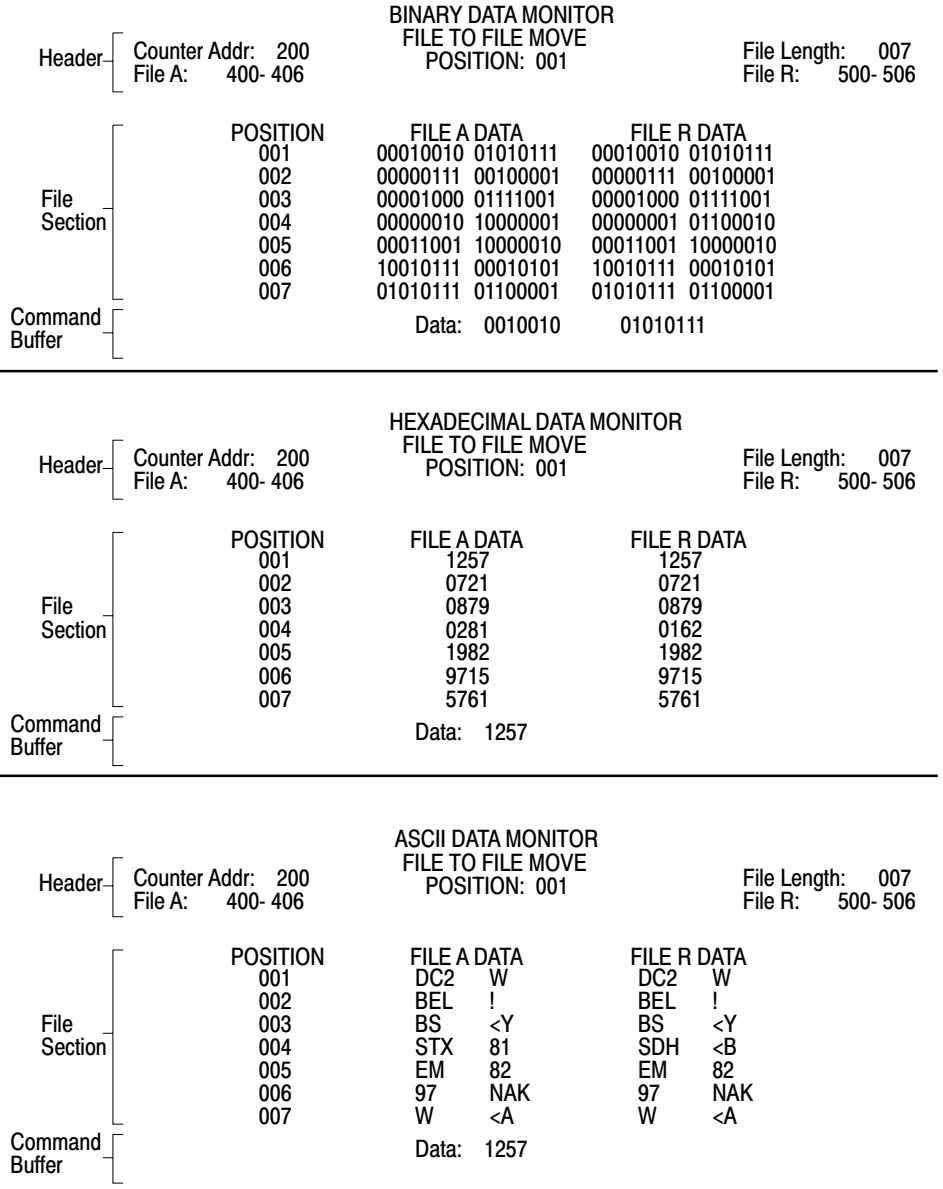
Data Monitor Display

Once you establish your file data, you'll want to edit, load, or monitor your file data. To perform these functions the processor has a data monitor mode (Figure 19.3). Use one of these displays:

- binary display (Display 0) lets you manipulate one bit at a time by displaying each word using binary digits.
- hexadecimal display (Display 1) lets you manipulate 4 digits which represents word values.
- ASCII display (Display 2) converts your four digits to the ASCII code.

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Figure 19.3
Data Monitor Displays



To print or display these monitor modes, see Table 19.B.

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Table 19.B
Data Monitor Functions

Display	[DISPLAY] [0]	Any	Displays the binary data monitor
Print	[DISPLAY] [0] [RECORD]	Any	Prints the first 20 lines of binary data monitor.
Display	[DISPLAY] [1]	Any	Displays the hexadecimal data monitor
Print	[DISPLAY] [1] [RECORD]	Any	Prints the first 20 lines of hexadecimal data monitor.
Display	[DISPLAY] [2]	Any	Displays the ASCII data monitor
Print	[DISPLAY] [2] [RECORD]	Any	Prints the first 20 lines of ASCII data monitor.

Data Monitor Functions

Three sections divide the data monitor display. They are identified in (Figure 19.3):

- **Header:** located at the top of the screen and contains information pertaining to its corresponding file instruction. For example: counter, file, and word addresses, also file length.
- **File Section:** located in the center of the screen and displays the data stored in a file. The column labeled POSITION refers to each word's position in the file. FILE A DATA represents the source file, and FILE R DATA represents the destination file.
- **Command Buffer:** located at the bottom center of the screen and is used to enter or change file data. It is always displayed in the program mode.

Adjusting the Data Table Size

You may have to expand your data table to provide additional space for files. To do this, follow the procedure in chapter 7.

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Chapter 20

Bit Shift Registers

Chapter Objectives

This chapter describes bit shift instructions. The bit shift instructions are:

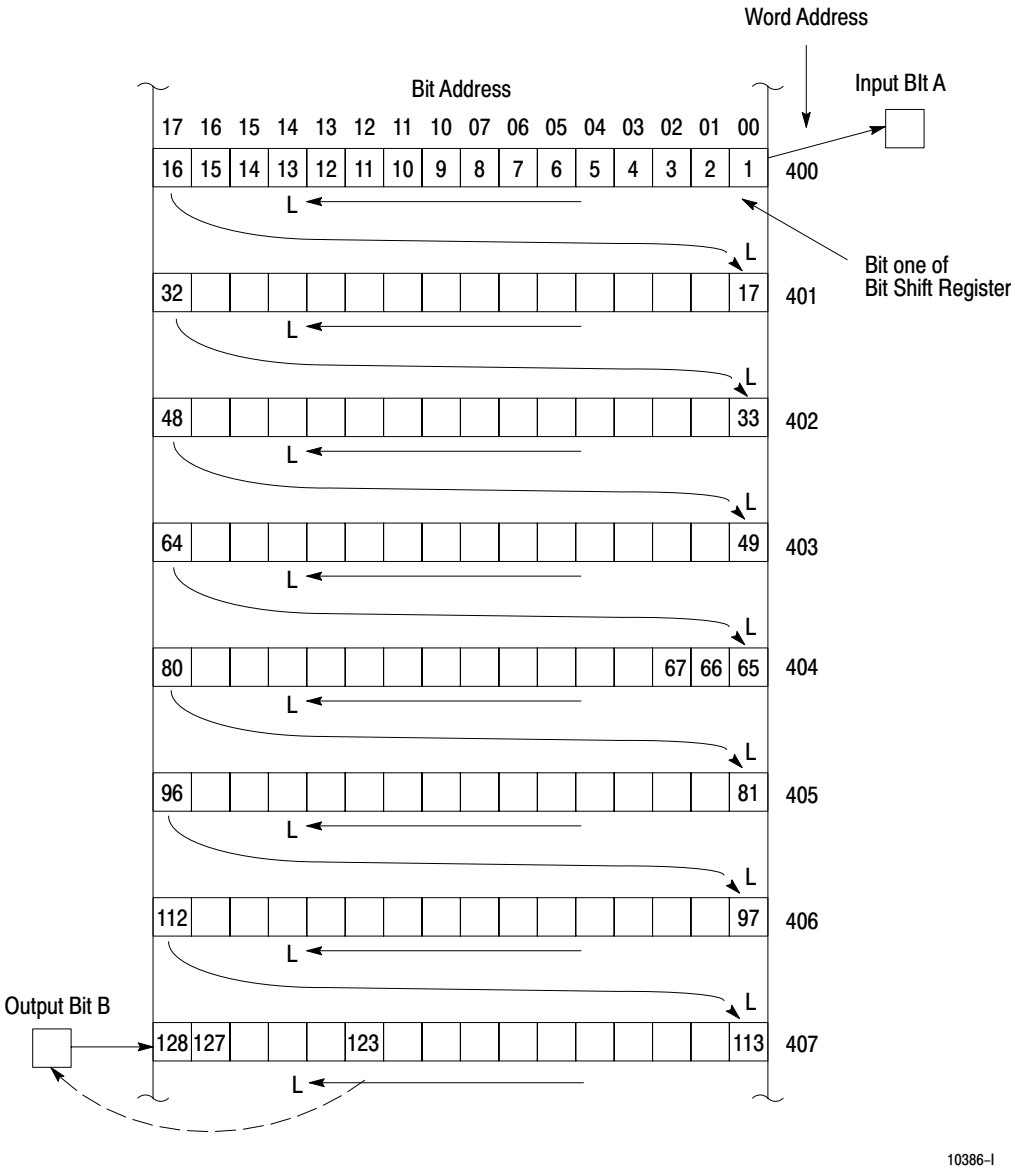
- The Bit Shift Left or Right instructions move one bit to the left or right upon the false-true transition of a rung. They are output instructions that construct and manipulate a synchronous bit shift register from 1-999 bits in length. You can perform these operations only in the complete mode.
- The Examine Off or Examine On Bit Shift instructions are condition instructions that examine bits in a shift register. You can specify the bit number to be examined and the starting address of the shift register.
- Bit Shift Set and Reset Bit Shift are output instructions that set or reset a specified bit in a bit shift register. You can specify the bit number to be manipulated and the starting address of the shift register.

Bit Shift Left

The Bit Shift Left output instruction constructs a synchronous bit shift register from 1-999 bits in length. Figure 20.1 shows a 128-bit register starting and ending at words 400 and 407.

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Figure 20.1
How the Processor Shifts a Bit to the Left



Upon false-true-rung transition, input bit A from a particular input word shifts into the first bit of the bit shift register. Bit 1 moves to the left and displaces bit 2; bit 2 displaces bit 3; and so on. Each bit displaces the one to its left until the last bit in the word (bit 16) is reached. Bit 16 displaces bit 17, which is really bit 1 of the next word (in this example, bit 401/00). Bumping continues throughout the file until last bit is ejected from the queue into output bit B.

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If the bit shift register of Figure 20.1 is 123 bits long, shifting ends at bit 12 of word 407. In this case, bits to the left of bit 12 in word 407 are not used for the bit shift register. However, they cannot be used for any other purpose. The value in bit 123 is shifted directly into output bit B when a bit shift occurs as shown by the dotted line in Figure 20.1.

The instruction operates in the complete mode. The status of the input bit is shifted into the first bit in the register and the status of the last bit in the register is shifted into the output bit in one scan.

Here are some characteristics of the Bit Shift Left instruction:

- Programmed as an output instruction
- Key sequence [Shift] [Reg] [1] [2]
- The counter is internally indexed and externally controlled by the ladder diagram logic in your program.
- Operates in complete mode

Programming a Bit Shift Left Instruction

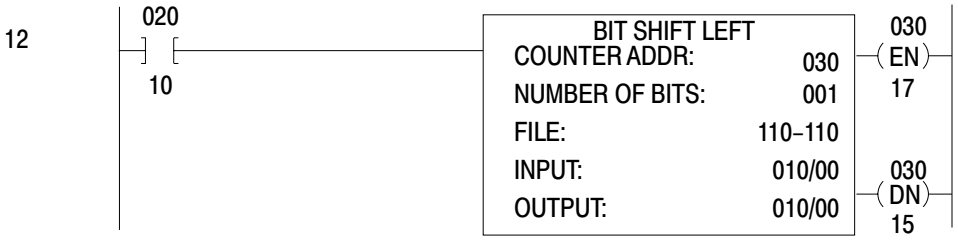
ATTENTION: The counter address specified for the Bit Shift Left instruction should be reserved for that instruction only. Do not manipulate the counter preset or accumulated values. Inadvertent changes to these values could result in hazardous or unpredictable machine operation or a run time error. Damage to equipment and/or personal injury could result.

To program a Bit Shift Left instruction:





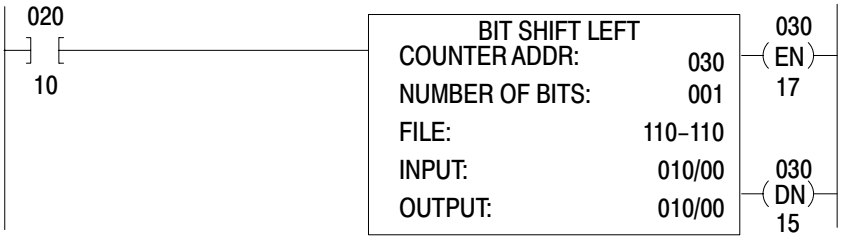
The prompt SHIFT REGISTER 12 appears in the lower left hand corner of the screen.



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A display represented by Figure 20.2 shows the format of a Bit Shift Left.

Figure 20.2
Bit Shift Left Format



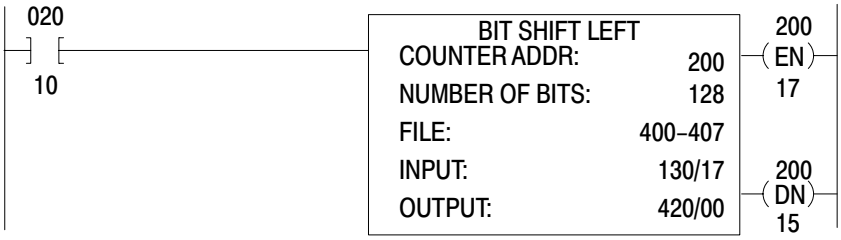
Numbers shown are default values. The number of default address digits initially displayed, 3, 4, or 5 will depend on the size of the data table. Initially displayed default values are governed by the I/O rack configuration.

This Value:	Stores This:
Counter Address	Address of the instruction in the timer/counter area of the data table. It represents the accumulated value of the instruction.
Number of Bits	Number of bits in the file.
File	Starting address of the file.
Input	Address of the input bit.
Output	Address of the output bit.

After you enter the following data, the instruction should look like Figure 20.3.

COUNTER ADDR	200
NUMBER OF BITS	128
FILE	The bit shift register starts and ends at words 400 and 407 respectively.
INPUT	The input bit is bit 17 of word 130.
OUTPUT	The output bit is bit 00 of word 420.

Figure 20.3
Bit Shift Left Example Rung



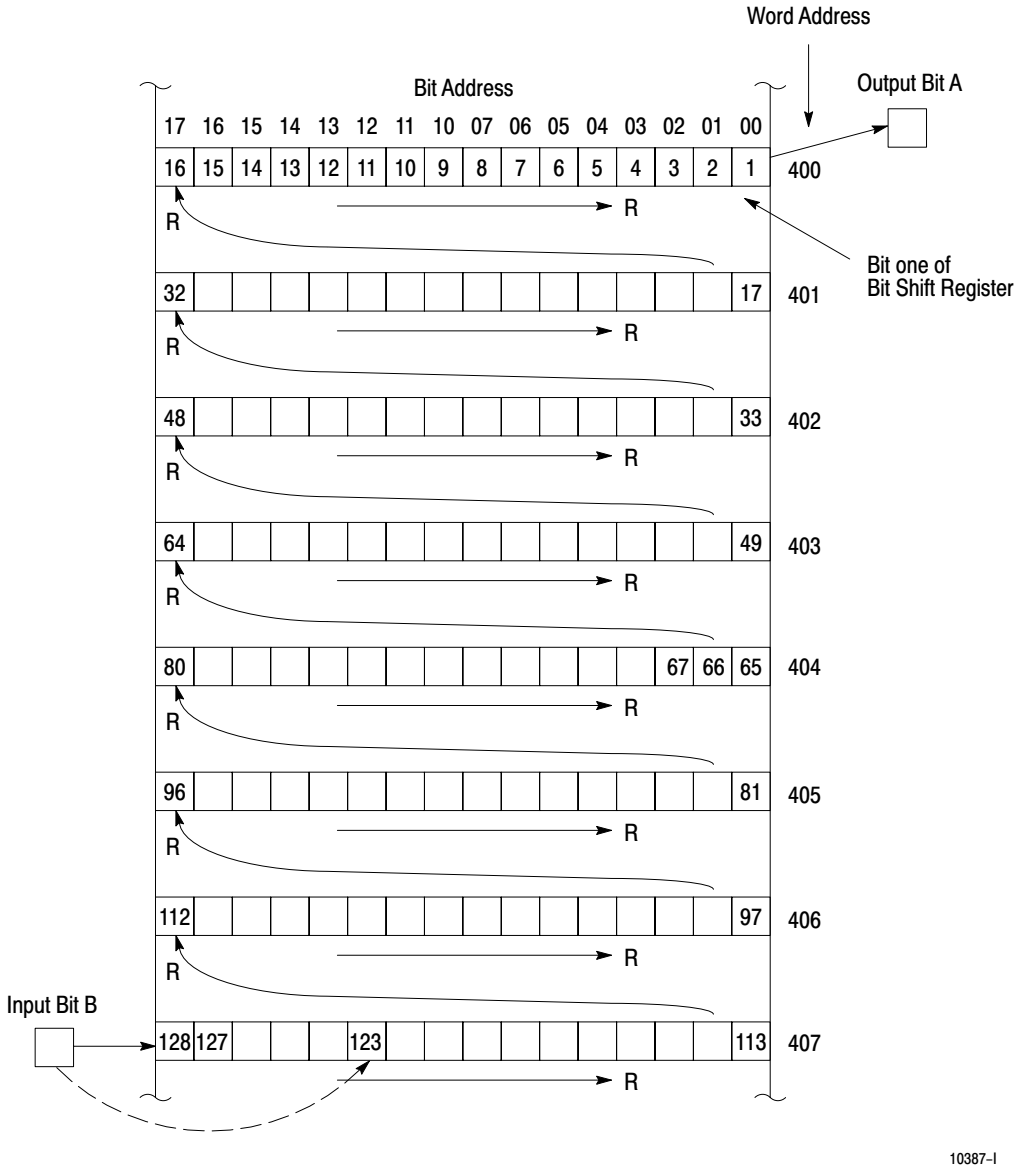
See chapter 19 for the procedure for using the data monitor. Note that bit 00 is the right side bit on the file display and bit 17 is on the left.

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Bit Shift Right

The Bit Shift Right output instruction constructs a synchronous bit shift register from 1 to 999 bits in length. Figure 20.4 shows a 128 bit register starting and ending at words 400 and 407.

Figure 20.4
How the Processor Shifts a Bit to the Right



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Upon false-to-true rung transition, input bit B from a particular input word will be inserted into the last bit of the bit shift register. In Figure 20.4, bit 128 moves right and displaces bit 127; bit 127 displaces bit 126. Each bit displaces the one on its right until the first bit in the word, 113, is reached. Bit 113 then displaces bit 112 in the previous word (in this example, bit 406/17). This bumping procedure continues throughout the queue until bit 1 is ejected from the file into output bit A.

If the bit shift register of Figure 20.4 had been 123 bits long it would have input data into bit 12 of word 407. In this case the bits to the left of bit 12 in word 407 would be unused and cannot be used for any other purpose. A Bit Shift Right will shift the on or off status of input bit B directly into bit 123 as shown by the dotted line.

The instruction operates in the complete mode. The status of the input bit is shifted into the last bit in the register and the status of the first bit in the register is shifted into the output bit in one scan.

Here are some characteristics of the Bit Shift Right instruction:

- Programmed as an output instruction
- Key sequence [Shift] [Reg] [1] [3]
- The counter is internally indexed and externally controlled by the ladder diagram logic in your program.
- Operates in complete mode
- Requires 6 words of your program

Programming Bit Shift Right Instruction



ATTENTION: The counter address specified for the Bit Shift Right instruction should be reserved for that instruction only. Do not manipulate the counter preset or accumulated values. Inadvertent change to these values could result in hazardous or unpredictable machine operation or a run time error. Damage to equipment and/or personal injury could result.

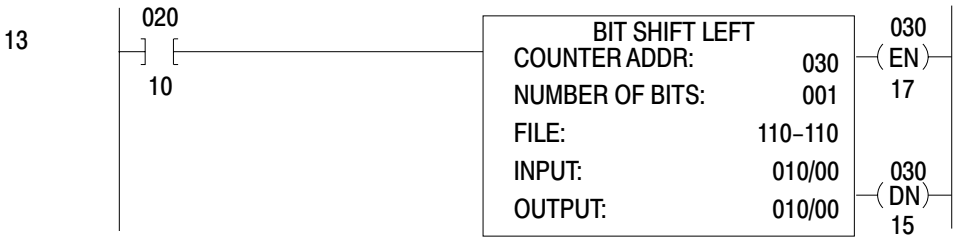
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To program a Bit Shift Right instruction:





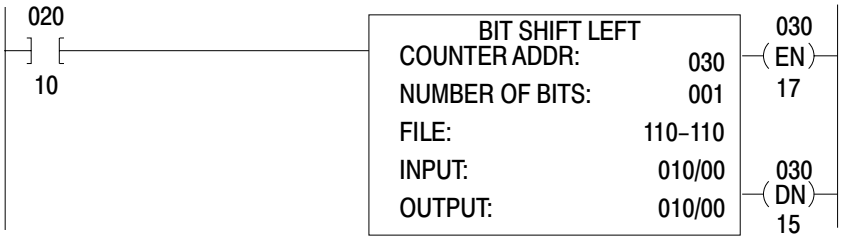
The prompt SHIFT REGISTER 12 appears in the lower left hand corner of the screen.



The format that appears and the technique for insertion of numbers, will be identical to that for Bit Shift Left except that the title will read Bit Shift Right.

The instruction should look like Figure 20.5:

Figure 20.5
Bit Shift Right Example Rung



See chapter 19 for the procedure for using the data monitor. Note that bit 00 is the right side bit on the file display and bit 17 is on the left.

Examine Off Bit Shift

This is a condition instruction that examines a user bit in a bit shift register, such as shown in Figure 20.1 or Figure 20.4, for an Off (0) condition. The instruction can be used alone or in conjunction with other condition instructions to affect the rung decision.

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Here are some characteristics of an Examine Off Bit Shift instruction:

- Program as an input instruction
- Key sequence [Shift] [Reg] [1] [8]
- Requires 3 words of your program

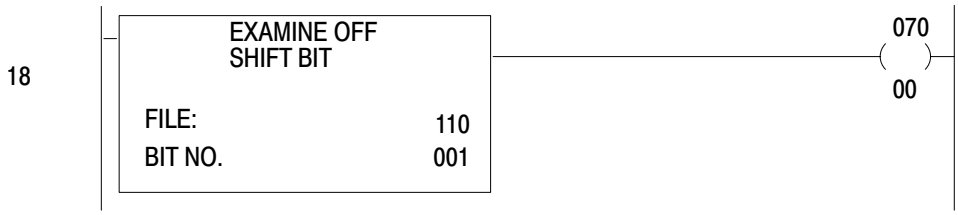
Programming an Examine Off Bit Shift Instruction

To program an Examine Off Bit Shift:



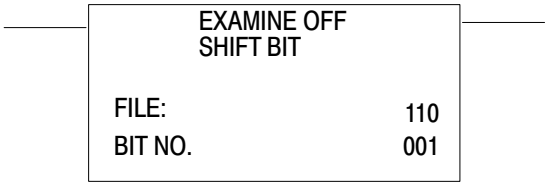


The prompt SHIFT REGISTER 12 appears in the lower left hand corner of the screen.



A display represented by Figure 20.6 shows the format of an Examine Off Bit Shift.

Figure 20.6
Examine Off Bit Shift Format



Numbers shown are default values. The number of default address digits initially displayed, 3, 4, or 5 will depend on the size of the data table. Initially displayed default values are governed by the I/O rack configuration.

This Value:	Stores This:
File	Starting address of the file (file of bit shift instruction).
Bit number	Decimal number of the bit to be examined (1-999).

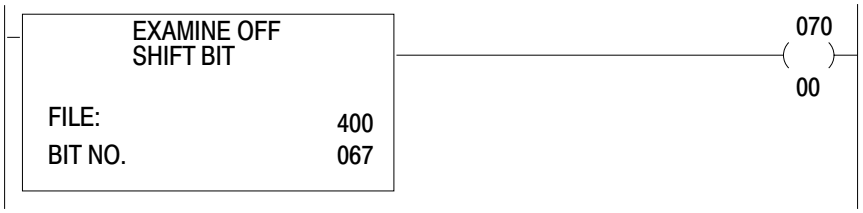
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After you have entered the following conditions:

- The file starts at word 400
- Bit number 67 is for an off (0) condition

The instruction should look like Figure 20.7.

Figure 20.7
Examine Off Bit Shift Example Rung



Examine On Bit Shift

This condition instruction examines a user specified bit in a bit shift register, such as shown in Figure 20.1 or Figure 20.4, for an On (1) condition. The instruction can be used alone or in conjunction with other input instructions to affect the rung decision.

Here are some characteristics of an Examine On Bit Shift instruction:

- Programmed as an input instruction
- Key sequence [Shift] [Reg] [1] [9]
- Requires 3 words of your program.

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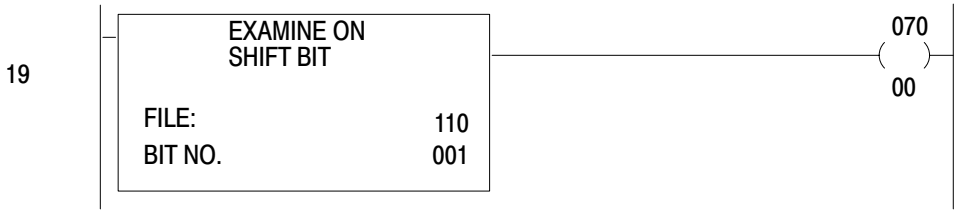
Programming an Examine On Bit Shift Instruction

To program an Examine On Bit Shift Instruction:



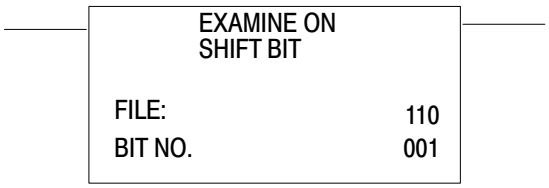


The prompt SHIFT REGISTER 12 appears in the lower left hand corner of the screen.



A display represented by Figure 20.8 shows the format of an Examine On Bit Shift.

Figure 20.8
Examine On Bit Shift Format



Numbers shown are default values. The number of default address digits initially displayed, 3, 4, or 5 will depend on the size of the data table. Initially displayed default values are governed by the I/O rack configuration.

This Value:	Stores This:
File	Starting address of the file (file of bit shift instruction).
Bit number	Decimal number of the bit to be examined (1-999).

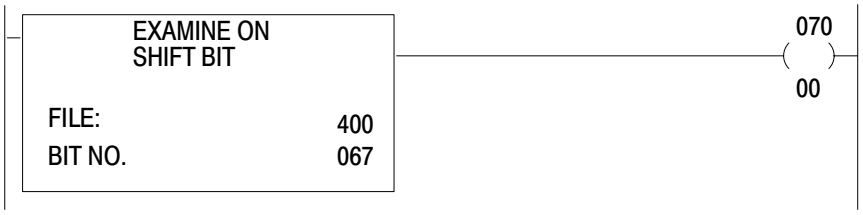
After you have entered the following conditions:

- The file starts at word 400
- Bit number 67 is for an on (1) condition.

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The instruction should look like Figure 20.9:

Figure 20.9
Examine On Bit Shift Example Rung



Set Bit Shift

The Set Bit Shift output instruction sets a specified bit in a bit shift register. You specify the bit number of the bit to be set and the starting address of the file. The instruction executes upon a true rung condition.

Important: If file is shifted and the Set Bit Shift rung is still true, new data in the same bit position will be set.

Here are some characteristics of the Set Bit Shift instruction:

- Programmed as an output instruction
- Key sequence [Shift] [Reg] [1] [6]
- Requires 3 words of your program.

Programming a Set Bit Shift Instruction

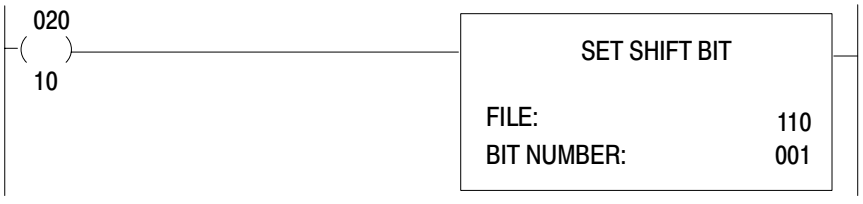
To program a Set Bit Shift instruction:





The prompt SHIFT REGISTER 12 appears in the lower left hand corner of the screen.

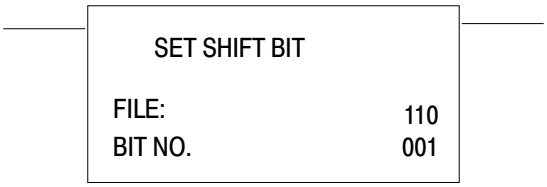
16



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A display represented by Figure 20.10 shows the format of a Set Bit Shift.

Figure 20.10
Set Bit Shift Format



Numbers shown are default values. The number of default address digits initially displayed, 3, 4, or 5 will depend on the size of the data table. Initially displayed default values are governed by the I/O rack configuration.

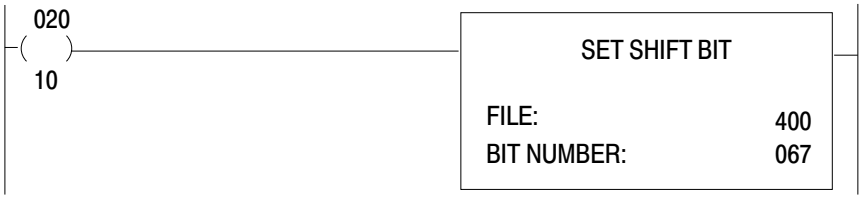
This Value:	Stores This:
File	Starting address of the file (file of bit shift instruction).
Bit number	Decimal number of the bit to be examined (1-999).

After entering the following conditions:

- The file starts at word 400
- Bit number 67 (Figure 20.1 or Figure 20.4) is on (1).

The instruction should look like Figure 20.11:

Figure 20.11
Set Bit Shift Example Rung



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Reset Bit Shift

The Reset Shift Bit output instruction turns off a specified bit in a bit shift register. You specify the bit number of the bit to be turned off and the starting address of the file. The instruction executes upon a true rung condition.

Important: If file is shifted, new data in the same bit position will be reset if the Reset Shift Bit rung is still true.

Here are some characteristics of a reset shift bit instruction:

- Programmed as an output instruction
- Requires 3 words of your program
- Key sequence [Shift] [Reg] [1] [7]

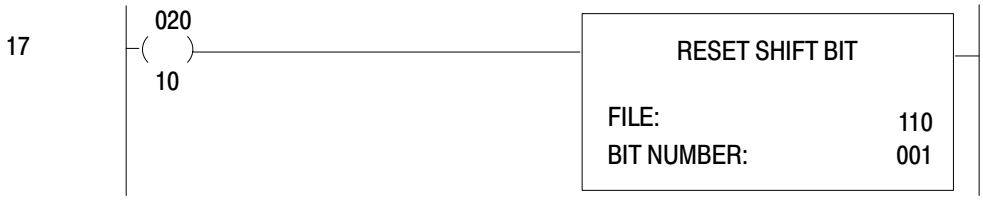
Programming a Reset Bit Shift Instruction

To program a Reset Bit Shift instruction:





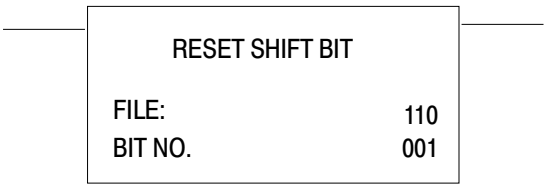
The prompt SHIFT REGISTER 12 appears in the lower left hand corner of the screen.



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A display represented by Figure 20.12 shows the format of a Reset Bit Shift.

Figure 20.12
Reset Bit Shift Format



Numbers shown are default values. The number of default address digits initially displayed, 3, 4, or 5 will depend on the size of the data table. Initially displayed default values are governed by the I/O rack configuration.

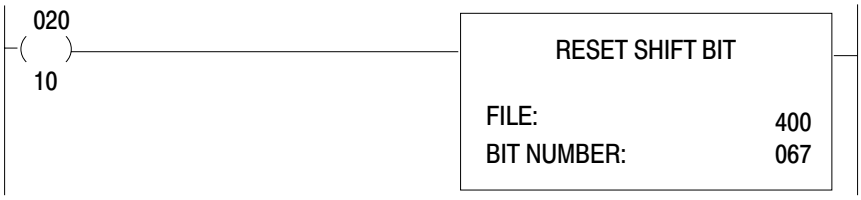
This Value:	Stores This:
File	Starting address of the file (file of bit shift instruction).
Bit number	Decimal number of the bit to be examined (1-999).

After you have entered the following conditions:

- The file starts at word 400_8.
- Bit number 67 (Figure 20.1 or Figure 20.4) is off (0).

The instruction should look like Figure 20.13:

Figure 20.13
Reset Shift Bit Example Rung



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Chapter 21

Sequencers

Chapter Objectives

This describes the three types of sequence instructions:

- sequencer input
- sequencer output
- sequencer load

These instructions either transfer information from the data table to output word addresses, compare I/O word information with information stored in tables, or transfer I/O word information into the data table.

Comparison with File Instructions

Sequencer instructions are similar to file instructions but have some marked differences. Both are block instructions that contain a counter and a file. The instructions require the entry of more than one address. Each has a corresponding data monitor display for monitoring, loading or editing file data.

File instructions operate on files that are 1 word (16 bits) wide. In contrast, sequencer instructions operate on files that are as many as 4 words (64 bits) wide with as many as 999 rows. A sequencer file can be represented graphically by a sequencer table (Figure 21.1.)

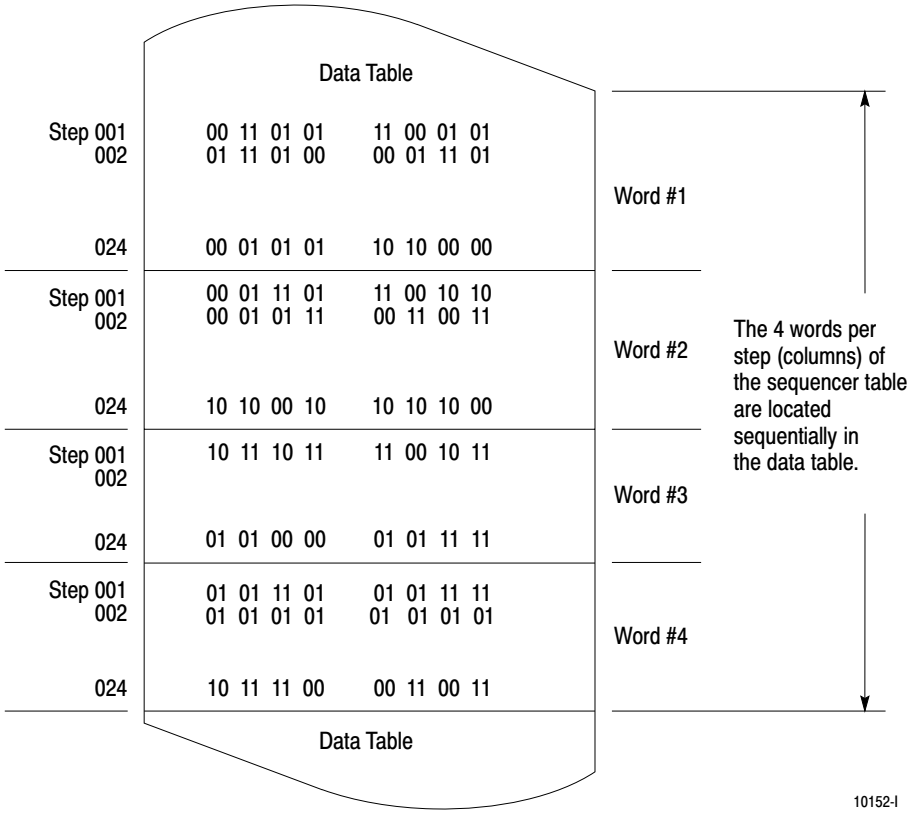
Figure 21.1
Sequencer Table

Step	Word 1	Word 2	Word 3	Word 4
001	00110101 11000101	00011101 11001010	10111011 11001011	01011101 01011111
002	01110100 00011101	00010111 00110011	"	01010101 01010101
003	"	"	"	"
"	"	"	"	"
"	"	"	"	"
"	"	"	"	"
"	"	"	"	"
"	"	"	"	"
"	"	"	"	"
024	00010101 10100000	10100010 10101000	01010000 01011111	10111100 00110011

Important: The sequencer's data table is one word wide by many long. A sequencer table appears in the data table as one continuous file. The length of the file in the data table equals the product of the number of steps and the length as shown in Figure 21.2. As an example, a 24 step x 4 word wide sequencer table occupies 96 consecutive words in the data table.

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Figure 21.2
Sequencer Table Format in the Data Table



Internally indexed file instructions perform the operation and then increment to the next step. In contrast, internally indexed sequencer instructions increment to the next step and then the operation is performed.

Mask

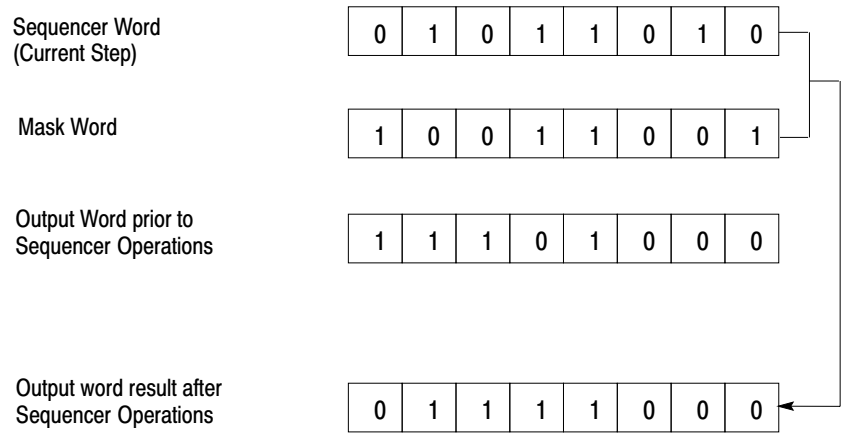
A special programming technique called a “mask” is used with the sequencer instructions. A mask is a means of controlling what bits are controlled/compared by the sequencer instruction. By masking bits, you ensure that the sequencer instruction does not affect them. The masked bits may then be used for other program purposes.

A zero (0) in a mask bit location prevents the sequencer instruction transferring data from its file to the output bit location. The output bit is left in its current/last state. A one (1) in a mask bit location allows the instruction to transfer data from the file to the output bit. For all data bits to transfer, a mask of all ones should be used.

Figure 21.3 shows the result of masking transfer data. Although a word contains 16 bits, only 8 bits are shown for clarity.

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Figure 21.3
Masking Transfer Data



Other instructions can change a mask in the user program. If a changing mask is required for different steps in the sequencer operation, a Get/Put or file move can be used.

ATTENTION: When choosing a mask word address, be sure that the next 1, 2, or 3 consecutive word addresses are not already assigned. Other data written into a mask could cause unpredictable machine operation. This could cause damage to your equipment and/or injury to your personnel.

Programming Limitations

Only one step is executed at a time for each instruction.

The Sequencer Input instruction can be programmed in the same rung as the Sequencer Output instruction. The sequencer input counter (step counter) can be indexed by the Sequencer Output instruction. The step counter in both instructions is given the same address. When programmed in this manner, the Sequencer Input and Output instructions will track through a controlled sequence of operations. The length of the sequencer is equal to the number of steps (Seq Length) in the sequencer data table.

Sequencer Instructions

Use Figure 21.4 while you read about each sequencer instruction.

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Figure 21.4
Sequencer Instructions

Key Sequence	1770-T3 Display	Instruction Notes
SEQ 0	SEQUENCER OUTPUT COUNTER ADDR: 030 CURRENT STEP: 001 SEQ LENGTH: 001 WORDS PER STEP: 1 FILE: 110– 110 MASK: 010– 010 OUTPUT WORDS 1: 010 2: [redacted] 3: [redacted] 4: [redacted] 030 (EN) 17 030 (DN) 15	Output instruction Increments, then transfers data. Same data transferred each scan that the rung is true. Counter is indexed by the instruction. Unused output bits can be masked. Requires 5–8 words of your program.
SEQ 1	SEQUENCER INPUT COUNTER ADDR: 030 CURRENT STEP: 000 SEQ LENGTH: 001 WORDS PER STEP: 1 FILE: 110– 110 MASK: 010– 010 INPUT WORDS 1: 010 2: [redacted] 3: [redacted] 4: [redacted]	Input instruction. Compares input data with current step for equality. Counter must be externally indexed by a counter instruction within your program. Unused input bits can be masked. Requires 5–8 words of your program.
SEQ 2	SEQUENCER LOAD COUNTER ADDR: 030 CURRENT STEP: 000 SEQ LENGTH: 001 WORDS PER STEP: 1 FILE: 110– 110 LOAD WORDS 1: 010 2: [redacted] 3: [redacted] 4: [redacted] 030 (EN) 17 030 (DN) 15	Output instruction. Increments, then loads data. Counter is indexed by the instruction. Does not mask. Requires 4–7 words of your program.

Important: Numbers shown are default values. Numbers in shaded areas must be replaced by user–entered values. The number of default address digits displayed (3 or 4) will depend on the size of the data table.

Here is an explanation of each value:

This Value:	Stores the:
Counter Address	Address of the instruction in the accumulated value area of the data table
Position	Position in the sequencer table (accumulated value of counter)
Seq Length	Number of steps (preset value of the counter)
Words per Step	Width of the sequencer table
File	Starting address of the source file
Mask	Starting address of the mask file
Word Address	Address of the source word or destination word outside of the file
Output Words	Words controlled by the instruction
Load Words	Words fetched by the instruction
Input Words	Words monitored by the instruction

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Sequencer Input

The Sequencer Input instruction compares all 16 bits of input data to data stored in its file (data table) for equality. Here are some characteristics of the sequencer input instruction.

- You can compare up to 64 bits.
- This instruction is programmed as an input instruction (can be programmed in the same rung as a sequencer output instruction).
- You can mask the unused input bits.
- The sequencer input instruction is externally controlled by a counter instruction with ladder logic in your program.
- This instruction requires 5-8 words of your program.

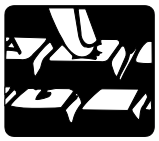
If the rung becomes:

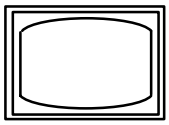
True	The instruction increments to the next step and compares the input word(s) to current step for equality.
False	No action is taken.



ATTENTION: The counter address for the Sequencer Output instruction should be reserved for that instruction. Do not manipulate the counter accumulated or preset values. Inadvertent changes to these values could result in hazardous machine operation or a run time error. Damage to equipment and/or personal injury could result.

To enter a Sequencer Input instruction, start by expanding your data table if required. Expand it to a size large enough to store your program.





SEARCH

The word SEARCH appears in the lower left corner of the Industrial Terminal Screen.

592

Puts the processor in the remote program mode.

50

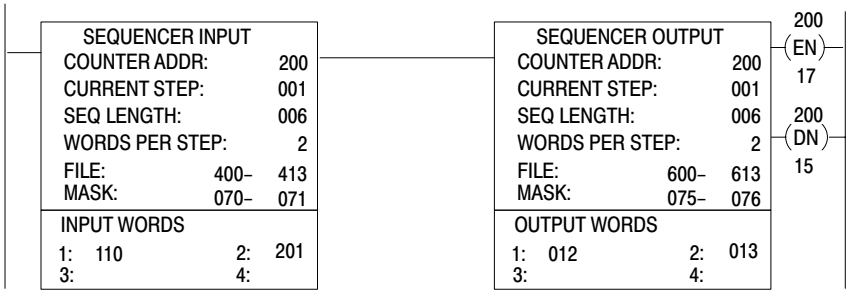
The DATA TABLE CONFIGURATION appears. The cursor is on the first digit of NUMBER OF 128 WORD D. T. BLOCKS.

04

To be able to use the sequencer input, output ,and load examples, do the following:

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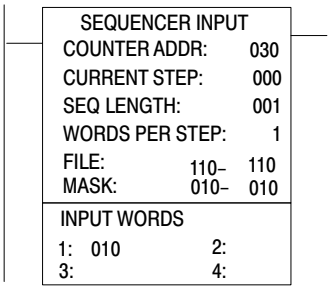
The cursor moves to the digit 4 and DATA TABLE SIZE changes to 512. This gives you a 512 word data table. After you adjust the data table press CANCEL COMMAND. You are now ready to insert this program.







The word SEQUENCER appears in the lower left hand corner of the screen.



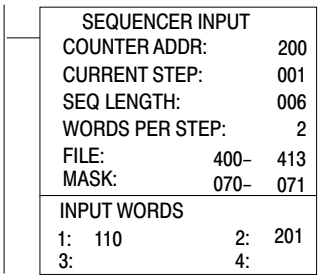
Notice that the words SEQUENCER INPUT are flashing, the cursor is on the first digit of counter address, and the default values are shown.

Insert the following values. Your cursor will move automatically throughout the sequencer instruction. The values are:

COUNTER ADDR:	200
CURRENT STEP:	001
SEQ LENGTH:	006
WORDS PER STEP:	2
FILE:	400
MASK:	070
INPUT WORDS:	1: 110
	2: 201

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The instruction should look like this:



To continue, enter your data using the binary data monitor mode. You will get your data from the worksheet in Figure 21.5. A filled in block means that a 1 should be inserted in the corresponding bit position.

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Figure 21.5
Completed Sequencer Input Worksheet

ALLEN-BRADLEY
Programmable Controller
Sequencer Table Bit Assignments

PAGE 1 OF 2

PROJECT NAME Bottle Filling Applications PROCESSOR Mini-PLC-2/16

DESIGNER Engineer DATA TABLE ADDR _____ TO _____

SEQUENCER Input

COUNTER ADDR: 200 FILE 400 TO 413 SEQ LENGTH: 006

WORD ADDR: 110 Timer 200

MASK ADDR: 070 071

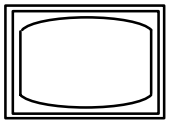
DEVICE NAME	WORD #1 17 10 07 00	WORD #2 17 10 07 00	WORD #3 17 10 07 00	WORD #4 17 10 07 00
	Auto *LS2* *LS1* *PC*	*Timer*		
MASK	■ ■ ■ ■	■		
STEP				
1	■ ■			
2	■ ■			
3	■ ■			
4	■ ■	■		
5	■ ■			
6	■			
FROM ADDR				
TO ADDR				

Note: A filled-in box means that each device is actuated

10145-I

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Start by positioning your cursor on the words SEQUENCER INPUT. Use the arrow keys to move the cursor.

DISPLAY

The word display appears in the lower left hand corner of the screen.

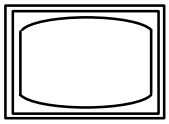
```
                                BINARY DATA MONITOR
                                SEQUENCER OUTPUT
0     COUNTER ADDR:   200              STEP:   001              SEQUENCER LENGTH:   006
                                       FILE:   400- 413
                OUTPUT ADDR:   110                    201
                DATA:   00000000 00000000    00000000 00000000
                MASK ADDR:     070                    071
                DATA:   00000000 00000000    00000000 00000000
                STEP        WORD 1                WORD 2
                001   00000000 00000000    00000000 00000000
                002   00000000 00000000    00000000 00000000
                003   00000000 00000000    00000000 00000000
                004   00000000 00000000    00000000 00000000
                005   00000000 00000000    00000000 00000000
                006   00000000 00000000    00000000 00000000
                              DATA:   00000000 00000000
```

The cursor is located on the last digit of the first word of DATA in the Command Buffer. The digits in step 1 for word 1 are intensified.

```
                                BINARY DATA MONITOR
                                SEQUENCER OUTPUT
00000010 00000000     COUNTER ADDR:   200              STEP:   001              SEQUENCER LENGTH:   006
                                                       FILE:   400- 413
                OUTPUT ADDR:   110                    201
                DATA:   00000000 00000000    00000000 00000000
                MASK ADDR:     070                    071
                DATA:   00000000 00000000    00000000 00000000
                STEP        WORD 1                WORD 2
                001   00000000 00000000    00000000 00000000
                002   00000000 00000000    00000000 00000000
                003   00000000 00000000    00000000 00000000
                004   00000000 00000000    00000000 00000000
                005   00000000 00000000    00000000 00000000
                006   00000000 00000000    00000000 00000000
                              DATA:   00000010 00000000
```


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```
                          BINARY DATA MONITOR
                          SEQUENCER OUTPUT
COUNTER ADDR:   200              STEP:   001          SEQUENCER LENGTH:   006
                                 FILE:   400- 413
          OUTPUT ADDR:   110                  201
          DATA:          00000000 00000000    00000000 00000000
          MASK ADDR:     070                  071
          DATA:          00000000 00000000    00000000 00000000
          STEP      WORD 1               WORD 2
          001       00000010 00000000    00000000 00000000
          002       00000000 00000000    00000000 00000000
          003       00000000 00000000    00000000 00000000
          004       00000000 00000000    00000000 00000000
          005       00000000 00000000    00000000 00000000
          006       00000000 00000000    00000000 00000000
                    DATA:    00000010 00000000
```

INSERT

Data is inserted into Step 001 of Word 1.

↓ ↓

Cursor down one line.

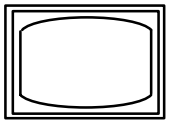
The cursor is on the last digit of the second word of DATA in the command buffer. The digits in step 2 for word 2 are intensified.

```
                          BINARY DATA MONITOR
                          SEQUENCER OUTPUT
COUNTER ADDR:   200              STEP:   001          SEQUENCER LENGTH:   006
                                 FILE:   600- 613
          OUTPUT ADDR:   012                  013
          DATA:          00000000 00000000    00000000 00000000
          MASK ADDR:     075                  076
          DATA:          00000000 00000000    00000000 00000000
          STEP      WORD 1               WORD 2
          001       00000010 00000000    00000000 00000000
          002       00000000 00000000    00000000 00000000
          003       00000000 00000000    00000000 00000000
          004       00000000 00000000    00000000 00000000
          005       00000000 00000000    00000000 00000000
          006       00000000 00000000    00000000 00000000
                    DATA:    00000010 00001001
```

00000010 00000001

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```
                        BINARY DATA MONITOR
                        SEQUENCER OUTPUT
COUNTER ADDR:  200          STEP:  001          SEQUENCER LENGTH:  006
                            FILE:  600- 613
OUTPUT ADDR:  012                       013
DATA:  00000000 00000000    00000000 00000000
MASK ADDR:  075                         076
DATA:  00000000 00000000    00000000 00000000
STEP        WORD 1          WORD 2
001    00000010 00000000    00000000 00000000
002    00000010 00000001    00000000 00000000
003    00000000 00000000    00000000 00000000
004    00000000 00000000    00000000 00000000
005    00000000 00000000    00000000 00000000
006    00000000 00000000    00000000 00000000
                DATA:  00000010 00000001
```

INSERT

↓ ↓

Cursor down one line.

The cursor is on the last digit of the third word of DATA in the command buffer. The digits in step 3 for word 3 are intensified.

Continue inserting your data.

003: 00000010 00010001
004: 00000010 00010001
005: 00000010 01000001
006: 00000010 00000000

To add data to WORD 2 press [Shift] [→] and cursor up or down as needed.

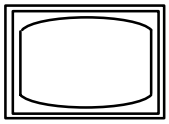
Do not press [Cancel Command]. We will use the display to add a mask.

DISPLAY

The word DISPLAY appears in the lower left hand corner of the screen.

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000

```
                    BINARY DATA MONITOR
                    SEQUENCER OUTPUT
COUNTER ADDR:  200          STEP:  001          SEQUENCER LENGTH:  006
                            FILE:  400- 413
OUTPUT ADDR:  110                       201
DATA:  00000000 00000000    00000000 00000000
MASK ADDR:  070                         071
DATA:  00000000 00000000    00000000 00000000
STEP        WORD 1          WORD 2
001  00000010 00000000      00000000 00000000
002  00000010 00000001      00000000 00000000
003  00000010 00010001      00000000 00000000
004  00000010 00010001      00000000 00000000
005  00000010 01000001      00000000 00000000
006  00000010 00000000      00000000 00000000
DATA:  00000010 00000000
```

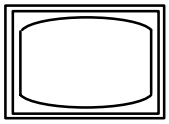
The cursor is on the first digit of DATA in the command buffer. The digits for INPUT ADDR 110, DATA are intensified. Cursor down one line. The display for MASK ADDR 070, DATA are intensified.

00000010 01010001

```
                    BINARY DATA MONITOR
                    SEQUENCER OUTPUT
COUNTER ADDR:  200          STEP:  001          SEQUENCER LENGTH:  006
                            FILE:  400- 413
OUTPUT ADDR:  110                       201
DATA:  00000000 00000000    00000000 00000000
MASK ADDR:  070                         071
DATA:  00000000 00000000    00000000 00000000
STEP        WORD 1          WORD 2
001  00000000 00000000      00000000 00000000
002  00000000 00000001      00000000 00000000
003  00000000 00000000      00000000 00000000
004  00000000 00000000      00000000 00000000
005  00000000 00000000      00000000 00000000
006  00000000 00000000      00000000 00000000
DATA:  00000010 01010001
```


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```
                                BINARY DATA MONITOR
                                SEQUENCER OUTPUT
COUNTER ADDR:   200                 STEP:   001              SEQUENCER LENGTH:   006
                                    FILE:   400- 413
                    OUTPUT ADDR:    110                 201
                    DATA:   00000000 00000000   00000000 00000000
                    MASK ADDR:      070                 071
                    DATA:   00000010 01010001   00000000 00000000
                    STEP        WORD 1              WORD 2
                    001     00000010 00000000   00000000 00000000
                    002     00000010 00000001   00000000 00000000
                    003     00000010 00010001   00000000 00000000
                    004     00000010 00010001   00000000 00000000
                    005     00000010 01000001   00000000 00000000
                    006     00000010 00000000   00000000 00000000
                                DATA:   00000010 01010001
```

SHIFT

CANCEL COMMAND

To display your rung.

Sequencer Output

The Sequencer Output instruction transfers the values of the current sequencer step to a specified output word. Here are some characteristics of the sequencer output instruction.

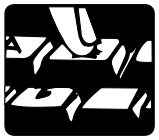
- You can transfer up to 64 bits.
- This instruction is programmed as an output instruction (can be programmed in the same rung as a sequencer input instruction).
- You can mask the unused output bits.
- The counter is internally indexed by the instruction (external counter instruction is not required).
- The instruction requires 5-8 words of your program.

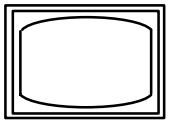
If the rung condition becomes:

True	The counter increments to the next step and transfers the data.
False	No action is taken.

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ATTENTION: The counter address for the Sequencer Output instruction should be reserved for that instruction. Do not manipulate the counter accumulated or preset values. Inadvertent changes to these values could result in hazardous machine operation or a RUN TIME ERROR. Damage to equipment and/or personal injury could result.

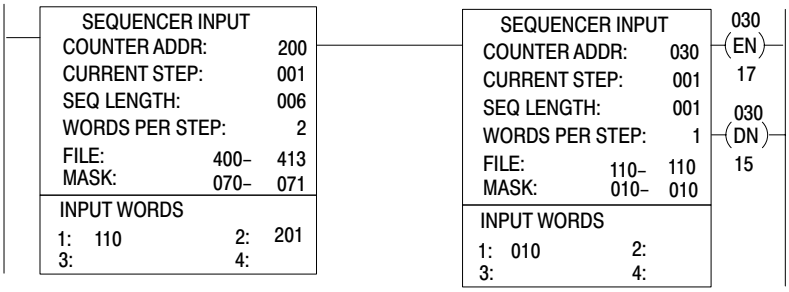




You are now ready to insert this instruction.

The word SEQUENCER appears in the lower left hand corner of the screen.

0



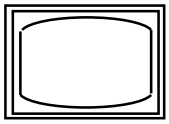
Notice that the words SEQUENCER OUTPUT are flashing, the cursor is on the first digit of the counter address, and the default values are shown.

Insert the following values. Your cursor will move automatically throughout the block instruction. The values are:

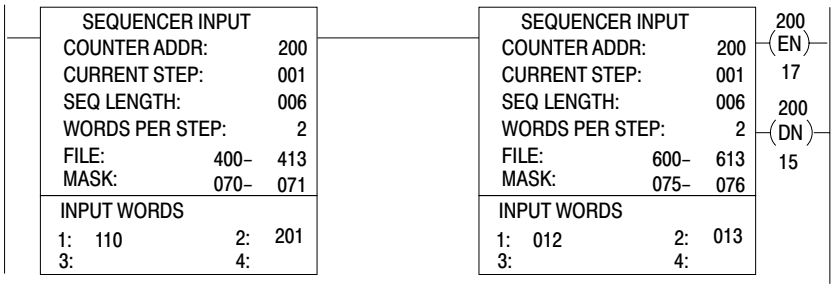
COUNTER ADDR:	200
CURRENT STEP:	001
SEQ LENGTH:	006
WORDS PER STEP:	2
FILE:	600
MASK:	075
OUTPUT WORDS:	1: 012
	2: 013

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Your sequencer output instruction should look like this:



To continue, enter your data using the binary data monitor mode. You will get your data from the worksheet in Figure 21.6. A filled-in block means that a 1 should be inserted in the corresponding bit location.

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Figure 21.6
Completed Sequencer Output Worksheet

ALLEN-BRADLEY
Programmable Controller
Sequencer Table Bit Assignments

PAGE 2 OF 2

PROJECT NAME Bottle Filling Applications PROCESSOR Mini-PLC-2/16

DESIGNER Engineer DATA TABLE ADDR _____ TO _____

SEQUENCER OUTPUT

COUNTER ADDR: 200 FILE 600 TO 613 SEQ LENGTH: 006

WORD ADDR: 012 013 _____ _____

MASK ADDR: 075 076 _____ _____

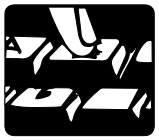
	WORD #1								WORD #2								WORD #3								WORD #4							
	17					10	07							00	17					10	07					00	17					10	07					00
DEVICE NAME		FTS	FTF	SOL		FTR	FTM	CMT	CM	Timer																										
MASK																																				
STEP																																				
1																																				
2																																				
3																																				
4																																				
5																																				
6																																				
FROM ADDR																																				
TO ADDR																																				

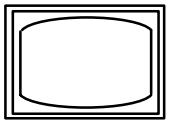
Note: A filled-in box means that each device is actuated

10148-I

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Start by positioning your cursor on the words SEQUENCER OUTPUT. Use the arrow keys to move the cursor.







The word DISPLAY appears in the lower left hand corner of the screen.

```
                                BINARY DATA MONITOR
                                SEQUENCER OUTPUT
COUNTER ADDR:   200                  STEP:   001                SEQUENCER LENGTH:   006
                                     FILE:   600- 613
                    OUTPUT ADDR:   012                  013
                    DATA:      00000000 00000000   00000000 00000000
                    MASK ADDR:     075                  076
                    DATA:      00000000 00000000   00000000 00000000
                    STEP       WORD 1              WORD 2
                    001    00000000 00000000   00000000 00000000
                    002    00000000 00000000   00000000 00000000
                    003    00000000 00000000   00000000 00000000
                    004    00000000 00000000   00000000 00000000
                    005    00000000 00000000   00000000 00000000
                    006    00000000 00000000   00000000 00000000
                                DATA:   00000000 00000000
```

0

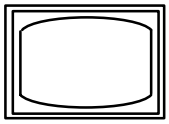
The cursor is on the last digit of DATA of the first word in the command buffer. The digits in step 1 for word 1 are intensified.

```
                                BINARY DATA MONITOR
                                SEQUENCER OUTPUT
COUNTER ADDR:   200                  STEP:   001                SEQUENCER LENGTH:   006
                                     FILE:   600- 613
                    OUTPUT ADDR:   012                  013
                    DATA:      00000000 00000000   00000000 00000000
                    MASK ADDR:     075                  076
                    DATA:      00000000 00000000   00000000 00000000
                    STEP       WORD 1              WORD 2
                    001    00000000 00000000   00000000 00000000
                    002    00000000 00000000   00000000 00000000
                    003    00000000 00000000   00000000 00000000
                    004    00000000 00000000   00000000 00000000
                    005    00000000 00000000   00000000 00000000
                    006    00000000 00000000   00000000 00000000
                                DATA:   00000000 00001010
```

00000000 00001010

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INSERT

```
                    BINARY DATA MONITOR
                    SEQUENCER OUTPUT
COUNTER ADDR:  200          STEP:  001          SEQUENCER LENGTH:  006
                            FILE:  600- 613
OUTPUT ADDR:  012                       013
DATA:  00000000 00000000    00000000 00000000
MASK ADDR:  075                         076
DATA:  00000000 00000000    00000000 00000000
STEP        WORD 1          WORD 2
001    00000000 00001010    00000000 00000000
002    00000000 00000000    00000000 00000000
003    00000000 00000000    00000000 00000000
004    00000000 00000000    00000000 00000000
005    00000000 00000000    00000000 00000000
006    00000000 00000000    00000000 00000000
DATA:  00000000 00001010
```

↓⇊

Data is inserted into Step 1 of Word 1. Cursor down one line.

The cursor is on the last digit of DATA of the second word in the command buffer. The digits in step 2 for word 2 are intensified.

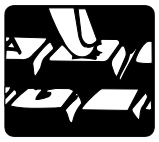
```
                    BINARY DATA MONITOR
                    SEQUENCER OUTPUT
COUNTER ADDR:  200          STEP:  001          SEQUENCER LENGTH:  006
                            FILE:  600- 613
OUTPUT ADDR:  012                       013
DATA:  00000000 00000000    00000000 00000000
MASK ADDR:  075                         076
DATA:  00000000 00000000    00000000 00000000
STEP        WORD 1          WORD 2
001    00000000 00001010    00000000 00000000
002    00000000 00000000    00000000 00000000
003    00000000 00000000    00000000 00000000
004    00000000 00000000    00000000 00000000
005    00000000 00000000    00000000 00000000
006    00000000 00000000    00000000 00000000
DATA:  00000000 00001010
```

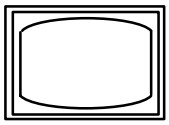
00000000 00001010

INSERT

```
                    BINARY DATA MONITOR
                    SEQUENCER OUTPUT
COUNTER ADDR:  200          STEP:  001          SEQUENCER LENGTH:  006
                            FILE:  600- 613
OUTPUT ADDR:  012                       013
DATA:  00000000 00000000    00000000 00000000
MASK ADDR:  075                         076
DATA:  00000000 00000000    00000000 00000000
STEP        WORD 1          WORD 2
001    00000000 00001010    00000000 00000000
002    00000000 00001010    00000000 00000000
003    00000000 00000000    00000000 00000000
004    00000000 00000000    00000000 00000000
005    00000000 00000000    00000000 00000000
006    00000000 00000000    00000000 00000000
DATA:  00000000 00001010
```


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↓⤓

Cursor down one line.

The cursor is on the last digit of DATA of the third word in the command buffer. The digits in step 3 for word 3 are intensified.

Continue adding your data:
003: 00001000 00100010
004: 00100000 00100010
005: 00000000 00100010
006: 00000010 00001010

To add data to WORD 2 press [Shift] [→] and cursor up or down as needed.

Do not press [Cancel Command]. We will use the display to add a mask.

DISPLAY

The word DISPLAY appears in the lower left corner of the Industrial Terminal Screen.

BINARY DATA MONITOR
SEQUENCER OUTPUT

COUNTER ADDR: 200 STEP: 001 SEQUENCER LENGTH: 006
FILE: 600– 613

OUTPUT ADDR: 012 013
DATA: 00000000 00000000 00000000 00000000
MASK ADDR: 075 076
DATA: 00000000 00000000 00000000 00000000

STEP	WORD 1	WORD 2
001	00000000 00001010	00000000 00000000
002	00000000 00001010	00000000 00000000
003	00001000 01000001	00000000 00000000
004	00000000 00010010	00000000 00000000
005	00000000 00100010	00000000 00000000
006	00000010 00001010	00000000 00000000

DATA: 00000000 00000000

000

The cursor is on the last digit OUTPUT ADDR(ess) of DATA in the command buffer. The digits for OUTPUT ADDR 012, DATA are intensified.

↓⤓

Cursor down one line.

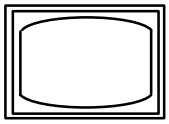
The digits for MASK ADDR 075. DATA are intensified.

00101010 10101010

The screen does not change.

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BINARY DATA MONITOR
SEQUENCER OUTPUT

COUNTER ADDR: 200 STEP: 001 SEQUENCER LENGTH: 006
FILE: 600– 613

OUTPUT ADDR: 012 013
DATA: 00000000 00000000 00000000 00000000

MASK ADDR: 075 076
DATA: 00101010 10101010 00000000 00000000

STEP	WORD 1	WORD 2
001	00000000 00001010	00000000 00000000
002	00000000 00001010	00000000 00000000
003	00001000 01000001	00000000 00000000
004	00100000 00010010	00000000 00000000
005	00000000 00100010	00000000 00000000
006	00000010 00001010	00000000 00000000

DATA: 00101010 10101010

INSERT

CANCEL COMMAND

To display your rung.

Sequencer Load

The Sequencer Load instruction places data into the sequencer file you established in the data table for this instruction. Here are some characteristics of the sequencer load instruction.

- This instruction is programmed as an output instruction.
- You cannot mask any unused bits.
- The counter is internally indexed by the instruction (external counter is not required).
- This instruction requires 4-7 words of the user program memory.
- A false-to-true rung transition enables the instruction.

When the rung becomes:

True	The instruction increments to the next step and loads the data.
False	No action is taken.

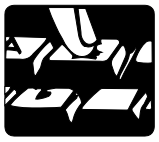
Use this instruction for:

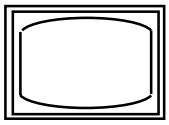
- Machine diagnostics – If the actual sequence of an operation becomes mismatched with the desired sequence of operation as contained in the sequencer input instruction, a fault signal can be enabled by the user program.
- Teach sequential operation – The I/O conditions representing the desired operation can be loaded into the sequencer input tables as the machine is manually stepped through the control cycle.

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ATTENTION: The counter address of the sequencer load instruction should be reserved for that instruction. Do not manipulate the counter accumulated or preset word. Changes to these values could result in unexpected machine operation with damage to equipment and injury to personnel.

You are now ready to program your sequencer load instruction.

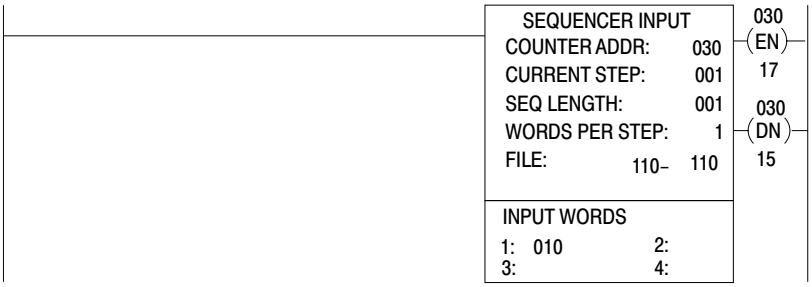




SEQ

2

The word SEQUENCER is displayed in the lower left corner of the screen.



Insert the following values. The cursor moves automatically throughout the Sequencer Load instruction. The values are:

COUNTER ADDRESS	056
CURRENT STEP	008
SEQ LENGTH	012
WORDS PER STEP	4
FILE	510
LOAD WORDS	1: 110
	2: 113
	3: 012
	4: 314

To continue, enter your data using the binary data monitor mode. You will get your data from the worksheet (Figure 21.7). A filled-in block means a 1 should be inserted in the corresponding bit location.

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Figure 21.7
Completed Sequencer Load Worksheet

ALLEN-BRADLEY
Programmable Controller
Sequencer Table Bit Assignments

PAGE _____ OF _____

PROJECT NAME Bottle Filling Applications PROCESSOR Mini-PLC-2/16

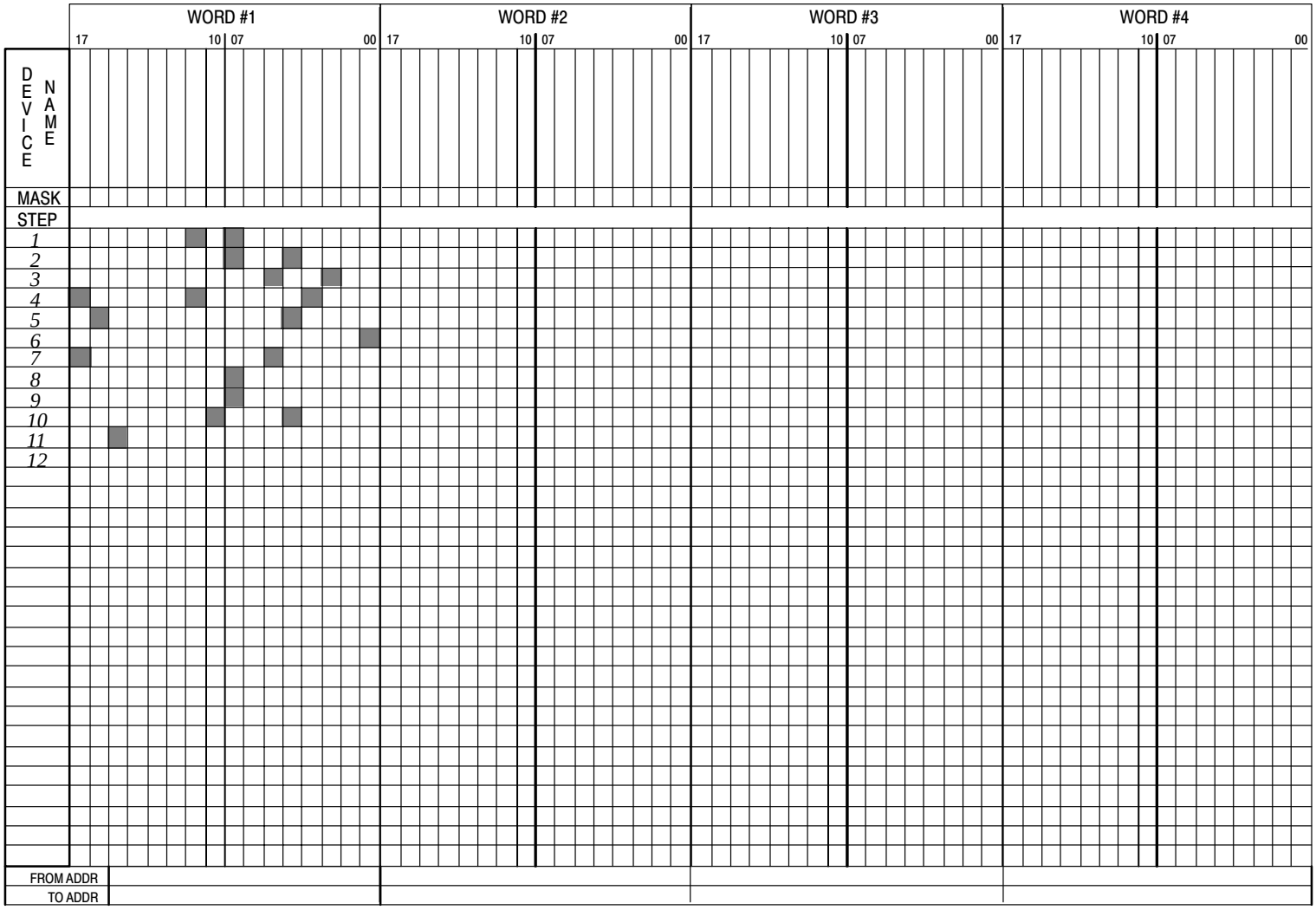
DESIGNER Engineer DATA TABLE ADDR _____ TO _____

SEQUENCER Load

COUNTER ADDR: 030 FILE 600 TO _____ SEQ LENGTH: 012

WORD ADDR: 110

MASK ADDR:

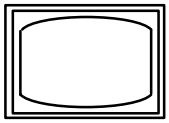


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Load your data from Figure 21.6 exactly as you did in the Sequence Input and Output instructions.







To display your rung.

Your Sequencer Load instruction should look like this.

BINARY DATA MONITOR
SEQUENCER OUTPUT

COUNTER ADDR: 056 STEP: 008 SEQUENCER LENGTH: 012

FILE: 510– 567

LOAD ADDR: 110
DATA: 00000000 00000000

STEP	WORD 1	
001	00000010	10000000
002	00000000	10001000
003	00000000	00100100
004	10000010	00001000
005	01000000	00010000
006	00000000	00000001
007	10000000	00100000
008	00000000	10000000
009	00000000	10000000
010	00000001	00010000
011	00100000	00000000
012	00000000	00000000

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Chapter 22

Selectable Timed Interrupt

Chapter Objectives

This chapter describes a method to execute subroutines at timed intervals. This method is called selectable timed interrupt (STI).

Introduction

A selectable timed interrupt is a special subroutine that can be programmed into the subroutine area and can be executed at timed intervals.

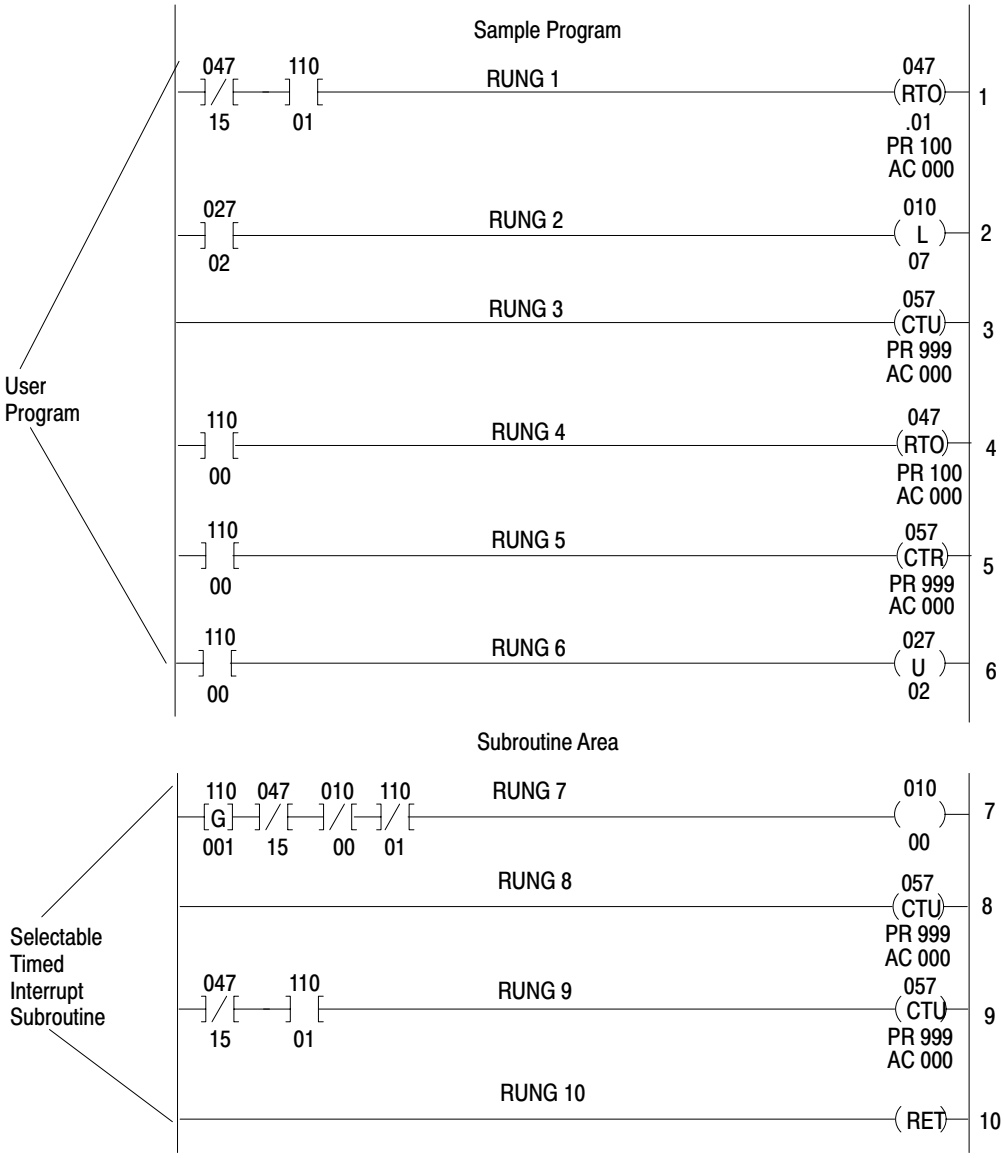
General programming facts are:

- The first instruction in the first rung of the subroutine area must be a Get instruction. This identifies it as an STI.
- The Get instruction must be used solely for the purpose of designating the time period of the STI.
- The STI subroutine execution time should not exceed approximately 2/3 STI interval.

Keystrokes: To program a selectable timed interrupt subroutine, a Get instruction must be the first instruction in the first rung after the use program subroutine area statement (Figure 22.1). This designates that an STI follows. Then, you can program your subroutine. The transition time from main program to STI and return is 100μs.

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Figure 22.1
Sample Program Rungs



ATTENTION: The Get instruction in the above example causes the subroutine to be scanned and the output to come on.

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The processor scans the user program (rungs 1-6) until it reaches the subroutine area. The processor then identifies the subroutine area as having an STI if:

1. The STI subroutine begins in the first rung of the subroutine area
2. The first instruction of the STI rung is a Get instruction



ATTENTION: The Get instruction must be used solely for the purpose of designating the time period of the STI. STI subroutine execution time should be limited to approximately 2/3 of the STI interval.

Selectable Timed Interrupt

The transition time from main program to STI and return is 50 microseconds.

The Get instruction must be used solely as the STI time base and can have any data table address (yyy) except a processor work area. Available time bases (xxx) are 1-999 milliseconds. Your program, through the use of a Get/Put instruction (see chapter 12) can be used to change the time base of the selectable timed interrupt. The STI subroutine must end with an unconditional Return instruction (rung 10 of Figure 22.1). The function is disabled if you enter zero as the time base in the Get instruction.

The Label instruction is optional and is only used when the main program wants to call the subroutine based on other conditions rather than selected time periods. If the subroutine timed interrupt is used as a direct subroutine with a Label instruction, you can have seven subroutines plus the STI. If the subroutine is not used as a direct subroutine, you can have eight subroutines plus the STI.

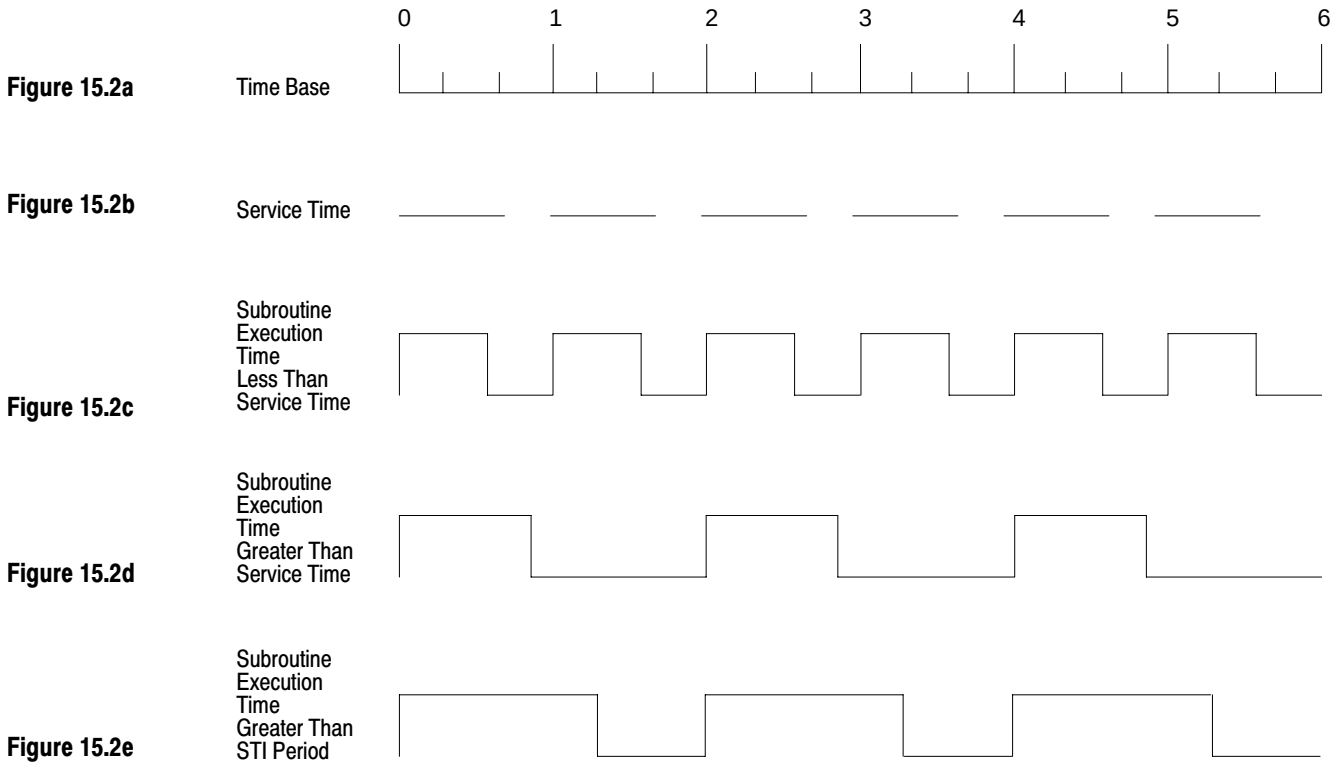
The STI is executed every time period once it has been enabled during the I/O scan. The program, or I/O scan, is interrupted when the STI subroutine is executed. The program returns to the point of interruption and continues execution just as if nothing has happened. However, during an I/O scan, if a block transfer is in process, the STI is not executed until the block transfer is completed. In addition, the STI is disabled during an insert/remove or a mode of operation change.

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Operational Overview

Service time (Figure 22.2b) is factory set at approximately 2/3 of the timed interrupt period. Your subroutine execution time plus program transition time (Figure 22.2c) should not exceed the maximum allowable service time (Figure 22.2b). When the program transition time plus subroutine execution time does not exceed service time, there is sufficient time for the processor to scan the subroutine.

Figure 22.2
Time Relationship of Subroutine Execution Time versus Service Time



Should the subroutine execution time plus program transition time exceed service time (Figure 22.2d), the selectable timed interrupt is no longer accurate. Two things happen:

- The STI too long bit (02702) is set. This bit is available for your use and can be used to initiate annunciators or other status indicators. The bit functions similar to a Latch instruction and must be reset with an Unlatch instruction.
- The processor completely executes the subroutine. It waits one full STI period before executing the subroutine again (Figures 22.2d and 22.2e).

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Chapter 23

Report Generation

Chapter Objectives

This chapter describes how to generate messages containing:

- ASCII characters
- graphic characters
- variable information

You can use the report generation function of the 1770-T3 industrial terminal to generate messages that contain ASCII and graphic characters, and variable data table information. The industrial terminal must be in the Mini-PLC-2/02, Mini-PLC-2/16, or Mini-PLC-2/17 mode. Messages are stored in the processor's memory after the END of program statement.

The 1770-T3 industrial terminal report generation features include:

- as many as 70 messages - you can choose the number of messages to be stored.
- simple programming - only 20 or 3 rungs of programming are required to display a message by program logic
- selectable communication rates - you can choose from seven communication rates: 110, 300, 600, 1200, 2400, 4800 or 9600 bits per second
- selectable parity bit - you can choose odd, even or no parity

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Report Generation Commands

Use the report generation commands (Table 23.A) to enter control words and to store, print, report, and delete messages and to display an index of existing messages.

Table 23.A
Report Generation Commands

Command	Key Sequence	Description
Enter report generation function	[RECORD][DISPLAY] Set baud rate (Message Code Keys)	Puts industrial terminal into report generation function. Same (entered from a peripheral device).
Message store	[M][S][,] (Message Number) [RETURN]	Stores message in processor memory. Use [ESC] to end message.
Message print	[M][P][,] (Message Number) [RETURN]	Prints message exactly as entered.
Message report	[M][R][,] (Message Number) [RETURN]	Prints message with current data table values or bit status.
Message delete	[M][D][,] (Message Number) [RETURN]	Removes message from processor memory.
Message index	[M][I][RETURN]	Lists messages used and the number of words in each message.
Automatic report generation.	[SEARCH][4][0] [M][R][RETURN]	Allows messages to be printed through program control.
Exit automatic report generation	[ESC] [CANCEL COMMAND] 1	Terminates automatic report generation.
Exit report	[ESC] [CANCEL COMMAND] 1	Returns to ladder diagram display. Terminates Report Generation Function.

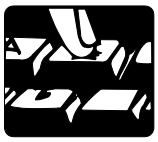
1 [CANCEL COMMAND] can only be used if the function was entered by a command from a peripheral device.

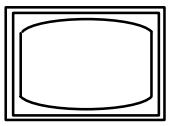
Message Control Word File – MS, 0

Bits from eight consecutive user-selected words control the 64 additional messages. The eight message control words are determined by establishing a 2-word message in the data table, called message 0. Store Message 0 by using the following keystrokes:

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You must be in report generation.





RECORD

These lines appear in the lower left hand corner of the screen.

CHANNEL C: 9600 BAUD; INPUT = ON; HANDSHAKE = ON
RECORD

The previous messages disappear. The following messages appear in the upper left hand corner of the screen.

DISPLAY

SWITCH TO ALPHANUMERIC OVERLAY

CONFIGURING MESSAGE AREA CONFIGURATION COMPLETE, PLEASE CONTINUE

MS,0 appears on the screen.

This prompt appears on the screen:

MS, 0

RETURN

MESSAGE CONTROL WORDS (ENTER 3 DIGIT WORD ADDRESS)
ADDRESS =

Enter the beginning word address of the message control word file. The industrial terminal calculates and displays the words in the message control word file. You can locate the message control word file in any unused data table area except processor work areas and input image table areas. If memory write protect is active, place the message control word file in the area of the data table which can be changed (010-177). Once you choose the start address, the industrial terminal displays a table (Table 23.B) which shows the message numbers associated with each message control word.

ESC

The display returns to the ladder diagram.

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Table 23.B
Example Message Control Word and Message Number Relationship

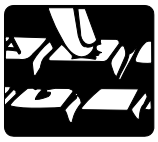
Control Words	Message Numbers
200	010-017
201	110-117
202	210-217
203	310-317
204	410-417
205	510-517
206	610-617
207	710-717

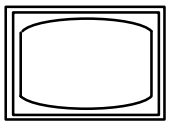
Important: This table assumes user selected messages control words begin at 200_8.

Message Store – MS

Accessible only in the Program or Remote Program mode, use this command to enter messages in memory. Access the message store command by:

You must be in report generation.





MS,nnn

MS,nnn appears on the screen.

nnn = message number

RETURN

A prompt READY FOR INPUT message is displayed. Any subsequent keys pressed then become part of the message. If you try to use a message number that already exists, the terminal displays MESSAGE ALREADY EXISTS.

ESC ESC

ESC

A prompt END OF MESSAGE STORE appears on the screen.

The display returns to the ladder diagram.

Each key you press, except [Shift], [Ctrl], [Esc], or [Rub Out] generates a code that is stored in one byte of memory. This includes ASCII and graphic characters as well as other keys such as [Rub Out] or [Esc].

You can enter messages which when reported give the current value of a data table word or byte. The messages can report the on or off status of a data table bit by using the delimiters shown in Table 23.C.

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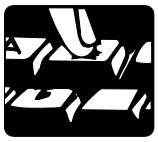
Table 23.C
Address Delimiters

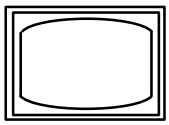
Delimiter Format	Explanation	Message Report Format
XXX	Enter 3-digit word address between delimiters.	Displays the 3-digit BCD value at assigned word address.
XXX1 or *XXX0*	Enter 3-digit word address and a “1” for upper byte or a “0” for lower byte between delimiters.	Displays the 3-digit octal value at assigned byte address.
XXXXX	Enter 5-digit bit address between delimiters.	Displays the On or Off status of the assigned bit address.
#XXX#	Enter 3, 4, or 5-digit word address between delimiters.	Displays the 3-digit BCD value at assigned word address.
!XXX!	Enter 3, 4, or 5-digit word address between delimiters.	Displays the 4-digit hex value at address.
&XXX1& &XXX0&	Enter 3, 4, or 5 digit word address and a “1”for upper byte or a “0” for lower byte between delimiters.	Displays the 3-digit octal value at the assigned byte address.
^XXXXX^	Enter 5, 6, or 7-digit bit address between delimiters.	Displays the On or Off status of the assigned bit address.

The desired delimiter is entered before and after the bit, byte, or word address. The delimiter tells the industrial terminal to print the current status or value of the bit, byte, or word at the address. You can enter as many consecutive addresses as needed by sharing the same delimiter, such as *XXX*XXX*XXX*.

As an example, suppose you want to report the on/off condition of a device SR6, during each cycle of machine operation. The delimiters denote the output address 013/05, and the cycle counter accumulated value (stored at 030). The desired message, “SR6 is (on or off) in cycle (xxx)”, is entered into memory with the following keystrokes:

You must be in report generation.





MS,n

MS,n appears on the screen.

n = message number

RETURN

READY FOR INPUT appears on the screen.

SR6 [space] IS [space] *01305* [space] IN [space] CYCLE [space] #030#

ESC ESC

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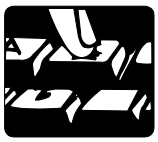
The words END OF MESSAGE STORE appear on the screen.

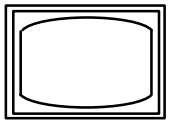
Returns the display to the ladder diagram.

Message Print – MP

Accessible in any mode, the message print command is to print the contents of a message to verify it. You can print a message with the following keystrokes:

You must be in report generation.





MP,n — MP,n appears on the screen.

n = message number

RETURN — Message n appears on the screen.

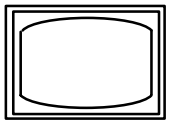
ESC — Returns the display to the ladder diagram.

The message print command is valid for message 0. It prints out message control word addresses in a form similar to that shown in table 23.A. If the location of the message control file is to be changed or you no longer need message 0, it can be deleted with the message delete command and re-entered at any time.

In the example, the message print command would give the following:

You must be in report generation.





MP,n — MP,n appears on the screen.

RETURN — SR6 IS *01305* IN CYCLE #030#

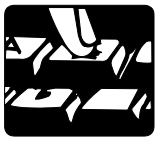
ESC — Returns the display to the ladder diagram.

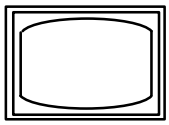
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Message Report – MR

Accessible in any mode, the message report command prints a message with the current data table value or bit status that corresponds to an address between the delimiters. For example, the message report command gives the following: bit 013/05 is off and counter 030 accumulated value is 000.

You must be in report generation.





MR,n — MR,n appears on the screen.

RETURN — n = message number

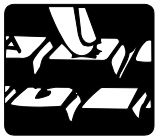
RETURN — SR6 IS OFF IN CYCLE 000

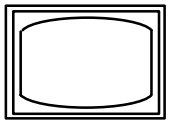
ESC — Returns the display to the ladder diagram.

Message Delete – MD

Accessible only in the Program or Remote Program mode, the message delete command is used to delete messages from memory. This command is accessed by:

You must be in report generation.





MD,n — MD,n appears on the screen

n = message number

RETURN — The prompt DELETION IN PROGRESS appears on the screen.

The message delete command cannot be terminated before completion. It terminates after the message has been cleared from memory and a MESSAGE DELETED prompt is printed.

ESC — The display returns to the ladder diagram.

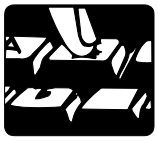
Important: Deleting MS,0 does not delete data in other stored messages.

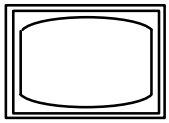
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Message Index – MI

Accessible in any mode, the message index command prints an MI list of the message numbers used and the amount of memory (in words) used for each message. In addition, the number of unused memory words available is listed. The message index command is accessed by the following keystrokes:

You must be in report generation.





MI

MI appears on the screen.

This command cannot be terminated before completion. It self-terminates after the list is completed.

ESC

The display returns to the ladder diagram.

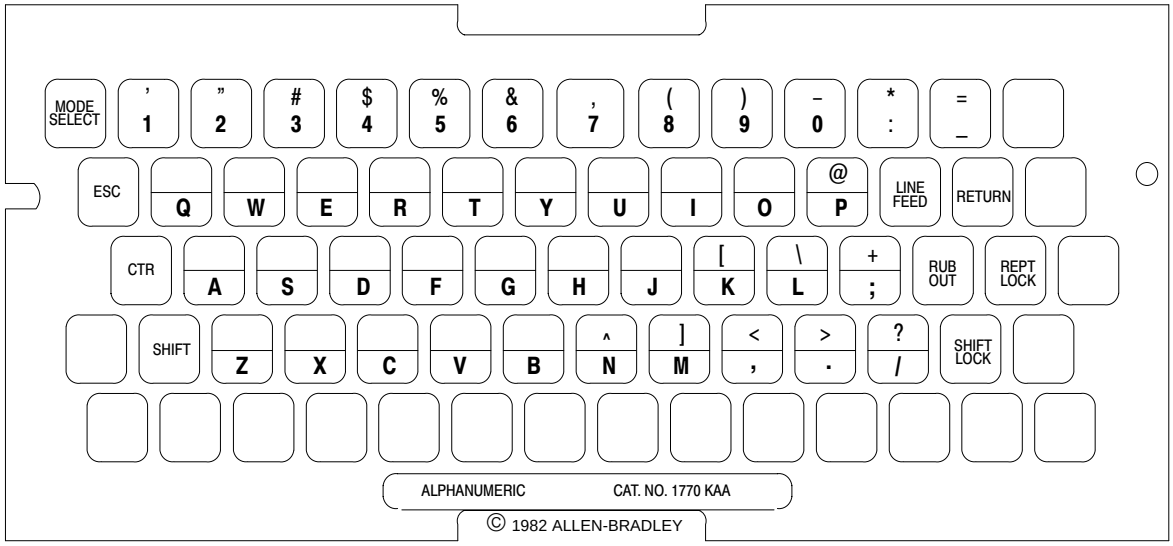
Entering a Message

Enter messages into memory from either the 1770-T3 industrial terminal or a peripheral device connected to channel C of the industrial terminal. Use one of two optional keytop overlays on the 1770-T3 industrial terminal, depending on whether graphic characters are desired (Figure 23.1):

- Alphanumeric Keytop Overlay (cat. no. 1770-KAA)
- Alphanumeric/Graphics Keytop Overlay (cat. no. 1770-KAB)

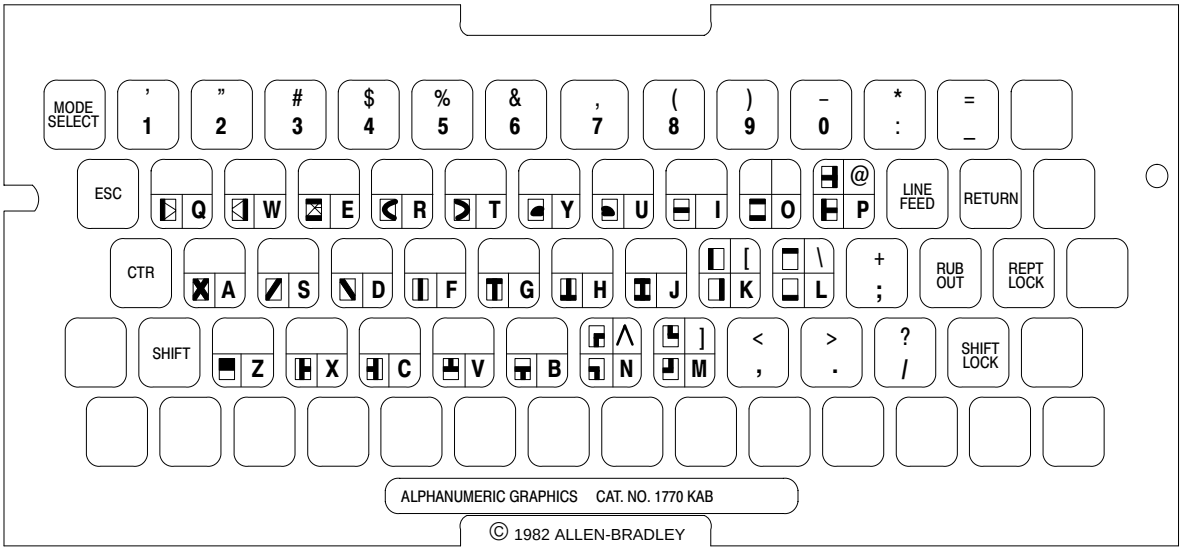
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Figure 23.1
Alphanumeric and Alphanumeric/Graphic Keytop Overlays



Alphanumeric Keytop Overlay (1770-KAA)

Alphanumeric/Graphic Keytop Overlay (1770-KAB)

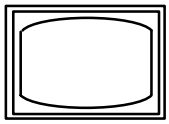


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If the processor is in the Program mode, you can enter a message by executing the following steps:





RECORD

These lines appear in the lower left hand corner of the screen.

CHANNEL C: 9600 BAUD; INPUT = ON; HANDSHAKE = ON
RECORD

The previous messages disappear. The following messages appear in the upper left hand corner of the screen.

DISPLAY

SWITCH TO ALPHANUMERIC OVERLAY

CONFIGURING MESSAGE AREA CONFIGURATION COMPLETE, PLEASE CONTINUE

At this point, change to the Alphanumeric Overlay (cat. no. 1770-KAA).

MS,n appears on a line underneath the previous message.

MS, n

The letter n represents the number of any message from 1-64.

The message READY FOR INPUT appears underneath the line MS,4.

RETURN

You may enter your alphanumeric message.

The message END OF MESSAGE STORE appears on the screen.

ESC ESC

You have exited message generation.

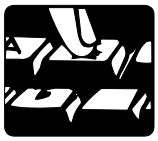
ESC

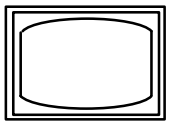
Messages are displayed on the 1770-T3 terminal or printed on a peripheral device manually using keystrokes each time a message is desired. Messages can also be activated by programming specific bits in the ladder diagram program.

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Manually Initiated Report Generation

You can display messages manually on the T3 terminal or the peripheral device by executing a key sequence each time a message is desired. You can display a message manually by executing the following steps:





RECORD

These lines appear in the lower left hand corner of the screen.

CHANNEL C: 9600 BAUD; INPUT = ON; HANDSHAKE = ON
RECORD

The following messages appear in the upper left hand corner of the screen.

DISPLAY

SWITCH TO ALPHANUMERIC OVERLAY

CONFIGURING MESSAGE AREA CONFIGURATION COMPLETE, PLEASE CONTINUE

At this point, change to the Alphanumeric Overlay (cat. no. 1770-KAA).

MR,n appears on the screen.

MR,n

The message n appears on the screen.

RETURN

You have exited message generation. Change to the PLC-2 Family overlay (cat. no. 1770-KCB).

ESC

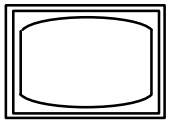
Automatic Report Generation

Once you have entered automatic report generation, your 1770-T3 terminal serves as a device that automatically displays messages as the program executes. These messages are displayed automatically through program control by energizing specific message request bits.

You can access automatic report generation if the processor is in the Run, Run/Program, Test, or Remote Test mode by performing the following keystrokes:

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ESC

40

The word SEARCH appears in the lower left hand corner of the screen.

The words AUTOMATIC REPORT GENERATION appear across the top of the screen and appear in the lower left hand corner of the screen. The word SEARCH changes to SEARCH 40.

CHANNEL C: 9600 BAUD; INPUT = ON; HANDSHAKE = ON RECORD

If your processor is in Program mode, the following message appears underneath the words AUTOMATIC REPORT GENERATION:

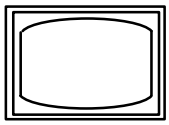
PROCESSOR NOT IN RUN OR TEST MODE.

Change modes and continue.

Press [Cancel Command] to exit report generation.

You can enter automatic report generation by another method if you have the Alphanumeric Key top overlay (cat. no. 1770-KAA) on the keytop and the processor is in the Run or Run/Program mode. The processor must also be in report generation. Perform the following steps:





MR

ESC

MR appears on the screen.

The words AUTOMATIC REPORT GENERATION appear across the top of the screen.

If your processor is in the Program mode, the following message appears underneath the words AUTOMATIC REPORT GENERATION:

PROCESSOR NOT IN RUN OR TEST MODE.

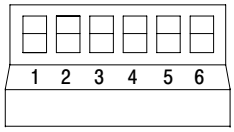
Change modes and continue.

Press [Esc] [Esc] to exit Automatic report generation

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Important: Automatic report generation can also be activated automatically upon initialization of the industrial terminal if you move parity switches 4 and 5 to the up position on the industrial terminal's main logic board (Figure 23.2). To find these switches, turn power off and remove the keyboard.

Figure 23.2
Parity Switch Locations



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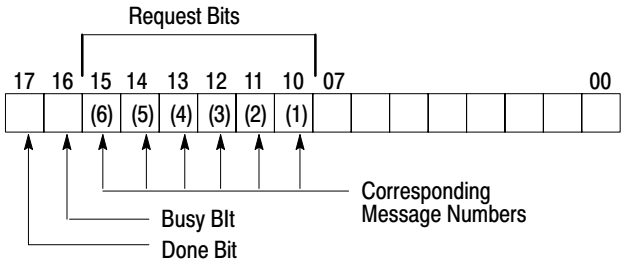
Once automatic report generation is activated, the message request bits are scanned by the industrial terminal for a false-to-true transition. Each time one of the request bits goes true, the corresponding message is printed automatically.

You can terminate automatic report generation by pressing [Esc]. The display returns to the ladder diagram if automatic report generation was entered by a command from a peripheral device.

Messages 1-6

Bits 10-15 of word 027 are used to control messages 1-6 (Figure 23.3). Bit 027/10 is the request message number 1, bit 027/11 is the request bit for message number 2 and so on. The remaining 64 messages have a user-defined file of message request bits for control. Bit 027/16, the busy bit is set when any of messages 1-6 are requested and remains set until all requested messages have been printed. Once all messages are printed, bit 027/17 stays on for 300 milliseconds and then resets.

Figure 23.3
Bit Assignments in Word 027

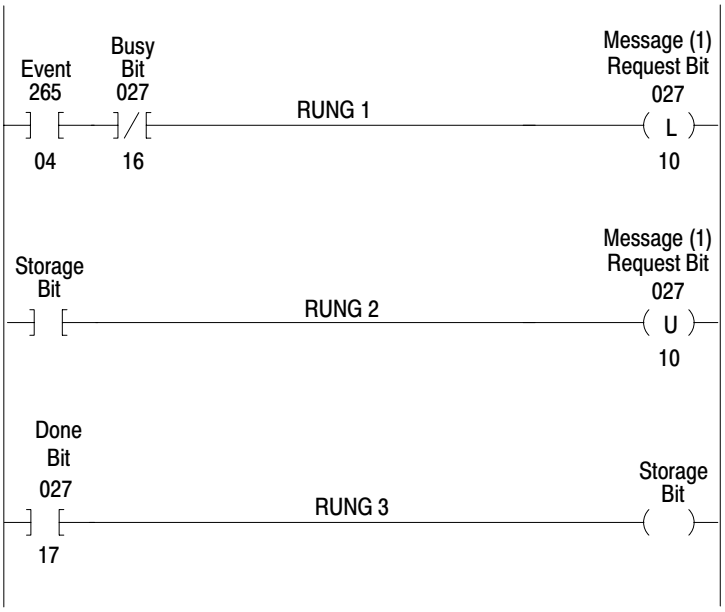


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You can display any of the six messages when the corresponding bit 10-15 of word 027 is latched on. An example program to display one of the messages 1-6 is shown in Figure 23.4. Three programming rungs are required to display each stored message. The rungs must be programmed in the order shown.

Figure 23.4
Example Program For Displaying Messages (1-6)



Additional Messages

The upper byte of each message control word contains the request bits for eight messages.

Figure 23.5
Bit Address and Message Number Relationship

Control Word Number	Control Word Address	Message Numbers
0	201	010–017
1	202	110–117
2	203	210–217
3	204	310–317
4	205	410–417
5	206	510–517
6	207	610–617
7	210	710–717

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You define the control word addresses that correspond to the control word number. The last three digits of the message request bit address are coded to represent a particular message. For example, message number 312 indicates the 12th bit of the 3rd control word. The message request bit address (follow the arrows in the figure above) is then 203/12. Likewise, message number 716 indicates the 16th bit of the 7th control word, with a message request bit of 207/16.

The message print command is valid for message 0. It prints out the message control word addresses in a form similar to that shown in Table 23.A. If the location of the message control file is to be changed or you no longer need message 0, it can be deleted with the message delete command and re-entered at any time.

Unlike messages 1-6, which share a common done bit (027/17), the additional 64 messages each have a separate done bit. After a particular message is printed, the done bit is set until the user program resets the request bit. Done bits are located in the lower byte of the message control words. Figure 23.6 shows this relationship. For example, if 204/15 is the request bit for a message, the done bit is located at 205/05, one byte below the request bit.

Figure 23.6
Extended Message Control Word

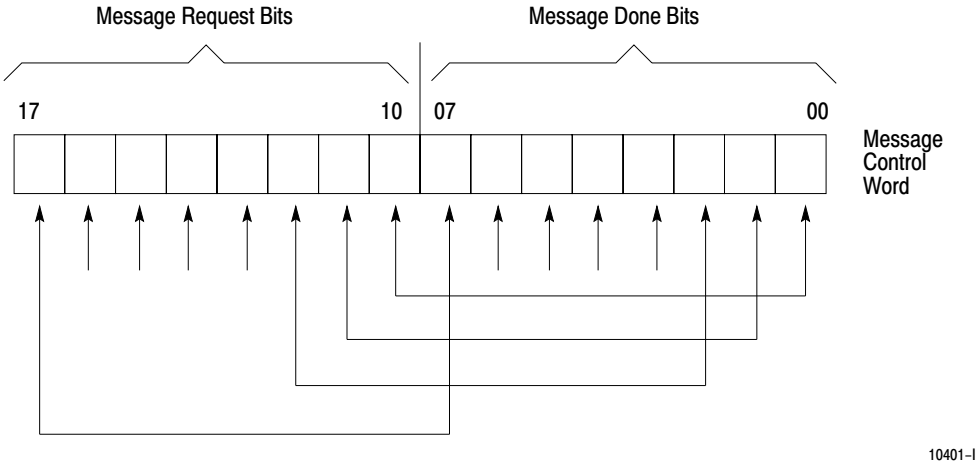
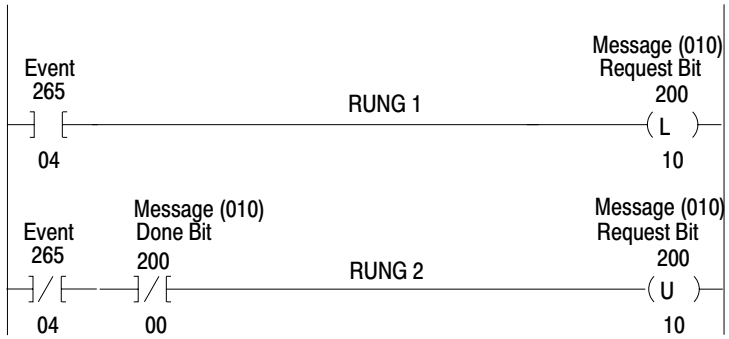


Figure 23.7 shows an example program that can be used to display each message.

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Figure 23.7
Example Program to Display Any of the Remaining 64 Messages



ATTENTION: Do not use message control words for any other purpose. This warning is especially critical for output image table locations when output or block transfer modules are placed in corresponding slots. Failure to observe this warning could result in hazardous or unexpected machine operation. This could damage equipment and injure personnel.

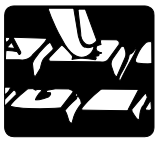
The message control word file can be located anywhere in the data table except in processor work areas and in the input image table. If Memory Write Protect is active, the message control word file must be placed in the area of the data table which can be changed (words 010-177).

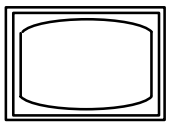
Graphic Programming

Several keys and special industrial terminal control codes are used to move through the display and perform a variety of functions (Table 23.D and Table 23.E).

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You can access graphic capability by executing the following keystrokes:





RECORD

These lines appear in the lower left hand corner of the screen.

CHANNEL C: 9600 BAUD; INPUT = ON; HANDSHAKE = ON
RECORD

The previous messages disappear. The following messages appear in the upper left hand corner of the screen.

DISPLAY

SWITCH TO ALPHANUMERIC OVERLAY CONFIGURING
MESSAGE AREA CONFIGURATION COMPLETE, PLEASE
CONTINUE

If your message will contain graphics, change to the Alphanumeric/Graphics Overlay (cat. no. 1770-KAB).

MS,n appears on a line underneath the previous message.

MR,n

The letter n represents the number of any message from 1-64.

The message READY FOR INPUT appears underneath the line MS,n.

RETURN

Turns on graphics capability.

CTRL | @ P | % 5 | _ G

You can enter your alphanumeric/graphic message.

Turns off graphics capability.

CTRL | @ P | $ 4 | _ G

The message END OF MESSAGE STORE appears on the screen.

ESC | ESC

You have exited message generation.

ESC

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Table 23.D
Alphanumeric/Graphic Key Definitions

Key	Function
[LINE FEED]	Moves the cursor down one line in the same column.
[RETURN]	Returns the cursor to the beginning of the next line.
[RUB OUT]	Deletes the last character or control code that was entered.
[REPT LOCK]	Allows the next character that is pressed to be repeated continuously until [REPT LOCK] is pressed again.
[SHIFT]	Allows the next key pressed to be a shift character.
[SHIFT LOCK]	Allows all subsequent keys pressed to be shift characters until [SHIFT] or [SHIFT LOCK] is pressed.
[CTRL]	Used as part of a key sequence to generate a control code.
[ESC]	Terminates the present function.
[MODE SELECT]	Terminates all functions and returns the mode select display to the screen.
Blank Yellow Keys	Space keys. Move the cursor one position to the right.

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Table 23.E
Industrial Terminal Control Codes

Control Code Key Sequence	Function
[CTRL][P] [Column #][;] [Line #][A]	Positions the cursor at the specified column and line number [CTRL][P][A] positions the cursor at the top left corner of the screen.
[CTRL][P][F]	Moves the cursor one space to the right.
[CTRL][P][U]	Moves the cursor one line up in the same column.
[CTRL][P][5][C]	Turns cursor on.
[CTRL][P][4][C]	Turns cursor off.
[CTRL][P][5][G]	Turns on graphics capability.
[CTRL][P][4][G]	Turns off graphics capability.
[CTRL][P][5][P]	Turns Channel C outputs on.
[CTRL][P][4][P]	Turns Channel C outputs off.
[CTRL][I]	Horizontal tab that moves the cursor to the next preset 8th position.
[CTRL][K]	Clears the screen from cursor position to end of screen and moves the cursor to the top left corner of the screen.
Key Sequence	**Attribute [1]**
[CTRL][P][0][T]	Attribute 0 = Normal Intensity
[CTRL][P][1][T]	Attribute 1 = Underline
[CTRL][P][2][T]	Attribute 2 = Intensify
[CTRL][P][3][T]	Attribute 3 = Blinking
[CTRL][P][4][T]	Attribute 4 = Reverse Video

[1] Any three attributes can be used at one time using the following key sequence: [CTRL][P][Attribute #][;][Attribute #][;][Attribute #][T]

In addition, standard ASCII control codes can be used with the industrial terminal (Table 23.F). These codes, although not displayed, can be interpreted and acted on by a peripheral device connected to channel C.

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Table 23.F
ASCII Control Codes

Control Code [1]	Display [2]	ASCII Mnemonic	Name
CTRL 0 [3]	N_U	NUL	NULL
CTRL A [3]	S_H	SOH	START OF HEADER
CTRL B [3]	S_X	STX	START OF TEXT
CTRL C [3]	E_X	ETX	END OF TEST
CTRL D	E_T	EOT	END OF TRANSMISSION
CTRL E	E_Q	ENQ	ENQUIRE
CTRL F	A_K	ACK	ACKNOWLEDGE
CTRL G	B_L	BEL	BELL
CTRL H	B_S	BS	BACKSPACE
CTRL I	H_T	HT	HORIZONTAL TAB
CTRL J	L_F	LF	LINE FEED
CTRL K	V_T	VT	VERTICAL TAB
CTRL L	F_F	FF	FORM FEED
CTRL M	C_R	CR	CARRIAGE RETURN
CTRL N	S_O	SO	SHIFT OUT
CTRL O	S_I	SI	SHIFT IN
CTRL P	D_L	DLE	DATA LINK ESCAPE
CTRL Q	D_1	DC1	DEVICE CONTROL 1
CTRL R	D_2	DC2	DEVICE CONTROL 2
CRTL S	D_3	DC3	DEVICE CONTROL 3
CTRL T	D_4	DC4	DEVICE CONTROL 4
CTRL U	N_K	NAK	NEGATIVE ACKNOWLEDGE
CTRL V	S_Y	SYN	SYNCHRONOUS IDLE
CTRL W	E_B	ETB	END OF TRANSMISSION BLOCK
CTRL X	C_N	CAN	CANCEL
CTRL Y	E_M	EM	END OF MEDIUM
CTRL Z	S_B	SUB	SUBSTITUTE
ESCAPE	E_C	ESC	ESCAPE
CTRL,	F_S	FS	FILE SEPARATOR
CTRL-	G_S	GS	GROUP SEPARATOR
CTRL.	R_S	RS	RECORD SEPARATOR
CTRL/	U_S	US	UNIT SEPARATOR
DELETE	D_T	DEL	DELETE

1 Some ASCII control codes are generated using non standard keystrokes.
2 Will be displayed when Control Code Display option is set ON in Alphanumeric mode, only. (Not in Report Generation mode).
3 Invalid key in Report Generation mode.

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The 1770-T3 industrial terminal screen size is 80 columns across by 24 lines down. An example sheet for graphic programs is shown in Figure 23.8 An example message using graphic and alphanumeric characters is shown in Figure 23.9.

Figure 23.8
Graphic Program Planning Sheet

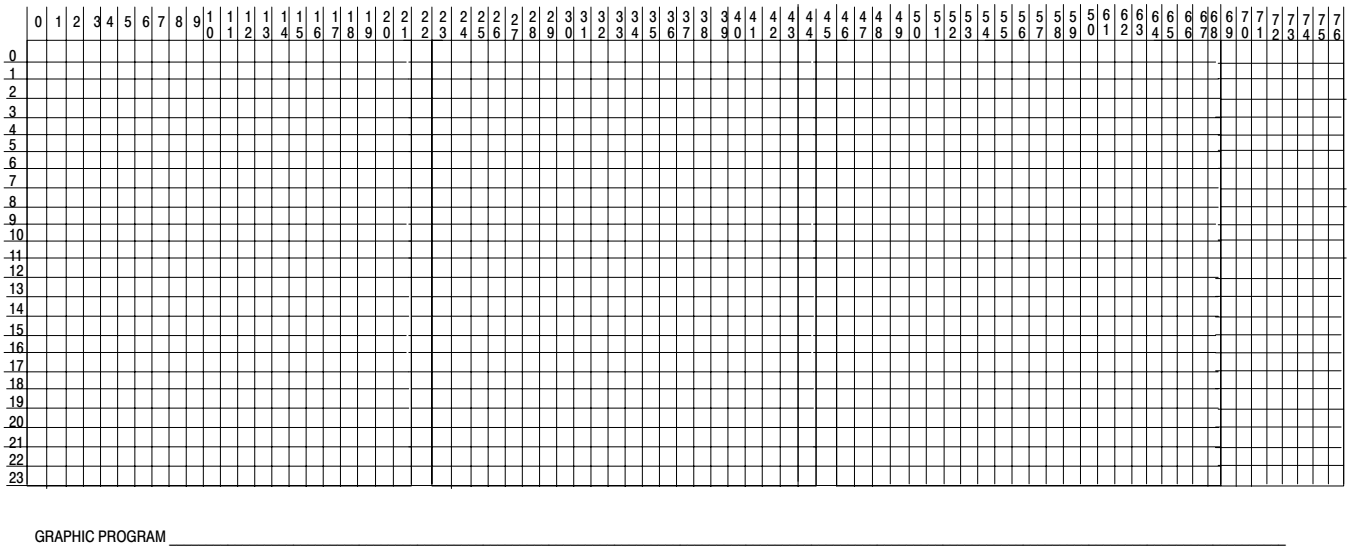
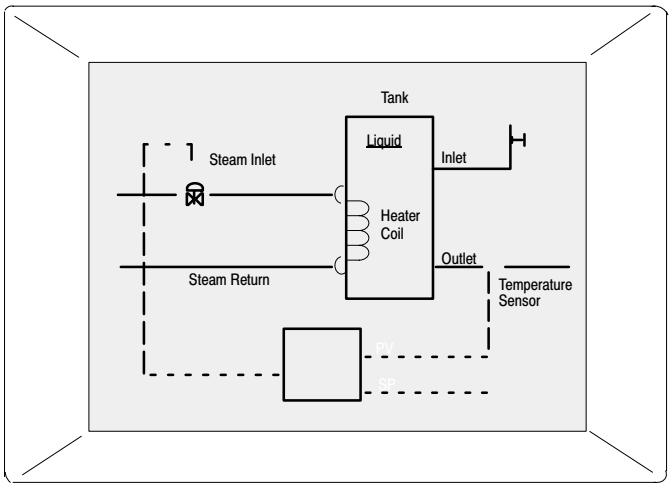


Figure 23.9
Example Graphic/ Alphanumeric Message



10261-I

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Use the control code, [CTRL] [P] <Column #>[;]<Line#>[A] for cursor positioning to conserve memory when possible. For example, [CTRL] [P] [3] [9] [;] [9] [A] uses 3 words of memory, storing CRTL P in one byte and remaining characters in one byte each. If the cursor had been at column 0, and line 0 and normal space, and line feed commands were used, it would have taken 24 words of memory to accomplish the same thing. The column and line numbers begin at zero rather than one.

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Chapter 24

Program Editing

Chapter Objectives

This chapter describes how to edit instructions in your program:

- rules for editing instructions
- editing relay-type instructions
- editing other instructions

Editing a Program

Changes to an existing program can be made through a variety of editing functions (Table 24.A). Instructions and rungs can be added or deleted; addresses, data, and bits can be changed.

If the memory write protect is active, you can change only data table values between word addresses 010 and 177.

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Table 24.A
Editing Functions [1]

Function	Key Sequence	Mode	Description
Insert a condition instruction	[INSERT] (instruction) (address) or [INSERT][⊢⊣] (instruction) (address)	Program	Position the cursor on the instruction that will precede the instruction to be inserted. Then press the key sequence. [1] [2] Position the cursor on the instruction that will follow the instruction to be inserted. Then press the key sequence. [1] [2]
Remove a condition instruction	[REMOVE] (instruction)	Program	Position the cursor on the instruction to be removed and press the key sequence. [1]
Insert a rung	[INSERT][RUNG]	Program	Position the cursor on the instruction in the preceding rung and press the key sequence. Enter instructions and complete the rung. [1]
Remove a rung	[REMOVE][RUNG]	Program	Position the cursor anywhere on the rung to be removed and press the key sequence. [1]
Change data of a word or block instruction	[INSERT][DATA]	Program	Position the cursor on the word or block instruction whose data is to be changed. Press the key sequence.
Change the address of a word or block instruction	[INSERT] (first digit) ⊢⊣ (Address)	Program	Position the cursor on a word or block instruction with data and press [Insert]. Enter the first digit of the first data value of the instruction. Then use the [ ] and [ ] key as needed to cursor up to the word address. Enter the appropriate digits of the word address.
Program on line	[SEARCH] 5 2		Initiates on–line programming.
Replace an instruction or change the address of an instruction without data	[Instruction] (Address)	Program	Position the cursor on the instruction to be replaced or whose address is to be Press the desired instruction key (or key sequence) and the required address(es).
Change data on line	[SEARCH] 5 1 (Data) [RECORD] [CANCEL COMMAND]	Run/Program	Position the cursor on the word or block instruction whose data is to be changed. Press the key sequence. Cursor keys can be used. Press [RECORD] to enter the new data into memory. To terminate on–line data change.
All editing functions	[CANCEL COMMAND]	Program Run/Program	Aborts the operation at the current cursor position. [1]

[1] These functions can also be used during on–line programming.

[2] When bit address exceeds 5 digits, press the [Expand Addr] key before entering address and enter a leading zero if necessary.

Important: Only addresses corresponding to Output Energize, Latch, and Unlatch instructions are cleared to 0.

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Inserting an Instruction

Only non-output instructions can be inserted in a rung. There are ways of doing this:

- First instruction of an existing rung
- First instruction of another rung
- Another location in the rung.

You insert an instruction using either of the two ways by performing the following steps.

First Instruction of an Existing Rung

1. Position the cursor of the first instruction of the existing rung.
2. Press [Insert][←].
3. Insert <instruction>.
4. Insert <address>.

First Instruction at the Beginning of Another Rung.

1. Position the cursor on the previous rung's output instruction.
2. Press [Insert].
3. Insert <instruction>.
4. Insert <address>.

If the cursor is on the END statement, the instruction is inserted before the END statement or subroutine area.

Another Location in the Rung

1. Position the cursor on the instruction immediately preceding your selected location.
2. Press the key sequence [Insert].
3. Press <instruction>.
4. Press <address>.

The new instruction is inserted after the cursor's present position.

You can enter bit addresses of 6 or 7 digits provided the data table is expanded to a 4- or 5-digit word address and you press [Expand Addr] before you enter the address.

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If, at any time, the memory is full, a MEMORY FULL message is displayed and you cannot enter more instructions.

Removing an Instruction

Only non-output instructions can be removed from a rung. Output instructions can be removed only be removing the complete rung.

Remove an instruction by performing the following steps.

1. Place the cursor on the instruction you are going to remove.

2. Press [Remove] <instruction>.

Bit values and data of word instructions are not cleared. The input image table bits are rewritten during the next I/O scan. If you press the wrong instruction, and INSTRUCTIONS DO NOT MATCH message is displayed.

Inserting a Rung

A rung can be inserted anywhere within a program. The cursor can be positioned on any instruction of a rung. The new rung is inserted after the rung which contains the cursor. The rung appears as an unconditional rung. You must complete the rung. You cannot edit instructions in the new rung until the rung is complete.

Insert a rung in a program by performing the following steps.

1. Press [Insert][Rung].

2. Insert <output instruction>.

3. Insert <output address>.

4. Press [Insert] <condition instruction>.

5. Insert <address>.

If the cursor is on the END statement, the rung need not be inserted. You can enter the rung as in initial program entry. if, at any time, the memory is full, a MEMORY FULL message is displayed you cannot enter more instructions.

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Removing a Rung

Removing a rung is the only way an output instruction can be removed. You can remove any rung, except the last one containing the END statement.

Remove a rung by performing the following steps.

1. Position the cursor anywhere on the rung you want to remove.

2. Press [Remove][Rung].

Only bits corresponding to Output Energize, Latch, or Unlatch instructions are cleared to zero. All other word and bit addresses are not cleared when a rung is removed.

Changing Data in a Word or Block Instruction

You can change the data of any word or block instruction, except Mathematics and Put instructions, in the program mode without removing and re-entering the instruction.

Change the data of any word or block instruction by performing the following steps.

1. Position the cursor on the appropriate word instruction.

2. Press [Insert] <data>.

When the last digit of the data is entered, the function is terminated and the data is entered into memory. Once you enter the first digit, you can use the [→][←] keys. The function can also be terminated and entered into memory before the last digit is entered if you press [Cancel Command].

Changing the Address of a Word or Block Instruction

You can change the address of a word or block instruction with data, excluding Mathematics and Put instructions, without removing and re-entering the instruction.

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Change the address of a word or block instruction by performing the following steps.

1. Position the cursor on the instruction you want to change.

2. Press [Insert].

The cursor, although not displayed, positions itself on the first data digit. Enter that digit to display the cursor.

3. Cursor back to the address digits using the [←] key.

4. Change <address> as needed. Use a leading zero if required.

Online Data Change

Certain data of a word or block instruction, excluding Mathematics and Put instructions, can be changed while the processor is in the Run/Program mode.

Change data while the processor is in the Run/Program mode by performing the following steps.

1. Position the cursor on the appropriate instruction.

2. Press [Search] 51.

The key sequence displays the message ON-LINE DATA CHANGE, ENTER DIGITS FOR: <Required information> near the bottom of the screen. The new digits are displayed in a command buffer as they are entered. After the new data is displayed:

3. Press [Insert] to enter the data into memory.

4. You can terminate this function by pressing [Cancel Command].



ATTENTION: When the address of an instruction whose data is to be changed duplicates the address of other instructions in the user program, this could cause unwanted machine motion. This could result in damage to the equipment and/or injury to personnel. The consequences of the change of each instruction should be thoroughly explored.

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Important: When the memory write protect is activated, online data change is not be allowed for addresses above 177. If you attempt to change data above address 177, the industrial terminal displays the error message MEMORY PROTECT ENABLED.

Search Functions

You can use the 1770-T3 terminal to search your program for:

- specific instruction and specific word addresses
- first condition or output instruction in a rung
- single rung display
- incomplete rung
- first and last rung and user boundaries
- remote mode select

See Table 24.B for a summary of search functions.

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Table 24.B
Search Functions

Function	Key Sequence	Mode	Description
Locate first rung of program	[SEARCH][↑]	Any	Positions cursor on the first instruction of the program.
Locate last rung of program area	[SEARCH][↓]	Any	Positions cursor on the temporary end instruction, subroutine area boundary, or the end statement depending on the cursor's location. Press key sequence again to move to the next boundary.
Locate first instruction of current rung	[SEARCH][←]	Remote Prog	Positions cursor on first instruction of the current rung.
Move cursor off screen	[SEARCH][←]	Remote Test Run/Program	Moves cursor off screen to left.
Locate output instruction of current rung	[SEARCH][→]	Any	Positions cursor on the output instruction of the current rung.
Locate rung without an output instruction	[SHIFT] [SEARCH]	Any	Locates any rung left incomplete due to an interruption in programming.
Locate specific instruction	[SEARCH] [Instruction key] (Address)	Any	Locates instruction searched for. Press [SEARCH] to locate the next occurrence of instruction.
Locate specific word address	[SEARCH] (address)	Any	Locates this address in the program (excluding -| |- and -| / |- instructions and addresses in files). Press [SEARCH] to locate the next occurrence of this address. 1
Single rung display	[SEARCH] [DISPLAY]	Any	Displays the first rung of a multiple rung display by itself. Press key sequence again to view multiple rungs.
Print	[SEARCH] [4][3]	Any	Prints a single rung.
Print	[SEARCH] [4][4]	Any	Prints a ladder diagram dump.
Print	[SEARCH] [4][5]	Remote Prog	Prints a total memory dump.
Print	[SEARCH] [5][0]	Any	Prints the first 20 lines of data table configuration.
Print	[SEARCH] [5][3]	Any	Prints the first 20 lines of bit manipulation.
Print	[SEARCH] [5][4]	Any	Prints the first 20 lines of memory layout display.
Program controls outputs	[SEARCH] [5][9][0]	Run/Program	Places the processor in run/program mode.
Program executes outputs disabled	[SEARCH] [5][9][1]	Remote Test	Places the processor in remote test mode.
Processor awaits commands	[SEARCH] [5][9][2]	Remote Program	Places the processor in remote program mode.

1 Enter leading zeros when bit address exceeds 5 digits or word address exceeds 3 digits.

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Searching for Specific Instructions and Specific Word Addresses

You can locate any instruction in your program by using methods described in this section. You can search for a block instruction searching for the counter address or the first entered address in the block.

You can locate any instruction in your program by performing the following steps.

1. Press [Search].

2. Insert <instruction>.

3. insert <address>. Enter leading zeros before the address if necessary.

Keystrokes: You can locate any address (excluding those associated with Examine On and Examine Off instructions and those contained within files) by performing the following steps.

1. Press [Search] 8.

2. Enter <address>.

The address you enter is the word address for the output instructions. The industrial terminal locates all uses of the word addresses associated with the word address except for -] [- and -]/[-.

Once either key sequence is pressed, this information and an EXECUTING SEARCH message is displayed near the bottom of the screen. The industrial terminal begins to search for the address and/or instruction from the cursor's position. It looks past the temporary end and subroutine area boundaries to the END statement. Then it continues searching from the beginning of the program to the point where the search began.

If found, the rung containing the first occurrence of the address and/or instruction is displayed as well as the rungs after it. If you press [Search] again, the next occurrence of the address and/or instruction is displayed. When it cannot be located or all addresses and/or instructions have been found, a NOT FOUND message is displayed.

If the instruction is found in the subroutine area or past the temporary end instruction, the area in which it is found is displayed in the lower portion of the screen.

This function can be terminated at any time by pressing [Cancel Command]. All other keys are ignored during the search.

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Searching for the First Condition or Output Instruction in a Rung

When the processor is operating in the Remote Program mode, you can access the first condition instruction of a rung from anywhere in the rung by performing the following steps.

1. Press [Search][←].

When the processor is not in the Program mode, the cursor moves off the screen to the left. To bring it back on the screen:

2. Press [→].

When the processor is operating in any mode, you can access the output instruction by performing the following step.

1. Press [Search][→].

Searching for a Single Rung

Single Rung Display
Upon power-up, a multiple rung display appears on the screen. You can select the single rung format by performing the following steps.

1. Press [Search][Display].

You can return to the multiple rung display.

2. Press [Search][Display] again.

Searching for an Incomplete Rung

You can locate an incomplete rung caused by an interruption in programming in any processor operating mode. Perform the following step.

1. Press [Shift][Search].

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Searching for the First and Last Rung and User Boundaries

You can locate the program boundaries including the first or last rung from any point in the program. Perform the following step.

1. Press [Search][↑] or [Search][↓].

The user program could contain a Temporary End instruction boundary and/or a subroutine area boundary. It always contains an END statement boundary.

When you press [Search][↑], the cursor goes directly to the first rung from anywhere in the program.

When you press [Search] [↓], the display goes to the next boundary in the direction indicated. By pressing the [SEARCH] [↓] key sequence again, a subsequent boundary is displayed until the program end statement is reached.

Boundaries are displayed at the top of the screen with subsequent program rungs displayed beneath. No rungs follow the END statement.

Clearing Memory

You can clear the data table, user program and messages using various clear memory functions. When memory write protect is active, the data table cannot be cleared except between and including addresses 010-177 (Table 24.C).

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Table 24.C
Clear Memory Functions

Function	Key Sequence	Mode	Description
Data table clear	[CLEAR MEMORY] [7][7] (Start Address) (End Address) [CLEAR MEMORY]	Remote Prog	Displays a start address and an end address field. Start and end word addresses determine boundaries for data table clearing. Clears the data table within and including addressed boundaries.
User program clear	[CLEAR MEMORY] [8][8]	Remote Prog	Position the cursor at the desired location in the program. Clears user program from the position of the cursor to the first boundary: i.e. temporary end, subroutine area or end statement. Does not clear data table or messages.
Partial memory clear	[CLEAR MEMORY] [9][9]	Remote Prog	Clears user program and messages from position of the cursor. Does not clear data table.
Total memory clear	[CLEAR MEMORY] [9][9]	Remote Prog	Position the cursor on the first instruction of the program. Clears user program and messages. Does not clear data table, unless the cursor is on the first program instruction.

IMPORTANT: When memory write protect is active, memory cannot be cleared except for data table addresses 010-177 with a programmed EEPROM installed.

Data Table Clear

You can clear all or part of the data table. Perform the following steps.

1. Press [Clear Memory] [7] [7].
2. Enter a start and end word address.
3. Press [Clear Memory].

The data table is cleared between and including these two word addresses. When memory write protect is active, the data table cannot be cleared except between and including addresses 010-177.

User Program Clear

You can clear all or part of the user program. Perform the following step.

1. Press [Clear Memory] [8] [8].

The user program is cleared from the cursor position to the first boundary: temporary end instruction, subroutine area or END statement. Neither the data table nor messages are cleared.

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Partial Memory Clear

You can clear part of the program and the messages. Perform the following step.

1. press [Clear Memory] [9] [9].

The user program and messages are cleared from the cursor position which can not be on the first instruction. None of the bits in the data table are cleared.

Total Memory Clear

You can clear the complete memory. Perform the following steps.

1. Position the cursor on the first instruction of the program.

2. Press [Clear Memory] [9] [9].

This resets all the data table bits to zero. Perform a total memory clear before entering the program.

Special Programming Aids

Special programming aids include:

- help directories
- online data change
- online programming
- online programming procedure
- data initialization key

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Help Directories

The 1770-T3 help directories list the functions or instructions common to a single multipurpose key such as the [Search] or [File] (Table 24.D).
A master help directory is also available which lists the eight function and instruction directories for the processors and the key sequence to access them. You can display the master help directory by pressing [Help]. You can press [Help] any time during a multi-key sequence. The remaining keys in the sequence can be pressed then without having to press [Cancel Command].

Table 24.D
Help Directories

Function	Key Sequence	Mode	Description
Help directory	[HELP]	Any	Displays a list of the keys that are used with the [HELP] key to obtain further directories.
Control function directory	[SEARCH] [HELP]	Any	Provides a list of all control functions that use the [SEARCH] key.
Record function directory	[RECORD] [HELP]	Any	Provides a list of functions that use the [RECORD] KEY.
Clear memory directory	[CLEAR MEMORY] [HELP]	Remote Prog	Provides a list of all functions that use the [CLEAR MEMORY] key.
Data monitor directory	[DISPLAY] [HELP]	Any	Provides the choice of data monitor display accessed by the [DISPLAY] key.
File instruction directory	[FILE] [HELP]	Any	Provides a list of all instructions that use the [FILE] key.
Sequencer instruction directory	[SEQ][HELP]	Any	Provides a list of all instructions that use the [SEQ] key.
Block transfer directory	[BLOCK XFER] [HELP]	Any	Provides a list of all instructions that use the [BLOCK XFER] key.
All directories	[CANCEL COMMAND]	Any	To terminate.

Important: If a particular function or instruction directory or an item in a directory is not available with the processor, the industrial terminal displays the message FUNCTION NOT AVAILABLE WITH THIS PROCESSOR.

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Online Programming

Online programming allows you to change the program during machine operation (processor is operating in the Run/Program mode and memory write protect is not active).



ATTENTION: Assign the task of online programming only to an experienced programmer who understands the nature of Allen-Bradley programmable controllers and the machinery being controlled. Check and re-check proposed online changes for accuracy. Assess all possible sequences of machine operation resulting from the change in advance. Be absolutely certain that the change must be done online and that the change solves the problem without introducing additional problems. Notify personnel in the machine area before changing machine operation online.

To minimize the chances of error, maintain accurate data table assignments sheets and use the data initialization key described in this section.

Online Programming Procedure

You can make the following changes to your program in the online programming mode:

- insert an instruction
- remove an instruction
- insert a rung
- remove a rung
- change an instruction or instruction address

The online programming mode is accessible from the industrial terminal by pressing the key sequence [Search] [5] [2]. The processor module must be in the run/program mode. The heading, ON-LINE PROGRAMMING appears in the top right-hand corner of the screen highlighted in reverse video.

You can not enter the following instructions during online programming:

- subroutine area
- temporary end
- MCR
- ZCL
- JMP
- JSR
- block transfer read and write

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The procedure for online programming in run/program mode is similar to the procedure for editing in program mode. However, the following three keys have a special purpose in online programming:

- [Record]
- [Cancel Command]
- [Data Init]

Use the [Record] key to enter a change to your program. Once pressed, the changed program is active.

Use the [Cancel Command] key to abort any online programming operation prior to pressing the [Record] key. Pressing [Cancel Command] restores the ladder diagram display and program logic to its original state prior to the online programming operation. You can also use it to terminate the online programming mode.

Data Initialization Key

The [Data Init] key performs two functions in the online programming mode:

- It allows entry of BCD data values (stored at the instruction address).
- It resets status bits.

Use the [Data Init] key when programming a data instruction whose address is not currently being used in the program. If you do not use [Data Init], data at the new address (possibly remaining from previous programming) may interfere with proper machine operation when you insert the new instruction into the program.



ATTENTION: When the address of a new instruction duplicates the address of other instructions in the program, the [Data Init] key should not be used without first assessing the consequences. Pressing the [Data Init] key zeros out the status bits stored at the existing instruction address. This may cause unwanted machine motion and result in equipment damage and/or injury to personnel.

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You must enter the data to be stored at the instruction's address and its operating parameters when programming the following instructions:

- Get
- Equal To
- Less Than
- Timers
- Counters
- Files
- Sequencers

The data stored at the instruction address is divided into two sections:

- BCD values (bits 00-13)
- status bits (bits 14-17)

During program execution,these bits are constantly changing to reflect current states and values of program instructions. Therefore, when programming on line, you must decide whether to use the current data or enter new data.

In summary, use [Data Init] to:

- enter a data instruction with an unused address
- enter new data
- clear the status bits of an already used address

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Chapter 25

Programming Techniques

Chapter Objectives

This chapter describes several programming techniques:

- one-shot programming
- re-start
- cascading timers
- temperature conversions
- program control

One-Shot Programming

The one-shot programming technique sets a bit for one program scan only. There are two types of one-shots:

- leading edge
- trailing edge

Leading Edge One Shot

A leading edge one-shot sets a bit for one scan when its input condition has made a false-to-true transition. The false-to-true transition represents the leading edge of the input pulse (Figure 25.1).

Figure 25.1
Leading Edge One Shot



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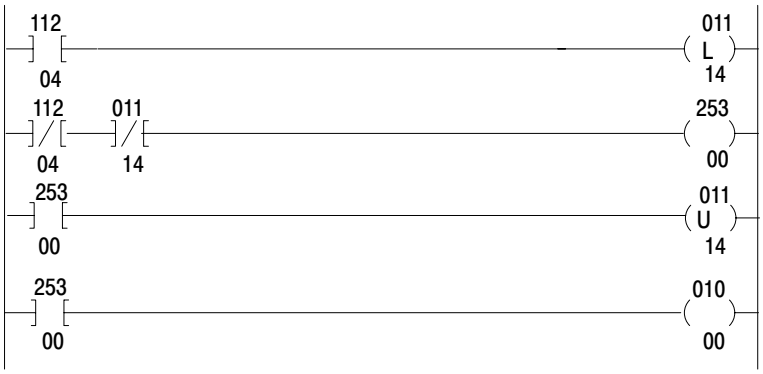
When bit 112/04 makes a false-to-true transition, the one-shot bit (bit 253/00) is set on for one scan. The length of time bit 112/04 remains on and does not affect the one-shot bit due to the next two rungs. Bit 011/14 is latched when bit 112/04 is set or bit 011/14 is unlatched when 112/04 is reset. Bit 010/00 is then energized because the one-shot bit (bit 253/00) is set for that scan.

During the next scan, either set of conditions prevents bit 253/00 from being set. The one-shot bit is set for another scan only when bit 112/04 makes a true-to-false and then a false-to-true transition.

Trailing Edge One Shot

A trailing edge one-shot sets a bit for one scan when its input condition has made a true-to-false transition. The true-to-false transition represents the trailing edge of the input pulse. Programming for a trailing edge one-shot is shown in Figure 25.2.

Figure 25.2
Trailing Edge One Shot



When bit 112/04 is set, bit 011/14 is latched. As soon as bit 112/04 makes a true-to-false transition, the one-shot bit (bit 253/00) is set and bit 011/14 is unlatched. Bit 253/00 remains on for only one scan and energizes bit 010/00.

The one-shot bit is set for another scan only when the input bit 112/04 makes a false-to-true transition then a true-to-false transition.

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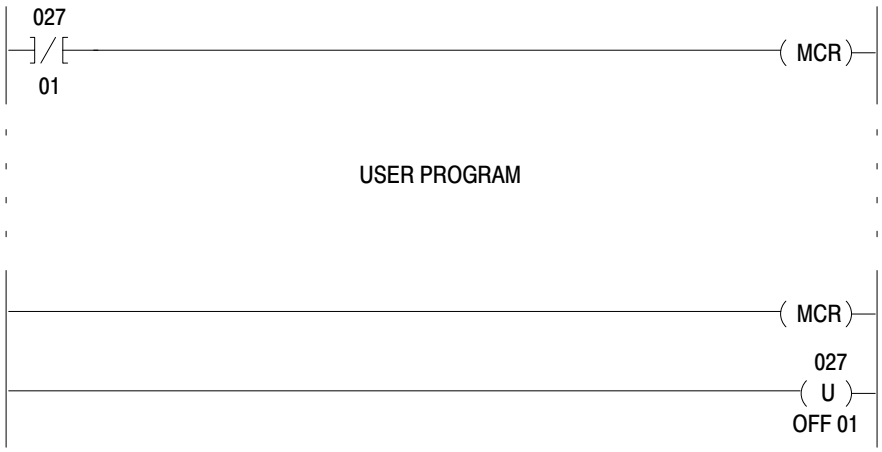
Restart

You may get into a situation that transfers the contents of the EEPROM into CMOS RAM memory. The data values (timers, counters and storage bits/words) that were present when the EEPROM was burned will also be transferred along with the ladder diagram.

You can use either one of two methods to inhibit operation:

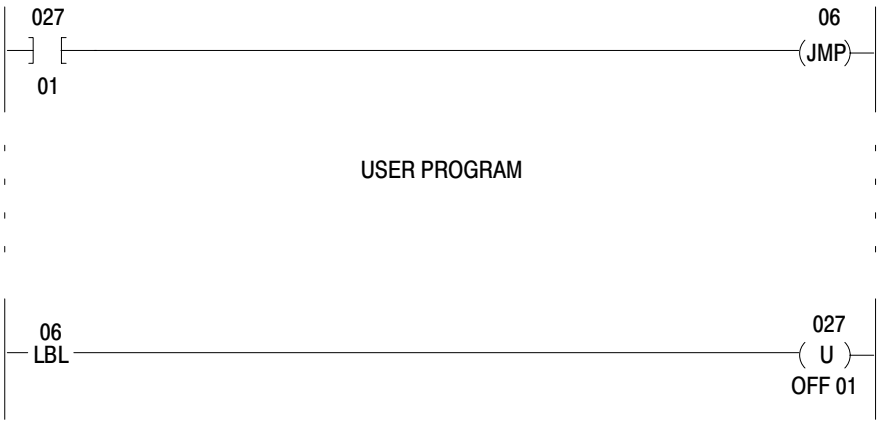
- MCR method - the processor is disabled for one scan before I/O update (Figure 25.3).

Figure 25.3
Automatic Restart Using an MCR Instruction



- JMP method - the program is jumped over once before I/O update (Figure 25.4).

Figure 25.4
Automatic Restart Using JMP Instruction



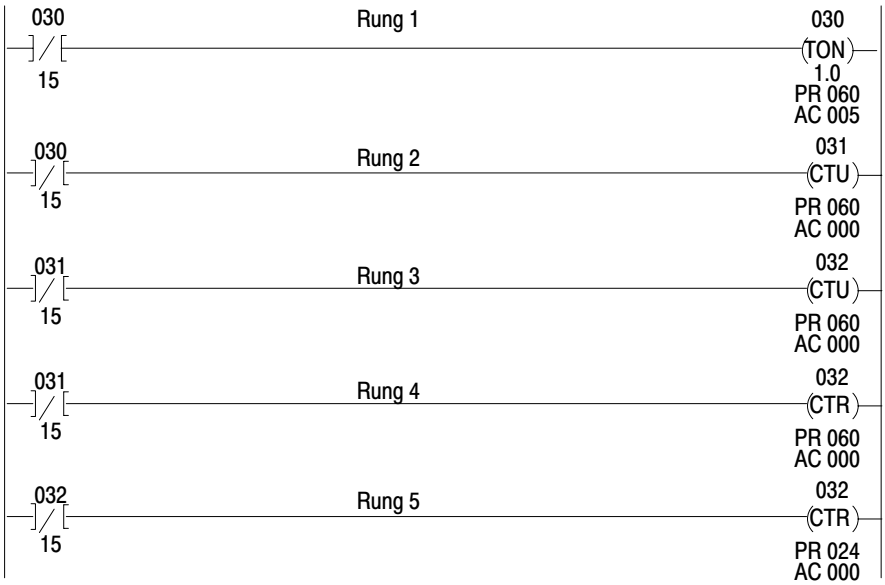
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The switch assembly on the I/O chassis determines how and when EEPROM to CMOS RAM transfer occurs. A transfer takes place if any change of CMOS RAM memory content occurs while the battery was being changed. If a transfer occurs (memory was altered), the data table contains the values programmed into the EEPROM. If transfer did not occur, memory did not change. The data table contains the values that existed at the time system power was removed.

Cascading Timers

Cascading is a programming technique that extends the ranges of timer and/or counter instructions beyond the maximum values that may be accumulated. A 24-hour clock program (Figure 25.5) is an example of cascading timers. Again, we emphasize not to enter these instructions using your online production equipment.

Figure 25.5
24-Hour Clock



ATTENTION: Do not use the clock program as a real time clock device. Failure to observe this caution may result in inaccurate program timing.

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Here is an explanation of each rung:

Rung 1: Free running timer. The timer done bit (030/15) is set for every 60 seconds or 1 minute intervals.

Rung 2: When AC = PR (accumulated value equals preset value) of the timer, counter 031 increments. This rung counts the minutes in an hour.

Rung 3: When AC=PR of counter 031, counter 032 increments. This rung counts the hours in a day.

Rung 4: When AC=PR of counter 031, 031/15 resets counter 031's accumulated value.

Rung 5: When AC = PR of counter 032, 032/15 resets counter 032's accumulated value.

Temperature Conversions

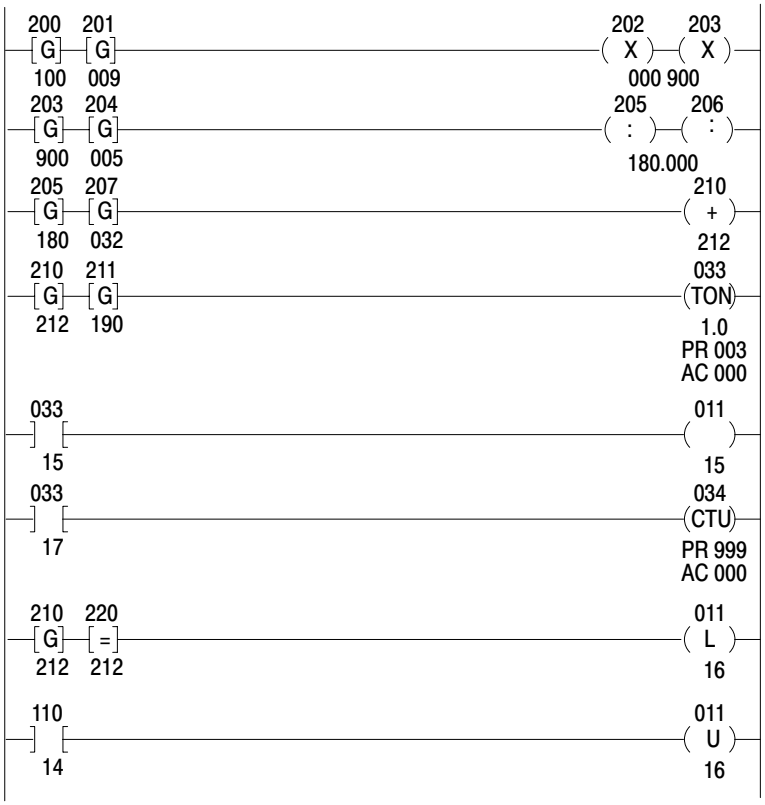
Do not use the following examples to program online production equipment. These examples are for demonstration purposes only.

Application One (ºC to ºF)

This application illustrates the conversion of temperature from degrees Celsius to degrees Fahrenheit (Figure 25.6).

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Figure 25.6
Converting Temperature Values



Suppose that you connected a thermocouple to an input module that measures Celsius temperature. A block transfer read transfers the temperature into the processor's data table.

For your ease, you would like to convert the recorded Celsius temperature in the data table to Fahrenheit values for display. This temperature must maintain certain range values for your application. You would like to:

- monitor the temperature from 87 to 100°C
- count the times the value falls below 190°F
- count the times the values stay at 212°F

Formula: $^{o}F = (9/5) \times {}^{o}(C) + 32$

In this example, the value read into the data table at address 200 is 100°C .

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Here is an explanation of each rung:

Rung 1: The Get instruction at address 201 multiplies the value of 100ºC by 9 and stores 900 at address 203.

Rung 2: The Get instruction at address 204 divides 5 into 900 and stores the quotient, 180, in address 205.

Rung 3: The Get instruction at address 207 adds 32 to the value 180 which is located at get addresses 205. The sum of 212 is stored at address 210. Thus 100ºC = 212ºF.

Rung 4: If the displayed temperature is less than 190ºF, the timer initiates timing for three seconds.

Rung 5: If three seconds have elapsed, an output at address 011/15 will energize a heating device which will bring the temperature back into the desired range.

Rung 6: Counter 034 counts the number of times the value falls below 190ºF. Therefore, when rung 4 is true the counter increments.

Rung 7: When the temperature equals 212ºF latching 011/16 enables an alarm.

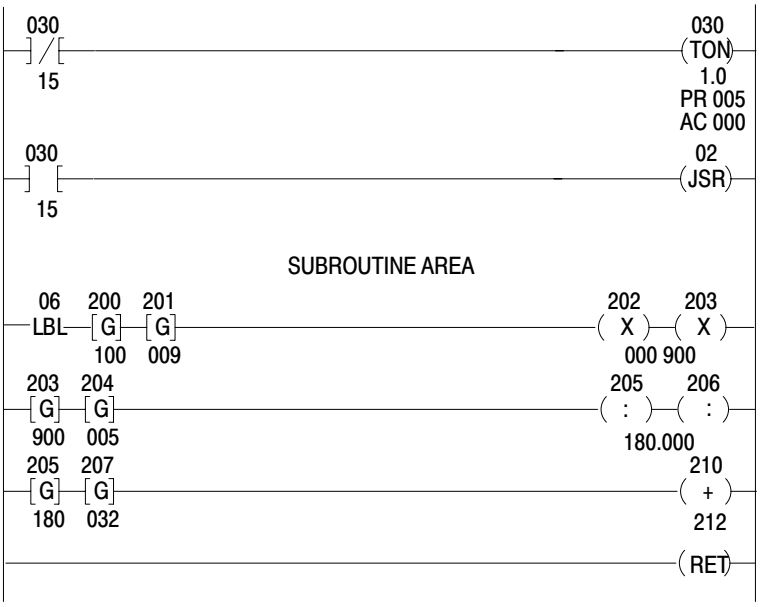
Rung 8: To shut the alarm off, unlatch 011/16. To do this, an operator would press a pushbutton connected to address 011/16.

Application Two (ºC to ºF Every Five Seconds)

This application is similar to application one, but we are only recording the converted temperature reading every five seconds (Figure 25.7).

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Figure 25.7
Recording Temperature Values Every 5 Seconds



Here is an explanation of each rung:

Rung 1: When rung 1 is true, the timer (this is an example of a free running timer) starts.

Rung 2: The JSR instruction jumps to the subroutine area label instruction when the timer's accumulated value reaches 5 seconds.

Rungs 3-5: Converts Celsius temperature to Fahrenheit temperature exactly as in application one.

Rung 6: The Return instruction signals the processor to return to the main program area.



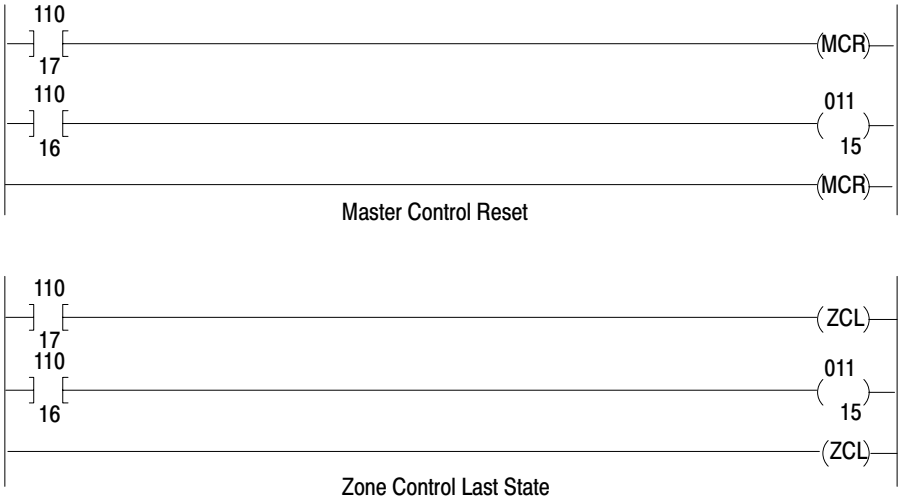
ATTENTION: You should make allowances for conditions which could be created by the use of the Jump To Subroutine instruction. The processor does not scan the subroutine program unless initiated by a Jump To Subroutine in the main program. Timers and counters within these rungs cease to function. You should reprogram critical rungs in the main program area.

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Program Control

This application illustrates the program control instructions, master control reset (MCR) and zone control last state (ZCL) (Figure 25.8).

Figure 25.8
Program Control



Before you program these two instructions, you must think about how you would want outputs to react when you change the process or operation.

Using the MCR instruction, rung logic shows:

- If bit 110/17 is false, then bit 011/15 is energized if 110/16 is set. This is normal operation.
- If bit 110/17 is true, then bit 011/15 is reset regardless of the state of 110/16. All outputs within an MCR zone are reset when the zone is disabled (start fence is false).

Using the ZCL instruction, rung logic shows:

- If bit 110/17 is false, then bit 011/15 is energized if 110/16 is set. This is normal operation.
- If address 110/17 is true, then bit 011/15 is left in its last state regardless of the state of 110/16. All outputs within a ZCL zone are left in their last state when the zone is disabled (start fence is false).

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Chapter 26

Program Troubleshooting

Chapter Objective

This chapter describes special troubleshooting technique:

- run time errors
- bit monitor/manipulation
- contract histogram
- force functions
- temporary end instruction
- ERR message for an illegal opcode

Run Time Errors

The processor and the 1770-T3 Industrial Terminal can diagnose certain errors that occur during the execution of your program.

What are Run Time Errors?

Run time errors are errors that occur while the processor executes your program, and are only apparent during this time. These errors result from improper programming techniques. For example, it is possible to program a series of instructions that the processor cannot properly perform. Or, it is possible to program paired instructions, such as a Jump/Label, with improper syntax.

If a run time error occurs and your processor is in the Run or Run/Program mode, the processor's green run LED goes out and it displays a run time error. The instruction with the illegal data is intensified on the industrial terminal screen, after re-entering the PLC-2 mode from the mode selection screen. The processor is automatically placed in the Remote Program mode. After you correct the program, change the mode select switch from Run or Run/Program to Program mode and then to Run or Run/Program mode. Or, you can cycle power in the Run mode to get the processor running again (if the processor's keyswitch is in the Run mode).

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Diagnosing a Run Time Error

The following steps help you diagnose run time errors:

1. Connect your industrial terminal to the processor.
2. Turn on the industrial terminal and notice the message, PLC-2 RUN-TIME ERROR. Press [1] [1] to continue. If the industrial terminal is already connected, then your ladder diagram is replaced by the display showing the run time error message on the mode selection screen.
3. Press [1] [1] to display the instruction that caused the error.
4. Correct the run time error by editing your program (Table 26.A).
5. Restart your processor.

Table 26.A
Possible Causes of Run Time Errors

Instruction	Cause
Jump	Jumping from the main program into the subroutine area or vice versa. Jumping backwards. Omitting the label instruction corresponding to the jump instruction. Jumping over a temporary end instruction.
Label	Multiple placement of the same label identification number. Removing a label instruction but leaving its reference, the jump or jump to subroutine instructions.
Jump to subroutine	To begin your main program. To jump forward in your main program. Use in the subroutine area. Omitting a return instruction. Omitting a corresponding label instruction. Jumping over a temporary end instruction.
Return	Processor does not find a return instruction from the subroutine area. Using a return instruction outside the subroutine area.
Files	AC>PR Duplicating counter's address. Manipulating the counter's accumulated value by means of external programming equipment or data highway hardware.
Sequencer	File address is out of range. Preset value equals 0.
Block transfer	Giving the module address a non-existent I/O rack number. Incorrect block length value.

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Bit Monitor/Manipulation

The bit monitor allows the status of all 16 bits of any data table word to be displayed. Bit manipulation allows data table bits to be selectively changed and is useful in setting initial conditions in the data of word instructions.

Bit Monitor Function

The bit monitor can function when the processor is operating in any mode. By pressing [Search] [5] [3] <word address>, the status of all 16 bits of the desired word is displayed. While the cursor is in the status field, you can use the [1] and [0] keys to change the addressed digit data/status values.

The status of the 16 bits in the next highest or next lowest word address can be displayed by pressing the [→] or [←] keys, respectively. Also, you can use bit monitor to force or display the status of force conditions.

Bit Manipulation Function

Bit manipulation can function when the processor is operating in the Program or Remote Program mode. When in Remote Test, or Run/Program mode, the program can override the bit status in the next scan.

Use [→] or [←] to cursor over to any bit. With the cursor on the desired bit, you can change its status by pressing [1] and [0].

To terminate this function, press [Cancel] [Command].



ATTENTION: If you need to change the status of any data table bit, be sure that the consequences of the change are thoroughly understood. If not, unpredictable machine operation could occur directly or indirectly as a result of changing the bit status. Damage to equipment and/or injury to personnel could result.

Contact Histogram

The contact histogram function displays the on or off history of a specific data table bit. You can monitor this function on the 1770-T3 Industrial Terminal. You can print it by a peripheral printer. If you use a peripheral device, set the baud rate for channel C of the Industrial Terminal to the baud rate of your printer.

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Data table bits, excluding those in the processor work area can be accessed by the contact histogram command. The on/off status of the bit and the length of time the bit remained on or off (in hours, minutes and seconds) is displayed on the Industrial Terminal. The seconds are displayed within 0.01 second (10 ms) resolution.

Two operating modes for the contact histogram shown in Table 26.B are:

Continuous: Accessed by pressing [Search] [6]. The user command displays the histogram from that instant.

Paged: Accessed by pressing [Search] [7]. The user command displays the histogram one page at a time and requires operator action to continue the histogram once the screen is filled.

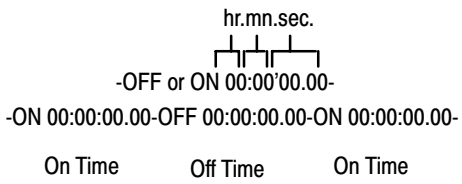
Table 26.B
Contact Histogram Functions

Function	Key Sequence	Mode	Description
Continuous contact histogram	[SEARCH][6] (Bit Address) [DISPLAY]	Any	Provides a continuous display of the on/off history of the addressed bit in hours, minutes and seconds. Can obtain a hardcopy printout of contact histogram by connecting a peripheral device to Channel C and selecting proper baud rate before indicated key sequence.
Paged Contact histogram	[SEARCH][7] (Bit Address) [DISPLAY]	Any	Displays 11 lines on/off history of the addressed bit in hours, minutes and seconds.
	[DISPLAY]		Displays the next 11 lines of contact histogram. Can obtain a hard copy printout of contact histogram by connecting peripheral device to Channel C and selecting proper baud rate.
Either	[CANCEL COMMAND]		To terminate.

After pressing [Search] [6] or [Search] [7], enter the bit address to be monitored. Bit addresses larger than 5 digits do not require leading zeros or the [Expand Addr] key. After pressing [Display] , the data of the histogram is displayed on every other line with 5 frames of data per line. Each frame of data contains the on/off status and the length of time in the format shown in Figure 26.1.

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Figure 26.1
Contact Histogram Display



If the bit is changing states faster than can be printed or displayed, a buffer stores these changes. If the buffer becomes full, all monitoring stops and a BUFFER FULL message is displayed. Subsequent changes in the on/off status of the device are lost until the histogram function finishes printing out or displaying the data in the buffer. Then a BUFFER RESET message is displayed and the histogram function resumes.

The industrial terminal screen can display up to 11 lines of data at one time. In the continuous mode, the screen automatically displays a new page of data when the screen is full.

In the paged mode, 11 lines fill the screen and the histogram stops. The buffer stores the subsequent changes until you press [Display] again. One page of data stored in the buffer is displayed. To terminate the contact histogram, press [Cancel Command].

Force Functions

You can use the force functions to selectively force an input bit or output bit on or off. The processor must be operating in the remote test or run/program mode.

The force functions determine the on/off status of input bits and output bits by overriding the I/O scan. You can force an input bit on or off regardless of the actual state of the corresponding input device. However, forcing an output terminal causes the corresponding output device to be on or off regardless of the rung logic or the status of the output image table bit.

When you attempt forcing, the processor I/O scan slows down to do the forcing. When forcing is terminated, the processor automatically switches back to the faster I/O scan mode.

When the processors is in the remote test mode, it holds outputs off regardless of attempts to force them on, even though the output bit instructions are intensified.

Bits may only be forced in the active input or output image tables. Enter [Search] [5] [0] to view the number of input/output racks available.

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Using a Force Function

You can use force functions in either of two ways using:

- bit manipulation/monitor display of an I/O word
- ladder diagram display of user program

By pressing [Search] [5] [3] <address>, the bit status and force status of the 16 corresponding input bits or output terminals of the desired word is displayed. use the [→] and [←] keys to cursor to the desired bit. Or, in the ladder diagram display, you can apply forcing by placing the cursor on an examine or energize instruction. In either case, after you position the cursor, you can use any one of the following key sequences for placing or removing a forced condition:

[Force On][Insert]
[Force Off][Insert]
[Force On][Remove]
[Force Off][Remove]

Removing a Force Function

You can remove all force on or all force off functions at once in ladder diagram display by pressing either of the following key sequences:

[Force On][Clear Memory]
[Force Off][Clear Memory]

The on/off status of a forced bit appears beneath the bit instruction in the rung.

In all operating modes, the Industrial Terminal displays a FORCED I/O message near the bottom of the screen when the processor forces the bits on or off. In every mode except the Program mode, the Industrial Terminal displays forced status “on” or “off” below each forced instruction.

Important: The industrial terminal displays the on/off status of Latch/Unlatch instructions below the instruction. However, the industrial terminal displays the status of Latch/Unlatch bits only in the Program/Remote Program mode.

All force functions are cleared when:

- you disconnect the industrial terminal from the processor
- the processor or industrial terminal loses ac power
- you press [Mode Select]

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ATTENTION: When an energized output is being forced off, keep personnel away from the machine area. Accidental removal of force functions instantly energizes the output device. Injury to personnel near the machine could result.

Forced Address Display

The industrial terminal displays a complete lists of bit addresses that are forced on or off by pressing:

[Search][Force On]
[Search][Force Off]

If all bits forced on or off cannot be displayed at one time, use the [Shift][←] and [Shift][→] keys to display additional forced bits.

Press [Cancel Command] to terminate this display.

Temporary End Instruction

You can use the Temporary End instruction to test or debug a program up to the point where it is inserted. The Temporary End instruction acts as a program boundary because instructions below it in user program are not scanned or operated upon. Instead, the processor immediately scans the I/O image table, then scans the user program from the first instruction to the Temporary End instruction.

When you insert the Temporary End instruction, the rungs below it, although visible and accessible, are not scanned. You can edit their content, if desired. The displayed section of user program made inactive by the Temporary End instruction contains the message INACTIVE AREA in the lower right-hand corner on the Industrial Terminal screen.

Inserting a Temporary End Instruction

Insert a Temporary End instruction in either of two ways:

First Method (Entering from the Remote Program or Program mode)

1. Cursor to the last rung of the main program to be kept active.
2. Position the cursor on the output instruction.
3. Press [Insert] [T. End].

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Second Method (Entering from the Remote Program or Program mode)

1. Cursor to the first rung of the main program to be made inactive.
2. Position the cursor on the first instruction in the rung.
3. Press [Insert] [←] [T. End].

Removing a Temporary End Instruction

Remove a Temporary End instruction by performing the following steps.

1. Position the cursor on the Temporary End instruction you are going to remove.
2. Press [Remove] [T. End].

Entering a Rung After a Temporary End Instruction

Enter a rung after a Temporary End instruction by performing the following steps.

1. Place the cursor on the Temporary End instruction.
2. Press [Rung].
3. Enter the new rung.

The industrial terminal prevents you from using the Temporary End instruction in any of the following ways, which would result in a run time error.

- Using more than one Temporary End instruction at a time.
- Using the Temporary End instruction in the subroutine area.
- Inserting or removing the instruction during online programming.
- Placing the instruction in the path of Jump or Jump To Subroutine instructions.

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Testing Your Program

This is the last phase of testing needed to help ensure proper start-up.



ATTENTION: Only trained personnel should conduct this test. Have a trained person at appropriate emergency stop switches to de-energize output devices that could cause hazardous operation.

To test your program do the following:

1. Connect the industrial terminal to your processor
2. Press [Search] [5] [9] [2] to select the Remote Program mode.
3. Enter your program.
4. Press [Search] [5] [9] [1] to select the Remote Test mode.
5. Examine your entered program. Make sure that no output device energizes unconditionally.
6. Connect an output module to a single device that causes machine motion.
7. Check the behavior of the connected output device. To do this, simulate the input conditions necessary to energize the output in the program while the processor is in the run/program mode of operation. Press [Search] [5] [9] [0].
8. Disconnect the output device.
9. Restore the connection from an output module to the next single output device to be tested.
10. Repeat steps 7-9 until you test all outputs.
11. Restore the connection from output modules to all devices causing machine motion. Restore power to any machine that you disconnected for start-up.
12. Perform a first run of your processor program with all output devices enabled.

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ERR Message for an Illegal Opcode

An illegal opcode is an instruction code that theprocessor does not recognize. It causes a run time error.

Important: The illegal opcode ERR message should not be confused with ERR messages caused when a 1770-T1 or 1770-T2 industrial terminal is connected to a processor that was using a 1770-T3 industrial terminal. These industrial terminal ERR messages do not contain the 4-digit hexadecimal value and will not cause the processor to fault.

If an illegal opcode occurs, compare the rung containing it to the equivalent rung in a hard copy printout of the program. You must either replace the error with its correct instruction or remove it. The ERR message caused by an illegal opcode cannot be removed directly. Instead, remove and replace the entire rung. You should identify and correct the cause of the problem and correct the ERR message.

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Appendix **A**

Specifications

	Mini-PLC-2/02 Processor without a power supply (1772-LZ)	**Mini-PLC-2/16 Processor** without a power supply (1772-LX)	**Mini-PLC-2/17 Processor** without a power supply (1772-LW)
Location	1771 I/O chassis left most slot		
Backplane Current	1.25 A Requirement		
Battery Back-up	Self-contained lithium battery maintains memory for 1 year with no AC applied to the processor		
Data Table Size	48-1920 Floating words	48-3968 Floating words	48-7808 Floating words
Memory Size 16-bit words RAM	2K	4K	7.75K
I/O Scan	0.82 ms (2-slot addressing) 2.00 ms (1-slot addressing) 2.15 ms (1/2-slot addressing)		
Program Scan	7.5 ms/K (minimum) 12 ms (typical application program)		
I/O Capacity (Typical) Bulletin 1771 I/O	128	256	256-512 (maximum)
Mode Selection	Key switch on the front panel and from the keyboard of the 1770-T3 terminal		
Environmental Conditions			
Operating Temperature	0 to 60° C (32 to 140° F)		
Storage Temperature	-40 to 85° C (-40 to 185° F)		
Relative Humidity	5% to 95% (without condensation)		
Keying (top connector)	Between 46 and 48 Between 54 and 56		

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	Mini-PLC-2/02 Processor with a power supply (1772-LZP)	**Mini-PLC-2/16 Processor** with a power supply (1772-LXP)	**Mini-PLC-2/17 Processor** with a power supply (1772-LWP)
	These processors have the same features as above and they also have a self-contained power supply		
Input Voltage	120/220 V ac (switch selectable)		
Input Voltage Range	97 to 132 V ac 194 to 264 V ac		
Nominal Input Power	96 VA		
Frequency	47 to 63 Hz		
Output Current to Backplane	4 A		
Keying (top connector)	Between 46 and 48 Between 54 and 56		

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Appendix **B**

Processor Comparison Chart

	Mini-PLC-2 LN3	Mini-PLC-2/15 LV	Mini-PLC-2/05 LS	Mini-PLC-2/05 LSP	Mini-PLC-2/02 LZ	Mini-PLC-2/02 LZP	Mini-PLC-2/16 LX	Mini-PLC-2/16 LXP	Mini-PLC-2/17 LW	Mini-PLC-2/17 LWP
Memory	1K	2K	3K	3K	2K	2K	4K	4K	7.75K	7.75K
I/O (Typical Maximum)	128	188	240	240	128	128	256	256	512	512
Keyswitch	•	•			•	•	•	•	•	•
Battery		•	•	•	•	•	•	•	•	•
EEPROM		•	•	•	•	•	•	•	•	•
I/O Power				2A		4A		4A		4A
Clock Calendar									•	•
Relay	•	•	•	•	•	•	•	•	•	•
TImer [1] Counter	40	488	488	488	488	488	488	488	488	488
Data Manipulation	•	•	•	•	•	•	•	•	•	•
Block Transfer	•	•	•	•	•	•	•	•	•	•
3-Digit Math		•	•	•	•	•	•	•	•	•
Program Control		•	•	•	•	•	•	•	•	•
Jump Subroutine		•	•	•	•	•	•	•	•	•
File Sequencer		•	•	•	•	•	•	•	•	•
6-Digit Math		AF1/4	•	•	•	•	•	•	•	•
Average Standard Deviation.		AF1/4							•	•
BCD-Binary Binary-BCD		AF1/4	•	•	•	•	•	•	•	•

[1] The **actual** number of counters can exceed 488 (because the number of counters is based on memory size). The **maximum** number of counters (using ALL available memory) is:

640	Mini-PLC-2/02
1280	Mini-PLC-2/16
2560	Mini-PLC-2/17

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	Mini-PLC-2 LN3	Mini-PLC-2/15 LV	Mini-PLC-2/05 LS	Mini-PLC-2/05 LSP	Mini-PLC-2/02 LZ	Mini-PLC-2/02 LZP	Mini-PLC-2/16 LX	Mini-PLC-2/16 LXP	Mini-PLC-2/17 LW	Mini-PLC-2/17 LWP
Natural Log Base 10 Log		AF4			Log(10)	Log(10)	Log(10)	Log(10)	•	•
Reciprocal Sin Cos Square Root		AF4	Sq Rt	Sq Rt	no recip	no recip	no recip	no recip	•	•
File Search Diagnostic		AF3								
STI			•	•	•	•	•	•	•	•
Bit Shift					•	•	•	•	•	•
FIFO Load/Unload					•	•	•	•	•	•
PID									•	•

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Appendix C

Number Systems

Objectives

This appendix describes the four numbering systems the processor uses:

- decimal
- octal
- binary
- hexadecimal

These numbering systems differ by their number sets and place values.

Decimal Numbering System

Timers, counters and math operations word values use the decimal numbering system. This is a numbering system made up of ten digits: the numbers 0 through 9 (Table C.A). All decimal numbers are composed of these digits. The value of a decimal number depends on the digits used and the place value of each digit.

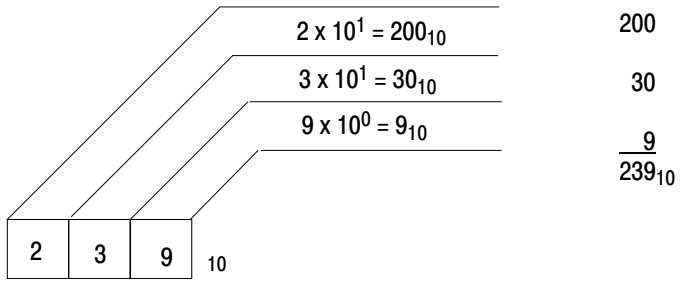
Table C.A
Numbering System Conversion Chart

Hexadecimal	Binary	Decimal	Octal
0	0000	0	000
1	0001	1	001
2	0010	2	002
3	0011	3	003
4	0100	4	004
5	0101	5	005
6	0110	6	006
7	0111	7	007
8	1000	8	010
9	1001	9	011
A	1010	10	012
B	1011	11	013
C	1100	12	014
D	1101	13	015
E	1110	14	016
F	1111	15	017

Each place value in a decimal number represents a power of ten starting with ten raised to the zero power (10^0=1) (Figure C.1). You can compute the decimal value of a number by multiplying each digit by its corresponding place value and adding these numbers together.

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Figure C.1
Decimal Numbering System



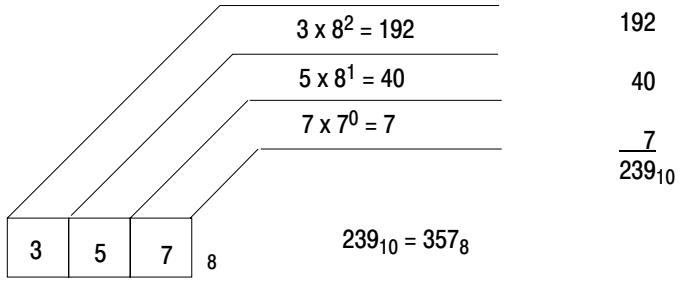
10404–I

Octal Numbering System

Byte word values use the octal numbering system. This is a numbering system made up eight digits: the numbers 0 through 7 (Table C.A). All octal numbers are composed of theses digits. The value of an octal number depends on the digits used and the place value of each digit.

Each place value in an octal number represents a power of eight starting with eight raised to the zero power (8^0=1) (Figure C.2). You can compute the decimal value of an octal number by multiplying each octal digit by its corresponding place value and adding these numbers together.

Figure C.2
Octal Numbering System



10404–I

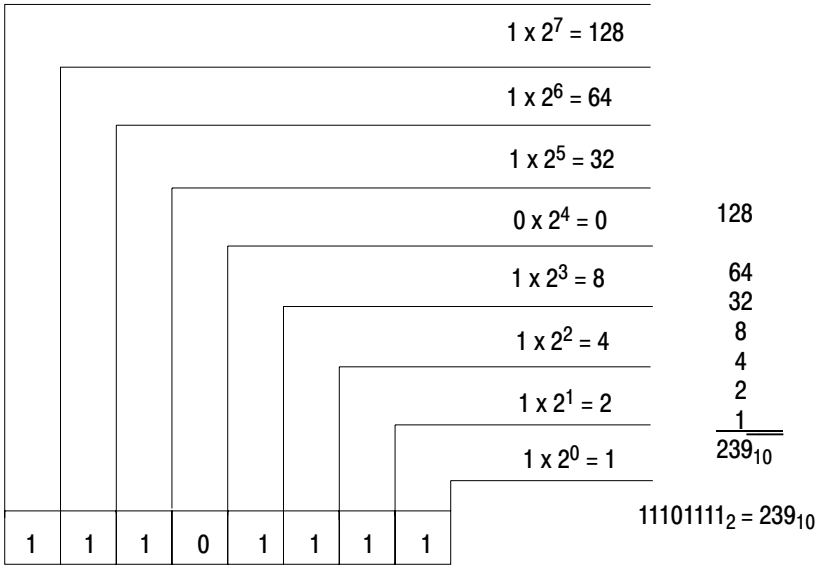
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Binary Numbering System

Binary numbering is used in all digital systems to store and manipulate data. This is a numbering system made up of two numbers: 0 and 1 (Table C.A). All binary numbers are composed of these digits. Information in memory is stored as an arrangement of 1 and 0. The value of binary number depends on the digits used and the place value of each digit.

Each place value in a binary number represents a power of two starting with two raised to the zero power (2^0=1) (Figure C.3). You can compute the decimal value of a binary number by multiplying each binary digit by its corresponding place value and adding these numbers together.

Figure C.3
Binary Numbering System



10406–I

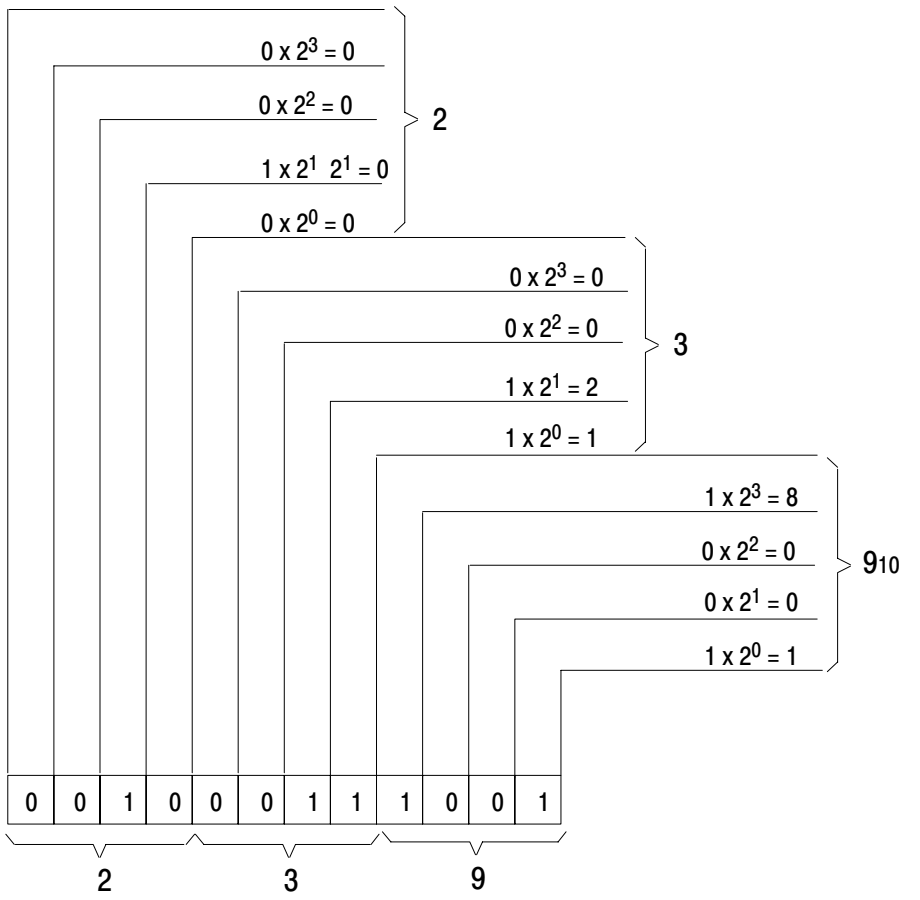
Binary Coded Decimal System

The binary coded decimal (BCD) format expresses a decimal value as an arrangement of binary digits. Each group of 4 binary digits is used to represent a decimal number from 0 to 9. All BCD numbers are composed of these digits. The value of BCD number depends on the digits used and the place value of these digits.

Each place value in a BCD number represents a power of two starting with two raised to the zero power (2^0=1) (Figure C.4). You can compute the decimal value of a binary number by multiplying each binary digit by its corresponding place value and adding these numbers together.

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Figure C.4
Binary Coded Decimal



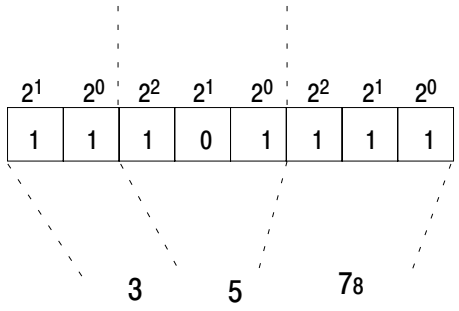
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Binary Coded Octal System

The binary coded octal (BCO) format expresses an octal value as an arrangement of binary digits (eight bits or one byte). The 8 bits are broken down into three groups: 2 bits, 3 bits, and 3 bits. The first group of binary digits is used to represent an octal number from 0 to 3; the other two groups represent an octal number from 0 to 7. All BCO numbers are composed of these digits.

Each place value in a BCO number represents a power of two starting with two raised to the zero power (2^0=1) (Figure C.5). You can compute the octal number for each group of bits by multiplying the binary digit by its corresponding place value and adding these numbers together.

Figure C.5
Binary Coded Octal



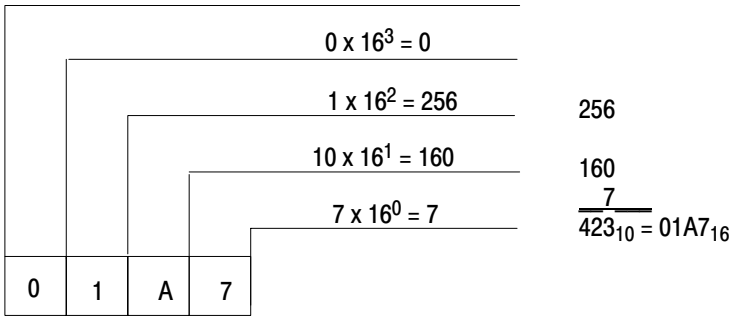
Hexadecimal Numbering System

Get and Put word values use the hexadecimal numbering system. This is a numbering system made up of 16 digits: the number 0-9 and the A-F. The letter A-F represent the decimal numbers 10-15, respectively. Four binary digits represent each hexadecimal character, you can convert from hexadecimal to binary by writing out the patterns for each hexadecimal character or group of four binary digits (Figure C.6).

Each place value in a hexadecimal character represents a power of 16 starting with 16 raised to the zero power (16^0=1) (Figure C.6). You can compute a decimal number for each group of hexadecimal characters by multiplying the decimal digit equivalent of each hexadecimal character by its corresponding place value and adding these number together.

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Figure C.6
Hexadecimal to Decimal Conversion



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Appendix D

Glossary

Introduction

To help build a common understanding of processor terminology, this glossary lists those terms and abbreviations used in this manual to describe and identify various Allen-Bradley processor system components and functions.

Each term in this glossary is concisely defined. These definitions provide a basis for understanding Allen-Bradley processors. In cases where a term may have more than one meaning, we give only those definitions directly related to our products.

When reading this glossary, you will notice that common electrical terms and symbols are not defined. We assume you have a working knowledge of basic electricity.

A

AC Input Module
An I/O module that converts various ac signals originating at user devices to the appropriate logic level signal for use within the processor.

AC Output Module
An I/O module that converts the logic level signal of the processor to a usable output signal to control a user ac device.

Accumulated Value
The number of elapsed timed intervals or counted events.

Address
(1) An alphanumeric value that uniquely identifies where data is stored.
(2) An alphanumeric value used to identify a specific I/O rack, module group, and terminal.

Ambient Temperature
The temperature of the air surrounding a module or system.

Analog
An expression of values which can vary continuously between specified limits.

Analog Input Module
A module that converts an analog input signal to a number that can be manipulated by the processor.

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Analog Output Module
A module that outputs a signal proportional to a number transferred to the module from the processor.

Arithmetic Capability
The ability to do addition, subtraction, multiplication, division, and other advanced math functions with the processor.

ASCII
American Standards Code for Information Interchange. It is a 7-bit code with an optional parity bit used to represent alphanumerics, punctuation marks, and control code characters.

Asynchronous
Recurrences or repeated operations that take place in patterns unrelated over time.

Asynchronous Shift Register
A shift register that is loaded and or unloaded based on external conditions and/or timing function.

Attribute
A means of flashing, underlining, and or blinking data on a display device.

B

Backplane
A printed circuit board, located in the back of a chassis, that contains a data bus, power bus, and mating connectors for modules to be inserted in the chassis.

Battery Backup
A battery or set of batteries that provides power to processor memory only in case of a system power outage.

Battery Low
A condition that exists when the backup battery voltage drops low enough to require battery replacement.

Baud
(1) A unit of data transmission speed equal to the number of code elements (bits per second). (2) A unit of signalling speed equal to the number of discrete conditions or signal events per second.

BCD
See Binary Coded Decimal.

Binary
A numbering system using only the digits 0 and 1. Also called base-2.

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Binary Coded Decimal (BCD)
A numbering system used to express individual decimal digits (0-9) in 4-bit binary notation.

Binary Word
A related group of ones and zeros that has meaning assigned by position, or by numerical value in the binary system of numbers.

Bit (Binary digit)
The smallest unit of information in the binary numbering system. Represented by the digits 0 and 1. The smallest division of a programmable controller word.

Bit Manipulation
The process of controlling data table bits (On or Off) through user instructions or keyboard entry.

Bit Rate
See Baud.

Bit Storage
A user-defined data table area in which bits can be set or reset without directly affecting or controlling output devices. However, any storage bit can be monitored as necessary in the user program.

Block
A group of words transmitted as a unit.

Block Length:
The total number of words transferred at one time.

Block Transfer:
A programming technique used to transfer as many as 64 words of data to, or form, an intelligent I/O module.

Branch
A parallel logic path within a rung.

Buffer
(1) In software terms, a register or group of registers used for temporary storage of data, to compensate for transmission rate differences between the transmitter and receiving device. (2) In hardware terms, an isolating circuit used to avoid the reaction of one circuit with another.

Burn
The process by which information is entered into PROM memory.

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Burn-In
The operation of a unit, at elevated temperatures, prior to its application with the objective of stabilizing its characteristics and detecting early failures.

Bus
(1) One or more conductors considered as a single identity that interconnect various parts of a system. For example, a data bus or address bus. (2) An electrical channel used to send or receive data.

Byte
Eight consecutive bits.

C

Cascading
(1) A programming technique that extends the ranges of timer and/or counter instructions beyond the maximum values that may be accumulated in a single instruction. (2) Using the output of a PID loop as a setpoint.

Central Processing Unit (CPU)
The circuits in a processor that control the interpretation and execution of the user program stored in processor memory.

Channel Timeout
The time a device allows between operations before terminating communication on a channel.

Character
One symbol of a set of symbols which normally include both alpha and numeric codes plus punctuation marks, and other symbols which may be read, stored, or written.

Chassis
A hardware assembly used to house devices such as I/O modules, adapter modules, processor modules, power supplies, and processor.

Clear
To return a memory to a non-programmed state; erased.

Clock
(1) A pulse generator which synchronizes the timing of various logic circuits. (2) Circuitry used to measure time.

Clock Rate
The speed (frequency) at which the processor operates, as determined by the time elapsed as words or bits are transferred through internal logic sequences.

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CMOS
Complementary Metal Oxide Semiconductor circuitry. See MOS.

Command
A function initiated by a user action.

Communication Rate
See Baud

Compatibility
(1) The ability of various specified units to replace one another, with little or no reduction in capability. (2) The ability of units to be interconnected and used without modification.

Complementary I/O:
An I/O technique that allows a processor to interface with input and output modules using a single physical address located in different I/O racks.

Computer Interface
A device designed for data communication between a processor and a computer.

Contact Histogram
A feature which allows a display (or printout) of the On and Off times for any selected data table bit.

Control
(1) A unit, such as a processor or relay panel, which operates an industrial application. (2) To cause a machine or process to function in a predetermined manner. (3) To energize or de-energize a processor output, or to set a data table bit to On or reset it to Off, by means of a program.

Control Panel
(1) A panel which may contain instruments or pushbutton switches. (2) In the Advisor system, a device which allows an operator to access and control plant operations through manipulation of the processor data table.

CPU
See Central Processing Unit.

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CRT Terminal
A terminal containing a cathode ray tub that displays user programs and information.

Cursor
(1) The intensified or blinking element in the user program or file display. (2) A means for indicating on a CRT screen where data entry or editing occurs.

Cycle
(1) A sequence of operations that is repeated regularly. (2) The time it takes for one such sequence to occur.

D

Data
A general term for any type of information.

Data Address
A location in memory where data can be stored.

Data Files
Groups of data values stored in the data table. These files are manipulated by the user program as required by the application.

Data Table
The part of processor memory that contains I/O values and files where data is monitored, manipulated, and changed for control purposes.

Data Terminal
(1) A device used only to send or receive data. (2) A peripheral device which can load, monitor, or dump processor memory data, including data table or data files. This also includes CRT devices and line printers.

Debugging
The process of detecting, locating, and correcting errors in hardware or software.

Decimal
Pertains to the base-10 numbering system.

Delimiter
A character that, when placed before and/or after a string of data, causes the data to be interrupted in a predetermined manner.

Diagnostic Command
Allows a computer to change or monitor the status of an interface module.

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Diagnostic Program
A user program designed to help isolate hardware malfunctions in the programmable controller and application equipment.

Diagnostics
Pertains to the detection and isolation of an error malfunction.

Digital
Information presented in a discrete number of codes.

Display
The image which appears on a CRT screen or on other image projection systems.

Documentation
An orderly collection of recorded hardware and software data such as tables, listings, and diagrams to provide reference information for processor application operation and maintenance.

Download
The process of transferring data from a bulk storage area to a memory with limited capacity.

Dump
To generate a copy of all or part of the processor memory contents through a data terminal.

Duplicate I/O
A method of expanding the number of I/O using the same location addresses.

E

EAF
Execute Auxiliary Function

EEPROM
Electrically Erasable PROM. A type of PROM that is programmed and erased by electrical pulses.

Edit
To deliberately modify a program.

Element
A display of a program instruction.

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Environment
In a systems context, the environment is anything that is not a part of the system itself. Knowledge about the environment is important because of the effect it can have on the system or because of possible interactions between the system and the environment.

EPROM
Erasable Programmable Read Only Memory. A PROM that can be erased with ultraviolet light, then reprogrammed with electrical pulses.

ERR
See Error Message.

Error Message (ERR)
The response to an opcode the industrial terminal cannot interpret.

Execution
The performance of a specific operation that is accomplished through processing one instruction, a series of instructions, or a complete program.

Execution Time
The total time required for the execution of one specific operation.

F

False
As related to processor instructions, a reset logic state.

Fault
Any malfunction which interferes with normal application operation.

Fault Zone
An area in the program which alters the operation portion of the application if a rack fault occur. Each fault zone is delimited by fence code.

Feedback
The signal or data transmitted to the processor from a controlled machine or process to denote its response to the command signal.

Fence Codes
Special program instructions which control and delimit specific program areas such as fault zones.

FIFO
See First-In-First-Out.

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File
(1) One or more data table words used to store related data. See File Organization. (2) A collection of related records treated as a unit. The records are organized or ordered on the basis of some common factor called a key. Records may be fixed or vary in length and can be stored in different devices and storage media.

File Address
The data table address of a file that determines to where, or from where, data will be transferred or moved.

File Creation
Establishing or writing records for a file into some storage device to provide later access by the processor or operator.

File Maintenance
(1) Adding, deleting, or changing the contents of records in a file. (2) Reorganizing the structure of a file to improve access to records or to change the storage space required.

File Management
(1) A term that defines the functions of creation, insertion, deletion, or updating of stored files and records in files. (2) The operations that are performed on files.

First-In-First-Out (FIFO)
The order that data is entered into, and retrieved from a file.

Flag Bit
A processor memory bit, controlled through firmware or a user program, used to signify a certain condition. Example: Battery Low

Flow Chart
A graphical representation for the definition, analysis, or solution of a problem. Symbols are used to represent a process or sequence of decisions and events.

Force Off Function
A feature which allows the user to reset an input image table bit or de-energize an output, independent of the processor program.

Force On Function
A feature which allows the user to set an image table bit or energize an output, independent of the processor program.

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H

Hardware
The mechanical, electrical, and electronic devices which compose a programmable controller and its application

Header Rung
The first level of a ladder diagram program. It is a requirement when programming PLC-2 family processors or on the Data Highway.

Hexadecimal Numbering System
A base-16 numbering system that uses the symbols 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, and A, B, C, D, E, F.

High=True
A signal type where the higher of two voltages indicates a logic state of On (1). See **Low=True**.

I

Image Table
An area in processor memory dedicated to I/O data. Ones and zeros (1 and 0) represent On and Off conditions, respectively. During every I/O scan, each discrete input controls a bit in the input image table; each discrete output is controlled by a bit in the output image table.

Information
The meaning assigned to data by known conventions.

Input Devices
Devices such as limit switches, pressure switches, pushbuttons, analog devices, and/or digital devices, that supply data to a processor.

Instruction
A command that causes a processor to perform one specific operation. The user enters a combination of instructions into processor memory to form a unique application program.

Integer
Any positive or negative whole number or zero.

Intelligent I/O Module
Microprocessor-based modules that perform processing or sophisticated closed-loop, application functions.

Interference
Any undesired electrical signal induced into a conductor by electrostatic or electromagnetic means.

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Interlock
A device actuated by the operation of some other device to which it is associated, to govern the succeeding operation of the same or allied devices.

I/O
Input/Output

I/O Channel
A data transmission link between a processor scanner module and an I/O adapter module.

I/O Chassis
See chassis

I/O Module
A device that interfaces between the user devices and the processor.

I/O Rack
See Rack.

I/O Scan Time
The time required for the processor to monitor inputs and control outputs.

I/O Terminal
A terminal on the I/O module. One I/O terminal has a corresponding bit address in the data table.

Isolated I/O Module
A module which has each input or output electrically isolated from every other input or output on that module.

K

K
2^{10} = 1K = 1024. Used to denote sizes of memory and can be used in bits, bytes, or words. Example: 2K = 2048.

k
Kilo. A prefix used with units of measurement to designate quantities 1000 times as great.

Keying
Plastic bands installed on backplane connectors to ensure that only one type of module can be inserted into a keyed connector.

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L

Ladder Diagram
An industry standard for representing control systems.

Ladder Diagram Programming
A method of writing a user program in a format similar to a relay ladder diagram.

Language
A set of symbols and rules used for representing and communicating information.

Latching Relay
A relay that maintains a given position by mechanical or electrical means until released mechanically or electrically.

Leading Edge One-Shot
A programming technique that sets a bit for one scan when its input condition has made a false-to-true transition. The false-to-true transition represents the leading edge of the input pulse.

Least Significant Bit (LSB)
The bit that represents the smallest value in a nibble, byte, or word.

Least Significant Digit (LSD)
The digit that represents the smallest value in a byte or word.

LED
Light-Emitting Diode.

LED Display
An illuminated visual readout composed of alphanumeric character segments.

Limit Switch
An electrical switch actuated by some part and/or motion of a machine or equipment.

Line
(1) A component part of system used to link various subsystems located remotely from the processor. (2) The source of power for operation. Example: 120V ac line.

Liquid Crystal Display (LCD)
A reflective visual readout of alphanumeric characters. Since its character segments are displayed only by reflected light, it has extremely low power consumption. Contrasted with LED Display, which emits light.

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Load
(1) The power used by a machine or apparatus. (2) To place data into an internal register under program control. (3) To place a program from an external storage device into central memory under operator control.

Load Resistor
A resistor connected in parallel with a high impedance load so the output circuit driving the load can provide at least the minimum current required for proper operation.

Local I/O Processor
A processor where I/O distance is physically limited and must be located near the processor. However, it may still be mounted in a separate enclosure. See **Remote I/O Processor.**

Location
A storage position in memory. Uniquely specified in Allen-Bradley processors by 5-, 6-, 7-, 8-, or 9-digit address.

Logic
A systematic means of solving complex problems through the repeated use of the AND, OR, NOT functions (they can be either true or false). Often represented by ladder diagrams.

Logic Diagram
A diagram which represents the logic elements and their interconnections.

Logic Level
The voltage magnitude associated with signal pulses representing ones and zeros (1 and 0) in binary computation.

Loop
A sequence of instructions which is executed repeatedly until a terminating condition is satisfied.

Low=True
A signal type where the lower of two voltages indicates a logic state of ON (1). See **High=True.**

Lower Nibble
The four least significant bits of a byte.

LSB
See Least Significant Bit.

LSD
See Least Significant Digit.

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M

Master
A device used to control secondary devices.

Master Control Relay (MCR)
A mandatory hardwired relay that can be de-energized by any series-connected emergency stop switch. Whenever the master control relay is de-energized, its contacts open to de-energize all application I/O devices.

Master Control Reset (MCR)
See MCR Zones

MCR Zones
User program areas where all non-retentive outputs can be turned off simultaneously. Each MCR zone must be delimited and controlled by MCR fence codes (MCR instructions).

Memory
A group of circuit elements that can store or retrieve data.

Memory Map
A diagram showing a system's memory addresses and what programs and data are assigned to each section of memory.

Message
(1) A meaningful combination of alphanumeric characters which establishes the content and format of a report. (2) An information unit designated for transfer by a single command form the application to the network.

MOS
Metal Oxide Semiconductor. A semiconductor device in which an electric field controls the conductance of a channel under a metal electrode called a gate.

Mnemonic
A term, usually an abbreviation, that is easy to remember.

Mode
A selected method of operation. Example: run, test, or program.

Modem
A contraction of Modulator/Demodulator. Equipment that connects data terminal equipment to a communication line.

Module
An interchangeable, plug-in item containing electronic components

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Module Addressing
A method of identifying the I/O modules installed in a chassis.

Module Group
Adjacent I/O modules which relate 16 I/O terminals to a single 16-bit image table word.

Module Slot
A location for installing an I/O module.

Monitor
(1) A CRT display. (2) To observe an operation.

Monitoring Controller
Used in an application where the process is continually checked to alert the operator of possible application malfunctions.

Most Significant Bit (MSB)
The bit representing the greatest value of a nibble, byte, or word.

Most Significant Digit (MSD)
The digit representing the greatest value of a byte or word.

Motor Controller
A device or group of devices that serve to govern, in a predetermined manner, the electrical power delivered to a motor.

Motor Starter
See Motor Controller.

MSB
See Most Significant Bit.

MSD
See Most Significant Bit.

Multiple-Rung Display
A feature that allows a number of rungs of program logic to be displayed simultaneously on the industrial terminal.

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N

National Bureau of Standards (NBS)
An organization under the United States Department of Commerce responsible for developing and disseminating federal standards in many areas.

National Electrical Code (NEC)
A set of regulations governing the construction and installation of electrical wiring and apparatus, established by the National Fire Protection Association and suitable for mandatory application by governing bodies exercising legal jurisdiction. It is widely used by state and local authorities within the United States.

NBS
See National Bureau of Standards.

NEC
See National Electrical Code.

NEMA Standards
Consensus standards for electrical equipment approved by the members of the National Electrical Manufacturers Association (NEMA).

NEMA Type 12
A category of industrial enclosures intended for indoor use to provide a degree of protection against dust, falling dirt, and dripping non-corrosive liquids. They do not provide protection against conditions such as internal condensation.

Noise
Unwanted disturbances imposed upon a signal that tend to obscure its data content.

Noise Immunity
The ability to function in the presence of noise.

Noise Spike
A noise disturbance of relatively short duration.

Non-Volatile Memory
A memory that is designed to retain its data while its power supply is turned off.

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O

Octal Numbering System
A numbering system that uses only the digits 0 through 7. Also called base-8.

Off Line
Equipment or devices that are not connected to, or do not directly communicate with, the central processing unit.

On Line
Equipment or devices which communicate with the device it is connected to.

Online Data Change
Allows the user to change various data table values using a peripheral device while the application is operating normally.

Online Editing
Allows the user to modify a program using a peripheral device while the application is operating normally.

One-Shot
A programming technique which sets a storage bit or output bit for only one program scan. See **Leading Edge One-Shot** and **Trailing Edge One-Shot.**

Open System
A system that can be connected to other systems because of compliance to some established standard(s).

Operating System
A software system that controls the operation of a processor system by providing for input/output, allocation of memory space, or translation of programs.

Output
Information transferred from processor images table words through output modules to control output devices.

Output Devices
Devices such as solenoids and motor starters that receive data from the programmable controller.

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P

Parallel Operation
A type of information transfer where all bits, bytes, or words are handled simultaneously.

Parallel Output
Simultaneous availability of two or more bits, channels, or digits.

Parallel Transmission
The simultaneous transmission of bits which constitute a character.

Parity
The use of a self-checking code employing binary digits in which the total number of ones is always even or odd.

Parity Bit
An additional bit added to a binary word to make the sum of the number of ones in a word always even or odd.

Parity Check
A check in which the parity bit is compared with a previously computed parity bit.

Peripheral Equipment
Units which communicate with the programmable controller, but are not part of the programmable controller. Example: a programming device or computer.

PID Control
See **Proportional, Integral, Derivative Control**.

PR
See **Preset Value**.

Preset Value (PR)
The number of time intervals or events to be counted.

Pressure Switch
A switch that is activated at a specified pressure.

Process
(1) Continuous and regular production executed in a definite uninterrupted manner. (2) One or more entities threaded together to perform a requested service.

Processor
The decision making data and storage sections of programmable controller.

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Program
A set of instructions used to control a machine or process.

Program Scan Time
The time required for the processor to execute the instructions in the program. The program scan time may vary depending on the instructions and each instruction's status during the scan.

Program Storage
The portion of memory reserved for saving programs, routines, and subroutines.

Programmable Controller
A solid-state control system which has a user-programmable memory for storage of instructions to implement specific functions such as I/O control, logic, timing, counting, report generation, Data Highway communication, arithmetic, data and file manipulation. A programmable controller consists of a central processor, input/output interface, and memory. A programmable controller is designed as an industrial control system.

Programming Plug
A user accessible connection that establishes the operating parameters of a module.

PROM
Programmable Read Only Memory. A type of ROM that requires an electrical operation to store data. In use, bits or words are read on demand but not changed.

Proportional Control
See **Proportional, Integral, Derivative Control.**

Proportional, Integral, Derivative Control
An intelligent I/O module or ladder diagram instruction which provides automatic closed-loop operation of multiple continuous process control loops. For each loop, this module can perform any or all of the following control functions:

- **Proportional Control** causes an output signal to change as a direct ratio of the error signal variation.
- **Integral Control** causes an output signal to change as a function of the error signal time duration.
- **Derivative Control** causes an output signal to change as a function of the rate of change of the error signal.

Protected Memory
Data and storage locations that are inhibited from being written into.

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R

Rack
An addressing concept equivalent to 128 discrete I/O.

Rack Fault
(1) A red diagnostic indicator that lights to signal a loss of communication between the processor and any remote I/O chassis. (2) The condition which is based on the loss of communication.

Read/Write Memory
A memory where data can be stored (write mode) or accessed (read mode). The write mode replaces previously stored data with current data; the read mode does not alter stored data.

Record
A group of data that is stored together and/or used together in processing. A collection of related data is treated as a unit. See **File**.

Redundancy
The duplication of devices for the purpose of enhancing the reliability or continuity of operations.

Redundant System
Two or more devices that actively control the outputs of a system. Each device in the system votes on every control decision. If one device makes a decision that does not agree with the decision made by the other devices, it drops out of the loop and the others continue to control the outputs.

Register
A memory word or area used for temporary storage of data used within mathematical, logical, or transferral functions.

Relay Logic
A representation of the program or other logic in a form normally used for relays.

Remote I/O Processor
A processor system where some or all of the I/O racks are remotely mounted from the processor. The location of remote I/O racks from the processor may vary depending on the application and the processor used. Also see **Local I/O Processor**.

Remote Mode Selection
A feature which allows the user to select or change processor modes of operation with a peripheral device from a remote location.

Remote Programming
A method of performing processor programming by connecting the programming device to the network rather than to the processor.

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Reply
Data transmitted in response to a request.

Report
An application data display or printout containing information in a user-designed format. Reports could include operator messages, part records, and production lists. Initially entered as messages, reports are stored in a memory area separate from the user program.

Report Generation
The printing or displaying of user-formatted application data by means of a data terminal. Report generation can be initiated by means of either a user program or a data terminal keyboard.

ROM
Read Only Memory. A type of memory with data content that cannot be changed or is changed infrequently. In use, bits and words are read on demand, but not changed.

RS-232-C
An EIA electrical connection standard. Most often used as a standard interface for serial binary communication between data terminal equipment and data communications equipment.

Rung
A group of processor instructions which controls an output or storage bit, or performs other control functions such as file moves, arithmetic and/or sequencer instructions. This is represented as one section of a logic ladder diagram.

S

Scan Time
See **Programming Scan Time** and **I/O Scan Time.**

Screen
The viewing surface of a CRT where data is displayed.

Scrolling
The vertical movement of data on a CRT display caused by the dropping of one line of displayed data for each new line added.

Search Function
Allows the user to quickly display and/or edit any instruction in the processor program.

Signal
The event or electrical quantity that conveys information from one point to another.

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State
The logic 0 or 1 condition in processor memory or at a circuit input or output.

Storage
See **Memory.**

Storage Bit
A bit in a data table word which can be set or reset, but is not associated with a physical I/O terminal point.

Subroutine
A program segment in the ladder diagram that performs a specific task and is available for use.

Subroutine Area (SBR)
A portion of memory where subroutines are stored.

Subsystem
(1) A part of a larger system having the properties of a system in its own right. (2) A system within another system.

Suppression Device
A unit that attenuates the magnitude of electrical noise.

Surge
A transient current or power.

Synchronous
A type of serial transmission that maintains a constant time interval between successive events.

Synchronous Shift Register
A shift register where only one change of state occurs per control pulse.

Syntax
Rules governing the structure of a language.

System
A set of one or more processors, I/O devices and modules, computers, the associated software, peripherals, terminals, and communication networks, that together, provide a means of performing information processing for controlling machines or processes.

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T

Tasks
A set of instructions, data, and control information capable of being executed by a CPU to accomplish a specific purpose.

Terminal Address
A 5-digit number which identifies a single I/O terminal. It is also related directly to a specific image table bit address.

Terminal Control System
The operating system used to execute Grafix programs, and to perform other activities while the Advisor is on line and in use by an operator.

Termination
(1) The load connected to the output end of a transmission line. (2) The provisions for ending a transmission line and connecting it to a bus bar or other terminating device.

Throughput
The rate at which equipment processes or transmits data.

Toggle Switch
A panel-mounted switch with an extended lever; normally used for On/Off switching.

Trailing Edge One-Shot
A programming technique that sets a bit for a scan when its input condition has made a true-to-false transition. The true-to-false transition represents the trailing edge of the input pulse.

True
As related to processor instructions, an enabled logic state.

Two's Complement
The negative of a binary number obtained by inverting all of the bits in the number and then adding 1 to the least significant bit.

U

Underflow Bit
A bit that is set to indicate the result of an operation is less than the minimum value that can be contained in a register.

Upload
The process of transferring end-device data from a network interface to the network controller. Control programs can be up-loaded to be verified against a master copy in memory

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Upload/Download
Commonly refers to the reading/writing of programs and data tables from or into processor memory. The commands to do these processes come from some supervisory device.

Upper Nibble
The four most significant bits of a byte.

V

Variable
A factor which can be altered, measured, or controlled.

Variable Data
Numerical information which can be changed during application operation. It includes timer and counter accumulated values, thumbwheel settings, and arithmetic results.

Volatile Memory
A memory that loses its information if the power is removed.

W

Wall Clock/Calendar
A device that continually measures time in a system without respect to what tasks the system is performing.

Watchdog Timer
A timer that monitors logic circuits controlling the processor. If the watchdog timer is not in its programmed time period, it will cause the processor to fault.

Word
A grouping or a number of bits in a sequence that is treated as a unit.

Word Length
The number of bits in a word. In a processor, these are generally only data bits. One processor word = 16 data bits.

Word Storage
An unused data table word which may be used to store data without directly controlling an output. Any storage word may be monitored as often as necessary by the user program.

Work Area
A portion of the data table reserved for specific processor functions.

Write
(1) The process of loading information into memory. (2) Block Transfer; a transfer of data from the processor data table to an intelligent I/O module

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Z

ZCL Instructions
A user-program fence for ZCL zones.

ZCL Zones
Assigned program areas which may control the same outputs through separate rungs, at different times. Each ZCL zone is bound and controlled by ZCL instructions. If all ZCL zones are disabled, the outputs would remain in their last state.

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Appendix E

Quick Reference

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Adjusting the Data Table

For Data Table Sizes Between 48 and 26 Words

Number of Timers and Counters	Data Table Size	Number of Timers and Counters	Data Table Size	Number of Timers and Counters	Data Table Size
000	0048				
001	0050	036	0120	071	0190
002	0052	037	0122	072	0192
003	0054	038	0124	073	0194
004	0056	039	0126	074	0196
005	0058	040	0128	075	0198
006	0060	041	0130	076	0200
007	0062	042	0132	077	0202
008	0064	043	0134	078	0204
009	0066	044	0136	079	0206
010	0068	045	0138	080	0208
011	0070	046	0140	081	0210
012	0072	047	0142	082	0212
013	0074	048	0144	083	0214
014	0076	049	0146	084	0216
015	0078	050	0148	085	0218
016	0080	051	0150	086	0220
017	0082	052	0152	087	0222
018	0084	053	0154	088	0224
019	0086	054	0156	089	0226
020	0088	055	0158	090	0228
021	0090	056	0160	091	0230
022	0092	057	0162	092	0232
023	0094	058	0164	093	0234
024	0096	059	0166	094	0236
025	0098	060	0168	095	0238
026	0100	061	0170	096	0240
027	0102	062	0172	097	0242
028	0104	063	0174	098	0244
029	0106	064	0176	099	0246
030	0108	065	0178	100	0248
031	0110	066	0180	101	0250
032	0112	067	0182	102	0252
033	0114	068	0184	103	0254
034	0116	069	0186	104	0256
035	0118	070	0188		

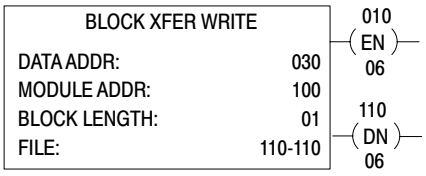
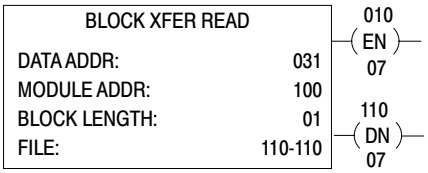
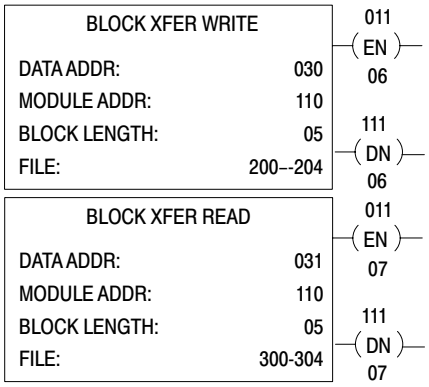
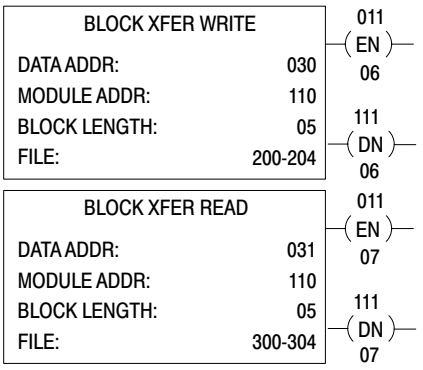
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For Data Table Sizes Between 384 and 7808 Words

Enter	Data Table Size	Enter	Data Table Size
The Mini-PLC-2/02 has this number of data table blocks.			
3	384	10	1280
4	512	11	1408
5	640	12	1536
6	768	13	1664
7	896	14	1792
8	1024	15	1920
9	1152		
The Mini-PLC-2/16 has this additional number of data table blocks.			
16	20488	24	3072
17	2176	25	3200
18	2304	26	3328
19	2432	27	3456
20	2560	28	3584
21	2688	29	3712
22	2816	30	3840
23	2944	31	3968
The Mini-PLC-2/17 has this additional number of data table blocks.			
32	4096	47	6016
33	4229	48	6144
34	4352	49	6272
35	4480	50	6400
36	4608	51	6528
37	4736	52	6656
38	4864	53	6784
39	4992	54	6912
40	5120	55	7040
41	5248	56	7168
42	5376	57	7296
42	5504	58	7424
44	5632	59	7552
45	5760	60	7680
46	5888	61	7808

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Block Transfer Instructions BLOCK XFER Key Method

Key Sequencer	1770-T3 Display	Instruction Notes
BLOCK XFER 0		Output instruction. Block length depends on kind of module. Entire file transferred in one scan. Done bit remains on for one scan after valid transfer.
BLOCK XFER 1		Data read from I/O module must be buffered Uses two words of user program for each instruction.
BLOCK XFER 0		Set block lengths equal or to default value for module. Enter both instruction blocks for bi-directional block transfer.
BLOCK XFER 1		Same module address used for read and write instruction. Enable read and write instructions in same scan. Order of operation determined by the module. Refer to the module user's manual. Enter both instruction blocks for bi-directional block transfer.

IMPORTANT: Numbers shown are default values. The number of default address digits displayed (3 or 4) will depend on the size of the data table.

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Here is an explanation of each value:

This Value:	Stores the:
Data Address	First possible address in the timer/counter accumulated value area of the data table
Module Address	RGS for R = rack, G = module, S = slot number
Block Length	Number of words to be transferred Enter 00 for default value or for 64 words
File	Address of the first word of the file
Enable bit -(EN)-	Automatically entered from the module address Set on when the rung containing the instruction is true
Done bit -(DN)-	Automatically entered from the module address Remains on for 1 program scan following successful transfer

Two GET Method



10410–I

Here is an explanation of the optional conditions:

This Condition:	Examine the:
WYZ	First timer/counter address (accumulated area).
XYZ	Timer/counter address 100_8 higher than WYZ (preset area).
RGS	Location of the block transfer module (I/O rack, module group. and module slot. S is a zero for the left slot and a 1 for the right slot. For a 2-slot module, S is always zero.
ABC	Starting address where data in transferred to/from.
0RGST	Output energize initiates Block Transfer. 0 = output byte R = rack G = module group S = module slot T = 6 for write operation; 7 for read operation

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Clearing Memory

Function	Key Sequencer	Mode	Description
Data table clear	[CLEAR MEMORY] [77] (Start Address_ (End Address) [CLEAR MEMORY]	Program	Displays a start address and an end address field. Start and end word addresses determine boundaries for data table clearing. Clears data table within and including addressed boundaries.
User program clear	[CLEAR MEMORY] [88]	Program	Position the cursor at the desired location in the program. Clears the user program from the position of the cursor to the first boundary: i.e. temporary end, subroutine area or end statement. Does not clear data table or messages.
Partial memory clear	[CLEAR MEMORY] [99]	Program	Clears user program and messages from position of the cursor. Does not clear data table unless the cursor is on the first program instruction.
Total memory clear	[CLEAR MEMORY] [99]	Program	Position the cursor on the first instruction of the program. Clears user program messages and data table.
Important: When memory protect is active, memory cannot be cleared except for data table addresses 010_8-177_8 with a programmed EEPROM installed.			

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Counter Instructions

Important: The counter word address, XXX, is assigned to the counter accumulated areas of the data table. To determine which addresses are valid accumulated areas, the third digit from the right must be an even number.

This Bit:	Contains This Information:
14	overflow/underflow bit
15	count complete bit
16	enable bit for CTD instruction
17	enable bit for CTU instruction

The word address displayed will be 3 or 4 digits long depending on the data table size. When entering the word address, use a leading zero if necessary.

Key Symbol	Instruction Name	1770-T3 Display	Rung Conditions	Status Bits
–(CTU)–	Up Counter	XXX –(CTU)– PR YYY AC ZZZ	Each time the rung goes true, the accumulated value is incremented one counter. The counter continues counting after the preset value is reached. The accumulated value can be reset by the CTR instruction	When the rung is true: If AC> 999 bit 14 is set When AC ≥ PR bits 15 and 17 are set When the rung is false: Bit 14 and 15 are retained; if they were set, bit 17 is reset
–(CTR)–	Counter Reset	XXX –(CTR)– PR YYY AC ZZZ	XXX – Word address of the CTU is resetting. The preset and accumulated values are automatically entered by the industrial terminal. When the rung is true the CTU and CTD accumulated value and status bits are rest to 000.	When the rung is true: Bits 14, 15, 16, 17 are reset When the rung is false: No action is taken
–(CTD)–	Down Counter	XXX –(CTD)– PR YYY AC ZZZ	Each time the rung goes true, the accumulated value is decreased by one count.	When the rung is true: AC is < 000 Bit 14 is set When AC<PR bits 15 and 16 are set When the rung is false: Bits 14 and 15 are retained; if they were set, bit 16 is reset

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Data Monitor Functions

Function	Key Sequence	Mode	Description
Display	[DISPLAY] [0]	Any	Displays the binary data monitor.
Print	[DISPLAY][0] [RECORDS]	Any	Prints the first 20 lines of binary data monitor.
Display	[DISPLAY][1]	Any	Displays the hexadecimal data monitor.
Print	[DISPLAY][1] [RECORD]	Any	Prints the first 20 lines of hexadecimal data monitor.
Display	[DISPLAY][2]	Any	Displays the ASCII data monitor.
Print	[DISPLAY][2] [RECORD]	Any	Prints the first 20 lines of ASCII data monitor.

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Data Transfer File Instructions

Key Sequence	1770-T3 Display	Instruction Notes
FILE 10	FILE TO FILE MOVE COUNTER ADDR: 030 POSITION: 001 FILE LENGTH: 003 FILE A: 200– 202 FILE B: 300– 302 RATE PER SCAN: 003 030 (EN) 17 030 (DN) 15	Output instruction. Modes: Complete, Distributed, and Incremental Counter is internally incremented by the instruction. Requires 5 words of user program.
FILE 11	WORD TO FILE MOVE COUNTER ADDR: 030 POSITION: 001 FILE LENGTH: 003 WORD ADDR: 010 FILE R: 110– 112 030 (DN) 15	Output instruction. Counter must be externally indexed by user program. Data is transferred every scan that rung is true. Requires 4 words of user program.
FILE 12	FILE TO WORD MOVE COUNTER ADDR: 030 POSITION: 001 FILE LENGTH: 003 FILE A: 200– 202 WORD ADDR: 010 030 (DN) 15	Same as Word-To-File.

Important: Numbers shown are default values. The number of default address digits displayed (3 or 4) will depend on the size of the data table.

Here is an explanation of each value:

This Value:	Stores This:
Counter address	Address of the instruction's file position in the accumulated value area of the data table.
Position	Current word being operated upon (accumulated value of the counter).
File length	Number of words in file (preset value of the counter).
File A	Starting address of the source file.
File R	Starting address of the destination file.
Word address	Address of the source word or destination word outside of the file.
Rate per scan	Number of words of data moved per scan.

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EAF Function Numbers

If you want to perform an operation of this type	Use this function number
The Mini-PLC-2/02, Mini-PLC-2/16 and Mini-PLC-2/17 can perform these functions.	
Addition	(01)
Subtraction	(02)
Multiplication	(03)
Division	(04)
Square Root	(05)
BCD to Binary	(13)
Binary to BCD	(14)
FIFO Load	(28)
FIFO Unload	(29)
Log10	(30)
Sin x	(35)
Cos x	(36)
10^x	(37)
The Mini-PLC-2/17 can perform these additional functions.	
Log_e	(31)
Y to the X $y^{+/-x}$	(33)
Powers of e $e^{+/-x}$	(32)
Reciprocal 1/x	(34)
Averaging	(06)
Standard Deviation	(07)
PID	(27)
Set Clock	(10)
Set Date	(11)
Set Leap Year and Day of the Week	(12)
Read Clock	(15)
Read Date	(16)
Read Leap Year and Day of the Week	(17)

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Editing Functions

Function	Key Sequence	Mode	Description
Insert a condition instruction	[INSERT] (instruction) (address) or [INSERT][—] (instruction) (address)	Program	Position the cursor on the instruction that will precede the instruction to be inserted. Then press the key sequence. 1 2 Position the cursor on the instruction that will follow the instruction to be inserted. Then press the key sequence. 1 2
Remove a condition instruction	[REMOVE] (instruction)	Program	Position the cursor on the instruction to be removed and press the key sequence. 1
Insert a rung	[INSERT][RUNG]	Program	Position the cursor on the instruction in the preceding rung and press the key sequence. Enter instructions and complete the rung. 1
Remove a rung	[REMOVE][RUNG]	Program	Position the cursor anywhere on the rung to be removed and press the key sequence. 1
Change data of a word or block instruction	[INSERT][DATA]	Program	Position the cursor on the word or block instruction whose data is to be changed. Press the key sequence.
Change the address of a word or block instruction	[INSERT] (first digit) [—] (Address)	Program	Position the cursor on a word or block instruction with data and press [Insert]. Enter the first digit of the first data value of the instruction. Then use the [ ] and [ ] key as needed to cursor up to the word address. Enter the appropriate digits of the word address.
Program on line	[SEARCH] 5 2		Initiates online programming.
Replace an instruction or change the address of an instruction without data	[Instruction] (Address)	Program	Position the cursor on the instruction to be replaced or whose address is to be Press the desired instruction key (or key sequence) and the required address(es).
Change data on line	[SEARCH] 5 1 (Data) [RECORD] [CANCEL COMMAND]	Run/Program	Position the cursor on the word or block instruction whose data is to be changed. Press the key sequence. Cursor keys can be used. Press [RECORD] to enter the new data into memory. To terminate online data change.
All editing functions	[CANCEL COMMAND]	Program Run/Program	Aborts the operation at the current cursor position. 1

1 These functions can also be used during online programming.

2 When bit address exceeds 5 digits, press the [Expand Addr] key before entering address and enter a leading zero if necessary.

IMPORTANT: Only addresses corresponding to output energize, latch and unlatch instructions are cleared to zero.

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Execution Times and Words Per Instruction

Approximate Execution Time Per Scan and Words Per Instruction

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average μ sec.	False average μ sec.	
These instructions are features of Mini-PLC-2/02, Mini-PLC-2/16, and Mini-PLC-2/17				
Examine On	–[ ]–	7 [10]	6 [10]	1 [1]
Examine Off	–[/]–	5 [10]	5 [10]	1 [1]
Output Energize	–( )–	8 [10]	8 [10]	1 [1]
Output Latch	–(L)–	7 [10]	6 [10]	1 [1]
Output Unlatch	–(U)–	7 [10]	6 [10]	1 [1]
Get	–[G]–	15 [10]	–	1 [1]
Put	–(PUT)–	12 [10]	7	1 [1]
Equal	–(=)–	12 [10]	13 [10]	1 [1]
Less Than	–(<)–	14 [10]	13 [10]	1 [1]
Get Byte	–]B[–	11 [10]	–	1 [1]
Limit Test	–]L[–	13 [10]	14 [10]	1 [1]
Counter Reset	–(CTR)–	19	6	1
Retentive Timer Reset	–(RTR)–	19	6	1
Timer On-Delay	–(TON)–	51	36	1
Retentive Timer On-Delay	–(RTO)–	52	33	1
Timer Off-Delay	–(CTD)–	55	39	1
Up Counter	–(CTU)–	38	30	1
Down Counter	–(CTD)–	36	31	1

[1] add 1 word per instruction when its address is 400_8 or greater
[2] add 2 words per instruction when its address is 400_8 or greater
[3] 1 word
[4] 999 words
[5] 1 bit
[6] 999 bits
[7] with 2 data values
[8] with 10 data values
[9] with 50 data values
[10] add 8 μs per instruction when its address is 400_8 or greater
[11] add 16 μs per instruction when its address is 400_8 or greater

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Approximate Execution Time Per Scan and Words Per Instruction (continued)

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average μ sec.	False average μ sec.	
Add	-(+)-	29 [10]	9 [10]	1 [1]
Subtract	-(-)-	32 [10]	8 [10]	1 [1]
Multiply	-(x)-(x)-	201 [11]	18 [11]	2 [2]
Divide	-(:)-(:)-	184 [9]	20 [11]	2 [2]
Add	EAF 01	247	30	3
Subtract	EAF 02	252	30	3
Multiply	EAF 03	915	30	3
Divide	EAF 04	1442	30	3
Square Root	EAF 05	1007	30	3
BCD to Binary	EAF 13	228	31	3
Binary to BCD	EAF 14	192	31	3
FIFO Load	EAF 28	409 [3]	116	3
		8051 [4]	116	
FIFO Unload	EAF 29	377 [3]	117	3
		8051 [4]	117	
Bit Shift Left		222 [5]	55	5
		534 [6]	55	
Bit Shift Right		234 [5]	56	5
		482 [6]	55	
Examine Off Bit Shift	EAF 18	58	18	3
Examine On Bit Shift	EAF 19	60	18	3
Set Bit Shift	EAF 16	61	20	3
Reset Bit Shift	EAF 17	61	20	3
Log 10	EAF 30	807	30	3
Sin X	EAF 35	538	30	3
Cos X	EAF 36	538	30	3

[1] add 1 word per instruction when its address is 400_8 or greater
[2] add 2 words per instruction when its address is 400_8 or greater
[3] 1 word
[4] 999 words
[5] 1 bit
[6] 999 bits
[7] with 2 data values
[8] with 10 data values
[9] with 50 data values
[10] add 8 μs per instruction when its address is 400_8 or greater
[11] add 16 μs per instruction when its address is 400_8 or greater

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Approximate Execution Time Per Scan and Words Per Instruction (continued)

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average μ sec.	False average μ sec.	
10x	EAF 37	685	30	3
Master Control Reset	–(MCR)–	7	7	1
Zone Control Last State	–(ZCL)–	12	8	1
Branch Start		8	6	1
Branch End		8	10	1
End, Temporary End	T. END	11	8	1
Subroutine Area	SBR	*	13	1
Immediate Input Update	–[I]–	62	–	1
Immediate Output Update	–(IOT)–	67	9	1
Label	LBL	17	–	1
Return	–(RET)–	*	0	1
Jump to Subroutine	–(JSR)–	*	9	1
Jump	–(JMP)–	34	10	1
Block Transfer Read		54	52	2
Block Transfer Write		54	52	2
Sequencer Output	SEQ 0	343	72	5
Sequence input	SEQ 1	418	36	5
Sequencer Load	SEQ 2	283	69	4
File-To-File Move	FILE 10	291	60	5
Word-To-File Move	FILE 11	153	49	4
File-To-Word Move	FILE 12	153	49	4

* = combined true execution time – 79 μs

1 add 1 word per instruction when its address is 400_8 or greater
2 add 2 words per instruction when its address is 400_8 or greater
3 1 word
4 999 words
5 1 bit
6 999 bits
7 with 2 data values
8 with 10 data values
9 with 50 data values
10 add 8 μs per instruction when its address is 400_8 or greater
11 add 16 μs per instruction when its address is 400_8 or greater

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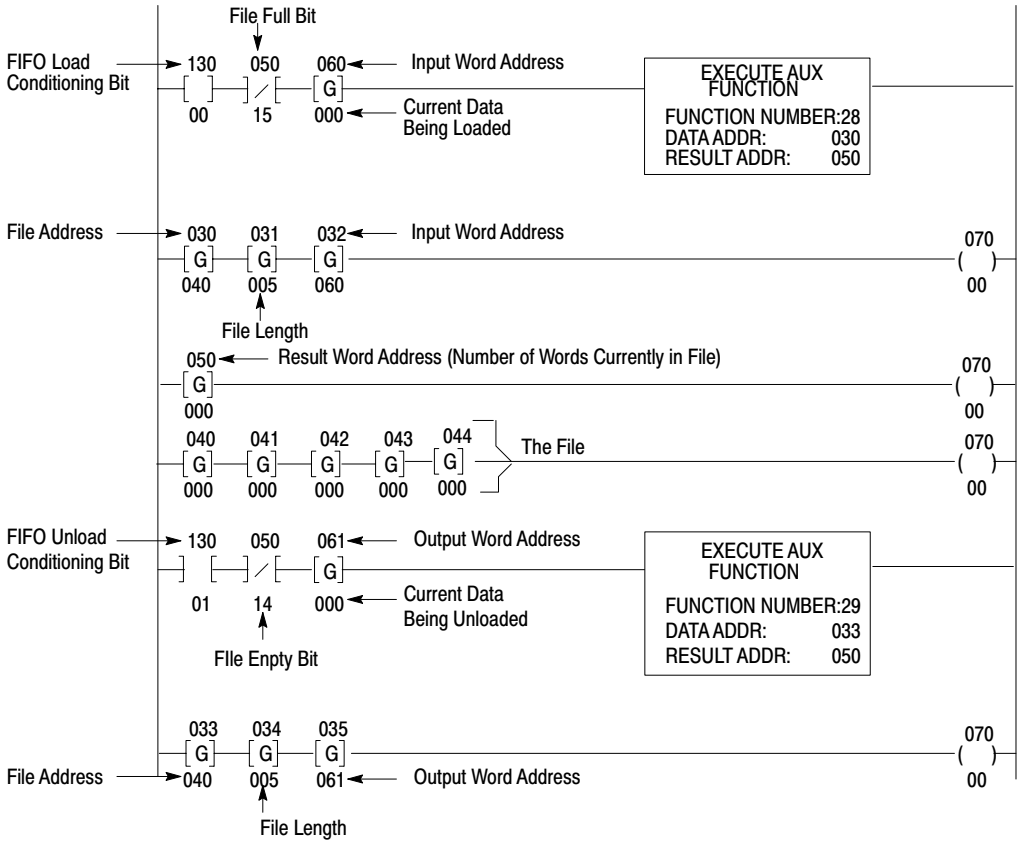
Approximate Execution Time Per Scan and Words Per Instruction (continued)

Instruction Name	Symbol	Instruction		Words Per Instruction
		True average μ sec.	False average μ sec.	
These EAF instructions are features of the Mini-PLC-2/17 only.				
Set Clock	EAF 10	217	30	3
Set Date	EAF 11	225	30	3
Set Leap Year and Day of Week	EAF 12	167	31	3
Read Clock	EAF 15	203	30	3
Read Date	EAF 16	205	30	3
Read Leap Year and Day of Week	EAF 17	138	31	3
PID	EAF 27	2450 (typical) 3500 (max.)	118	3
Log_e	EAF 31	1727	30	3
Powers of e ($e^{+/-x}$)	EAF 32	2071	30	3
Powers of Y ($y^{+/-x}$)	EAF 33	1500	30	3
Reciprocal (1/x)	EAF 34	1620	30	3
Average (3-digit	EAF 06	2463 [7]	101	3
		6787 [8]	101	
		2784 [9]		
		2103 [7]	98	
Average (6-digit)	EAF 06	3374 [8]	98	3
		10038 [9]	98	
Standard Deviation (3-digit)	EAF 07	4260 [7]	119	3
		34430 [8]	119	
Standard Deviation (6-digit)	EAF 07	162384 [9]	119	3
		13532 [7]	101	
		23322 [8]	101	
		70746 [9]	101	

[1] add 1 word per instruction when its address is 400_8 or greater
[2] add 2 words per instruction when its address is 400_8 or greater
[3] 1 word
[4] 999 words
[5] 1 bit
[6] 999 bits
[7] with 2 data values
[8] with 10 data values
[9] with 50 data values
[10] add 8 μs per instruction when its address is 400_8 or greater
[11] add 16 μs per instruction when its address is 400_8 or greater

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FIFO Load and FIFO Unload



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Graphic Programming

Alphanumeric/Graphic Key Definitions

Key	Function
[LINE FEED]	Moves the cursor down one line in the same column.
[RETURN]	Returns the cursor to the beginning of the next line.
[RUB OUT]	Deletes the last character or control code that was entered.
[REPT LOCK]	Allows the next character that is pressed to be repeated continuously until [REPT LOCK] is pressed again.
[SHIFT]	Allows the next key pressed to be a shift character.
[SHIFT LOCK]	Allows all subsequent keys pressed to be shift characters until [SHIFT] or [SHIFT LOCK] is pressed.
[CTRL]	Used as part of a key sequence to generate a control code.
[ESC]	Terminates the present function.
[MODE SELECT]	Terminates all functions and returns the mode select display to the screen.
Blank Yellow Keys	Space keys. Move the cursor one position to the right.

Industrial Terminal Control Codes

Control Code Key Sequence	Function
[CTRL][P] [Column #][;] [Line #][A]	Positions the cursor at the specified column and line number [CTRL][P][A] positions the cursor at the top left corner of the screen.
[CTRL][P][F]	Moves the cursor one space to the right.
[CTRL][P][U]	Moves the cursor one line up in the same column.
[CTRL][P][5][C]	Turns cursor on.
[CTRL][P][4][C]	Turns cursor off.
[CTRL][P][5][G]	Turns on graphics capability.
[CTRL][P][4][G]	Turns off graphics capability.
[CTRL][P][5][P]	Turns Channel C outputs on.
[CTRL][P][4][P]	Turns Channel C outputs off.
[CTRL][I]	Horizontal tab that moves the cursor to the next preset 8th position.
[CTRL][K]	Clears the screen from cursor position to end of screen and moves the cursor to the top left corner of the screen.
Key Sequence	**Attribute** [1]
[CTRL][P][0][T]	Attribute 0 = Normal Intensity
[CTRL][P][1][T]	Attribute 1 = Underline
[CTRL][P][2][T]	Attribute 2 = Intensify
[CTRL][P][3][T]	Attribute 3 = Blinking
[CTRL][P][4][T]	Attribute 4 = Reverse Video

[1] Any three attributes can be used at one time using the following key sequence:
[CTRL][P][Attribute #][;][Attribute #][;][Attribute #][T]

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ASCII Control Codes

Control Code [1]	Display [2]	ASCII Mnemonic	Name
CTRL 0 [3]	N_U	NUL	NULL
CTRL A [3]	S_H	SOH	START OF HEADER
CTRL B [3]	S_X	STX	START OF TEXT
CTRL C [3]	E_X	ETX	END OF TEST
CTRL D	E_T	EOT	END OF TRANSMISSION
CTRL E	E_Q	ENQ	ENQUIRE
CTRL F	A_K	ACK	ACKNOWLEDGE
CTRL G	B_L	BEL	BELL
CTRL H	B_S	BS	BACKSPACE
CTRL I	H_T	HT	HORIZONTAL TAB
CTRL J	L_F	LF	LINE FEED
CTRL K	V_T	VT	VERTICAL TAB
CTRL L	F_F	FF	FORM FEED
CTRL M	C_R	CR	CARRIAGE RETURN
CTRL N	S_O	SO	SHIFT OUT
CTRL O	S_I	SI	SHIFT IN
CTRL P	D_L	DLE	DATA LINK ESCAPE
CTRL Q	D_1	DC1	DEVICE CONTROL 1
CTRL R	D_2	DC2	DEVICE CONTROL 2
CRTL S	D_3	DC3	DEVICE CONTROL 3
CTRL T	D_4	DC4	DEVICE CONTROL 4
CTRL U	N_K	NAK	NEGATIVE ACKNOWLEDGE
CTRL V	S_Y	SYN	SYNCHRONOUS IDLE
CTRL W	E_B	ETB	END OF TRANSMISSION BLOCK
CTRL X	C_N	CAN	CANCEL
CTRL Y	E_M	EM	END OF MEDIUM
CTRL Z	S_B	SUB	SUBSTITUTE
ESCAPE	E_C	ESC	ESCAPE
CTRL,	F_S	FS	FILE SEPARATOR
CTRL-	G_S	GS	GROUP SEPARATOR
CTRL.	R_S	RS	RECORD SEPARATOR
CTRL/	U_S	US	UNIT SEPARATOR
DELETE	D_T	DEL	DELETE

1 Some ASCII control codes are generated using non standard keystrokes.
2 Will be displayed when Control Code Display option is set ON in Alphanumeric mode, only. (Not in Report Generation mode).
3 Invalid key in Report Generation mode.

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Help

Help Directories

Function	Key Sequence	Mode	Description
Help directory	[HELP]	Any	Displays a list of the keys that are used with the [HELP] key to obtain further directories.
Control function directory	[SEARCH] [HELP]	Any	Provides a list of all control functions that use the [SEARCH] key.
Record function directory	[RECORD] [HELP]	Any	Provides a list of functions that use the [RECORD] KEY.
Clear memory directory	[CLEAR MEMORY] [HELP]	Remote Prog	Provides a list of all functions that use the [CLEAR MEMORY] key.
Data monitor directory	[DISPLAY] [HELP]	Any	Provides the choice of data monitor display accessed by the [DISPLAY] key.
File instruction directory	[FILE] [HELP]	Any	Provides a list of all instructions that use the [FILE] key.
Sequencer instruction directory	[SEQ][HELP]	Any	Provides a list of all instructions that use the [SEQ] key.
Block transfer directory	[BLOCK XFER] [HELP]	Any	Provides a list of all instructions that use the [BLOCK XFER] key.
All directories	[CANCEL COMMAND]	Any	To terminate.

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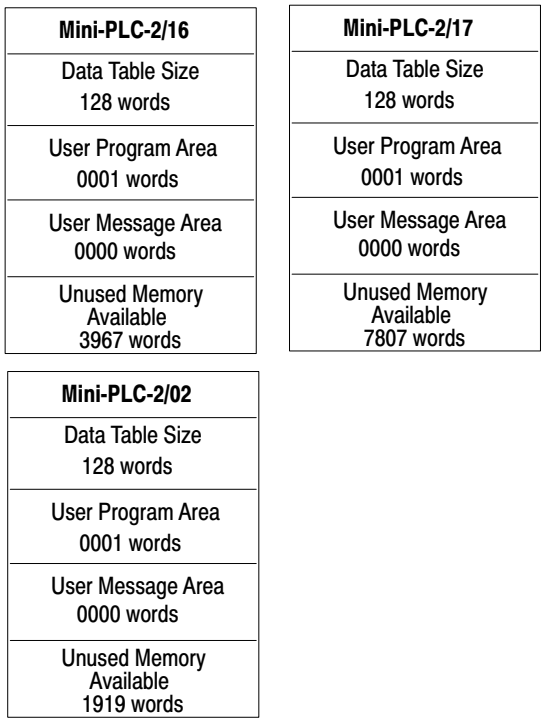
Memory Layout

To examine memory layout:

SEARCH — The word SEARCH appears in the lower left hand corner of the screen.

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Memory Layout Display



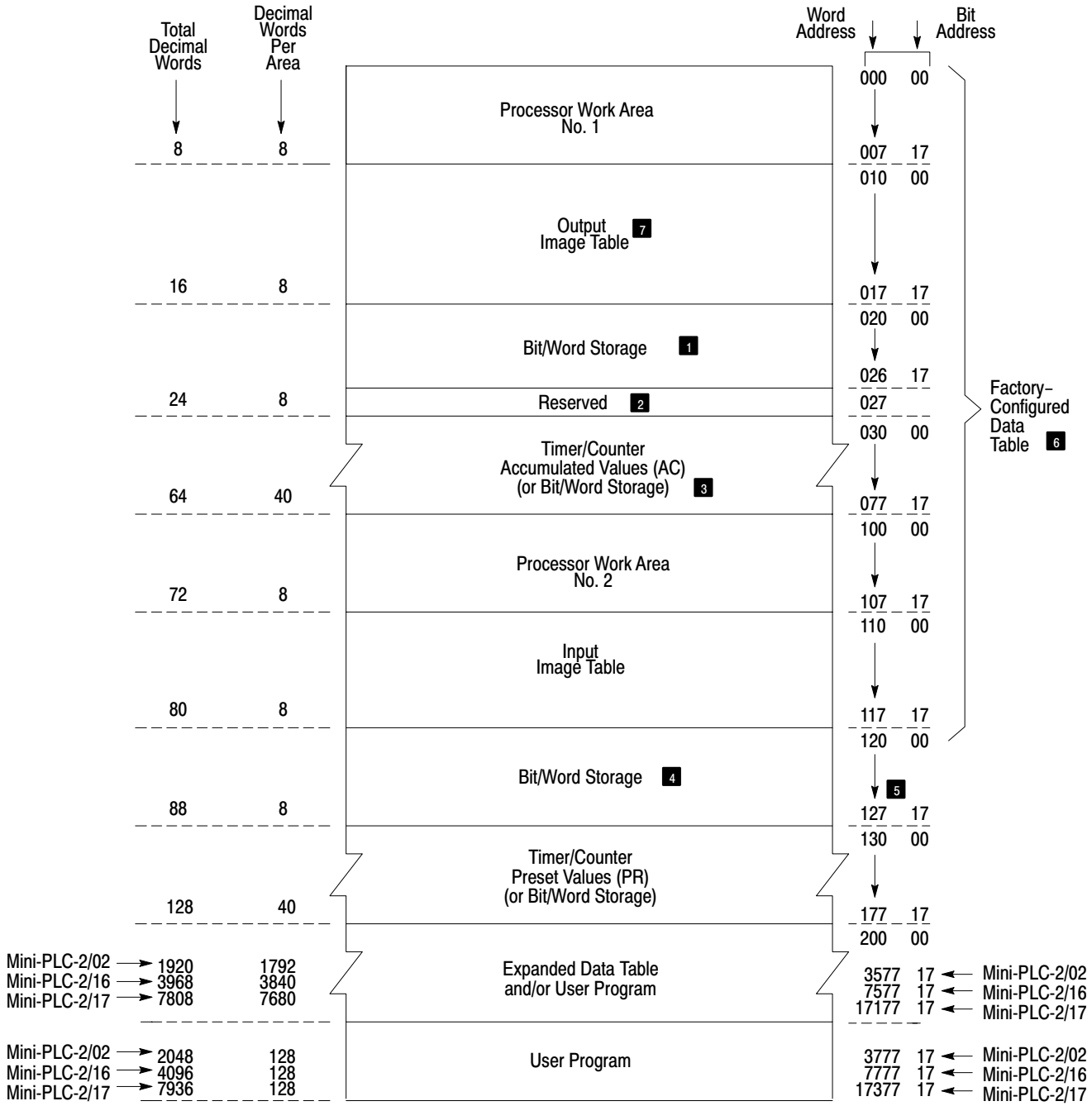
This illustrates the memory layout display for a 178 word data table.

Even if there are no messages or programs in the memory, the END statement is there and it requires one word. Adding the number of words in the four areas equals the memory size (decimal).

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Memory Structure

Data Table Factory Configured for 2-Slot Addressing

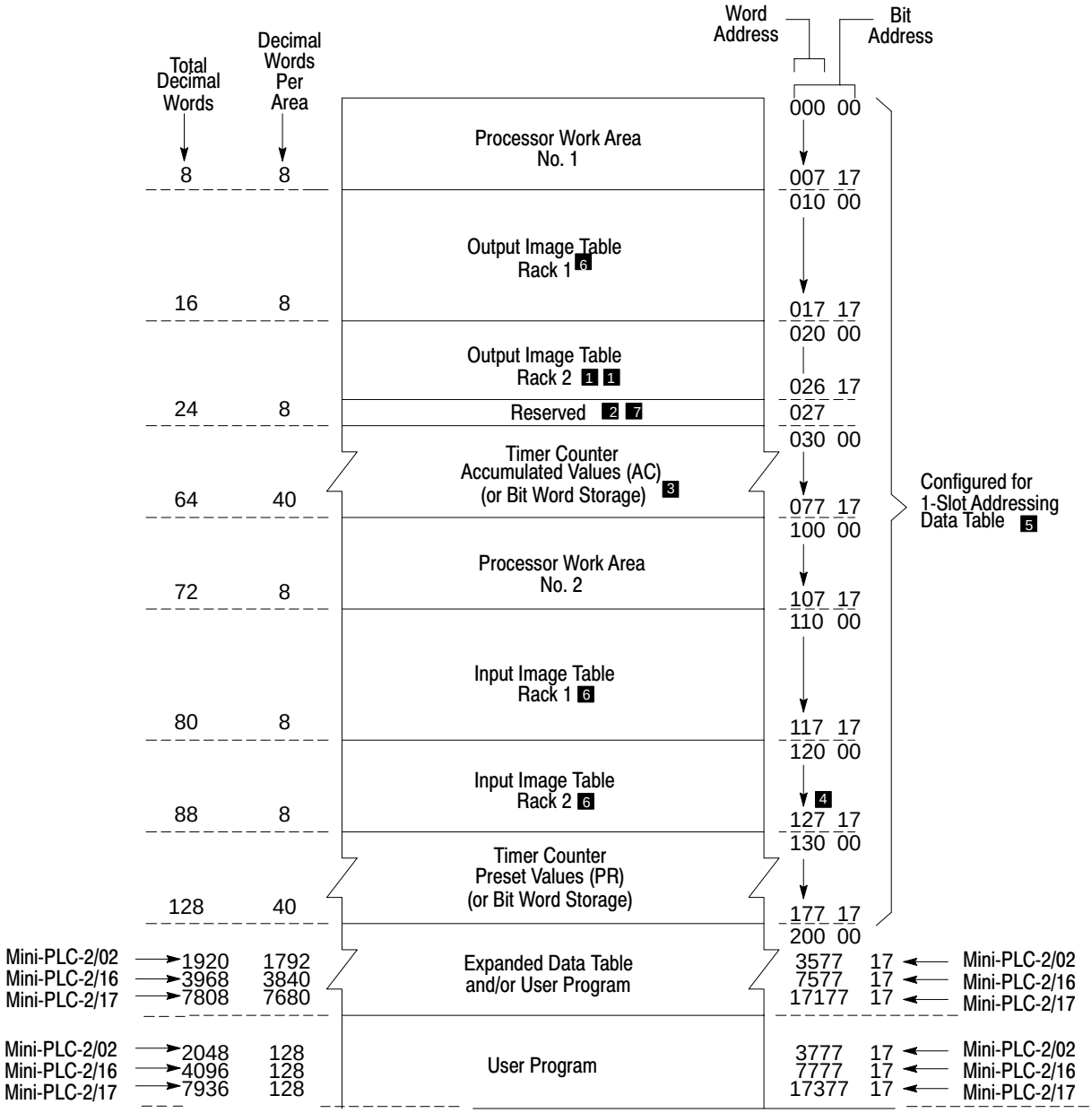


1 May not be used for accumulated values.
2 Not available for bit/word storage. Bits in this word are used by the processor.
3 Unused timer/counter memory words can reduce data table size and increase user program area.
4 May not be used for preset values.
5 Do not use word 127 for block transfer data storage.
6 Can be decreased to 48 words.
7 Do not use for bit/word storage.

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Data Table Configured for 1-Slot Addressing

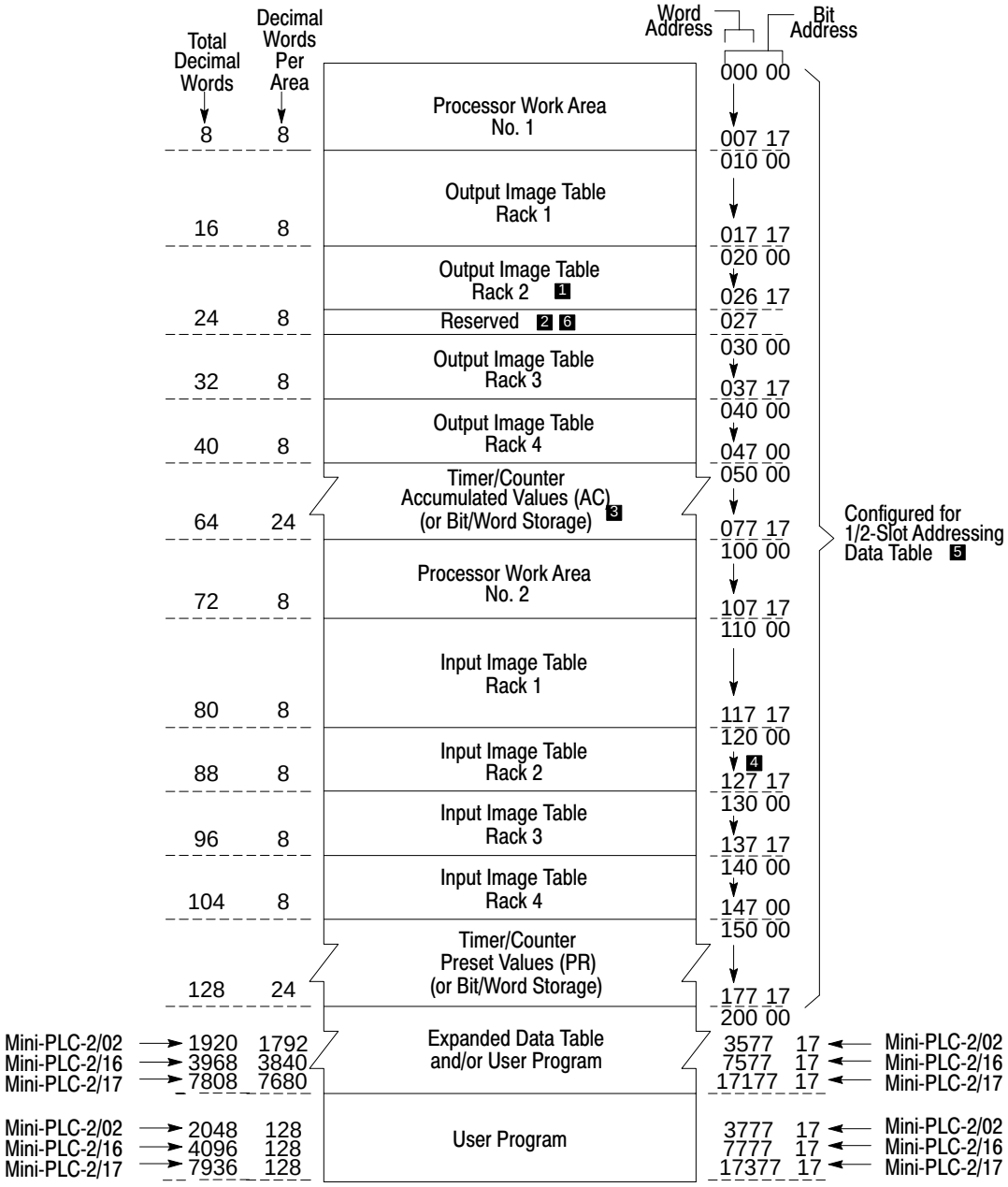


1. May not be used for accumulated values.
2. Not available for bit/word storage. Bits in this word are used by the processor.
3. Unused timer/counter memory words can reduce data table size and increase user program area.
4. Do not use word 127 for block transfer data storage.
5. Can be decreased to 48 words.
6. Used with 1-slot addressing.
7. You cannot put an output or block transfer module in rack 2, I/O group 7 when using 1-slot addressing. You can put an input module in rack 2, I/O group 7.

10349–I

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Data Table Configured for 1/2-Slot Addressing



1 May not be used for accumulated values.
2 Not available for bit/word storage. Bits in this word are used by the processor.
3 Unused timer/counter memory words can reduce data table size and increase user program area.
4 Do not use word 127 for block transfer data storage.
5 Can be decreased to 48 words.
6 You cannot put an output or block transfer module in rack 2, I/O Group 7 when using 1/2-slot addressing. You can put an input module in rack 2, I/O group 7.

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PID Control Block

Control Word 01 Bit Descriptions: Status Bits

00	–	Equation (Set by User) Independent Gain =0	Dependent Gain = 1
01	–	Mode (Set by User) Auto =)	Manual = 1
02	–	Control Action (Set by User) Direct (SP–PV) = 0	Reverse (PV–SP) = 1
03	–	Output Limiting (Set by User) No – 0	Yes = 1
04	–	Set Output (Set by User) Inhibited = 0	Enabled = 1
05	–	Cascade Bit (Set by User) 3 No = 0 Secondary Cascade Loop = 1	
06	–	Derivative Uses Error (set by User) 3 PV = 0	E = 1
07	–	Input Format (for Series C or later) Binary = 0 BCD = 1	
10	–	Dead Band (set by Instruction) 1 Out of DB = 0	Within DB = 1
11	–	Maximum Output Alarm (set by Instruction) 1 Within limit = 0	Above limit = 1
12	–	Minimum Output Alarm (Set by Instruction) 1 Within limit = 0	Below limit = 1
13	–	Set point Error (Set by Instruction) 1 In range = 0	Out of range = 1
14	–	Reserved 2	
15	–	Done bit (set by Instruction) 1 Not executed = 0 Executed = 1	
16	–	Reserved 2	
17	–	Enabled bit (set by Instruction) 1 Not enabled = 0	Enabled = 1

1 Do not change. Values are set by PID function.
2 Do not change Reserved bits.
3 Do not change while the processor is operating.

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Control Word 02 Bit Descriptions: Status and SIgn Bits

00	–	K_Ix10 (Set by User) Do not move decimal = 0 Move decimal to right = 1
01	–	K_P/10 (Set by User) Do not move decimal = 0 Move decimal = 1
02	–	Feedforward/Bias Sign (Set by User) Pos = 0 Neg = 1
03	–	Maximum Scaling Sign (Set by User) Pos = 0 Neg = 1
04	–	Minimum Scaling Sign (Set by User) Pos = 0 Neg = 1
05	–	Set Point Sign (Set by User) Pos = 0 Neg = 1
06	–	Process Variable Sign (Set by Instruction) 1 Pos = 0 Neg = 1
07	–	Error Sign (Set by Instruction) 1 Pos = 0 Neg = 1
10	–	Resume Control From Last State 2 Disabled – on first scan, a new CO is calculated Enabled = on first scan, the accumulated integral value is back-calculated from the last CO value
11	–	Bumpless Transfer With Proportional Controllers 3 0 = no adjustment to Bias 1 = bumpless manual to auto mode by adjusting Bias

1 Do not change these vales. They are set by the PID function.
2 This bit should only be set after the PID program has been run to obtain a valid last CO value
3 Do not change while the processor is operating.

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Words 03 through 09

All range values are unitless unless noted otherwise.

Independent Gain Equation		**Dependent Gain Equation**
Range 0000-9999	Word 03 **Set Point – SP** [1]	Range 0000-9999
Range 00.00-99.99	Word 04 **Proportional Gain**	Range 00.00-99.99
Term K_I Range Bit set 0.000-9.999 Bit reset 0.000-9.999 Units rep/sec	Word 05 **Integral Gain**	Term 1/TI Range 00.00-99.99 Units rep/min
Term KD Range Bit set 00.01-99.99 Bit reset 000.1-999.9 Units – sec	Word 06 **Derivative Gain**	Term TD Range 00.00-99.99 Unites – min
Range 0000-4095 or 0000-FFFF [3]	Word 07 **Feedforward – FFWD** [1]	Range 0000-4095 or 0000-FFFF [3]
Range 0000-9999	Word 08 **Maximum Scaling Value** [1] [2]	Range 0000-9999
Range 0000-9999	Word 09 **Minimum Scaling Value**	Range 0000-9999

[1] Can be negative number by setting appropriate sign bits.
[2] Do not change while processor is operating.
[3] With word 02 Bit 11 set.

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Table 1.B
Words 10 through 24

Independent Gain Equation		**Dependent Gain Equation**
Range 0000-9999	Word 10 **Zero Crossing Dead Band**	Range 0000-9999 Units 0000-9999
Range 0000-100% Units Percent Range 0000-100% Unites Percent	Word 11 **Set Output Value** Word 12 **Maximum Control Output**	Range 0000-100% Units Percent Range 0000-100% Units Percent
Range 0000-100% Units Percent	Word 13 **Minimum Control Output**	Range 0000-100% Units Percent
Range 0000-99.99 Units sec	Word 14 **Loop Update Time**	Range 00.00-99.99 Units sec
Range 0000-9999	Word 15 **Process Variable – PV**	Range 0000-9999
Range 0000-9999	Word 16 **Error** [2]	Range 0000-9999
Range 0000-100% Units Percent	Word 17 **Control Output** [2]	Range 0000-100% Units Percent
	Words 18 through 24 Reserved [3]	

[1] Do not change while processor is operating.
[2] Do not change. These values are set by the PID function.
[3] Do not change Reserved bits.

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PROC Indicator

If the PROC indicator	And the processor	You should
Green	is in the Run mode operating normally • program is executing • outputs are enabled. is in MEM STORE mode and EEPROM memory module is being programmed. The indicator will be ON for a few seconds and then then turn OFF.	No action required
Blinking Green	has an I/O configuration error • there is an illegal backplane switch combination (i.e., switch 4 is ON, switch 5 is OFF) • the I/O is not in complementary fashion (32-pt. I/O only).	Check the switch settings and module placement.
Red	has a possible hardware failure • program is not executing • if switch 1 of the switch group assembly if OFF, outputs are disabled data lines on the I/O chassis could be shorted to ground	Cycle power. If the problem still persists, call your A-B representative.
Off	is operating normally in Program or Remote Test mode is operating in Run mode, it has a memory or program error	Change the processor to Program mode, correct problem and cycle power. If problem still persists, call your A-B representative.

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Report Generation

Address Delimiters

Delimiter Format	Explanation	Message Report Format
XXX	Enter 3-digit word address between delimiters.	Displays the 3-digit BCD value at assigned word address.
XXX1 or *XXX0*	Enter 3-digit word address and a "1" for upper byte or a "0" for lower byte between delimiters.	Displays the 3-digit octal value at assigned byte address.
XXXXX	Enter 5-digit bit address between delimiters.	Displays the On or Off status of the assigned bit address.
#XXX#	Enter 3, 4, or 5-digit word address between delimiters.	Displays the 3-digit BCD value at assigned word address.
!XXX!	Enter 3, 4, or 5-digit word address between delimiters.	Displays the 4-digit hex value at address.
&XXX1& &XXX0&	Enter 3, 4, or 5 digit word address and a "1"for upper byte or a "0" for lower byte between delimiters.	Displays the 3-digit octal value at the assigned byte address.
XXXXX	Enter 5, 6, or 7-digit bit address between delimiters.	Displays the On or Off status of the assigned bit address.

Report Generation Commands

Command	Key Sequence	Description
Enter report generation function	[RECORD][DISPLAY] Set baud rate (Message Code Keys)	Puts industrial terminal into report generation function. Same (entered from a peripheral device).
Message store	[M][S][,] (Message Number) [RETURN]	Stores message in processor memory. Use [ESC] to end message.
Message print	[M][P][,] (Message Number) [RETURN]	Prints message exactly as entered.
Message report	[M][R][,] (Message Number) [RETURN]	Prints message with current data table values or bit status.
Message delete	[M][D][,] (Message Number) [RETURN]	Removes message from processor memory.
Message index	[M][I][RETURN]	Lists messages used and the number of words in each message.
Automatic report generation.	[SEARCH][4][0] [M][R][RETURN]	Allows messages to be printed through program control.
Exit automatic report generation	[ESC] [CANCEL COMMAND] 1	Terminates automatic report generation.
Exit report	[ESC] [CANCEL COMMAND] 1	Returns to ladder diagram display. Terminates Report Generation Function.

1 [CANCEL COMMAND] can only be used if the function was entered by a command from a peripheral device.

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Search

Search Functions

Function	Key Sequence	Mode	Description
Locate first rung of program	[SEARCH][↑]	Any	Positions cursor on the first instruction of the program.
Locate last rung of program area	[SEARCH][↓]	Any	Positions cursor on the temporary end instruction, subroutine area boundary, or the end statement depending on the cursor's location. Press key sequence again to move to the next boundary.
Locate first instruction of current rung	[SEARCH][←]	Remote Prog	Positions cursor on first instruction of the current rung.
Move cursor off screen	[SEARCH][←]	Remote Test Run/Program	Moves cursor off screen to left.
Locate output instruction of current rung	[SEARCH][→]	Any	Positions cursor on the output instruction of the current rung.
Locate rung without an output instruction	[SHIFT] [SEARCH]	Any	Locates any rung left incomplete due to an interruption in programming.
Locate specific instruction	[SEARCH] [Instruction key] (Address)	Any	Locates instruction searched for. Press [SEARCH] to locate the next occurrence of instruction.
Locate specific word address	[SEARCH] (address)	Any	Locates this address in the program (excluding -| |- and -| / |- instructions and addresses in files). Press [SEARCH] to locate the next occurrence of this address. [1]
Single rung display	[SEARCH] [DISPLAY]	Any	Displays the first rung of a multiple rung display by itself. Press key sequence again to view multiple rungs.
Print	[SEARCH] [4][3]	Any	Prints a single rung.
Print	[SEARCH] [4][4]	Any	Prints a ladder diagram dump.
Print	[SEARCH] [4][5]	Remote Prog	Prints a total memory dump.
Print	[SEARCH] [5][0]	Any	Prints the first 20 lines of data table configuration.
Print	[SEARCH] [5][3]	Any	Prints the first 20 lines of bit manipulation.
Print	[SEARCH] [5][4]	Any	Prints the first 20 lines of memory layout display.
Program controls outputs	[SEARCH] [5][9][0]	Run/Program	Places the processor in run/program mode.
Program executes outputs disabled	[SEARCH] [5][9][1]	Remote Test	Places the processor in remote test mode.
Processor awaits commands	[SEARCH] [5][9][2]	Remote Program	Places the processor in remote program mode.

[1] Enter leading zeros when bit address exceeds 5 digits or word address exceeds 3 digits.

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Sequencer Instructions

Key Sequence	1770-T3 Display	Instruction Notes
SEQ 0	SEQUENCER OUTPUT COUNTER ADDR: 030 CURRENT STEP: 001 SEQ LENGTH: 001 WORDS PER STEP: 1 FILE: 110- 110 MASK: 010- 010 OUTPUT WORDS 1: 010 2: [ ] 3: [ ] 4: [ ] 030 (EN) 17 030 (DN) 15	Output instruction Increments, then transfers data. Same data transferred each scan that the rung is true. Counter is indexed by the instruction. Unused output bits can be masked. Requires 5-8 words of your program.
SEQ 1	SEQUENCER INPUT COUNTER ADDR: 030 CURRENT STEP: 000 SEQ LENGTH: 001 WORDS PER STEP: 1 FILE: 110- 110 MASK: 010- 010 INPUT WORDS 1: 010 2: [ ] 3: [ ] 4: [ ]	Input instruction. Compares input data with current step for equality. Counter must be externally indexed by a counter instruction within your program. Unused input bits can be masked. Requires 5-8 words of your program.
SEQ 2	SEQUENCER LOAD COUNTER ADDR: 030 CURRENT STEP: 000 SEQ LENGTH: 001 WORDS PER STEP: 1 FILE: 110- 110 LOAD WORDS 1: 010 2: [ ] 3: [ ] 4: [ ] 030 (EN) 17 030 (DN) 15	Output instruction. Increments, then loads data. Counter is indexed by the instruction. Does not mask. Requires 4-7 words of your program.

Important: Numbers shown are default values. Numbers in shaded areas must be replaced by user-entered values. The number of default address digits displayed (3 or 4) will depend on the size of the data table.

Here is an explanation of each value:

This Value:	Stores the:
Counter Address	Address of the instruction in the accumulated value area of the data table
Position	Position in the sequencer table (accumulated value of counter)
Seq Length	Number of steps (preset value of the counter)
Words per Step	Width of the sequencer table
File	Starting address of the source file
Mask	Starting address of the mask file
Word Address	Address of the source word or destination word outside of the file
Output Words	Words controlled by the instruction
Load Words	Words fetched by the instruction
Input Words	Words monitored by the instruction

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Switch Group Assembly Settings

Set Switches 1, 4, 5 and 8

If you want:	Then set:	And
Outputs to remain in their last state when a fault (red LED in ON) is detected [1]	Switch 1 ON	--
Outputs to de-energize when a fault (red LED is ON) is detected [1]	Switch 1 OFF	--
2-slot addressing [2]	Switch 4 OFF	Switch 5 OFF
1-slot addressing [3]	Switch 4 OFF	Switch 5 ON
1/2-slot addressing [4]	Switch 4 ON	Switch 5 ON
RAM memory protect disabled	Switch 8 OFF	--
RAM memory protect enabled [5]	Switch 8 ON	

[1] Last state switch only on PLC-2/16 and -2/17 series C or later, and PLC-2/02 series A or later.

[2] When using 2-slot addressing and 8-pt. I/O modules: a 16-slot chassis equals one rack which can address 128 I/O. See chapters 5 and 7.

[3] When using 1-slot addressing and 16-pt. I/O modules: a 16-slot chassis equals two racks which can address 256 I/O. See chapters 5 and 7.

[4] When using 1/2-slot addressing and 16-pt. I/O modules: a 16-slot chassis can address four racks which equals 512 I/O. See chapters 5 and 7.

[5] When memory protect is enabled, you can only change the status and value of the bits in the first 128 words (word addresses up to 177_8) of the data table.

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Set Switches 6 and 7

If	And	Then
Without and EEPROM installed in your processor		
Switch 6 is OFF	Switch 7 may be either ON or OFF	With a battery installed and a program stored in RAM memory, your processor powers-up in the mode identified by the position of the mode select switch. If the mode select switch is in the RP position, the processor will power-up in the remote program mode. Without a battery installed and without a program stored in RAM memory, your processor powers-up in the program mode or remote program mode (depending on the keyswitch position) and a `PROCESSOR MEMORY INVALID` message appears on the 1770-T3 terminal.
Switch 6 is ON	Switch 7 may be either ON or OFF	If the mode select switch is in RP position with valid memory, the processor powers up in the same mode (run/program, remote test or remote test or remote program) that it powered down in. If the switch is not in the R/P position, then the power up mode is determined by the position of the switch (run or program).
If	**And**	**Then**
With an EEPROM installed in your processor		
Switch 6 is OFF	Switch 7 may be either ON or OFF	Contents of the EEPROM memory module area transferred to RAM memory whether or not RAM memory is valid. If switch 6 is OFF, your processor powers-up in the mode selected by the keyswitch. [2]
Switch 6 is ON	Switch 7 is ON	Contents of the EEPROM memory module are not transferred to RAM memory is RAM memory is valid. [1] Contents of the EEPROM memory module are transferred to RAM memory if RAM memory is not valid. [2]
Switch 6 is ON	Switch 7 is OFF	With a battery installed and a program stored in RAM memory, your processor powers-up in the mode identified by the position of the mode select switch. [1] Contents of the EEPROM memory module are not transferred to RAM memory. Without a battery installed and without a program stored in RAM memory, your processor powers-up in the program mode and a `PROCESSOR MEMORY INVALID` message appears on the 1770-T3 terminal.

[1] If the mode select switch is in the RP position, then the processor powers-up in the last programmed mode or operation, i.e. Run/Program, Remote Test, Remote Program.

[2] If the mode select switch is in the RP position, then the processor powers-up running (RUN/PROG mode). We recommend that you put the mode select switch in the PROG position so that the processor will power-up in the program mode.

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Timer Instructions

Important: The timer word address, XXX, is assigned to the timer accumulated areas of the data table. To determine which addresses are valid accumulated areas, the third digit from the right must be an even number.

The time base 1.0, 0.1 or 0.01 second. Preset values, YYY, and accumulated values, ZZZ, can vary from 000-999.

Bit 15 is the timed bit.
Bit 17 is the enable bit.

The word address displayed will be 3 or 4 digits long depending on the data table size. When entering the word address, use a leading zero if necessary.

Key Symbol	Instruction Name	1770-T3 Display	Rung Conditions	Status Bits
–(TON)–	Timer On Delay	XXX –(TON)– TB PR YYY AC ZZZ	When the rung is true, the timer begins to increment the accumulated value at a rate specified by the time base. When the rung is false, the timer resets the accumulated value to 000.	When the rung is true and AC = PR: bits 15 and 17 set When the rung is false: bits 15 and 17 reset
–(TOF)–	Timer Off Delay	XXX –(TOF)– TB PR YYY AC ZZZ	When the rung is true, the timer resets the accumulated value to 000. When the rung is false, the timer begins to increment the accumulated value.	When the rung is true: bits 15, 17 are set When the rung is false and AC = PR: bits 15 and 17 reset
–(RTO)–	Retentive Timer	–(RTO)– TB PR YYY AC ZZZ	When the rung is true, the timer begins to increment the accumulated value. When false, the accumulated value is retained.	When the rung is true and AC = PR: bits 15 and 17 set When the rung is false: bit 15 no action taken, but bit 17 is reset
–(RTR)–	Retentive Timer	XXX –(RTR)– PR YYY AC ZZZ	XXX – Word address of the retentive timer. It is resetting. The preset and accumulated values are automatically entered by the industrial terminal. When the rung is true,t he accumulated value and status bits are reset.	When the rung is true: bits 15 and 17 are reset When the rung is false: no action is taken

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Diagnostic Word 027

Internal Control Functions

Diagnostic Word: Word 027

Bits in word 027 are used by the processor for internal control functions.

This Bit:	Stores this Information:
00	(Battery low) – set when the battery is low.
01	(EEPROM) – set indicates that EEPROM transferred at power-up. This bit is always reset (0) when the processor powers down
02	(STI too long) – set indicates subroutine execution time plus program transition time exceed service time.
03	Reserved.
04	
05	
06	
07	Reserved for Data Highway – set when the processor is connected to the line and actively communicating with the Data Highway.
10	Report Generation message 1 enable bit
11	Report Generation message 2 enable bit
12	Report Generation message 3 enable bit
13	Report Generation message 4 enable bit
14	Report Generation message 5 enable bit
15	Report Generation message 6 enable bit
16	Report Generation busy bit
17	Report Generation done bit

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