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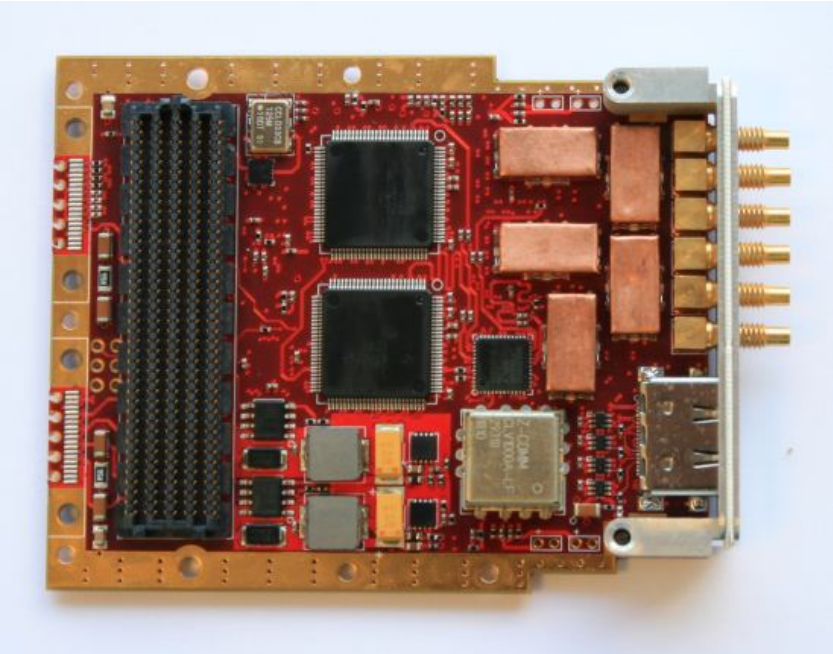
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# FMC110
# User Manual



Abaco Systems, USA

Support Portal

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# Revision History

| Date | Revision | Revision |
|---|---|---|
| 2010-06-01 | Initial release | 1.0 |
| 2010-07-01 | Update in Temperature and voltage parameters table. | 1.1 |
| 2010-09-01 | Added details about programming the FMC110, including SPI timing waveforms.<br>Added FMC signal description in the Appendix.<br>Added CPLD register definition in the Appendix. | 1.2 |
| 2010-09-20 | Updated photo. Modified block diagram. | 1.3 |
| 2010-10-03 | Text corrections in pin list. | 1.4 |
| 2010-10-12 | Update address. Update block diagram | 1.5 |
| 2011-01-21 | Correction in section 4.1.2. | 1.6 |
| 2011-03-01 | Added MICTOR connector references | 1.7 |
| 2011-03-09 | Added coax connector type specification. | 1.8 |
| 2011-04-14 | Added FMC connector type specification.<br>Updated trigger input specification. | 1.9 |
| 2011-08-01 | Update external clock/reference input level.<br>Correction in pin-out table (ADC0_DA_N<1> was not specified) | 1.10 |
| 2012-01-10 | Added I2C pins to the pin-out table. | 1.11 |
| 2012-09-18 | Added changes between revision 1 and revision 2 boards | 1.12 |
| 2012-12-07 | Added monitoring device type | 1.13 |
| 2013-09-16 | Updated Figure 1 and Table 3 - CPLD I/O Voltage Levels to 2.5V or VADJ | 1.14 |
| 2014-03-06 | Changed input power level of external reference | 1.15 |
| 2014-04-09 | Revised some descriptions and fixed typos | 1.16 |
| 2014-06-19 | Changed pin 20 into “shell” in Table 2. HDMI connector pin out. | 1.17 |

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# 1 Acronyms and related documents

## 1.1 Acronyms

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| DDR | Double Data Rate |
| EPROM | Erasable Programmable Read-Only Memory |
| FBGA | Fineline Ball Grid Array |
| FMC | FPGA Mezzanine Card |
| FPGA | Field Programmable Gate Array |
| JTAG | Join Test Action Group |
| LED | Light Emitting Diode |
| LVTTL | Low Voltage Transistor Logic level |
| LSB | Least Significant Bit(s) |
| LVDS | Low Voltage Differential Signaling |
| MGT | Multi-Gigabit Transceiver |
| MSB | Most Significant Bit(s) |
| PCB | Printed Circuit Board |
| PLL | Phase-Locked Loop |
| PSSR | Power Supply Rejection Ratio |

**Table 1: Glossary**

## 1.2 Related Documents

- FPGA Mezzanine Card (FMC) standard ANSI/VITA 57.1-2010
- Datasheet ADS5400, TI
- Datasheet DAC5681Z, TI
- Datasheet AD9517, Analog Devices
- Datasheet ADT7411 Rev B, Analog Devices

# 2 General description

The FMC110 is a dual-channel A/D and dual-channel D/A FMC daughter card. The card provides two 12-bit A/D channels and two 16-bit D/A channels that enable simultaneous sampling at a maximum rate of 1 Gsps.

The sample clock can be supplied externally through a coax connection or by an internal clock source (optionally locked to an external reference). A trigger input for customized sampling control is also available.

The FMC110 daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1). The card has a high-pin count connector, front panel I/O, and can be used in a conduction-cooled environment.

The FMC110 allows flexible control of clock source, sampling frequency, and calibration through a SPI communication bus. The card is also equipped with power supply and temperature monitoring, and it offers several power-down modes to switch off unused functions.

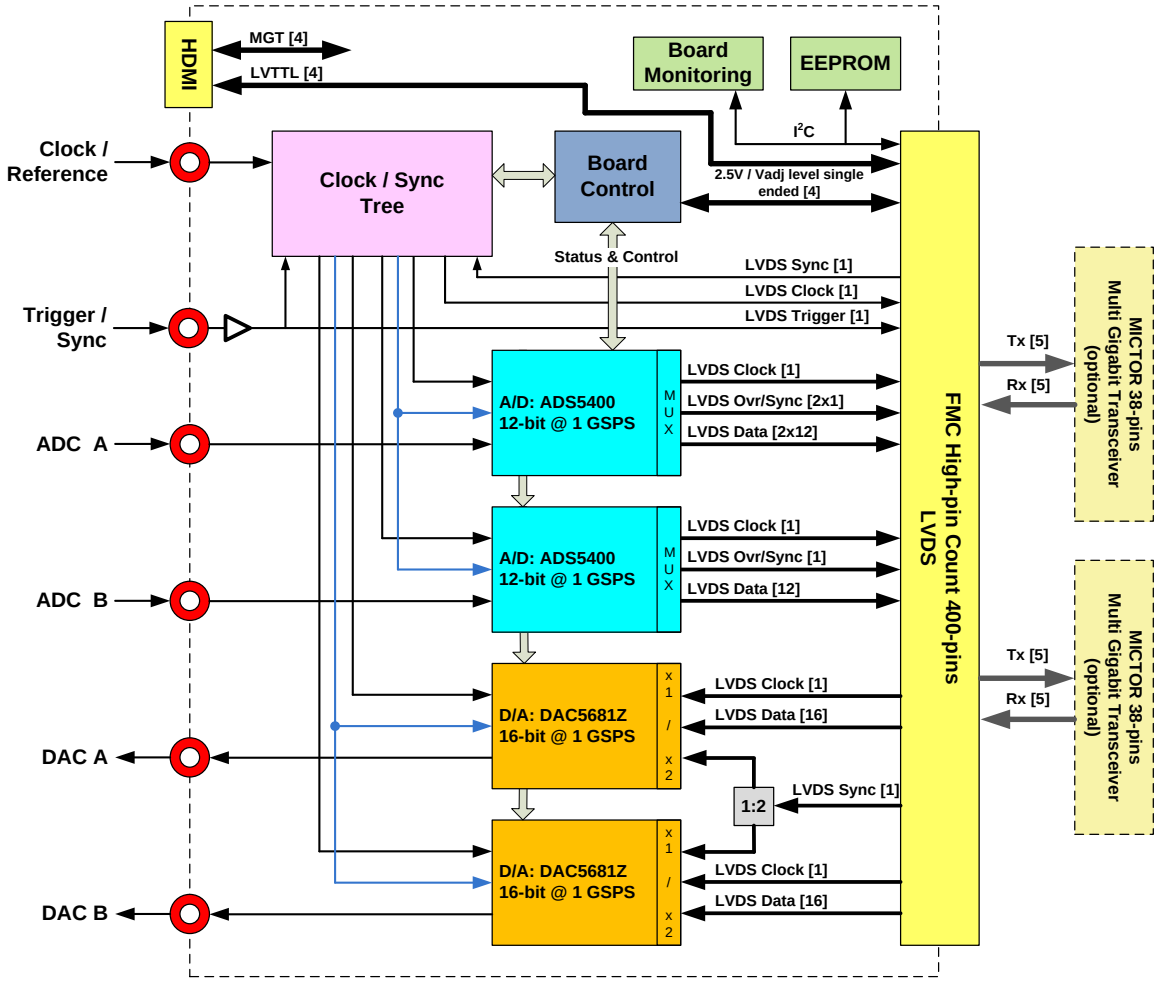



**Figure 1: FMC110 block diagram**

# 3 Installation

## 3.1 Requirements and handling instructions

- The FMC110 daughter card must be installed on a carrier card compliant to the FMC standard.
- The FMC carrier card must support the high-pin count connector (HPC 400-pins).
- The carrier card must support VADJ/VIO_B voltage of +2.5V (LVDS support) for FMC110 revision 1. The carrier card can support VADJ/VIO_B voltage range of 1.65V to 3.3V for FMC110 revision 2, but typically VADJ will be 1.8V or 2.5V for LVDS operation.
- Do not flex the card.
- Prevent electrostatic discharges by observing ESD precautions when handling the card.

## 3.2 LVDS requirements

The A/D channels are based on TI's ADS5400 and can operate in 1-bus or 2-bus mode. In 1-bus mode, all data is transferred to output port A at a maximum rate of 1Gbps per DDR LVDS pair. In 2-bus mode, the data is demultiplexed over output port A and B at a maximum rate of 500Mpbs per DDR LVDS pair.

Output port B of one A/D channel is not available due to the limited amount of LVDS connections on the FMC connector. In 2-bus mode, the sync feature can be used to realign the data coming from the two separate paths on the carrier board.

Each D/A channel has an independent DDR LVDS data bus. The full rate of 1Gsps is supported, but the digital transfer rate can be lowered by enabling the interpolation (x2 or x4) in the D/A devices.

# 4 Design

## 4.1 Physical specifications

### 4.1.1 Board Dimensions

The FMC110 card complies with the FMC standard known as ANSI/VITA 57.1. The card is a single-width, conduction-cooled mezzanine module (with region 1 and front panel I/O).

### 4.1.2 Front panel coax inputs

There are six coax connectors available from the front panel. From top to bottom; 1st analog input (A), 1st analog output (B), 2nd analog output (C), 2nd analog input (D), clock input (CL), trigger input (TR).

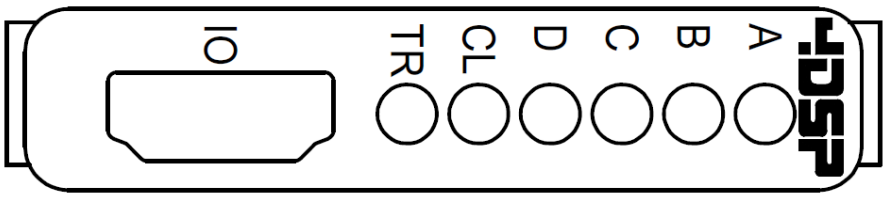



**Figure 2: Bezel drawing**

### 4.1.3 Front panel HDMI I/O

The 19-pin HDMI connector on the front panel (IO) holds four Multi-gigabit transceivers (two Tx pairs / two Rx pairs) and 4x LVTTL I/O (5V tolerant). Contact Abaco for other configurations.

| Pin Number | Signal Name | Pin Number | Signal Name |
|---|---|---|---|
| **1** | DP_M2C_P<0> | **SHELL** | GND |
| **2** | Shield | **19** | N.C. |
| **3** | DP_M2C_N<0> | **18** | N.C. |
| **4** | DP_M2C_P<1> | **17** | N.C. |
| **5** | Shield | **16** | FRONT_IO<1> |
| **6** | DP_M2C_N<1> | **15** | FRONT_IO<0> |
| **7** | DP_C2M_P<2> | **14** | FRONT_IO<3> |
| **8** | Shield | **13** | FRONT_IO<2> |
| **9** | DP_C2M_N<2> | **12** | DP_C2M_N<3> |
| **10** | DP_C2M_P<3> | **11** | Shield |

**Table 2. HDMI connector pin out**

### 4.1.4 Front I/O (LVTTL/TTL)

A voltage translator is used for the (LV)TTL signals available on the front panel. The front side is either 3.3V for LVTTL or 5.0V for TTL (build option). These inputs are 5V tolerant when powered with 3.3V. The direction is controlled by the CPLD.

## 4.2 Electrical specifications

The FMC110 uses high-speed LVDS outputs. Revision 1 boards require +2.5V on VADJ power supply (supplied by the carrier card). Revision 2 boards can operate with a VADJ voltage range of 1.65V to 3.3V, but typically VADJ will be 1.8V or 2.5V for LVDS operation.

The voltage on VIO_B pins will be at the same level as VADJ as it is connected directly to VADJ on the FMC110.

The data converters operate in LVDS mode (clock and data pairs). All other status and control signals, like serial communication busses, operate at LVCMOS level ($V_{OH}$ = VADJ).

### 4.2.1 EEPROM

The FMC110 card carries a 2Kbit EEPROM which is accessible from the carrier card through the $I^2C$ bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01µA when SCL and SDA are kept at 3P3VAUX level. These signals may also be left floating since pull-up resistors are present on the card.

### 4.2.2 JTAG

The CPLD device is included in the JTAG chain accessible from the FMC connection. The user should **NOT** reprogram or erase the CPLD.

### 4.2.3 FMC HPC

The high-pin count connector has four dedicated LVDS clock pairs and can host up to 80 LVDS (data) pairs. Refer to appendix A for a detailed pin-out.

| | # Pairs | # Clock pairs | # Data pairs |
|---|---|---|---|
| **LVDS Clock** | 1 | 1 | |
| **LVDS Trigger** | 1 | 1 | |
| **LVDS Sync** | 1 | 1 | |
| **ADC #1 (port A)** | | | 14 |
| LVDS Clock | 1 | | |
| LVDS Data | 12 | | |
| LVDS Ovr / LVDS Sync | 1 | | |
| **ADC #1 (port B)** | | | 13 |
| LVDS Clock | 0 | | |
| LVDS Data | 12 | | |
| LVDS Ovr / LVDS Sync | 1 | | |
| **ADC #2 (port A)** | | | 14 |
| LVDS Clock | 1 | | |
| LVDS Data | 12 | | |
| LVDS Ovr / LVDS Sync | 1 | | |
| **DAC #1** | | | 18 |
| LVDS Clock | 1 | | |
| LVDS Sync | 1 | | |
| LVDS Data | 16 | | |
| **DAC #2** | | | 17 |
| LVDS Clock | 1 | | |
| LVDS Sync | 0 | | |
| LVDS Data | 16 | | |
| **2.5V or VADJ level I/O routed to CPLD (see board revision)** | | | 2 (4) |
| **2.5V or VADJ level I/O routed to FRONT (see board revision)** | | | 2 (4) |
| | | | |
| | **# Total pairs** | **3** | **80** |

**Table 3. HPC signal usage**[1]

[1] Signal CLK3_BIDIR_P/N is not connected.

## Main characteristics

| Analog inputs | |
|---|---|
| **Number of channels** | 2 |
| **Channel resolution** | 12-bit |
| **Input voltage range** | Max. 1.5Vp-p to 2.0Vp-p (programmable)<br>Contact Abaco for a 1Vp-p option to match the A/D input voltage range with the D/A output voltage range. |
| **Input impedance** | 50Ω AC-coupled |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **Analogue input bandwidth** | 2 GHz (TBD) |
| **Performance (Fin = 400 MHz)** | ENOB = 8.8 bit, SFDR = 64 dBc, SNRFS = 57 dB |
| **Calibration** | Gain ±24%<br>Offset ±30mV<br>Phase 0-72ps |
| **Analog outputs** | |
| **Output voltage range** | Max. 1.0Vp-p |
| **Load** | 50Ω |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **Performance (Fout = 400 MHz)** | TBD |
| **Analogue Bandwidth** | Max. 500MHz |
| **External Clock/Reference input** | |
| **Input level** | -6dBm to +7dBm |
| **Input impedance** | 50Ω AC-coupled |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **Input range** | 10 – 100 MHz (reference clock)<br>100 – 1000 MHz (sample clock) |
| **External Trigger/Sync input** | |
| **Input threshold level** | 1.25V typical (LVTTL level supported) |
| **Input impedance** | 2.5kΩ DC-coupled |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **Frequency range** | Up to 625 MHz |
| **ADC Output** | |
| **Output data width** | 1-bus mode, 1x 12-pairs DDR 1Gbps<br>2-bus mode, 2x 12-pairs DDR 500Mbps |
| **Data Format** | Two's Complement / Offset binary |
| **FMC connector type** | HPC (ASP-134488-01) |
| **Sampling Frequency Range** | 100 – 1000 MHz |
| **Internal Clock/Reference** | |
| **Format** | LVPECL |

| | |
|---|---|
| **Frequency Range** | 100 MHz (reference clock)<br>100, 125, 200, 250, 500, or 1000 MHz (sample clock)<br>(contact Abaco for customized frequencies) |

**Table 4 : FMC110 daughter card main characteristics**

## 4.3 Analog input channels

The FMC110 has two single-ended analog inputs AC-coupled to the A/D devices. A wideband RF transformer (TC1-1-13M, 4.5-3000MHz) is used. The maximum input voltage range is programmable in the A/D device from $1.5V_{P-P}$ to $2.0V_{P-P}$.

## 4.4 Analog output channels

The FMC110 has two single-ended analog outputs that are AC-coupled from the D/A device. An RF transformer (TC4-1W, 3-800MHz) is used. The analog outputs are designed to drive a 50Ω load. The maximum output voltage range is $1.0V_{P-P}$.

## 4.5 External clock input

The external clock input can be configured in two ways (see also Figure 5):

1. Sample clock input, connecting to the clock input of the AD9517.
2. Reference clock input, connecting to the reference input of the AD9517.

## 4.6 External trigger/sync input

The external trigger input can be configured in different ways (build options). The trigger input can be 50Ω terminated to accep most common high-speed signalling standards like single-ended LVPECL. By default, the 50Ω termination is not mounted in order to support LVTTL/LVCMOS and similar input standards. Differential input is also possible using the coax shield as inverted signal. By default, the input is single-ended and DC-coupled with an input impedance of approximately 2.5kΩ. The input threshold is approximately 1.25V.

The trigger input can also be used as sync input to synchronize local A/D converters or multiple FMC110 cards.

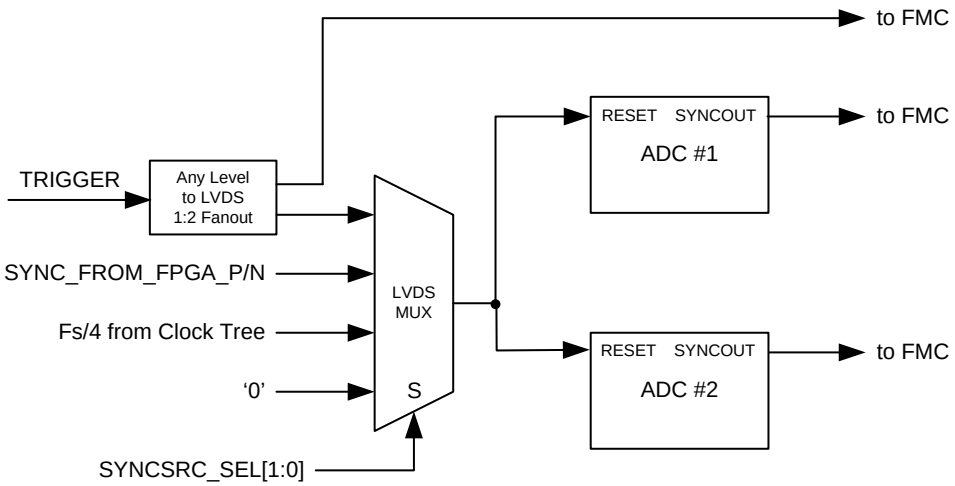



**Figure 3: A/D Synchronization topology**

To correctly align the digital output samples (when A/D in 2-bus mode or two A/D parallel), a reset signal needs to be generated. This can be a single pulse, a repetitive pulse, or a low-to-high step. The reset input generates a pulse on the sync output. The carrier hardware must use these sync pulses to correctly align the digital output samples.

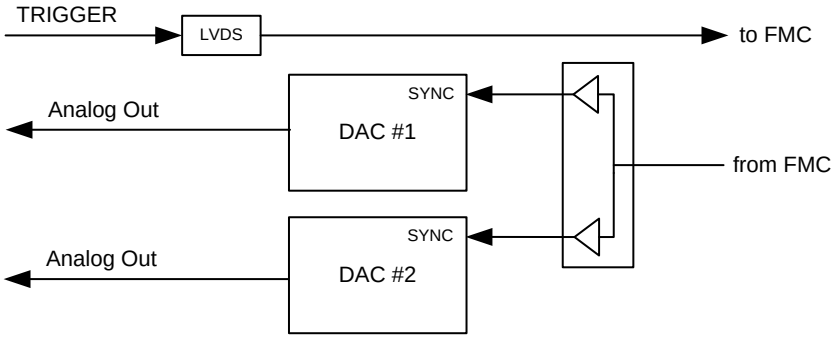



**Figure 4: D/A Synchronization topology**

Synchronization of multiple D/A devices in parallel is done through the SYNC input. The SYNC signal is driven by the FPGA. It can also be derived from the trigger input. Since the SYNC input has an internal 100R termination resistor, a 1: 2 fan-out buffer is used to connect a single LVDS signal to both D/A converters.

## 4.7 Clock Tree

The FMC110 offers a clock architecture that combines flexibility and high performance. Components have been chosen to minimize jitter and phase noise to reduce degradation of the data conversion performance. The user may choose to use an external or internal sampling clock.

The clock tree has a PLL and clock distribution section. The PLL ensures locking of the internal clock to an externally supplied reference. An onboard reference is used if no external is reference present.

A VC(X)O is used as internal clock source and can connect to the distribution section instead of the external clock input. The distribution section drives the A/D and D/A devices with the LVPECL outputs. One LVDS clock output is connected to the FMC connector as a reference for the digital data transferred to the D/A devices. One LVDS clock output connects to the synchronization circuitry.

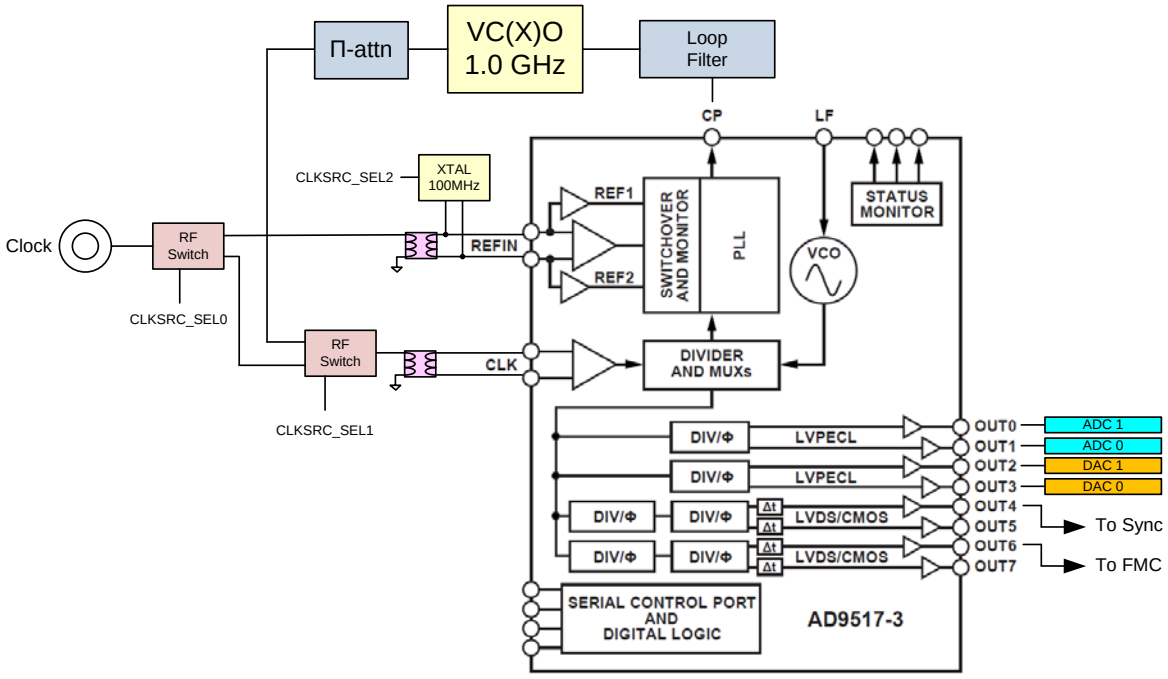



**Figure 5: Clock tree**

### 4.7.1 Control

The AD9517 supports polarity change on the LVPECL outputs. This enables parallel operation of the A/D converters. See section 4.11.

The clock tree contains two RF switches (ADG918) and requires the following control signals (driven from the CPLD):

- CLKSRC_SEL0 connects the external clock input to the reference input of the AD9517 or the 2nd RF switch.
- CLKSRC_SEL1 connect either the onboard VCXO or the external clock to the clock input of the AD9510. This signal also controls the VCXO power supply[2].
- CLKSRC_SEL2 enables/disables the onboard reference oscillator.

## 4.8 Multi-Gigabit Transceivers (revision 1 only)

The FMC110 connector hosts 10 MGT pairs (10 Tx and 10 Rx pairs). These are connected to two 38-pin MICTOR headers. The arrangement is such that different interconnect topologies are supported:

[2] The VCXO should be powered down to avoid interference with the external clock when external clock is used.

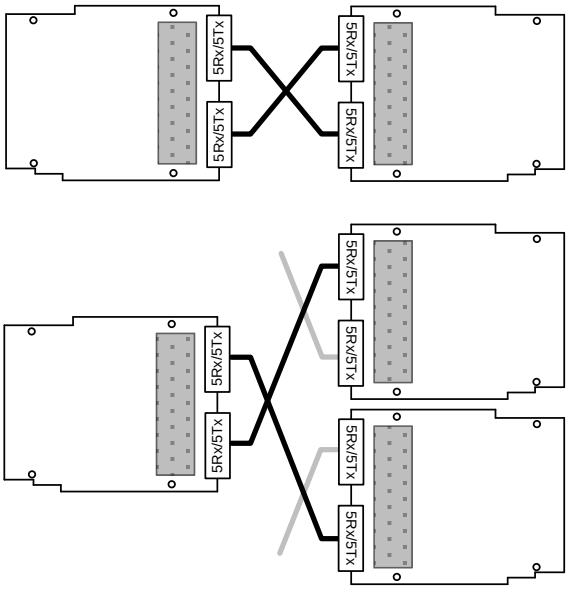



**Figure 6: MGT interconnect topologies**

**TOP VIEW**

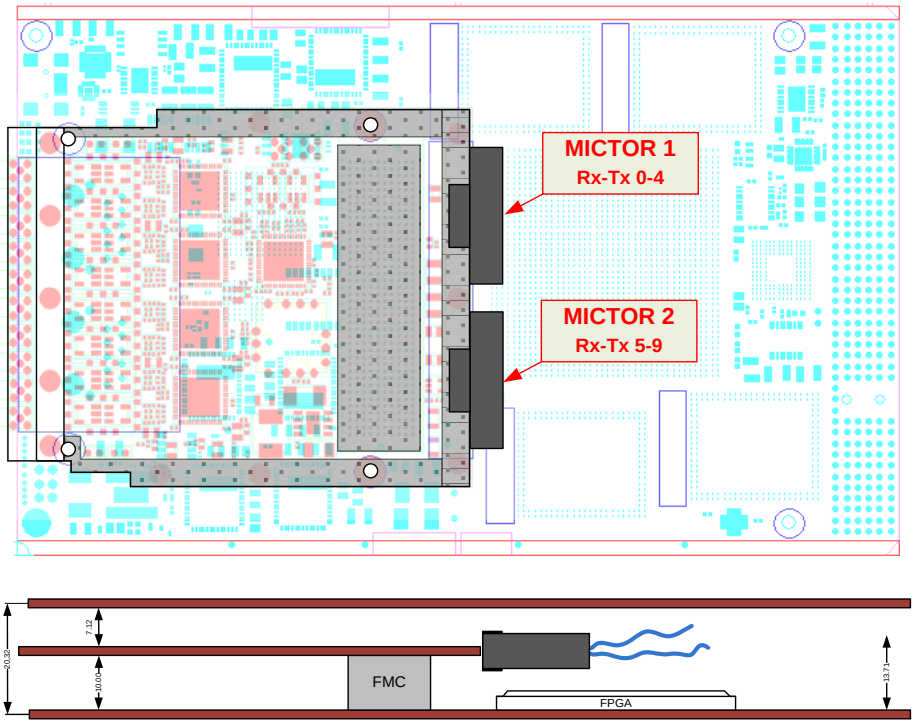



**Figure 7: Abaco CPCI board stack (slot-to-slot)**

| MICTOR 1 | | | | |
|---|---|---|---|---|
| Pin | Signal | Midplate | Signal | Pin |
| 1 | GND | GND | GND | 2 |
| 3 | TX0_P* | GND | RX0_P* | 4 |
| 5 | TX0_N* | GND | RX0_N* | 6 |
| 7 | GND | GND | GND | 8 |
| 9 | TX1_P* | GND | RX1_P* | 10 |
| 11 | TX1_N* | GND | RX1_N* | 12 |
| 13 | GND | GND | GND | 14 |
| 15 | TX2_P* | GND | RX2_P* | 16 |
| 17 | TX2_N* | GND | RX2_N* | 18 |
| 19 | GND | GND | GND | 20 |
| 21 | TX3_P* | GND | RX3_P* | 22 |
| 23 | TX3_N* | GND | RX3_N* | 24 |
| 25 | GND | GND | GND | 26 |
| 27 | TX4_P | GND | RX4_P | 28 |
| 29 | TX4_N | GND | RX4_N | 30 |
| 31 | GND | GND | GND | 32 |
| 33 | IO0 | GND | | 34 |
| 35 | IO1 | GND | | 36 |
| 37 | GND | GND | GND | 38 |

| MICTOR 2 | | | | |
|---|---|---|---|---|
| Pin | Signal | Midplate | Signal | Pin |
| 1 | GND | GND | GND | 2 |
| 3 | RX9_P | GND | TX9_P | 4 |
| 5 | RX9_N | GND | TX9_N | 6 |
| 7 | GND | GND | GND | 8 |
| 9 | RX8_P | GND | TX8_P | 10 |
| 11 | RX8_N | GND | TX8_N | 12 |
| 13 | GND | GND | GND | 14 |
| 15 | RX7_P | GND | TX7_P | 16 |
| 17 | RX7_N | GND | TX7_N | 18 |
| 19 | GND | GND | GND | 20 |
| 21 | RX6_P | GND | TX6_P | 22 |
| 23 | RX6_N | GND | TX6_N | 24 |
| 25 | GND | GND | GND | 26 |
| 27 | RX5_P | GND | TX5_P | 28 |
| 29 | RX5_N | GND | TX5_N | 30 |
| 31 | GND | GND | GND | 32 |
| 33 | IO2 | GND | | 34 |
| 35 | IO3 | GND | | 36 |
| 37 | GND | GND | GND | 38 |

**Table 5: MGT connector pin out[3]**

A low phase noise 125MHz XTAL is used as reference clock. A 1:2 LVDS fan-out buffer is used to feed the reference clock to both connections on the FMC connector.

The pairs marked with * connect to either the MICTOR header or the HDMI connector. The assembly is determined with 0Ω resistors. A maximum of four pairs can connect to the HDMI connector. Contact Abaco for custom configurations.

**N.B.** These connectors are not available on the FMC110 revision 2.

## 4.9 Power supply

Power is supplied to the FMC110 card through the FMC connector. The pin current rating is 2.7A, but the overall maximum as specified by the FMC standard is limited according to Table 6.

[3] Signals IO[0:3] connects to the CPLD and has no defined function yet.

| Voltage | # pins | Max Amps | Max Watt |
|---|---|---|---|
| +3.3V | 4 | 3 A | 10 W |
| +12V | 2 | 1 A | 12 W |
| VADJ (+2.5V) | 4 | 4 A | 10 W |
| VIO_B (+2.5V) | 2 | 1.15 A | 2.3 W |

**Table 6: FMC standard power specification**

The power provided by the carrier card can be very noisy. Special care is taken with the power supply generation on the FMC110 card to minimize the effect of power supply noise on clock generation and data conversion.

Clean analog supply is derived from +12V in two steps for maximum efficiency. The first step uses a highly efficient switched regulator. From this power rail, the analog supply is derived with low dropout, low noise, high PSRR, and linear regulators. There is additional noise filtering at several stages in the power supply.

The regulators have sufficient copper area to dissipate the heat in combination with proper airflow (see section 6.3 Cooling).

| Power plane | Typical | Maximum |
|---|---|---|
| VADJ | 674 mA | |
| 3P3V | 105 mA | |
| 12P0V | 913 mA | |
| 3P3VAUX (Operating)<br>3P3VAUX (Standby) | 0.1 mA<br>0.01 µA | 3 mA<br>1 µA |

**Table 7a: Typical/Maximum current drawn from FMC110 revision 1**

| Power plane | Typical | Maximum |
|---|---|---|
| VADJ | 25 mA | |
| 3P3V | 590 mA | |
| 12P0V | 913 mA | |
| 3P3VAUX (Operating)<br>3P3VAUX (Standby) | 0.1 mA<br>0.01 µA | 3 mA<br>1 µA |

**Table 8b: Typical/Maximum current drawn from FMC110 revision 2**

The total power consumption: 12W

## 4.10 Parallel A/D operation (Fs up to 2GHz)

Both A/D converters can operate in parallel, capturing the same signal, but they are clocked with 180 degree clock phase difference. The out of phase clocks are generated locally. The analog signal needs to be split externally.

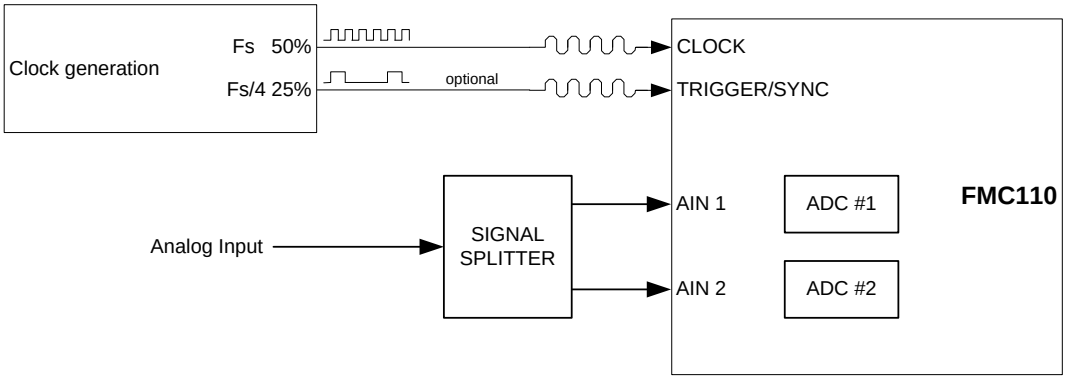



**Figure 8: Parallel A/D operation**

Gain, phase, and offset errors may be compensated by the calibration features of the ADS5400 if the programmability range is not exceeded (refer to Table 4).

The INL (integral non-linearity) of the converters needs to be taken into account. INL represents the number of LSBs the output of a converter is from the expected output for a given input voltage. For example, if a converter would ideally put out a code of N for an input voltage M, but actually puts out a code N+2, then the INL at that point is two. The ADS5400 has an INL of ±2 LSB (±4 LSB maximum). When interleaving converters, the output codes could differ by as much as 8 LSB for the same input voltage and may drastically reduce the number of effective bits.

A single device has a typical performance of 57dBFS (Fin= 1.2GHz). The INL specification of the ADS5400 makes high-performance interleaving difficult. A very rough estimation is that the SNR can decrease below 50dBFS, even if phase, offset, and gain calibration have been performed. INL problems can partly be corrected in the digital domain, but may require lengthy calibration.

## 4.11 Synchronizing multiple cards

To synchronize multiple cards, they need to be supplied with synchronized clock signals. In addition, an external synchronization signal is required to align the samples in the digital domain. Refer to section 4.7 for details about synchronisation.

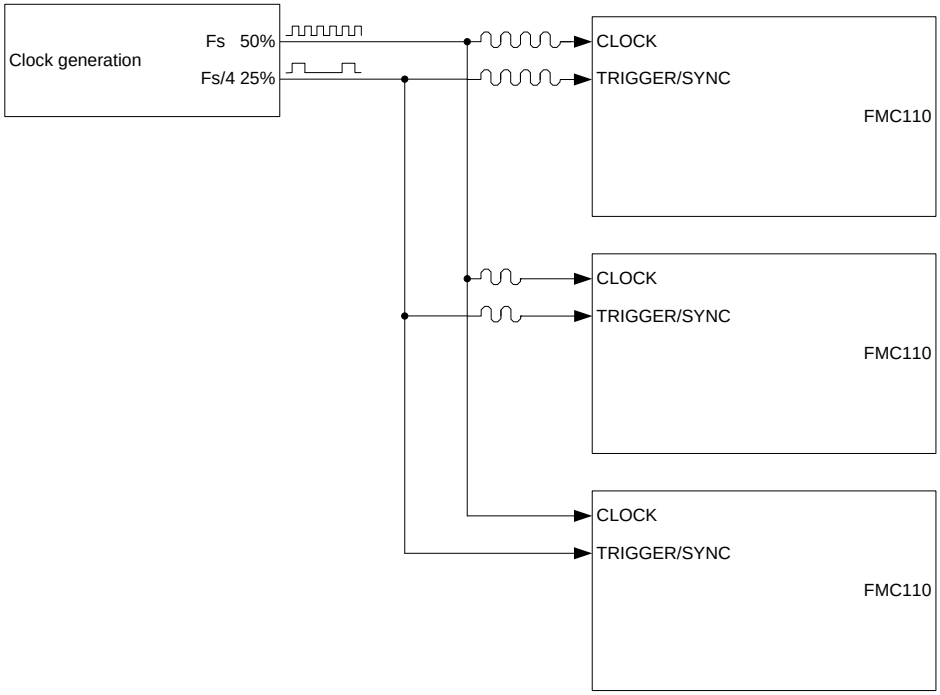



**Figure 9: Synchronizing multiple cards**

# 5 Controlling the FMC110

## 5.1 Architecture

The FMC needs to be controlled from the carrier hardware through a single SPI communication bus. The SPI communication bus is connected to a CPLD which has the following tasks:

- Distribute SPI access from the carrier hardware along the local devices:
  - 2x ADS5400 (A/D converters)
  - 2x DAC5681Z (D/A converters)
  - 1x AD9517 (Clock Tree)
- Select clock source based on a SPI command from the carrier hardware (CLKSRC_SEL).
- Select sync source based on a SPI command from the carrier hardware (SYNCSRC_SEL).
- Generate SPI reset for AD9517 (CLK_N_RESET) and both DAC5681Z (DAC_N_RESET)
- Control the direction of the front I/O transceivers (FRONT_IO_DIR).
- Control the FAN header power (FAN_N_EN).
- Collect local status signals and store them in a register which can be accessed from the carrier hardware.
- Drive a LED according to the level of the status signals.

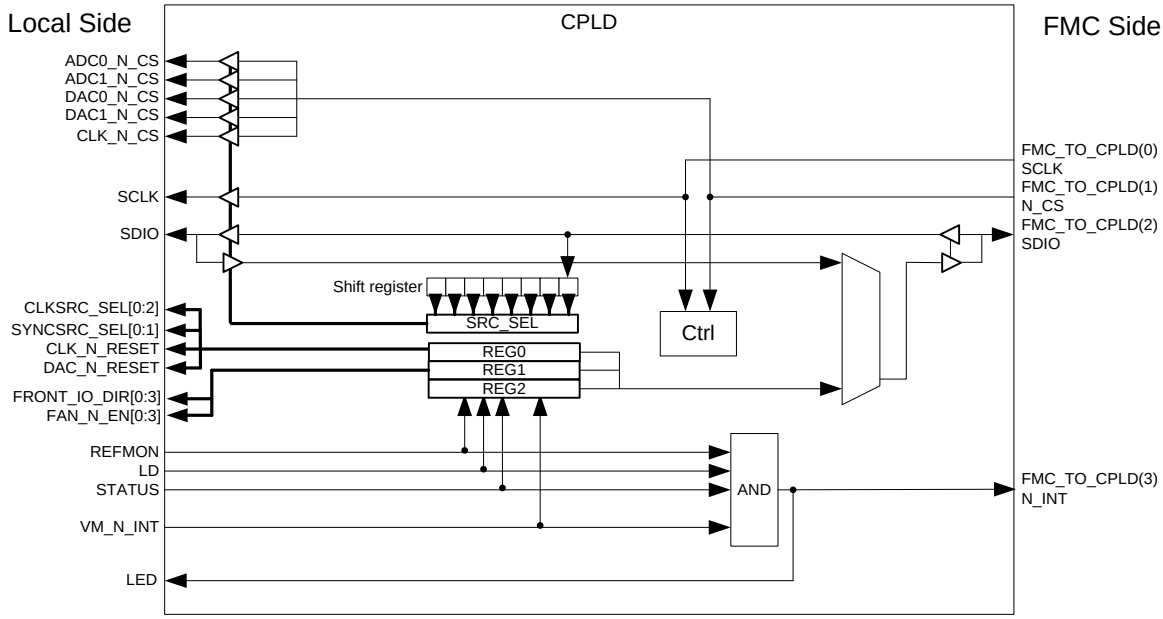



**Figure 10: CPLD architecture**

**Notes:**

- SDO on the AD9517, ADS5400, and DAC5681Z devices is not connected. SDIO is used bidirectional (3-wire SPI)
- N_PD on the AD9517 is not connected.
- N_SYNC on the AD9517 on the revision 1 boards is not connected. On revision 2 boards N_SYNC is connected to the CPLD for future use.
- ENA1BUS and ENPWD on the ADS5400 are not connected.
- N_RESET on the both DAC5681Z devices is shared.

## 5.2 SPI Programming

The SPI programmable devices on the FMC110 can be accessed as described in their datasheet, but each SPI communication cycle needs to be preceded with a preselection byte. The preselection byte is used by the CPLD to forward the SPI command to the right destination. The preselection bytes are defined as follows:

- CPLD 0x00
- ADS5400 #1 0x80
- ADS5400 #2 0x81
- DAC5681Z #1 0x82
- DAC5681Z #2 0x83
- AD9517 0x84

The CLPD has three internal registers which are described in Appendix B CPLD Register map. The registers of the other devices are transparently mapped.

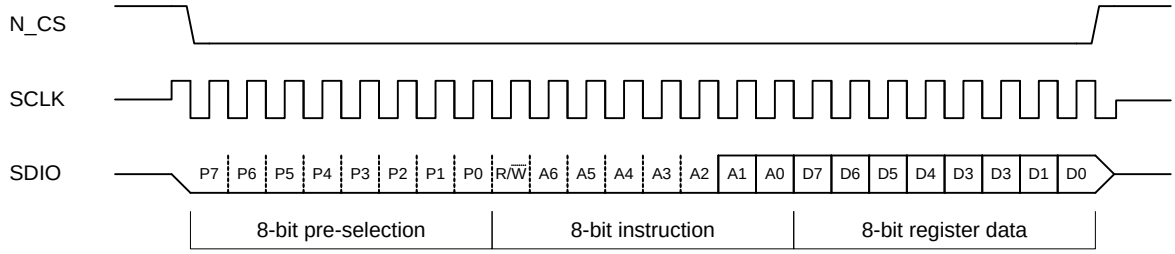



**Figure 11: Write instruction to CPLD registers A1:A0**

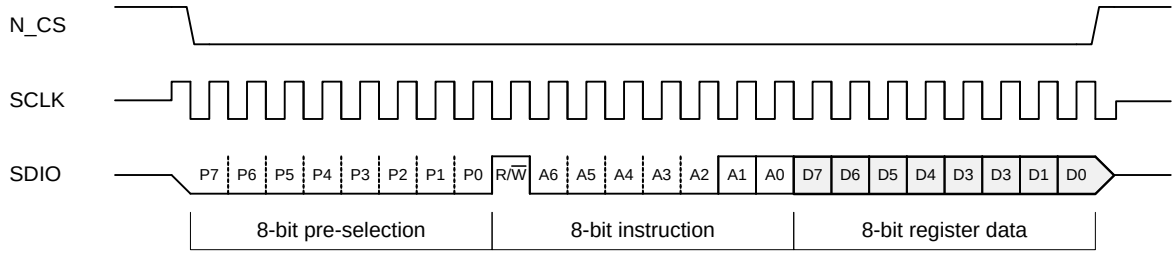



**Figure 12: Read instruction to CPLD registers A1:A0**

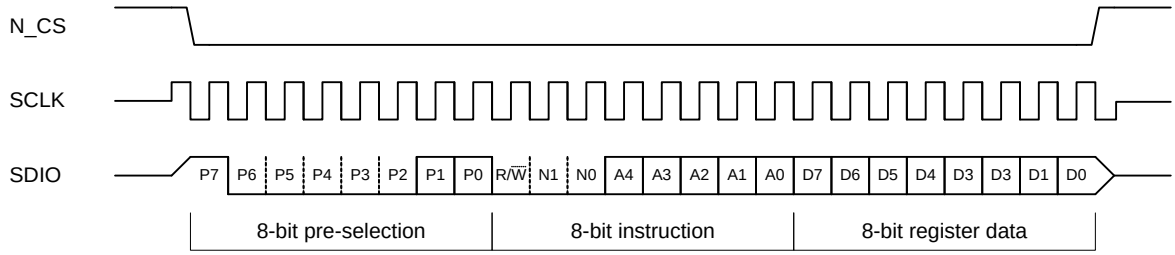



**Figure 13: Write instruction to ADS5400 / DAC5681Z registers A4:A0**

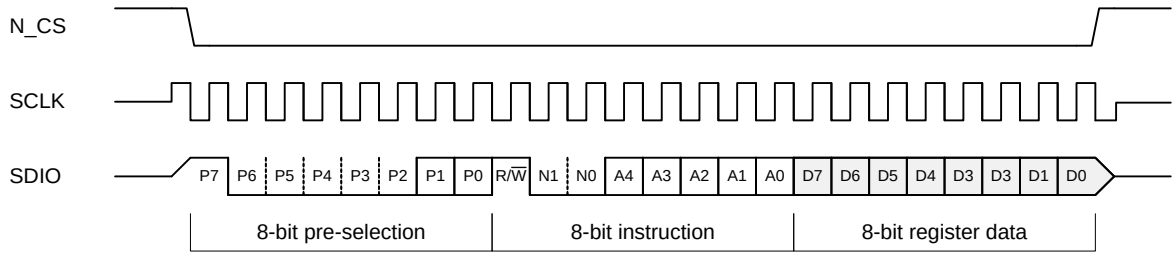



**Figure 14. Read instruction to ADS5400 / DAC5681Z registers A4:A0**

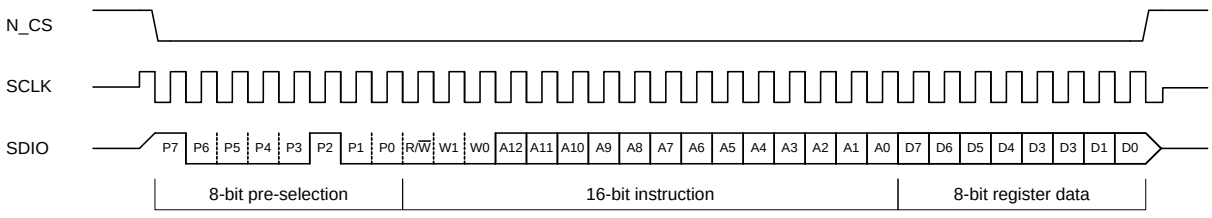



**Figure 15: Write instruction to AD9517 registers A12:A0**

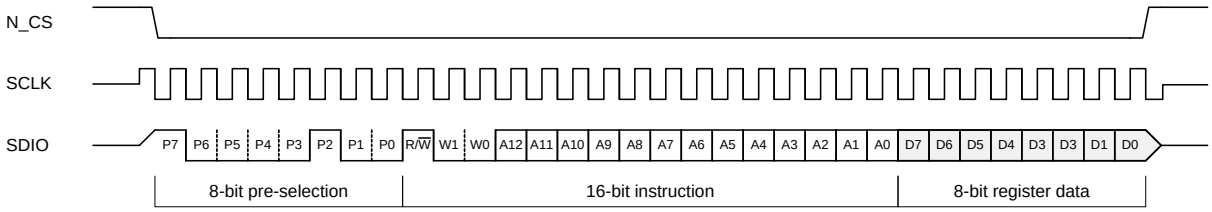



**Figure 16: Read instruction to AD9517 registers A12:A0**

# 6 Environment

## 6.1 Temperature

Operating temperature:

- -40˚C to +85˚C (Industrial)

Storage temperature:

- -40˚C to +120˚C

## 6.2 Monitoring

The onboard monitoring may be used to monitor the voltage on the different power rails as well as the temperature of the A/D devices. The onboard monitoring device is the ADT7411.

It is recommended that the carrier card and/or host software uses the power-down features if the temperature is too high. Normal operations can resume once the temperature is within the operating conditions boundaries.

| Parameter: | ADT7411 address 1001 000 | Formula |
|---|---|---|
| On-chip temperature | | |
| On-chip AIN0 ($V_{DD}$) | +3.3V | |
| External AIN1 | +3.3V Analog CLK | AIN1 * 2 |
| External AIN2 | +1.8V Digital | AIN2 |
| External AIN3 | VADJ | AIN3 |
| External AIN4 | +2.5V Analog CLK | AIN4 |
| External AIN5 | +3.3V Digital | AIN5 * 2 |
| External AIN6 | +3.3V Analog ADC | AIN6 * 2 |
| External AIN7 | +3.3V VCP | AIN7 * 2 |
| External AIN8 | +12V | AIN8 * 7.04 |

**Table 9: Temperature and voltage parameters**

## 6.3 Cooling

Two different types of cooling are available for the FMC110.

### 6.3.1 Convection cooling

The air flow provided by the fans of the chassis the FMC110 is enclosed in will dissipate the heat generated by the onboard components. A minimum airflow of 300 LFM is recommended.

Optionally, low profile FANs can be glued on top of the A/D devices. The card has a FAN power connection that can be switched on and off under carrier card control (individually driven from the CPLD).

For standalone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC to ensure that the temperature of the devices is within the allowed range. Abaco's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

### 6.3.2 Conduction cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions the junction temperature of power consuming devices will exceed the operating conditions recommended by the devices manufacturers (mostly +85˚C).

The FMC110 is designed for maximum heat transfer to conduction-cooled ribs. A customized cooling frame that connects directly to the surface of the A/D devices is allowed. This conduction cooling mechanism should be applied in combination with proper chassis air flow. Contact Abaco for detailed mechanical information.

# 7 Safety

This module presents no hazard to the user.

# 8 EMC

This module is designed to operate within an enclosed host system built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

# 9 Warranty

| | *Hardware* | *Software/Firmware* |
|---|---|---|
| Basic Warranty (included) | 1 Year from Date of Shipment | 90 Days from Date of Shipment |
| Extended Warranty (optional) | 2 Years from Date of Shipment | 1 Year from Date of Shipment |

# Appendix A HPC pin-out FMC110

| AV57.1 | HPC Pin | FMC110 Signal | AV57.1 | HPC Pin | FMC110 Signal | AV57.1 | HPC Pin | FMC110 Signal |
|---|---|---|---|---|---|---|---|---|
| CLK0_M2C_N | H5 | CLK_TO_FPGA_N | HA00_N_CC | F5 | ADC1_OVRA_N | HB10_N | K32 | DAC1_DATA_P<4> |
| CLK0_M2C_P | H4 | CLK_TO_FPGA_P | HA00_P_CC | F4 | ADC1_OVRA_P | HB10_P | K31 | DAC1_DATA_N<4> |
| CLK1_M2C_N | G3 | TRIGGER_TO_FPGA_N | HA01_N_CC | E3 | ADC0_CLKA_N | HB11_N | J31 | DAC1_DATA_P<5> |
| CLK1_M2C_P | G2 | TRIGGER_TO_FPGA_P | HA01_P_CC | E2 | ADC0_CLKA_P | HB11_P | J30 | DAC1_DATA_N<5> |
| CLK2_BIDIR_N | K5 | SYNC_FROM_FPGA_N | HA02_N | K8 | ADC0_DA_N<8> | HB12_N | F32 | DAC1_DATA_P<3> |
| CLK2_BIDIR_P | K4 | SYNC_FROM_FPGA_P | HA02_P | K7 | ADC0_DA_P<8> | HB12_P | F31 | DAC1_DATA_N<3> |
| CLK3_BIDIR_N | J3 | N.C. | HA03_N | J7 | ADC0_DA_N<10> | HB13_N | E31 | DAC1_DATA_P<6> |
| CLK3_BIDIR_P | J2 | N.C. | HA03_P | J6 | ADC0_DA_P<10> | HB13_P | E30 | DAC1_DATA_N<6> |
| LA00_N_CC | G7 | ADC0_DB_N<9> | HA04_N | F8 | ADC0_DA_N<9> | HB14_N | K35 | DAC1_DATA_P<1> |
| LA00_P_CC | G6 | ADC0_DB_P<9> | HA04_P | F7 | ADC0_DA_P<9> | HB14_P | K34 | DAC1_DATA_N<1> |
| LA01_N_CC | D9 | ADC0_DA_N<7> | HA05_N | E7 | ADC0_DA_N<11> | HB15_N | J34 | DAC1_DATA_P<2> |
| LA01_P_CC | D8 | ADC0_DA_P<7> | HA05_P | E6 | ADC0_DA_P<11> | HB15_P | J33 | DAC1_DATA_N<2> |
| LA02_N | H8 | ADC0_DB_N<7> | HA06_N | K11 | ADC0_DA_N<5> | HB16_N | F35 | DAC1_DATA_P<0> |
| LA02_P | H7 | ADC0_DB_P<7> | HA06_P | K10 | ADC0_DA_P<5> | HB16_P | F34 | DAC1_DATA_N<0> |
| LA03_N | G10 | ADC0_DB_N<8> | HA07_N | J10 | ADC0_DA_N<0> | HB17_N_CC | K38 | ADC0_DB_N<1> |
| LA03_P | G9 | ADC0_DB_P<8> | HA07_P | J9 | ADC0_DA_P<0> | HB17_P_CC | K37 | ADC0_DB_P<1> |
| LA04_N | H11 | ADC0_DB_N<6> | HA08_N | F11 | ADC0_DA_N<1> | HB18_N | J37 | ADC0_DB_N<0> |
| LA04_P | H10 | ADC0_DB_P<6> | HA08_P | F10 | ADC0_DA_P<1> | HB18_P | J36 | ADC0_DB_P<0> |
| LA05_N | D12 | ADC0_DA_N<3> | HA09_N | E10 | ADC0_DA_N<6> | HB19_N | E34 | ADC0_DB_N<5> |
| LA05_P | D11 | ADC0_DA_P<3> | HA09_P | E9 | ADC0_DA_P<6> | HB19_P | E33 | ADC0_DB_P<5> |
| LA06_N | C11 | ADC0_OVRA_N | HA10_N | K14 | ADC0_DA_N<4> | HB20_N | F38 | FRONT_IO<1> |
| LA06_P | C10 | ADC0_OVRA_P | HA10_P | K13 | ADC0_DA_P<4> | HB20_P | F37 | FRONT_IO<0> |
| LA07_N | H14 | ADC0_DA_N<2> | HA11_N | J13 | ADC1_DA_N<10> | HB21_N | E37 | FRONT_IO<3> |
| LA07_P | H13 | ADC0_DA_P<2> | HA11_P | J12 | ADC1_DA_P<10> | HB21_P | E36 | FRONT_IO<2> |
| LA08_N | G13 | DAC_SYNC_N | HA12_N | F14 | ADC1_DA_N<8> | GBTCLK0_M2C_N | D5 | GBTCLK0_N |
| LA08_P | G12 | DAC_SYNC_P | HA12_P | F13 | ADC1_DA_P<8> | GBTCLK0_M2C_P | D4 | GBTCLK0_P |
| LA09_N | D15 | FMC_TO_CPLD<1> | HA13_N | E13 | ADC1_DA_N<11> | GBTCLK1_M2C_N | B21 | GBTCLK1_N |
| LA09_P | D14 | FMC_TO_CPLD<0> | HA13_P | E12 | ADC1_DA_P<11> | GBTCLK1_M2C_P | B20 | GBTCLK1_P |
| LA10_N | C15 | FMC_TO_CPLD<3> | HA14_N | J16 | ADC1_DA_N<9> | DP0_C2M_N | C3 | DP_C2M_N<0> |
| LA10_P | C14 | FMC_TO_CPLD<2> | HA14_P | J15 | ADC1_DA_P<9> | DP0_C2M_P | C2 | DP_C2M_P<0> |
| LA11_N | H17 | ADC0_DB_N<10> | HA15_N | F17 | ADC1_DA_N<2> | DP0_M2C_N | C7 | DP_M2C_N<0> |
| LA11_P | H16 | ADC0_DB_P<10> | HA15_P | F16 | ADC1_DA_P<2> | DP0_M2C_P | C6 | DP_M2C_P<0> |
| LA12_N | G16 | DAC0_DATA_P<15> | HA16_N | E16 | ADC1_DA_N<7> | DP1_C2M_N | A23 | DP_C2M_N<1> |
| LA12_P | G15 | DAC0_DATA_N<15> | HA16_P | E15 | ADC1_DA_P<7> | DP1_C2M_P | A22 | DP_C2M_P<1> |
| LA13_N | D18 | DAC0_DATA_P<14> | HA17_N_CC | K17 | ADC1_CLKA_N | DP1_M2C_N | A3 | DP_M2C_N<1> |
| LA13_P | D17 | DAC0_DATA_N<14> | HA17_P_CC | K16 | ADC1_CLKA_P | DP1_M2C_P | A2 | DP_M2C_P<1> |
| LA14_N | C19 | DAC0_DATA_P<13> | HA18_N | J19 | ADC1_DA_N<4> | DP2_C2M_N | A27 | DP_C2M_N<2> |
| LA14_P | C18 | DAC0_DATA_N<13> | HA18_P | J18 | ADC1_DA_P<4> | DP2_C2M_P | A26 | DP_C2M_P<2> |
| LA15_N | H20 | DAC0_DATA_P<12> | HA19_N | F20 | ADC1_DA_N<3> | DP2_M2C_N | A7 | DP_M2C_N<2> |
| LA15_P | H19 | DAC0_DATA_N<12> | HA19_P | F19 | ADC1_DA_P<3> | DP2_M2C_P | A6 | DP_M2C_P<2> |
| LA16_N | G19 | ADC0_DB_N<11> | HA20_N | E19 | ADC1_DA_N<0> | DP3_C2M_N | A31 | DP_C2M_N<3> |
| LA16_P | G18 | ADC0_DB_P<11> | HA20_P | E18 | ADC1_DA_P<0> | DP3_C2M_P | A30 | DP_C2M_P<3> |
| LA17_N_CC | D21 | ADC0_DB_N<3> | HA21_N | K20 | ADC1_DA_N<6> | DP3_M2C_N | A11 | DP_M2C_N<3> |
| LA17_P_CC | D20 | ADC0_DB_P<3> | HA21_P | K19 | ADC1_DA_P<6> | DP3_M2C_P | A10 | DP_M2C_P<3> |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LA18_N_CC | C23 | ADC0_DB_N<4> | HA22_N | J22 | ADC1_DA_N<5> | DP4_C2M_N | A35 | DP_C2M_N<4> |
| LA18_P_CC | C22 | ADC0_DB_P<4> | HA22_P | J21 | ADC1_DA_P<5> | DP4_C2M_P | A34 | DP_C2M_P<4> |
| LA19_N | H23 | DAC0_DATA_P<10> | HA23_N | K23 | ADC1_DA_N<1> | DP4_M2C_N | A15 | DP_M2C_N<4> |
| LA19_P | H22 | DAC0_DATA_N<10> | HA23_P | K22 | ADC1_DA_P<1> | DP4_M2C_P | A14 | DP_M2C_P<4> |
| LA20_N | G22 | DAC0_DATA_P<11> | HB00_N_CC | K26 | DAC1_DATA_P<11> | DP5_C2M_N | A39 | DP_C2M_N<5> |
| LA20_P | G21 | DAC0_DATA_N<11> | HB00_P_CC | K25 | DAC1_DATA_N<11> | DP5_C2M_P | A38 | DP_C2M_P<5> |
| LA21_N | H26 | ADC0_DB_N<2> | HB01_N | J25 | DAC1_DATA_P<12> | DP5_M2C_N | A19 | DP_M2C_N<5> |
| LA21_P | H25 | ADC0_DB_P<2> | HB01_P | J24 | DAC1_DATA_N<12> | DP5_M2C_P | A18 | DP_M2C_P<5> |
| LA22_N | G25 | DAC0_DATA_P<8> | HB02_N | F23 | DAC1_DATA_P<14> | DP6_C2M_N | B37 | DP_C2M_N<6> |
| LA22_P | G24 | DAC0_DATA_N<8> | HB02_P | F22 | DAC1_DATA_N<14> | DP6_C2M_P | B36 | DP_C2M_P<6> |
| LA23_N | D24 | DAC0_DATA_P<9> | HB03_N | E22 | DAC1_DATA_P<15> | DP6_M2C_N | B17 | DP_M2C_N<6> |
| LA23_P | D23 | DAC0_DATA_N<9> | HB03_P | E21 | DAC1_DATA_N<15> | DP6_M2C_P | B16 | DP_M2C_P<6> |
| LA24_N | H29 | DAC0_DATA_P<6> | HB04_N | F26 | DAC1_DATA_P<10> | DP7_C2M_N | B33 | DP_C2M_N<7> |
| LA24_P | H28 | DAC0_DATA_N<6> | HB04_P | F25 | DAC1_DATA_N<10> | DP7_C2M_P | B32 | DP_C2M_P<7> |
| LA25_N | G28 | DAC0_DATA_P<7> | HB05_N | E25 | DAC1_DATA_P<13> | DP7_M2C_N | B13 | DP_M2C_N<7> |
| LA25_P | G27 | DAC0_DATA_N<7> | HB05_P | E24 | DAC1_DATA_N<13> | DP7_M2C_P | B12 | DP_M2C_P<7> |
| LA26_N | D27 | DAC0_DCLK_N | HB06_N_CC | K29 | DAC1_DCLK_N | DP8_C2M_N | B29 | DP_C2M_N<8> |
| LA26_P | D26 | DAC0_DCLK_P | HB06_P_CC | K28 | DAC1_DCLK_P | DP8_C2M_P | B28 | DP_C2M_P<8> |
| LA27_N | C27 | DAC0_DATA_P<5> | HB07_N | J28 | DAC1_DATA_P<8> | DP8_M2C_N | B9 | DP_M2C_N<8> |
| LA27_P | C26 | DAC0_DATA_N<5> | HB07_P | J27 | DAC1_DATA_N<8> | DP8_M2C_P | B8 | DP_M2C_P<8> |
| LA28_N | H32 | DAC0_DATA_P<3> | HB08_N | F29 | DAC1_DATA_P<7> | DP9_C2M_N | B25 | DP_C2M_N<9> |
| LA28_P | H31 | DAC0_DATA_N<3> | HB08_P | F28 | DAC1_DATA_N<7> | DP9_C2M_P | B24 | DP_C2M_P<9> |
| LA29_N | G31 | DAC0_DATA_P<4> | HB09_N | E28 | DAC1_DATA_P<9> | DP9_M2C_N | B5 | DP_M2C_N<9> |
| LA29_P | G30 | DAC0_DATA_N<4> | HB09_P | E27 | DAC1_DATA_N<9> | DP9_M2C_P | B4 | DP_M2C_P<9> |
| LA30_N | H35 | DAC0_DATA_P<1> | | | | | | |
| LA30_P | H34 | DAC0_DATA_N<1> | | | | | | |
| LA31_N | G34 | DAC0_DATA_P<2> | | | | | | |
| LA31_P | G33 | DAC0_DATA_N<2> | | | | | | |
| LA32_N | H38 | DAC0_DATA_P<0> | | | | | | |
| LA32_P | H37 | DAC0_DATA_N<0> | | | | | | |
| LA33_N | G37 | ADC0_OVRB_N | | | | SCL | C30 | I2C_SCL |
| LA33_P | G36 | ADC0_OVRB_P | | | | SDA | C31 | I2C_SDA |

**Table 10: HPC signal description (FMC110)**

| Signal | Group | Direction | I/O Standard | Description |
|---|---|---|---|---|
| ADC0_CLKA_N<br>ADC0_CLKA_P | A/D 0 | Output | LVDS | Digital data clock from 1st ADC. This ADC can operate in mux mode, using data port A and data port B |
| ADC0_DA_N<11..0><br>ADC0_DA_P<11..0> | A/D 0 | Output | LVDS | Data port A of 1st ADC. Data is valid on both edges of ADC0_CLKA_P/N (DDR) |
| ADC0_OVRA_N<br>ADC0_OVRA_P | A/D 0 | Output | LVDS | Over-range bit synchronous to the samples present on port A of 1st ADC. Can be used as sync signal. |
| ADC0_DB_N<11..0><br>ADC0_DB_P<11..0> | A/D 0 | Output | LVDS | Data port B of 1st ADC. Data is valid on both edges of ADC0_CLKA_P/N (DDR) |
| ADC0_OVRB_N<br>ADC0_OVRB_P | A/D 0 | Output | LVDS | Over-range bit synchronous to the samples present on port B of 1st ADC. Can be used as sync signal. |
| ADC1_CLKA_N<br>ADC1_CLKA_P | A/D 1 | Output | LVDS | Digital data clock from 2nd ADC. This ADC cannot operate in mux mode, using data port A only |
| ADC1_DA_N<11..0><br>ADC1_DA_P<11..0> | A/D 1 | Output | LVDS | Data port A of 2nd ADC. Data is valid on both edges of ADC1_CLKA_P/N (DDR) |
| ADC1_OVRA_N<br>ADC1_OVRA_P | A/D 1 | Output | LVDS | Over-range bit synchronous to the samples present on port A of 2nd ADC. Can be used as sync signal. |
| SYNC_FROM_FPGA_N<br>SYNC_FROM_FPGA_P | A/D 0, A/D 1 | Input | LVDS | Signal used to apply a sync pulse to both ADCs in order to align the digital outputs on sample basis. |
| CLK_TO_FPGA_N<br>CLK_TO_FPGA_P | D/A 0, D/A 1 | Output | LVDS | Clock to be used as reference clock for generating DAC clock and data signals. Typically ½ times the sample clock frequency. |
| DAC0_DCLK_N<br>DAC0_DCLK_P | D/A 0 | Input | LVDS | Digital data clock to 1st DAC. |
| DAC0_DATA_N<15..0><br>DAC0_DATA_P<15..0> | D/A 0 | Input | LVDS | Data bus to 1st DAC. Data should be valid on both edges of DAC0_DCLK_P/N (DDR) |
| DAC1_DCLK_N | D/A 1 | Input | LVDS | Digital data clock to 2nd DAC. |

| | | | | |
|---|---|---|---|---|
| DAC1_DCLK_P | | | | |
| DAC1_DATA_N<15..0><br>DAC1_DATA_P<15..0> | D/A 1 | Input | LVDS | Data bus to 2nd DAC. Data should be valid on both edges of DAC0_DCLK_P/N (DDR) |
| DAC_SYNC_N<br>DAC_SYNC_P | D/A 0, D/A 1 | Input | LVDS | Signal used as transmit enable for both DACs. |
| TRIGGER_TO_FPGA_N<br>TRIGGER_TO_FPGA_P | TRIGGER | Output | LVDS | Representation of the signal connected to the external trigger input. |
| FMC_TO_CPLD<0> | CONTROL | Input | CMOS VIO | SPI clock connected to the CPLD |
| FMC_TO_CPLD<1> | CONTROL | Input | CMOS VIO | SPI chip select connected to the CPLD |
| FMC_TO_CPLD<2> | CONTROL | Bidir | CMOS VIO | SPI data in/out connected to the CPLD |
| FMC_TO_CPLD<3> | CONTROL | Output | CMOS VIO | Interrupt connected the CPLD (reserved for future use) |
| FRONT_IO<3..0> | I/O | Bidir | CMOS VIO | Connected to the transceivers on the HDMI connector (Table 2). The direction of the transceivers is controlled through a CPLD register. |
| I2C_SCL | CONTROL | Input | LVTTL 3.3V | I2C data, connects to the voltage monitoring and EERROM. |
| I2C_SDA | CONTROL | Bidir | LVTTL 3.3V | I2C data, connects to the voltage monitoring and EERROM. |

# Appendix B CPLD Register map

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Name | '0' | DACR | CLKR | SYNCSRC | | CLKSRC | | |

**Table 11: Register CPLD_REG0 definition**

| Field | | Description |
|---|---|---|
| **CLKSRC** | | **Selection of clock source** |
| | '000' | External clock |
| | '011' | Internal clock, External Reference |
| | '110' | Internal clock, Internal Reference |
| | others | Do not use |
| **SYNCSRC** | | **Selection of synchronisation source** |
| | '00' | External Trigger |
| | '01' | Carrier (trough SYNC_FROM_FPGA_P/N) |
| | '10' | Clock Tree |
| | '11' | No Sync |
| **CLKR** | | **Clock tree SPI reset** |
| | '0' | Normal operation |
| | '1' | Reset, resetting the clock tree is normally not required. This bit is **not** self-clearing. |
| **DACR** | | **D/A device SPI reset** |
| | '0' | Normal operation |
| | '1' | Reset, resetting the D/A device is normally not required. This bit is **not** self-clearing. |

**Table 12 Register CPLD_REG0 description**

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FAN3 | FAN2 | FAN1 | FAN0 | DIR3 | DIR2 | DIR1 | DIR0 |

**Table 13: Register CPLD_REG1 definition**

| Field | | Description |
|---|---|---|
| **DIRx** | | Direction of Front IO transceiver (x = 0 to 3) |
| | ‘0’ | Signal x is input (FMC110 is receiver) |
| | ‘1’ | Signal x is output (FMC110 is transmitter) |
| **FANx** | | Power control for FAN header (x = 0 to 3) |
| | ‘0‘ | Apply power to FAN header x |
| | ‘1‘ | Cut power to FAN header x |

**Table 14 Register CPLD_REG1 description**

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | Reserved | | | IRQ | VM | STATUS | LD | REFMON |

**Table 15: Register CPLD_REG2 definition (read)**

| Field | | Description |
|---|---|---|
| **REFMON** | | Reflect the status of the REFMON output of the AD9517 |
| **LD** | | Reflect the status of the LD output of the AD9517 |
| **STATUS** | | Reflect the status of the STATUS output of the AD9517 |
| **VM** | | Reflect the status of the INT# output of the ADT7411 (inverted) |
| | ‘0‘ | INT# is not asserted |
| | ‘1‘ | INT# is asserted, access to the ADT7411 trough the $I^2C$ bus is required to determine the source of the interrupt |
| **IRQ** | | Logic function: **NOT** (REFMON **AND** LD **AND** STATUS **AND** INT#) |
| | ‘0‘ | All status signals indicate OK |
| | ‘1‘ | One or more status signals indicate ERROR |

**Table 16 Register CPLD_REG2 description (read)**

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | Reserved | | | LED_SEL | | | | |

**Table 17: Register CPLD_REG2 definition (write)**

| Field | | Description |
|---|---|---|
| **LED_SEL** | | Writing to this register determines which status signal is reflected on the LED. |
| | ‘XXXX1‘ | REFMON |
| | ‘XXX10‘ | LD |
| | ‘XX100‘ | STATUS |
| | ‘X1000‘ | VM |
| | ‘10000‘ | IRQ |

**Table 18 Register CPLD_REG2 description (write)**

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