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CONDOR ENGINEERING

MIL-STD-1553

Hardware Installation Manual



Supporting Products:

- cPCI-1553
- IP-1553
- PCCARD-1553
- PMC-1553
- Q104-1553P
- QVXI-1553X
- VXI/VME-1553-IP
- cPCI-1553-IP
- ISA-1553
- PCI-1553
- Q104-1553
- QPMC-1553
- VME-1553
- IP-D1553
- PC-1553-IP
- PCI-1553-IP
- QPCI-1553
- QVME-1553
- VXI-1553

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Condor Engineering
101 W. Anapamu Street
Santa Barbara, CA 93101
(805) 965-8000
(805) 963-9630 (fax)
support@condoreng.com (e-mail)
http://www.condoreng.com (Internet)

Contents and Tables

Contents

Chapter 1 Overview

Introduction 1
Hardware Platforms 1
About this Manual 4

Chapter 2 ISA-1553 Installation

Installation Procedure 5
- Pre-installation Procedure 5
- Software Installation 5
- Hardware Installation 6

Board Layout 6
ISA-1553 Connector Description 7
- ISA-1553 Transition Cables 8

1553 - Bus Coupling 8
External Input 9
External Output 9
Setting the MEM16 Decode 9
ISA-1553 Memory Map 10
- Selecting Memory Addresses 11

Interrupt Line Select (IRQ3-7, 9-12, 14-15) 11

Chapter 3 PCI-1553 Installation

Installation Procedure 13
- Pre-installation Procedure 13
- Software Installation 13
- Hardware Installation 14

Board Characteristics and Layout 14
PCI-1553 Connector Description 15
- PCI-1553 Transition Cables 16

Signal Descriptions 17
- Transformer versus Direct Coupling 17
- MIL-STD-1553B Signals 17

External Input 17

External Output 18
External Hardwired RT Address 18
Memory Map Issues 18

Chapter 4 QPCI-1553 Installation

QPCI-1553 Installation Procedure 19
Pre-installation Procedure 19
Software Installation 19
Hardware Installation 20
QPCI-1553 Board Layout 20
Status LEDs 21
QPCI Connector Description 21
QPCI-1553 Mounting Plate Pin Out 22
QPCI-1553 Transition Cable 23
Signal Descriptions 24
MIL-STD-1553B Signals 24
IRIG Signaling 25
Memory Map Issues 25

Chapter 5 cPCI-1553 Installation

cPCI-1553 Installation Procedure 27
Pre-installation Procedure 27
Software Installation 27
Hardware Installation 28
cPCI-1553 Board Layout 28
Status LEDs 29
cPCI Connector Description 29
cPCI-1553 Rear Panel Pin Assignments 29
cPCI-1553 Front Panel Pin Assignments 30
Signal Descriptions 31
Transformer versus Direct Coupling 31
MIL-STD-1553B Signals 32
External Input 32
External Output 33
External Hardwired RT Address 33
Memory Map Issues 33

Chapter 6 PMC-1553 Installation

PMC-1553 Installation Procedure 35
Pre-installation Procedure 35
Software Installation 35
Hardware Installation 36
PMC-1553 Board Layout 36

Status LEDs 37
PMC Connector Description 37
PMC-1553 Rear Panel Pin Assignments 38
PMC-1553 Front Panel Pin Out 39
Signal Descriptions 39
Transformer versus Direct Coupling 39
MIL-STD-1553B Signals 40
External Input 40
External Output 41
External Hardwired RT Address 41
Memory Map Issues 41

Chapter 7 QPMC-1553 Installation
QPMC-1553 Installation Procedure 43
Pre-installation Procedure 43
Software Installation 43
Hardware Installation 44
QPMC-1553 Board Layout 44
Status LEDs 45
QPMC Connector Description 45
QPMC-1553 P14 Pin Assignments 46
QPMC-1553 Front Panel Pin Out 47
QPMC-1553 Transition Cable 48
Signal Descriptions 49
MIL-STD-1553B Signals 49
IRIG Signaling 49
Memory Map Issues 49

Chapter 8 PCCARD-1553 Installation
Installation Procedure 51
Pre-installation Procedure 51
Software Installation 51
Hardware Installation 52
Board Layout 54
PCCARD-1553 Connector Description 54
PCCARD-1553 Transition Cables 54
1553 - Bus Coupling 55
External Input 56
External Output 56
PCCARD-1553 Memory Map Issues 57
Interrupt Line Select (IRQ3-7, 9-12, 14-15) 57

Chapter 9 QVME-1553, VME-1553, QVXI-1553X, and VXI-1553 Installation

QVME/VME/QVXI/VXI-1553 Installation Procedure 59
Pre-installation Procedure 59
Software Installation 59
Hardware Installation 60
VME-1553 Board Layout 60
QVME-1553 Board Layout 61
VXI-1553 Board Layout 62
VME Front Panel Connector Description 62
QVME/VME/QVXI/VXI-1553 Transition Cables 63
VME-1553 P2 Connector 64
VXI-1553 P2 Connector 65
QVME-1553 P2 Connector 66
QVXI-1553X P2 Connector 67
Signal Descriptions 67
Transformer versus Direct Coupling 67
MIL-STD-1553B Signals 67
External Input 68
External Output 68
Discrete I/O 68
IRIG Signaling 69
Memory Map Issues 69

Chapter 10 Q104-1553 and Q104-1553-P Installation

Installation Procedure 71
Pre-installation Procedure 71
Software Installation 71
Hardware Installation 72
Board Layout 73
Q104-1553 and Q104-1553-P Connector Description 73
Q104-1553 and Q104-1553-P Transition Assemblies 74
1553 - Bus Coupling 75
External Input 75
External Output 75
Setting the MEM16 Decode 76
IRIG Signaling 76
Q104-1553 (ISA) Memory Map 76
Selecting Memory Addresses 78
Q104-1553-P [PCI Interface] Memory Map – PCI Stack Locator 78
Interrupt Line Select for the Q104-1553 (IRQ3-7, 9-12, 14-15) 79

Chapter 11 Standard IP-1553 Based Product Installation

Installation Procedure 81
Pre-installation Procedure 81
Software Installation 81
Hardware Installation 82
IP Connector Description 83
IP-1553 Transition Cable 84
TAGCLK and INCMD 85
Transformer versus Direct Coupling 85
MIL-STD-1553B Signals 86
VME/VXI-AIC-xx02 Jumper Settings 86
IP-1553 Jumper Location 87
External Input 87
External Output 88
External Hardwired RT Address 88
Memory Map Issues 88
IP Carrier Jumper Settings 89
PCI-1553-IP and cPCI-1553-IP Jumper Settings 89
PC-1553-IP Jumper Settings (ISA Carrier) 89
VME-1553-IP and VXI-1553-IP Jumper Settings 90
Configuring the Software Addressing 91

Chapter 12 IP-D1553 Installation

IP-D1553 Installation Procedure 93
Pre-installation Procedure 93
Software Installation 93
Hardware Installation 94
IP-D1553 Board Layout 94
Status LEDs 95
IP-D1553 Connector Description 95
IP-D1553 Pin Assignments 96
Signal Descriptions 97
Transformer versus Direct Coupling 97
MIL-STD-1553B Signals 98
External Input 98
External Output 98
RT Address 98
IRIG Signaling 99
Memory Map Issues 99

Chapter 13 Interface Signals

MIL-STD-1553 Bus Characteristics 101
Redundancy Management 102
1553 – Physical Bus Definition 102
Physical Bus Length 102
Transformer versus Direct Coupling 102
Supported Bus Coupling Methods 103
Direct Coupling 103
Transformer Coupling 103
Coupling Selection 103
MIL-STD-1553B Signals 104
Output Voltage Level 104
Input Voltage Threshold 104
Connections to a MIL-STD-1553 Bus 104
Discrete Signals 106
External Discrete Input 106
BC Trigger 107
RT Trigger 107
BM Trigger 107
Reset Tag Timer 107
Reset Timetag on Sync Mode Code 107
External Discrete Output 108
BM Trigger Output 108
RT Synchronize Mode Code Output 108
External Hardwired RT Address 108

Appendix A Glossary of Terms

Term List 111

Figures

Figure 1. ISA-1553 Board Photograph 7
Figure 2. PCI-1553 Photograph 15
Figure 3. DB15 Transitions Cables for PCI-1553, ISA-1553, and VME-1553. 16
Figure 4. QPCI-1553 Board Layout 20
Figure 5. Transition Cable for QPCI1553 Four Channel Cable. 21
Figure 6. cPCI-1553 Board Layout 28
Figure 7. PMC-1553 Board Layout 36
Figure 8. Transition Cable from each Champ 50 Connector on a cPCI-1553-IP or PMC-1553 37
Figure 9. QPMC-1553 Board Layout 44
Figure 10. Transition Cable for QPMC1553 (4-channel cable shown) 45
Figure 11. PCCARD-1553 Card with Transition Cable Attached 54
Figure 12. PCMCIA 33 Pin Doublewide Connector for PCCard-1553 55
Figure 13. VME-1553 Board Layout 60
Figure 14. QVME-1553 BoardLayout 61
Figure 15. VXI-1553 Board Layout. 62
Figure 16. Q104-1553, Shown with Optional PC/104-*Plus* Connector Installed 73
Figure 17. Jumper Block JB-1. 77
Figure 18. Jumper Block JB-1 78
Figure 19. IP-1553 Transition Cable Wiring 84
Figure 20. IP Module Ribbon Connectors for VME and VXI Front Panels 85
Figure 21. 25-pin D-sub Connector Cable for ISA and PCI IP Carriers 85
Figure 22. IP-1553 Jumper and Connector Locations 87
Figure 23. VME-1553-IP 91
Figure 24. VXI-1553-IP 91
Figure 25. IP-D1553 Board Layout 94
Figure 26. IP Module Ribbon Connectors for VME and VXI Front Panels 95
Figure 27. 25-pin D-sub Connector Cable for PCI IP Carriers 96
Figure 28. MIL-STD-1553A Data Bus Interface Schematic 105
Figure 29. MIL-STD-1553B Data Bus Interface Schematic 105

Tables

Table 1. ISA-1553 Pin Assignments....7
Table 2. ISA-1553 Memory Address Jumper Options....10
Table 3. PCI-1553 Connector Pin Assignments....16
Table 4. QPCI-1553 Front Bezel Pin Assignments....22
Table 5. QPCI-1553 Transition Cable, D50 Pin Assignments....23
Table 6. One-channel QPCI-1553 Transition Cable, 1553 Connectors....24
Table 7. Two-channel QPCI-1553 Transition Cable, 1553 Connectors....24
Table 8. Four-channel QPCI-1553 Transition Cable, 1553 Connectors....24
Table 9. IRIG Formats....25
Table 10. cPCI-1553 Rear Panel Pin Assignments....30
Table 11. cPCI-1553 Trigger I/O Front Panel Pin Assignments....31
Table 12. cPCI-1553 Coupling Options....32
Table 13. PMC-1553 Rear Panel Pin Assignments....38
Table 14. PMC-1553 Front Panel Pin Assignments....39
Table 15. PMC-1553 Coupling Options....40
Table 16. QPMC-1553 P14 Pin Assignments....46
Table 17. QPMC-1553 Front Panel Pin Assignments....47
Table 18. QPMC-1553 Transition Cable Pin Assignments....48
Table 19. Transition Cable 1553 Connectors....49
Table 20. PCCARD-1553 Pin Assignments....55
Table 21. QVME/VME/QVXI/VXI-1553 Front Panel Pin Assignments....62
Table 22. VME-1553 P2 Connector Pinout....64
Table 23. VXI-1553 P2 Connector Pinout....65
Table 24. QVME-1553 P2 Connector Pinout....66
Table 25. Q104-1553 P1 Connector Pin Assignments....73
Table 26. Q104-1553 Memory Address Jumper Options....77
Table 27. PCI Stack Locator jumpers....79
Table 28. The Pin Assignments for IP-1553 P4....83
Table 29. IP-1553 Jumpers for Direct or Transformer Coupling....86
Table 30. Setting IP-1553 Carrier Base Address....90
Table 31. IP-D1553 Field I/O Pin Assignments....96
Table 32. Glossary of Terms....111

CHAPTER 1

Overview

Introduction

This manual is the complete guide for the installation of Condor Engineering's MIL-STD-1553 product line. These high-performance MIL-STD-1553 interface boards give you a wide range of options, providing compatibility with almost any system configuration.

Chapter 1 provides an overview of Condor Engineering's MIL-STD-1553 products. Chapters 2 through 12 describe hardware installation of Condor Engineering's advanced, BusTools/1553-API-based, MIL-STD-1553 interface product lines. These products provide one, two, or 4 dual-redundant interface channels per card. Chapter 13 describes 1553 and discrete interface signals.

For detailed descriptions of all products, including available options, please see the latest Configuration Guide for Military Interface Products. This guide is available on the Condor Engineering Internet site, http://www.condoreng.com/.

Hardware Platforms

Installation for the following 1553 interface products are described in this document:

- PCI-1553 MIL-STD-1553A/B 1 or 2 channel PCI card

  The PCI-1553 card has one or two fully independent, single-function or multi-function interfaces to MIL-STD-1553A/B channels on the PCI bus. Included with the product is a DB15 to 1553 tri-ax cable jack connector transition cable for each channel.

- QPCI-1553 MIL-STD-1553A/B 1, 2, or 4 channel PCI Card

  The QPCI-1553 provides 1, 2, or 4 single or multi-function MIL-STD-1553A/B interface channels on the PCI bus. Included with the

product is a transition cable to provide easy connectivity from the SCSI 68-pin connector to 1553 tri-axial cable jack connector.

- cPCI-1553 MIL-STD-1553A/B 1 or 2 channel cPCI card

  The cPCI-1553 card provides one or two fully independent, single-function or multi-function interfaces to MIL-STD-1553A/B channels on the cPCI bus. The board allows user selection of Front Panel Tri-axial Jacks or Rear Backplane 1553 I/O.

- PMC-1553 MIL-STD-1553A/B single channel PCI Mezzanine Card

  The PMC-1553 provides either a single-function or a multi-function interface to a MIL-STD-1553A/B channel on the PMC form factor. The board allows user selection of front panel or J14 Rear 1553 I/O. Included with the product is a transition cable from Champ-50 to 1553 tri-axial cable jack connectors.

- QPMC-1553 MIL-STD-1553A/B 1, 2, or 4 channel PCI Mezzanine Card

  The QPMC-1553 provides 1, 2, or 4 single or multi-function MIL-STD-1553A/B interface channels on the PMC form factor. The board is available in front panel or J14 Rear 1553 I/O. Included with the product is a transition cable to provide easy connectivity from the SCSI 68-pin connector to 1553 tri-axial cable jack connector.

- Q104-1553 and Q104-1553-P MIL-STD-1553A/B 1, 2, or 4 channel PC/104 Card

  The Q104-1553/P provides 1, 2, or 4 single or multi-function MIL-STD-1553A/B interface channels on the PC/104 and PC/104-*Plus* form factor.

- ISA-1553 MIL-STD-1553A/B 1 or 2 Channel PC/AT card

  The ISA-1553 card provides one or two fully independent, single-function or multi-function interfaces to MIL-STD-1553A/B channels on the ISA bus. Included with the product is a DB15 to 1553 tri-axial cable jack connector transition cable for each channel.

- PCCARD-1553 MIL-STD-1553A/B 1 Channel PCMCIA card

  The PCCARD-1553 card provides one, single-function or multi-function interfaces to MIL-STD-1553A/B channel for the PCMCIA slot. Included with the product is a transition cable.

- QVME-1553, VME-1553, VXI-1553 MIL-STD-1553A/B 1, 2 or 4 Channel VME/VXI card

  The QVME/QVXI-XVME/VXI-1553 cards provide one, two, or four fully independent, single-function or multi-function interfaces to MIL-STD-1553A/B channels on the VME/VXI bus. Included with the product is a connector transition cable for each channel.

- IP-1553 MIL-STD-1553B single channel IP Module card.

  The IP-1553 provides either a single-function or a multi-function interface to a MIL-STD-1553B channel on an ANSI/VITA 4 compliant IP Module. A transition cable to 1553 tri-axial cable jack connectors is included when the IP-1553 is purchased installed on a carrier card.

- IP-D1553 MIL-STD-1553A/B single or dual channel IP Module card.

  The IP-D1553 provide one or two single- or multi-function 1553A/B channels on a single wide IP Module. A transition cable to 1553 connectors is provided when shipped on a carrier.

- cPCI-1553-IP MIL-STD-1553B one or two channel modular cPCI card (single bus on 3U form factor)
- VME-1553-IP MIL-STD-1553B one or two channel modular VME card
- VXI-1553-IP MIL-STD-1553B one or two channel modular VXI card
- PC-1553-IP MIL-STD-1553B one or two channel modular PC/AT card
- PCI-1553-IP MIL-STD-1553B 1 or 2 channel modular PCI card

The PCI-1553-IP, cPCI-1553-IP, VME-1553-IP, and VXI-1553-IP cards provide one or two modular, fully independent, single-function or multi-function interfaces to MIL-STD-1553 channels on PCI, PC/AT (ISA), cPCI, VME, and VXI buses, respectively. These modular interfaces include one or two IP-1553 modules, a carrier board, transition cabling to 1553 tri-ax connectors, and API support for various operating systems.

Any of these modular solutions (with the exception of the PC/AT (ISA) carrier,) may be offered with the dual channel IP-D1553, allowing up to eight 1553 channels on a single carrier.

Multi-function interfaces support simultaneous Bus Controller, Remote Terminals (up to 31), and Bus Monitor functionality. Single-function interfaces support either BC, or up to 31 RTs, or Bus Monitor functionality.

This manual's convention is to refer to a 1553 interface as a channel. A 1553 interface channel consists of dual redundant 1553 buses. There is a primary bus referred to as bus A and a secondary bus referred to as bus B. Some Condor Engineering products have up to four 1553-interface channels. This document refers to those as channel 1 through channel 4. Modular products that may contain up to eight 1553 channels are designated by the slot in which they are installed.

About this Manual

In addition to this chapter, this manual includes:

- Chapter 2, ISA-1553 Installation– describes configuration and installation of ISA-1553 boards.
- Chapter 3, PCI-1553 Installation – describes configuration and installation of PCI-1553 boards.
- Chapter 4, QPCI-1553 Installation – describes configuration and installation of QPCI-1553 boards.
- Chapter 5, cPCI-1553 Installation – describes configuration and installation of cPCI-1553 boards.
- Chapter 6, PMC-1553 Installation – describes configuration and installation of PMC-1553 boards.
- Chapter 7, QPMC-1553 Installation – describes how to install the QPMC-1553 board.
- Chapter 8, PCCARD-1553 Installation – describes configuration and installation of PCCARD-1553 boards.
- Chapter 9, QVME-1553, VME-1553, QVXI-1553X, and VXI-1553 Installation – describes configuration and installation of QVME/VME/VXI-1553 boards.
- Chapter 10, Q104-1553 and Q104-1553-P Installation – describes the configuration and installation of the PC/104 Q104-1553 and the PC/104-*Plus* Q104-1553-P boards.
- Chapter 11, Standard IP-1553 Based Product Installation – describes the configuration and installation of IP-1553, PC-1553-IP, PC-1553-IP, VME-1553-IP, and VXI-1553-IP boards.
- Chapter 12, IP-D1553 Installation – describes installation and configuration of the IP-D1553 board.
- Chapter 13, Interface Signals – describes BusTools 1553 and discrete interface signals.
- Appendix A, Glossary of Terms – lists and defines terms that are used in this document.

CHAPTER 2

ISA-1553 Installation

Installation Procedure

This section tells how to install the ISA-1553 board.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

1. Check your system for memory and I/O conflicts and select the desired memory and I/O addresses and hardware interrupt for the board.

   See the “Quick Start” installation guide.

2. Using the supplied software disks, install the software.

   Be sure to follow the instructions in the “Software Installation Manual” for the operating system you intend to use. When the software installation is complete, you must power the computer off.

Hardware Installation

After installing the software, follow the steps to install the hardware:

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you change the jumpers.
2. Set the jumpers on the board to the desired settings for your operating system. (See the "ISA-1553 Memory Map" section for specific settings).
3. Remove the cover from your PC. Remove the blank mounting plate from one of the unused slots in your computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.
4. There are two BNC connectors in the transition cable assembly providing the trigger input and output. The connectors are labeled as input and output. Chapter 13, "Interface Signals" discusses trigger functions.
5. Connect the supplied transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly. The ISA-1553 I/O configuration is defined below.

Note: If you are using "transformer" coupling, than connect the bus "A" and "B" "stubs" from the transformers to the connectors on the transition cable assembly.

If you are using "direct" coupling and this is the last connection on the bus a "Tee" should be used and a 78-ohm terminator should be connected to provide the proper termination for the bus. Otherwise, use a "Tee" with a cable on each end of the "Tee".

Board Layout

Figure 1 shows the location of the connectors. The connector furthest from the ISA bus connector (P1) contains the 1553 Channel #1 interface, while the lower connector (P3) contains the 1553 Channel #2 interface.

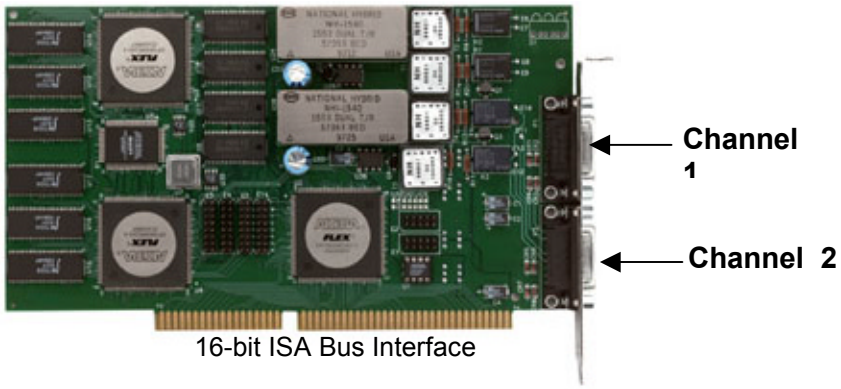


Figure 1. ISA-1553 Board Photograph

ISA-1553 Connector Description

The ISA-1553 card edge connector P4 implements the ISA bus interface.

The ISA-1553 provides two DB15 connectors, P1 and P3, which are accessible from the outside of the PC after the ISA-1553 has been installed.

Connections for 1553 channel #1 are contained on P1, and the connections for 1553 channel #2 are contained on P3. (While the connector locations on the ISA-1553 board are opposite from the locations on the PCI-1553 board, the pinouts of the connectors are identical). The following table lists the pin assignments:

Table 1. ISA-1553 Pin Assignments

Upper Connector P1 Channel 1 Interface		Lower Connector P3 Channel 2 Interface	
Pin Number	**Signal Name**	**Pin Number**	**Signal Name**
1	BUS1_B+	1	BUS2_B+
2	BUS1_B-	2	BUS2_B-
3	GND	3	GND
4	BUS1_A+	4	BUS2_A+
5	BUS1_A-	5	BUS2_A-
6	BUS1_SHIELD	6	BUS2_SHIELD
7	BUS1_EXTIN	7	BUS2_EXTIN
8	BUS1_EXTOUT	8	BUS2_EXTOUT
9	BUS1_SHIELD	9	BUS2_SHIELD
10	BUS1_RTA0	10	BUS2_RTA0
11	BUS1_RTA1	11	BUS2_RTA1

Upper Connector P1 Channel 1 Interface		Lower Connector P3 Channel 2 Interface	
Pin Number	**Signal Name**	**Pin Number**	**Signal Name**
12	BUS1_RTA2	12	BUS2_RTA2
13	BUS1_RTA3	13	BUS2_RTA3
14	BUS1_RTA4	14	BUS2_RTA4
15	BUS1_RTADP	15	BUS2_RTADP

ISA-1553 Transition Cables

The ISA-1553 is supplied with one or two transition cables (Figure 3), which mate with the DB15 connectors on the board and provide 1553 cable jacks for mating with user-supplied 1553 wiring.

These transition cables also route the discrete input and output signals to BNC-type connectors.

The transition cables are identical to those supplied with PCI-1553 boards.

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website.

1553 - Bus Coupling

The 1553 connections can be coupled in two different manners:

- Direct coupled (short stub) – Isolation Transformer 1.4:1
- Transformer coupled (long stub)

Use direct coupling when the distance from the board's isolation transformer to the data bus is less than or equal to one-foot. Use transformer coupling when the distance exceeds one-foot, but is less than 25 feet.

There are isolation transformers on the board for both direct and transformer coupling. There are 53.6-ohm isolation resistors on the board for direct coupling. Transformer coupling requires an external transformer and isolation resistor at the junction to the main 1553 bus to match the stub impedance to the bus. (The Air Force mandates that transformer coupling be used).

The bus coupling (transformer or direct) is controlled by two relays that are selected under software control. See the API routine BusTools_SetVoltage().

See chapter 13, “Interface Signals“ for a complete description of the 1553 interface signals.

External Input

EXTIN is a TTL signal that is activated by a low to high transition. The minimum high pulse is 400 ns, but it may stay high indefinitely. When a pulse is high for 200 to 400 ns, it can’t be determined whether it will produce an active input. EXTIN has one of four functions that are programmed in software:

- BC trigger
- RT trigger
- BM trigger
- Reset Tag Timer.

This signal is an input of the Altera 10K50. It is pulled up to +5 volts by a 4.7K-ohm on-board resistor and is protected by a 100-ohm series resistor and diodes to both VCC and Ground.

See chapter 13, “Interface Signals“ for a complete description of the functions of the discrete input signal.

External Output

EXTOUT is an active high TTL signal that goes active for 50 microseconds. Software controls the firing of this output. It may be enabled for BM trigger or RT Synchronize mode code.

This signal is an output of the Altera 10K50 and is protected by a 100-ohm series resistor and diodes to both VCC and Ground.

See chapter 13, “Interface Signals“ for a complete description of the functions of the discrete output signal.

Setting the MEM16 Decode

Jumper posts E14 Pins 6-14 are assigned to the “usa” bit that forces the hardware to decode the ISA sa[16…14] signals along with the la[23…17] signals as qualifiers for the MEM16 signal. MEM16 is the asynchronous handshake that informs the initiator that it can accept a 16-bit word transfer (PC/AT 16-bit board versus 8-bit XT board). The EISA/ISA specification does not allow sa[] signals to be used to qualify MEM16, as the adapters within a 128K boundary must all be 16-bit or all

be 8-bit boards. In reality, many platforms do not follow the specification and we have found that qualifying MEM16 with sa[16…14] works best on the vast majority of PC's. However, a very few PC's delay the sa[] signals too long to qualify them for MEM16.

You may insert a jumper across E14 Pins 6-14 to *disable* the use of sa[16…14] qualifiers. When the jumper is removed (default), the board uses sa[16…14] to qualify MEM16.

ISA-1553 Memory Map

The ISA-1553 board may be mapped into any available 16K-byte block in upper memory between segment addresses A000:0000 and E400:0000 (physical addresses A0000 to E4000 hexadecimal). The memory address is determined by the jumper settings on header E14 (listed below). (If a jumper is removed, it selects and reads back as a "one" when reading hardware register "jumpers/revision_number" at offset 0x0A). (The following table refers to the values silk-screened onto the board, not the pin numbers specified by the schematic).

The ISA-1553 memory is paged by an internal page register, which is accessed in memory space at word-offset 0x08 (See the "MIL-STD-1553 Universal Core Architecture Reference Manual" for more information).

Table 2. ISA-1553 Memory Address Jumper Options

Selected Physical Address Range	E14: 1-9	E14: 2-10	E14: 3-11	E14: 4-12	E14: 5-13
0A0000 - 0A3FFF	ON	OFF	ON	ON	ON
0A4000 - 0A7FFF	ON	OFF	ON	ON	OFF
0A8000 - 0ABFFF	ON	OFF	ON	OFF	ON
0AC000 - 0AFFFF	ON	OFF	ON	OFF	OFF
0B0000 - 0B3FFF	ON	OFF	OFF	ON	ON
0B4000 - 0B7FFF	ON	OFF	OFF	ON	OFF
0B8000 - 0BBFFF	ON	OFF	OFF	OFF	ON
0BC000 - 0BFFFF	ON	OFF	OFF	OFF	OFF
0C0000 - 0C3FFF	OFF	ON	ON	ON	ON
0C4000 - 0C7FFF	OFF	ON	ON	ON	OFF
0C8000 - 0CBFFF	OFF	ON	ON	OFF	ON
0CC000 - 0CFFFF	OFF	ON	ON	OFF	OFF
0D0000 - 0D3FFF	OFF	ON	OFF	ON	ON
0D4000 - 0D7FFF	OFF	ON	OFF	ON	OFF
0D8000 - 0DBFFF	OFF	ON	OFF	OFF	ON
0DC000 - 0DFFFF	OFF	ON	OFF	OFF	OFF
0E0000 - 0E3FFF	OFF	OFF	ON	ON	ON

Selected Physical Address Range	E14: 1-9	E14: 2-10	E14: 3-11	E14: 4-12	E14: 5-13
0E4000 - 0E7FFF	OFF	OFF	ON	ON	OFF

Selecting Memory Addresses

Prior to selecting the memory block that the hardware is mapped into, the available system memory resources must be determined. For upper memory, the C800 and D000 segments (96K bytes) are allocated for adapter boards on the ISA platform. Before installing the board, you must find a 16K-byte block that is free, starting at one of the base addresses listed in the table.

When using any program to determine if a memory or I/O space is available for use remember that most such programs only report what the operating system knows. If no operating system driver has been installed for a memory or I/O region, the program might report that it is available, even if some device is really using that region.

Keep in mind that if multiple boards are being used in the same platform, then sufficient memory space must be available for each board. With four boards (up to eight 1553 channels), this requires 64K free bytes.

The "Software Installation Manual" lists specific steps that might assist you in determining which upper memory address space is available.

Interrupt Line Select (IRQ3-7, 9-12, 14-15)

The ISA-1553 board features software-programmable interrupt line selection. There are no interrupt jumpers to set. However, you still must choose the interrupt to use, one that isn't being used by another board.

When installing the software for 32-Bit Windows you are asked to select the hardware interrupt number. Selecting "0" disables hardware interrupts; the API subsequently defaults to polling the board.

With a dual-channel ISA-1553 board, both channels share the same hardware interrupt line. The BusTools/1553-API correctly handles sharing the interrupt between the two channels.

CHAPTER 3

PCI-1553 Installation

Installation Procedure

This section tells how to install the PCI-1553 board.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

As the PCI-1553 board is a Plug-and-Play board, there are no switches or jumpers on the board.

1. For 32-Bit Windows Operating Systems, install the software before installing the hardware. For UNIX and VxWorks systems install the hardware first, then the software.

2. Using the supplied software disks, follow the instructions in the "Quick Start" installation guide.

   Be sure to follow the instructions applicable to your operating system. This is especially important when installing the software on a 32-Bit Windows system.

3. When the software installation is complete, restart your computer.

Hardware Installation

Follow these steps to install the hardware:

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
2. Remove the cover from your PC. Remove the blank mounting plate from one of the unused PCI slots in your computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.
3. There are two BNC connectors in the transition cable assembly providing the trigger input and output. The connectors are labeled as input and output.

   The trigger functions are discussed in chapter 13, "Interface Signals".
4. Connect the supplied transition cable assembly to the board and then connect your MIL-STD-1553 channel to the cable assembly. The PCI-1553 I/O configuration is defined below.

Note: If you are using "transformer" coupling, then connect the bus "A" and "B" "stubs" from the transformers to the connectors on the transition cable assembly

If you are using "direct" coupling, and this is the last connection on the bus, use a "Tee" and connect a 78-ohm terminator to provide the proper termination for the bus. Otherwise, you should use a "Tee" with a cable on each end of the "Tee".

Board Characteristics and Layout

The PCI-1553 is a three-quarter-length PCI board designed to PCI Specification 2.1. It is a 32-bit board, capable of operating in PCI systems that run at up to the full 33 MHz clock rate supported by PCI Version 2.1. The card edge connector, P2, implements the PCI bus interface.

The PCI-1553 supports 5-volt PCI signaling. It is keyed to prevent installation into a 3.3-volt system. Per the PCI specification, the data bus format is Little Endian.

In keeping with the Plug and Play nature of the PCI bus, there are no user-settable switches or jumpers on the board. The PCI-1553 implements Interrupt A (INTA#) only. PCI interrupts are sharable. On boards that support two channels, this interrupt is shared by both channels..

Addresses are assigned by the Plug and Play BIOS or by the operating system.

Figure 2, shows the location of the three interface connectors on the PCI-1553 board. The card edge connector at the bottom of the card is the PCI bus interface, and is designated P2.

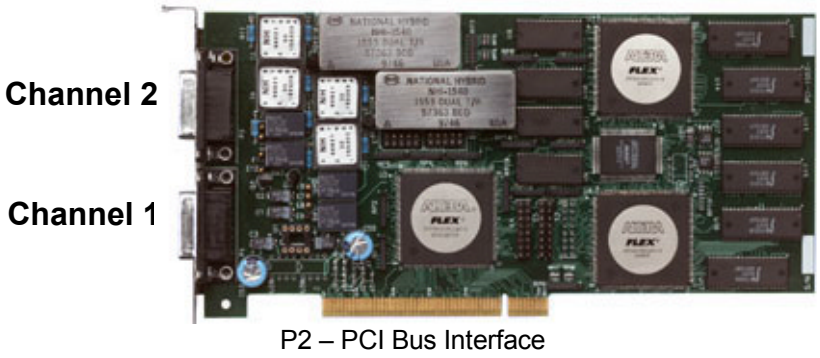


Figure 2. PCI-1553 Photograph

PCI-1553 Connector Description

The PCI-1553 provides two DB-15 connectors, P1 and P3, which are accessible from the outside of the PC after the PCI-1553 has been installed..

Connections for 1553 Channel 1 are contained on P1, and the connections for 1553 Channel 2 are contained on P3. (While the connector locations on the PCI-1553 board are reversed from the locations on the ISA-1553 board, the connectors pin assignments are identical). The following table shows pin assignments.

Table 3. PCI-1553 Connector Pin Assignments

Lower Connector P1 Channel 1 Interface		Upper Connector P3 Channel 2 Interface	
Pin Number	**Signal Name**	**Pin Number**	**Signal Name**
1	BUS1_B+	1	BUS2_B+
2	BUS1_B-	2	BUS2_B-
3	GND	3	GND
4	BUS1_A+	4	BUS2_A+
5	BUS1_A-	5	BUS2_A-
6	BUS1_SHIELD	6	BUS2_SHIELD
7	BUS1_EXTIN	7	BUS2_EXTIN
8	BUS1_EXTOUT	8	BUS2_EXTOUT
9	BUS1_SHIELD	9	BUS2_SHIELD
10	BUS1_RTA0	10	BUS2_RTA0
11	BUS1_RTA1	11	BUS2_RTA1
12	BUS1_RTA2	12	BUS2_RTA2
13	BUS1_RTA3	13	BUS2_RTA3
14	BUS1_RTA4	14	BUS2_RTA4
15	BUS1_RTADP	15	BUS2_RTADP

PCI-1553 Transition Cables

The PCI-1553 is supplied with one or two transition cables (Figure 3), which mate with the DB15 connectors on the board and provide 1553 cable jacks for mating with customer-supplied 1553 wiring. These transition cables also route the discrete input and output signals to BNC-type connectors. The transition cables are identical to those supplied with the ISA-1553 boards.

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website.



Figure 3. DB15 Transitions Cables for PCI-1553, ISA-1553, and VME-1553.

Signal Descriptions

See chapter 13, “Interface Signals”, for a complete description of the 1553 interface signals.

Transformer versus Direct Coupling

MIL-STD-1553B allows for two methods of connecting a terminal to the bus. Transformer coupling provides better noise immunity and isolation over long distances and requires external transformer couplers. Direct coupling is often used in the laboratory because it requires no transformers between boxes. Bus coupling is under software control.

MIL-STD-1553B Signals

A+ and A- are the differential pair for channel A. SHIELD is used in most environments to shield the cable used for the stub connections. B+ and B- are the differential pair for channel B. SHIELD is also used to shield the channel B pair. Both shields are tied together and to the center tap of the isolation transformers on the PCI-1553 board.

PCI-1553 boards may contain two complete dual-redundant 1553 channels, channel 1 and channel 2. The P1 connector is located on the bottom of the board (component side up) and is used for channel 1. The P3 connector is located on the top of the board (component side up) and is used for channel 2.

External Input

EXTIN is a TTL signal that is activated by a low to high transition. The minimum high pulse is 400 ns, but it may stay high indefinitely. When a pulse is high for 200 to 400 ns, it can’t be determined whether it will produce an active input. EXTIN has one of four functions that are programmed in software: BC trigger, RT trigger, BM trigger, and Reset Tag Timer.

This signal is an input of the Altera 10K50, is pulled up to +5 volts by a 4.7K ohm resistor located on the board, and is protected by a 100 ohm series resistor and diodes to both VCC and Ground.

See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete input signal.

External Output

EXTOUT is an active high TTL signal that goes active for 50 microseconds. Software controls the firing of this output. It may be enabled for BM trigger or RT Synchronize Mode Code.

This signal is an output of the Altera 10K50, and is protected by a 100-ohm series resistor and diodes to both VCC and Ground.

See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete output signal.

External Hardwired RT Address

This feature is currently not implemented but could be if requested. The RTAD[4…0] signals are for externally hardwiring the boards to respond as a single RT. The RTADP is the parity signal. If the RT address is hardwired, the board is not able to simulate the Bus Controller or to respond to any other RT address even when so enabled by the software.

See chapter 13, “Interface Signals”, for a complete description of the external RT address discrete signals.

Memory Map Issues

The PCI-1553 requires a 32-megabyte address block. When using the PCI-1553, the BIOS maps the board into memory space at an address above the total amount of RAM installed in the computer.

The supplied software supports the PCI-1553 under 32-Bit Windows, Linux, and Solaris.

CHAPTER 4

QPCI-1553 Installation

QPCI-1553 Installation Procedure

This section explains how to install the QPCI-1553 board. The QPCI-1553 is a single, dual, or quad channel 1553 interface board.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment. If it has, contact the shipper right away.

Software Installation

The QPCI-1553 board is a Plug-and-Play board. There are no switches or jumpers on the board required for software installation.

1. For 32-Bit Windows install the software before installing the hardware.

   For UNIX and VxWorks systems install the hardware first, then the software.

2. Using the supplied software disks. Be sure to follow the instructions applicable to your operating system.

Note: When you install on a 32-Bit Windows systems (Windows 95/98/NT/2000/Me/XP), you must restart your computer after installation.

Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
2. Remove the cover from your PC. Remove the mounting plate from one of the unused PCI slots in your computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with your board.

   The QPCI I/O configuration is defined below. A transition cable is provided from the QPCI I/O connector to MIL-STD-1553 cable jacks and a D50 connector for other I/O signals.

Note: If this is the last connection on the bus, use a “Tee” to connect a 78-ohm terminator to provide proper termination for the bus. Otherwise, use a “Tee” with a cable on each end. For “transformer”, coupling, connect bus “A” and “B” “stubs” to the connectors on the interface card.

QPCI-1553 Board Layout

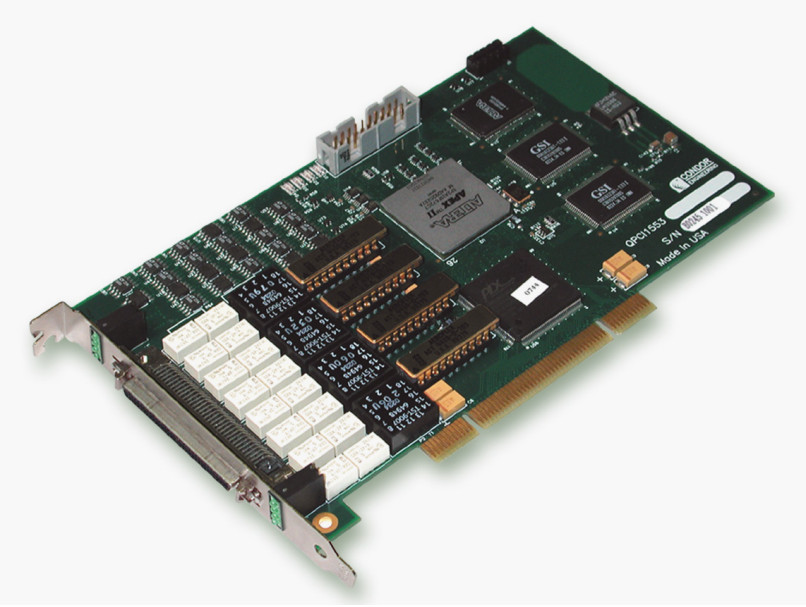


Figure 4. QPCI-1553 Board Layout

Status LEDs

There are four bi-colored status LEDs on the top (component side) of the QPCI-1553:

- **B0, B1, B2, B3 LED's - 1553 Bus Activity** – The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic and illuminates red if that channel runs internally (transceiver transmit is inhibited).

There are eight LED's on the mounting plate of the QPCI-1553:

- **CH 1, CH 2, CH 3, CH 4 - 1553 Bus Activity -** The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic.
- **INIT DONE, INIT ERR – Configuration Status** – INIT DONE illuminates green on successful FPGA configuration; INIT ERR illuminates green on failed FPGA configuration. The QPCI-1553 configures from an onboard configuration device, so the INIT DONE LED should be illuminated under normal conditions.
- **BIT PASS, BIT FAIL** – **Built-in-test Status –** BIT PASS illuminates green on successful Built In Test; BIT FAIL illuminates green on failed BIT. Both LEDs are off before the first BIT attempt.

QPCI Connector Description

The QPCI-1553 uses a single 68-pin SCSI connector (P1) on the mounting plate for all I/O. Separate cable assemblies are provided with one-channel, two-channel, and four-channel boards.

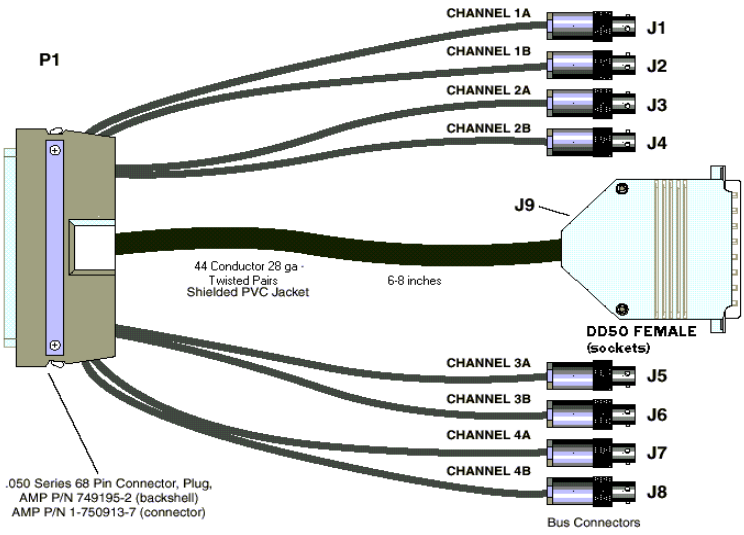


Figure 5. Transition Cable for QPCI1553 Four Channel Cable.

QPCI-1553 Mounting Plate Pin Out

The mounting plate connector pin out is specified in the following table.

Table 4. QPCI-1553 Front Bezel Pin Assignments

Front Bezel Connector (J1)			
Pin	**Function**	**Pin**	**Function**
1	1553 CH1A+	35	ADISC7
2	1553 CH 1A-	36	ADISC8
3	1553 CH 1A Shield	37	ADISC9
4	GND (for ADISC1)	38	ADISC10
5	1553 CH 1B+	39	485/422 CH1+
6	1553 CH 1B-	40	485/422 CH1-
7	1553 CH 1B Shield	41	485 Shield
8	RTADDR1_0/ADISC1	42	EXT CLK+/Trigger+
9	RTADDR1_1/ADISC2	43	EXT CLK-/Trigger-
10	1553 CH 2A+	44	GND (for ADISC4)
11	1553 CH 2A-	45	GND (for ADISC6)
12	1553 CH 2A Shield	46	GND (for ADISC5)
13	GND (for ADISC2)	47	LRUA Shield
14	1553 CH 2B+	48	LRUA+
15	1553 CH 2B-	49	LRUA -
16	1553 CH 2B Shield	50	GND (for ADISC7)
17	RTADDR1_2/ADISC3	51	IRIGB IN or CLKIN
18	RTADDR1_3/ ADISC4	52	IRIGB OUT or CLKOUT
19	1553 CH 3A+	53	IRIGB GND or CLKGND
20	1553 CH 3A-	54	GND (for ADISC8)
21	1553 CH 3A Shield	55	-
22	GND	56	-
23	1553 CH 3B+	57	-
24	1553 CH 3B-	58	GND (for ADISC9)
25	1553 CH 3B Shield	59	LRUB+
26	-	60	LRUB -
27	GND	61	LRUB Shield
28	1553 CH 4A+	62	-
29	1553 CH 4A-	63	GND (for ADISC10)
30	1553 CH 4A Shield	64	RTADDR1_4/ADISC5
31	GND (for ADISC3)	65	RTADDR1_P/ ADISC6
32	1553 CH 4B+	66	-
33	1553 CH 4B-	67	-
34	1553 CH 4B Shield	68	GND (overall Shield)

QPCI-1553 Transition Cable

The pin-outs for the QPCI transition cable are provided in the following tables.

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website.

Table 5. QPCI-1553 Transition Cable, D50 Pin Assignments

Transition Cable J5 (J3)* Pinout			
1	RTADD1_0/ADSIC 1	26	GND (for ADISC9)
2	RTADD1_1/ADSIC 2	27	-
3	GND (for ADISC1)	28	GND (for ADISC10)
4	RTADD1_2/ADSIC 3	29	LRUA Shield
5	RTADD1_3/ADSIC 4	30	-
6	GND (for ADISC2)	31	-
7	RTADD1_4/ADSIC 5	32	-
8	RTADD1_P/ADSIC 6	33	-
9	ADSIC 7	34	485/422 CH1+
10	ADSIC 8	35	485/422 CH1-
11	ADSIC 9	36	485 Shield
12	GND	37	LRUA+
13	EXT CLK+/Trigger+	38	LRUA -
14	EXT CLK-/Trigger-	39	GND (for ADISC7)
15	-	40	LRUB+
16	GND	41	LRUB -
17	-	42	LRUB Shield
18	ADSIC 10	43	-
19	GND (for ADISC4)	44	-
20	GND (for ADISC6)	45	GND (for ADISC3)
21	GND (for ADISC5)	46	IRIGB IN or CLKIN
22	-	47	IRIGB OUT or CLKOUT
23	-	48	IRIGB GND or CLKGND
24	-	49	-
25	GND (for ADISC8)	50	GND (overall Shield)

Note: For one-channel cable assemblies, this connector is J3; for two and four channel assemblies this connector is J5.

Table 6. One-channel QPCI-1553 Transition Cable, 1553 Connectors

Transition Cable 1553 Connectors	
Connector	***Signal***
J1	*Channel 1, Bus A*
J2	*Channel 1, Bus B*

Table 7. Two-channel QPCI-1553 Transition Cable, 1553 Connectors

Transition Cable 1553 Connectors	
Connector	***Signal***
J1	*Channel 1, Bus A*
J2	*Channel 1, Bus B*
J3	*Channel 2, Bus A*
J4	*Channel 2, Bus B*

Table 8. Four-channel QPCI-1553 Transition Cable, 1553 Connectors

Transition Cable 1553 Connectors	
Connector	***Signal***
J1	*Channel 1, Bus A*
J2	*Channel 1, Bus B*
J3	*Channel 2, Bus A*
J4	*Channel 2, Bus B*
J6	*Channel 3, Bus A*
J7	*Channel 3, Bus B*
J8	*Channel 4, Bus A*
J9	*Channel 4, Bus B*

Signal Descriptions

See chapter 13, “Interface Signals”, for a complete description of the 1553 interface signals.

MIL-STD-1553B Signals

1553 CH*n*A+ and 1553 CH*n*A- are the differential pair for bus A. 1553 CH*n* B+ and 1553 CH*n* B- are the differential pair for bus B.

1553 CH *n*A/B SHIELD is tied to the center tap of the isolation transformer of the respective bus on the QPCI-1553 board.

IRIG Signaling

IRIG time may be received on the signals IRIG IN and IRIG GND. The following IRIG formats are accepted:

Table 9. IRIG Formats

Format	Modulation Frequency	Frequency/ Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

When enabled by the software, IRIG OUT transmits IRIG B002 data from the onboard IRIG encoder. The IRIG OUT signal can source/sink 16 mA at valid TTL levels.

Memory Map Issues

The QPCI-1553 requires an 8MB address block. The BIOS maps the QPCI-1553 board into memory space at an address above the total amount of RAM in the computer. The QPCI-1553 also has a 128 byte PCI configuration register. Direct access to this register is not available through the API.

CHAPTER 5

cPCI-1553 Installation

cPCI-1553 Installation Procedure

This section describes installation of the cPCI-1553 boards. The cPCI-1553 is a CompactPCI interface.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

As the cPCI-1553 board is a Plug-and-Play board, there are no switches or jumpers on the board related to board configuration.

1. For 32-Bit Windows install the software before installing the hardware. For UNIX and VxWorks systems install the hardware first, then the software.

2. Using the supplied software disks, follow the instructions in the "Quick Start" installation guide.

   Be sure to follow the instructions applicable to your operating system. This is especially important when installing the software on a 32-Bit Windows system.

3. When the software installation is complete, restart your computer.

Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
2. Set the jumpers on the cPCI-1553 module to the desired settings for your MIL-STD-1553 coupling and I/O configuration. See the "Hardware Description" section for specific settings.
3. Install the cPCI-1553 in your cPCI chassis.
4. Connect the MIL-STD-1553 bus to the desired interface. See the "Hardware Description" for 1553 I/O options.

   The cPCI I/O configuration is defined below. Front Panel BJ77 panel jacks are provided for front panel interface, as are Rear I/O pins on the cPCI J2 Rear I/O connector.

Note: If this is the last connection on the bus, use a "Tee" to connect a 78-ohm terminator to provide proper termination for the bus. Otherwise, use a "Tee" with a cable on each end. For "transformer", coupling, connect the bus "A" and "B" "stubs" to the connectors on the interface card.

cPCI-1553 Board Layout

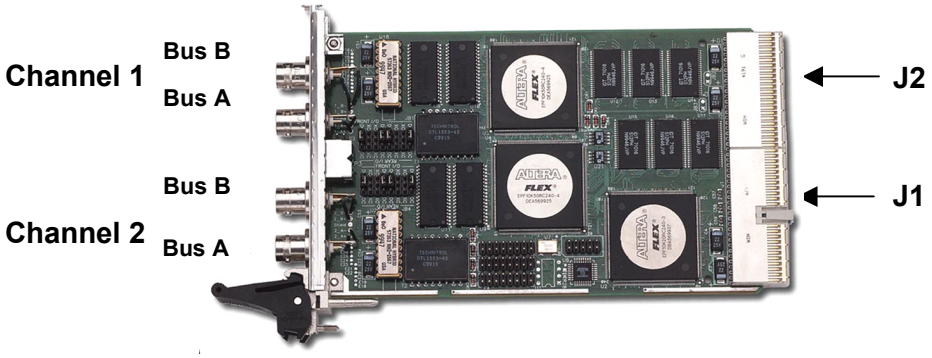


Figure 6. cPCI-1553 Board Layout

Status LEDs

There are four status LEDs on the rear side of the cPCI-1553:

- **Top LED: FPGA Configuration Status** – Indicates the status of the Local Processing Unit (LPU) FPGA. Once the FPGA is configured, the LED illuminates
- **Second LED: PCI Activity** – Illuminates when the host is actively accessing the cPCI-1553 board
- **Third LED: 1553 Channel 1 Activity** – Illuminates when traffic is detected on the first 1553 channel
- **Fourth LED: 1553 Channel 2 Activity** – Illuminated when traffic is detected on the second 1553 channel

cPCI Connector Description

The cPCI-1553 is designed to the CompactPCI Specification (PICMG 2.0 R3.0). PCI logic signals are routed through connector J1.

The cPCI-1553 uses panel mounted BJ77 tri-axial connectors for front panel I/O. Rear I/O signals are routed to connector J2 for rear panel I/O. Jumper blocks JB1 and JB4 determine the coupling and destination of the 1553 signals.

Trigger I/O is routed to the PS2 connector on the front panel.

Note: JB2 and JB3 MUST NOT BE INSTALLED when the cPCI-1553 is used in a PXI backplane.

cPCI-1553 Rear Panel Pin Assignments

The rear panel I/O J2 connector pin assignment is specified in the following table. Standard cPCI pin numbering convention is observed, where Row A is nearest the PCB edge. Any pin not listed in the table is not connected to the cPCI-1553 board.

Table 10. cPCI-1553 Rear Panel Pin Assignments

J2 Pin Out	
Pin Number	**Signal Name**
A22	BUS1_A+
B22	BUS1_A-
A20	BUS1_B+
B20	BUS1_B-
B15	BUS1_EXTOUT
B1	BUS1_RTA0
B3	BUS1_RTA1
B5	BUS1_RTA2
B7	BUS1_RTA3
B9	BUS1_RTA4
B11	BUS1_RTADP
B17	GROUND
C22	BUS2_A+
D22	BUS2_A-
C20	BUS2_B+
D20	BUS2_B-
C15	BUS2_EXTOUT
C1	BUS2_RTA0
C3	BUS2_RTA1
C5	BUS2_RTA2
C7	BUS2_RTA3
C9	BUS2_RTA4
C11	BUS2_RTADP

cPCI-1553 Front Panel Pin Assignments

1553 signals are routed to Front Panel tri-axial connectors. Silkscreen indicates channel numbering.

Trigger I/O is routed to the PS2 connector on the front panel. See Table 11 for pin assignments.

Table 11. cPCI-1553 Trigger I/O Front Panel Pin Assignments

Front Panel Pin Out	
Pin Number	**Signal Name**
1, 2	Ground
3	BUS1_EXTIN
5	BUS1_EXTOUT
4	BUS2_EXTIN
6	BUS2_EXTOUT

Signal Descriptions

See chapter 13 “Interface Signals”, for a complete description of the 1553 interface signals.

Transformer versus Direct Coupling

MIL-STD-1553B allows for two methods of connecting a terminal to the bus:

- Transformer coupling provides noise immunity over long distances and requires external transformer couplers.
- Direct coupling is often used in the laboratory because it requires no transformers between boxes.

Jumper block JB1 is used to set coupling and signal routing for channel 1, while JB4 is used to select coupling and signal routing for channel 2.

The software function BusTools_SetVoltage() *cannot* configure the coupling mode or I/O routing. The output voltage level may be set using this command on configurations that support Variable Transmit Amplitude. Jumpers are used to set the cPCI-1553 board for either coupling method. The board comes with jumpers set for direct-coupled mode as default.

Be sure that only direct coupling or transformer-coupling jumpers are set at any given time.

Table 12. cPCI-1553 Coupling Options

Function	Jumpers Installed
Front Panel Direct coupled, channel A	1-2, 10-11
Front Panel Transformer coupled, channel A	4-5, 7-8
Front Panel Direct coupled, channel B	13-14, 22-23
Front Panel Transformer coupled, channel B	16-17, 19-20
Rear Panel I/O Direct coupled, channel A	2-3, 11-12
Rear Panel I/O Transformer coupled, channel A	5-6, 8-9
Rear Panel I/O Direct coupled, channel B	14-15, 23-24
Rear Panel I/O Transformer coupled, channel B	17-18, 20-21

Note: The coupling method is set by these jumpers; the software function BusTools_SetVoltage() *cannot* be used to configure the coupling mode or signal routing.

MIL-STD-1553B Signals

A+ and A- are the differential pair for channel A. SHIELD is used in most environments to shield the cable used for the stub connections. B+ and B- are the differential pair for channel B. SHIELD is also used to shield the channel B pair. Both shield are tied together and to the center tap of the isolation transformers on the cPCI-1553 board.

External Input

EXTIN is a TTL signal that is activated by a low to high transition. The minimum high pulse is 400 ns, but it may stay high indefinitely. When a pulse is high for 200 to 400 ns, it can't be determined whether it will produce an active input. EXTIN has one of four functions that are programmed in software: BC trigger, RT trigger, BM trigger and Reset Tag Timer.

This signal is an input of the Altera 10K50, is pulled up to +5 volts by a 4.7K ohm resistor located on the board, and is protected by a 100 ohm series resistor and diodes to both VCC and Ground.

See chapter 13, "Interface Signals", for a complete description of the functions of the discrete input signal.

External Output

EXTOUT is an active high TTL signal that goes active for 50 microseconds. Firing this output is under software control. It may be enabled for BM trigger or RT Synchronize Mode Code.

This signal is an output of the Altera 10K50, and is protected by a 100-ohm series resistor and diodes to both VCC and Ground.

See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete output signal.

External Hardwired RT Address

This feature is currently not implemented but could be if requested. The RTAD[4…0] signals are used to externally hardwire the boards to respond as a single RT. The RTADP is the parity signal. If the RT address is hardwired, the board is not able to simulate the Bus Controller or to respond to any other RT address even when so enabled by the software.

See chapter 13, “Interface Signals”, for a complete description of the external RT address discrete inputs.

Memory Map Issues

The cPCI-1553 requires a 32-megabyte address block. The BIOS maps the cPCI-1553 board into memory space at an address above the total amount of RAM in the computer. The supplied software supports the cPCI-1553 under 32-Bit Windows and Linux.

CHAPTER 6

PMC-1553 Installation

PMC-1553 Installation Procedure

This section tells how to install the PMC-1553 board.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

As the PMC-1553 board is a Plug-and-Play board, there are no switches or jumpers on the board required for software installation.

1. Using the supplied software disks, follow the instructions in the "Quick Start" installation guide.

   Be sure to follow the instructions applicable to your operating system. This is especially important when installing the software on a 32-Bit Windows system.

2. When the software installation is complete, restart your computer.

Hardware Installation

Follow these steps to install the hardware:

1. For 32-Bit Windows install the software before installing the hardware. For UNIX and VxWorks systems install the hardware first, then the software.
2. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
3. Set the jumpers on the PMC-1553 module to the desired settings for your MIL-STD-1553 configuration. See the "Hardware Description" section for specific settings.
4. Attach the PMC-1553 to your carrier using the hardware provided.
5. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with your board (Front Panel version only.)

   The PMC I/O configuration is defined below. A transition cable is provided from the PMC I/O configuration to MIL-STD-1553 jacks and Trig IN/OUT jacks.

Note: If this is the last connection on the bus, use a "Tee" to connect a 78-ohm terminator to provide proper termination for the bus. Otherwise, use a "Tee" with a cable on each end. For "transformer", coupling, connect the bus "A" and "B" "stubs" to the connectors on the interface card.

PMC-1553 Board Layout



Figure 7. PMC-1553 Board Layout

Status LEDs

There are three status LEDs visible from the front panel of the PMC-1553:

- **Bottom LED (farthest from I/O connector) - FPGA Configuration Status** – Indicates the status of the Local Processing Unit (LPU) FPGA. Before FPGA configuration, the LED is off. Once the FPGA is configured successfully, the LED illuminates.
- **Center LED - Host Bus Activity** – Illuminates when the host bus is actively accessing the PMC-1553 board.
- **Top LED (nearest to I/O connector) - 1553 Bus Activity** – Illuminates when traffic is detected on the 1553 bus

PMC Connector Description

The PMC-1553 is a PMC board designed to PCI Specification 2.1. The PCI bus logic signals are routed through connectors P11 and P12.

The PMC-1553 uses a Champ-50 connector (P1) for the front panel I/O version. The I/O signals are routed to P14 for the rear panel I/O versions. (P1 is not installed on rear panel I/O versions.). Jumper block JB1 determines the destination of the 1553 signals.

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website..

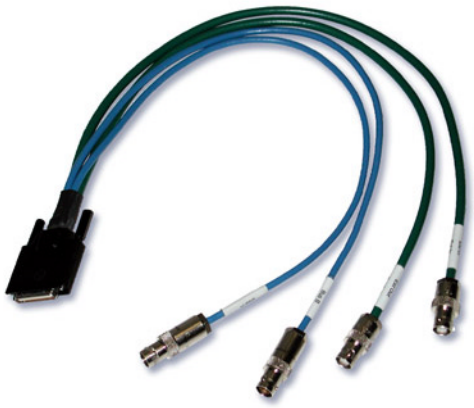


Figure 8. Transition Cable from each Champ 50 Connector on a cPCI-1553-IP or PMC-1553

PMC-1553 Rear Panel Pin Assignments

The following table specifies the rear panel connector pin assignments. Any pin not listed in the table is not connected to the PMC-1553 board.

Table 13. PMC-1553 Rear Panel Pin Assignments

Pin Number	Signal Name
1	BUS_A+
2	BUS_A-
3,4,7,8	BUS_SHIELDS
6	BUS_B+
5	BUS_B-
11	BUS_EXTIN
15	BUS_EXTOUT
19	BUS_RTA0
23	BUS_RTA1
27	BUS_RTA2
31	BUS_RTA3
35	BUS_RTA4
39	BUS_RTADP
9, 13, 17, 21, 25, 29, 33, 37, 43, 44, 59, 60	GROUNDS
42	JTAG TCK
46	JTAG TDO
50	JTAG TMS
58	JTAG TDI
41	Altera DCLK
45	Altera CONFIGDONE
47, 48	+5 volts filtered
49	Altera NCONFIG
53	Altera STATUSN
57	Altera DATA0

PMC-1553 Front Panel Pin Out

The front panel connector pin assignment is specified in Table 14.

Table 14. PMC-1553 Front Panel Pin Assignments

Pin Number	Signal Name
27	BUS_A+
29	BUS_A-
25, 31	BUS_SHIELD
33	BUS_B+
35	BUS_B-
3, 41	BUS_EXTIN
1, 39	BUS_EXTOUT
20	BUS_RTA0
18	BUS_RTA1
16	BUS_RTA2
14	BUS_RTA3
12	BUS_RTA4
22	BUS_RTADP
5, 11, 13, 17, 19, 21, 23	GROUND

Signal Descriptions

See chapter 13, “Interface Signals“ for a complete description of the 1553 interface signals.

Transformer versus Direct Coupling

MIL-STD-1553B allows for two methods of connecting a terminal to the bus:

- Transformer coupling provides noise immunity over long distances and requires external transformer couplers.
- Direct coupling is often used in the laboratory because it requires no transformers between boxes.

The software function BusTools_SetVoltage() *cannot* configure the coupling mode or the output voltage level. The PMC hardware sets the output amplitude to MIL-STD-1553B levels. To set the PMC-1553 board for either coupling method, you must install jumpers. The board comes with factory-installed jumpers for direct-coupled mode.

Be sure that only direct coupling or transformer-coupling jumpers are set at any given time. See Table 15 below.

Table 15. PMC-1553 Coupling Options

Function	JB1 Jumpers Installed
Front Panel Direct coupled, channel A	1-2, 10-11
Front Panel Transformer coupled, channel A	4-5, 7-8
Front Panel Direct coupled, channel B	13-14, 22-23
Front Panel Transformer coupled, channel B	16-17, 19-20
Rear Panel I/O Direct coupled, channel A	2-3, 11-12
Rear Panel I/O Transformer coupled, channel A	5-6, 8-9
Rear Panel I/O Direct coupled, channel B	14-15, 23-24
Rear Panel I/O Transformer coupled, channel B	17-18, 20-21

Note: The coupling method is set by these jumpers; the software function BusTools_SetVoltage() *cannot* be used to configure the coupling mode (or the output voltage level, which is fixed by the PMC hardware to MIL-STD-1553B levels).

MIL-STD-1553B Signals

A+ and A- are the differential pair for channel A. SHIELD is used in most environments to shield the cable used for the stub connections. B+ and B- are the differential pair for channel B. SHIELD is also used to shield the channel B pair. Both shields are tied together and to the center tap of the isolation transformers on the PMC-1553 board.

External Input

EXTIN is a TTL signal that is activated by a low to high transition. The minimum high pulse is 400 ns, but it may stay high indefinitely. When a pulse is high for 200 to 400 ns, it can't be determined whether it will produce an active input. EXTIN has one of four functions that are programmed in software: BC trigger, RT trigger, BM trigger and Reset Tag Timer.

This signal is an input of the Altera 10K50, is pulled up to +5 volts by a 4.7K ohm resistor located on the board, and is protected by a 100 ohm series resistor and diodes to both VCC and Ground.

See chapter 13, "Interface Signals", for a complete description of the functions of the discrete input signal.

External Output

EXTOUT is an active high TTL signal that goes active for 50 microseconds. Firing this output is under software control. It may be enabled for BM trigger or RT Synchronize Mode Code.

This signal is an output of the Altera 10K50, and is protected by a 100-ohm series resistor and diodes to both VCC and Ground.

See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete output signal.

External Hardwired RT Address

This feature is currently not implemented but could be if requested. The RTAD[4…0] signals are used to externally hardwire the boards to respond as a single RT. The RTADP is the parity signal. If the RT address is hardwired, the board is not able to simulate the Bus Controller or to respond to any other RT address even when so enabled by the software.

See chapter 13, “Interface Signals”, for a complete description of the external RT address discrete inputs.

Memory Map Issues

The PMC-1553 requires a 32-megabyte address block. The BIOS maps the PMC-1553 board into memory space at an address above the total amount of RAM in the computer. The supplied software supports the PMC-1553 under 32-Bit Windows, and Linux.

CHAPTER 7

QPMC-1553 Installation

QPMC-1553 Installation Procedure

This section explains how to install the QPMC-1553 board. The QPMC-1553 is a single, dual or quad channel 1553 interface board on PMC board.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

The QPMC-1553 board is a Plug-and-Play board. There are no switches or jumpers on the board required for software installation.

1. For 32-Bit Windows install the software before installing the hardware. For UNIX and VxWorks systems install the hardware first, then the software.

2. Using the supplied software disks, follow the instructions in the "Quick Start" installation guide.

   Be sure to follow the instructions applicable to your operating system.

3. If you install on a 32-Bit Windows systems (Windows 95/98/NT/2000/Me/XP) you must restart you compete after installation.

Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
2. Attach the QPMC-1553 to your carrier using the hardware provided.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with your board (Front Panel version only.)

   The QPMC I/O configuration is defined below. A transition cable is provided from the QPMC I/O connector to MIL-STD-1553 cable jacks and a D50 connector for other I/O signals.

Note: If this is the last connection on the bus, use a "Tee" to connect a 78-ohm terminator to provide proper termination for the bus. Otherwise, use a "Tee" with a cable on each end. For "transformer", coupling, connect the bus "A" and "B" "stubs" to the connectors on the interface card.

QPMC-1553 Board Layout

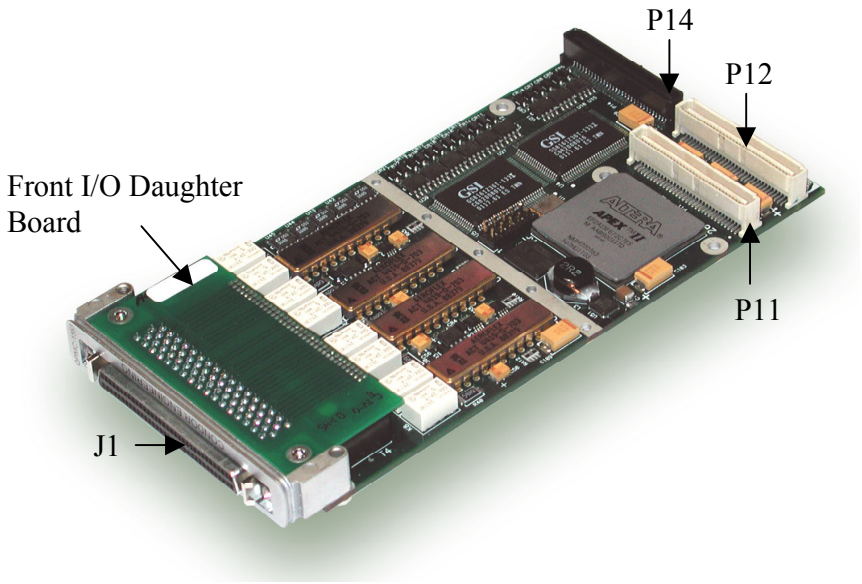


Figure 9. QPMC-1553 Board Layout

Status LEDs

There are six bi-colored status LEDs on the backside of the QPMC-1553:

- **B0, B1, B2, B3 LED's - 1553 Bus Activity** – The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic and illuminates red if that channel runs internally (transceiver transmit is inhibited).
- **CFG OK LED – Configuration Status** – Red prior to FPGA configuration. Green upon successful FPGA configuration.

QPMC Connector Description

The QPMC-1553 is designed to PCI Specification 2.2. The PCI bus logic signals route through connectors P11 and P12.

The QPMC-1553 uses a daughter board with a 68 pin SCSI connector (J1) on the front panel I/O version. The I/O signals are routed to P14 for the rear panel I/O versions.

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website..

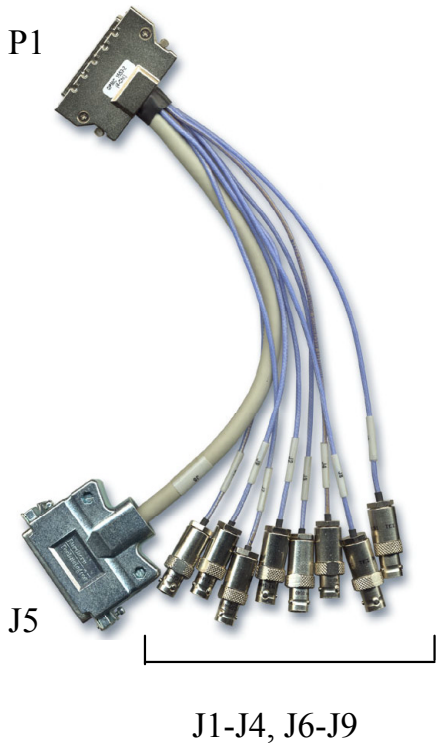


Figure 10. Transition Cable for QPMC1553 (4-channel cable shown)

QPMC-1553 P14 Pin Assignments

The following table specifies the rear panel connector pin assignments.

Table 16. QPMC-1553 P14 Pin Assignments

P14 Connector Assignments			
Pin	**Function**	**Pin**	**Function**
1	RTADDR2_P/ ADISC14	2	RTADDR1_P/ ADISC6
3	GND	4	RTADDR1_4/ ADISC5
5	ADISC15	6	RTADDR1_3/ ADISC4
7	--	8	--
9	ADISC16	10	HWRT_EN
11	--	12	--
13	ADISC17	14	RTADDR1_2/ ADISC3
15	GND	16	1553 CH2A-
17	ADISC18	18	1553 CH2A+
19	GND	20	1553 Shield
21	RTADDR2_4/ ADISC13	22	1553 CH2B-
23	GND	24	1553 CH2B+
25	GND	26	GND
27	1553 CH3B+	28	1553 CH3A-
29	ADISC7	30	1553 CH3A+
31	GND	32	1553 CH3B-
33	GND	34	GND
35	ADISC8	36	1553 CH1B-
37	GND	38	1553 CH1B+
39	RTADDR2_0/ ADISC9	40	GND
41	--	42	--
43	RTADDR2_1/ ADISC10	44	RTADDR1_1/ ADISC2
45	--	46	--
47	RTADDR2_2/ ADISC11	48	RTADDR1_0/ ADISC1
49	GND	50	1553 CH1A-
51	RTADDR2_3/ ADISC12	52	1553 CH1A+
53	IRIGB OUT	54	IRIGB IN
55	GND	56	IRIGB GND
57	GND	58	EXT_IN-
59	1553 Shield	60	EXT_IN+
61	1553 CH4B-	62	1553 CH4A-
63	1553 CH4B+	64	1553 CH4A+

QPMC-1553 Front Panel Pin Out

The front panel connector pin assignment is specified in the following table.

Table 17. QPMC-1553 Front Panel Pin Assignments

Front Bezel Connector (J1)			
Pin	**Function**	**Pin**	**Function**
1	1553 CH1A+	35	ADISC7
2	1553 CH 1A-	36	ADISC8
3	1553 Shield	37	RTADDR2_0/ ADISC9
4	GND	38	RTADDR2_1/ ADISC10
5	1553 CH 1B+	39	--
6	1553 CH 1B-	40	--
7	1553 Shield	41	GND
8	RTADDR1_0/ ADISC1	42	EXT_IN+
9	RTADDR1_1/ ADISC2	43	EXT_IN-
10	1553 CH 2A+	44	RTADDR2_2/ ADISC11
11	1553 CH 2A-	45	RTADDR2_3/ ADISC12
12	1553 Shield	46	GND
13	GND	47	GND
14	1553 CH 2B+	48	--
15	1553 CH 2B-	49	--
16	1553 Shield	50	GND
17	RTADDR1_2/ ADISC3	51	IRIGB IN
18	RTADDR1_3/ ADISC4	52	IRIGB OUT
19	1553 CH 3A+	53	IRIGB GND
20	1553 CH 3A-	54	GND
21	1553 Shield	55	RTADDR2_4/ ADISC13
22	GND	56	RTADDR2_P/ ADISC14
23	1553 CH 3B+	57	ADISC15
24	1553 CH 3B-	58	ADISC16
25	1553 Shield	59	--
26	HWRT_EN	60	--
27	GND	61	GND
28	1553 CH 4A+	62	ADISC17
29	1553 CH 4A-	63	ADISC18
30	1553 Shield	64	RTADDR1_4/ ADISC5
31	GND	65	RTADDR1_P/ ADISC6
32	1553 CH 4B+	66	--
33	1553 CH 4B-	67	--
34	1553 Shield	68	GND

QPMC-1553 Transition Cable

The pinouts for the QPMC transition cable are provided in the following two tables.

Table 18. QPMC-1553 Transition Cable Pin Assignments

Transition Cable J5 Pinout			
1	RTADDR1_0/ ADSIC 1	26	ADSIC 16
2	RTADDR1_1/ ADSIC 2	27	ADSIC 17
3	GND	28	ADSIC 18
4	RTADDR1_2/ ADSIC 3	29	GND
5	RTADDR1_3/ ADSIC 4	30	-
6	GND	31	-
7	RTADDR1_4/ ADSIC 5	32	-
8	RTADDR1_P/ ADSIC 6	33	-
9	ADSIC 7	34	-
10	ADSIC 8	35	-
11	RTADDR2_0/ ADSIC 9	36	GND
12	GND	37	-
13	EXT CLK+	38	-
14	EXT CLK -	39	GND
15	HWRT_EN (low true)	40	-
16	GND	41	-
17	-	42	GND
18	RTADD2_1/ ADSIC 10	43	EXT_IN+
19	RTADD2_2/ ADSIC 11	44	EXT_OUT-
20	RTADD2_3/ ADSIC 12	45	GND
21	GND	46	IRIGB IN
22	RTADD2_4/ ADSIC 13	47	IRIGB OUT
23	RTADD2_P/ ADSIC 14	48	IRIGB GND
24	ADSIC 15	49	-
25	GND	50	GND (overall shield)

Table 19. Transition Cable 1553 Connectors

Transition Cable 1553 Connectors	
Connector	***Signal***
J1	*Channel 1, Bus A*
J2	*Channel 1, Bus B*
J3	*Channel 2, Bus A*
J4	*Channel 2, Bus B*
J6	*Channel 3, Bus A*
J7	*Channel 3, Bus B*
J8	*Channel 4, Bus A*
J9	*Channel 4, Bus B*

Signal Descriptions

See chapter 13, “Interface Signals”, for a complete description of the 1553 interface signals.

MIL-STD-1553B Signals

1553 CH*n*A+ and 1553 CH*n*A- are the differential pair for bus A. 1553 CH*n* B+ and 1553 CH*n* B- are the differential pair for bus B. 1553 SHIELD is tied to the center tap of all the isolation transformers on the QPMC-1553 board and should be used as the overall shield for each differential pair.

IRIG Signaling

IRIG time may be received on the signals IRIG IN and IRIG GND. The following IRIG formats are accepted:

Format	Modulation Frequency	Frequency/ Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

When enabled by the software, IRIG OUT will transmit IRIG B002 data from the onboard IRIG encoder. IRIG OUT signal can source/sink 16 mA at valid TTL levels.

Memory Map Issues

The QPMC-1553 requires an 8-megabyte address block. The BIOS maps the QPMC-1553 board into memory space at an address above the total amount of RAM in the computer.

CHAPTER 8

PCCARD-1553 Installation

Installation Procedure

This section tells how to install the PCCARD-1553 board. The PCCARD-1553 is a PCMCIA card with a single 1553 Channel.

Pre-installation Procedure

Before you begin, inspect the packaging material to insure that the board is not damaged from shipping. If it has, contact the shipper right away.

The PCCARD-1553 installs into the PC Card Reader or PCMCIA slot on your computer. You must have a PC Card Reader on your host computer before you can install the PCCARD-1553.

Software Installation

1. Check your system for memory and I/O conflicts and select the desired memory and I/O addresses and hardware interrupt for the board. See the "Quick Start" installation guide.
2. Using the supplied software disks, install the software. Be sure to follow the instructions in the "Quick Start" installation guide for your operating system.
3. When the software installation is complete, power the computer off.

Hardware Installation

After installing the software, follow the steps below to install the hardware.

Windows NT 4.0

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag.

   This prevents static discharge from damaging the board when you change the jumpers.

2. Turn-off the power to the PC and insert the PCCARD-1553 into the lower PC Card slot.

   The upper PC Card slot on many older laptop PCs is not compatible with the PCCARD-1553 device. On newer PCs, the PCCARD-1553 can function in the upper PC Card slot.

3. Power-up the computer. The driver should be loaded automatically upon power-up.

32-Bit Windows

1. After installing the software install the PCCARD-1553 and restart your system.

   The Windows 98/95 Plug and Play hardware manager should detect new hardware and configure the drivers for your board.

2. When prompted, reboot your computer.

Windows 95

1. If the *New Hardware Found* dialog box doesn't appear when you start your system, select Add New Hardware from the Control Panel.
2. If Windows 95 does not automatically detect the device drivers and it prompts you for a path to the driver location, enter C:\Windows\Inf\Other and click OK.

Windows 98

1. When the *Add New Hardware* dialog box detects the new hardware with its corresponding device number next to the hardware device, click NEXT.
2. Select "*Display a list of all the drivers in a specific location, so you can select the driver you want*." Click NEXT.

3. When the hardware you are installing appears in the Models Window, select the device and click NEXT.

   If nothing appears, go to step 5. Click NEXT again.

4. Click FINISH, then Click YES to reboot.
5. If the *New Hardware Found* dialog box does not come up when you start your system, select Add New Hardware from the Control Panel.
6. If the device drivers are not automatically detected and you are prompted for a path to the driver location, enter C:\Windows\Inf\Other and click OK.

Connect the supplied transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly. The PCCARD-1553 I/O configuration is defined below.

Note: If you are using “transformer” coupling, connect the bus “A” and “B” “stubs” from the transformers to the connectors on the transition cable.

If you are using “direct” coupling and this is the last connection on the bus a “Tee” should be used and a 78-ohm terminator should be connected to provide the proper termination for the bus. Otherwise, use a “Tee” with a cable on each end of the “Tee”.

Board Layout

Figure 11 shows the location of the connectors.

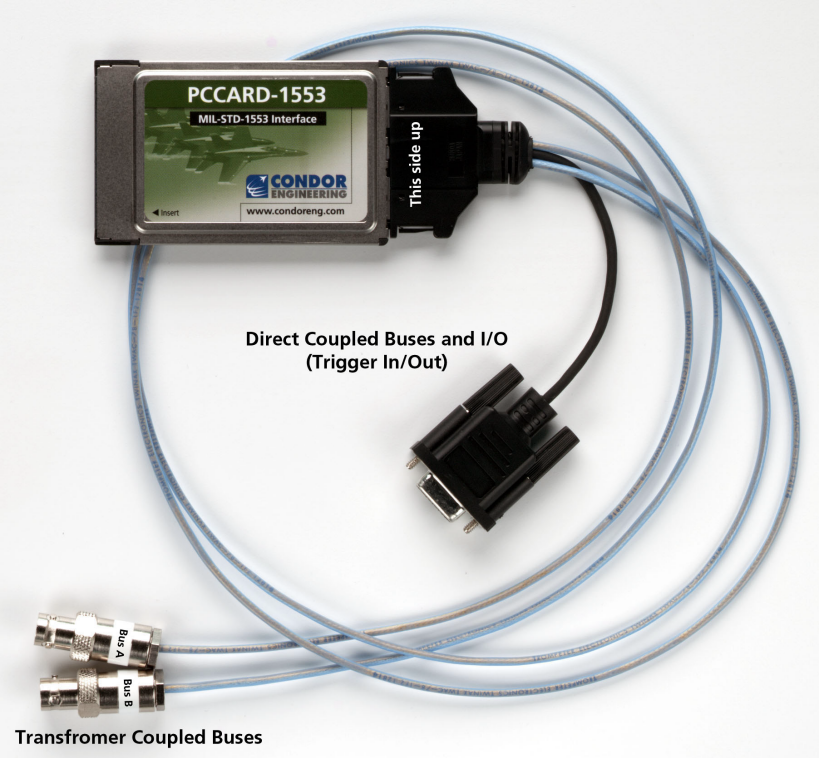


Figure 11. PCCARD-1553 Card with Transition Cable Attached

PCCARD-1553 Connector Description

The PCCARD-1553 connector P1 implements the PCMCIA interface. The PCCARD-1553 P2 connector is intended to connect to the supplied transition cable.

PCCARD-1553 Transition Cables

The transition cable supplied with the PCCARD-1553 provides access to the 1553 and I/O signals. When connected to the P2 connector of the PCCARD-1553 this transition cable provides two twin-ax connectors for connection to the transformer coupled “A” and “B” 1553 busses (J1 and J2 respectively). It also has a 9-pin female D-subminiature type connector (P2) that provides the signals as described in the following pin assignments table:

Table 20. PCCARD-1553 Pin Assignments

P2, Transition Cable	
Pin Number	**Signal Name**
1	Bus A+, direct coupled
2	Bus A-, direct coupled
3	Bus A shield
4	EXTIN, IRIG IN
5	GND
6	Bus B+, direct coupled
7	Bus B-, direct coupled
8	Bus B shield
9	EXTOUT, IRIG OUT



Figure 12. PCMCIA 33 Pin Doublewide Connector for PCCard-1553

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website..

1553 - Bus Coupling

Bus outputs can be coupled in two different manners:

- Direct coupled (short stub) - Isolation Transformer 1.4:1
- Transformer coupled (long stub)

Use direct coupling when the distance from the board's isolation transformer to the data bus is one-foot or less. Use transformer coupling when the distance exceeds one-foot, but is less than 25 feet.

There are isolation transformers on the board for both direct and transformer coupling. There are 53.6-ohm isolation resistors on the board for direct coupling. Transformer coupling requires an external

transformer and isolation resistor at the junction to the main 1553 bus to match the stub impedance to the bus. (The Air Force mandates the use of transformer coupling).

The manner of bus coupling is determined by the transition cable connection chosen by the user, J1 and J2 for transformer coupling and P2 for direct coupling.

External Input

The External Input signal line is shared between EXTIN, a trigger input, and IRIG IN, the IRIG decoder input. The selection of EXTIN or IRIG is under software control through the API. For a complete explanation of IRIG selection and use, see the "Universal Core Architecture Reference" manual.

A low to high transition triggers the EXTIN, TTL signal. The minimum high pulse is 400 ns, but it may stay high indefinitely. When a pulse is high for 200 to 400 ns, it is indeterminate whether it will produce an active input. EXTIN has one of four functions that are programmed in software:

- BC trigger
- RT trigger
- BM trigger
- Reset Tag Timer.

EXTIN signal is pulled low through a 4.7KΩ resistor and passed through a 4.7KΩ series resistor to an input pin of an Altera Apex 20KE FPGA device using 3.3V I/O and its internal PCI clamp diode enabled.

See chapter 13 "Interface Signals", for a complete description of the functions of the discrete input signal.

External Output

The External Output signal line is shared between EXTOUT, a trigger output, and IRIG OUT, the IRIG generator output. The selection of EXTOUT or IRIG is under software control through the API. For a complete explanation of IRIG selection, see the "Universal Core Architecture Reference manual".

EXTOUT is an active high TTL signal that goes active for 50 microseconds. Software controls the firing of this output. You may enable this output for BM trigger or RT Synchronize mode code. This

signal is an output pin of an Altera Apex 20KE FPGA device using 3.3V I/O and its internal PCI clamp diode enabled

See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete output signal.

PCCARD-1553 Memory Map Issues

The PCCARD-1553 board may be mapped into any available 8K-byte block in upper memory between segment addresses A000:0000 and E400:0000 (physical addresses A0000 to E4000 hexadecimal). The memory address is used by Card Service to map the PCCARD-1553 memory and must not conflict with any other device. The PCCARD-1553 memory is paged by an internal page register, which is accessed in memory space at word-offset 0x08 (See the “MIL-STD-1553 Universal Core Architecture Reference Manual” for more information).

When using any program to determine if a memory or I/O space is available for use remember that most such programs only report what the operating system knows. If no operating system driver has been installed for a memory or I/O region, the program might report that it is available, even if some device is really using that region.

Keep in mind that if multiple boards are being used in the same platform, then sufficient memory space must be available for each board.

The “Quick Start” installation guide lists specific steps that might assist you in determining which upper memory address space is available.

Interrupt Line Select (IRQ3-7, 9-12, 14-15)

The PCCARD-1553 board features software-programmable interrupt line selection. There are no interrupt jumpers to set. However, you still must choose the interrupt to use, one that isn’t being used by another board.

When installing the software for 32-Bit Windows you are asked to select the hardware interrupt number. Selecting “0” disables the hardware interrupts; the API defaults to polling the board.

Many PCMCIA controllers do not adequately document their own interrupt routing from the Card, through Card Services, then to the system. Therefore, enabling interrupts without complete knowledge of the system may lead to unexpected conditions.

CHAPTER 9

QVME-1553, VME-1553, QVXI-1553X, and VXI-1553 Installation

QVME/VME/QVXI/VXI-1553 Installation Procedure

This section tells how to install the QVME/VME/VXI-1553 hardware and software.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.
2. If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.
3. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

1. Using the supplied software disks, follow the instructions in the “Quick Start” installation guide.
2. Be sure to follow the instructions applicable to your operating system.

Hardware Installation

Follow these steps to install the hardware:

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
2. Install the board into your VME chassis. Take into account the other VME boards in the chassis and chassis design when installing the board.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with your board.

   Table 21 and Table 22 show the VME I/O configuration. A transition cable is provided from the VME I/O configuration to MIL-STD-1553 jacks and Trig IN/OUT jacks.

Note: If this is the last connection on the bus, use a “Tee” to connect a 78-ohm terminator to provide proper termination for the bus. Otherwise, use a “Tee” with a cable on each end. For “transformer”, coupling, connect the bus “A” and “B” “stubs” to the connectors on the interface card.

VME-1553 Board Layout

Figure 13 shows the VME-1553 board with 4 separate 1553 channels labeled Channel 1 through Channel 4.

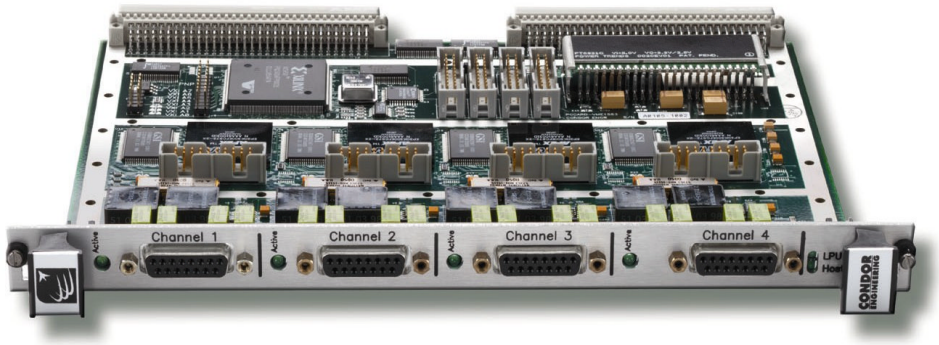


Figure 13. VME-1553 Board Layout

QVME-1553 Board Layout

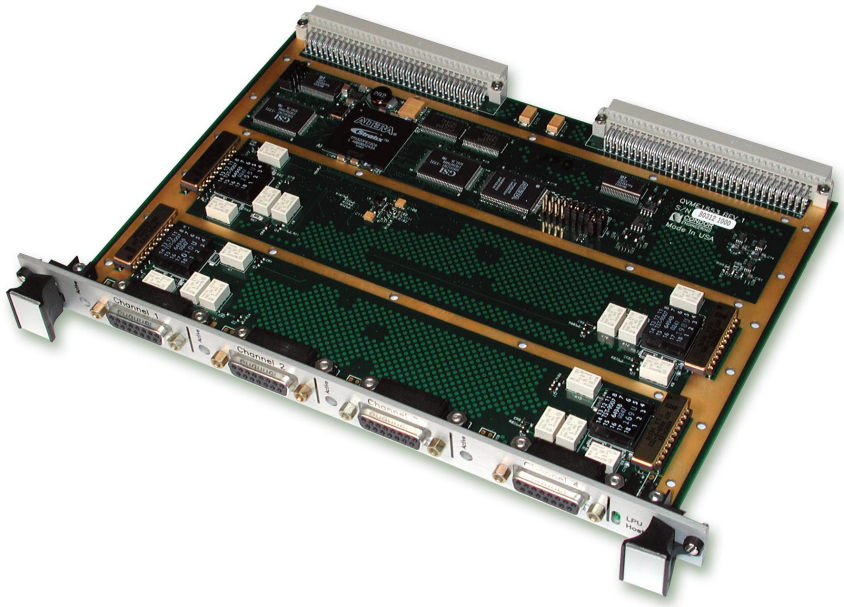


Figure 14. QVME-1553 BoardLayout

VXI-1553 Board Layout



Figure 15. VXI-1553 Board Layout.

VME Front Panel Connector Description

The QVME/VME/QVXI/VXI-1553 provides four DB15 front panel connectors, P3 through P6. These boards have one-channel, two-channel, and four-channel configurations available. Table 21 shows the pin assignments.

Table 21. QVME/VME/QVXI/VXI-1553 Front Panel Pin Assignments

Front Panel Connector Px Channel n Interface	
Pin Number	**Signal Name**
1	BUSn_B+
2	BUSn_B-
3	GND
4	BUSn_A+

Front Panel Connector Px Channel n Interface	
Pin Number	**Signal Name**
5	BUSn_A-
6	BUSn_SHIELD
7	BUSn_EXTIN
8	BUSn_EXTOUT
9	BUSn_SHIELD
10	No connection
11	GND*
12	IRIGB_IN*
13	IRIGB_GND*
14	GND*
15	IRIGB_OUT*

Note: *These signals available on QVME-1553 and QVXI-1553X only, no connection on VME/VXI-1553

Connector Px where x stands for 3 (Channel 1), 4 (Channel 2), 5 (Channel 3), or 6 (Channel 4). Channel n where n stands for 1,2,3, or 4.

QVME/VME/QVXI/VXI-1553 Transition Cables

The VME-1553 is supplied with one, two, or four transition cables (Figure 3), which mate with the DB15 connectors on the board and provide 1553 cable jacks for mating with customer-supplied 1553 wiring.

These transition cables also route the discrete input and output signals to BNC-type connectors.

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website..

VME-1553 P2 Connector

Table 22. VME-1553 P2 Connector Pinout

Pin	Row A	Row B	Row C
1	CH0_RTA0	+5 VDC	CH2_RTA0
2	CH0_RTA1	GND	CH2_RTA1
3	CH0_RTA2	N/C	CH2_RTA2
4	CH0_RTA3	A24	CH2_RTA3
5	CH0_RTA4	A25	CH2_RTA4
6	CH0_RTADP	A26	CH2_RTADP
7	CH0_SHIELD	A27	CH2_SHIELD
8	CH0 A+	A28	CH2 A+
9	CH0 A-	A29	CH2 A-
10	CH0 B+	A30	CH2 B+
11	CH0 B-	A31	CH2 B-
12	CH0_TRIG_IN_EXT	GND	CH2_TRIG_IN_EXT
13	CH0_TRIG_OUT_EXT	+5 VDC	CH2_TRIG_OUT_EXT
14	CH1 A+	D16	CH3 A+
15	CH1 A-	D17	CH3 A-
16	CH1 B+	D18	CH3 B+
17	CH1 B-	D19	CH3 B-
18	CH1_SHIELD	D20	CH3_SHIELD
19	GND	D21	CH3_RTA0
20	EXT CLK+	D22	CH3_RTA1
21	EXT CLK-	D23	CH3_RTA2
22	CH1_RTA0	GND	CH3_RTA3
23	CH1_RTA1	D24	CH3_RTA4
24	CH1_RTA2	D25	CH3_RTADP
25	CH1_RTA3	D26	CH3_TRIG_IN_EXT
26	CH1_RTA4	D27	CH3_TRIG_OUT_EXT
27	CH1_RTADP	D28	CH1_RX
28	CH1_TRIG_IN_EXT	D29	CH1_TX
29	CH1_TRIG_OUT_EXT	D30	CH2_RX
30	MODID	D31	CH2_TX
31	CH0_RX	GND	CH3_RX
32	CH0_TX	+5 VDC	CH3_TX

VXI-1553 P2 Connector

Table 23. VXI-1553 P2 Connector Pinout

Pin	Row A	Row B	Row C
1	n.c.	+5 VDC	n.c.
2	n.c.	GND	n.c.
3	n.c.	N/C	n.c.
4	n.c.	A24	n.c.
5	n.c.	A25	n.c.
6	n.c.	A26	n.c.
7	n.c.	A27	n.c.
8	n.c.	A28	n.c.
9	n.c.	A29	n.c.
10	n.c.	A30	n.c.
11	n.c.	A31	n.c.
12	n.c.	GND	n.c.
13	n.c.	+5 VDC	n.c.
14	n.c.	D16	n.c.
15	n.c.	D17	n.c.
16	n.c.	D18	n.c.
17	n.c.	D19	n.c.
18	n.c.	D20	n.c.
19	n.c.	D21	n.c.
20	n.c.	D22	n.c.
21	n.c.	D23	n.c.
22	n.c.	GND	n.c.
23	n.c.	D24	n.c.
24	n.c.	D25	n.c.
25	n.c.	D26	n.c.
26	n.c.	D27	n.c.
27	n.c.	D28	n.c.
28	n.c.	D29	n.c.
29	n.c.	D30	n.c.
30	MODID	D31	n.c.
31	n.c.	GND	n.c.
32	n.c.	+5 VDC	n.c.

QVME-1553 P2 Connector

Table 24. QVME-1553 P2 Connector Pinout

Pin	Row A	Row B	Row C
1	CH0_RTA0	+5 VDC	CH2_RTA0
2	CH0_RTA1	GND	CH2_RTA1
3	CH0_RTA2	N/C	CH2_RTA2
4	CH0_RTA3	A24	CH2_RTA3
5	CH0_RTA4	A25	CH2_RTA4
6	CH0_RTADP	A26	CH2_RTADP
7	CH0_SHIELD	A27	CH2_SHIELD
8	CH0 A+	A28	CH2 A+
9	CH0 A-	A29	CH2 A-
10	CH0 B+	A30	CH2 B+
11	CH0 B-	A31	CH2 B-
12	CH0_TRIG_IN_EXT	GND	CH2_TRIG_IN_EXT
13	CH0_TRIG_OUT_EXT	+5 VDC	CH2_TRIG_OUT_EXT
14	CH1 A+	D16	CH3 A+
15	CH1 A-	D17	CH3 A-
16	CH1 B+	D18	CH3 B+
17	CH1 B-	D19	CH3 B-
18	CH1_SHIELD	D20	CH3_SHIELD
19	GND	D21	CH3_RTA0
20	IRIGB_IN	D22	CH3_RTA1RTA1
21	IRIGB_GND	D23	CH3_RTA2H3_RTA2
22	CH1_RTA0	GND	CH3_RTA3
23	CH1_RTA1	D24	CH3_RTA4
24	CH1_RTA2	D25	CH3_RTADP
25	CH1_RTA3	D26	CH3_TRIG_IN_EXT
26	CH1_RTA4	D27	CH3_TRIG_OUT_EXT
27	CH1_RTADP	D28	DISCRETE_1
28	CH1_TRIG_IN_EXT	D29	DISCRETE_2
29	CH1_TRIG_OUT_EXT	D30	GND
30	MODID	D31	DISCRETE_3
31	IRIGB_OUT	GND	DISCRETE_4
32	CH0_TX	+5 VDC	GND

QVXI-1553X P2 Connector

Since the QVXI-1553 consists of a QVME-1553 installed on a C-size VME to VXI extender, rear I/O is limited to the 32-bit VME interface specified by the VXI Consortium. No rear I/O is supported in this configuration.

However, these signals may be brought to the front panel through an adapter available from the extender manufacturer.

Signal Descriptions

See chapter 13, “Interface Signals”, for a complete description of the 1553 interface signals.

Transformer versus Direct Coupling

MIL-STD-1553B allows for two methods of connecting a terminal to the bus.

- Transformer coupling provides noise immunity over long distances and requires external transformer couplers.
- Direct coupling is often used in the laboratory because it requires no transformers between boxes.

Set either transformer and direct coupling by calling the API function BusTools_SetVoltage(), and setting the coupling option.

You may order certain board configurations with Fixed Amplitude transceivers installed on the card. In such a case, the outputs are fixed at MIL-STD output levels, and issuing the command above will not influence the card’s output amplitude.

MIL-STD-1553B Signals

A+ and A- are the differential pair for channel A. SHIELD is used in most environments to shield the cable used for the stub connections. B+ and B- are the differential pair for channel B. SHIELD is also used to shield the channel B pair. Both shields are tied together and to the center tap of the isolation transformers on the VME-1553 board.

External Input

On VME/VXI-1553 EXTIN is a TTL signal that is activated by a low to high transition. The minimum high pulse is 400 ns, but it may stay high indefinitely. A pulse high for 200 to 400 ns does not reliably produce an active input. EXTIN has one of four functions that are programmed in software: BC trigger, RT trigger, BM trigger and Reset Tag Timer.

This signal is an input of the APEX 20K300E with it's PCI clamp diode enabled, is pulled up to +3.3 volts by a 4.7K ohm resistor located on the board, and is protected by a 4.7K ohm series resistor.

See chapter 13, "Interface Signals", for a complete description of the functions of the external input signal.

External Output

On VME/VXI-1553 EXTOUT is an active high TTL signal that goes active for 50 microseconds. Firing this output is under software control. It may be enabled for BM trigger or RT Synchronize Mode Code.

This signal is an output of the APEX 20K300E with its PCI clamp diode enabled, and is protected by a 4.7K-ohm series.

See chapter 13, "Interface Signals", for a complete description of the functions of the discrete output signal.

Discrete I/O

The QVME-1553 has four discrete I/O pins available on the VME P2 connector. See chapter 13, "Interface Signals", for a complete description of the functions of the discrete signals.

The QVXI-1553X has four discrete I/O pins available on the VME P2 connector. Routing these to the backplane through the jumper connector provided with the VXI extender is not recommended. However, these signals may be brought to the front panel through an adapter available from the extender manufacturer. See chapter 13, "Interface Signals", for a complete description of the functions of the discrete signals.

IRIG Signaling

The QVME-1553 has IRIG-B capability. IRIG time may be received on the signals IRIG IN and IRIG GND. The following IRIG formats are accepted:

Format	Modulation Frequency	Frequency/ Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

When enabled by the software, IRIG OUT will transmit IRIG B002 data from the onboard IRIG encoder. IRIG OUT signal can source/sink 16 mA at valid TTL levels.

Memory Map Issues

The VME-1553 uses A16 addressing for the configuration register and A24 or A32 for addressing the 1553 channels. The base address of the A16 configuration register is (ID * 0x40) + 0xC000. You set ID using the eight VXI jumpers (VXI A0 – VXI A7) on JB1. These jumpers are asserted (1) when unconnected and de-asserted (0) when connected. This provides a range of A16 addresses from 0xC000 to FFC0. Make sure to specify a 0x40 byte region within this range and that does not interfere with any other devices.

The VME-1553 uses an eight-megabyte address block to address up to four separate 1553 channels. This allows both A24 and A32 addressing to access all channels. The base address for the board is programmable. You supply this address during initialization. You must select a base address with sufficient room to allow mapping eight-megabytes without interfering with other devices in the system.

You program the A24/A32 address by writing the board's base address to the offset register (byte address offset 6) in the A16 configuration space. You select A24 or A32 addressing by writing to bit 3 of the Control Register (byte address offset 8). Writing a 0 selects A24 addressing, writing a 1 selects A32 address. If you select A32 addressing you must select a base address on an even 512-Kbyte boundary. If you select A24 addressing, you can only select 0x0 or 0x800000 as the base address. Refer to the "MIL-STD-1553 Universal Core Architecture Reference Manual" (1600100-0001) for details of the A16 register usage.

The supplied software supports the VME-1553 under 32-Bit Windows using National Instruments NI-VXI interface and VxWorks.

CHAPTER 10

Q104-1553 and Q104-1553-P Installation

Installation Procedure

This section explains how to install the Q104-1553 and Q104-1553-P boards. The Q104-1553 is an ISA bus PC/104 form factor board. The Q104-1553-P is a PCI bus PC/104-*Plus* form factor board.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

1. Check your system for memory and I/O conflicts and select the desired memory and I/O addresses and hardware interrupt for the board.

   See the "Quick Start" installation guide.

2. Using the supplied software disks, install the software.

   Be sure to follow the instructions in the "Software Installation Manual" for the operating system you intend to use. When the software installation is complete, you must power the computer off.

Hardware Installation

After installing the software, follow the steps to install the hardware:

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you change the jumpers.
2. The Q104 uses jumpers to select installation location. Boards that are configured for the ISA interface (Q104-1553) use JB1 to select ISA base address. Boards that use the PCI interface (Q104-1553-P) use the jumpers at JB1 to select the PC/104-*Plus* stack location.
3. Set the jumpers on the Q104-1553 board to the desired settings for your operating system.
4. Insert the board into your PC/104 chassis. Note that mount hardware is captive to the ISA and PCI connectors (where applicable.)
5. A mating connector and retaining clip is provided for the I/O interface.

Note: If you are using “transformer” coupling, than connect the bus “A” and “B” “stubs” from the transformers to the connectors on the board.

If you are using “direct” coupling and this is the last connection on the bus a “Tee” should be used and a 78-ohm terminator should be connected to provide the proper termination for the bus. Otherwise, use a “Tee” with a cable on each end of the “Tee”.

Board Layout

Figure 16, shows the location of the connectors.

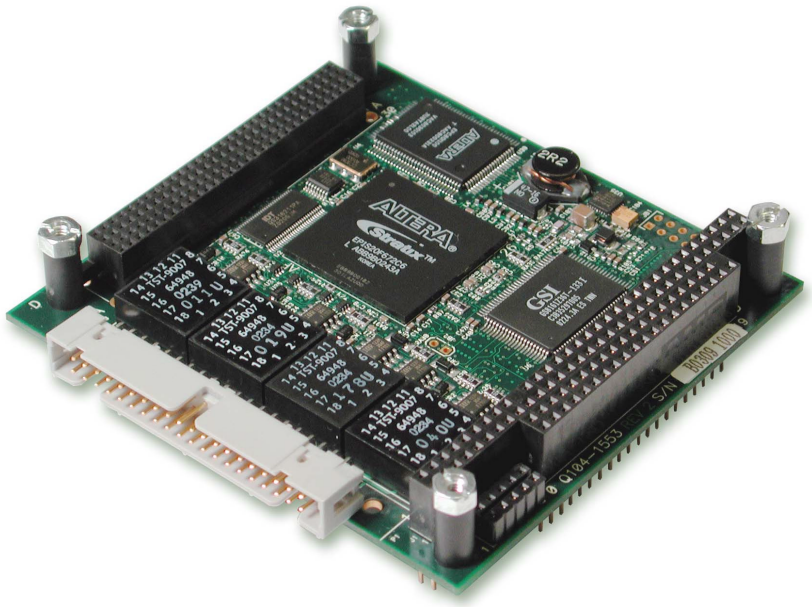


Figure 16. Q104-1553, Shown with Optional PC/104-*Plus* Connector Installed

Q104-1553 and Q104-1553-P Connector Description

The Q104-1553 connectors J1 and J2 implement the 16-bit ISA bus interface. Additionally, on Q104-1553-P configurations, J3 is installed for the *Plus* PCI interface.

The board I/O signals are all routed to connector P1. Signal assignments are listed in Table 23.

Table 25. Q104-1553 P1 Connector Pin Assignments

P1 connector			
Pin	**Function**	**Pin**	**Function**
1	1553_CH1 A+	21	1553_CH2 Shield
2	1553_CH1 Shield	22	Discrete I/O 5
3	1553_CH1 A-	23	1553_CH2 B+
4	GND	24	GND

P1 connector			
Pin	**Function**	**Pin**	**Function**
5	1553_CH1 B+	25	1553_CH2 B-
6	RS-485 Shield	26	Discrete I/O 6
7	1553_CH1 B-	27	1553_CH3 A+
8	IRIGB Return	28	Discrete I/O 7
9	RS-485 0+	29	1553_CH3 A-
10	IRIGB In	30	Discrete I/O 8
11	RS-485 0-	31	1553_CH3 Shield
12	IRIGB Out	32	Discrete I/O 9
13	RS-485 1+	33	1553_CH3 B+
14	Discrete I/O 1	34	Discrete I/O 10
15	RS-485 1-	35	1553_CH3 B-
16	Discrete I/O 2	36	1553_CH4 B-
17	1553_CH2 A+	37	1553_CH4 A+
18	Discrete I/O 3	38	1553_CH4 B+
19	1553_CH2 A-	39	1553_CH4 A-
20	Discrete I/O 4	40	1553_CH4 Shield

Note: P1 pin assignments flow from pin 1 to pin 40 as would be seen from the perspective of a ribbon cable assembly. Therefore, pins 1 and 2 are top-bottom adjacent on the connector and ribbon, located nearest the PC/104 connector, J1.

Q104-1553 and Q104-1553-P Transition Assemblies

The Q104-1553 and Q104-1553-P ships with a connector mate for P1, which may be used to assemble a custom cable to mate to MIL-STD-1553 wiring. Unless the Direct Coupled order-option has been selected, customer wiring should route to standard Coupling Transformers on the target MIL-STD-1553 system. All user cables must conform to MIL-STD-1553 requirements to ensure signal integrity between the Q104 and other bus agents.

This cable may also be built to route the discrete input and output, IRIG B, and RS-485 signals to the target hardware.

1553 - Bus Coupling

The Q104-1553 and Q104-1553-P provides Transformer Coupled 1553 connections at P1 as the standard configuration. Direct Coupled connection is available on the same pins by special-order. Contact Condor Sales for ordering information.

Note the following differences between Transformer and Direct Coupled options:

- Direct coupled (short stub) – Isolation Transformer 1.4:1
- Transformer coupled (long stub)

Use direct coupling when the distance from the isolation transformer to the data bus is less than or equal to one-foot. Use transformer coupling when the distance exceeds one-foot, but is less than 25 feet.

Isolation transformers on the board provide for both direct and transformer coupling, while the particular interface used is specified by the product ordering code. The standard configuration is Transformer Coupled. Additionally, there are 53.6-ohm isolation resistors on the board for direct coupling. Transformer coupling requires an external transformer and isolation resistor at the junction to the main 1553 bus to match the stub impedance to the bus. (The Air Force mandates that transformer coupling be used).

Since the bus coupling (transformer or direct) is specified by the order code for the board, calling the API routine BusTools_SetVoltage() will have no effect on bus coupling.

See chapter 13, “Interface Signals” for a complete description of the 1553 interface signals.

External Input

See chapter 13, “Interface Signals“ for a complete description of the functions of the discrete input signal.

External Output

See chapter 13, “Interface Signals“ for a complete description of the functions of the discrete output signal.

Setting the MEM16 Decode

Onboard jumpers are assigned to the "usa" bit that forces the hardware to decode the ISA sa[16…14] signals along with the la[23…17] signals as qualifiers for the MEM16 signal. MEM16 is the asynchronous handshake that informs the initiator that it can accept a 16-bit word transfer (PC/AT 16-bit board versus 8-bit XT board). The EISA/ISA specification does not allow sa[] signals to be used to qualify MEM16, as the adapters within a 128K boundary must all be 16-bit or all be 8-bit boards. In reality, many platforms do not follow the specification and we have found that qualifying MEM16 with sa[16…14] works best on the vast majority of ISA platform PCs. However, a very few PCs delay the sa[] signals too long to qualify them for MEM16.

By default, the board uses sa[16…14] to qualify MEM16. Contact Condor Technical Support to disable usage of the MEM16 signal.

IRIG Signaling

The Q104-1553 has an optional IRIG-B capability. IRIG time may be received on the signals IRIG IN and IRIG GND. The following IRIG formats are accepted:

Format	Modulation Frequency	Frequency/ Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

When enabled by the software, IRIG OUT will transmit IRIG B002 data from the onboard IRIG encoder. IRIG OUT signal can source/sink 16 mA at valid TTL levels.

Q104-1553 (ISA) Memory Map

The Q104-1553 resides in ISA memory space in a host system. The board may be mapped into any available 16K-byte block in upper memory between segment addresses A000:0000 and E400:0000 (physical addresses A0000 to E4000 hexadecimal.) The memory address is determined by the jumper settings on header JB1 (listed below). Refer to the image of JB1 for pin 1 orientation.

Note that the most significant address bit is located closest to the silkscreen 'JB1' on the circuit board. This corresponds to JB1 pins 1-2.



Figure 17. Jumper Block JB-1.

Note: Pins 1-2 are at top as viewed above.

The Q104-1553 memory is paged by an internal page register, accessed at a word offset dedicated to each particular channel. (See the "MIL-STD-1553 Universal Core Architecture Reference Manual" for more information).

Table 26. Q104-1553 Memory Address Jumper Options

Selected Physical Address Range	JB1: 1-2	JB1: 3-4	JB1: 5-6	JB1: 7-8	JB1: 9-10
0A0000 - 0A3FFF	ON	OFF	ON	ON	ON
0A4000 - 0A7FFF	ON	OFF	ON	ON	OFF
0A8000 - 0ABFFF	ON	OFF	ON	OFF	ON
0AC000 - 0AFFFF	ON	OFF	ON	OFF	OFF
0B0000 - 0B3FFF	ON	OFF	OFF	ON	ON
0B4000 - 0B7FFF	ON	OFF	OFF	ON	OFF
0B8000 - 0BBFFF	ON	OFF	OFF	OFF	ON
0BC000 - 0BFFFF	ON	OFF	OFF	OFF	OFF
0C0000 - 0C3FFF	OFF	ON	ON	ON	ON
0C4000 - 0C7FFF	OFF	ON	ON	ON	OFF
0C8000 - 0CBFFF	OFF	ON	ON	OFF	ON
0CC000 - 0CFFFF	OFF	ON	ON	OFF	OFF
0D0000 - 0D3FFF	OFF	ON	OFF	ON	ON
0D4000 - 0D7FFF	OFF	ON	OFF	ON	OFF
0D8000 - 0DBFFF	OFF	ON	OFF	OFF	ON
0DC000 - 0DFFFF	OFF	ON	OFF	OFF	OFF
0E0000 - 0E3FFF	OFF	OFF	ON	ON	ON
0E4000 - 0E7FFF	OFF	OFF	ON	ON	OFF

Selecting Memory Addresses

Prior to selecting the memory block that the hardware is mapped into, the available system memory resources must be determined. For upper memory, the C800 and D000 segments (96K bytes) are allocated for adapter boards on the ISA platform. Before installing the board, you must find a 16K-byte block that is free, starting at one of the base addresses listed in the table.

When using any program to determine if a memory or I/O space is available for use remember that most such programs only report what the operating system knows. If no operating system driver has been installed for a memory or I/O region, the program might report that it is available, even if some device is really using that region.

Keep in mind that if multiple boards are being used in the same platform, then sufficient memory space must be available for each board. Two boards (up to eight 1553 channels) require 64K free bytes.

Q104-1553-P [PCI Interface] Memory Map – PCI Stack Locator

The Q104-1553-P resides in PCI memory space in a host system. While PCI devices are inherently Plug-and-Play, the mechanical implementation of the PC/104-*Plus* stack-through connector requires that the board be aware of its physical location in the PC/104-*Plus* stack for signal timing integrity. This is so that the card may observe the correct PCI clock and IDSEL pins in the –*Plus* connector, associated with that stack location. Refer to the PC/104-*Plus* specification for complete details.

In general, the host card is located at the bottom of the PC/104-Plus stack. This is often referred to as Slot 0. The next added card in the stack is designated Slot 1, and the stack grows upwards in this manner. The host adjusts clock traces onboard so that all slots see their PCI clock adjusted for no apparent skew

The most significant address bit is located closest to the silkscreen ‘JB1’ on the circuit board. This corresponds to JB1 pins 1-2.



Figure 18. Jumper Block JB-1

Note: Pins 1-2 are at top as viewed above

Table 27. PCI Stack Locator Jumpers

Slot Location	JB1: 7-8	JB1: 9-10
Slot 1	ON	ON
Slot 2	ON	OFF
Slot 3	OFF	ON
Slot 4	OFF	OFF

Note: An installed shunt indicates an active-low input signal to the clock selection circuitry.

The Q104-1553-P shall be mapped into an available 8MB memory window in PCI memory. Refer to the image of JB1 for pin 1 orientation.

Interrupt Line Select for the Q104-1553 (IRQ3-7, 9-12, 14-15)

The Q104-1553 board features software-programmable interrupt line selection. There are no interrupt jumpers to set. However, you still must choose the interrupt to use, one that isn't being used by another board.

When installing the software for 32-Bit Windows, you are asked to select the hardware interrupt number. Selecting "0" disables the hardware interrupts; the API defaults to polling the board. The Linux installation uses 7 as the default IRQ.

The Q104-1553-P is a PCI plug-n-play board. All channels on a Multi-channel Q104-1553 board share the same hardware interrupt line. The BusTools/1553-API handles sharing the interrupt between the channels.

CHAPTER 11

Standard IP-1553 Based Product Installation

Installation Procedure

This section tells how to install the IP-1553, PC-1553-IP, PCI-1553-IP, VME-1553-IP, cPCI-1553-IP, and VXI-1553-IP boards. The latter five products are packaged systems based upon the IP-1553 and are composed of a carrier board and one or two IP modules. If you have purchased only the IP-1553 module, you must provide your own carrier board and cabling.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

1. For 32-Bit Windows install the software before installing the hardware. For UNIX and VxWorks systems install the hardware first, then the software.

2. Check your system for memory and I/O conflicts and select the desired memory and I/O addresses and hardware interrupt for the board.

   See the “Quick Start” installation guide.

3. Using the supplied software disks, install the software.

   Be sure to follow the instructions in the "Software Installation Manual" for the operating system you intend to use. When the software installation is complete, you must power the computer off.

Hardware Installation

Follow these steps to install the hardware:

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you change the jumpers.
2. Set the jumpers on the IP-1553 module(s) to the desired settings for your MIL-STD-1553 configuration. See Table 29.
3. If you have purchased a packaged system with a carrier, the carrier board provides the interface to your operating system that is documented separately in the carrier board user's manual.
4. If you have purchased an IP-1553 configuration without a carrier board, you must first install the IP on your own carrier board. The connectors are aligned to prevent improper installation. Re-install the carrier board with the IP module in your system.
5. If you purchased an IP-1553 configuration that included the carrier board, a transition cable is provided which adapts from the carrier I/O connector to MIL-STD-1553 jacks.
   - Connect your MIL-STD-1553 bus to the PL-74 connectors provided on the transition cable. The IP I/O connector is defined below.
   - The transition cable should be connected to the ***second*** I/O connector used by the IP-1553. For example if the IP-1553 is being installed into Slots A-B, then the transition cable should be connected to I/O connector B. (The transition cable should never be connected to connector A).

Note: If this is the last connection on the bus, use a "Tee" and connect a 78-ohm terminator to provide the proper termination for the bus. Otherwise, you should use a "Tee" with a cable on each end of the "Tee".

If you are using "transformer" coupling, simply connect the bus "A" and "B" "stubs" to the connectors on transition cable.

IP Connector Description

The IP-1553 is a double size IP Module. It contains four AMP 50-pin plug connectors, part number 173279-3. The connectors are designated IP A Logic (P1), IP A I/O (P2), IP B Logic (P3) and IP B I/O (P4).

Most IP carriers, including all carriers supplied by Condor Engineering, route the I/O connector pins on the IP-1553 to the same-numbered pins on the carrier I/O connectors.

IP logic signals are routed through connector P1. Connector P2 is used only for mechanical support. Connector P3 is used only to supply power and ground connections. Connector P4 provides the I/O (e.g., the MIL-STD-1553 and discrete I/O connections).

Table 28. The Pin Assignments for IP-1553 P4

IP Connector P4, Carrier Connector B, C, or D Pin Number	Signal Name	Signal Type	CONM-D25 25-Pin D-type Connector Pin Number
1, 39	EXTOUT	TTL Output	11
3, 41	EXTIN	TTL Input	12
5,7,9,11,13,17, 19,21,23	GND	Power Return	1,2,3
8	TAGCLK	TTL Spare I/O	
10	INCMD	TTL Spare I/O	
12	RTAD4	TTL Input	
14	RTAD3	TTL Input	
16	RTAD2	TTL Input	
18	RTAD1	TTL Input	
20	RTAD0	TTL Input	14
22	RTADP	TTL Input	15
25	SHIELDA	Shield	4
27	1553A+	Bi-directional 1553	5
29	1553A-	Bi-directional 1553	6
31	SHIELDB	Shield	7
33	1553B+	Bi-directional 1553	8
35	1553B-	Bi-directional 1553	9

Note: For products using the 50-pin header I/O connector, the DB25 connector is wired to the ribbon cable as follows: Pins 19 - 43 (on the ribbon) are connected to pins 1 - 25 (on the DB25).

When you connect the transition output cable to a carrier, ensure that you use the proper I/O connector. Use the following connector for ISA, PCI, cPCI, VME, or VXI Bus carriers supplied by Condor Engineering:

1. If the IP is in the first dual slot (Slots A and B), connect the cable to the IP B I/O connector on the carrier.
2. For ISA-based IP carriers, if the IP is in the second dual slot (Slots B and C), connect to the IP C I/O connector on the carrier.
3. If the IP is in the third dual slot (Slots C and D), connect the cable to the IP D I/O connector on the carrier.
4. For the VME/VXI Bus carrier, take care when using Slots C and D for the IP-1553. The IP D I/O connector is wired to the P2 connector on the VME/VXI backplane. Be sure there is no conflict with other signals that might also connect to the backplane. See the IP carrier manual for more information.

IP-1553 Transition Cable

When ordered with a carrier, the IP-1553 comes with a transition cable. That cable translates from the applicable 50-pin connector to standard 1553 tri-axial cable jacks and Trigger I/O BNC cable jacks. For carriers that use a 50-pin header I/O connection, Figure 19, show the cable wiring.

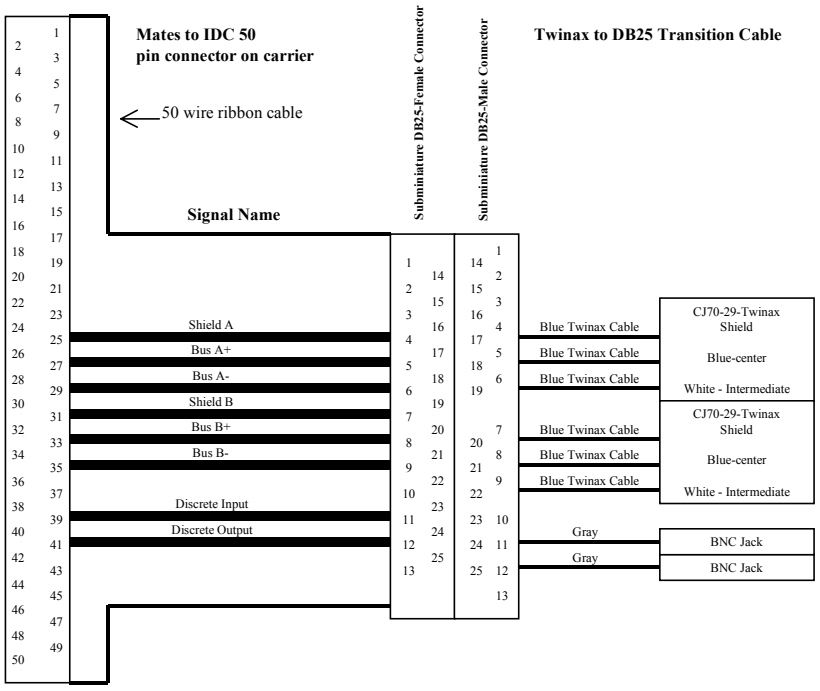


Figure 19. IP-1553 Transition Cable Wiring

For all other carriers, Condor supplies a transition cable that routes 1553 signals to tri-axial cable jacks and External I/O to BNC cable jacks. See chapter 13, “Interface Signals”, for a complete description of the 1553 interface signals.



Figure 20. IP Module Ribbon Connectors for VME and VXI Front Panels

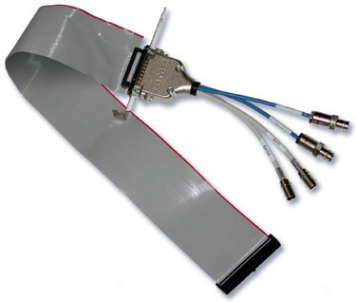


Figure 21. 25-pin D-sub Connector Cable for ISA and PCI IP Carriers

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor’s website..

TAGCLK and INCMD

These are spare TTL-level signals, reserved for future use. They should be left open.

Transformer versus Direct Coupling

MIL-STD-1553B allows for two methods of connecting a terminal to the bus. Transformer coupling provides noise immunity over long distances

and requires external transformer couplers. Direct coupling is often used in the laboratory because it requires no transformers between boxes. To set the IP-1553 board for either coupling method, jumpers must be installed. The board comes with factory-installed jumpers for direct-coupled mode.

Ensure that only the direct coupling or only the transformer-coupling jumpers are set at any given time. Table 29 shows jumper placement.

Table 29. IP-1553 Jumpers for Direct or Transformer Coupling

Function	Jumpers Installed
Direct coupled, channel A	E2-1 to E2-16, E2-4 to E2-13
Transformer coupled, channel A	E2-2 to E2-15, E2-3 to E2-14
Direct coupled, channel B	E2-5 to E2-12, E2-8 to E2-9
Transformer coupled, channel B	E2-6 to E2-11, E2-7 to E2-10

Note: The coupling method is set by these jumpers; the software function BusTools_SetVoltage() *cannot* be used to configure the coupling mode (or the output voltage level, which is fixed by the IP-1553 hardware to MIL-STD-1553B levels).

MIL-STD-1553B Signals

1553A+ and 1553A- are the differential pair for channel A. SHIELDA is used in most environments to shield the cable used for the stub connections. 1553B+ and 1553B- are the differential pair for channel B. SHIELDB is to shield the channel B pair. Both shields are tied together and to the center tap of the isolation transformers on the IP-1553 board.

VME/VXI-AIC-xx02 Jumper Settings

VME/VXI-AIC based configurations come with the IP-1553 installed in Slot C/D only. The IP-1553 memory space and I/O space are both mapped into A32 space with a fixed base address. Contact the factory before modifying the VME/VXI-AIC base address jumpers, as this disables access to the IP-1553. Consult the VME-AIC documentation for a description of the IP-1553 configuration.

IP-1553 Jumper Location

Figure 22 shows the location of jumpers on the IP-1553 board.

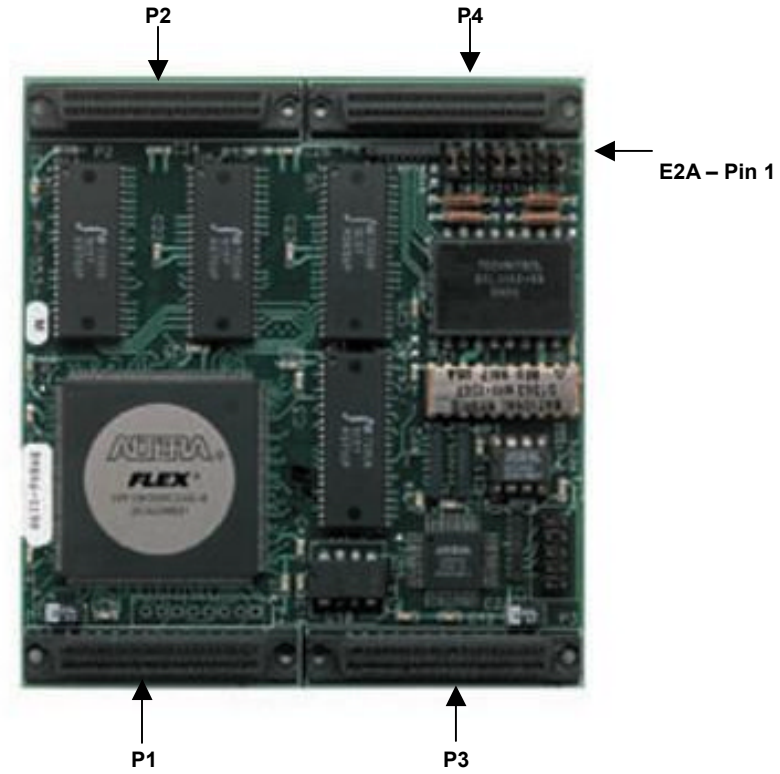


Figure 22. IP-1553 Jumper and Connector Locations

External Input

EXTIN is a TTL signal activated by a low to high transition. The minimum high pulse is 400 ns, but it may stay high indefinitely. EXTIN has one of four functions that are programmed in software: BC trigger, RT trigger, BM trigger and Reset Tag Timer. EXTIN is an input of the Altera 10K50 and is pulled to ground through a 330-ohm resistor on the IP module. See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete input signal.

External Output

EXTOUT is an active high TTL signal that goes active for 50 microseconds. Firing this output is under software control. It may be enabled for BM trigger or RT Synchronize mode code. This signal is an output from the Altera 10K50 and is pulled to ground through a 330-ohm resistor on the IP module. See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete output signal.

External Hardwired RT Address

This feature is currently not implemented but could be if requested. The RTAD[4…0] signals are for externally hardwiring the boards to respond as a single RT. The RTADP is the parity signal. If the RT address is hardwired, the board isn’t able to simulate the Bus Controller or to respond to any other RT address even when so enabled by the software. See chapter 13, “Interface Signals”, for a complete description of the external RT address discrete inputs.

Memory Map Issues

The IP-1553 module uses a 2K-byte IP-bus memory block, two bytes of IP-bus I/O space, and 64-bytes of ID space on the carrier board. The actual addresses depend on the carrier board in use, the slots in use, and the base address of the carrier board in host address space.

IP carrier boards typically map the IP-bus onto the host bus in a manner that is unique for each carrier board. Before setting the memory space jumpers on the carrier board, make sure that the chosen address range is available. PCI carrier boards do not have memory address jumpers since the memory range is assigned by the BIOS during system initialization.

When using any program to determine if a memory or I/O space is available for use, remember that most such programs report only what the operating system knows. If no operating system driver has been installed for a memory or I/O region, the program might report that it is available, even if some device is already using that region.

IP Carrier Jumper Settings

Please consult the manual supplied with your IP carrier board for proper setting of the jumpers, if any, associated with the carrier. These jumpers set the memory addresses and interrupt settings used by the IP-1553 board.

PCI-1553-IP and cPCI-1553-IP Jumper Settings

The PCI-1553-IP (PCI carrier) and cPCI-1553-IP (Compact PCI) carrier jumpers are factory set. Do not change these settings unless directed to do so by Condor Engineering Technical Support. The EEPROM is factory-programmed to support the large memory map mode of the carrier. By default, EEPROM programming is disabled.

The BIOS maps these carriers into memory space at an address above the top of RAM. I/O address space isn't used since the boards map the IP-1553 I/O and ID spaces into host memory space. The supplied software supports the PCI-1553-IP and cPCI-1553-IP with the IP module installed into any available pair of connectors, under 32-Bit Windows.

Although BusTools/1553-API works with either the large- or the small-memory mapping carrier modes, above or below the 1-Mbyte-address boundary, only the large-memory map above 1-Mbyte has been tested. Changing carrier memory map to small requires reprogramming a component on the carrier. Programming that component is beyond the scope of this document.

PC-1553-IP Jumper Settings (ISA Carrier)

Ensure that the base address of the PC-1553-IP carrier is available on your PC and no other boards map that address. The base address and the IP slot pair. The software controlling the board needs this information.

The PC-1553-IP carrier board maps into a 16K-byte region in upper memory. The factory default maps the carrier at address D0000 through D3FFF. The I/O address is not used (since the carrier maps the I/O port into memory space at an address known by the software driver). The software supports the PC-1553-IP with the IP module installed into any available pair of connectors.

The base address of the carrier board is set per Table 30. Installing a jumper sets a zero, while removing a jumper sets an address line as a one.

Table 30. Setting IP-1553 Carrier Base Address

Shunt Location	Address Line	Address Bit Affected
E7-1 to E6-1	A23	80 0000
E7-2 to E6-2	A22	40 0000
E7-3 to E6-3	A21	20 0000
E7-4 to E6-4	A20	10 0000
E7-5 to E6-5	A19	08 0000
E7-6 to E6-6	A18	04 0000
E7-7 to E6-7	A17	02 0000
E7-8 to E6-8	A16	01 0000
E7-9 to E6-9	A15	00 8000
E7-10 to E6-10	A14	00 4000

Be sure to verify this information with the carrier board user's manual.

BusTools/1553-API support hardware interrupts on native PCI and ISA IP carrier. You may either select an unused hardware interrupt for use by the carrier, or select no interrupt.

VME-1553-IP and VXI-1553-IP Jumper Settings

When using the VME-1553-IP or VXI-1553-IP, map the memory address of the carrier into either A32 or A24 space, and the I/O address of the carrier into A16 address space. You can install the IP into slots A/B or slots C/D.

The VMIC VME Manager defaults map the IP-1553 memory space into A32 space (at the carrier default address of 0x60000000) and the I/O space into A16 space (at the carrier default address of 0x6000).

VxWorks-based systems typically map the IP-1553 memory space into A24 space and the I/O space into A16 space, depending on the Board Support Package (BSP). The jumpers on the carrier need to be changed to support this configuration.

See the carrier board user's manual for a description of A16, A24, and A32 address spaces, and information about setting the carrier base addresses.

Be careful when using slots C/D for the IP-1553. Some VME/VXI carriers connect signals from the "D" I/O interface connector to the backplane P2 connector. This can result in the IP-1553 I/O connecting signals to the VME backplane, and bussing them together with signals from other boards. See the carrier hardware reference manual and the backplane hardware reference manual for more information.

Configuring the Software Addressing

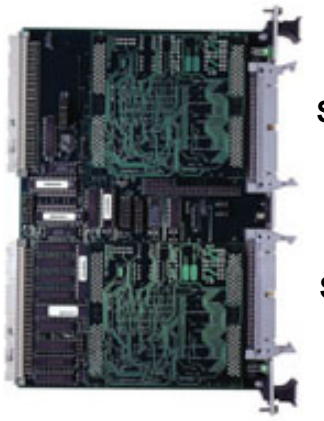




Figure 23. VME-1553-IP **Figure 24. VXI-1553-IP**

See BusTools_API_InitExtended() for more information about configuring software for the various modules and carriers.

CHAPTER 12

IP-D1553 Installation

IP-D1553 Installation Procedure

This section describes installation of the IP-D1553 board. The IP-D1553 is a single-wide, one or two channel IndustryPack board. The IP-D1553 is available in single- or multi-function configurations. The IP-D1553 is compatible with the GreenSpring PCI40, GreenSpring VIPC-616/618, and Acromag AVME9660 carrier boards. See chapter 11, “Standard IP-1553 Based Product Installation”, for details of the carriers. If you are supplying your own carrier boards, that carrier must support IP memory access.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.
2. If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.
3. Inspect the packaging material to insure that the board hasn't been damaged during shipment.

   If it has, contact the shipper right away.

Software Installation

The IP-D1553 installation requirements depend on the carrier board. Refer to the manual for your carrier board for specific installation instructions.

Note: The IP-D1553 requires that the carrier support a minimum addressable IP Memory space of 4MB.

1. For VxWorks and UNIX, install the hardware before the software. For 32-Bit Windows install the software before the hardware.
2. Using the supplied software disks, follow the instructions in the "Quick Start" installation guide.
3. Be sure to follow the instructions applicable to your operating system.
4. If you install on a 32-Bit Windows systems (Windows 95/98/NT/2000/Me/XP), restart you compete after installation.

Hardware Installation

Follow these steps to install the hardware:

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
2. Attach the IP-D1553 to your carrier.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with your carrier board.

Note: If this is the last connection on the bus, use a "Tee" to connect a 78-ohm terminator for proper bus termination. Otherwise, use a "Tee" with a cable on each end. For "transformer", coupling, connect the bus "A" and "B" "stubs" to the connectors on the interface card.

IP-D1553 Board Layout

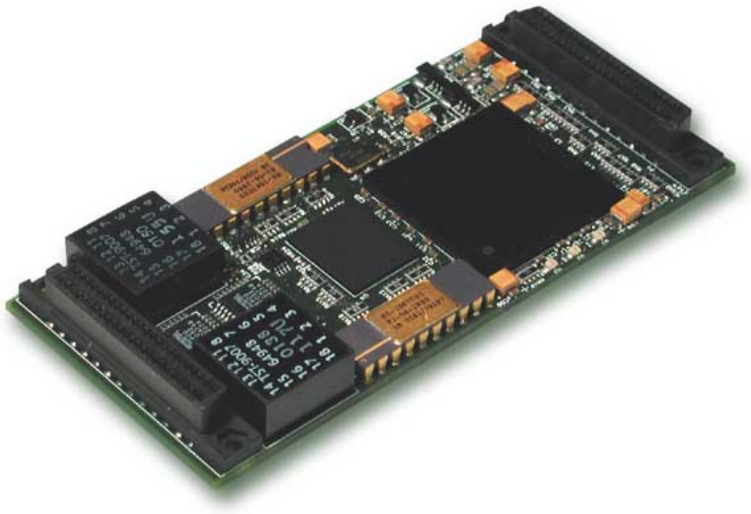


Figure 25. IP-D1553 Board Layout

Status LEDs

There are three status LEDs visible from the board edge of the IP-D1553:

- **D1 - Configuration Status** – Indicates the status of the Local Processing Unit (LPU) FPGA. Before FPGA configuration, the LED is off. After successful FPGA configuration (at power-up), the LED lights.
- **D2 / D3 - 1553 Bus Activity** – Illuminates on detection of traffic on the applicable 1553 bus while running in external mode.

IP-D1553 Connector Description

I/O for the IP-D1553 routes though the I/O connector, as defined by the Industry Pack specification. The carrier then routes the I/O signal to a Field I/O connector.

For the latest details on Condor-supplied cabling, consult the Online Cabling Guide available from Condor's website..

When ordered with a carrier, the IP-D1553 includes a transition cable. That cable translates from the Field I/O 50-pin connector to standard 1553 tri-axial cable jacks and Trigger I/O BNC cable jacks or to common D-type connectors. Cabling is the responsibility of the integrator for carriers that use Backplane I/O. For carriers that use a 50-pin header Field I/O connector, Figure 26 shows the cable wiring provided with a single channel IP-D1553.



Figure 26. IP Module Ribbon Connectors for VME and VXI Front Panels

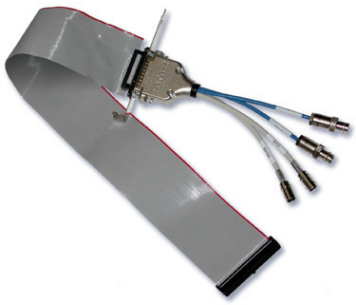


Figure 27. 25-pin D-sub Connector Cable for PCI IP Carriers

IP-D1553 Pin Assignments

The following table specifies the Field I/O connector pin assignments. Any pin not listed in the table is not connected to the IP-D1553 board. Pins with the *[standard]* label are for the standard transformer couple IP-D1553 boards. Pins with the *[optional]* label are available only with the optional direct couple configuration.

Table 31. IP-D1553 Field I/O Pin Assignments

Pin Number	Signal Name
25,31	CH0 1553_SHIELD
27	CH0 A+_XC *[standard]*
28	CH0 A+_DC *[optional]*
29	CH0 A-_XC *[standard]*
30	CH0 A-_DC *[optional]*
32	CH0 B+_DC *[optional]*
33	CH0 B+_XC *[standard]*
34	CH0 B-_DC *[optional]*
35	CH0 B-_XC *[standard]*
37, 46	CH1 1553_SHIELD
42	CH1 A+_XC *[standard]*
43	CH1 A+_DC *[optional]*
44	CH1 A-_XC *[standard]*
45	CH1 A-_DC *[optional]*
47	CH1 B+_DC *[optional]*
48	CH1 B+_XC *[standard]*
49	CH1 B-_DC *[optional]*
50	CH1 B-_XC *[standard]*

Pin Number	Signal Name
41	EXTIN
39	EXTOUT
9	RTA0
11	RTA1
13	RTA2
15	RTA3
17	RTA4
19	RTADP
8, 10, 12, 14, 16, 18.	RTA_grounds
21	IRIG_OUT
20	GND
23	IRIG_IN
22	IRIG_IN_GND
1-7	Reserved
24, 26, 36, 38, 40	Reserved

Signal Descriptions

See chapter 13, “Interface Signals”, for a complete description of the 1553 interface signals.

Transformer versus Direct Coupling

MIL-STD-1553B allows for two methods of connecting a terminal to the bus:

- Transformer coupling provides noise immunity over long distances and requires external transformer couplers.
- Direct coupling is often used in the laboratory because it requires no transformers between boxes.

The Standard Configuration of the IP-D1553 connects Transformer Coupled stubs to the Field I/O connector. Optionally, the IP-D1553 is available with Direct Coupled stubs connected to the I/O connector.

Cables provided by Condor Engineering terminates to the 1553 Interface in the Transformer Coupled configuration.

The IP-D1553 can not use the API function BusTools_SetVoltage() to configure the coupling mode or the output voltage level on the IP-D1553.

MIL-STD-1553B Signals

A+ and A- are the differential pair for bus A. In most environments, SHIELD, shields the cable used for the stub connections. B+ and B- are the differential pair for bus B. SHIELD also shields the bus B pair. The shields for Bus A and Bus B are tied together and to the center tap of the isolation transformers on the IP-D1553 board. However, the shield for Channel 1 is independent of the shield for Channel 2 for isolation purposes. It is the responsibility of the integrator to determine the correct shield wiring for their application.

External Input

One EXTIN signal is provided as a board-wide input for the IP-D1553. EXTIN is a logic signal that is activated by a high to low transition. EXTIN has one of four functions that are programmed in software: BC trigger, RT trigger, BM trigger, and Reset Tag Timer. This input may be assigned to either, or both, 1553 channels on the IP-D1553.

This signal is an input of the Altera FPGA, pulled to a logic Low by a resistor located on the board, and is protected by a 100-ohm series resistor.

See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete input signal.

External Output

EXTOUT is an active high TTL signal that goes active for 50 microseconds. Firing this output is under software control. It may be enabled for BM trigger or RT Synchronize Mode Code. This signal is an output of the Altera FPGA, and is protected by a 100-ohm series resistor. See chapter 13, “Interface Signals”, for a complete description of the functions of the discrete output signal.

RT Address

This optional feature is only available on special orders. The RTAD[4…0] signals externally hardwire the boards to respond as a single RT. The RTADP is the parity signal. If the RT address is hardwired, the board is not able to simulate the Bus Controller or to respond to any other RT address even when so enabled by the software.

See chapter 13, “Interface Signals”, for a complete description of the external RT address discrete inputs.

IRIG Signaling

IRIG time may be received on the signals IRIG IN and IRIG GND. The following IRIG formats are accepted:

Format	Modulation Frequency	Frequency/ Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

When enabled by the software, IRIG OUT transmits IRIG B002 data from the onboard IRIG encoder. IRIG OUT signal can source/sink 16 mA at valid TTL levels

Memory Map Issues

The IP-D1553 requires that the carrier board support accesses to IP IP Memory Space, with a minimum IP Memory window of 4MB. Additionally, ID Space and I/O Space accesses are supported; however, reads to I/O Space do not contain meaningful data. For complete details of a particular carrier board’s implementation, refer to the carrier’s user manual.

CHAPTER 13

Interface Signals

Each of the boards in the BusTools family provides one or more dual-redundant MIL-STD-1553 interface channels and discrete inputs discrete outputs. Certain boards can "hardwire" the RT address of the board. This chapter describes the characteristics of these signals.

MIL-STD-1553 Bus Characteristics

MIL-STD-1553, "Aircraft Internal Time Division Command/Response Multiplex Data Bus", is a military standard, which has become one of the basic tools for the integration of avionics systems. Over the last 25 years, it has become the predominant, internationally accepted network of choice for the integration of military systems. MIL-STD-1553 applications have now expanded beyond military aircraft to include satellites, missiles, tanks, ships, and the International Space Station.

The standard defines the requirements for a one-megabit per second half-duplex dual redundant signaling bus. The signaling voltage levels and required bus interconnections are completely specified.

Defined by the standard are three types of terminals that may be connected to the bus: Bus Controller (BC), Remote Terminals (RTs), and optional Bus Monitors (BMs). Additionally, the standard defines the type and format of each message that is permitted on the bus. This definition includes the exact timing, format, and meaning of the control and status words, and the number and size of data words. The standard doesn't define the contents of the data words or their meaning.

BusTools/1553 boards support all MIL-STD-1553 message formats.

Redundancy Management

The 1553 interface channel is a “hot backup” dual redundant bus channel. All Condor Engineering 1553 products support dual redundant buses. The Bus Controller selects which of the dual redundant buses to transmit the current communications. The RT responds only on that bus. The Bus Controller determines when to switch buses and implements any desired method for redundancy management. All members of the BusTools hardware family provide the ability for the programmer to select, on a message-by-message basis, the bus used for communication. The standard prohibits concurrent operation on both buses, which is considered a failure.

1553 – Physical Bus Definition

A MIL-STD-1553 bus consists of a length of twisted-pair wires, with an over-braided shield. Each end of the bus is terminated with a 78-ohm resistor, which is connected between the two twisted wires. The shield is connected to chassis ground.

Physical Bus Length

The maximum length of a MIL-STD-1553 bus is not specified by the standard and must be determined for each application by analysis. Bus lengths exceeding 300 feet (using transformer coupling) have been successfully implemented. All Condor Engineering BusTools boards, being MIL-STD-1553 compatible, are capable of operation on maximum length 1553 buses.

Connections to the bus use Bus Couplers.

Transformer versus Direct Coupling

MIL-STD-1553B allows two methods of connecting a terminal to the bus.

- Direct coupled (short stub)
- Transformer coupled (long stub)

Transformer coupling provides better noise immunity and isolation over long distances and requires external transformer couplers. Direct coupling is often used in the laboratory because it requires no external transformers (although both methods make use of an internal transformer on the board).

Note: MIL-STD-1553 Cable Stub Requirements (paragraph 4.5.1.5) dictate minimal stub length. Other paragraphs note that direct couple stubs should not exceed one foot, while Transformer Coupling provides allow stub length up to 20 Feet. A mezzanine board, such as the IP-1553, IP-D1553, PCM-1553, or QPMC-1553, which traces length through the host carrier, and cabling solutions typically violate the one-foot guideline. Therefore, direct couple stubs are discouraged.

Transformer Coupling is the standard configuration of the IP-D1553. Condor Engineering cables terminates to the 1553 Interface in this manner. However, Direct Coupling is also available for users that require such terminations to their 1553 implementations.

Supported Bus Coupling Methods

All Condor Engineering 1553 products supply isolation transformers on the board for both direct and transformer coupling. The Air Force mandates the use of transformer coupling. However, sometimes, direct coupling is used in laboratory environments. Direct coupling eliminates the cost of the bus couplers needed for transformer coupling.

Direct Coupling

You can use Direct Coupling when the distance from the isolation transformer inside the device to the data bus does not exceed one foot. There are 53.6-ohm isolation resistors on the board for direct coupling.

Transformer Coupling

Use Transformer Coupling when the distance exceeds one foot but is less than 25 feet. Transformer coupling requires an external transformer and isolation resistor at the junction to the main 1553 bus to match the stub impedance to the bus.

Coupling Selection

Bus coupling (transformer or direct) is controlled by jumpers on the board, or by relays that are selected under software control. See the Hardware Installation sections of this manual for setting the jumpers (on those boards with jumpers). See the API routine BusTools_SetVoltage() for setting the bus coupling via software control.

MIL-STD-1553B Signals

A+ and A- are the differential pair for channel A. SHIELD is used in most environments to shield the cable used for the stub connections. B+ and B- are the differential pair for channel B. SHIELD is also used to shield the channel B pair. Both shields are tied together and to the center tap of the isolation transformers on the board.

Normally, the A+ (or B+) signal is connected to the center pin of the PL-74 connector, while the A- (or B-) signal is connected to the gold barrel. The shield is always connected to the outer shell of the connector.

Dual channel boards contain a second dual-redundant 1553 interface, which is wired in a manner identical to the first.

Output Voltage Level

The output voltage level is fixed at MIL-STD-1553 levels, or on certain model boards, is adjustable using a software function. For those boards that support adjustable output levels, see the API routine BusTools_SetVoltage() for setting the output voltage.

Input Voltage Threshold

All current Condor Engineering 1553 boards have a fixed receiver voltage threshold specified by MIL-STD-1553.

Connections to a MIL-STD-1553 Bus

Figure 28 and Figure 29 describe the connections to a MIL-STD-1553 bus, both direct and transformer coupled. Coupler boxes are available from a variety of sources, including Condor Engineering.

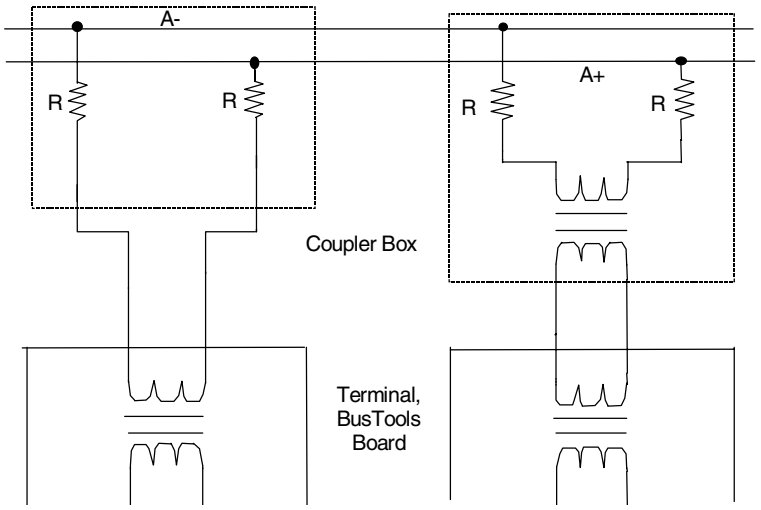
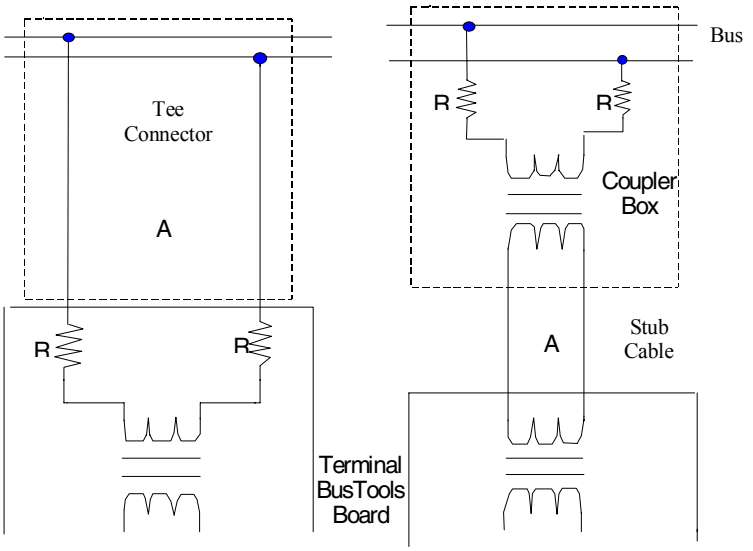


Figure 28. MIL-STD-1553A Data Bus Interface Schematic



a. Direct Coupled (Short Stub) b. Transformer Coupled (Long Stub)

R - Isolation resistor

Figure 29. MIL-STD-1553B Data Bus Interface Schematic

Discrete Signals

All of Condor Engineering's 1553 interface boards have discrete I/O signals. You can refer to the chapters for each board type for a description of their I/O design. The PCI-1553, ISA-1553, IP-1553, cPCI-1553, PMC-1553, QVME/VME/VXI-1553, PCCard-1553, and IP-D1553 have a single pair of discrete I/O (EXTIN and EXTOUT) per channel.

The QPCI-1553, Q104-1553 and Q014-1553P have 10 discrete lines, the QPMC-1553 has 18 discrete lines and the QVME-1553 has 4 discrete lines. These discrete lines are shared between the channels and are programmable, so the user application sets whether they are input or output. In addition, the QPMC-1553, QPCI-1553, and Q104-1553/P have two discrete lines (discrete 7 and discrete 8) are programmable for either input and output triggers that you can use for the same functions as EXTIN and EXTOUT on the other Condor Engineering Boards (see "External Discrete Input" and "External Discrete Output" below). You may also connect an RS-485/422 differential I/O signal to the differential trigger ports on these boards for use as differential triggers. See chapter 11 of the "MIL-STD-1553 Universal Core Architecture Manual" for a description QPCI-1553 and QPMC-1553 discrete operation.

The BusTools/1553-API has several functions for setting, reading and writing the QPCI-1553, Q104-1553, Q014-1553P and QPMC-1553 discrete lines. These functions are:

- BusTools_DiscreteSetIO
- BusTools_DiscreteRead
- BusTools_DiscreteWrite
- BusTools_DiscreteGetIO
- BusTools_DiscreteTriggerOut
- BusTools_DiscreteTriggerIn
- BusTools_DiscreteDiffOut

See the "BusTools/1553-API Software Reference Manual" for a description of these functions.

External Discrete Input

EXTIN is a TTL signal that is activated by a low to high transition. The board determines the minimum high pulse width required for detection. Refer to the applicable hardware reference chapter for specific input duration requirements. EXTIN has one of four functions that are

programmed in software: BC trigger, RT trigger, BM trigger, and Reset Tag Timer.

BC Trigger

After sensing an active input, the hardware sets the bc_run bit, starting the Bus Controller. See the function BusTools_BC_Trigger() to enable this mode. Holding the external input signal active, or pulsing the external input signal has no effect on the board, unless the software clears the bc_run bit. If the board is currently running as a BC, pulsing this signal has no effect. You can synchronize multiple buses to within 40 microseconds using this input.

RT Trigger

RT trigger is essentially the same as the BC, but activates all RTs that are previously set up by the application when bit 13 of 1553_control_register1 is set. To enable this mode, see the BusTools_SetOptions() function.

BM Trigger

After sensing the input to be active, the hardware starts capturing 1553 data, if the software sets the enable_external_trigger bit in the BM trigger header word. To enable this mode, see BusTools_BM_TriggerWrite() function.

Reset Tag Timer

After sensing the input active, the tag timer is reset if bit 6 of 1553_control_register1 is set. A single tag timer is used for the Bus Monitor and all Remote Terminals. To enable this mode, see the BusTools_TimeTagMode() function.

Reset Timetag on Sync Mode Code

This function does not involve the discrete input, but is included because it provides another method for controlling the Timetag Counter. When this mode is enabled, the Timetag counter is cleared to zero when the RT simulation processes a Sync Mode Code. After clearing the Timetag counter, the counter can continues counting, from zero. See the function BusTools_SetOptions() for further information about this mode.

External Discrete Output

EXTOUT is an active high TTL signal that goes active for 50 microseconds. This output is under Software control. It may be enabled for BM trigger or RT Synchronize Mode Code.

BM Trigger Output

The BM trigger output fires when the BM trigger occurs. You must enable the external_output_on_trigger flag stored in the bm_trigger_buffer in RAM. For more information, see the BusTools_BM_TriggerWrite() function.

RT Synchronize Mode Code Output

This signal fires when a simulated RT receives a Synchronize Mode Code, providing you set the fire external trigger (FET) bit of the orphaned_hardware_bits register. For a Broadcast Synchronize Mode Code, the output is active for at least 50 microseconds and up to 250 microseconds. See the function BusTools_SetOptions() for additional information.

External Hardwired RT Address

The QPCI-1553, QPMC-1553, Q104-1553, Q104-1553-P, and QVME-1553 can use Hardwired RT addressing. All other Condor Engineering 1553 interface boards do not support Hardwired RT addressing unless specifically ordered with that feature. To enable hardwired RT addressing on the QPCI-1553, Q104-1553, and Q104-1553P, you install jumper JP1 [QPCI] or JB2 [Q104]. There is also a factory preset for Hardwired RT addressing on special orders. The QPMC-1553 requires that you ground pin 26 (HWRT_EN) on the SCSI 68 pin connector which is pin 15 on the D50 connector. When you enable this feature the board will respond to any message to the Hardwired RT address (if the parity is properly set to be odd) with a “busy’ response until you start the RT function running by calling BusTools_RT_StartStop().

The QPMC-1553 has Hardwired RT addressing on channels 1 and 2, while the QPCI-1553 supports Hardwired RT addressing only on Channel 1. Using this feature requires six discrete I/O lines. The QPMC-1553 has 18 discretes and the QPCI has 10 discretes. When using Hardwired RT addressing, 5 discrete lines form the address while the sixth line is for parity (odd).

During initialization of the QPMC-1553 or QPCI-1553, the API checks the discrete control register (0x110) for the rta1 or rta2 bits to be set. They indicate that the board is using Hardwired RT addressing. rta1 is for channel 1 and rta2 is for channel 2 (QPMC-1553 only). If these bits are set, the API checks bit pe1 (channel 1) or pe2 (channel2) in the discrete control register for parity errors. If there is a parity error, the API initialization returns with an error. Otherwise the API reads and stores encoded RT address.

The user application must read the hardwired RT address using BusTools_RT_GetRTAddr() and initialize the board with that address. You can override the Hardwired RT address by simply initializing with another RT address. Using Hardwired RT addressing does not limit the function of the board. You can still continue to use the Bus Controller and Bus Monitor. You can also program multiple RTs.

APPENDIX A

Glossary of Terms

Term List

This section lists some of the terms that are used throughout this document, and gives a brief explanation of their meaning.

Table 32. Glossary of Terms

Term	Meaning
1553	A component or message in accordance with MIL-STD-1553.
1773	A component in accordance with MIL-STD-1773, which is an optically coupled version of MIL-STD-1553.
3.x	One of several compatible versions of the Windows operating System.
32-Bit Windows®	Windows 95, Windows 98, Windows 98Se, Windows Me, Windows 2000, or Windows XP.
API	Application Programmer's Interface. A defined and documented software interface, which permits software written by one person or organization to interact with the software written by another person or organization without requiring either party to know the details of the implementation of the other's software.
BC	Bus Controller. One of three possible devices that may be connected to a MIL-STD-1553 bus. Determines the message traffic on a 1553 bus.
BC-RT	A 1553 message that transfers data from the BC to a RT. Also called a RT Receive message.
BIOS	Basic Input/Output System. The resident software that initializes the computer hardware, and provides low-level access to some of the computer components.
BM	Bus Monitor. One of three possible devices that may be connected to a MIL-STD-1553 bus. A passive monitor, which cannot create or request traffic on a 1553 bus.
Broadcast	A class of 1553 messages characterized by multiple receivers and one sender. Broadcast messages are directed to the broadcast Remote Terminal number (31), but are actually received and processed by all Remote Terminals on the bus.
Broadcast BC-RT	A specific 1553 message directed to RT address 31, where all RTs receive the data sent by the BC, and that they do not respond with a status word.
Broadcast Mode	A class of 1553 messages, where a mode code is directed to RT address

Term	Meaning
Code	31. This causes all RTs on the bus to process the message, and not respond with a status word.
Broadcast RT-BC	A message type that is not defined or permitted on a MIL-STD-1553 bus system.
Broadcast RT-RT	A specific 1553 message, where two command words are transmitted by the BC, and that the first command word tells all RTs to listen. The second command word instructs a specific RT to ignore the listen command and to transmit data.
BSP	Board Support Package. Software used by VxWorks to setup the hardware on a specific processor board. Roughly equivalent to the BIOS on a PC or PC/AT.
cPCI	Compact version of the PCI interface. See PCI below.
DLL	Dynamic Link Library. A stand-alone library of software functions that may be used by an application. The DLL may be updated or changed without requiring that the application be re-compiled or re-built.
FPGA	Field Programmable Gate Array
IP Carrier	An interface board designed to adapt one or more IP Modules to a different mechanical and electrical bus structure.
IP Module	A modular mezzanine card based on the VITA 4-1995 IP Module Draft Standard 1.0.d.0. The IP-1553 is a doublewide IP Module.
include file	A file with an extension of ".h", used by "C" programmers to contain function and data structure definitions that are shared among various program modules.
Linux	UNIX based operating system for PCs
Microcode	The instructions for the programmable element of the 1553 interface contained in the WCS.
Microsecond	1/1000000 (millionth) of a second. Abbreviated as uS or uSec.
Millisecond	1/1000 (thousandth) of a second. Abbreviated as mS or mSec.
MIL-STD-1553	A military communication standard that specifies the interconnection of one Bus Controller, multiple Remote Terminals, and optionally, one or more Bus Monitors, into an integrated communication system.
MIL-STD-1773	An optically coupled version of MIL-STD-1553.
Mode Code	A class of 1553 messages, using Sub Address 0 or 31, and with the word count interpreted as the mode code number. Mode codes have zero or one data word, depending on the mode code number. While all word counts are potentially valid, only a subset of the possible mode codes are valid, as specified by the standard.
NT	An Microsoft operating system, Windows NT
Operating System	The software that operates the computer, such as Windows 98 or Windows NT.
OS	Operating System. The software that operates the computer.
PC	Personal Computer. A specific type of computer, based on the Intel 80x86 processor line.
PCI	Peripheral Component Interconnect. A board-level communication bus used in Personal Computers (and other computer systems) based on the PCI Specification from the PCI Special Interest Group.
Playback	The ability to regenerate MIL-STD-1553 message traffic on the physical bus using data that was previously recorded.
PMC	PCI Mezzanine Card. A slim modular mezzanine card based on the PCI

Term	Meaning
	specification.
RT	Remote Terminal. One of three possible devices that may be connected to a MIL-STD-1553 bus. Responds to a Bus Controller.
RT Number	The address of a specific RT. A value between 0 and 30, with 31 being reserved for the Broadcast function.
RT Receive	A 1553 message that transfers data from the Bus Controller to a Remote Terminal. Also called a BC-RT message or just a Receive message.
RT Transmit	A 1553 message that transfers data from a Remote Terminal to the Bus Controller. Also called a RT-BC message or just a Transmit message.
RT-BC	A 1553 message that transfers data from a RT to the BC. Also called a RT Transmit message.
RT-RT	A class of 1553 messages, where there are two command words transmitted by the BC. The first command tells a specific RT to listen for data, the second command word instructs another RT to transmit data. The BC is neither the source nor destination for the data.
Sub Address	The address within a RT that acts as the source or destination of a specific message. Sub Addresses 1 through 30 are used for messages, SA 0 and 31 are reserved for mode codes.
WCS	Writeable Control Store
window	A functional component of an application. A display.
Windows	One of several operating systems supplied by Microsoft corporation.
WinTel	The Windows/Intel computing platform, commonly implemented on a PC (Personsal Computer).

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