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Find the *Abaco Systems / Condor Engineering QPCI-1553-2M-W* at our website: *Click HERE*

CHAPTER 5

QPCI-1553 and QPCX-1553 Installation

QPCI-1553 and QPCX Installation Procedure

This section explains how to install the QPCI-1553 and QPCX-1553 boards. The QPCI-1553 / QPCX-1553 is a single, dual, or quad channel 1553 interface board supporting universal PCI signaling. The main difference between the two is that the newer QPCX supports the 66MHz PCI bus. With API version 5.64 and newer, the two boards are drop in replaceable. Prior to API version 5.64, the QPCX will work but will not support hardware interrupts. Note that there are differences in the 1553 shields between the two boards as described in this chapter.

Pre-installation Procedure

Before you begin:

1. If possible, use a static free workstation.

   If such a workstation is not available, touch a ground such as the metal part of your computer (to discharge any static electricity) before handling the board.

2. Inspect the packaging material to insure that the board hasn't been damaged during shipment. If it has, contact the shipper immediately.

Software Installation

The QPCI-1553 / QPCX-1553 board is a Plug-and-Play board. There are no switches or jumpers on the board required for software installation.

1. For 32-Bit Windows install the software before installing the hardware.

   For UNIX and VxWorks systems install the hardware first, then the software.

2. Using the supplied software disks. Be sure to follow the instructions applicable to your operating system.

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Note: When you install on a 32-Bit Windows systems (Windows 95/98/NT/2000/Me/XP), you must restart your computer after installation.

Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when you open the chassis.
2. Remove the cover from your PC. Remove the mounting plate from one of the unused PCI slots in your computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with your board.

   The QPCI-1553 / QPCX-1553 I/O configuration is defined below. A transition cable is provided from the QPCI-1553 / QPCX-1553 I/O connector to MIL-STD-1553 cable jacks and a D50 connector for other I/O signals.

Note: If you are using “transformer” coupling, than connect the bus “A” and “B” “stubs” from the transformers to the connectors on the transition cable assembly.

If this is the last connection on the bus, use a “Tee” to connect a 78-ohm terminator to provide proper termination for the bus. Otherwise, use a “Tee” with a cable on each end. For “transformer”, coupling, connect bus “A” and “B” “stubs” to the connectors on the interface card.

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QPCI-1553 Board Layout

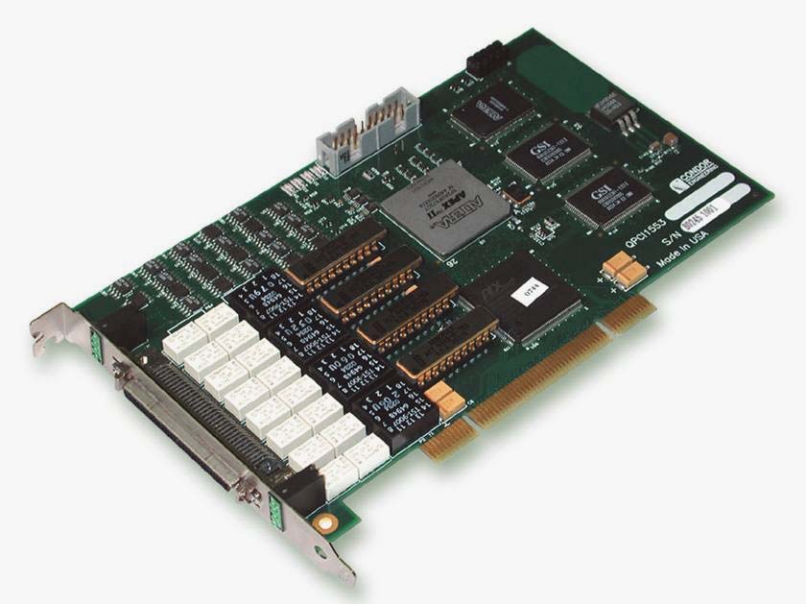


Figure 4. QPCI-1553

QPCX-1553 Board Layout

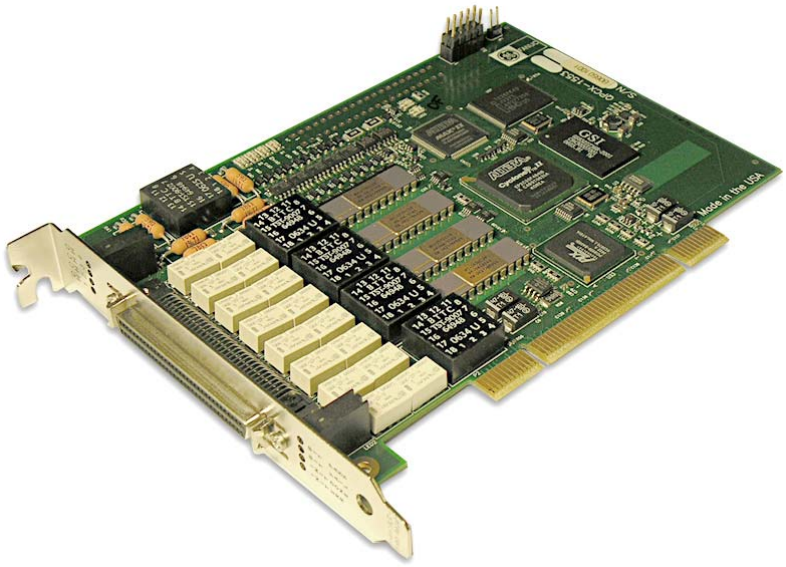


Figure 5. QPCX-1553

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Status LEDs

There are eight LED's on the mounting plate of the QPCI-1553 / QPCX-1553:

- **CH 1, CH 2, CH 3, CH 4 – 1553 Bus Activity -** The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic.
- **INIT DONE, INIT ERR – Configuration Status** – INIT DONE illuminates green on successful FPGA configuration; INIT ERR illuminates green on failed FPGA configuration. The QPCI-1553 / QPCX-1553 configures from an onboard configuration device, so the INIT DONE LED should be illuminated under normal conditions.
- **BIT PASS, BIT FAIL** – **Built-in-test Status –** BIT PASS illuminates green on successful Built In Test; BIT FAIL illuminates red on failed BIT. Both LEDs are off before the first BIT attempt.

There are four bi-colored status LEDs on the top (component side) of the QPCI-1553 / QPCX-1553:

- **B0, B1, B2, B3 LED's – 1553 Bus Activity** – Labeled D1 – D4 respectively on the PCB, the status LED for each 1553 channel illuminates green when receiving 1553 bus traffic and illuminates red if that channel runs internally (transceiver transmit is inhibited).

There are two additional bi-colored status LEDs on the top (component side) of the QPCX-1553:

- **LED3 – CPLD Configuration** –Green indicates CPLD configuration loaded whereas red indicates a load failure.
- **LED4 – Power Good** –Green indicates onboard 1.2V & 2.5V supplies are within tolerance and red indicates there is an out of tolerance condition.

QPCI-1553 / QPCX-1553 Connector Description

The QPCI-1553 / QPCX-1553 use a single 68-pin SCSI connector (P1) on the mounting plate for all I/O. Separate Transition Cable assemblies are provided with one-channel, two-channel, and four-channel boards.

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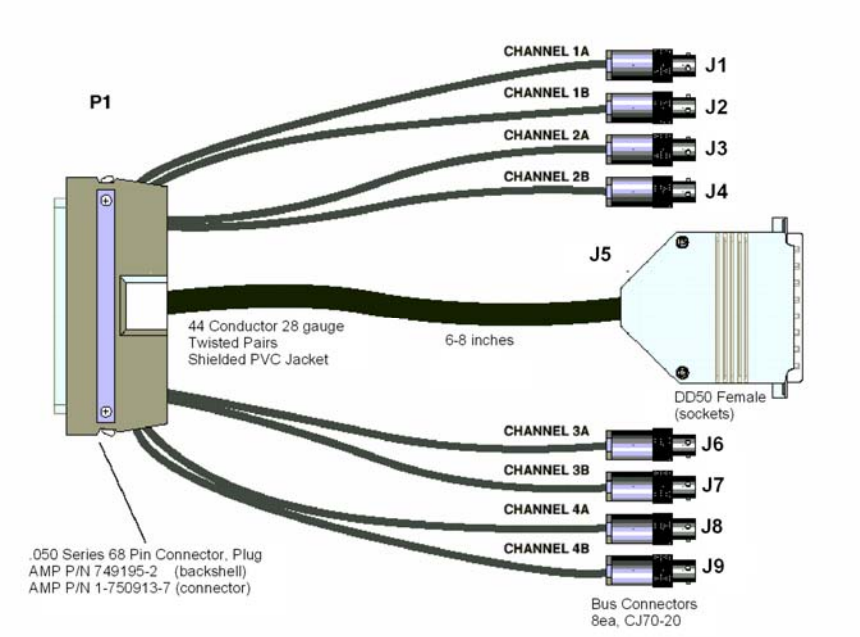


Figure 6. Transition Cable for 4 channel QPCI-1553 / QPCX-1553

QPCI-1553 / QPCX-1553 Mounting Plate Pinout

The mounting plate connector pinout is specified in the following table.

Table 4. QPCI-1553 / QPCX-1553 Front Panel Pin Assignments

Front Bezel Connector (J1)			
Pin	**Function**	**Pin**	**Function**
1	1553 CH1A+	35	ADISC7
2	1553 CH 1A-	36	ADISC8
3	1553 CH 1A Shield*	37	ADISC9
4	GND	38	ADISC10
5	1553 CH 1B+	39	485/422 CH1+
6	1553 CH 1B-	40	485/422 CH1-
7	1553 CH 1B Shield*	41	GND
8	RTADDR1_0/ADISC1	42	EXT CLK+/Trigger+
9	RTADDR1_1/ADISC2	43	EXT CLK-/Trigger-
10	1553 CH 2A+	44	GND
11	1553 CH 2A-	45	GND
12	1553 CH 2A Shield*	46	GND
13	GND	47	LRUA Shield**
14	1553 CH 2B+	48	LRUA+
15	1553 CH 2B-	49	LRUA -
16	1553 CH 2B Shield*	50	GND

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Front Bezel Connector (J1)			
Pin	**Function**	**Pin**	**Function**
17	RTADDR1_2/ADISC3	51	IRIGB IN
18	RTADDR1_3/ ADISC4	52	IRIGB OUT
19	1553 CH 3A+	53	IRIGB IN Return
20	1553 CH 3A-	54	GND
21	1553 CH 3A Shield*	55	-
22	GND	56	-
23	1553 CH 3B+	57	-
24	1553 CH 3B-	58	GND
25	1553 CH 3B Shield*	59	LRUB+
26	-	60	LRUB -
27	GND	61	LRUB Shield**
28	1553 CH 4A+	62	-
29	1553 CH 4A-	63	GND
30	1553 CH 4A Shield*	64	RTADDR1_4/ADISC5
31	GND	65	RTADDR1_P/ ADISC6
32	1553 CH 4B+	66	-
33	1553 CH 4B-	67	-
34	1553 CH 4B Shield*	68	GND

Notes:

* For the QPCI, the individual 1553 Shields are tied to their respective transformer secondary center taps. For the QPCX, the transformer secondary center taps are not connected. However, to provide backward compatibility to the QPCI, the QPCX can be ordered with these signals tied to their respective transformer secondary center taps.

** For the QPCI, the LRUx Shield signals are tied to their respective transformer secondary center taps. On the QPCX, these signals do not exist and are open.

QPCI-1553 / QPCX-1553 Transition Cable

The pin-outs for the QPCI-1553 / QPCX-1553 transition cable are provided in the following tables.

For the latest details on GE Fanuc Intelligent Platforms-supplied cabling, consult the Online Cabling Guide available from GE Fanuc Intelligent Platforms' website.

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Table 5. QPCI-1553 / QPCX-1553 Transition Cable, D50 Pin Assignments

Transition Cable J5 (J3)* Pinout			
1	RTADD1_0/ADSIC 1	26	GND
2	RTADD1_1/ADSIC 2	27	-
3	GND	28	GND
4	RTADD1_2/ADSIC 3	29	LRUA Shield**
5	RTADD1_3/ADSIC 4	30	-
6	GND	31	-
7	RTADD1_4/ADSIC 5	32	-
8	RTADD1_P/ADSIC 6	33	-
9	ADSIC 7	34	485/422 CH1+
10	ADSIC 8	35	485/422 CH1-
11	ADSIC 9	36	485 Shield
12	GND	37	LRUA+
13	EXT CLK+/Trigger+	38	LRUA -
14	EXT CLK-/Trigger-	39	GND
15	-	40	LRUB+
16	GND	41	LRUB -
17	-	42	LRUB Shield**
18	ADSIC 10	43	-
19	GND	44	-
20	GND	45	GND
21	GND	46	IRIGB IN
22	-	47	IRIGB OUT
23	-	48	IRIGB IN Return
24	-	49	-
25	GND	50	GND

Note: For one-channel cable assemblies, this connector is J3; for two and four channel assemblies this connector is J5.

** For the QPCI, the LRUx Shield signals are tied to their respective transformer secondary center taps. On the QPCX, these signals do not exist and are open

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Table 6. One-channel QPCI-1553 / QPCX-1553 Transition Cable, 1553 Connectors

Transition Cable 1553 Connectors	
Connector	***Signal***
J1	*Channel 1, Bus A*
J2	*Channel 1, Bus B*

Table 7. Two-channel QPCI-1553 / QPCX-1553 Transition Cable, 1553 Connectors

Transition Cable 1553 Connectors	
Connector	***Signal***
J1	*Channel 1, Bus A*
J2	*Channel 1, Bus B*
J3	*Channel 2, Bus A*
J4	*Channel 2, Bus B*

Table 8. Four-channel QPCI-1553 / QPCX-1553 Transition Cable 1553 Connectors

Transition Cable 1553 Connectors	
Connector	***Signal***
J1	*Channel 1, Bus A*
J2	*Channel 1, Bus B*
J3	*Channel 2, Bus A*
J4	*Channel 2, Bus B*
J6	*Channel 3, Bus A*
J7	*Channel 3, Bus B*
J8	*Channel 4, Bus A*
J9	*Channel 4, Bus B*

Signal Descriptions

See chapter 18, “Interface Signals”, for a complete description of the 1553 interface signals.

MIL-STD-1553B Signals

1553 CH*n*A+ and 1553 CH*n*A- are the differential pair for bus A. 1553 CH*n* B+ and 1553 CH*n* B- are the differential pair for bus B.

1553 CH *n*A/B SHIELD is tied to the center tap of the isolation transformer of the respective bus on the QPCI-1553 board. These signals are not connected on the QPCX-1553 unless by special order.

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LRU Port Connection

The QPCI-1553 / QPCX-1553 provides a transformer-coupled stub connection where you can attach a Line Replaceable Unit device under test. You can attach one or more channels on the QPCI-1553 / QPCX-1553 card to the onboard Test Bus and communicate with the external LRU device over this port. In this mode, an external LRU TX-coupled device is attached to this connection without requiring external coupling transformers or terminators, as those are provided by the card's Test Bus.

LRUA+ and LRUA- are the differential pair for bus A. LRUB+ and LRUB- are the differential pair for bus B.

LRUA/B SHIELD tie to the center taps of the isolation transformers for the LRU Port on the QPCI-1553 board. These signals are not connected on the QPCX-1553 board.

IRIG Signaling

IRIG time may be received on the signals IRIG IN and IRIG IN Return. The following IRIG formats are accepted:

Table 9. IRIG Formats

Format	Modulation Frequency	Frequency/ Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

When enabled by the software, IRIG OUT transmits IRIG B002 data from the onboard IRIG encoder. The IRIG OUT signal can source/sink 16 mA at valid TTL levels.

Avionics Discrete I/O

The QPCI-1553 / QPCX-1553 has ten discrete I/O signals available on the interface connector. See chapter 18, "Interface Signals", for a complete description of the functions of the discrete signals.

Six of these discrete I/O signals are optionally shared with the first channel's Hardwire RT functionality. See chapter 18, "Interface Signals".

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Hardwired RT Address

The QPCI-1553 / QPCX-1553 provide Hardwired RT Addressing on the first channel. This operational mode is enabled by installing a shunt across JP1. When enabled, the board responds to any message to the Hardwired RT address (if the parity is properly set to be odd) with a "busy' response until you start the RT function running by calling BusTools_RT_StartStop().

Hardwired RT Addressing input polarity is Active High. Onboard pull-ups assure that floating inputs are read as logic one, and grounded inputs are read as logic zero. Parity evaluation is odd; that is, the total of inputs that read logic one [parity inclusive] must be an odd number or the card does not respond to any bus traffic.

Differential Triggers

The QPCI-1553 / QPCX-1553 has one differential trigger input and one differential trigger output available on the interface connector. See chapter 18, "Interface Signals", for a complete description of the functions of the differential trigger signal.

Memory Map Issues

The QPCI-1553 / QPCX-1553 maps into an 8MB address block (BAR2). The BIOS maps the QPCI-1553 / QPCX-1553 board into memory space at an address above the total amount of RAM in the computer. The QPCI-1553 uses a 128-byte PCI configuration space for the PLX (BAR0) whereas the QPCX-1553 uses 512-bytes. The QPCI also allocates a 128 byte PLX I/O space which is required but not actually used (BAR1) whereas the QPCX allocates 256-bytes. Direct access to these registers is not available through the API.

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