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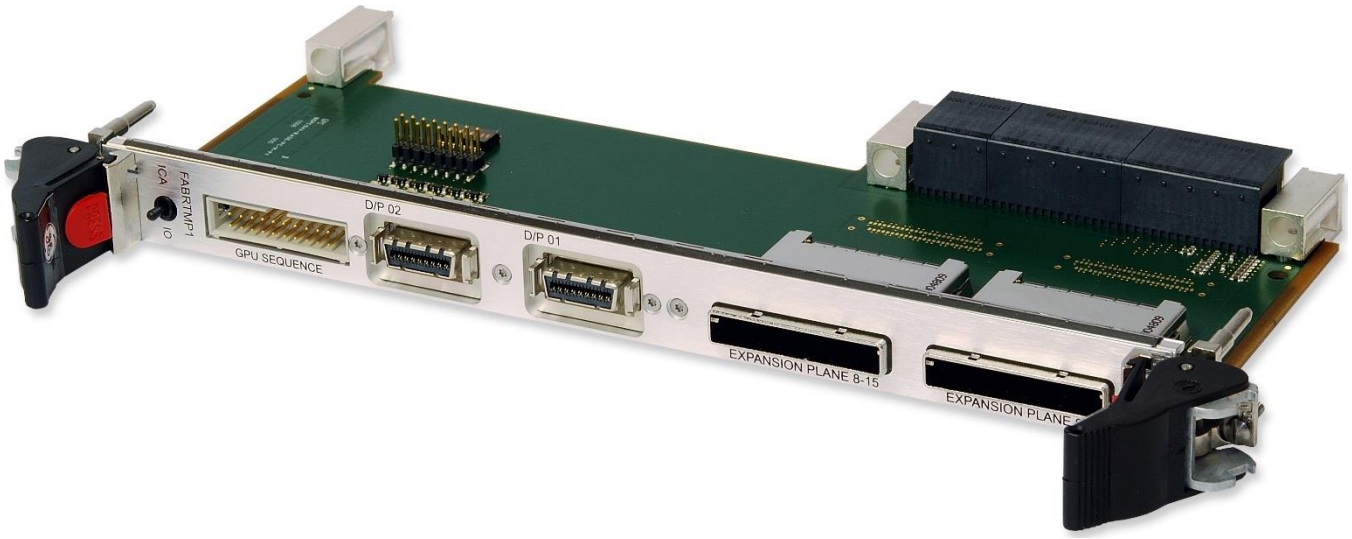
Find the *Abaco Systems FABRTMP1-11* at our website: *Click HERE*

Hardware Reference Manual

FABRTMP1 Fabric RTM

Edition 2DG

Publication No. FABRTMP1-HRM/2DG



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Document History

Revision	Date	Description
1	June 2010	Board Artwork Rev 1
1 + errata	October 2011	Corrections to Sections 1.5 and 1.6
2	September 2011	Board artwork Rev 2 plus addition of backplane and PCIe connector pinouts
2DG	November 2016	Rebranding only, no technical content change

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WARNING

Warnings alert you to the risk of severe personal injury.



CAUTION

Cautions alert you to system danger or loss of data.



NOTE

Notes call attention to important features or instructions.



TIP

Tips give guidance on procedures that may be tackled in a number of ways.



LINK

Links take you to other documents or websites. The purple link color may also be used within a body of text or paragraph to indicate a link (or hyperlink) to a different part of the same document.

Numbers

All numbers are expressed in decimal.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

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LINKS

IPN250 Hardware Reference Manual, publication number IPN250-HRM

IPN250RTM Hardware Reference Manual, publication number IPN250RTM-HRM/2DG

SCVPX6U Hardware Reference Manual, publication number SCVPX6U-HRM

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH

NOTES

Cross-document links are intended for use where the document files are saved under their original file names in the same directory on a server, PC hard drive, or similar. If accessing this document via the Abaco website, cross-doc links will not work.

If you are accessing this document in hard copy or downloaded form, check the Abaco website to ensure that you have the latest version.

Third-party Documents

ANSI/VITA 65-2010 (R2012) - OpenVPX System Specification

ANSI/VITA 46.0-2007 (R2013) - VPX Baseline Standard

Third-party Websites

LINK

http://www.vita.com

NOTE

Technical literature describing components used on the FABRTMP1 products is available from the manufacturers' websites.

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1 • FABRTMP1

1.1 Functional Description

The FABRTMP1 is a Fabric Rear Transition Module (RTM) for use with the Abaco Systems OVPX64UBP backplane. While the FABRTMP1 is primarily intended for use with the NPN240 Graphics Processor and IPN250 Single Board Computer, it is actually a general-purpose RTM. Any features specific to the NPN240 and IPN250 do not make the FABRTMP1 unusable for other payload boards.

The FABRTMP1 provides access to the payload board's fabric connectivity via connector styles commonly used throughout the industry.

The OVPX64UBP backplane functionality is described in the SCVPX6U development chassis manual.



LINK

SCVPX6U Hardware Reference Manual, publication number SCVPX6U-HRM

1.2 Fitting RTMs

See the VPX I/O Modules manual for fitting instructions.



LINK

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH

1.3 Current Requirements

The FABRTMP1 draws a maximum of 76.5 mA from the VPX +3.3 V Auxiliary supply. The other VPX voltage rails (Vs1, Vs2 and Vs3) are brought to the FABRTMP1 but are not used by it.

1.4 VPX Keying

In the default build state, all three guide modules on the FABRTMP1 are unkeyed. Contact Abaco to discuss alternative requirements.

1.5 Product Code

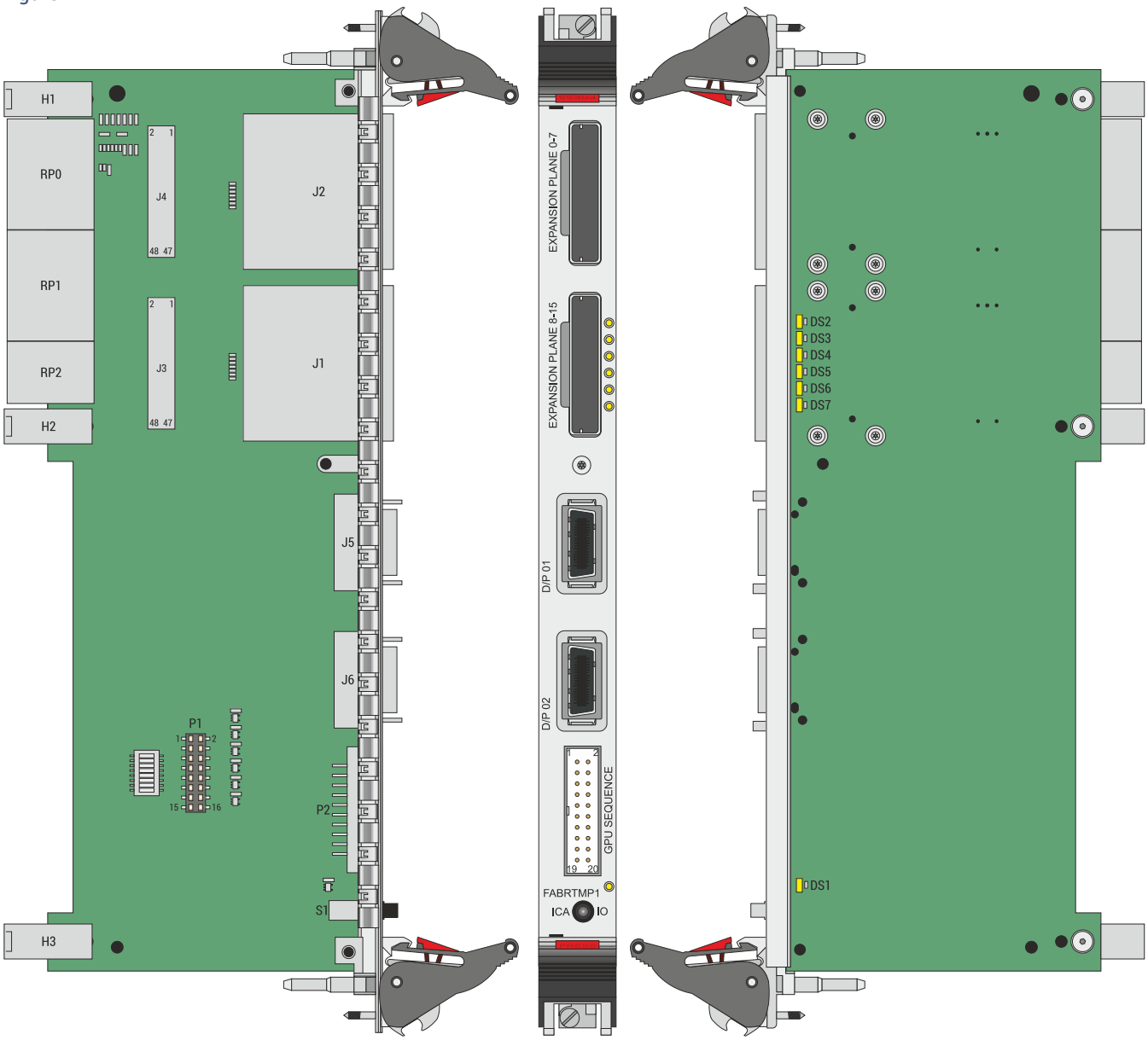
FABRTMP1-11 (P1/P2 Fabric RTM, Level 1 Build option, 0.8" pitch).

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1.6 Layout

Figure 1-1 shows the front and top views of the FABRTMP1 to illustrate the position of the various switches, connectors, headers and LEDs described in this document. The FABRTMP1 has a 0.8-inch pitch front panel.

Figure 1-1 FABRTMP1



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1.7 Open VPX Slot Profile

The FABRTMP1 supports the SLT6-PAY-4F1Q2UT2T-10.2.1 OpenVPX Payload Slot Profile with the following fabric connectivity:

- RP0/RJ0 is used by the Utility plane
- RP1/RJ1 is partly used by the Data plane. Some single-ended signals are used by the Utility plane. Others are user-defined
    - Data plane of 4 fat pipes
- RP2/RJ2 is partly used by the Expansion plane. Single-ended signals are user-defined
    - Expansion plane of 1 quad fat pipe (consisting of 32 differential pairs)

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2 • Connectors

2.1 VPX Backplane Connectors (RP0 to RP2)

See the VPX I/O Modules manual for more details on signal routing.



LINK

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH

2.1.1 RP0

Table 2-1 RP0 Pin Assignments

Pin	A	B	C	D	E	F	G
15	VS2	VS2	VS2	N/C	VS1	VS1	VS1
14	VS3	VS3	VS3	N/C	VS3	VS3	VS3
13	N/C	N/C	GND	N/C	GND	N/C	N/C
12	N/C	N/C	GND	P3V3_AUX	GND	GA4~	GAP~
11	GA0~	GA1~	GND	N/C	GND	GA2~	GA3~
10	N/C	N/C	GND	N/C	N/C	GND	N/C
9	GND	N/C	N/C	GND	N/C	N/C	GND
8	DP01_R0P	DP01_R0N	GND	DP01_T0P	DP01_T0N	GND	N/C
7	GND	DP01_R1P	DP01_R1N	GND	DP01_T1P	DP01_T1N	GND
6	DP01_R2P	DP01_R2N	GND	DP01_T2P	DP01_T2N	GND	VBAT
5	GND	DP01_R3P	DP01_R3N	GND	DP01_T3P	DP01_T3N	GND
4	DP02_R0P	DP02_R0N	GND	DP02_T0P	DP02_T0N	GND	SYSCON~
3	GND	DP02_R1P	DP02_R1N	GND	DP02_T1P	DP02_T1N	GND
2	DP02_R2P	DP02_R2N	GND	DP02_T2P	DP02_T2N	GND	N/C
1	GND	DP02_R3P	DP02_R3N	GND	DP02_T3P	DP02_T3N	GND

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2.1.2 RP1

Table 2-2 RP1 Pin Assignments

Pin	A	B	C	D	E	F	G
16	N/C	N/C	GND	N/C	N/C	GND	BP_PWR~
15	GND	N/C	N/C	GND	N/C	N/C	GND
14	N/C	N/C	GND	N/C	N/C	GND	GPU1_NODE_RESET~
13	GND	N/C	N/C	GND	N/C	N/C	GND
12	N/C	N/C	GND	N/C	N/C	GND	GPU1_SEQ_IN
11	GND	N/C	N/C	GND	N/C	N/C	GND
10	N/C	N/C	GND	N/C	N/C	GND	MASKABLERESET~
9	GND	N/C	N/C	GND	N/C	N/C	GND
8	EP00_RP	EP00_RN	GND	EP00_TP	EP00_TN	GND	GPU1_SEQ_OUT
7	GND	EP01_RP	EP01_RN	GND	EP01_TP	EP01_TN	GND
6	EP02_RP	EP02_RN	GND	EP02_TP	EP02_TN	GND	GPU1_POWR_SDA
5	GND	EP03_RP	EP03_RN	GND	EP03_TP	EP03_TN	GND
4	EP04_RP	EP04_RN	GND	N/C	N/C	GND	BP_PWR~
3	GND	EP05_RP	N/C	GND	N/C	N/C	GND
2	EP06_RP	EP06_RN	GND	N/C	N/C	GND	GPU1_NODE_RESET~
1	GND	EP07_RP	N/C	GND	N/C	N/C	GND

2.1.3 RP2

Table 2-3 RP2 Pin Assignments

Pin	A	B	C	D	E	F	G
8	EP08_RP	EP08_RN	GND	EP08_TP	EP08_TN	GND	GPU2_SEQ_IN
7	GND	EP09_RP	EP09_RN	GND	EP09_TP	EP09_TN	GND
6	EP10_RP	EP10_RN	GND	EP10_TP	EP10_TN	GND	GPU2_SEQ_OUT
5	GND	EP11_RP	EP11_RN	GND	EP11_TP	EP11_TN	GND
4	EP12_RP	EP12_RN	GND	EP12_TP	EP12_TN	GND	GPU2_POWR_SDA
3	GND	EP13_RP	EP13_RN	GND	E13P_TP	EP13_TN	GND
2	EP14_RP	EP14_RN	GND	EP14_TP	EP14_TN	GND	GPU2_POWR_SCL
1	GND	EP15_RP	EP15_RN	GND	E15P_TP	EP15_TN	GND

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2.1.4 Signal Descriptions

Table 2-4 Signal Descriptions

Mnemonic	Description
N/C	No connection
VS1, VS2	+12V backplane supply
VS3	+5V backplane supply
P3V3_AUX	+3.3V auxiliary backplane supply
VBAT	Battery backup supply connection
BP_PWR~	An external Power button may be connected between BP_PWR~ and GND
GND	The DC voltage reference for the system
GA[4:0]~, GAP~	Geographical Addressing and parity bits. The sum of all GA bits, including the parity bit, should be odd
SYSCON~	VPX System Controller status
MASKABLERESET	VPX Maskable Reset signal
DP0x_R[4:1]P/N	Data Plane fat pipe port x (x = 1 & 2) receive differential pairs
DP0x_T[4:1]P/N	Data Plane fat pipe port x (x = 1 & 2) transmit differential pairs
EPxx_RP/N	Expansion Plane quad fat pipe expansion port xx (xx = 00 to 15) receive differential pairs
EPxx_TP/N	Expansion Plane quad fat pipe expansion port xx (xx = 00 to 15) transmit differential pairs
GPUx_NODE_RESET~, GPUx_SEQ_IN, GPUx_SEQ_OUT, GPUx_POWR_SDA, GPUx_POWR_SCL	Power sequencing signals for GPUx (x = 1 or 2). Availability depends on the payload card

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2.2 PCI Express Interface Connectors (J1 to J4)

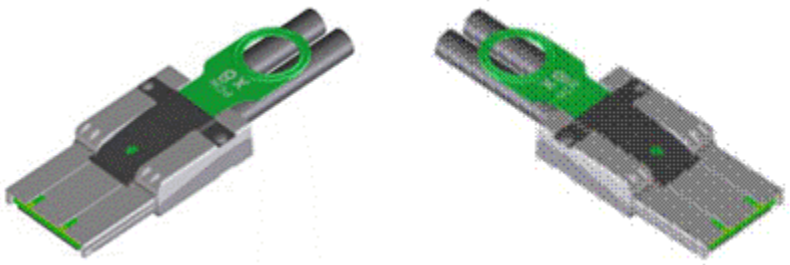
The FABRTMP1 offers 32 differential pairs of PCIe for Fabric connection. These are connected as two ports of the 8-lane PCIe, which may be combined to form a single 16-lane PCIe port. These 32 differential pairs are defined as Expansion ports in slot profile SLT6-PAY-4F1Q2UT2T-10.2.1. If only a single Expansion Plane Port is required, Expansion Plane 0 (EP00) must be used (to comply with the OpenVPX specification).

J1 and J2 provide the 8-lane PCIe interfaces via PCI Express Cabling Standard PCIe cable connectors (Molex 75586-0007 type) with the pinouts shown in Table 2-5. J2 provides lanes 0 to 7, and J1 provides lanes 8 to 15. The power and management signals required for full PCI Express cable specification support are unused and are pulled up to P3V3_AUX to maximize the noise immunity of the cable. For similar reasons, the clock signals are looped back via 100Ω resistors.

J3 and J4 (when fitted) provide mid-bus probe interfaces via 2x25-way headers with the pinouts shown in Table 2-6. These are only suitable for 'Agilent' N4241-A-matching PCIe probes.

Abaco offers cable C-ASY000286-813, which is a PCIe cable (0.5 m in length) with Molex 74546-0813 connectors, as shown in Figure 2-1.

Figure 2-1 PCIe Cable



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Table 2-5 J1 and J2 Pin Assignments

J2 Header				J1 Header			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	GND	A1	GND	B1	GND	A1	GND
B2	EP00_RP	A2	EP00_TP	B2	EP08_RP	A2	EP08_TP
B3	EP00_RN	A3	EP00_TN	B3	EP08_RN	A3	EP08_TN
B4	GND	A4	GND	B4	GND	A4	GND
B5	EP01_RP	A5	EP01_TP	B5	EP09_RP	A5	EP09_TP
B6	EP01_RN	A6	EP01_TN	B6	EP09_RN	A6	EP09_TN
B7	GND	A7	GND	B7	GND	A7	GND
B8	EP02_RP	A8	EP02_TP	B8	EP10_RP	A8	EP10_TP
B9	EP02_RN	A9	EP02_TN	B9	EP10_RN	A9	EP10_TN
B10	GND	A10	GND	B10	GND	A10	GND
B11	EP03_RP	A11	EP03_TP	B11	EP11_RP	A11	EP11_TP
B12	EP03_RN	A12	EP03_TN	B12	EP11_RN	A12	EP11_TN
B13	GND	A13	GND	B13	GND	A13	GND
B14	Pulled up to P3V3_AUX	A14	Looped back via 100Ω	B14	Pulled up to P3V3_AUX	A14	Looped back via 100Ω
B15		A15		B15		A15	
B16		A16	GND	B16		A16	GND
B17	GND	A17	N/C	B17	GND	A17	N/C
B18	GND	A18	N/C	B18	GND	A18	N/C
B19	GND	A19[1]	P3V3_AUX via 10kΩ pull-up	B19	GND	A19[1]	P3V3_AUX via 10kΩ pull-up
B20	P3V3_AUX via 10kΩ pull-up	A20		B20	P3V3_AUX via 10kΩ pull-up	A20	
B21		A21		B21		A21	
B22	GND	A22	GND	B22	GND	A22	GND
B23	EP04_RP	A23	EP04_TP	B23	EP12_RP	A23	EP12_TP
B24	EP04_RN	A24	EP04_TN	B24	EP12_RN	A24	EP12_TN
B25	GND	A25	GND	B25	GND	A25	GND
B26	EP05_RP	A26	EP05_TP	B26	EP13_RP	A26	EP13_TP
B27	EP05_RN	A27	EP05_TN	B27	EP13_RN	A27	EP13_TN
B28	GND	A28	GND	B28	GND	A28	GND
B29	EP06_RP	A29	EP06_TP	B29	EP14_RP	A29	EP14_TP
B30	EP06_RN	A30	EP06_TN	B30	EP14_RN	A30	EP14_TN
B31	GND	A31	GND	B31	GND	A31	GND
B32	EP07_RP	A32	EP07_TP	B32	EP15_RP	A32	EP15_TP
B33	EP07_RN	A33	EP07_TN	B33	EP15_RN	A33	EP15_TN
B34	GND	A34	GND	B34	GND	A34	GND

[1] Option to pull-down.

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Table 2-6 J3 and J4 Pin Assignments

J4 Header				J3 Header			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
		G1	GND			G1	GND
2	GND	1	EP00_TP	2	GND	1	EP08_TP
4	EP00_RP	3	EP00_TN	4	EP08_RP	3	EP08_TN
6	EP00_RN	5	GND	6	EP08_RN	5	GND
8	GND	7	EP01_TP	8	GND	7	EP09_TP
10	EP01_RP	9	EP01_TN	10	EP09_RP	9	EP09_TN
12	EP01_RN	11	GND	12	EP09_RN	11	GND
14	GND	13	EP02_TP	14	GND	13	EP10_TP
16	EP02_RP	15	EP02_TN	16	EP10_RP	15	EP10_TN
18	EP02_RN	17	GND	18	EP10_RN	17	GND
20	GND	19	EP03_TP	20	GND	19	EP11_TP
22	EP03_RP	21	EP03_TN	22	EP11_RP	21	EP11_TN
24	EP03_RN	23	GND	24	EP11_RN	23	GND
26	GND	25		26	GND	25	EP12_TP
28	EP04_RP	27	EP04_TN	28	EP12_RP	27	EP12_TN
30	EP04_RN	29	GND	30	EP12_RN	29	GND
32	GND	31	EP05_TP	32	GND	31	EP13_TP
34	EP05_RP	33	EP05_TN	34	EP13_RP	33	EP13_TN
36	EP05_RN	35	GND	36	EP13_RN	35	GND
38	GND	37	EP06_TP	38	GND	37	EP14_TP
40	EP06_RP	39	EP06_TN	40	EP14_RP	39	EP14_TN
42	EP06_RN	41	GND	42	EP14_RN	41	GND
44	GND	43	EP07_TP	44	GND	43	EP15_TP
46	EP07_RP	45	EP07_TN	46	EP15_RP	45	EP15_TN
48	EP07_RN	47	GND	48	EP15_RN	47	GND
G2	GND			G2	GND		

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2.3 InfiniBand Connectors (J5 and J6)

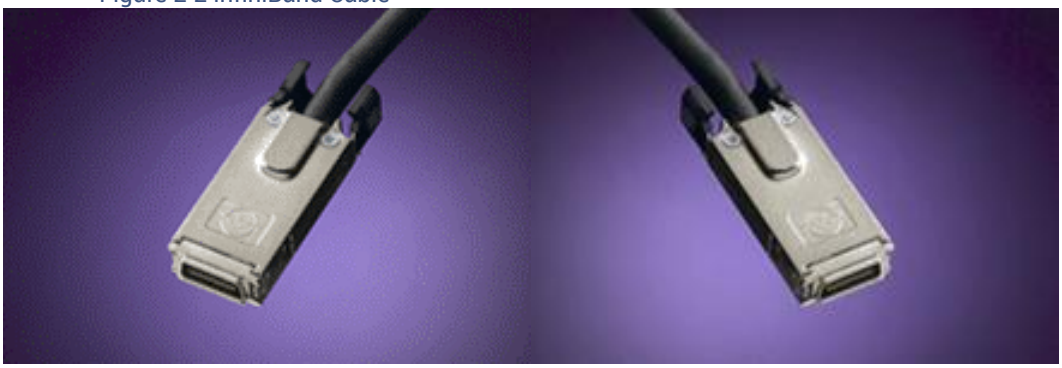
The FABRTMP1 also offers two Fabric ports that use InfiniBand connectors. These are defined as Data ports in slot profile SLT6-PAY-4F1Q2UT2T-10.2.1. If only a single Data Plane Port is required, Data Plane 0 (DP0) must be used (to comply with the OpenVPX specification). Molex 91804-0411 connectors are used for these ports.

Table 2-7 J5 and J6 Pin Assignments

J5 Header				J6 Header			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DP01_R0P	G1	GND	1	DP02_R0P	G1	GND
2	DP01_R0N			2	DP02_R0N		
3	DP01_R1P	G2	GND	3	DP02_R1P	G2	GND
4	DP01_R1N			4	DP02_R1N		
5	DP01_R2P	G3	GND	5	DP02_R2P	G3	GND
6	DP01_R2N			6	DP02_R2N		
7	DP01_R3P	G4	GND	7	DP02_R3P	G4	GND
8	DP01_R3N			8	DP02_R3N		
9	DP01_T3N	G5	GND	9	DP02_T3N	G5	GND
10	DP01_T3P			10	DP02_T3P		
11	DP01_T2N	G6	GND	11	DP02_T2N	G6	GND
12	DP01_T2P			12	DP02_T2P		
13	DP01_T1N	G7	GND	13	DP02_T1N	G7	GND
14	DP01_T1P			14	DP02_T1P		
15	DP01_T0N	G8	GND	15	DP02_T0N	G8	GND
16	DP01_T0P			16	DP02_T0P		
		G9	GND			G9	GND

Abaco can supply a suitable 4-lane InfiniBand cable (0.5 m in length) with Molex 74506-3001 connectors, as shown in Figure 2-2.

Figure 2-2 InfiniBand Cable



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2.4 Power Sequencing Header (P2)

The FABRTMP1 allows the power-up sequence of an NPN240 board to be controlled by up to two IPN250 boards. This feature is optional and is transparent to users when the FABRTMP1 is used in a system without NPN240 or IPN250 boards.

The NPN240 has two Graphics Processor Units (GPUs), which can be connected as follows:

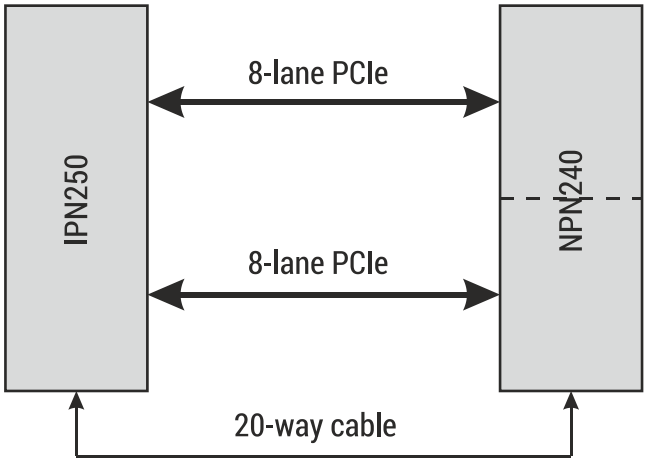
- Both GPUs can be connected to a single IPN250, using 8-lane PCIe buses between the IPN250 and the GPUs
- Both GPUs can be connected to separate IPN250s using 16-lane PCIe buses

In either situation, but particularly where there are two IPN250 boards in the system, in-rush current at power-up could be very high. To reduce the in-rush current, the start-up of the boards can be staggered.

A 20-way ribbon cable can be used to link between the NPN240 and either one or two IPN250s. This ribbon cable connects the signals that control the start-up sequence of the boards. The same ribbon cable IDC connector (P2) is used whether the FABRTMP1 is used with the IPN250 or the NPN240.

When the system contains a single IPN250 and a single NPN240, all 20 ways of the ribbon cable are connected between the two boards. This situation is shown in Figure 2-3.

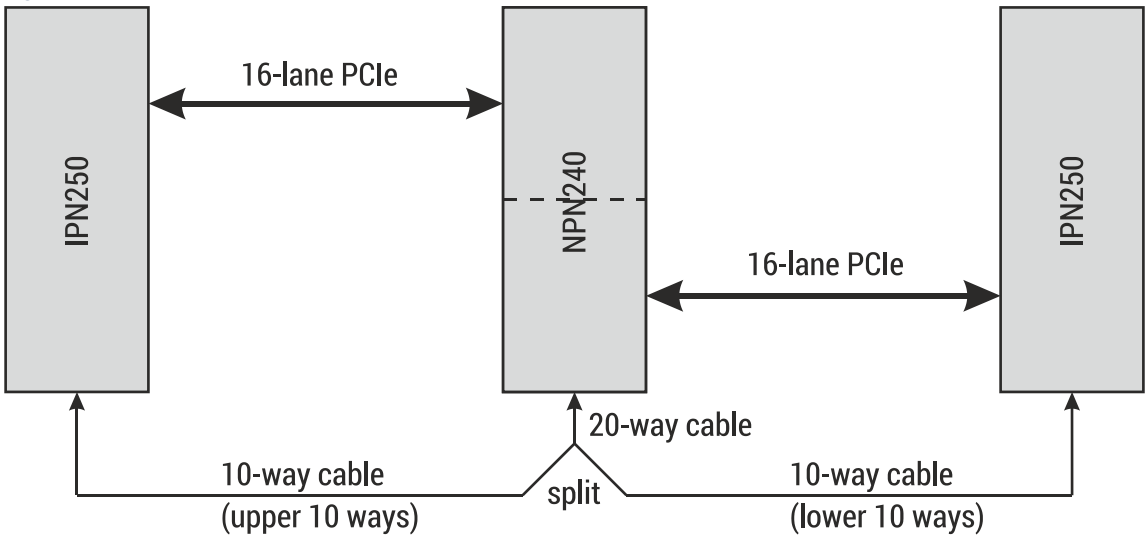
Figure 2-3 Ribbon Cable Connection of One IPN250 and One NPN240



When the system contains two IPN250s and a single NPN240, all 20 ways of the ribbon cable are connected on the FABRTMP1 connected to the NPN240, but 10 ways are connected to one of the FABRTMP1s connected to an IPN250 and the other 10 ways are connected to the second FABRTMP1 connected to an IPN250. This situation is shown in Figure 2-4.

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Figure 2-4 Ribbon Cable Connection of One NPN240 and Two IPN250s



NOTE

Maintain pin order through the cable, i.e. wire pin 1 of the fully populated 20-way IDC connector to pin one of one of the partially populated IDC connectors, and wire pin 20 of the fully populated IDC connector to pin 20 of the second partially-populated IDC connector.

Table 2-8 P2 Header Pin Assignments

Pin	Signal	Pin	Signal
1	GPU1_NODE_RST~	2	GND
3	GPU1_SEQ_IN	4	GND
5	GPU1_SEQ_OUT	6	GND
7	GPU1_POWR_SDA	8	GND
9	GPU1_POWR_SCL	10	GND
11	GPU2_NODE_RST~	12	GND
13	GPU2_SEQ_IN	14	GND
15	GPU2_SEQ_OUT	16	GND
17	GPU2_POWR_SDA	18	GND
19	GPU2_POWR_SCL	20	GND

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3 • Switches, Links and LEDs

3.1 Switches and Links

As the DIP switch may not be suitable for harsh environments (in which case it may be removed), equivalent functionality is offered via link block P1.

CAUTION

Use links *or* switches, *not* both. Whichever is not used should be set/left open.

3.1.1 Geographical Addressing

The FABRTMP1 can provide the Geographical Address (GA) of the payload board connected to it (i.e. setting the GA for that slot). The GA is configured on the FABRTMP1 using DIP switches/links. It is also possible to set the GA of the slot using DIP switches or links on the backplane.

CAUTION

Only set the GA on *either* the backplane *or* the FABRTMP1, *not* both (this may result in the incorrect address being set). Whichever is not used should have all the DIP switches/links left open.

The advantage of setting the GA on the FABRTMP1 is that the address will move with the RTM, should it ever be moved within the rack. The advantage of setting the GA on the backplane is that the GA is then locked to the slot. It is left to the user to decide which approach suits the application.

The first six DIP switches/links are used for setting the GA (including the parity), as shown in Table 3-1. Closing a switch/Linking the pins takes the function to the low/GND (active) state.

CAUTION

Do not use the same GA for more than one slot.

Table 3-1 Switch/Link Pin Assignments

Switch	Link Pins	Function	Associated LED
1	1 & 2	GAP~	DS2
2	3 & 4	GA4~	DS3
3	5 & 6	GA3~	DS4
4	7 & 8	GA2~	DS5
5	9 & 10	GA1~	DS6
6	11 & 12	GA0~	DS7
7	13 & 14	Unconnected[2]	-
8	15 & 16	SYSCON~	DS1

[2] Leave open.

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3.1.2 System Controller

The payload board associated with this FABRTMP1 can be made System Controller via DIP switches/links on the FABRTMP1, the backplane **or** the IPN250RTM.

CAUTION

Only set one of the options as System Controller – backplane, IPN250RTM *or* FABRTMP1. More than one may result in the incorrect payload board or multiple payload boards being set as System Controller. Whichever is not used should have DIP switches/links left open.

The last DIP switch/link is used for setting the System Controller, as shown in Table 3-1. Closing the switch/Linking the pins makes the associated payload board System Controller.

CAUTION

A system should not contain more than one System Controller.

3.1.3 Backplane Power Switch (S1)

Moving this center-biased momentary-action 3-way toggle switch in either direction activates the Backplane Power (BP_PWR~) function on payload boards that support this feature.

3.2 LEDs

3.2.1 System Controller LED (DS1)

This yellow LED reflects the System Controller status of the payload card. It is lit when the card is System Controller. See for the location of the LED.

NOTE

This LED shows the value set on the signal, which may not be the same as set by the DIP switch/link on the FABRTMP1 if another DIP switch/link associated with the slot in which the FABRTMP1 is fitted is set on the backplane or IPN250RTM.

3.2.2 Geographic Address LEDs (DS2 to DS7)

These LEDs show the GA of the slot. See Figure 3-1 for the locations of the LEDs.

Table 3-2 Geographic Address LEDs

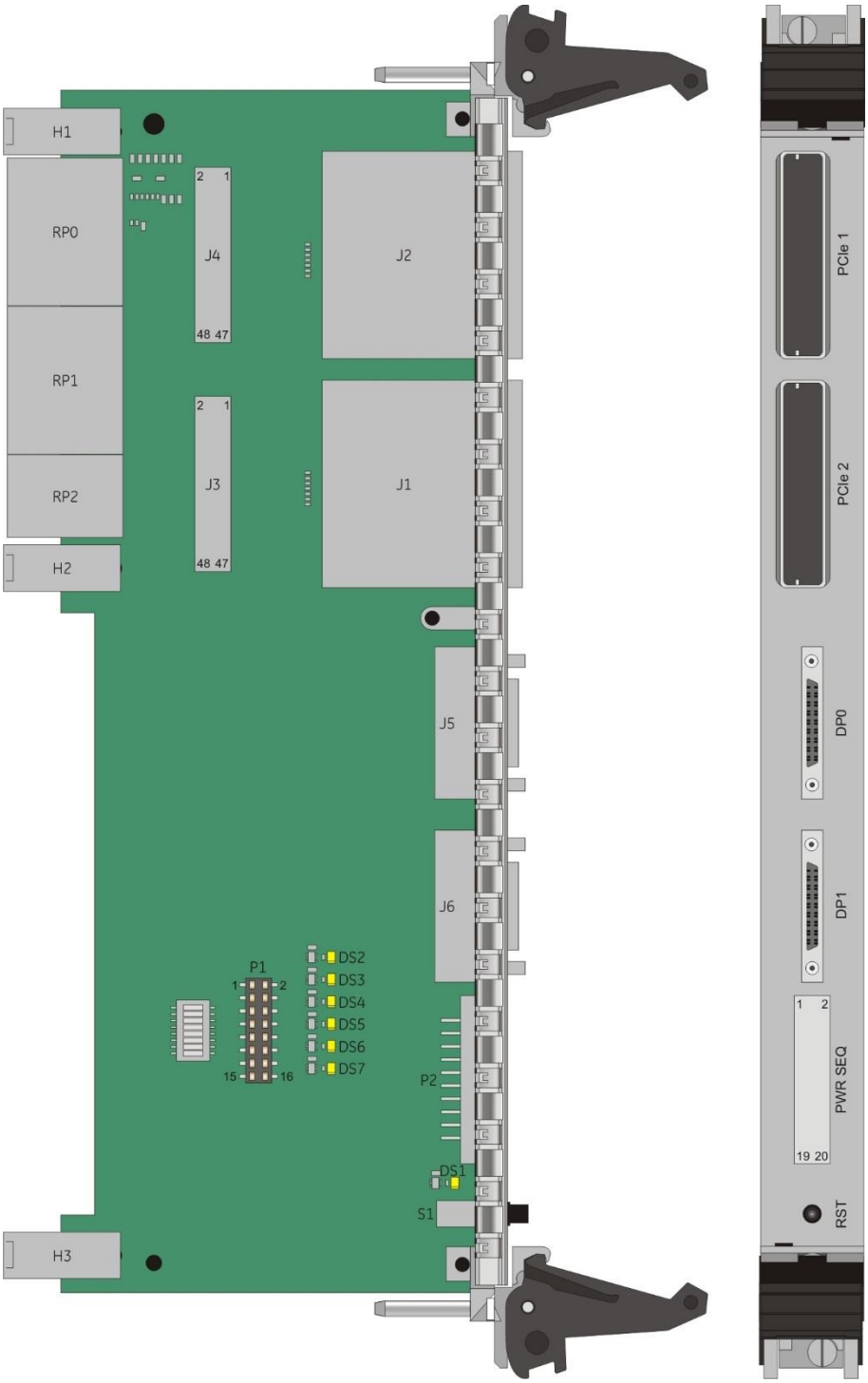
Number	Color	Signal Connected To
DS2	Yellow	GAP~
DS3	Yellow	GA4~
DS3	Yellow	GA3~
DS5	Yellow	GA2~
DS6	Yellow	GA1~
DS7	Yellow	GA0~

NOTE

These LEDs show the values set on the signals, which may not be exactly as set by the DIP switches/links on the FABRTMP1 if other DIP switches/links associated with the slot in which the FABRTMP1 is fitted are set on the backplane.

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Figure 3-1 FABRTMP1 LED Locations



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