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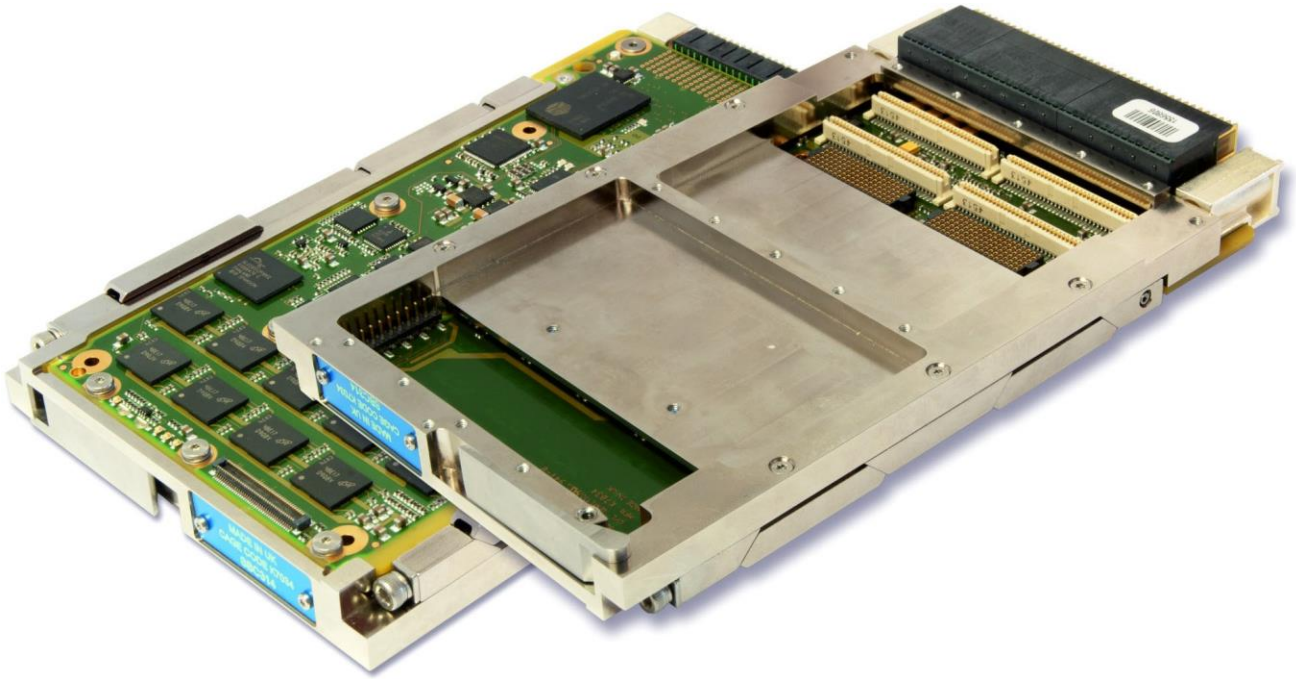
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Hardware Reference Manual

SBC314 3U OpenVPX HPEC Embedded Computer

Publication No. SBC314-HRM Rev. B



abaco SYSTEMS

Document History

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Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

About This Manual

Conventions

Notices

This manual may use the following types of notice:



WARNING

Warnings alert you to the risk of severe personal injury.



CAUTION

Cautions alert you to system danger or loss of data.



NOTE

Notes call attention to important features or instructions.



TIP

Tips give guidance on procedures that may be tackled in a number of ways.



LINK

Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

Unless specifically stated, this manual uses “SBC314” to refer to both the SBC314 and the SBC314X.

Further Information

Abaco Website

You can find information regarding Abaco products on the following website:

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https://www.abaco.com

Abaco Documents

This document is distributed via the Abaco website. You may register for access to manuals via the website.

LINKS

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH

VPX3UX300A Hardware Reference Manual, publication number VPX3UX300A-HRM

VPX3UX600A Hardware Reference Manual, publication number VPX3UX600A-HRM

FBIT for SBC314 Software Reference Manual, publication number FBIT-SBC314-SRM

Third-party Documents

http://www.freescale.com/	For T1042 and T2081 processorinformation
http://www.plx.com/	For PCI Express information

NOTE

Technical literature describing components used on the SBC314 is available from the manufacturers' websites.

Technical Support Contact Information

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1 • Introduction

The Abaco Systems SBC314 is a member of the VPXtreme3 family of 3U VPX Single Board Computers. It uses the Freescale T1042 or T2081 QorIQ processor running at up to 1.4/1.8 GHz.

The SBC314 offers up to 4 GByte of DDR3 SDRAM with ECC and up to 256 MByte of NOR Flash memory, together with up to three GbE channels, serial, USB 2.0, and SATA interfaces. Flexible configuration of serial fabrics is provided to suit a variety of system interconnect requirements, with up to eight lanes of PCIe available on the backplane.

The T1042/T2081 processor is connected to all onboard PCI devices and the mezzanine site using PCIe through a non-blocking switch architecture. One 64-bit PMC site is provided, supporting PCI-X operation at up to 133 MHz, allowing for standard commercial or custom mezzanines to be installed to add further functionality to the board. The site also supports XMC mezzanine cards, supporting a four lane PCIe link to the site, for higher bandwidth connectivity to the host and high-speed rear I/O.

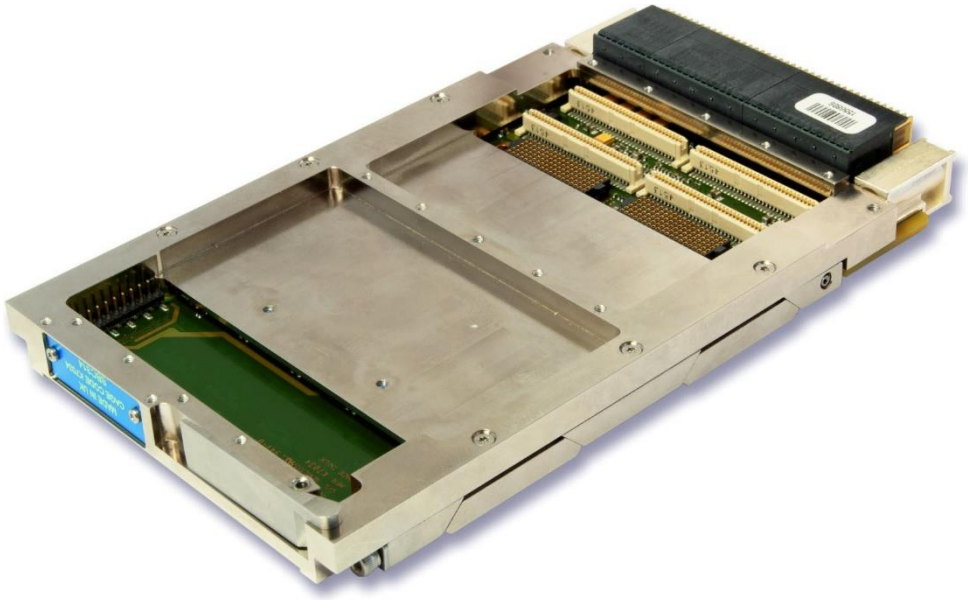
The SBC314 couples familiar software interfaces and reliability with high-speed fabric interfaces, offering significant increases in inter-board bandwidth.

This manual also covers the SBC314X, which is an XMC-only variant.

NOTE

Unless specifically stated, this manual uses “SBC314” to refer to both the SBC314 and the SBC314X.

Figure 1-1 SBC314 (Conduction-cooled) General View



1.1 Safety Notices

The following general safety precautions represent warnings of certain dangers of which Abaco Systems is aware. Failure to comply with these or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Abaco Systems assumes no liability for the user's failure to comply with these requirements. Also follow all warning instructions contained in associated system equipment manuals.

WARNING

Use extreme caution when handling, testing, and adjusting this equipment. This device may operate in an environment containing potentially dangerous voltages.

Ensure that all power to the system is removed before installing any device.

To minimize electric shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet IEC safety standards.

1.1.1 Handling

Figure 1-2 ESD Label (Present on Board Packaging)



2 • Configuration

Also see the 3U VPX SBC Family manual.

LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

2.1 Inspection

The SBC314 is shipped from Abaco with no jumpers installed.

2.2 Jumper Configuration

This manual refers to jumper settings as **In** or **Out**. Meanings are as follows:

In = jumper installed -

Out = jumper not installed -

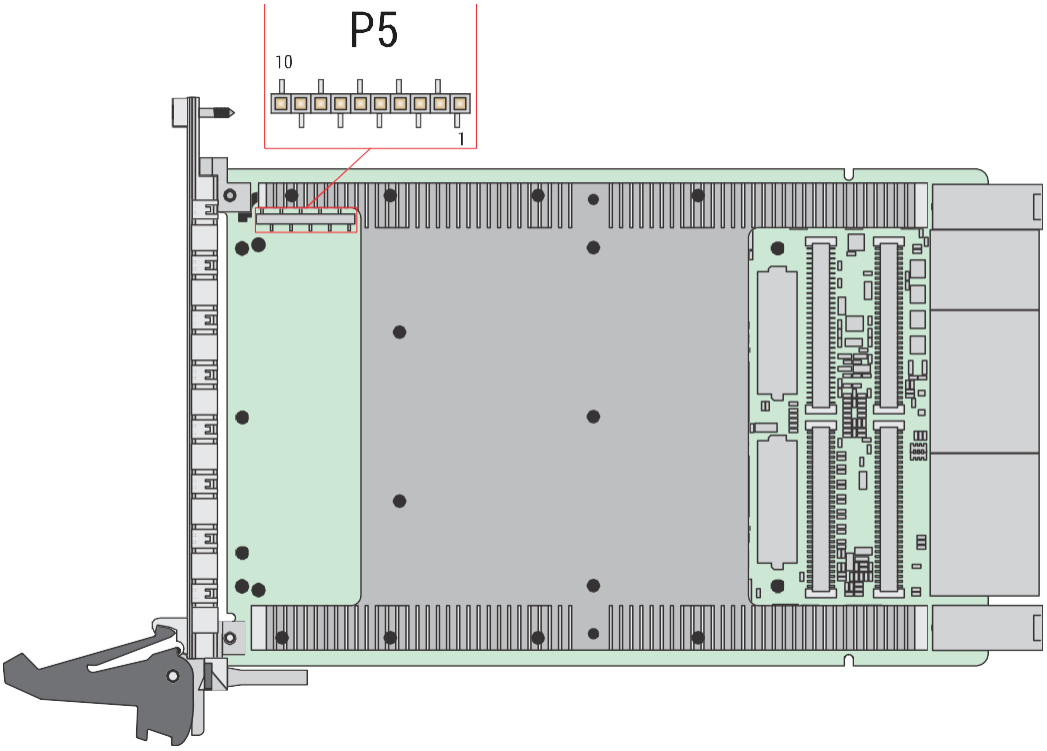
NOTES

Ordinary operation requires no jumpers to be installed.

Standard 2 mm pitch headers are used in the figure below.

The states of most of the jumpers can be read from a register - see Jumper Status Register (0x6CD).

Figure 2-1 Header Pin Positions



2.2.1 Boot Area Selection (P5 Pins 1 to 4)

The Boot Flash (for all processing cores) is divided into two sections, allowing two different boot images to be stored. There is also an Abaco-programmed Recovery boot image stored in a separate SPI Flash. These jumpers are used to select which image is used at boot time.

Pins 1 & 2	Pins 3 & 4	Active Boot Image
Out	Out	Main
In	Out	Alternate
Out	In	Recovery
In	In	Reserved

In normal operation, jumpers are not installed on these headers and the SBC314 boots from the Main boot image.

2.2.2 NVRAM Write-Enable Jumper (P5 Pins 5, 6)

This jumper controls the write-protection for the NVRAM device on the SBC314. This device holds firmware boot parameters as well as user data.

Setting	Function
Out	The NVRAM is write-protected
In	The NVRAM is write-enabled



NOTE

The VPX backplane NVMRO signal (on P0 Connector pin A4) and the onboard EEPROM DIP switch also play a part in configuring the NVRAM write-protection. See Section 4.5.3, "NVRAM" for details.

2.2.3 Flash Password Unlock Jumper (P5 Pins 7, 8)

For software to access the password to enable the Flash persistent sector protection to be changed, a jumper must be installed on this header. See Section 4.5.1 "NOR Flash"for further details.

Setting	Function
Out	Persistent sector protection cannot be altered
In	Persistent sector protection can be altered



NOTE

The VPX backplane NVMRO signal (on P0 Connector) must also be set inactive before the persistent sector protection can be altered.

2.2.4 Configuration Memory Write-Enable Jumper (P5 Pins 9, 10)

The SBC314 write-enables the Configuration Memory when a jumper is installed on this header (see Section 4.5.5, "Configuration EEPROM").

Setting	Function
Out	Configuration memory write-disabled
In	Configuration memory write-enabled

2.3 Mezzanine Installation

The SBC314 supports both PMCs and XMCs; the SBC314X only supports XMCs. See the 3U VPX SBC Family manual for other details.



LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM



TIP

Where a mezzanine is not pre-installed, prove operation of the SBC314 *before* installing the mezzanine.

2.3.1 PMC Installation



CAUTION

Ensure that the PMC 5V VIO software configuration is set according to the requirements of the corresponding PMC (see Section 4.15.4, "EEPROM DIP Switch"). Damage to the PMC may otherwise result.

2.4 Software Board Configuration

The SBC314 contains an I^2C EEPROM DIP Switch device (see Section 4.15.4, "EEPROM DIP Switch"), which may be used to configure additional board options under software control.

The VPX backplane NVMRO signal (on P0 Connector pin A4) must be pulled low before these settings can be modified (see Section 4.5.5, "Configuration EEPROM"). For details on how to monitor or change these settings, see the appropriate Software Reference Manual.

2.4.1 CPU UART Configuration

The SBC314 supports operating the UARTs within the T1042/T2081 in the following modes, which may be selected using this configuration option:

- COM1 and COM2 with flow control (the default)
- COM1, COM2, COM3 and COM4 without flow control

See Section 6.1.4, "Signal Definitions"for corresponding pinout changes.

This setting only takes effect following a reset of the SBC314.

3 • Installation and Powerup/Reset

Review Safety Notices before installing the SBC314. Also see the 3U VPX SBC Family manual.

LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

3.1 Power Supply Requirements

The SBC314's typical power requirements when running meaningful tests have been measured between 18 and 27 W (depending on temperature and processor speed). For more details, see Section A.3, "Electrical Specifications".

No voltage is required to be supplied on the Vs1 supply, as the SBC314 does not connect to these pins.

3.2 Board Installation

By default, the receptacles on the SBC314 for the guide pins are not keyed.

Correct adjustment of the screw-driven wedgelocks on conduction-cooled versions of the SBC314 requires a calibrated torque wrench with a hexagonal head of size 2.5 mm, set to 0.9 Nm (8 in-lb) ± 0.1 Nm/1 in-lb.

3.3 Connecting to SBC314

COM1 is configured by default as DTE with settings of 115200 baud, 8 bits/character, 1 stop bit, parity disabled and no flow control.

The appropriate RTM is VPX3UX600A, which provides access to the three Ethernet ports. In 3U racks, use the VPX3UX300A.

LINKS

VPX3UX600A Hardware Reference Manual, publication number VPX3UX600A-HRM

VPX3UX300A Hardware Reference Manual, publication number VPX3UX300A-HRM

The following items are also required:

- A null-modem 9-way D-type cable for connecting COM1 to a control terminal or PC running terminal emulation software
- For the Ethernet ports, a CAT5 (or better) straight-through patch cable for 10/100/1000BASE-TX

3.4 Reset and Powerup Sequence

A power sequencer monitors the backplane supply voltages and will hold the SBC314 in reset or shut down the onboard power supplies if the backplane supplies are not within specified limits.

The green Power Good LED is lit when the backplane and all onboard supplies are within specification.

The +5V supply to the mezzanine cards is switched, under the control of the Power Manager device, so that the 5V and 3.3V supplies are applied to the mezzanine card at approximately the same time.

4 • Functional Description

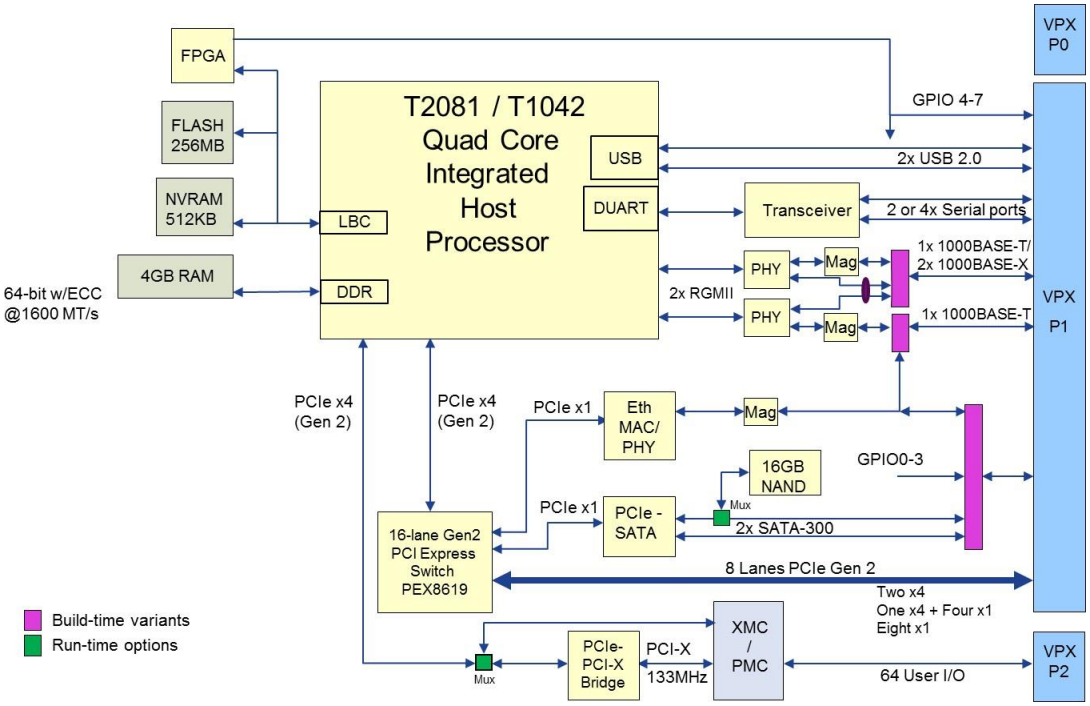
4.1 Features

- 3U OpenVPX single board computer
- Two PowerPC processor options
  - Freescale T1042 (four e5500 64-bit cores at up to 1.4 GHz)
  - Freescale T2081 (four e6500 64-bit dual-threaded cores with Altivec at up to 1.8 GHz)
- Up to 4 GByte DDR3L SDRAM
- Up to 256 MByte of NOR Flash
- Up to 16 GByte SATA SSD
- 512 KByte of Autostore NVRAM
- PCIe Gen2 data plane ports from VPX P1
  - (options for two x4, one x4 + four x1, or eight x1)
- One PMC/XMC site (XMC only on SBC314X)
- Up to three GbE ports
- Two RS-232/422 COM ports (or four RS-232)
- Up to two SATA ports
- Two USB 2.0
- Up to eight single-ended GPIO (5V tolerant)
- Board Management Microcontroller
- VITA65 OpenVPX Compatible
  - MOD3-PAY-2F2T-16.2.5-3
  - MOD3-PAY-2F2U -16.2.3-3

4.2 Architecture

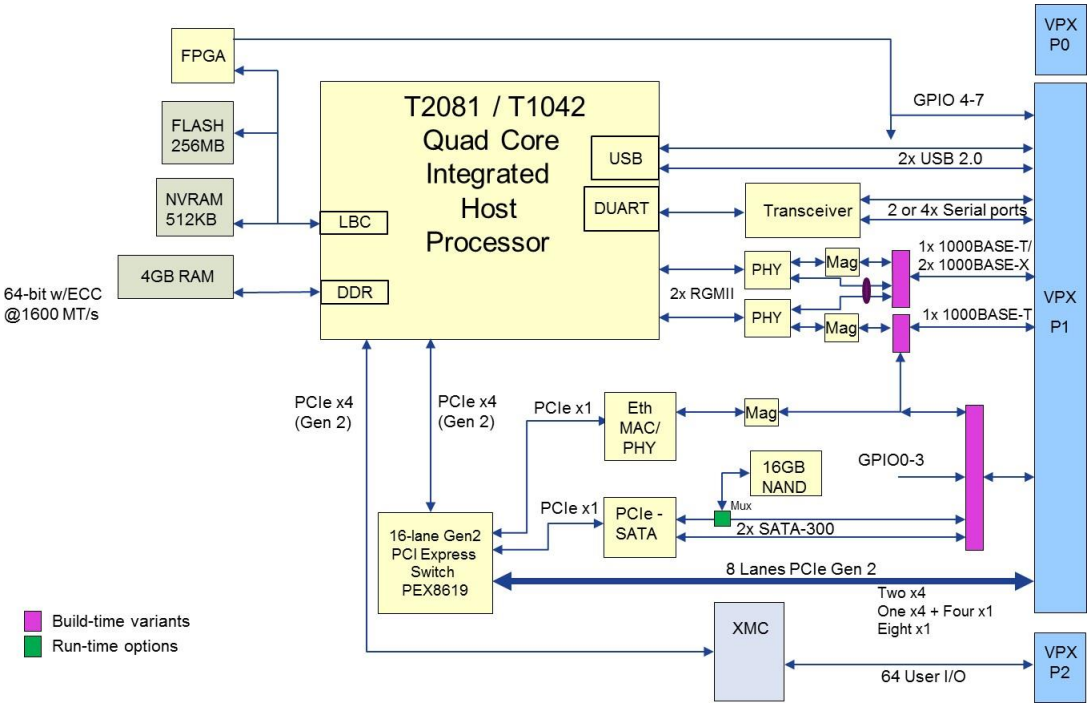
The architecture of the standard SBC314 is as shown below:

Figure 4-1 SBC314 Block Diagram



The SBC314X variant has a slightly different feature set. The architecture for this variant is shown below:

Figure 4-2 SBC314X Block Diagram



NOTES

1 - Due to the increasingly short lifetimes of system components, the I/O devices used on the SBC314 are not guaranteed to remain fixed in the future.

2 - Hardware should be accessed only through mechanisms provided by the Operating System's Board Support Package, and not directly by application software.

3 - If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimize direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.

4 - Abaco-supported Operating Systems guarantee compatibility at the application level through hardware independent mechanisms.

5 - A special "Avionics" configuration of the SBC314 is available to special order. This hasminor functional differences which are detailed elsewhere in the document.

4.3 Integrated Host Processor

4.3.1 Processor Features

The following table compares the features of the Freescale QorIQ T2081 and T1042 integrated host processors:

Processor	Cores	Maximum Frequency	Cache
T2081	4x e6500 64-bit, Altivec, dual-threaded	1.8 GHz	2 MByte banked L2 512 KByte Platform
T1042	4x e5500 64-bit, single-thread	1.4 GHz	256 KByte/core L2 256 KByte Platform

4.3.2 PowerPC Processing Cores

The T2081/T1042 contain four high-performance PowerPC processing cores. Each core includes:

- 32 KByte Level 1 instruction and data caches
- Physical addressing: 36-bit (T1042)/40-bit (T2081)
- Double Precision Floating Point Unit
- MMU with embedded Hypervisor privilege level

Table 4-1 Processor Frequencies

Processor	Core Frequency (GHz)	Platform Frequency	Memory Bus Frequency
T1042	1.4 or 1.2	600 MHz	800 MHz
T2081	1.5 or 1.8	TBD MHz	800 MHz

Depending on the application, it is possible for software to dynamically configure processors to run at lower clock frequencies to minimize power.

4.3.3 Trust Architecture

The T2081/T1042 CPUs contain a set of hardware features that support a trusted boot environment where only trusted code may be executed and hardware features that could be used to compromise security are disabled. The implementation of this architecture is fully described in the Freescale white paper "An Introduction to the QorIQ Platform's Trust Architecture".

The SBC314 provides the ability to program fuses within the CPU to configure security keys, access to which is controlled by the security state of the processor.

If you wish to use this feature of the platform, contact Abaco for more information.

4.3.4 Memory Map

The T2081/T1042 CPUs support a fully programmable memory map, shared between each of the processing cores. Memory windows are software-configured and the hardware does not carry out any configuration of the memory map. For this reason, no memory maps are provided in this manual.

Where addresses are provided in this manual, they are stated as a fixed offset from a software-programmable base address.

Refer to applicable software manuals for more information.

4.3.5 Reset Configuration Word

The CPU is configured, during reset, by loading a data structure called the Reset Configuration Word (RCW) from non-volatile memory. This specifies the operating frequency and numerous configuration options of the processor.

Normally the RCW is loaded from Abaco-configured settings within the FPGA (see Appendix C, "FPGA ROM Contents") and no user interaction is required. If more sophisticated configuration is required, it is possible to load the data structure from an I^2C EEPROM instead, by setting the relevant software configuration option in the I^2C EEPROM DIP Switch.



CAUTION

Do not change the source of the RCW unless advised to do so by Abaco. Incorrect or invalid settings may damage the processor or prevent the SBC314 from booting.

When booting from the Recovery boot area, the Abaco-configured RCW settings are always used. This allows the board to be recovered if the data in the I^2C EEPROM is invalid or becomes corrupted.

4.3.6 Local Bus

The T2081/T1042 has a 16-bit multiplexed address/data local bus, which is used to access the following devices on the SBC314:

- FPGA
- Flash
- NVRAM

4.3.7 Local Bus Memory Map

All eight device chip selects for the local bus are made available, shared between the devices as defined in the table below. The minimum possible window size is 32 KBytes.

Chip Select	Target	Device Width	Required Window Size
CS0	(Top half) NOR Flash - Boot area (2x 8 MByte) (Bottom half) RCW (in FPGA)	16	32 MBytes
CS1	NOR Flash	16	256 MBytes
CS2	NVRAM	8	512 KBytes
CS3	FPGA registers	8	4 KBytes
CS4	FPGA UART (BMM)	8	8 Bytes
CS5	Not used		
CS6	Not used		
CS7	Not used		

4.3.8 Processor Power Management

The T2081/T1042 devices implement the following power management features:

- Independent control of Doze/Nap modes for each processing core
- Device sleep state

4.4 SDRAM

The SBC314 provides one bank of nine DDR3L SDRAM devices connected to the memory controller within the processor. The T2081/T1042 CPUs contain a 64-bit DDR3 memory controller, which has full ECC error-correction support, with the ability to detect single and two-bit errors and correct single-bit errors within a nibble. The memory interface is capable of operating at 1600 MT/s.

4.4.1 Capacity

The SBC314 provides up to a total of 4 GByte of SDRAM in a single bank, connected to a separate memory controller. The RAM configuration is defined below:

Total RAM	Number of Devices	Device Type	Number of Banks per Controller
4 GByte	9	4 Gbit monolithic	1

The CPU controls the frequency of the RAM interface; Table 4-1 shows the possible configurations.

4.4.2 Serial Presence Detect

The SBC314 implements a mechanism similar to the JEDEC DDR3 SPD to indicate the RAM layout and timing information to system. The SPD uses a virtual I^2C ROM that is embedded within the FPGA.

4.5 Non-Volatile Memory

4.5.1 NOR Flash

The SBC314 provides 256 MByte of Flash memory, connected to the FPGA. The Flash uses 16-bit wide Spansion S29GL family devices, arranged in 128 KByte sectors. The Flash has an erase capacity of 100,000 cycles per sector and typical data retention of 20 years.

Table 4-2 Flash Organizations

Flash Size	Banks	Flash Bank Organization
256 MByte	1	1x 2 Gbit (S70 stacked die)



CAUTION

Integrity of Flash data cannot be guaranteed if a hard reset occurs during a Flash write cycle.

Boot Flash

The top 16 MByte of Flash memory is used as Boot Flash, and holds initialization and operating system boot routines. The Boot Flash region contains two independent 8 MByte boot areas (Main and Alternate). The active boot image can be selected using the P5 jumpers during development - see Section 2.2.1, "Boot Area Selection (P5 Pins 1 to 4)"for further information.



NOTE

The recovery area is in SPI Flash.

User Flash

Any Flash that is not used as Boot Flash is designated as User Flash and is intended to hold user application code or data. The CPU's Local Bus Controller uses CS1 to access User Flash. CS1 also provides access to the areas accessed by CS0 (at the top of the Flash array), but is not affected by the state of the Boot Image Select jumpers (P5 pins 1 to 4).

Flash Sector Protection

The SBC314 uses Spansion S29GL Flash devices, which provide advanced methods of sector protection to ensure the integrity of code data contained in the Flash array. Protection is defined on a per-sector basis, where a sector is 128 KByte in size. Locked sectors cannot be erased or programmed, they may only be read.

No write-protection of Flash is provided by hardware. Software must be used to configure the Flash devices to protect against corruption of Flash data. The following types of protection are provided:

- Persistent sector protection provides non-volatile protection that remains in place when a board is power cycled or reset. Each Flash sector may be set as locked (write-protected) or unlocked (write-enabled) by writing to configuration registers within the Flash. The configuration of this protection is only possible if the software provides the correct 'unlock' password. The password is stored in the FPGA, and it can only be read when the conditions in the flow chart are met (see Figure 4-3). If these conditions are not met, the software is unable to change the sector protection and those sectors that are locked may not be erased or reprogrammed under any circumstances.
- Non-persistent protection may also be used. In this case, sectors locked using Persistent mode may not be erased or reprogrammed, but previously unlocked may now be locked. However, this protection is only present until a power cycle or hardware reset occurs.



NOTE

Do not rely on non-persistent protection, as it may be subsequently altered by software. If further protection is required, use the Persistent protection method.

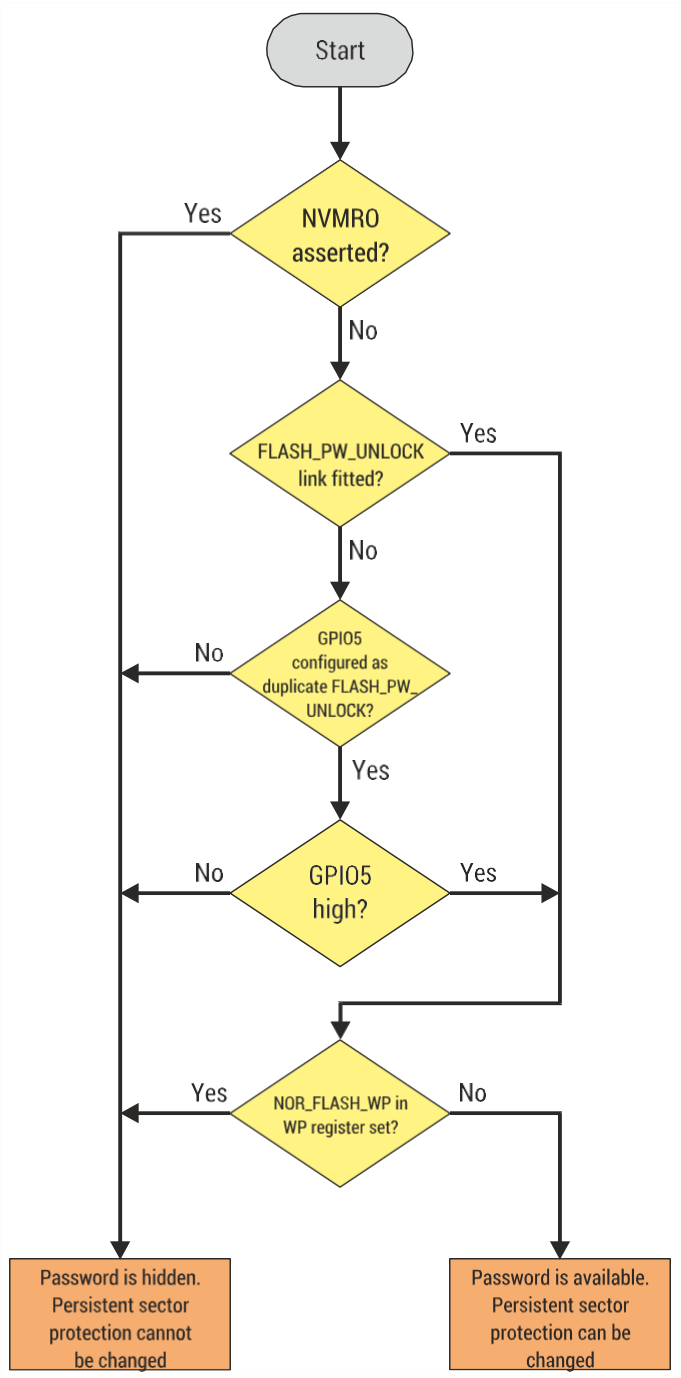
For further details of these protection mechanisms, see the S29GL Flash Family datasheet.

Software can detect the setting (installed or not installed) of the Flash Protection Unlock Jumper (P5 pins 7-8) - see Section 5.39, "Jumper Status Register (0x6CD).

Write-Protection

The following diagram shows the conditions necessary for the password to be made available for the persistent sector protection to be changed:

Figure 4-3 NOR Flash Write-Protection



NOTE

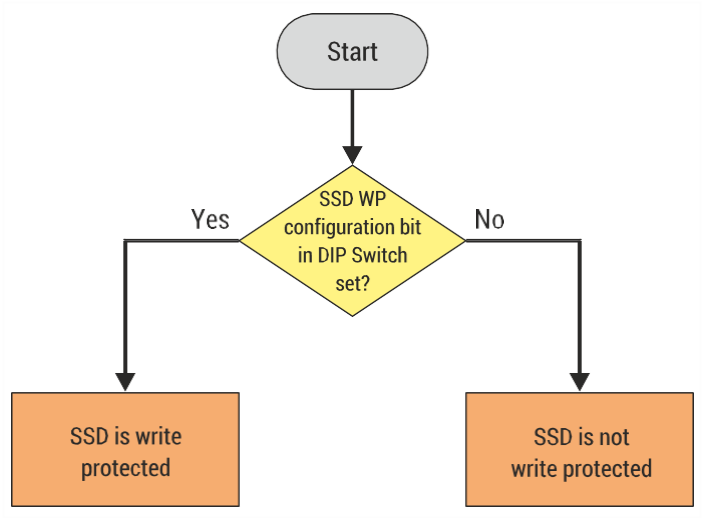
The default value of the NOR_FLASH_WP FPGA register is 'set'. Software must explicitly clear this bit to modify the Flash.

4.5.2 NAND Flash Solid State Drive

The SBC314 optionally supports up to 16 GByte of NAND Flash storage. This functionality is implemented using a SATA NAND Drive from Silicon Motion, device part number SM631 rev BA (1.2V core). The device incorporates wear leveling to maximize product lifespan.

Write-Protection

The following diagram shows the conditions necessary for the SSD to be write- protected:



NOTE

The state of the NVMRO backplane signal is ignored in this case.

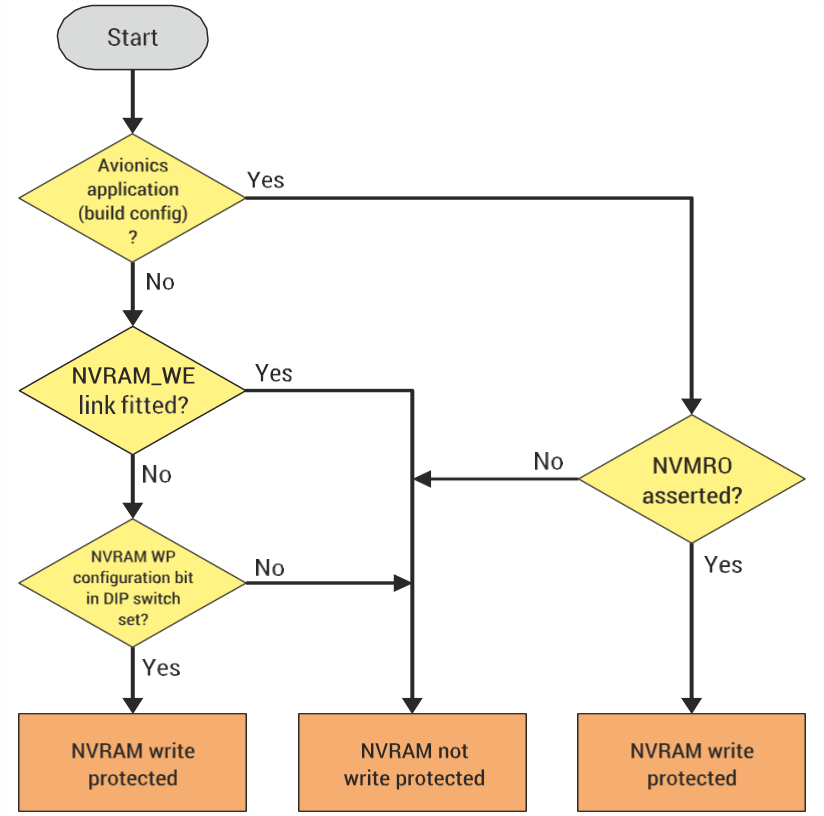
4.5.3 NVRAM

The SBC314 has 512 KByte of non-volatile RAM for configuration data storage and general purpose use. This functionality is implemented using an 8-bit wide Cypress CY14V104LA-BA45XI NVRAM device. This has unlimited read/write endurance and stated data retention is greater than 20 years.

CS2 on the CPU's Local Bus Controller is used to access the NVRAM, which can be read from and written to in the same way as standard RAM.

Write-Protection

The following diagram shows the conditions necessary for the NVRAM to be write-protected:



The NVRAM is write-protected when conditions in the flow chart are met. See the following sections for details:

- Section 2.2.2 for the NVRAM Write-Enable jumper's hardware status
- Section 5.39 for the NVRAM Write-Enable jumper's software status
- Section 5.36 for the NVMRO software status
- Section 4.15.4 for the EEPROM DIP Switch
- Section 5.47 for the EEPROM DIP Switch's software status
- Section 5.38 for the Write-Protection status of the NVRAM

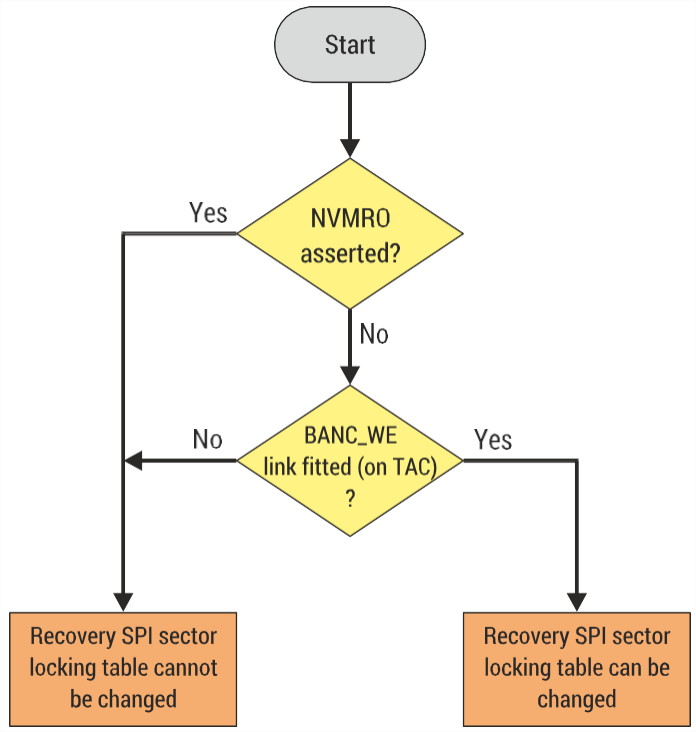
4.5.4 SPI Recovery Flash

An 8 MByte Micron N25Q064A11EF640 SPI Flash device is connected on the SPI interface of the CPU. This provides storage for recovery boot.

The lower 2 MByte of the SPI Flash is protected by default, and cannot be unprotected by the user. The remaining 6 MByte of the SPI Flash is for User storage.

Write-Protection

Recovery SPI write-protection is controlled by a table inside the Flash. The following diagram shows the conditions necessary for the Recovery SPI sector locking table to be changed:



4.5.5 Configuration EEPROM

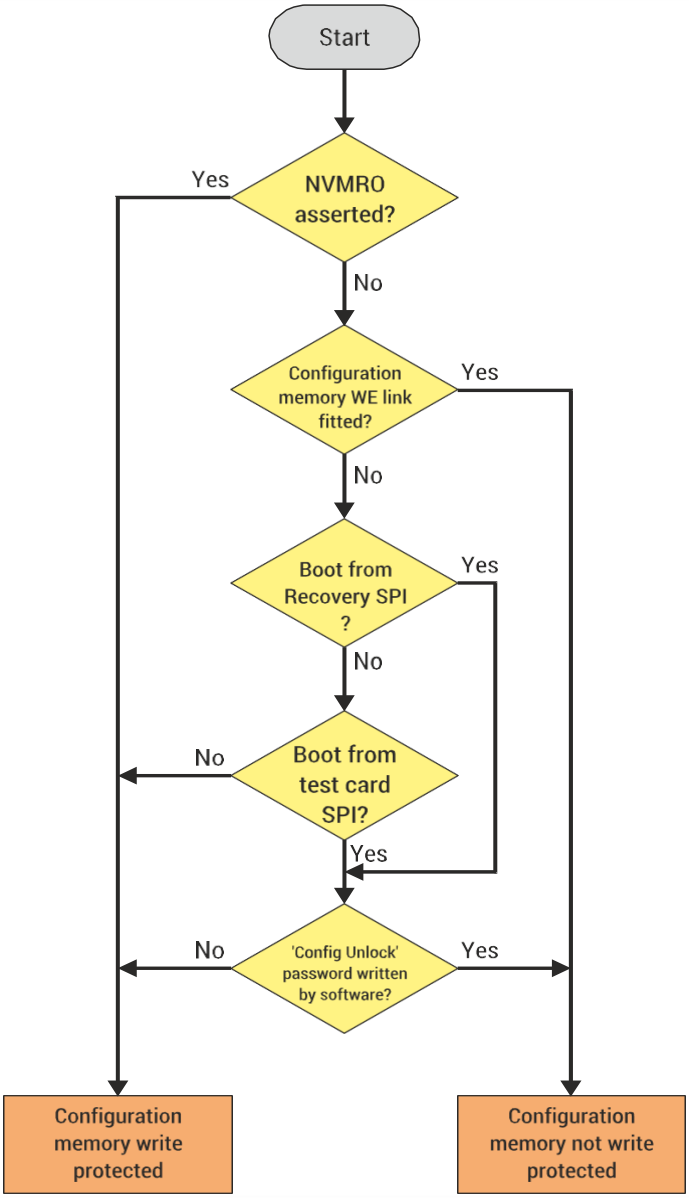
A 32 KByte 24LC256 EEPROM is attached to I²C Bus 1. If selected by the software configuration option, this can store the RCW for the CPU. The remainder of the Config EEPROM is available for general purpose use.

The device is write-enabled only when the conditions described in the flow chart (Figure 4-4) are met.

Write-Protection

The following diagram shows the conditions necessary for the Configuration Memory to be write-protected, and applies to all of the configuration memories on the SBC314: I2C Config EEPROM (see Section 4.15.2), I^2C EEPROM DIP switch (see Section 4.15.4), PCIe Switch Config EEPROM (see Section 4.7.2), Ethernet 2 config Flash, Power Manager and clock synthesizer firmware stores.

Figure 4-4 Configuration Memory Write-Protection



NOTE

The 'config unlock' password mechanism provides a method to perform jumperless in-system configuration changes. This can only be performed by the recovery bootloader.

4.6 VPX Interface

Also see the 3U VPX SBC Family manual.



3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

The interface to the VPX backplane is compatible with the following specifications:

- VITA 46.0
- VITA46.4 (for PCIe I/O)
- VITA46.9 (for PMC/XMC I/O)
- VITA46.11 (for system management)
- VITA65 (OpenVPX)

4.6.1 OpenVPX Compatibility

The SBC314 provides build options that are compatible with the following module profiles, as defined by the VITA65 OpenVPX Specification:

- MOD3-PAY-2F2U-16.2.3-3 payload module profile
- MOD3-PAY-2F2T-16.2.5-3 payload module profile

4.6.2 PCIe

See Section 4.7, "PCIe Infrastructure".

4.6.3 REF_CLK

The REF_CLK signal is driven with a 100 MHz PCIe differential output, using CML signaling, output when the SBC314 is configured as the System Controller. This can be subsequently disabled by software using a register: see Section 5.30.

REF_CLK is intended to be used as an optional PCIe common clock signal, and should only be routed to *one* other PCIe link partner.

When used as an NT endpoint, the SBC314 does not support receiving a PCIe reference clock.

4.6.4 AUX_CLK

The SBC314 can output a 25 MHz LVDS differential clock on AUX_CLK. It does not use this signal as an input.

4.6.5 Maskable Reset

The SBC314 is hard reset when MSKRST~ is asserted for more than 10 µs, unless the mask bit in a register is set by software - see VPX Control Register (0x6C1). The reset is masked by default.

The SBC314 can also drive MSKRST~ under software control, for example to reset a subset of other boards in the system, by setting a bit in the VPX Control Register.



NOTE

Maskable reset is not supported if the SBC314 is configured in the SBC310-compatible pinout; the signal is used for a serial port in this case.

4.6.6 Global Discrete

The SBC314 provides registers to drive GDISC1 under software control, to read its status and to generate an interrupt (with programmable polarity and edge/level selection). See Section 5.17, "GDiscrete1 Registers"for more information.

The Avionics Watchdog in the SBC314 can also be configured to generate an output on GDISC1.

4.7 PCIe Infrastructure

4.7.1 PCIe Features

The SBC314 uses PCIe for all high-speed serial interconnects, except where specified.

The SBC314 uses a PLX PEX8619 16-lane PCIe switch. This provides a x4 link to the CPU, operating at Gen2 speed (5 Gbit/s). The SBC314 supports 8 lanes of PCIe fabric to the VPX backplane and these backplane PCIe links are all connected directly to the PCIe switch. A PCIe Non-Transparent (NT) bridge function is supported between the CPU and the backplane fabric using the backplane links configured in NT mode.

The SBC314 provides a 100 MHz PCIe reference clock output to the backplane for use when the SBC314 is the system Root Complex. This uses DC-coupled CML signaling levels on the VPX REF_CLK pins. There is no option to provide (or receive) a 25 MHz REF_CLK.

The P1 connector is configured for PCIe in accordance with ANSI/VITA 46.4-2012.

4.7.2 PCIe Switch

Configuration EEPROM

The PCIe Switch circuitry includes an EEPROM that automatically configures the switch at initial powerup.



NOTE

If the SBC314 boots from the Recovery SPI or the TAC, the PCIe switch does not load its config EEPROM. This enables recovery in case of bad EEPROM data.

The PCIe Switch configuration EEPROM is an Atmel AT25256B-MAHL device, which is not directly connected to any CPU host bus. It is programmed by sending commands through the switch using the I^2C slave interface.

The configuration EEPROM is write-protected according to the conditions shown in Figure 4-4 and supports in-field updating by host software.

The central PCIe switch includes an I^2C slave interface for configuration by the CPU.

Powerup Configuration

The PCIe switch power-on configuration is set by pin straps. These are configured as detailed below:

Strap Name	Setting	Result	Comment
DEBUG_SEL0	1	PLX reserved	
FAST_BRINGUP#	1	PLX reserved	
NT_ENABLE#	1	NT disabled	Use EEPROM to enable NT mode
NT_P2P_EN#	1	NT Peer-to-peer disabled	
NT_UPSTRM_PORTSEL[3:0]	1111	NT upstream port = 15	Use EEPROM to select NT upstream port. [Datasheet requires port 15 when NT is disabled]
PLL_BYPASS#	1	PLX reserved	
PORTCFG[3:0]	0011	3x4+4x1	CPU and backplane links all x4, others x1 See Table 4-3
PROBE_MODE#	1	PLX reserved	
RESERVED17#	1	PLX reserved	
RESERVED16	0	PLX reserved	
SERDES_MODE_EN#	1	PLX reserved	
SMBUS_EN#	1	Master I^2C bus not used	
SPARE[5,1,0]#	111	PLX reserved	
SSC_ISO_ENABLE#	1	Spread spectrum clock not used	
TESTMODE[3:0]	1111	PLX reserved	
UPCFG_TIMER_EN#	1	Upconfig timer disabled	
UPSTRM_PORTSEL[3:0]	0000	CPU is upstream port	

Lane and Port Allocation

The PCIe Switch lane and port allocation is as shown below.

Table 4-3 PCIe Switch Lane and Port Allocation

Ports	Lanes	Port Width	Link To	Lane Reverse	Direction
All Configurations					
0	0 to 3	4	CPU	N	Up
13	14	1	Ethernet NIC	N/A	Down
11	13	1	SATA bridgea	N/A	Down
3,15	12,15	2	Not used	N/A	Down
Two x4 Configuration - STRAP_PORTCFG=3[b]					
1	8-11	4	Backplane Ac	N	Down/NT
2	4 to 7	4	Backplane Bc	N	Down/NT
One x4 and four x1 Configuration - STRAP_PORTCFG=2					
1	8 to 11	4	Backplane Ac	N	Down/NT
2	4	1	Backplane B0	N/A	Down/NT
10	5	1	Backplane B1	N/A	Down/NT
12	6	1	Backplane B2	N/A	Down/NT
14	7	1	Backplane B3	N/A	Down/NT
Eight x1 Configuration - STRAP_PORTCFG=1					
1	8	1	Backplane A0	N/A	Down/NT
5	9	1	Backplane A1	N/A	Down/NT
7	10	1	Backplane A2	N/A	Down/NT
9	11	1	Backplane A3	N/A	Down/NT
2	4	1	Backplane B0	N/A	Down/NT
10	5	1	Backplane B1	N/A	Down/NT
12	6	1	Backplane B2	N/A	Down/NT
14	7	1	Backplane B3	N/A	Down/NT

a.For correct operation, this lane must be configured to operate at Gen1 only.
b.This is the default configuration. Other configurations can be programmed into the EEPROM Switch - see Section 4.15.4, "EEPROM DIP Switch".
c.As defined by ANSI VITA 46.4.

By default, the SBC314 PCIe Fabric is configured to Gen2 (5 Gbit/s operation). If Gen1 is required, contact Abaco for the EEPROM settings.

Only one NT port can be selected at a time for connecting to other intelligent hosts, to provide address translation and mailboxes. These are available only on ports 4 to 11.

The configuration of these ports is altered by writing to the PCI Switch Configuration EEPROM under software control. The default configuration of the switch is with two x4 links with no NT ports.

4.7.3 SERDES Configurations

The following table shows the CPU SERDES configurations required to support the PCIe links:

	SERDES Lanes							
SRDS_PRTCL_S1	A	B	C	D	E	F	G	H
T1042 = 0x00 T2081 = 0xAA	PEX2 x4 (to switch)				PEX1 x4 (to XMC/PMC)			

4.7.4 SATA

A Silicon Image SIL3132 PCIe SATA controller implements the two SATA ports. It is connected back to the CPU via the central PCIe switch.

4.7.5 XMC/PMC Site PCI

The PMC site supports a 64-bit PCI bus capable of PCI-X operation at frequencies of up to 133 MHz. See Section 4.20.1, “PMCs” for further information.

The XMC site has a x4 PCIe link to the CPU. See Section 4.20.2, “XMCs” for further information.

The PCIe fabrics for the XMC site and the host side of the PMC bus bridge are multiplexed with an analog multiplexer, and connected to lanes E to H on the Integrated Host Processor.

4.7.6 Clocks and Clocking

The primary source of all the PCIe clocks is a Vectron VC801 oscillator. This is a 25 MHz device, running at 1.8V supply voltage. The oscillator output feeds into an IDT 9FGV0841 clock synthesizer. This device generates PCIe Gen2 quality, differential REFCLKs at 100 MHz for the eight PCIe endpoints on the SBC314.

The common-clocking output requirement on the backplane PCIe links is implemented by using a direct output from the synthesizer. This can be enabled or disabled under software control. When enabled, the output is a 100 MHz DC- coupled CML REFCLK pair. The SBC314 does not have any facility to receive a REFCLK from another board.

Clocks for the PCI-X bus to the PMC site are generated within the PCI-X bridge.

4.7.7 LED Display

There are 14 green LEDs that indicate the up/down link status of the PCIe links - on- and off-board. The LEDs are directly connected to the PCIe switch - see Section 4.21, “LEDs” for details of how the lanes are allocated.

An LED is provided per lane, not per link. Each LED lights when the lane is up at Gen2 speed, flashes when it is up at Gen1 speed, and goes out when the link is down.

A red LED indicates that the PCIe switch is asserting a fatal error condition. See the PCIe switch data sheet for details of what this means.

4.8 I/O

The SBC314 has the following I/O connectivity:

- Serial Ports
- Ethernet
- USB
- SATA
- GPIO

Due to pinout restrictions, some I/O shares pins on the various connectors. See Section 4.14, "I/O Funciton Rationalization" for further information.

4.9 Serial Port Communication Ports

The SBC314 provides up to four external serial ports.

4.9.1 COM1 and COM2

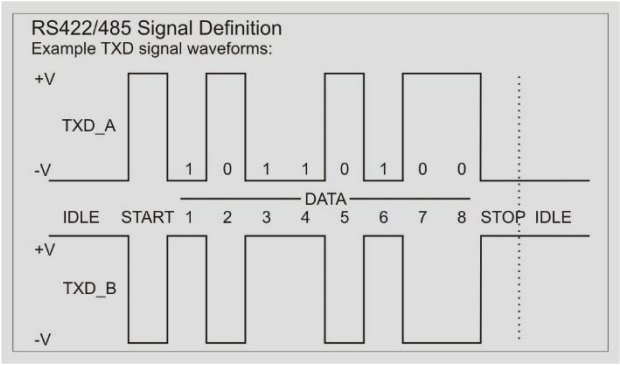
The CPU's DUART1 interface provides two debug ports with RTS/CTS hardware flow control. The signals for these ports are connected to ISL41334 serial transceivers capable of generating RS-232 or RS-422 signal levels.

Table 4-4 COM1/COM2 Signal Availability

COM1			COM2		
RS-232 Signal	RS-422 Signal	Pin	RS-232 Signal	RS-422 Signal	Pin
COM1_TXD	COM1_TXD_A	P1 G9	COM2_TXD	COM2_TXD_A	P1 G13
COM1_RXD	COM1_RXD_A	P1 G11	COM2_RXD	COM2_RXD_A	P2 G11
COM1_RTS	COM1_TXD_B	P2 G3	COM2_RTS	COM2_TXD_B	P2 G7
COM1_CTS	COM1_RXD_B	P2 G5	COM2_CTS	COM2_RXD_B	P2 G9

The option to operate the ports in RS-422 mode, or to disable or loopback the transceivers, under software control, is provided by registers: COM Port Enable Register (0x6BB), COM Port Mode Register (0x6BC), and COM Port Loopback Enable Register (0x6BE). The transceivers are disabled by default and must be enabled before any serial transfers can take place.

Figure 4-5 Example Waveforms



If the SBC314 is configured for SBC310-compatible I/O, COM2 is relocated as shown below. This is indicated by the SBC310 Mode bit (bit 1) in the Availability Configuration Register (0x6E8).

Signal	Pin
COM2_TXD	P1 G13
COM2_RXD	P1 G15
COM2_RTS	P2 G7
COM2_CTS	P2 G9

The baud rate is software programmable, derived from the platform frequency using the following equation:

Baud Rate = (1/16) * (Platform Frequency/(2 * Divisor Value))

The serial ports support baud rates up to 115200 baud in RS-232 mode, and up to 921600 baud in RS-422 mode.

The table below shows the divisors used for some commonly used baud rates and the percentage error associated with the use of an integer divider. The percentage error will increase significantly at higher baud rates. Different divisors will be required if a different Platform Frequency is used.

Target Baud Rate	Platform Frequency	Divisor (Decimal)	Divisor (Hex)	Actual Baud Rate	Error
9600	800 MHz	2604	0A2C	9600.61	0.0064%
19200	800 MHz	1302	0516	19201.23	0.0064%
38400	800 MHz	651	028B	38402.46	0.0064%
56000	800 MHz	446	01BE	56053.81	0.0961%
115200	800 MHz	217	00D9	115207.37	0.0064%
128000	800 MHz	195	00C3	128205.13	0.1603%
256000	800 MHz	98	0062	255102.04	-0.3508%

The actual performance of these ports will be limited by the throughput capability of the software driver and processor loading.

Software debug ports are configured by default as DTE with settings of 115200 baud, 8 bits/character, 1 stop bit, parity disabled and no flow control.

These ports can also operate as four separate two-wire (TX and RX) UARTs, as described below.

4.9.2 COM3 and COM4

The CPU can configure its DUARTs as four separate two-wire UARTs, without flow control. This feature is fixed by a field in the RCW. A bit in the I^2C EEPROM DIP switch allows one of two Abaco-supplied RCWs to be selected: typically RCW A configures two 4-wire ports and RCW B configures four 2-wire ports. If enabled, the extra ports are labeled COM3 and COM4.

When all four serial ports are used, COM1 and COM2 are driven by DUART1 within the CPU, and COM3 and COM4 are driven by DUART2. In this mode COM1 to COM4 must all be operated as RS-232 ports; RS-422 operation is not supported.



NOTE

The transceiver and loopback enable controls for COM3 are linked to those of COM1, and the transceiver and loopback enable controls for COM4 are linked to those of COM2.

Table 4-5 COM3/COM4 Signal Availability

COM3			COM4		
Signal	P2 Pin	COM1 Equivalence	Signal	P2 Pin	COM2 Equivalence
COM3_TXD	G3	COM1_RTS	COM4_TXD	G7	COM2_RTS
COM3_RXD	G5	COM1_CTS	COM4_RXD	G9	COM2_CTS

4.9.3 Host-to-BMM Serial Port

The FPGA contains an IP core for a 16550-compatible UART, which may be used by software running on the host processor to communicate with the onboard BMM if required.

The input clock to the BMM UART baud rate generator is 25 MHz – the input clock is the IFC bus clock (typically 50 MHz).

4.10 Ethernet

The CPU provides two Ethernet ports, connected via RGMII links to two Marvell 88E1512 PHYs. In 1000BASE-T configurations, the PHYs are isolated from the backplane using transformer-coupled magnetics.

All Ethernet channels support the IEEE 1588 precision timestamp protocol.

The Ethernet ports are mapped to Freescale and Intel Ethernet Controller interfaces as shown below:

T1042/T1081 Module	Ethernet Port	PHY Address
FM1_mEMAC4	ETH0	0
FM1_mEMAC5	ETH1	1
Intel I210	ETH2	2

LEDs are provided on the rear of the board to allow the status of each Ethernet interface to be monitored. See Section 4.21, "LEDs" for more details.

4.10.1 Third Ethernet Port

An optional third Ethernet port is implemented using an external Network Interface Controller (NIC). This is an Intel I210 ('Springville') part, which connects to the host via the central PCIe switch. Port 2, if used, is always configured to BASE-T mode, although its speed (10/100 or 1000 Mbit/s) depends on the build variant, i.e., which other backplane I/O interfaces are in use. Similarly, if 1000 Mbit/s is used, other backplane I/O interfaces are omitted due to backplane pin limitations.

If the third port is restricted to 10/100 Mbit/s because of other backplane I/O usage, then software should take appropriate steps to avoid advertising 1000 Mbit/s during negotiation. It is common for links to fail to come up if both endpoints advertise 1000 Mbit/s but the wiring only supports 10/100.

4.10.2 1000BASE-T Options

Two ports of 10/100/1000BASE-T Ethernet, ETH0 and ETH1, are provided on the VPX P1 connector. A third BASE-T Ethernet channel is optional (see the previous section). All build options with two or more 1000BASE-T Ethernet ports use the Ethernet pinout defined by OpenVPX module profile MOD3-PAY-2F2T-16.2.5-3.

ETH0		ETH1		ETH2		
Signal	P1 Pin	Signal	P1 Pin	Signal (1000)	P1 Pin	Signal (10/100)
ETH0_0P	A15	ETH1_0P	A13	ETH2_0P	A9	TX2+
ETH0_0N	B15	ETH1_0N	B13	ETH2_0N	B9	TX2-
ETH0_1P	D15	ETH1_1P	D13	ETH2_1P	D9	RX2+
ETH0_1N	E15	ETH1_1N	E13	ETH2_1N	E9	RX2-
ETH0_2P	B16	ETH1_2P	B14	ETH2_2P	B12	
ETH0_2N	C16	ETH1_2N	C14	ETH2_2N	C12	
ETH0_3P	E16	ETH1_3P	E14	ETH2_3P	D11	
ETH0_3N	F16	ETH1_3N	F14	ETH2_3N	E11	

4.10.3 1000BASE-X Options

The SBC314 supports 1000BASE-X Ethernet build options, as follows:

- Two 1000BASE-X Ethernet channels
- One 1000BASE-T plus two 1000BASE-X Ethernet channels

All build options with 1000BASE-X Ethernet ports use the Ethernet pinout defined by OpenVPX module profile MOD3-PAY-2F2T-16.2.3-3.

ETH1		ETH2	
Signal	P1 Pin	Signal	P1 Pin
ETH1_RXP	A15	ETH2_0P	A13
ETH1_RXN	B15	ETH2_0N	B13
ETH1_TXP	D15	ETH2_1P	D13
ETH1_TXN	E15	ETH2_1N	E13
ETH0_RXP	B16	ETH2_2P	B14
ETH0_RXN	C16	ETH2_2N	C14
ETH0_TXP	E16	ETH2_3P	E14
ETH0_TXN	F16	ETH2_3N	F14

4.11 USB

The CPU provides two USB2.0 ports to the P1 connector using on-chip PHYs.

USB1		USB2	
Signal	P1 Pin	Signal	P1 Pin
USB1_P	B10	USB2_P	E10
USB1_N	C10	USB2_N	F10
USB1_PWR	A11	USB2_PWR	B11

Power for these ports is provided by a Texas Instruments TPS2060. The SBC314 can deliver 500mA current on each port. The per-port power control and over- current fault detection signals are wired back to the CPU and are available in the host port controller blocks.

4.12 SATA

A Silicon Image Sil3132 PCIe to SATA controller, capable of operation at 3 Gbit/s, provides two SATA ports on the SBC314. The Sil3132 is connected to the PCIe switch via a x1 Gen1 PCIe link.

The first SATA port (SATA0) is connected directly to the P1 connector. The second SATA port is connected to the onboard SSD.

A second backplane SATA port (SATA1) on the P1 connector is a build option at the expense of four of the GPIO pins.

SATA0		SATA1		
Signal	P1 Pin	Signal	P1 Pin	GPIO Line
SATA0_TXP	D9	SATA1_TXP	D11	GPIO_0
SATA0_TXN	E9	SATA1_TXN	E11	GPIO_1
SATA0_RXP	A9	SATA1_RXP	B12	GPIO_2
SATA0_RXN	B9	SATA1_RXN	C12	GPIO_3

An LED on the rear of the board shows SSD use (see Section 4.21, "LEDs").

4.12.1 Limitations of SATA Use

Onboard SSD

Port 1 on the SATA controller can either be used for external SATA port 1 or the onboard SSD. An onboard multiplexer selects between these uses under software control - all other variants affecting SATA are fixed at build time.

I/O

One or both external SATA ports may be traded for other I/O, e.g., GPIO or Ethernet 2, in certain build variants - see Section 4.14, "I/O Function Rationalization".

Port 0 on the SATA controller is dedicated to external SATA port 0. This port is not available if Ethernet port 2 is used, unless Ethernet Ports 0 and 1 are configured in 1000BASE-X mode using the MOD3-PAY-2F2U-16.2.3-3 profile.

External SATA port 1 is not available if Ethernet port 2 is in use in 1000BASE-T mode, unless Ethernet Ports 0 and 1 are configured in 1000BASE-X mode using the MOD3-PAY-2F2U-16.2.3-3 profile.

4.13 GPIO

The SBC314 supports up to eight GPIO lines, each with interrupt generation capabilities. Each GPIO has a separate software-programmable direction control (input/output) and supports open-drain signaling when configured in output mode.

The GPIO ports have 3.3V LVCMOS signaling for output discretes and 3.3V LVCMOS signaling with 5V tolerance for input discretes.

The GPIO output high voltage may be as low as 2.0V, unless the external load current is less than 10µA.

The GPIO signals are routed to the P1 connector and P2 connector as follows:

GPIO Line	Pin	GPIO Line	Pin
0	P1 D11	4	P1 E12
1	P1 E11	5	P1 F12
2	P1 B12	6	P2 G13
3	P1 C12	7	P2 G15

GPIO[3:0] are not available if external SATA1 is used, or if Ethernet port 2 is set to 1000 Mbit/s.


LINK

See Section 4.15.4, "EEPROM DIP Switch" for further details of GPIO alternate features.

4.13.1 Redundant GPIO

GPIO with redundant tracking is available as a build variant.

Redundant GPIO is implemented by electrically connecting the circuits associated with GPIO[3:0] with those associated with GPIO[7:4]. In this mode therefore, only four external GPIOs are available. The backplane signals named GPIO4 to GPIO7 are used. This allows test software to read back the value output by any pin configured as an output by using the equivalent redundant pin as an input.

The FPGA implements no special behavior for (GPIO) output testing. To achieve this testing, software should configure the 'standard' GPIO (GPIO[7:4]) in output mode,

configure the ‘redundant’ GPIO (GPIO3:0]) in input mode, and read the ‘redundant’ GPIO input status in the normal way.

The FPGA implements no special behavior for (GPIO) input testing. Software can configure both the ‘standard’ GPIO and the ‘redundant’ GPIO in input mode, and read the actual status of both pins in the normal way.

If a mismatch between the standard and redundant GPIO pin states is detected, the redundant GPIO asserts its interrupt state. Mismatch interrupts are generated regardless of whether the GPIO is configured in input, output or test mode.

When not performing testing, software should configure the direction of both paired GPIOs to be the same. This will maximize resistance to open-circuit faults.

Software can determine how a GPIO is configured from the corresponding bits in the GPIO7:0 Availability and GPIO7:0 Interrupt High/Low Registers as follows:

GPIO7:0 Availability Bit	GPIO7:0 Interrupt High/Low Bit	GPIO Configuration
1	Read/write - controls interrupt polarity	Standard
0	Read only - 1	Redundant
0	Read only - 0	GPIO not available

4.14 I/O Function Rationalization

The figures below illustrate which of the possible I/O logic routes are selected to provide the four I/O variants that are generally available, and which are fixed at build time (see Section A.6, "Product Codes").

Figure 4-6 I/O Variants 1 and A

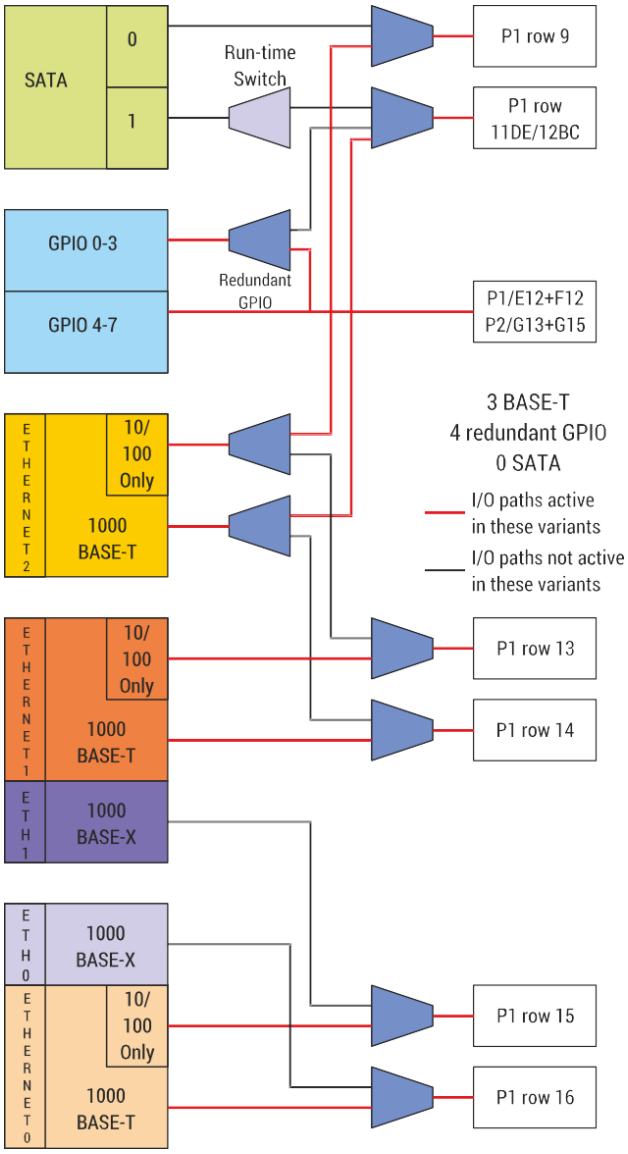


Figure 4-7 I/O Variants 2 and B

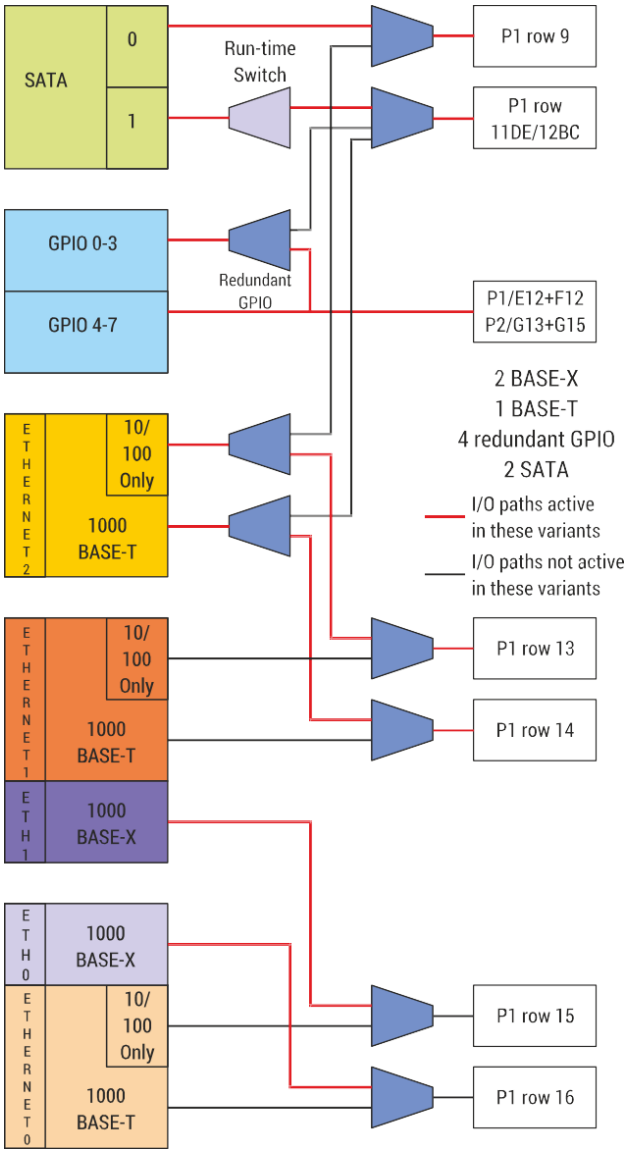


Figure 4-8 I/O Variants 3 and C

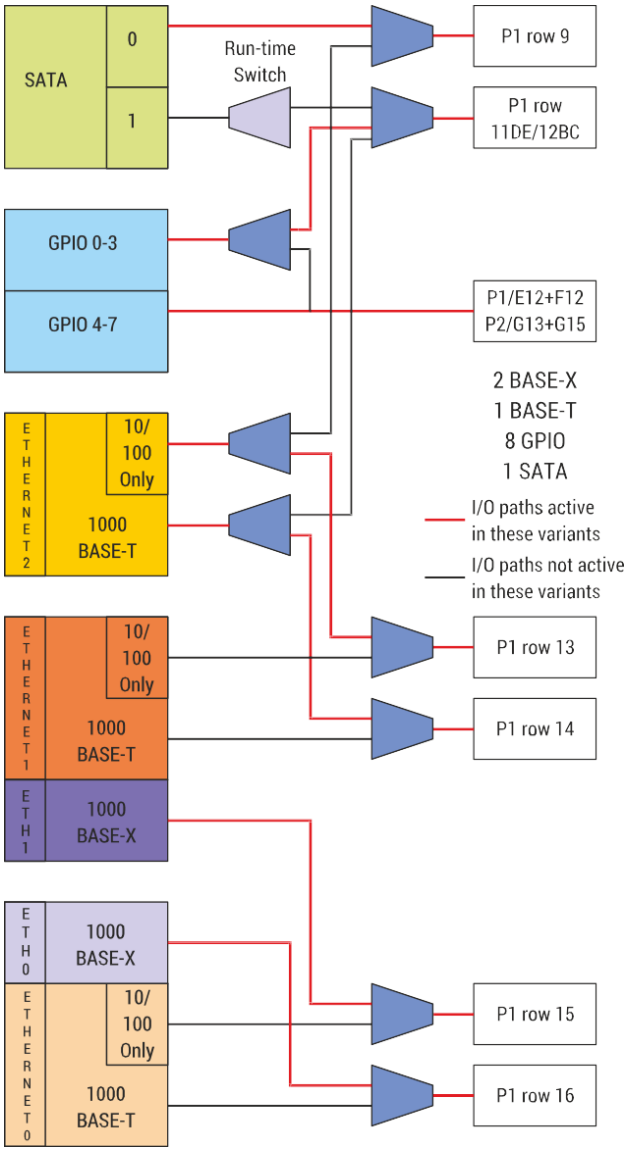
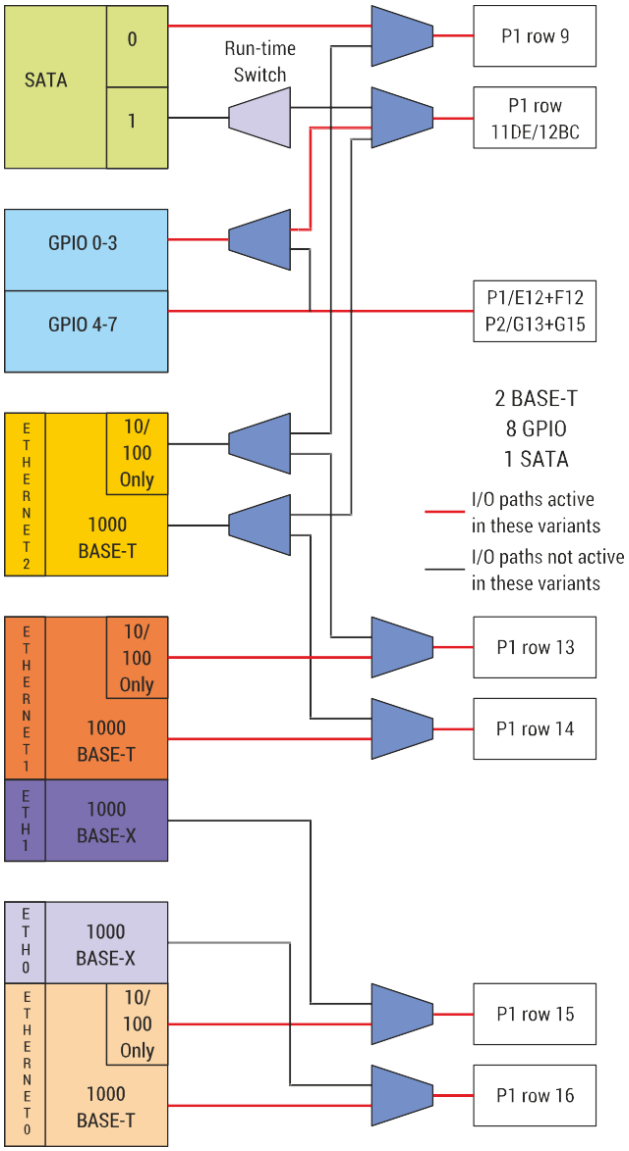


Figure 4-9 I/O Variants 4 and BD



4.15 I²C Buses

There are three major I²C buses on the SBC314:

1. The 'Main' bus. This is internal to the board and gives access from the CPU to various slave devices.
2. The 'Sensor' bus. This is mastered by the BMM and gives access to various sensor devices.
3. The 'Backplane' bus. This is only connected to the BMM and the backplane. It supports communication between system management agents without CPU intervention.

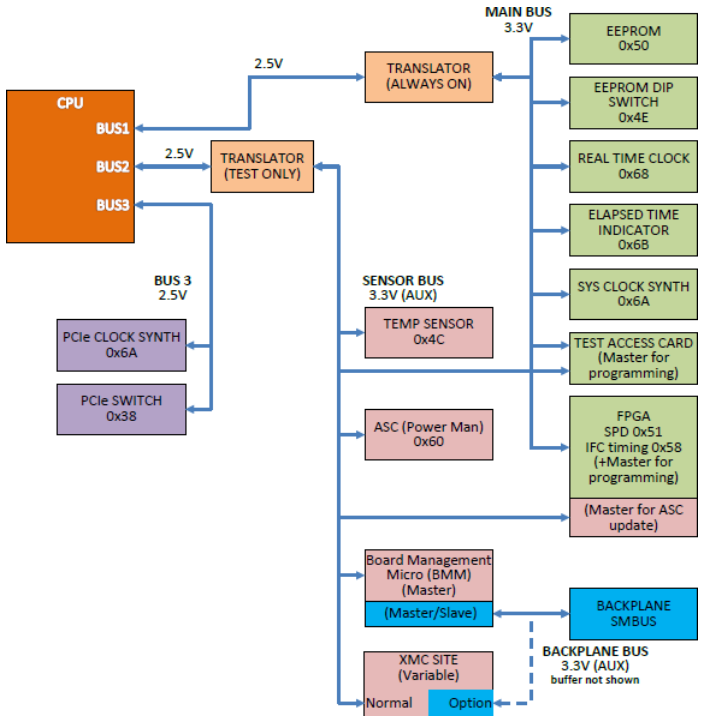
A small number of extra devices are connected to a third CPU I²C bus (labeled 'Bus 3' below).

If the CPU wishes to access devices on the Sensor bus, it must issue a command to the BMM to do this.

A translation buffer (with software disable function) is provided to electrically link a second CPU bus into the Sensor bus for test purposes, or if the BMM is not installed, or if the CPU negotiates ownership of the Sensor bus with the BMM. This buffer should not be used when the BMM is active, since the BMM is not multi-master capable.

The XMC site SMbus is normally connected to the Sensor bus. However, a build option allows this to be moved to the Backplane bus instead.

The following diagram shows the I²C bus topology:



4.15.1 I²C Reset

An I²C bus may potentially lock-up if the reset is applied (stopping the I²C clock) when a slave device (without a reset pin) is driving out data.

The CPU provides a software mechanism to recover from this state, so no hardware recovery mechanism is provided. The CPU and PCIe switch apply a reset pattern to the appropriate I²C buses before configuring from their EEPROMs.

4.15.2 CPU Config EEPROM

A 32 KByte 24LC256 EEPROM is attached to the 'Main' I²C Bus. If selected by the software configuration option, this can store the RCW for the CPU. The EEPROM is write-protected according to the conditions described in Section 4.5.5, "Configuration EEPROM".

4.15.3 Slave Addresses

Main Bus

The slave addresses of devices connected to CPU I²C 'Main' bus are listed below:

Device	Address (Main Bus) – 7 bit
EEPROM	0x50
EEPROM DIP Switch	0x4E
Real Time Clock	0x68
Elapsed Time Indicator	0x6B
SYS CLOCK Synthesizer	0x6A
FPGA/SPD	0x51
FPGA/IFC timing	0x58

Sensor Bus

The slave addresses of devices connected to CPU I²C 'Sensor' bus are listed below:

Device	Address (Sensor Bus) – 7 bit
Temperature Sensor	0x4C
ASC (Power Manager)	0x60

Bus 3

The slave addresses of devices connected to CPU I²C 'Bus 3' are listed below:

Device	Address (Bus 3) – 7 bit
PCIe Switch	0x38 - see Section 4.7.2, "PCIe Switch" and device data sheet for details
PCIe Clock synthesizer	0x6A - see Section 4.7.6, "Clocks and Clocking" for details

4.15.4 EEPROM DIP Switch

The SBC314 incorporates an EEPROM DIP switch, which is used to control functions as listed in the following table:

Register/Bit	Function
REG0 bit 0	XMC GA bit 2
REG0 bit 1	XMC GA bit 1
REG0 bit 2	XMC GA bit 0 For PMC deployments, program the XMC GA value 5D (101b) to select 5V VIO. Otherwise, VIO will be 3V3. VIO will always be set to 3V3 for combined XMC/PMC cards
REG0 bit 3	1 = Write-protect SSD 0 = Write-enable SSD
REG0 bit 4	1 = Select RCW B 0 = Select RCW A [RCW B is normally used to select four 2-wire UARTs, RCW A to select two 4-wire UARTs. See Appendix C, "FPGA ROM Contents" for RCW contents]. This bit has no effect if the RCW is loaded from the I^2C EEPROM. See below for Avionics Application build variant details. In this case, this bit has no effect
REG0 bit 5	1 = Load RCW from I^2C EEPROM 0 = Load RCW from FPGA
REG1 bit 0	1 = Reserved for GPIO4 special functiona 0 = GPIO4 standard function Also see Section 4.18.3, Avionics Watchdog Timer". GPIO4 has a special function there, which is enabled by software - not by this EEPROM register
REG1 bit 1	1 = Use GPIO5 as duplicate 'FLASH_PASSWORD_UNLOCK' link inputa 0 = GPIO5 standard function
REG1 bit 2	1 = Use GPIO6 as duplicate 'BOOT_ALTERNATE' link inputa 0 = GPIO6 standard function
REG1 bit 3	1 = Use GPIO7 as duplicate 'BOOT_RECOVERY' link inputa 0 = GPIO7 standard function
REG1 bit 4	1 = Boot site swap - invert physical state of 'BOOT_ALTERNATE' link/input 0 = Do not swap
REG1 bit 5	1 = Write-protect NVRAM 0 = Write-enable NVRAM

a. GPIO[7:4] alternative and duplicate link functions are active high.

The DIP switch programmed values are sampled at reset time. The SBC314 must be reset for any updates to take effect.

The DIP switch can only be updated when the conditions in the Config Memory write-protection flow chart are met (see Figure 4-4).

LINK

The DIP switch configuration register layout is detailed EEPROM DIP Switch Configuration Register 0 (0x6EA) and EEPROM DIP Switch Configuration Register 1 (0x6EB).

Avionics Application

In this build variant, the EEPROM DIP switch is not installed and a dedicated RCW with the following fixed values is loaded from the FPGA:

- DIPSW0[5:0] = 000000_b. This selects RCW A in the FPGA, Write-EnableSSD, XMC GA = 000
- DIPSW1[5:0] = 000010_b. This selects no write-protection of NVRAM; boot site not swapped; GPIO5 has alternate function; GPIO4, GPIO6 and GPIO7 have standard functions.

4.15.5 Real Time Clock

The SBC314 provides a Maxim DS3231 RTC, which has a minimum of 1 second resolution. This device can be powered from the P3V3_AUX supply, or the VBAT signal (P1 Connector pin G3) when the main power supply is removed. The interrupt output of the RTC can generate an interrupt to the processor via the FPGA interrupt controller.

4.15.6 Elapsed-Time Indicator

A Dallas DS1682 ETI logs the amount of time the SBC314 is powered and the number of power cycles.

4.15.7 Temperature Sensor

The SBC314 temperate sensor is an ADT7461, which monitors the temperature in the vicinity of the CPU, giving an indication of the core temperature. The interrupt outputs of this device can generate interrupts to the CPU, via the FPGA interrupt controller, at two software-defined thresholds.

4.15.8 Power Manager

The SBC314 uses a Lattice L-ASC10 programmable Power Manager to control all the onboard power supplies to meet supply sequencing requirements.

The Power Manager I^2C bus is connected to the BMM 'Sensor' I^2C bus. The standard method of reading Power Manager registers is to send a command via the BMM.

In addition to controlling the onboard supplies, the Power Manager also monitors each rail, and its voltage can be read from registers internal to the device, across the I^2C interface. The following table shows the allocation of power rails to the ASC monitor inputs:

ASC Input	Rail Monitored	Nominal Voltage	Trim	Input Attenuation
VMON1	VCORE	+0.9-1.05V	Y	x1
VMON2	P1V0	+1.0V	Y	x1
VMON3	P1V35	+1.35V	Y	x1
VMON4	P1V8	+1.8V	Y	x1
VMON5	VTT_DDR	+0.675V	N	x1
VMON6	P1V2	+1.2V	N	x1
VMON7	P2V5	+2.5V	N	x3
VMON8	P3V3	+3.3V	N	x3
VMON9	P3V3_AUX	+3.3V	N	x3
HVMON	P5V	+5.0V	N	x4

The Full Scale Input voltage of the ADC in the ASC is 2.048V, so voltages above 2V are attenuated inside the ASC. Software should enable the input attenuator when reading voltages above 2V (the Power Manager automatically corrects for this in the ADC output register). When reading the input voltages via the BMM, this correction is handled by the BMM firmware.

The SBC314 is reset whenever any of the monitored power rails are below specification. The board remains in reset until all of the monitored power rails return to specification.

The Power Manager drives a green Power Good LED (DS200) when all onboard power supplies are within tolerance. See Section 4.21, "LEDs".

Onboard Power Sequencing

The SBC314 uses the Power Manager device to sequence the power supplies in the required order for onboard devices. The sequencing is commanded by logic in the main FPGA, which uses a dedicated link channel to access internal functions of the Power Manager.

Onboard VCORE Adjustment

For the T2081, the VCORE rail can be adjusted within the range 0.9V to 1.1V by using the TRIM1_SETPOINT0 register in the Power Manager (see the Lattice L-ASC10 data sheet for details). Refer to the T2081 data sheet for details of how to determine the correct VCORE voltage for a T2081 build - this value is stored (by the device manufacturer) in laser fuses inside every CPU.



CAUTION

Do *not* change the VCORE rail for a T1042 build.

4.15.9 Board Management Microcontroller

The SBC314 has a BMM, which provides a proprietary mechanism to enable sharing of BIT results between boards in a system and remote monitoring of board status.

The BMM is connected to a backplane I^2C Serial Management bus (using the SM connections on the P0 Connector) which is bused between all slots in the system. The BMM on each board is addressed based on its Geographic Address as shown in the following table. These are the byte addresses that would be used to write to the device on the bus (i.e., the 7-bit device address and the LSB set to '0').

Slot	GA[4:0]	I^2C Address	Slot	GA[4:0]	I^2C Address	Slot	GA[4:0]	I^2C Address
1	11110	0xB0	8	10111	0xBE	15	10000	0xCE
2	11101	0xB2	9	10110	0xC0	16	01111	0xD0
3	11100	0xB4	10	10101	0xC4	17	01110	0xD2
4	11011	0xB6	11	10100	0xC6	18	01101	0xD4
5	11010	0xB8	12	10011	0xC8	19	01100	0xD6
6	11001	0xBA	13	10010	0xCA	20	01011	0xD8
7	11000	0xBC	14	10001	0xCC	21	01010	0xDA

The System Management pins of the XMC site are also connected to the BMM Serial Management Bus. The lower 3 bits of its address are determined by the Geographic Address pins generated by the DIP Switch, as shown in the table below. Again, these are the byte addresses that would be used to write to the device on the bus (i.e., the 7-bit device address and LSB set to '0').

VPX_GA[2:0]	I^2C Address	VPX_GA[2:0]	I^2C Address
000	0xA0	100	0xA8
001	0xA2	101	0xAA
010	0xA4	110	0xAC
011	0xA6	111	N/A

The BMM is also connected to the COM port from the FPGA.

The BMM is also connected to the I^2C 'Sensor' Bus, providing access for out-of- band monitoring of board status information such as voltage rail status or board temperatures by any other board in the system.

The BMM is powered from the P3V3_AUX supply, meaning that board configuration information or BIT status can be read out of the device without enabling the main power rail. An I^2C buffer is sited on the I^2C 'Sensor' Bus to allow the BMM to access the Power Manager device when the onboard supplies are not powered up.

4.16 Timers

4.16.1 General Purpose Timers

The CPU provides eight 31-bit general-purpose timers, each capable of generating interrupts to the processor. Each group of four timers can be set to operate from a divider of the platform's clock (divided by 8, 16, 32 or 64). Each group of timers can also be cascaded to form two 63-bit timers, one 95-bit timer or one 127-bit timer, if required.

The FPGA provides four additional 32-bit counters. The source clock for these counters can be chosen from 25 MHz, 2 MHz or the CPU IFC bus clock, and a programmable pre-scaler can be used to achieve 1:2, 1:4 or 1:8 reduction of the clock input. The timers can be programmed to generate an interrupt on expiry, and any 32-bit value can be loaded into the timer as a start value. The timers can be programmed to roll-over on expiry and reload the initial start value, or they can be programmed into one-shot mode where they will stop counting when expired. Together, these features provide a highly flexible timer solution. The FPGA timers are intended only to be used by Abaco software drivers (see the relevant software manual for details). Also see Section 5.14, "Timer Registers".

As well as the Watchdog timer provided by the FPGA (see below), each e500mc core also provides an internal Watchdog timer that can be configured to generate an internal interrupt, core reset, or system reset.

4.16.2 Avionics Watchdog Timer

An Avionics Watchdog Timer is included in the FPGA - see Section 4.18.3, "Avionics Watchdog Timer" for more details.

Legacy Watchdog

The SBC314 does not include a legacy watchdog timer, i.e., one that is compatible with the 'Haswell standard' Watchdog. The Avionics Watchdog Timer that is included, provides functionality as described later.

4.17 Resets and Interrupts

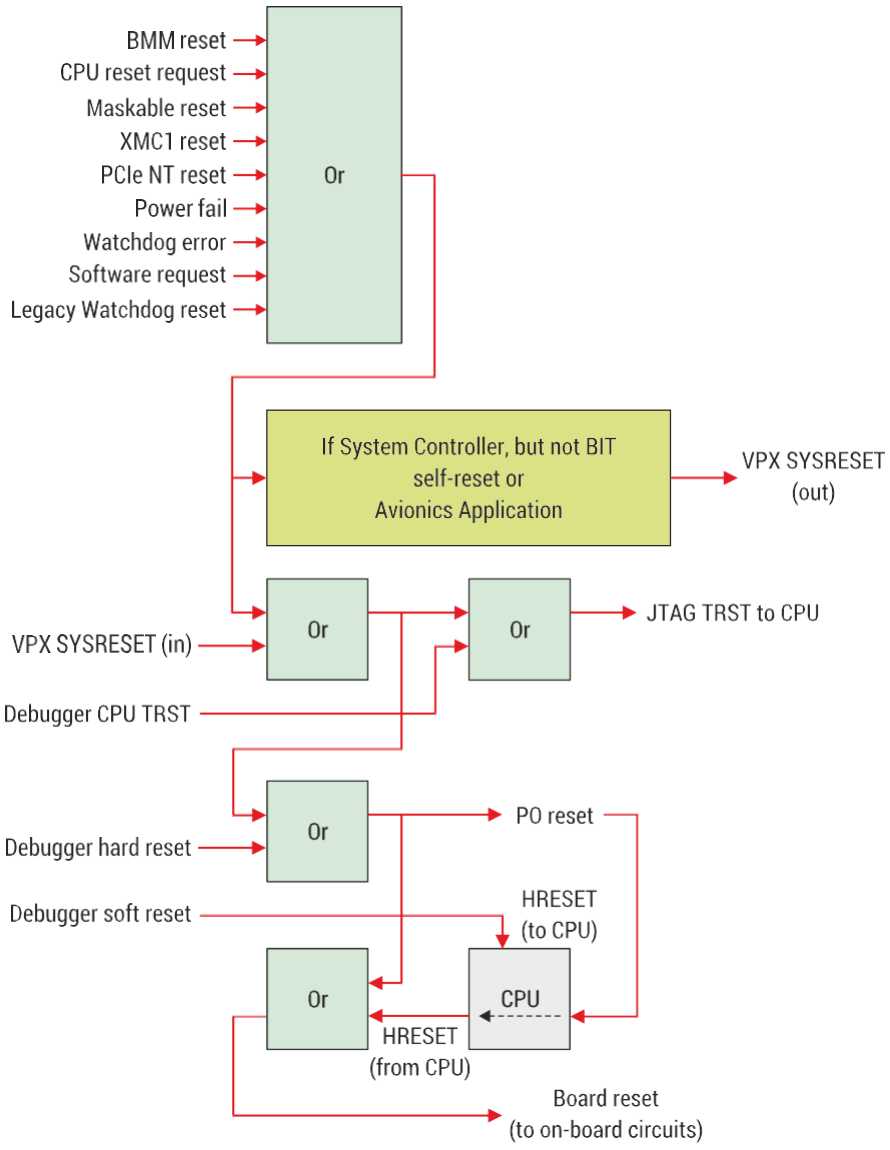
The Programmable Interrupt Controller within the CPU controls the resets and interrupts to the processing cores.

The following table shows the various external interrupt sources to the Interrupt Controller and their relative priorities. It also shows whether the previous state of the processor is recoverable.

Priority	Interrupt	Cause	Recoverability
0	Power-on reset	PORESET~ input	Non-recoverable
1	Hard Reset Input	HRESET~ input	Non-recoverable
2	External Interrupt	IRQ~ inputs	Recoverable

4.17.1 Reset Logic

External to the CPU, the FPGA controls all other on and off-board reset signals; this reset logic is as shown below.



4.17.2 Reset Causes

The following list of reset causes will each generate a CPU power-on reset (PORESET), and a hard reset to all onboard circuits. If the reset source is asserted for less than 10 ms, then the reset logic will extend the reset to a minimum of 10 ms.

The SBC314 records the reason for reset in a memory-mapped register that is accessible to software.

Power Fail

The SBC314 is reset, and remains in reset, whenever any of the monitored power rails are below specification.

BMM Reset

The reset logic resets the SBC314 whenever the BMM Reset Out input from the BMM is asserted.

CPU Reset Request

The reset logic resets the SBC314 whenever the CPU Reset Request input from the CPU is asserted.


NOTE

Some FPGA register bits are 'sticky'. These maintain their state if the reset cause is a CPU reset request.

Maskable Reset

When the Maskable Reset backplane signal is asserted, this resets the CPU (PORESET) and also resets all onboard circuits.


NOTE

This reset cause can be enabled or disabled by software. The default configuration of the SBC314 is to ignore the Maskable Reset backplane signal.

XMC1 Reset Request

The reset logic resets the SBC314 when the XMC card asserts its MRSTO output.


NOTE

This signal can be enabled/disabled under software control. The default setting is 'enabled'.

PCIe NT Reset

The reset logic resets the SBC314 when the PCIe switch asserts a reset request from the NT bridge, i.e., the SBC314 is acting as an endpoint under the control of an external PCIe Root Complex.


NOTE

This can be enabled/disabled under software control. The default setting is 'disabled'.

Watchdog Error

The reset logic resets the SBC314 whenever the Avionics Watchdog detects an error condition.

Software Request

The SBC314 FPGA incorporates a mechanism for application software to initiate a self-reset; this is the 'HRESET' bit (see BIT Control/Status Register (0x629).

The SBC314 FPGA includes several register bits and scratchpad storage that are not cleared on a software-initiated self-reset. These register bits are sticky for both the BIT HRESET register in the FPGA and the CPU_RESET_REQ output from the CPU.

4.17.3 SYSRESET

Receipt of a SYSRESET input from the backplane resets the CPU (PORESET) and all other onboard circuits.

When configured as VPX System Controller, the SBC314 usually drives the VPX SYSRESET backplane signal low when an onboard reset condition is asserted. The exception to this is when the reset is caused by software setting the BIT_HRESET register, in which case software can decide whether to send SYSRESET out to the backplane.

In the Avionics Application build variant, the SBC314 drives the VPX SYSRESET backplane signal low when an onboard reset condition is asserted, regardless of whether it is System Controller.

4.17.4 Debugger Resets

The Debugger header on the TAC is responsible for various resets being asserted, as shown below:

Reset Source	*Reset outputs asserted/not asserted by debugger resets*				
	CPU JTAG Reset	CPU PO Reset	CPU HRESET[a]	SYSRESET OUT	Board Reset
Debugger JTAG Reset	Asserted	Not asserted	Not asserted	Not asserted	Not asserted
Debugger HRESET	Not asserted	Asserted	Not asserted	Not asserted	Asserted
Debugger SRESET	Not asserted	Not asserted	Asserted	Not asserted	Asserted
Other resets as listed	Asserted	Asserted	Not asserted	Sometimes asserted	Asserted

a.This column indicates when the reset logic drives HRESET to the CPU. The CPU always drives HRESET to the FPGA when PORESET is asserted.

4.17.5 Board Reset

The reset logic resets all other circuits on the SBC314 when any of the reset causes above are asserted or the HRESET signal is asserted (by either the FPGA itself or by the CPU).

The Reset Cause register is updated whenever either the Power-on reset or CPU Hard Resets are initially asserted. For clarity, this means that the register only logs the *initial* cause of the reset - if subsequent reset inputs overlap with earlier ones then these are *not* logged (although they may extend the reset).

The FPGA drives the Power-on Configuration word (POR_CFG) onto the CPU bus whenever the CPU is in power-on reset. This tells the CPU which device to boot from, and also includes a sticky Scratch register that boot software can use to record boot progress.

The BIT Status register and the state of backplane pin GPIO5 (which can be used as BIT FAST_START) are mirrored into the CPU Power-on Configuration Word.

4.17.6 XMC_RESET_IN

The SBC314 asserts XMC RESET_IN when the backplane SYSRESET is asserted.

When configured to do so, the SBC314 asserts XMC RESET_IN when the GDiscrete1 backplane signal is asserted.

When configured to do so, the SBC314 asserts XMC RESET_IN when the VPX Maskable reset backplane signal is asserted.

4.17.7 External Interrupts

PCI Interrupts

Devices on the PCIe switch, and on the PMC/XMC, are connected via PCIe to the CPU, and have their interrupts connected to their respective PCIe-PCI bridges to convert them into PCIe messages. These are then passed to the interrupt controller in the CPU. The internal interrupt signals that are used for this purpose in the CPU are shared with external interrupt signals as shown in the following table. For this reason, these external interrupts are not used and are pulled high.

PCIe Switch Interrupts	External Interrupt Pin	PMC/XMC Interrupts	External Interrupt Pin
INT B	IRQ[1]	INT B	IRQ[5]
INT C	IRQ[2]	INT C	IRQ[6]
INT D	IRQ[3]	INT D	IRQ[7]

The INTA signals from the PCIe ports are routed as dedicated inputs to the Interrupt Controller and are not shared with external pins.

FPGA Interrupts

The FPGA connects to the IRQ[0] and IRQ[4] interrupt inputs to the CPU. These inputs are configured as active-low, level-sensitive. The FPGA registers provide the option to route the internal and external interrupt sources shown below to either of these interrupt inputs under software control via registers - see Section 5.43, "Interrupt Controller Registers".

The FPGA interrupt controller supports the following interrupt sources:

- Two interrupts from the GPIO controller
- An input from the GDiscrete1 VPX backplane signal
- A critical temperature interrupt from the temperature sensor
- A temperature interrupt from the temperature sensor
- An interrupt from the Real Time Clock
- An interrupt from each of the two Ethernet PHYs
- An interrupt from the central PCIe switch
- An interrupt from the Avionics Watchdog
- A single timer interrupt, which is a wired-OR combination of the interrupt requests from all of the FPGA Timer modules
- A single interrupt from the BMM communication UART

4.18 FPGA

A Lattice MachXO2 device connected to the CPU Local Bus provides the following functions, some of which are described more fully, below:

- Run-time variants
- Power sequencing
- Miscellaneous power control outputs
- Reset logic
- Configuration logic
- Local bus interface unit
- Control/status registers
- Interrupt controller
- GPIO module
- UART (BMM communication)
- Timers
- Avionics watchdogs
- I^2C slave interface (SPD emulation)
- In-field upgrade module
- Configuration memory error detection

4.18.1 Configuration Logic

The Configuration Logic is responsible for sampling the contents of the I^2C EEPROM DIP switch, and the SBC314X indicator, which control various run-time configuration options.

Host software is responsible for writing to the EEPROM DIP switch directly - the 'Main' I^2C bus is used for this. The new setting does not take effect until the next reset occurs.



LINK

The DIP switch configuration register layout is detailed in EEPROM DIP Switch Configuration Register 0 (0x6EA) and EEPROM DIP Switch Configuration Register 1 (0x6EB).

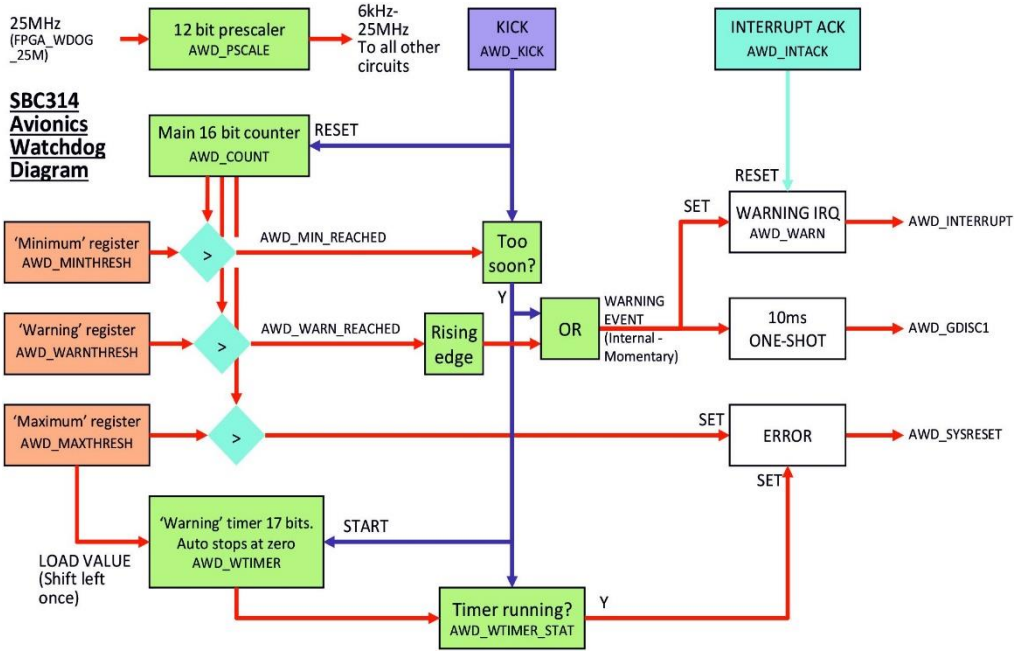
The Configuration Logic is also responsible for determining where the CPU should boot from, and for the non-volatile memory write-protection settings (see Section 4.5, "Non-volatile Memory").

4.18.2 GPIO Module

The GPIO module supports a total of eight GPIO signals, and is derived from the Abaco Haswell Common register set, with extensions to support redundant GPIOs and non-maskable interrupts.

The module outputs an interrupt to the FPGA interrupt controller when any of the GPIO interrupts are active and enabled. There are two interrupt outputs to the FPGA interrupt controller, allowing different GPIOs to be routed to different CPU interrupts. Detailed operation of the GPIO module is described in Section 5.15, "GPIO7:0 Registers".

4.18.3 Avionics Watchdog Timer



The Avionics Watchdog Timer circuit:

- runs from a 25 MHz master clock, and has a 12-bit software configurable prescaler, enabling the counter rate to run in the range ~6 kHz to 25 MHz
- has a resolution of 16 bits
- allows software to configure the parameters of Minimum Kick Interval, Kick Warning Time, and Maximum Kick Interval (expiration) time
- allows software to read its state and current count value
- supports time-out values between 0.1 ms and 5 s

The Avionics Watchdog, when configured to do so:

- sends an interrupt to the processor if no software Kick is received within the Kick Warning Time
- sets the backplane GDiscrete1 output if no software Kick is received within the Kick Warning Time
- resets the processor and all other SBC components if no software Kick is received within the Maximum Kick Interval
- asserts the backplane SYSRESET output if no software Kick is received within the Maximum Kick Interval
- sends a non-maskable interrupt to the processor if a software Kick is received before the Minimum Kick Interval
- sets the backplane GDiscrete1 output if a software Kick is received before the Minimum Kick Interval
- resets the processor and all other SBC components if a second Minimum Kick violation (software Kick received before Minimum Kick Interval) occurs within two Maximum Kick Intervals

- asserts the backplane SYSRESET output if a second Minimum Kick violation (software Kick received before Minimum Kick Interval) occurs within two Maximum Kick Intervals

The Avionics Watchdog Timer circuit is disabled at initial power up.

The Avionics Watchdog can be configured so that it cannot be disabled after it is started. This can also be dependent on the state of the GPIO4 backplane input.

Once enabled by software, the Avionics Watchdog Timer circuit prevents software from altering the Watchdog operating parameters.

Once configured by software, the Avionics Watchdog countdown and trip logic is completely independent of the SBC processor function - including the processor clock, clock crystal, and any distribution/divide-down circuitry.

It is possible for software to determine that a reset occurred due to an Avionics Watchdog expiry event.

See Section 5.53, "Avionics Watchdog Registers" for more details.

4.18.4 In-field Upgrade Module

The in-field upgrade module provides:

- A software interface to the Lattice Embedded Function Block (EFB). This allows software to reprogram the FPGA firmware. See Lattice Technical Notes TN1205 and TN1246
- An I^2C master interface that can be used to reprogram the main clock synthesizer firmware



NOTE

Contact Abaco for assistance in using either of these functions.

4.18.5 Configuration Memory Error Detection

The core of the Configuration Memory Error Detector is a Lattice 'SEDFA' primitive.

The error detector runs continuously while the P3V3_AUX rail is in spec. If the SEDFA detects an error, it will reload the FPGA causing the board to restart as if from a power up.

The error detector has a 'force error' input to allow testing of the error response behavior.



LINK

For more information, refer to the Lattice *MachXO2 SRAM SED Usage Guide*, Technical note TN1206.

4.19 AXIS Support

Also see the 3U VPX SBC Family manual.


LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

The SBC314 provides the required hardware support, using AUXCLK for the AXIS timer and the Maskable Reset for the legacy AXIS timer reset. For more details, see Section 5.13, "AXIS Registers".

4.20 Mezzanines

Also see the 3U VPX SBC Family manual.


LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

The SBC314 has one mezzanine site that supports both PMCs and XMCs.

4.20.1 PMCs

The site has J11, J12, J13, and J14 connectors. The interface is also 5V-tolerant and supports the use of 5V PMCs at 33 MHz signaling rate only.


CAUTION

Ensure that the 5V VIO is set correctly - see Section 4.15.4, "EEPROM DIP Switch".

The PCI bus is connected to a Pericom PI7C9X130 PCI-Express to PCI Bridge, which provides frequency negotiation, clocks and arbitration for the bus. The speed of the bus is based on the capability of the PMC, and is determined by the bridge during reset. The current operating frequency of the bus may be ascertained by reading registers within the bridge.

The PCI-X bus for the PMC site is implemented using a PCIe to PCI-X transparent bridge.

The PMC site supports Processor PMCs (as defined by VITA32-2002) operating in non-Monarch mode only. This includes support for PMCs with two PCI masters.

The PMC site has a dedicated PCI bus, so fitting a PMC that runs at a lower frequency does not limit the performance of other functions of the SBC314.

The presence of a PMC in the site is shown in a register - see XMC1/PMC1 I/O Configuration Register (0x6AF).

4.20.2 XMCs

The site also has J15 and J16 connectors. J15 provides a x4 PCIe link to the CPU. The XMC site fabric interface supports PCIe Gen 2 operating speed.

The System Management pins of the XMC site are connected to a dedicated I^2C interface on the BMM. The geographic address of the XMC site is configured to 000_b.

The presence of an XMC in the site is shown in a register - see XMC1/PMC1 I/O Configuration Register (0x6AF).

Fault Voltage Isolation

The signals on the XMC site I/O interface provide 100V fault voltage isolation to other signals. This is only supported by the special SBC314X variant that does not support PMC cards.



NOTE

The rating of the VPX backplane connector for normal operation is 50V AC. However, the connector manufacturer warrants that it will withstand 500V for 1 minute at sea level.

4.21 LEDs

LEDs are mounted on the back of the SBC314 to reflect the status of the following functions:

- Power Supplies
- BIT
- SATA activity
- Reset status
- Ethernet links
- PCIe links

The following diagram shows the positions of the LEDs.

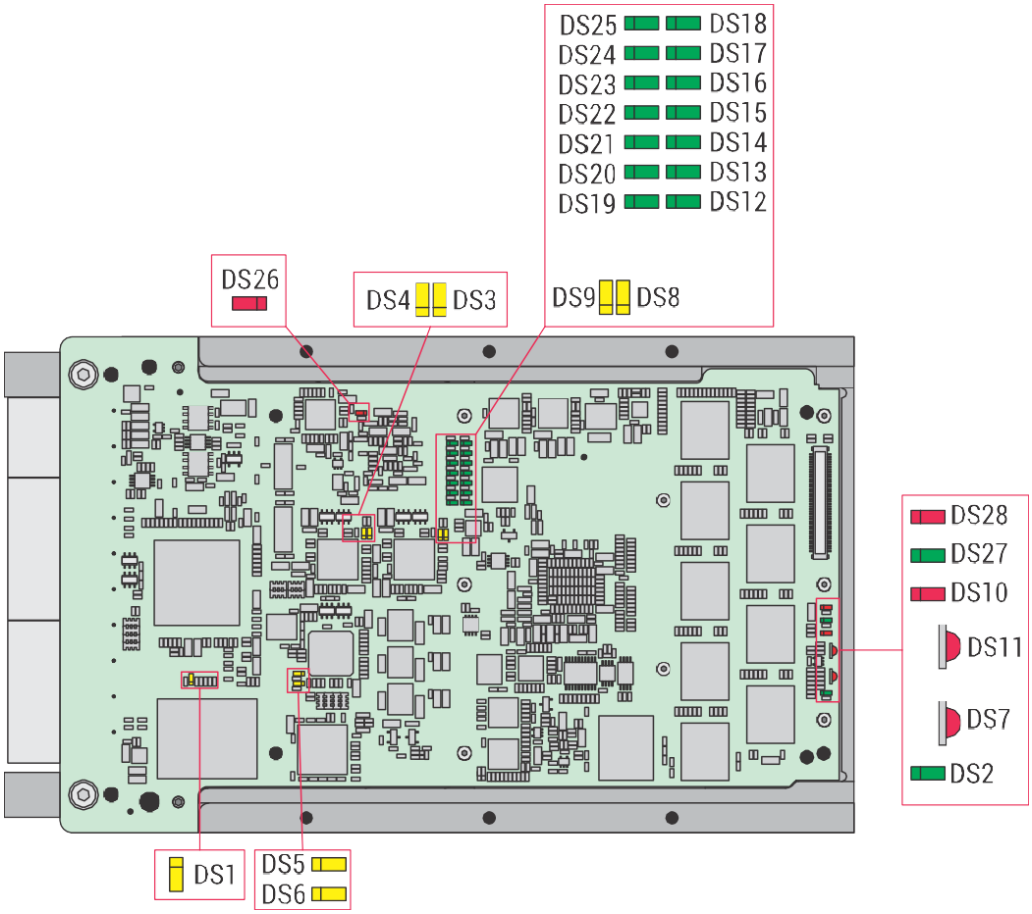


Table 4-6 LED Details

LED	Color	Default Function	Description
DS1	Yellow	SSD_LED_ACT_R	Onboard SSD activity
DS2	Green	BIT_PASS_LED	BIT pass
DS3	Yellow	ETH0_LED_ACT_L	Ethernet 0 Link/activity
DS4	Yellow	ETH0_LED_1000_L	Ethernet 0 1 Gbit/s mode
DS5	Yellow	ETH2_LED_ACT_L	Ethernet 2 Link/activity
DS6	Yellow	ETH2_LED_1000_L	Ethernet 2 1 Gbit/s mode
DS7	Red/ Blue/ Green	Red = LED_USER_4 Blue = LED_USER_5 Green = LED_USER_6	BIT status 2 (yellow)/User RGB 2
DS8	Yellow	ETH1_LED0	Ethernet 1 Link/activity
DS9	Yellow	ETH1_LED1	Ethernet 1 1 Gbit/s mode
DS10	Red	BMM_FAIL_LED_R	BIT fail
DS11	Red/ Blue/ Green	Red = LED_USER_1 Blue = LED_USER_2 Green = LED_USER_3	BIT status 1 (yellow)/User RGB 1
DS12	Green	PCIE_SW_LANE0_R	See Table 4-3
DS13	Green	PCIE_SW_LANE2_R	
DS14	Green	PCIE_SW_LANE4_R	
DS15	Green	PCIE_SW_LANE6_R	
DS16	Green	PCIE_SW_LANE8_R	
DS17	Green	PCIE_SW_LANE10_R	
DS18	Green	PCIE_SW_LANE13_R	
DS19	Green	PCIE_SW_LANE1_R	
DS20	Green	PCIE_SW_LANE3_R	
DS21	Green	PCIE_SW_LANE5_R	
DS22	Green	PCIE_SW_LANE7_R	
DS23	Green	PCIE_SW_LANE9_R	
DS24	Green	PCIE_SW_LANE11_R	
DS25	Green	PCIE_SW_LANE14_R	
DS26	Red	PCIE_SW_FATAL_ERR	PCIe switch fatal error
DS27	Green	POWER GOOD	All power good
DS28	Red	RESET LED	Board is in reset

4.21.1 Power Good LED (DS27)

This green LED is driven by the Power Manager. When on, it indicates that all on- and off-board power supplies are within their specified limits.

4.21.2 BIT LEDs (DS2, DS7, DS10 and DS11)

DS10 may be lit either by the BMM or under software control via a register - see LED Control Register (0x622). It is lit by default after reset. DS10 is powered from the auxiliary power supply, and so can be lit even when the main power supplies are not active or have failed. DS7 and DS11 are unlit after reset and are driven under software control from the LED Control Register.

When used by BIT, DS10 either indicates that BIT has not yet run (straight after a reset) or has run but failed. DS7 and DS11 show progress through BIT, and so may provide information for debugging purposes in the event of failure. DS2 shows that BIT has passed.

BIT Fail LED (DS10)	BIT Passed LED (DS2)	Status
On	Off	BIT not yet run (Reset state) or BIT failed
Off	On	BIT complete and passed

For more details on BIT usage, see the SBC314 BIT manual.


LINK

FBIT for SBC314 Software Reference Manual, publication number FBIT-SBC314-SRM

The BITFAIL~ signal on the P2 Connector is driven active low using an open- drain driver when the red BIT LED is lit.

4.21.3 Reset Status LED (DS28)

The main Board Reset signal drives this red LED to show that the board is in reset.

4.21.4 Ethernet PHY 1 Link Status LEDs (DS3 - DS6, DS8,DS9)

These yellow LEDs are controlled by PHY 1.

Function	LED ID	Description
ETH0 Activity	DS3	Ethernet port 0 activity off = no link on = link active flashing = activity
ETH1 Activity	DS8	Ethernet port 1 activity off = no link on = link active flashing = activity
ETH2 Activity	DS5	Ethernet port 2 activity off = no link on = link active flashing = activity
ETH0 Gigabit	DS4	Ethernet port 0 operating in 1000BASE-T mode
ETH1 Gigabit	DS9	Ethernet port 1 operating in 1000BASE-T mode
ETH2 Gigabit	DS6	Ethernet port 2 operating in 1000BASE-T mode

4.21.5 PCIe Switch Link Status LEDs (DS12 to DS26)

On- and off-board PCIe links have associated green LEDs, which are lit to indicate that the link is active, and flash to indicate the link speed.

Switch Lane	LED	Status
0	DS12	LED off = Lane is disabled LED on = Lane is enabled, 5.0 GT/s (Gen2) LED blinking, 0.5s on/off = Lane is enabled, 2.5 GT/s, reduced lanes are up (Gen1)
1	DS19	
2	DS13	
3	DS20	
4	DS14	
5	DS21	
6	DS15	
7	DS22	
8	DS16	
9	DS23	
10	DS17	
11	DS24	
13	DS18	
14	DS25	

Further information on the link status may be obtained by software reading the PCIe device registers.

4.21.6 4.21.6 SATA Activity LED

An LED on the onboard SATA SSD indicates SATA activity. There is no SATA LED on the controller.

4.22 JTAG

The SBC314 provides access to the processor COP interface via JTAG. The physical interface is via a proprietary Test Access Card (TAC), which is outside the normal mechanical envelope.

The CPU uses a dedicated JTAG chain from the TAC.

The SBC314 connects the backplane VPX JTAG interface (on P0 Connector) to the JTAG interfaces of the PMC and XMC sites.

The device order on the backplane VPX JTAG interface is:

- Backplane -> XMC site -> PMC site -> Backplane

The SBC314 provides a route-through circuit so that the backplane chain continues to work when one or other socket is not populated. If a socket is populated, then the mezzanine must either implement JTAG or loop the chain through, otherwise the other socket will not be reachable in the chain.

The SBC314 provides no terminations on the mezzanine chain, since no active circuits are connected

4.23 Front Panel

Also see the 3U VPX SBC Family manual and Section 2.3, "Mezzanine Installation".

LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

4.23.1 Air-cooled Versions (Build Levels 1 to 3)

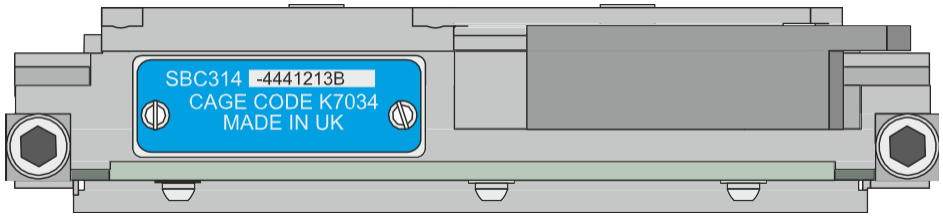


Mezzanine Card Slot

The SBC314 front panel has provision for front I/O from the mezzanine card.

If you are installing a non-Abaco mezzanine card, it must comply with the air-cooled mezzanine standard (IEEE 1386.1) to ensure that it mates correctly with the SBC314 mechanics.

4.23.2 Conduction-cooled Versions (Build Levels 4 and 5)



Mezzanine Card

If you are installing a non-Abaco mezzanine card, it must comply with the standard for rugged, conduction-cooled mezzanines (VITA20-2001) to ensure that it mates correctly with the SBC314 mechanics.

The SBC314 has different heatsinks depending on whether the XMC secondary thermal interface is included or not. This must be specified at the time of ordering

5 • FPGA Registers

5.1 Overview


LINK

The Offsets column provides links to the individual register descriptions.

Any offsets in the range 0x500 to 0x72F that do not have an entry in the following table are reserved.

Offsets	Registers	Access
0x500 to 0x5FF	In-Field Upgrade Module	
0x600	Board ID	R
0x601	Board Revision	R
0x60B	FPGA Revision	R
0x610 to 0x61A	Board ID String 1 to 11	R
0x61B	Reset Cause 1	R
0x61C	Reset Cause 2	R
0x620	BMM Control	RW
0x622	LED Control	RW
0x625	BIOS/SPI Control	RW
0x629	BIT Control and Status	RW
0x648	AXIS Timestamp 0	R
0x649	AXIS Timestamp 1	R
0x64A	AXIS Timestamp 2	R
0x64B	AXIS Timestamp 3	R
0x64C	AXIS Timestamp 4	R
0x64D	AXIS Timestamp 5	R
0x64E	AXIS Clock Frequency	R
0x64F	AXIS Clock Control	RW
0x650	Timer 0 Control and Status 1	RW
0x651	Timer 0 Control and Status 2	RW
0x652	Timer 0 IRQ Clear	W
0x654	Timer 0 Data Byte 0 (LS Byte)	RW
0x655	Timer 0 Data Byte 1	RW
0x656	Timer 0 Data Byte 2	RW
0x657	Timer 0 Data Byte 3 (MS Byte)	RW
0x658	Timer 1 Control and Status 1	RW
0x659	Timer 1 Control and Status 2	RW

Offsets	Registers	Access
0x65A	Timer 1 IRQ Clear	RW
0x65C	Timer 1 Data Byte 0 (LS Byte)	RW
0x65D	Timer 1 Data Byte 1	RW
0x65E	Timer 1 Data Byte 2	RW
0x65F	Timer 1 Data Byte 3 (MS Byte)	RW
0x660	Timer 2 Control and Status 1	RW
0x661	Timer 2 Control and Status 2	RW
0x662	Timer 2 IRQ Clear	RW
0x664	Timer 2 Data Byte 0 (LS Byte)	RW
0x665	Timer 2 Data Byte 1	RW
0x666	Timer 2 Data Byte 2	RW
0x667	Timer 2 Data Byte 3 (MS Byte)	RW
0x668	Timer 3 Control and Status 1	RW
0x669	Timer 3 Control and Status 2	RW
0x66A	Timer 3 IRQ Clear	RW
0x66C	Timer 3 Data Byte 0 (LS Byte)	RW
0x66D	Timer 3 Data Byte 1	RW
0x66E	Timer 3 Data Byte 2	RW
0x66F	Timer 3 Data Byte 3 (MS Byte)	RW
0x670	GPIO7:0 Out	RW
0x671	GPIO7:0 In	R
0x672	GPIO7:0 Direction	RW
0x673	GPIO7:0 Interrupt Enable	RW
0x674	GPIO7:0 Interrupt Level/Edge	RW
0x675	GPIO7:0 Interrupt High/Low	RW
0x676	GPIO7:0 Both Edges	RW
0x677	GPIO7:0 Interrupt Status	RW
0x678	GPIO7:0 Availability	R
0x679	GPIO7:0 Interrupt Select	RW
0x67A	GPIO7:0 Interrupt Non-Maskable	RW
0x67B	GPIO7:0 Test Mode	RW
0x684	GPIO15:08 Availability	R
0x688	GDiscrete1 Out	RW
0x689	GDiscrete1 In	R
0x68A	GDiscrete1 Direction	RW
0x68B	GDiscrete1 Interrupt Enable	RW
0x68C	GDiscrete1 Interrupt Level/Edge	RW

Offsets	Registers	Access
0x68D	GDiscrete1 Interrupt High/Low	RW
0x68E	GDiscrete1 Both Edges	RW
0x68F	GDiscrete1 Interrupt Status	RW
0x690	GDiscrete1 Availability	R
0x691	GDiscrete1 Interrupt Select	RW
0x692	GDiscrete1 Interrupt Non-Maskable	RW
0x693	GDiscrete1 Test Mode	RW
0x6A0	Ethernet Availability	R
0x6A1	COM Port Availability	R
0x6A2	COM Port 4-Wire Configuration	R
0x6A3	COM Port Modem Configuration	R
0x6A4	SATA Port Availability	R
0x6A5	USB2.0 Port 7:0 Availability	R
0x6A6	USB3.0 Port 7:0 Availability	R
0x6A7	USB2.0 Port 15:8 Availability	R
0x6A8	USB3.0 Port 15:8 Availability	R
0x6A9	Display Availability	R
0x6AA	VGA Display Availability	R
0x6AB	DVI/HDMI Display Availability	R
0x6AC	Display-Port Display Availability	R
0x6AD	Ancillary/Audio Availability	R
0x6AE	Front Panel Configuration	R
0x6AF	XMC1/PMC1 I/O Configuration	R
0x6B0	XMC2/PMC2 I/O Configuration	R
0x6B1	SSD Availability	R
0x6B2	SSD Secure Hardware Erase Capability	R
0x6BB	COM Port Enable	RW
0x6BC	COM Port Mode	RW
0x6BE	COM Port Loopback Enable	RW
0x6BF	SSD Erase Control	RW
0x6C0	SSD Cache Flush Control	RW
0x6C1	VPX Control	RW
0x6C2	Backplane Controls	RW
0x6C5	Fault Log Control	RW
0x6C6	Scratch Pad	RW
0x6C7	Test	RW
0x6C8	XMC1/PMC1 Status	R

Offsets	Registers	Access
0x6C9	XMC2/PMC2 Status	R
0x6CA	Backplane Status	R
0x6CB	SSD Status	R
0x6CC	Write-Protection Status	R
0x6CD	Jumper Link Status	R
0x6CE	Boot Location Status	R
0x6D0	Thermal Status	R
0x6D1	Alarm Status	R
0x6E0	Interrupt Status (Low)	R
0x6E1	Interrupt Status (High)	R
0x6E2	Interrupt Enable (Low)	RW
0x6E3	Interrupt Enable Main (High)	RW
0x6E4	Interrupt Select (Low)	RW
0x6E5	Interrupt Select (High)	RW
0x6E6	Interrupt Non-Maskable (Low)	RW
0x6E7	Interrupt Non-Maskable (High)	RW
0x6E8	Availability/Configuration	R
0x6E9	Reset Control	RW
0x6EA	EEPROM DIP Switch Configuration 0	R
0x6EB	EEPROM DIP Switch Configuration 1	R
0x6EC	Configuration Unlock Password	W
0x6ED	Control	RW
0x6EE	Scratch Pad 2	RW
0x6EF	LED Control 2	RW
0x6F0 to 0x6F7	Flash Password	R
0x700	Avionics Watchdog Configuration	RW
0x701	Avionics Watchdog Prescaler (Low Byte)	RW
0x702	Avionics Watchdog Enable	RW
0x703	Avionics Watchdog Status	R
0x704	Avionics Watchdog Kick	W
0x705	Avionics Watchdog Interrupt Acknowledge	W
0x706	Avionics Watchdog Main Counter Low Byte	R
0x707	Avionics Watchdog Main Counter High Byte	R
0x708	Avionics Watchdog Warning Timer Bits 8:1	R
0x709	Avionics Watchdog Warning Timer Bits 16:9	R
0x70A	Avionics Watchdog Minimum Threshold Low Byte	RW
0x70B	Avionics Watchdog Minimum Threshold High Byte	RW

Offsets	Registers	Access
0x70C	Avionics Watchdog Warning Threshold Low Byte	RW
0x70D	Avionics Watchdog Warning Threshold High Byte	RW
0x70E	Avionics Watchdog Maximum Threshold Low Byte	RW
0x70F	Avionics Watchdog Maximum Threshold High Byte	RW
0x720 to 0x72F	Scratchpad Memory	RW
0x0 to 0x7	BMM UART	RW

Where: RW = Read/Write, R = Read only, W = Write only.



NOTE

All entries in this section use the little-endian numbering convention - i.e., in 8-bit registers, bit 7 is the MSB and bit 0 is the LSB.

5.2 In-Field Upgrade Module Registers (0x500 to 0x5FF)

This register space is used to access the In-Field Upgrade Module - see Section 4.18.4, "In-field Upgrade Module" for details.

5.3 Board ID Register (0x600)

0x82 = SBC314
0x83 = SBC314X



NOTE

The SBC314X does not provide PMC support. Software should not attempt to access PMC components (e.g., the PCIe/PCI-X bridge).

5.4 Board Revision Register (0x601)

Bits	Description	Notes
7 to 4	Major assembly revision (board artwork)	0x1 = Rev 1, 0x2 = Rev 2, etc.
3 to 0	Minor revision (hardware build state revision)	0x0 = Rev A (default), 0x1 = Rev B, etc.

5.5 FPGA Revision Register (0x60B)

This holds the revision of the FPGA code, where:

0x1 = Rev 1
0x2 = Rev2
etc.

5.6 Board ID String Registers 1 to 11 (0x610 to 0x61A)

These read back ASCII values for “SBC314” or “SBC314X”, depending on the PCB variant that the FPGA detects. Offset 0x610 holds the first character and offset 0x61A holds the last character.

NOTE

Code should be written to read bytes until the first NULL is encountered *or* the last byte (0x61A) is reached.

5.7 Reset Cause Register 1 (0x61B)

For the non-reserved bits:

1 = The last reset was caused by the named event
0 = The last reset was not caused by the named event.

Bits	Reset Cause
7	A power failure
6	Requested by XMC1 (XMC1_RESET_OUT_L)
5	Reserved
4	Requested by VPX Maskable Reset input (MSKRST_L)
3	Software requested (BIT_HRESET is set in the BIT Control and Status Register)
2 to 0	Reserved

If no bits are set in either this or the Reset Cause Register 2, then the reset was caused by a power failure.

5.8 Reset Cause Register 2 (0x61C)

Bits	Reset Cause
7	Requested by VPX backplane (VPX_SYSRESET_L)
6	Requested by CPU (CPU_RESET_REQ_L)
5	Requested by Avionics Watchdog (AWD_SYSRESET)
4	Requested by legacy Watchdog. NOTE This will never be set as the legacy Watchdog is not implemented
3	Requested by debugger HRESET (BDM_HRESET_L)
2	Requested by PCIe Switch NT bridge (PCIE_NT_RESET_L)
1	Requested by BMM (BMM_RESET_OUT_L)
0	Requested by debugger SRESET (BDM_SRESET_L)

5.9 BMM Control Register (0x620)

Bit	Description
7	BIT Fail LED output enable. This allows the FPGA to control the BIT Fail LED (see the LED Control Register). The BMM normally controls the BIT Fail LED - only set this bit if the BMM is not populated. 1 = Enable BIT Fail LED output from FPGA 0 = Disable BIT Fail LED output from FPGA (default)
6	Reserved. Reads as 0_b
5	BMM serial port mode. This value is driven out unaltered to the BMM_SERIAL_MODE output pin: 1 = BMM Serial port disabled 0 = BMM Serial port enabled (normal operation) (default)
4	BMM_PGD (program data = BIT Fail LED) pin output enable: 1 = Enable output to BMM_PGD pin 0 = Disable output to BMM_PGD pin (default)
3	Connected directly to the BMM VPP pin. It defaults to 1
2	Connected directly to the BMM PGC (clock) pin. It defaults to 1
1	Connected directly to the BMM PGM (program enable) pin. It defaults to 0
0	BMM PGD pin (= BIT Fail LED) output value - see also bit 4. This reads back the actual pin value regardless of the setting of bit 4. It defaults to 0

5.10 LED Control Register (0x622)

Bits	Description
7	BIT Pass LED: 1 = LED lit 0 = LED not lit (default) (This bit is sticky on BIT_HRESET or CPU_RESET_REQ_L)
6	BIT Fail LED: 1 = LED lit 0 = LED not lit (default) The BIT Fail LED is normally controlled via the BMM. This bit is ignored if bit 7 of the BMM Control Register is zero. (This bit is sticky on BIT_HRESET or CPU_RESET_REQ_L)
5	BIT Status 1 LED (yellow): 1 = LED lit 0 = LED not lit (default) (This bit is sticky on BIT_HRESET or CPU_RESET_REQ_L)
4	BIT Status 2 LED (yellow): 1 = LED lit 0 = LED not lit (default) (This bit is sticky on BIT_HRESET or CPU_RESET_REQ_L)
3 to 0	Reserved. Read as 0x0

5.11 BIOS/SPI Control Register (0x625)

Bits	Description
7	Select alternate boot area: 1 = Select alternate boot area 0 = Select normal boot area (default) (This bit is sticky except on power failure) See boot area selection in Configuration Logic
6	Select recovery boot area (SPI Flash): 1 = Select recovery boot area (SPI) 0 = Select normal boot area (default) (This bit is sticky except on power failure) See boot area selection in Configuration Logic This bit takes precedence over bit 7
5	Override Boot Source jumper links (boot from the source specified by bits 7 and 6) 1 = Use bits 7 and 6 0 = Use jumper links/EEPROM DIP switch (default) (This bit is sticky except on power failure) See boot area selection in Configuration Logic
4 to 0	Reserved. Read as $0\ 0000_b$

5.12 BIT Control/Status Register (0x629)

Apart from bits 7 and 1, this register has no effect within the FPGA; it is provided solely for BIT software to store its context.

Bits	Description
7	BIT_HRESET[a] request: 1 = Board reset requested 0 = Board reset not requested (default) This bit clears itself after the reset occurs
6 and 5	BIT Run Status: 00 = BIT not previously run (default) 01 = Fast BIT performed 10 = Full BIT performed 11 = Fast Start performed (This bit is sticky unless the reset cause is a power failure)
4	BIT Pass/Fail: 1 = BIT failed (default) 0 = BIT passed (This bit is sticky unless the reset cause is a power failure)
3	Fast BIT: 1 = Fast BIT enabled (via a BIOS setting) 0 = Fast BIT disabled (default) (This bit is sticky unless the reset cause is a power failure)
2	Fast Start: 1 = Fast Start enabled (via a BIOS setting) 0 = Fast Start disabled (default) (This bit is sticky unless the reset cause is a power failure)
1	Controls whether BIT_HRESET request also causes SYSRESET: 1 = BIT_HRESET request also causes a SYSRESET output 0 = BIT_HRESET request does not cause a SYSRESET output (default) This is independent of whether the board is System Controller. By itself, this bit does not generate a reset of any kind (BIT_HRESET has that function)
0	BIT run: 1 = BIT has been run 0 = BIT not been run (default) (This bit is sticky unless reset cause is a power failure)

[a] The name _HRESET is retained from the common Haswell register set, although in fact this generates a PORESET in Freescale terminology.

5.13 AXIS Registers

5.13.1 AXIS Timestamp Register 0 (0x648)

This returns bits 7 to 0 of the AXIS timestamp value.



NOTE

Read this byte first, as the act of reading this register latches the current timestamp value into registers 1 to 5.

5.13.2 AXIS Timestamp Register 1 (0x649)

This returns bits 15 to 8 of the AXIS timestamp value.

5.13.3 AXIS Timestamp Register 2 (0x64A)

This returns bits 23 to 16 of the AXIS timestamp value.

5.13.4 AXIS Timestamp Register 3 (0x64B)

This returns bits 31 to 24 of the AXIS timestamp value.

5.13.5 AXIS Timestamp Register 4 (0x64C)

This returns bits 39 to 32 of the AXIS timestamp value.

5.13.6 AXIS Timestamp Register 5 (0x64D)

This returns bits 47 to 40 of the AXIS timestamp value.

5.13.7 AXIS Clock Frequency Register (0x64E)

This returns the AXIS Master clock period in nanoseconds. When the SBC314 is AXIS clock master, the frequency is 25 MHz (40 ns).



NOTE

Do not use this register when the SBC314 is AXIS clock slave - the frequency cannot be determined in this case.

Software may use this register to determine if the AXIS timer is implemented - it returns zero if there is no AXIS timer.

5.13.8 AXIS Clock Control Register (0x64F)

Bits	Description
7	AXIS clock output enable[a]: 1 = The SBC314 drives a 25 MHz output onto the VPX AUXCLK pair 0 = The SBC314 does not drive the VPX AUXCLK pair This bit is sticky (except for power failure), so that the clock output continues through a reset. The reset value of this signal is 1 when the board is System Controller, 0 otherwise
6	AXIS reset output[b]: 1 = The SBC314 drives the Maskable Reset backplane signal low. 0 = The SBC314 does not drive the Maskable Reset backplane pin (high Z) (default)
5	AXIS reset input enable.Use of Maskable Reset for the AXIS timer reset is optional. If not used, the AXIS timer will reset from either power up or SYSRESET: 1 = The AXIS timer is reset when Maskable Reset is asserted (low) (default) 0 = The AXIS timer is *not* reset by Maskable Reset
4 to 0	Reserved. Read as $0\ 0000_b$

As the SBC314 uses AUXCLK for the AXIS timer, this bit is the same as bit 1 in the Backplane Controls Register (0x6C2). For maximum software compatibility, it can be accessed in either place, although only one physical signal exists.
As the SBC314 uses Maskable Reset for the AXIS timer reset, this bit is the same as bit 3 of the VPX Control Register (0x6C1). For maximum software compatibility, it can be accessed in either place, although only one physical signal exists.

5.14 Timer Registers

5.14.1 Timer 0 Control and Status Register 1 (0x650), Timer 1 Control and Status Register 1 (0x658), Timer 2 Control and Status Register 1 (0x660) & Timer 3 Control and Status Register 1 (0x668)

Bits	Description
7	Timer IRQ status: 1 = Pending 0 = No interrupt
6	Reserved. Reads as 0_b
5 and 4	Clock source select: 00 = Use 2 MHz FPGA clock[a] (default) 01 = Use 25 MHz (Watchdog clock source) 10 = Use CPU IFC bus clock 11 = Reserved
3	Timer Read selection: 1 = Read Timer Load value 0 = Read current time value (default)
2 and 1	Clock divider (when the 2 MHz clock is used): 00 = 1:1 (2 MHz) (default) 01 = 1:2 (1 MHz) 10 = 1:4 (500 kHz) 11 = 1:8 (250 kHz)
0	Enable Timer IRQ: 1 = IRQ enabled 0= IRQ masked (default)

a.This has a poor frequency tolerance, since it does not use a crystal source.

5.14.2 Timer 0 Control and Status Register 2 (0x651), Timer 1 Control and Status Register 2 (0x659), Timer 2 Control and Status Register 2 (0x661) & Timer 3 Control and Status Register 2 (0x669)

Bits	Description
7 to 5	Reserved. Read as 000_b
4	Timer read latch select: 1 = Latch all timers on read of Timer 0 LS Byte 0 = Latch individual timers on the read of individual Timer LS Byte (default) NOTE Setting this bit in *any* Timer Control and Status Register 2 has the same effect of latching *all* timers on a read of the Timer 0 LS Byte
3 and 2	Reserved. Read as 00_b
1	Timer One-shot Enable: 1=Timer will count down and stop 0=Timer will count down and reload at terminal count (default)
0	Timer Enable: 1=Timer enabled 0 = Timer disabled (default)

5.14.3 Timer 0 IRQ Clear Register (0x652), Timer 1 IRQ Clear Register (0x65A), Timer 2 IRQ Clear Register (0x662) and Timer 3 IRQ Clear Register (0x66A)

Any write to this register clears the timer IRQ.

5.14.4 Timer 0 Data Byte 0 to 3 Registers (0x654 to 0x657)

Reads

The value read is either the current timer value or the timer load value, depending on bit 3 of the Timer 0 Control and Status Register 1 (T0C&SR1[3]):

Offset	Register Name	Value if T0C&SR1[3] = 0	Value if T0C&SR1[3] = 0	Timer Bits
0x654	Timer 0 Data Byte 0 (least significant byte)	Current timer (default 0x00)	Timer load (default 0xFF)	7 to 0
0x655	Timer 0 Data Byte 1	Current timer (default 0x00)	Timer load (default 0xFF)	8 to 15
0x656	Timer 0 Data Byte 2	Current timer (default 0x00)	Timer load (default 0xFF)	16 to 23
0x657	Timer 0 Data Byte 3 (most significant byte)	Current timer (default 0x00)	Timer load (default 0xFF)	42 to 31

Reading byte 0 latches the upper bits of the timer value to prevent rollover.

Writes

Writes always update the timer load value, irrespective of the setting of bit 3 of the Timer 0 Control and Status Register 1.

Offset	Register Name	Timer Bits
0x654	Timer 0 Data Byte 0 (least significant byte)	7 to 0
0x655	Timer 0 Data Byte 1	8 to 15
0x656	Timer 0 Data Byte 2	16 to 23
0x657	Timer 0 Data Byte 3 (most significant byte)	42 to 31

Writing to byte 3 causes the timer immediately to reload the complete 32-bit load value.

5.14.5 Timer 1 Data Byte 0 to 3 Registers (0x65C to 0x65F)

Functionality is as per Timer 0.

Offset	Register Name	Timer Bits
0x65C	Timer 1 Data Byte 0 (least significant byte)	7 to 0
0x65D	Timer 1 Data Byte 1	8 to 15
0x65E	Timer 1 Data Byte 2	16 to 23
0x65F	Timer 1 Data Byte 3 (most significant byte)	42 to 31

The value read depends on bit 3 of the Timer 1 Control and Status Register 1.

5.14.6 Timer 2 Data Byte 0 to 3 Registers (0x664 to 0x667)

Functionality is as per Timer 0.

Offset	Register Name	Timer Bits
0x664	Timer 2 Data Byte 0 (least significant byte)	7 to 0
0x665	Timer 2 Data Byte 1	8 to 15
0x666	Timer 2 Data Byte 2	16 to 23
0x667	Timer 2 Data Byte 3 (most significant byte)	42 to 31

The value read depends on bit 3 of the Timer 2 Control and Status Register 1.

5.14.7 Timer 3 Data Byte 0 to 3 Registers (0x66C to 0x66F)

Functionality is as per Timer 0.

Offset	Register Name	Timer Bits
0x66C	Timer 3 Data Byte 0 (least significant byte)	7 to 0
0x66D	Timer 3 Data Byte 1	8 to 15
0x66E	Timer 3 Data Byte 2	16 to 23
0x66F	Timer 3 Data Byte 3 (most significant byte)	42 to 31

The value read depends on bit 3 of the Timer 3 Control and Status Register 1.

5.15 GPIO7:0 Registers

In the following descriptions, bits 7 to 0 of each register map to GPIO pins 7 to 0 respectively.

5.15.1 GPIO7:0 Out Register (0x670)

The value of the bit in this register is driven onto the appropriate GPIO pin when the corresponding direction is set to output. The default is 0x00.

5.15.2 GPIO7:0 In Register (0x671)

The value of the bit in this register returns the status of the appropriate GPIO pin, regardless of the corresponding direction. The default is 0x00.

5.15.3 GPIO7:0 Direction Register (0x672)

For each GPIO:

1 = Output
0 = Input (default)

5.15.4 GPIO7:0 Interrupt Enable Register (0x673)

For each GPIO:

1 = Interrupt enabled
0 = Interrupt masked (default)

If any GPIO interrupt is configured as non-maskable (see GPIO7:0 Interrupt Non-Maskable Register (0x67A)) and enabled, then no further changes to any settings that affect that GPIO can be made (except for GPIO7:0 Test Mode Register (0x67B) and GPIO7:0 Out Register (0x670)).

5.15.5 GPIO7:0 Interrupt Level/Edge Register (0x674)

For each GPIO:

1 = Edge
0 = Level (default)

5.15.6 GPIO7:0 Interrupt High/Low Register (0x675)

For GPIOs configured as 'standard' signals, this register sets the interrupt detection sensitivity of each interrupt pin (active high/low or rising/falling edge depending on the level/edge mode):

1 = Active high/rising edge
0 = Active low/falling edge (default)

If the GPIO7:0 Availability Register indicates that a GPIO is not available, the corresponding bit in this register becomes read-only and indicates whether it is a redundant GPIO:

1 = Redundant GPIO
0 = GPIO not implemented

See Section 4.13.1, "Redundant GPIO" for more details.

5.15.7 GPIO7:0 Both Edges Register (0x676)

For each GPIO:

1 = Both-edges mode enabled
0 = Both-edges mode disabled (default)

When enabled, Both-edges mode causes interrupts to be generated on both rising and falling edges.


NOTE

The GPIO bit must be in Edge mode for Both-edges mode to work.

5.15.8 GPIO7:0 Interrupt Status Register (0x677)

For each GPIO:

1 = Interrupt pending
0 = No interrupt (default)

Write a '1' to a bit to clear the interrupt pending status.

5.15.9 GPIO7:0 Availability Register (0x678)

For each GPIO:

1 = GPIO available
0 = GPIO not available

This register allows software to easily determine which of the GPIO7:0 signals are available on the SBC314. All GPIO signals use shared backplane pins and are only available when the SBC314 is configured with the appropriate build option.

If this register indicates that the GPIO is not available, then the GPIO7:0 Interrupt High/Low Register indicates whether it is a redundant GPIO.

5.15.10 GPIO7:0 Interrupt Select Register (0x679)

For each GPIO:

1 = Interrupt routed to secondary GPIO interrupt output
0 = Interrupt routed to main GPIO interrupt output (default).

5.15.11 GPIO7:0 Interrupt Non-Maskable Register (0x67A)

For each GPIO:

1 = GPIO interrupt is non-maskable
0 = GPIO interrupt is maskable (default)

Once a GPIO interrupt has been set as non-maskable in this register, it cannot be set to maskable again until after the next reset has occurred.

5.15.12 GPIO7:0 Test Mode Register (0x67B)

For each GPIO:

1 = GPIO in test mode (input circuits receive the value in GPIO7:0 Out Register (0x670))
0 = GPIO not in test mode (input circuits receive the pin value) (default).

5.16 GPIO15:8 Availability Register (0x684)

This register returns zero to indicate that GPIO15:8 are never available on the SBC314.

5.17 GDiscrete1 Registers

There is one VPX GDISC1 pin, which is always present on the P1 Connector pin G1. There is no 'redundant' pin, but there is a redundant copy of the signal in the FPGA for test purposes.

The GDiscrete1 registers work similarly to the GPIO registers, except that open- drain behavior is enforced (i.e., output driving high is disallowed; if programmed this way, the output is tri-stated).

In each register, bit 7 applies to the GDISC1 pin and bit 3 applies to the redundant copy of the signal. The other bits have no function and are fixed at zero.

5.17.1 GDiscrete1 Out Register (0x688)

The value of the bit in this register is driven onto the GDISC1 signal when the corresponding direction is set to output. The default is 0x00.

5.17.2 GDiscrete1 In Register (0x689)

The value of the bit in this register returns the status of the GDISC1 pin, regardless of the corresponding direction. The default is 0x00.

5.17.3 GDiscrete1 Direction Register (0x68A)

1 = Output
0 = Input (default)

5.17.4 GDiscrete1 Interrupt Enable Register (0x68B)

1 = Interrupt enabled
0 = Interrupt masked (default)

If the GDiscrete1 interrupt is configured as non-maskable (see Section 5.17.11) and enabled, then no further changes to any settings that affects GDiscrete1 can be made (except for GDiscrete1 Test Mode and GDiscrete1 Out).

5.17.5 GDiscrete1 Interrupt Level/Edge Register (0x68C)

1 = Edge
0 = Level (default)

5.17.6 GDiscrete1 Interrupt High/Low Register (0x68D)

Bit 7 of this register sets the interrupt detection sensitivity of the interrupt pin (active high/low or rising/falling edge depending on the level/edge mode):

1 = Active high/rising edge
0 = Active low/falling edge (default)

5.17.7 GDiscrete1 Both Edges Register (0x68E)

1 = Both-edges mode enabled
0 = Both-edges mode disabled (default)

When enabled, Both-edges mode causes interrupts to be generated on both rising and falling edges.



NOTE

The GDiscrete1 bit must be in Edge mode for Both-edges mode to work.

5.17.8 GDiscrete1 Interrupt Status Register (0x68F)

1 = Interrupt pending
0 = No interrupt (default)

Write a '1' to a bit to clear the interrupt pending status.

5.17.9 GDiscrete1 Availability Register (0x690)

The GDISC1 pin is always available (bit 7 is set to '1').

5.17.10 GDiscrete1 Interrupt Select Register (0x691)

0 = Interrupt routed to GDiscrete1 interrupt output (default).

(Unlike the GPIOs, there is only one interrupt output, as there is only one signal.)

5.17.11 GDiscrete1 Interrupt Non-Maskable Register (0x692)

1 = GDiscrete1 interrupt is non-maskable
0 = GDiscrete1 interrupt is maskable (default)

Once the GDiscrete1 interrupt has been set as non-maskable in this register, it cannot be set to maskable again until after the next reset has occurred.

5.17.12 GDiscrete1 Test Mode Register (0x693)

1 = GDiscrete1 in test mode (input circuits receive the value in GDiscrete1 Out Register)
0 = GDiscrete1 not in test mode (input circuits receive the pin value) (default).

5.18 Availability Registers

These show whether a feature is available on the SBC314. See Chapter 4, "Functional Description" for complete details.



NOTE

Even when a feature is marked as unavailable in these registers, the device may still be visible to software, but may not be routed to backplane pins.

5.18.1 Ethernet Availability Register (0x6A0)

Bits	Description
7 to 3	Ethernet ports 7:3 are not available: 0 = Ethernet port is not available
2	Ethernet port 2 availability depends on build options: 0 = Ethernet port is not available 1 = Ethernet port is available
1	Ethernet port 1 is always available: 1 = Ethernet port is available
0	Ethernet port 0 is always available: 1 = Ethernet port is available

5.18.2 COM Port Availability Register (0x6A1)

Bits	Description
7 to 2	COM ports 8:3 are not available: 0 =COM port is not available
1	COM port 2 is always available: 1 = COM port is available
0	COM port 1 is always available: 1 = COM port is available

5.18.3 COM Port 4-wire Configuration Register (0x6A2)



NOTE

The CPU UARTs can be configured as either 2x4 wire or 4x2 wire in the CPU's RCW. The FPGA always reports the COM ports as 2x4 wire because it may not have access to the RCW. Software should refer to the RCW contents to determine the final COM port configuration.

Bits	Description
7 to 2	COM ports 8:3 are not available
1	COM port 2 always supports 4-wire mode: 1 = COM port is available in 4-wire (RS-232 or RS-422) mode
0	COM port 1 always supports 4-wire mode: 1 = COM port is available in 4-wire (RS-232 or RS-422) mode

5.18.4 COM Port Modem Configuration Register (0x6A3)

Full modem lines are not supported on the SBC314:

Bits	Description
7 to 0	COM ports 8:1 modem configuration: 0 =Full modem line support is not available

5.18.5 SATA Port Availability Register (0x6A4)

The value returned by a read depends on the SBC314 variant, i.e., the value at V in the product code SBC314-xxxxxVxx. See Section A.6, "Product Codes".

Variant	SATA Ports Available[a]	Register Value
1 or A	0	0x0
2 or B	2 (ports 0 and 1)	0x1
3 or C	1 (port 0 only)	0x3
4 or D	1 (port 0 only)	0x3

a.SATA ports 2 to 7 are never available.

5.18.6 USB2.0 Ports 7:0 Availability Register (0x6A5)

Bits	Description
7 to 2	USB2.0 ports 7:2 are not available: 0 = USB2.0 port is not available
1	USB2.0 port 1 is always available: 1 = USB2.0 port is available
0	USB2.0 port 0 is always available: 1 = USB2.0 port is available

5.18.7 USB3.0 Ports 7:0 Availability Register (0x6A6)

USB3.0 ports 7:0 are not available on the SBC314:

Bits	Description
7 to 0	USB3.0 ports 7:0 availability: 0 = USB3.0 port is not available

5.18.8 USB2.0 Ports 15:8 Availability Register (0x6A7)

USB2.0 ports 15:8 are not available on the SBC314:

Bits	Description
7 to 0	USB2.0 ports 15:8 availability: 0 = USB2.0 port is not available

5.18.9 USB3.0 Ports 15:8 Availability Register (0x6A8)

USB3.0 ports 15:8 are not available on the SBC314:

Bits	Description
7 to 0	USB3.0 ports 15:8 availability: 0 = USB3.0 port is not available

5.18.10 Display Availability Register (0x6A9)

No displays are available on the SBC314:

Bits	Description
7 to 0	Display 7:0 availability: 0 = Display is not available

5.18.11 VGA Display Availability Register (0x6AA)

No VGA displays are available on the SBC314:

Bits	Description
7 to 0	Display 7:0 VGA availability: 0 = Display is not VGA

5.18.12 DVI/HDMI Display Availability Register (0x6AB)

No DVI/HDMI displays are available on the SBC314:

Bits	Description
7 to 0	DVI/HDMI Display 7:0 availability: 0 = Display type is not DVI/HDMI

5.18.13 Display-Port Display Availability Register (0x6AC)

No Display-Port displays are available on the SBC314:

Bits	Description
7 to 0	Display 7:0 Display-Port availability: 0 = Display is not Display-Port type

5.18.14 Ancillary/Audio Availability Register (0x6AD)

None of the features in this register are available on the SBC314:

Bits	Description
7	Front panel I/O availability: 0 = Front panel I/O is not available
6 and 5	Reserved. Read as 00b
4	COM port 4 presence on front panel: 0 = COM port 4 not present
3	COM port 3 presence on front panel: 0 = COM port 3 not present
2	COM port 2 presence on front panel: 0 = COM port 2 not present
1	COM port 1 presence on front panel: 0 = COM port 1 not present
0	Audio availability: 0 = Audio is not available

5.19 Front Panel Configuration Register (0x6AE)

No front panel I/O is available on the SBC314

Bit	Description
7	Ethernet port 1 presence on front panel: 0 = Ethernet port 1 not present
6	SATA port 1 presence on front panel: 0 = SATA port 1 not present
5	USB2.0 port 1 presence on front panel: 0 = USB2.0 port 1 not present
4	Video port 1 presence on front panel: 0 = Video port 1 not present
3	Ethernet port 0 presence on front panel: 0 = Ethernet port 0 not present

Bit	Description
2	SATA port 0 presence on front panel: 0 = SATA port 0 not present
1	USB2.0 port 0 presence on front panel: 0 = USB2.0 port 0 present
0	Video port 0 presence on front panel: 0 = Video port 0 not present

5.20 XMC1/PMC1 I/O Configuration Register (0x6AF)

On the SBC314, PMC1 I/O is fully P64 compliant (not a subset). On the SBC314X variant, PMC1 is not implemented.


NOTE

On the SBC314, XMC1 I/O is X12d/X8d/X24s compliant.

Bits	Description
7	P64s compliant configuration: 1 = I/O is P64 compliant
6	Reduced P64s configuration: 0 = I/O is not a subset of P64
5 and 4	Reserved. Read as 00_b
3	XMC X12d configuration: 1 = I/O is X12d compliant
2	XMC X8d configuration: 1 = I/O is X8d compliant
1	XMC X24s configuration: 1 = I/O is X24s compliant
0	XMC X38s configuration: 0 = I/O is not X38s compliant

5.21 XMC2/PMC2 I/O Configuration Register (0x6B0)

There is no PMC2/XMC2 site on the SBC314.

5.22 SSD Availability Register (0x6B1)

If installed, the SSD is numbered SSD0. However, it is physically connected to port 1 of the SATA controller.

Bits	Description
7 to 0	SSD7:0 availability: 1 = SSD available 0 = SSD not available

5.23 SSD Secure Hardware Erase Capability Register (0x6B2)

When Hardware Secure Erase is available, triggering a hardware erase function will result in a secure erase algorithm being executed.

NOTE

Hardware Secure Erase is not currently available, but may be in the future.

Bits	Description
7 to 0	SSD7:0 Hardware Secure Erase capability: 0 = Hardware Secure Erase not available (default) 1 = Hardware Secure Erase available

5.24 COM Port Enable Register (0x6BB)

Bits	Description
7 to 2	COM ports 8:3 are not available
1	COM2 enable: On the SBC314, the transceivers for *both* COM1 and COM2 are enabled by the COM1 control; the COM2 control is ignored
0	COM1 (and COM2) enable: 1 = COM port transceivers enabled 0 = COM port transceivers disabled (default) Software should set this bit to a '1' after the desired COM Port Mode (i.e., RS-232/RS-422) is set

5.25 COM Port Mode Register (0x6BC)

Bits	Description
7 to 2	COM ports 8:3 are not available
1	COM2 mode: 1 = COM port transceiver in RS-422 mode 0 = COM port transceiver in RS-232 mode
0	COM1 mode: 1 = COM port transceiver in RS-422 mode 0 = COM Port transceiver in RS-232 mode

5.26 COM Port Loopback Enable Register (0x6BE)

Test software can use loopback mode to test the basic functionality of the transceiver.

Bits	Description
7 to 2	COM ports 8:3 are not available
1	COM2 loopback enable: On the SBC314, loopback mode for *both* COM1 and COM2 is enabled by the COM1 control; the COM2 control is ignored
0	COM1 (and COM2) loopback enable: 1 = COM port transceiver loopback mode enabled 0 = COM port transceiver loopback mode disabled (normal operation) (default)

5.27 SSD Erase Control Register (0x6BF)

To trigger a hardware erase, software must write to a bit with a “1”,”0”,”1” pattern on consecutive write cycles to this register. This is to protect against ‘accidental’ erase functions. The value read from this register represents the state of the output and not the last value written.

Bits	Description
7 to 0	SSD7:0 Hardware erase: 1 = Hardware Erase pin active 0 = Hardware Erase pin negated (default)

5.28 SSD Cache Flush Control Register (0x6C0)

The bits in this register directly control the Cache Flush pin of the corresponding SSD device.

Bits	Description
7 to 0	SSD7:0 Cache Flush: 1 = Cache Flush pin active 0 = Cache Flush pin negated (default)

5.29 VPX Control Register (0x6C1)

Bits	Description
7 to 5	Reserved. Read as 000_b
4	VPX Maskable Reset mask: 1 = The SBC314 will reset when it sees an active low signal on the Maskable Reset backplane pin 0 = The SBC314 will *not* reset when it sees an active low signal on the Maskable Reset backplane pin (default)
3	VPX Maskable Reset out:[a] 1 = The SBC314 drives the Maskable Reset backplane signal low 0 = The SBC314 does not drive the Maskable Reset backplane pin (High Z) (default)
2	NVMRO override:

Bits	Description
	1 = The SBC314 drives NVMRO backplane signal low 0 = The SBC314 does not drive the NVMRO backplane signal. (High Z) (default) NOTES This bit can only be set when the SBC314 is the VPX System Controller (the VPX_SYSCON pin is set low). This bit cannot be set if the SPARE_LOCAL input is low (configured for avionics application)
1 and 0	Reserved. Read as 00_b

a.As the SBC314 uses Maskable Reset for the AXIS timer reset, this bit is the same as bit 6 of the AXIS Clock Control Register (0x64F). For maximum software compatibility, it can be accessed in either place, although only one physical signal exists.

5.30 Backplane Controls Register (0x6C2)

Bits	Description
7 to 2	Reserved. Read as 0000 00_b
1	VPX AUXCLK output enable[a]: 1 = The SBC314 drives a 25 MHz output onto the VPX AUXCLK pair 0 = The SBC314 does not drive the VPX AUXCLK pair (default) This bit is sticky (except for power failure), so that the clock output continues through a reset. The reset value of this signal is 1 when the board is System Controller, 0 otherwise
0	VPX REFCLK output enable: 1 = The SBC314 drives a 100 MHz PCIe reference clock output onto the VPX REFCLK pair 0 = The SBC314 does not drive the VPX REFCLK pair. The reset value of this bit is 1 when the SBC314 is System Controller or 0 otherwise

a.As the SBC314 uses AUXCLK for the AXIS timer, this bit is the same as bit 7 of the AXIS Clock Control Register (0x64F). For maximum software compatibility, it can be accessed in either place, although only one physical signal exists.

5.31 Fault Log Control Register (0x6C5)

This determines whether the fault log is triggered by various (power) events:

Bits	Description
7 to 4	Reserved. Read as 0x0
3	Fault log ignore BMM 1 = Fault log is *not* triggered by a BMM power-down request 0 = Fault log *is* triggered by a BMM power-down request
2	Fault log ignore 5V 1 = Fault log is *not* triggered by backplane 5V going down 0 = Fault log *is* triggered by backplane 5V going down
1	Fault log ignore 1 = Fault log is *not* triggered by backplane 3.3V going down 0 = Fault log *is* triggered by backplane 3.3V going down
0	Fault log ignore 1 = Fault log is *not* triggered by backplane 3.3V_AUX going down 0 = Fault log *is* triggered by backplane 3.3V_AUX going down

5.32 Scratch Pad Register (0x6C6)

This is a generic read/write register available to software to validate FPGA access. It is sticky when reset using BIT_HRESET or CPU_RESET_REQ_L. On the SBC314, this register is driven out in the CPU POR_CFG word during Power-On/ Reset.

The pin status of the backplane bit GPIO5 is driven out as bit 7 of the CPU POR_CFG word. In some applications, this is used as a BIT Fast Start indicator.

7	6	5	4	3	2	1	0
GPIO5	Bits 6 to 0 of Scratch Pad Register						

5.33 Test Register (0x6C7)

Bits	Description
7 and 6	Reserved. Read as 00_b
5	Trigger the clock synthesizer programmer to execute a program cycle to the clock synthesizer. Write the sequence '1', '0', '0', '1' using consecutive writes to start the cycle. This will cause a board reset
4	Test input to FPGA configuration memory error detector: 1 = Force error detector to flag an error at the end of the current cycle 0 = Do not force error (default) Setting this bit will cause the FPGA to reload, and the SBC314 will reset
3	CPU I^2C bus 2 to Sensor bus buffer enable: 1 = CPU I^2C bus 2 connected to Sensor bus 0 = CPU I^2C bus 2 isolated from Sensor bus (default) This permits the CPU to access the I^2C Sensor bus directly. It should only be enabled when the BMM is inactive, or not fitted. It is sticky when reset using BIT_HRESET or CPU_RESET_REQ_L

Bits	Description
2	Disable the PCIe switch EEPROM: 1 = Disable the PCIe switch auto-loading from its EEPROM 0 = Enable the PCIe switch EEPROM (default) Software can use this to prevent the PCIe switch from loading the configuration table stored in its private EEPROM. It is sticky when reset using BIT_HRESET or CPU_RESET_REQ_L
1 and 0	Mezzanine site override: 11 = Force PMC site 10 = Force XMC site 0x = Enable auto detection (default) Test software can use this to override the automatic mezzanine detection logic. It is sticky when reset using BIT_HRESET or CPU_RESET_REQ_L

5.34 PMC1/XMC1 Status Register (0x6C8)

Bit	Description
7	XMC1 presence: 1 = XMC1 is fitted 0 = XMC1 is not fitted
6	XMC1 VPWR voltage. On the SBC314, the XMC VPWR rail is always 5V. 0 = XMC1 VPWR rail is 5V (default)
5	XMC1 BIST status: 1 = XMC1 BIST is active 0 = XMC1 BIST is not active
4	XMC1 Reset Out (MRSTO) status: 1 = XMC1 Reset Out is active 0 = XMC1 Reset Out is not active In the default state, MRSTO always causes the SBC314 to reset. This behavior can be disabled in the Reset Control Register
3	Reserved. Reads as 0_b
2	PMC1 enumeration-ready status: 1 =PMC1 ERDY pin is active (OK to enumerate) 0 =PMC1 ERDY pin is not active
1	PMC1 VIO voltage: 1 = PMC1 VIO voltage = 5V 0 = PMC1 VIO voltage = 3.3V On the SBC314, the PMC VIO voltage is configured using a bit in the EEPROM DIP switch
0	PMC1 presence 1 = PMC1 is fitted 0 = PMC1 is not fitted

5.35 PMC2/XMC2 Status Register (0x6C9)

There is no PMC2/XMC2 site on the SBC314.

5.36 Backplane Status Register (0x6CA)

Bits	Description
7	SYSCON status: 1 = SBC314 is fitted in the System Controller slot (VPX_SYSCON_L input is low) 0 = SBC314 is not fitted in the System Controller slot
6	NVMRO status: 1 = Backplane VPX_NVMRO signal is asserted 0 = Backplane VPX_NVMRO signal is not asserted
5	VPX_GAP (Geographic Address Parity) pin status. This bit reads the state of the VPX GA parity pin. It is *not* inverted
4 to 0	VPX_GA4:0 (Geographic Address) status (inverted): 1 = GA pin pulled low 0 = GA pin not pulled low The GA bits are inverted here so that the host software can read a true slot number

5.37 SSD Status Register (0x6CB)

Bits	Description
7 to 0	SSD7:0 Write-Protect Status: 1 = SSD is write-protected 0 = SSD is not write-protected

5.38 Write-Protection Status Register (0x6CC)

Bit	Description
7	PCIe switch configuration EEPROM write- protection status: 1 = Hardware write-protection is active 0 = Hardware write-protection is not active
6	Ethernet 2 NIC configuration Flash write-protection status: 1 = Hardware write-protection is active 0 = Hardware write-protection is not active
5	SPD EEPROM Flash write-protection status: 1 = Hardware write-protection is active 0 = Hardware write-protection is not active On the SBC314, the SPD data is embedded within the FPGA configuration data. It is therefore always write-protected (except when updating the FPGA data)
4	FPGA configuration data write-protection status: 1 = Hardware write-protection is active 0 = Hardware write-protection is not active See Section 4.18.4, "In-field Upgrade Module" for details
3	Main NOR Flash write-protection status: 1 = Hardware write-protection is active (default) 0 = Hardware write-protection is not active The main NOR Flash write-protection relies mainly on software sector locking - see Spansion data for details. This bit is writable, unlike other bits in this register. NOR Flash protection must be explicitly removed by writing a zero here
2	Recovery SPI Flash write-protection status: 1 = Hardware write-protection is active 0 = Hardware write-protection is not active

Bit	Description
1	NVRAM write-protection status: 1 = Hardware write-protection is active 0 = Hardware write-protection is not active
0	EEPROM DIP switch write-protection status: 1 = Hardware write-protection is active 0 = Hardware write-protection is not active

5.39 Jumper Status Register (0x6CD)

The bits in this register reflect *only* the state of the physical jumpers. Other related functions, e.g., use of GPIO pins to duplicate these jumpers, are specified and reported elsewhere.

Bit	Description
7	NVRAM write-enable jumper (P5 pins 5 and 6): 1 = Jumper is installed 0 = Jumper is not installed
6	Boot Recovery jumper (P5 pins 3 and 4): 1 = Jumper is installed 0 = Jumper is not installed
5	Configuration memory write-enable jumper (P5 pins 9 and 10): 1 = Jumper is installed 0 = Jumper is not installed
4	Boot Alternate jumper (P5 pins 1 and 2): 1 = Jumper is installed 0 = Jumper is not installed
3	Boot Test Card jumper: 1 = Jumper is installed 0 = Jumper is not installed
2	BANC write-enable jumper: 1 = Jumper is installed 0 = Jumper is not installed
1	Test card jumper: 1 = Test card is installed 0 = Test card is not installed
0	Flash password unlock jumper (P5 pins 7 and 8): 1 = Jumper is installed 0 = Jumper is not installed

5.40 Boot Location Status Register (0x6CE)

Bits	Description
7	Reserved for auto-swap failover. Reads as 0_b The SBC314 does not support auto-swap failover
6 and 5	Active boot ROM location 11 = SBC314 booted from the test card (Abaco only) 10 = SBC314 booted from Alternate area (NOR Flash) 01 = SBC314 booted from Recovery area (SPI) 00 = SBC314 booted from Main area (NOR Flash) (default)
4	SPD location. The SBC314 always boots using the onboard SPD EEPROM: 0 = SBC314 booted using onboard SPD EEPROM (default)
3	Ethernet configuration ROM location. The SBC314 always boots using the onboard Ethernet configuration ROM. 0 = SBC314 booted using onboard Ethernet Configuration ROM (default)
2	Reserved. Reads as 0_b
1 and 0	RCW location: 1x = SBC314 booted using RCW in I^2C EEPROM 01 = SBC314 booted using RCW B in FPGA (overlaid over NOR Flash Chip Select 0) 00 = SBC314 booted using RCW A in FPGA (overlaid over NOR Flash Chip Select 0) (default) NOTE If the SBC314 booted from an SPI Flash (either Recovery or TAC), then the RCW is always loaded from that SPI Flash, and these bits must be ignored

5.41 Thermal Status Register (0x6D0)

Bits	Description
7	Reserved. Reads as 0_b
6	Thermal sensor THERM status: 1 = Thermal sensor THERM output is asserted 0 = Thermal sensor THERM output is not asserted (default)
5	Thermal sensor ALERT status: 1 = Thermal sensor ALERT output is asserted 0 = Thermal sensor ALERT output is not asserted (default)
4 to 0	Reserved. Read as 00000_b

5.42 Alarm Status Register (0x6D1)

Bits	Description
7 to 4	Reserved. Read as 0x0
3	Non-correctable ECC error in SPD ROM 1 = Non-correctable ECC error was detected in SPD ROM 0 = No non-correctable ECC error was detected in SPD ROM (default)
2	Correctable ECC error in SPD ROM 1 = Correctable ECC error was detected in SPD ROM 0 = No correctable ECC error was detected in SPD ROM (default)
1	Non-correctable ECC error in RCW ROM 1 = Non-correctable ECC error was detected in RCW ROM 0 = No non-correctable ECC error was detected in RCW ROM (default)
0	Correctable ECC error in RCW ROM 1 = Correctable ECC error was detected in RCW ROM 0 = No correctable ECC error was detected in RCW ROM (default)

5.43 Interrupt Controller Registers

In the following registers, the mapping of bits in the "(Low)" registers to interrupt sources is as follows:

Bit	Interrupt Source
7	Ethernet 1 PHY
6	Ethernet 0 PHY
5	Real Time Clock
4	Thermal Sensor Alert/Therm2
3	Thermal Sensor Critical
2	GDiscrete1
1	GPIO (secondary)
0	GPIO (main)

The mapping of bits in the "(High)" registers to interrupt sources is as follows:

Bits	Description/Interrupt Source
7 to 4	Reserved. Read as 0x0
3	BMM UART
2	(Any) Timer
1	Avionics Watchdog
0	PCIe switch



NOTE

If any interrupt is configured as non-maskable and is enabled, then no further changes to the FPGA interrupt controller registers for that interrupt can be made.

5.43.1 Interrupt Status (Low) Register (0x6E0)

For all bits in this register:

1 = An interrupt from this source is active.
0 = No interrupt from this source is active (default).

5.43.2 Interrupt Status (High) Register (0x6E1)

For interrupt bits in this register:

1 = An interrupt from this source is active.
0 = No interrupt from this source is active (default).

5.43.3 Interrupt Enable (Low) Register (0x6E2)

All bits in this register are active high:

1 = The interrupt source is enabled for output.
0 = The interrupt source is disabled for output (default).

5.43.4 Interrupt Enable Main (High) Register (0x6E3)

All interrupt bits in this register are active high:

1 = The interrupt source is enabled for output.
0 = The interrupt source is disabled for output (default).

5.43.5 Interrupt Select (Low) Register (0x6E4)

For all bits in this register:

1 = The interrupt source is routed to the secondary interrupt output (INT4).
0 = The interrupt source is routed to the primary interrupt output (INT0) (default).

5.43.6 Interrupt Select (High) Register (0x6E5)

For interrupt bits in this register:

1 = The interrupt source is routed to the secondary interrupt output (INT4).
0 = The interrupt source is routed to the primary interrupt output (INT0) (default).

5.43.7 Interrupt Non-Maskable (Low) Register (0x6E6)

All bits in this register are active high:

1 = The interrupt source is configured as non-maskable.
0 = The interrupt source configured as maskable (default).



NOTE

Once any bit in this register has been set, it cannot be cleared again until after the next reset has occurred.

5.43.8 Interrupt Non-Maskable (High) Register (0x6E7)

All interrupt bits in this register are active high:

1 = The interrupt source is configured as non-maskable.
0 = The interrupt source configured as maskable (default).


NOTE

Once any interrupt bit in this register has been set, it cannot be cleared again until after the next reset has occurred.

5.44 Availability/Configuration Register (0x6E8)

Bits	Description
7 to 5	Reserved. Read as 000b
4	Reports the status of the STACKED_FLASH_FITTED_L build variant input: 1 = Stacked Flash (S70) is installed 0 = Normal Flash (S29) is installed
3	Reports the status of the SPARE_LOCAL built variant input: 1 = SPARE_LOCAL built variant installed 0 = SPARE_LOCAL built variant not installed SPARE_LOCAL is used to engage various FPGA behaviors for a specific avionics application
2	Reports the status of the NOR Flash chip Ready/Busy pin See the Spansion NOR Flash data sheet for details of how to use this bit
1	SBC310 mode build variant indicator: 1 = SBC310 compatible pinout 0 = Not SBC310 compatible pinout The SBC310 compatible pinout uses the VPX Maskable Reset backplane pin for a serial port signal, so Maskable Reset features are not available on this variant
0	Ethernet mode build variant indicator: 1 = ETH0 and ETH1 are configured in 1000BASE-X mode 0 = ETH0 and ETH1 are configured in 1000BASE-T mode

5.45 Reset Control Register (0x6E9)

Bit	Description
7	Disable reset request from XMC reset output: 1 = Assertion of XMC reset out is ignored 0 = Assertion of XMC reset out causes the SBC314 to reset (default)
6	Reserved. Reads as 0_b
5	Forward a VPX Maskable Reset to the XMC reset input control: 1 = Assert a reset to the XMC site when the MSKRST input is asserted 0 = Do not assert a reset to the XMC site when the MSKRST input is asserted (default) If bit 4 in the VPX Control Register is set, then any MSKRST input will reset the whole SBC314, including the XMC site
4	Forward GDiscrete1 fault to XMC reset input control: 1 = Assert a reset to the XMC site when a GDiscrete1 input fault is detected (a mismatch between the main input signal and the redundant copy) 0 = Do not assert a reset to the XMC site when a GDiscrete1 input fault is detected (default)
3	Forward GDiscrete1 to the XMC reset input control: 1 = Assert a reset to the XMC site when the GDiscrete1 input is asserted 0 = Do not assert a reset to the XMC site when the GDiscrete1 input is asserted (default)
2	XMC reset control: 1 = Assert a reset to the XMC site 0 = Do not assert a reset to the XMC site (default) This allows software to unconditionally reset the XMC site
1	Accept a reset request from the PCIe Switch NT reset output: 1 = Assertion of a PCIe switch NT reset causes the SBC314 to reset 0 = Assertion of a PCIe switch NT reset is ignored (default)
0	PCIe Switch Reset: 1 = Assert a hard reset to the PCIe switch 0 = Do not assert a hard reset to the PCIe switch (default) This control allows software to reset the PCIe switch

5.46 EEPROM DIP Switch Configuration Register 0 (0x6EA)

This register returns the state of the EEPROM DIP Switch Register 0 when the SBC314 was last reset. Only 6 bits are implemented.

Bits	Description
7 and 6	Reserved. Read as 00_b
5	Load RCW from EEPROM: 1 = Load RCW from I^2C EEPROM 0 = Load RCW from main ROM/FPGA - see Section 4.18.1, "Configuration Logic"
4	RCW selection - see Section 4.18.1, "Configuration Logic": 1 = Use RCW B 0 = Use RCW A
3	Write-protect SSD: 1 = Write-protect SSD 0 = Do not write-protect SSD
2 to 0	XMC geographic address: For XMC deployments, this is connected directly to the XMC, not used by the FPGA For PMC deployments, this controls the PMC VIO voltage: 101_b = VIO is 5V Others = VIO is 3V3


LINK

See Appendix C, "FPGA ROM Contents" for RCW details.

5.47 EEPROM DIP Switch Configuration Register 1 (0x6EB)

This register returns the state of the EEPROM DIP Switch Register 1 when the SBC314 was last reset. Only 6 bits are implemented.

Bits	Description
7 and 6	Reserved. Read as 00_b
5	NVRAM write-protect: 1 = Write-protect NVRAM 0 = Do not write-protect NVRAM
4	Boot site swap (NOR Flash only) 1 = Swap Alternate/Main boot areas 0 = Do not swap Alternate/Main boot areas
3	GPIO7 alternate function: 1 = GPIO7 (active high) duplicates function of Boot Recovery link 0 = No special function
2	GPIO6 alternate function: 1 = GPIO6 (active high) duplicates function of Boot Alternate link 0 = No special function
1	GPIO5 alternate function: 1 = GPIO5 (active high) duplicates function of Flash Password link 0 = No special function
0	GPIO4 alternate function: 1 = GPIO4 special function enabled (reserved for future use) 0 = No special function The Avionics Watchdog uses GPIO4 for a special function - this is enabled by software directly in the Watchdog, not by this configuration bit. See Section 4.16.2, "Avionics Watchdog Timer"

5.48 Configuration Unlock Password Register (0x6EC)

Software uses this register to write configuration memory unlock passwords, to unlock various configuration memories without fitting links. Contact Abaco for full details.

5.49 Control Register (0x6ED)

Bits	Description
7 to 2	Reserved. Read as 0000 00_b
1	SATA port 1 output multiplex control: 1 = SATA port 1 routed to onboard SSD 0 = SATA port 1 routed to VPX backplane (default)
0	CPU Fuse programming supply enable: 1 = Enable fuse programming supply 0 = Disable fuse programming supply (default) See Freescale documentation for details of programming the security fuses

5.50 Scratch Pad Register 2 (0x6EE)

This is a general-purpose read/write register available to application software. It is not used within the FPGA. It is only reset by a power cycle, and defaults to 0x00.

5.51 LED Control Register 2 (0x6EF)

Bit	Description
7	LED 2 tri-color mode: 1 = LED 2 in RGB mode - controlled by other bits in this register 0 = LED 2 in legacy BIT (yellow) mode - controlled by the BIT Status 2 LED bit in the LED Control Register (default)
6	LED 2 red segment control: 1 = Red segment switched on 0 = Red segment switched off (default)
5	LED 2 green segment control: 1 = Green segment switched on 0 = Green segment switched off (default)
4	LED 2 blue segment control: 1 = Blue segment switched on 0 = Blue segment switched off (default)
3	LED 1 tri-color mode: 1 = LED 1 in RGB mode - controlled by other bits in this register 0 = LED 1 in legacy BIT (yellow) mode - controlled by the BIT Status 1 LED bit in the LED Control Register (default)
2	LED 1 red segment control: 1 = Red segment switched on 0 = Red segment switched off (default)
1	LED 1 green segment control: 1 = Green segment switched on 0 = Green segment switched off (default)
0	LED 1 blue segment control: 1 = Blue segment switched on 0 = Blue segment switched off (default)

5.52 Flash Password Registers (0x6F0 to 0x6F7)

This block of 8 bytes provides the NOR Flash password to host software. See the Write-Protection description in Section 4.5.1, "NOR Flash" for full details.

5.53 Avionics Watchdog Registers

5.53.1 Avionics Watchdog Configuration Register (0x700)

This register is locked while the watchdog is running (bit 0 of the Avionics Watchdog Enable Register is set).

Bits	Description
7 and 6	Reserved. Read as 00_b
5 and 4	Interlock configuration: 11 = Reserved 10 = Once enabled, the Watchdog can never be disabled 01 = Once enabled, the Watchdog can only be disabled when GPIO4 is high (default)[a] 00 = The Watchdog can be disabled without restriction
3 and 2	Reserved. Read as 00_b
1	Warning GDiscrete1 assertion: 1 = Warning assertion asserts GDiscrete1 (default) 0 = Warning assertion does not assert GDiscrete1
0	Reserved. Reads as 0_b

a.For certain customer configurations, the polarity of the GPIO4 Watchdog interlock defeat input is inverted. For setting '01', the Watchdog can only be disabled when GPIO4 is low.

5.53.2 Avionics Watchdog Prescaler (Low Byte) Register (0x701)

Together with bit 7:4 of the Avionics Watchdog Enable Register, this determines the 12-bit division ratio used to generate the counting rate of the Watchdog. On the SBC314, the input clock is 25 MHz. Program the desired division ratio minus 1, e.g.,

0x000 => 25 MHz
0x001 => 12.5 MHz
0x063 (99_D) => 250 kHz
0x9C3 (2499_D) => 10 kHz
0xFFF (4095_D) => 6.1 kHz (approximately)

The default is 0x063 (250 kHz).

This register is locked while the Watchdog is running (bit 0 of the Avionics Watchdog Enable Register is set).

5.53.3 Avionics Watchdog Enable Register (0x702)

Bits 7:4 in this register are locked while the Watchdog is running (bit 0 is set). Bit 0 in this register is locked according to bit 5 in the Avionics Watchdog Configuration Register.

Bits	Description
7 to 4	4 MSBs of the prescaler - see the Avionics Watchdog Prescaler (Low Byte) Register. The default is 0x0
3 to 1	Reserved. Read as 000_b
0	Watchdog enable: 1 = Watchdog enabled 0 = Watchdog disabled (default) Ensure the Watchdog is fully configured before enabling it

5.53.4 Avionics Watchdog Status Register (0x703)

Bits	Description
7 to 4	Reserved. Reads as 0x0
3	Warning timer status: 1 = Warning timer running (one 'minimum' kick violation detected) 0 = Warning timer not running (no 'minimum' kick violation has occurred in the last two 'maximum' periods) (default)
2	Warning interrupt output status: 1 = Warning interrupt is being asserted 0 = Warning interrupt is not being asserted (default)
1	Warning count reached: 1 = Main counter has reached the warning threshold 0 = Main counter has not reached the warning threshold (default)
0	Minimum count reached: 1 = Main counter has reached the minimum threshold 0 = Main counter has not reached the minimum threshold (default)

5.53.5 Avionics Watchdog Kick Register (0x704)

Any write to this register kicks the Watchdog.

5.53.6 Avionics Watchdog Interrupt Acknowledge Register (0x705)

Any write to this register acknowledges the Watchdog warning interrupt.

5.53.7 Avionics Watchdog Main Counter Low Byte Register (0x706)

This register returns the value of the low byte of the main counter, and latches the current value of the high byte for reading later.

5.53.8 Avionics Watchdog Main Counter High Byte Register (0x707)

This register returns the value of the high byte of the main counter at the instant when the main counter low byte register was last read.



NOTE

Software must read the *low* byte and then the *high* byte in that order.

5.53.9 Avionics Watchdog Warning Timer Bits 8:1 Register (0x708)

This register returns the value of bits 8:1 of the 17-bit warning timer, and latches the current value of bits 16:9 for reading later.

Bit 0 of the 17-bit warning timer cannot be read.

5.53.10 Avionics Watchdog Warning Timer Bits 16:9 Register (0x709)

This register returns the value of bits 16:9 of the 17-bit warning timer at the instant when the warning timer low byte register was last read.



NOTE

Software must read the *low* register and then the *high* register in that order.

The Warning Timer Status bit in the Avionics Watchdog Status Register indicates whether this timer is running.



NOTE

The warning timer is a down counter. It may be treated as a 16-bit timer counting at half the rate of the main counter.

5.53.11 Avionics Watchdog Minimum Threshold Low Byte Register (0x70A)

This register holds the low byte of the 16-bit minimum threshold value. It defaults to 0x00. Configure this register before enabling the Watchdog. It is locked while the Watchdog is running (bit 0 of the Avionics Watchdog Enable Register is set).

5.53.12 Avionics Watchdog Minimum Threshold High Byte Register (0x70B)

This register holds the high byte of the 16-bit minimum threshold value. It defaults to 0x00. Configure this register before enabling the Watchdog. It is locked while the Watchdog is running (bit 0 of the Avionics Watchdog Enable Register is set).

5.53.13 Avionics Watchdog Warning Threshold Low Byte Register (0x70C)

This register holds the low byte of the 16-bit warning threshold value. It defaults to 0x00. Configure this register before enabling the Watchdog.

If this register is updated while the Watchdog is running, no warning will be generated until after the next kick has occurred.

5.53.14 Avionics Watchdog Warning Threshold High Byte Register (0x70D)

This register holds the high byte of the 16-bit warning threshold value. It defaults to 0x00. Configure this register before enabling the Watchdog.

If this register is updated while the Watchdog is running, no warning will be generated until after the next kick has occurred.

5.53.15 Avionics Watchdog Maximum Threshold Low Byte Register (0x70E)

This register holds the low byte of the 16-bit maximum threshold value. It defaults to 0x00. Configure this register before enabling the Watchdog. It is locked while the Watchdog is running (bit 0 of the Avionics Watchdog Enable Register is set).

5.53.16 Avionics Watchdog Maximum Threshold High Byte Register (0x70F)

This register holds the high byte of the 16-bit maximum threshold value. It defaults to 0x00. Configure this register before enabling the Watchdog. It is locked while the Watchdog is running (bit 0 of the Avionics Watchdog Enable Register is set).

5.54 Scratchpad Memory Registers (0x720 to 0x72F)

This is a 16-byte scratchpad memory area that is available for application software. It is not used within the FPGA. It is not cleared or modified by any reset condition, and so the contents will be undefined at powerup.

5.55 BMM UART Registers (0x0 to 0x7)

The UART is accessed by a dedicated chip select, so its base address is software-configurable. It is functionally equivalent to an industry standard 16550 UART.

The input clock to the UART baud rate divider is the CPU IFC (local bus) clock. This is software-configurable, but is typically 50 MHz.

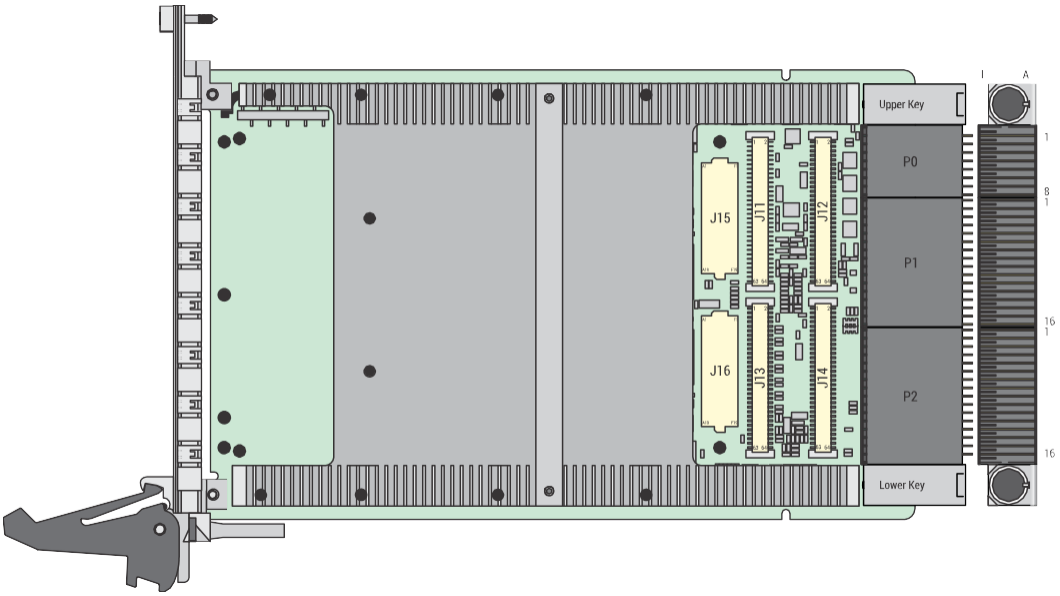
See the Lattice “Reference Design RD1042” documentation for register details

6 • Connectors

Table 6-1 Connector Functions

Connector	Function	Connector	Function
P0, P1, P2	VPX interface	J15, J16	XMC Site 1
J11, J12, J13, J14	PMC Site 1	P4 (rear of PCB)	Test Access Card

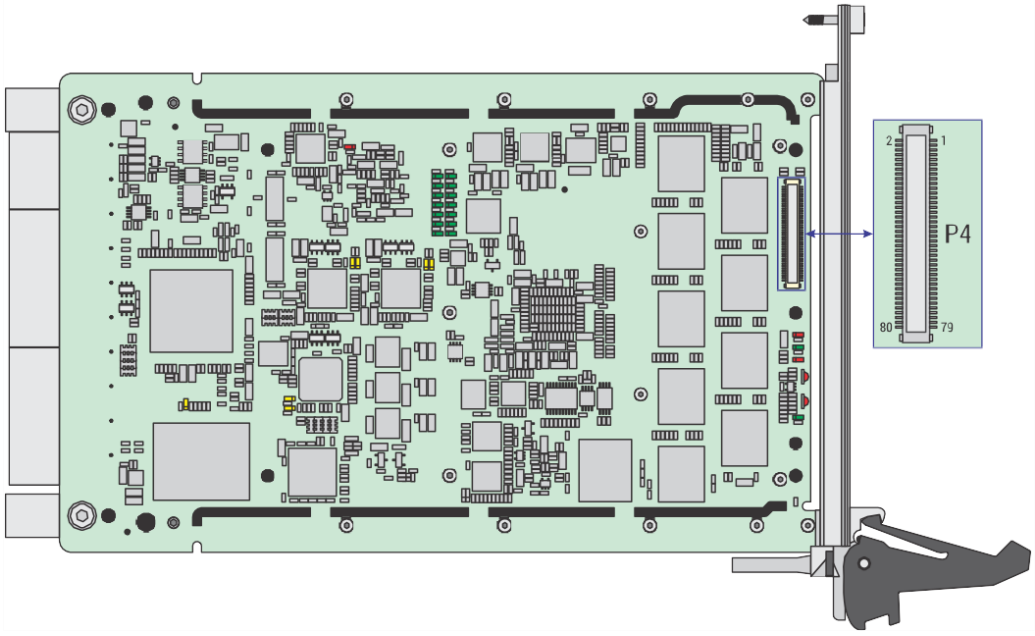
Figure 6-1 Connector Positions (Top)



NOTE

The SBC314's guide pin receptacles are unkeyed by default, but may be keyed to customer requirements. Contact Abaco for more details.

Figure 6-2 Connector Positions (Back)



6.1 Backplane Connectors

The pin assignments of the SBC314 VPX backplane connectors (P0 to P2) are shown in the 7-row format as used in the VPX specifications.



NOTE

Direction of fabrics is shown such that TX is an output from the SBC314 and RX is an input to the SBC314.

6.1.1 P0 Connector

Connector type Tyco TE-2102772-2-P0.

Pin	A	B	C	D	E	F	G
1	VS2	VS2	VS2	N/C	VS1 (N/C)	VS1 (N/C)	VS1 (N/C)
2	VS2	VS2	VS2	N/C	VS1 (N/C)	VS1 (N/C)	VS1 (N/C)
3	VS3	VS3	VS3	N/C	VS3	VS3	VS3
4	NVMRO	SYSRESET~	GND	N12V_AUX	GND	N/C	N/C
5	SM_DATA	SM_CLK	GND	P3V3_AUX	GND	GA4~	GAP~
6	GA0~	GA1~	GND	P12V_AUX	GND	GA2~	GA3~
7	TRST~	TMS	GND	TDI	TDO	GND	TCK
8	GND	AUXCLK_P	AUXCLK_N	GND	REFCLK_P	REFCLK_N	GND

6.1.2 P1 Connector

Connector type Tyco TE-2102771-2-P1.

Pin	A	B	C	D	E	F	G
1	PCIE_A_L0_RXP	PCIE_A_L0_RXN	GND	PCIE_A_L0_TXP	PCIE_A_L0_TXN	GND	GDISC1
2	GND	PCIE_A_L1_RXP	PCIE_A_L1_RXN	GND	PCIE_A_L1_TXP	PCIE_A_L1_TXN	GND
3	PCIE_A_L2_RXP	PCIE_A_L2_RXN	GND	PCIE_A_L2_TXP	PCIE_A_L2_TXN	GND	VBAT
4	GND	PCIE_A_L3_RXP	PCIE_A_L3_RXN	GND	PCIE_A_L3_TXP	PCIE_A_L3_TXN	GND
5	PCIE_B_L0_RXP	PCIE_B_L0_RXN	GND	PCIE_B_L0_TXP	PCIE_B_L0_TXN	GND	SYSCON~
6	GND	PCIE_B_L1_RXP	PCIE_B_L1_RXN	GND	PCIE_B_L1_TXP	PCIE_B_L1_TXN	GND
7	PCIE_B_L2_RXP	PCIE_B_L2_RXN	GND	PCIE_B_L2_TXP	PCIE_B_L2_TXN	GND	TMP_DET_BP~a
8	GND	PCIE_B_L3_RXP	PCIE_B_L3_RXN	GND	PCIE_B_L3_TXP	PCIE_B_L3_TXN	GND
9	SATA0_RXP ETH2_0P	SATA0_RXN ETH2_0N	GND	SATA0_TXP ETH2_1P	SATA0_TXN ETH2_1N	GND	COM1_TXD
10	GND	USB1_P	USB1_N	GND	USB2_P	USB2_N	GND
11	USB1_PWR	USB2_PWR	GND	SATA1_TXP ETH2_3P GPIO_0	SATA1_TXN ETH2_3N GPIO_1	GND	COM1_RXD
12	GND	SATA1_RXP ETH2_2P GPIO_2	SATA1_RXN ETH2_2N GPIO_3	GND	GPIO_4 (GPIO_0_REDNDNT)	GPIO_5/FAST STRT (GPIO_1_REDNDNT)	GND
13	ETH1_0P ETH2_0P	ETH1_0N ETH2_0N	GND	ETH1_1P ETH2_1P	ETH1_1N ETH2_1N	GND	COM2_TXD
14	GND	ETH1_2P ETH2_2P	ETH1_2N ETH2_2N	GND	ETH1_3P ETH2_3P	ETH1_3N ETH2_3N	GND
15	ETH0_0P ETH1_RXP	ETH0_0N ETH1_RXN	GND	ETH0_1P ETH1_TXP	ETH0_1N ETH1_TXN	GND	MSKRST~/ COM2_RXD
16	GND	ETH0_2P ETH0_RXP	ETH0_2N ETH0_RXN	GND	ETH0_3P ETH0_TXP	ETH0_3N ETH0_TXN	GND

a. This pin is reserved in VITA46.0. It may be isolated from the backplane if required for other purposes in the future.

6.1.3 P2 Connector

Connector type Tyco TE-2102771-2-P2.

Pin	A	B	C	D	E	F	G
1	PMC_IO_04/ XMC_IO_F09	PMC_IO_02/ XMC_IO_F08	GND	PMC_IO_03/ XMC_IO_C09	PMC_IO_01/ XMC_IO_C08	GND	BITFAIL~
2	GND	PMC_IO_08/ XMC_IO_F11	PMC_IO_06/ XMC_IO_F10	GND	PMC_IO_07/ XMC_IO_C11	PMC_IO_05/ XMC_IO_C10	GND
3	PMC_IO_12/ XMC_IO_F13	PMC_IO_10/ XMC_IO_F12	GND	PMC_IO_11 XMC_IO_C13	PMC_IO_09/ XMC_IO_C12	GND	COM1_RTS
4	GND	PMC_IO_16/ XMC_IO_F15	PMC_IO_14/ XMC_IO_F14	GND	PMC_IO_15/ XMC_IO_C15	PMC_IO_13/ XMC_IO_C14	GND
5	PMC_IO_20/ XMC_IO_F17	PMC_IO_18/ XMC_IO_F16	GND	PMC_IO_19/ XMC_IO_C17	PMC_IO_17/ XMC_IO_C16	GND	COM1_CTS
6	GND	PMC_IO_24/ XMC_IO_F19	PMC_IO_22/ XMC_IO_F18	GND	PMC_IO_23/ XMC_IO_C19	PMC_IO_21/ XMC_IO_C18	GND
7	PMC_IO_28/ XMC_IO_E01	PMC_IO_26/ XMC_IO_D01	GND	PMC_IO_27/ XMC_IO_B01	PMC_IO_25/ XMC_IO_A01	GND	COM2_RTS
8	GND	PMC_IO_32/ XMC_IO_E03	PMC_IO_30/ XMC_IO_D03	GND	PMC_IO_31/ XMC_IO_B03	PMC_IO_29/ XMC_IO_A03	GND
9	PMC_IO_36/ XMC_IO_E11	PMC_IO_34/ XMC_IO_D11	GND	PMC_IO_35/ XMC_IO_B11	PMC_IO_33/ XMC_IO_A11	GND	COM2_CTS
10	GND	PMC_IO_40/ XMC_IO_E13	PMC_IO_38/ XMC_IO_D13	GND	PMC_IO_39/ XMC_IO_B13	PMC_IO_37/ XMC_IO_A13	GND
11	PMC_IO_44/ XMC_IO_E05	PMC_IO_42/ XMC_IO_D05	GND	PMC_IO_43/ XMC_IO_B05	PMC_IO_41/ XMC_IO_A05	GND	N/C COM2_RX
12	GND	PMC_IO_48/ XMC_IO_E07	PMC_IO_46/ XMC_IO_D07	GND	PMC_IO_47/ XMC_IO_B07	PMC_IO_45/ XMC_IO_A07	GND
13	PMC_IO_52/ XMC_IO_E09	PMC_IO_50/ XMC_IO_D09	GND	PMC_IO_51/ XMC_IO_B09	PMC_IO_49/ XMC_IO_A09	GND	GPIO_6 (GPIO_2_REDNDNT) SEQ_IN
14	GND	PMC_IO_56/ XMC_IO_E15	PMC_IO_54/ XMC_IO_D15	GND	PMC_IO_55/ XMC_IO_B15	PMC_IO_53/ XMC_IO_A15	GND
15	PMC_IO_60/ XMC_IO_E17	PMC_IO_58/ XMC_IO_D17	GND	PMC_IO_59/ XMC_IO_B17	PMC_IO_57/ XMC_IO_A17	GND	GPIO_7 (GPIO_3_REDNDNT) SEQ_OUT
16	GND	PMC_IO_64/ XMC_IO_E19	PMC_IO_62/ XMC_IO_D19	GND	PMC_IO_63/ XMC_IO_B19	PMC_IO_61/ XMC_IO_A19	GND

6.1.4 Signal Definitions

See the 3U VPX SBC Family manual and Section 4.6, "VPX Interface" for other signal descriptions.

LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

Signal	Description
BITFAIL~	BIT Fail Output. Reflects the status of the BIT Fail LED. This output is open-drain and so may be used to wire-OR signals from a number of cards. The output also has a series current limiting resistor and so may be used to drive an LED directly
COMn_CTS	Serial port n (n = 1 or 2) Clear to Send input (RS-232 mode). This signal may become COMn_RXD (n = 3 or 4) when selected via the DIP Switch and RCW
COMn_RTS	Serial port n (n = 1 or 2) Ready to Send output (RS-232 mode). This signal may become COMn_TXD (n = 3 or 4) when selected via the DIP Switch and RCW
COMn_RXD	Serial port n (n = 1 or 2) Receive Data input (RS-232 mode)
COMn_TXD	Serial port n (n = 1 or 2) Transmit Data output (RS-232 mode)
ETHq_nN/P	BASE-T GbE channel q differential pairs, where q = 0 to 2, n = 0 to 3
ETHq_RXN/P ETHq_TXN/P	BASE-X GbE Channel q receive and transmit differential pairs, where q = 0 or 1
FAST STRT	BIT control signal
GA[0:4]~	Reflected in Backplane Status Register (0x6CA)
GPIO_[7:0]	General purpose input/output, where n = 0 to 7
TCK, TDI, TDO, TMS, TRST~	JTAG interface, routed to the Scanbridge device on the TAC. TCK is AC terminated and connects directly to Scanbridge. TDO is driven by the Scanbridge when selected by the JTAG master
N/C	No connection
NVMRO	Reflected in Backplane Status Register (0x6CA)
PCIE_x_Ln_RXN/P	PCIe backplane fabric receive negative/positive inputs. Link (x) = A or B. Lane (n) = 1 to 4. These should be connected to the transmit outputs of another board to create a link. See Section 4.7.2, "PCIe Switch" for how these lanes may be configured.
PCIE_x_Ln_TXN/P	PCIe backplane fabric transmit negative/positive outputs. Link (x) = A or B. Lane (n) = 1 to 4. These should be connected to the receive inputs of another board to create a link. See Section 4.7.2, "PCIe Switch" for how these lanes may be configured
SATAn_RXN/P, SATAn_TXN/P	SATA channel n (n=0, 1) Receive input and Transmit output differential pairs
SEQ_IN/OUT	Power Supply Sequence Input/Output
SM_CLK, SM_DATA	Connected to the BMM via an I^2C buffer. Allows access to certain on-board resources from an external I^2C master
SYSCON~	Reflected in Backplane Status Register (0x6CA)
SYSRESET~	The SBC314 may drive this low if configured as System Controller
TMP_DET_BP~	Anti-tamper pin. Connected to the CPU's TMP_DETECT pin directly. This pin should be grounded, or left open, as needed in the application
USBn_N/P	Universal Serial Bus differential pairs
USBn_Power	Universal Serial Bus switched power outputs (5V)
VBAT	This can be used to power the real-time clock on the SBC314 (maximum current approximately 1µA)

6.2 PMC Connectors

6.2.1 J11 and J12 Connectors

Connector type Molex-71439-0864-J11-PCB and Molex-71439-0864-J12.

J11				J12			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TCK	2	N12V_AUX	1	P12V_AUX	2	TRST~
3	GND	4	INTA~	3	TMS	4	TDO
5	INTB~	6	INTC~	5	TDI	6	GND
7	BUSMODE1	8	P5V	7	GND	8	N/C
9	INTD~	10	N/C	9	N/C	10	N/C
11	GND	12	N/C	11	BUSMODE2	12	P3V3
13	CLK	14	GND	13	RESET_IN	14	BUSMODE3
15	GND	16	GNT_A~	15	P3V3	16	BUSMODE4
17	REQ_A~	18	P5V	17	N/C	18	GND
19	VIO	20	AD31	19	AD30	20	AD29
21	AD28	22	AD27	21	GND	22	AD26
23	AD25	24	GND	23	AD24	24	P3V3
25	GND	26	C/BE3~	25	IDSELA	26	AD23
27	AD22	28	AD21	27	P3V3	28	AD20
29	AD19	30	P5V	29	AD18	30	GND
31	VIO	32	AD17	31	AD16	32	C/BE2~
33	FRAME~	34	GND	33	GND	34	IDSELB
35	GND	36	IRDY~	35	TRDY~	36	P3V3
37	DEVSEL~	38	P5V	37	GND	38	STOP~
39	XCAP	40	LOCK~	39	PERR~	40	GND
41	N/C	42	N/C	41	P3V3	42	SERR~
43	PAR	44	GND	43	C/BE1~	44	GND
45	VIO	46	AD15	45	AD14	46	AD13
47	AD12	48	AD11	47	M66EN	48	AD10
49	AD09	50	P5V	49	AD8	50	P3V3
51	GND	52	C/BE0~	51	AD7	52	REQ_B~
53	AD06	54	AD05	53	P3V3	54	GNT_B~
55	AD04	56	GND	55	N/C	56	GND
57	VIO	58	AD03	57	N/C	58	EREADY
59	AD02	60	AD01	59	GND	60	RESET_OUT~
61	AD00	62	P5V	61	ACK64~	62	P3V3
63	GND	64	REQ64~	63	GND	64	MONARCH~

6.2.2 J13 and J14 Connectors

Connector type Molex-71439-0864-J13 and Molex-71439-0864-J14.

J13				J14			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	N/C	2	GND	1	PMC_IO_01	2	PMC_IO_02
3	GND	4	C/BE7~	3	PMC_IO_03	4	PMC_IO_04
5	C/BE6~	6	C/BE5~	5	PMC_IO_05	6	PMC_IO_06
7	C/BE4~	8	GND	7	PMC_IO_07	8	PMC_IO_08
9	VIO	10	PAR64	9	PMC_IO_09	10	PMC_IO_10
11	AD63	12	AD62	11	PMC_IO_11	12	PMC_IO_12
13	AD61	14	GND	13	PMC_IO_13	14	PMC_IO_14
15	GND	16	AD60	15	PMC_IO_15	16	PMC_IO_16
17	AD59	18	AD58	17	PMC_IO_17	18	PMC_IO_18
19	AD57	20	GND	19	PMC_IO_19	20	PMC_IO_20
21	VIO	22	AD56	21	PMC_IO_21	22	PMC_IO_22
23	AD55	24	AD54	23	PMC_IO_23	24	PMC_IO_24
25	AD53	26	GND	25	PMC_IO_25	26	PMC_IO_26
27	GND	28	AD52	27	PMC_IO_27	28	PMC_IO_28
29	AD51	30	AD50	29	PMC_IO_29	30	PMC_IO_30
31	AD49	32	GND	31	PMC_IO_31	32	PMC_IO_32
33	GND	34	AD48	33	PMC_IO_33	34	PMC_IO_34
35	AD47	36	AD46	35	PMC_IO_35	36	PMC_IO_36
37	AD45	38	GND	37	PMC_IO_37	38	PMC_IO_38
39	VIO	40	AD44	39	PMC_IO_39	40	PMC_IO_40
41	AD43	42	AD42	41	PMC_IO_41	42	PMC_IO_42
43	AD41	44	GND	43	PMC_IO_43	44	PMC_IO_44
45	GND	46	AD40	45	PMC_IO_45	46	PMC_IO_46
47	AD39	48	AD38	47	PMC_IO_47	48	PMC_IO_48
49	AD37	50	GND	49	PMC_IO_49	50	PMC_IO_50
51	GND	52	AD36	51	PMC_IO_51	52	PMC_IO_52
53	AD35	54	AD34	53	PMC_IO_53	54	PMC_IO_54
55	AD33	56	GND	55	PMC_IO_55	56	PMC_IO_56
57	VIO	58	AD32	57	PMC_IO_57	58	PMC_IO_58
59	N/C	60	N/C	59	PMC_IO_59	60	PMC_IO_60
61	N/C	62	GND	61	PMC_IO_61	62	PMC_IO_62
63	GND	64	N/C	63	PMC_IO_63	64	PMC_IO_64

6.2.3 Signal Descriptions

See the 3U VPX SBC Family manual for other signal descriptions.

LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

Signal	Description
BUSMODE[4:2]	On the SBC314, the bus mode is always PCI. BUSMODE2 is pulled-up. BUSMODE[4:3] are pulled down to GND
EREADY	Reflected in PMC1/XMC1 Status Register (0x6C8)
MONARCH~	Monarch mode is not supported on the SBC314. This signal is pulled high
RESET_OUT~	This signal can be driven by a Monarch PMC to reset the SBC314

6.3 XMC Connectors

6.3.1 J15 Connector

Connector type:

- Samtec-ASP-103612-04-J15 when VITA42 XMC variant is specified
- Tyco TE-2102061-2 when VITA61 XMC variant is specified

Pin	A	B	C	D	E	F
1	PCIE_TX0P	PCIE_TX0N	P3V3	PCIE_TX1P	PCIE_TX1N	VPWR
2	GND	GND	TRST~	GND	GND	RESET_IN~
3	PCIE_TX2P	PCIE_TX2N	P3V3	PCIE_TX3P	PCIE_TX3N	VPWR
4	GND	GND	TCK	GND	GND	RESET_OUT~
5	NC	NC	P3V3	NC	NC	VPWR
6	GND	GND	TMS	GND	GND	P12V_AUX
7	NC	NC	P3V3	NC	NC	VPWR
8	GND	GND	TDI	GND	GND	N12V_AUX
9	N/C	N/C	N/C	N/C	N/C	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PCIE_RX0P	PCIE_RX0N	MBIST~	PCIE_RX1P	PCIE_RX1N	VPWR
12	GND	GND	GA1	GND	GND	PRESENT~
13	PCIE_RX2P	PCIE_RX2N	P3V3_AUX	PCIE_RX3P	PCIE_RX3N	VPWR
14	GND	GND	GA2	GND	GND	SM_DATA
15	NC	NC	N/C	NC	NC	VPWR
16	GND	GND	NVMRO	GND	GND	SM_CLK
17	NC	NC	N/C	NC	NC	N/C
18	GND	GND	N/C	GND	GND	N/C
19	REFCLK_P	REFCLK_N	N/C	N/C	N/C	N/C

NOTE

Signal names correspond to the viewpoint of the XMC.

6.3.2 J16 Pinout

Connector type:

- Samtec-ASP-103612-04-J15 when VITA42 XMC variant is specified
- Tyco TE-2102061-2 when VITA61 XMC variant is specified

Pin	A	B	C	D	E	F
1	XMC_IO_A01	XMC_IO_B01	N/C	XMC_IO_D01	XMC_IO_E01	N/C
2	GND	GND	N/C	GND	GND	N/C
3	XMC_IO_A03	XMC_IO_B03	N/C	XMC_IO_D03	XMC_IO_E03	N/C
4	GND	GND	N/C	GND	GND	N/C
5	XMC_IO_A05	XMC_IO_B05	N/C	XMC_IO_D05	XMC_IO_E05	N/C
6	GND	GND	N/C	GND	GND	N/C
7	XMC_IO_A07	XMC_IO_B07	N/C	XMC_IO_D07	XMC_IO_E07	N/C
8	GND	GND	XMC_IO_C08	GND	GND	XMC_IO_F08
9	XMC_IO_A09	XMC_IO_B09	XMC_IO_C09	XMC_IO_D09	XMC_IO_E09	XMC_IO_F09
10	GND	GND	XMC_IO_C10	GND	GND	XMC_IO_F10
11	XMC_IO_A11	XMC_IO_3B11	XMC_IO_C11	XMC_IO_D11	XMC_IO_E11	XMC_IO_F11
12	GND	GND	XMC_IO_C12	GND	GND	XMC_IO_F12
13	XMC_IO_A13	XMC_IO_B13	XMC_IO_C13	XMC_IO_D13	XMC_IO_E13	XMC_IO_F13
14	GND	GND	XMC_IO_C14	GND	GND	XMC_IO_F14
15	XMC_IO_A15	XMC_IO_B15	XMC_IO_C15	XMC_IO_D15	XMC_IO_E15	XMC_IO_F15
16	GND	GND	XMC_IO_C16	GND	GND	XMC_IO_F16
17	XMC_IO_A17	XMC_IO_B17	XMC_IO_C17	XMC_IO_D17	XMC_IO_E17	XMC_IO_F17
18	GND	GND	XMC_IO_C18	GND	GND	XMC_IO_F18
19	XMC_IO_A19	XMC_IO_B19	XMC_IO_C19	XMC_IO_D19	XMC_IO_E19	XMC_IO_F19

6.3.3 Signal Descriptions

See the 3U VPX SBC Family manual for other signal descriptions.



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3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

Signal	Description
MBIST~	Reflected in PMC1/XMC1 Status Register (0x6C8)

6.4 Test Access Card Connector (P4)

Connector type Molex-55201-0878.

P4 is used to connect to the TTAC, which provides factory-level connectivity. Pinout information is not provided here, as access to the signals can only be achieved using the TAC.

A • Specifications

A.1 Mechanical Specifications

Weight	SBC314/X build levels 4 and 5 = 452g including the heatsink but excluding any mezzanine. SBC314/X build levels 1 to 3 = 306g including the heatsink and front panel but excluding any mezzanine
Dimensions	The air-cooled SBC314/X is available in 0.8" and 1.0" pitch form factors compatible with VITA48.1. The conduction-cooled SBC314/X is available in 0.8" and 0.85" pitch form factors compatible with VITA48.2, and in a 0.8" pitch form factor compatible with VITA46.0
Wedgelocks	Correct adjustment requires a calibrated torque wrench with a hexagonal head of size 2.5mm, set to 0.9 Nm/ 8 in-lb ± 0.1 Nm/1 in-lb

A.2 Technical Specifications

Features	Details	Comments
Processor	Freescale T1042/T2081	(4 x e5500)/(4 x e6500) PowerPC processing cores @ up to 1.4/1.8 GHz
RAM	Up to 8 GByte DDR3 SDRAM with ECC	Running at up to 800 MHz
ROM	Up to 256 MByte NOR Flash memory	8 MByte allocated to Boot Flash and the rest to User Flash. Advanced sector protection features
NOVRAM	512 KByte	Non-volatile storage for data that must not be lost when power is removed
Solid State Drive	Up to 16 GByte options	SATA Solid State Drive
Infrastructure	PCIe	High bandwidth serial-interconnect. Non-blocking switch architecture
Ethernet	2/3x 10/100/1000BASE-T ports 2 x 1000BASE-X ports	Third BASE-T port imposes limitations on other I/O features due to backplane pinout
Serial ports	2 x RS-232/422/485 Async	T1042/T1081 provides software-configurable COM1 & COM2 debug ports
USB2.0	2 backplane ports	
SATA	2 backplane channels	The external SATA ports support operation at SATA 2.0 speeds (3 Gbit/s)
Discrete Digital I/O	Up to 8-bits, 3.3V LVCMOS compatible, 5V tolerant	Able to generate edge- or level-triggered interrupts
PCIe	8 lanes on VPX P1	2.5 or 5 GHz. Configurable in up to 8 ports with one non-transparent ports
PMC/XMC sites	One PMC/XMC site	64-bit PCI-X interface at up to 133 MHz. x4 PCIe interface
DMA controllers		Two (T1042) or three (T2081) 8 channel DMA controllers
Timers	8 x 31-bit timers	Provided by the T1042/T1081. Programmable frequency with up to 15 ns resolution. Ability to cascade to form larger timers
Watchdog timer	Two 32-bit timers One 16-bit timer	Each core includes watchdog timer with programmable interrupt and reset thresholds. Avionics watchdog timer with 25 MHz clock included in the FPGA
Real-Time Clock	Time Of Day/Calendar	1 second resolution. Standby power may be connected from the VBAT pin to maintain data during power down
ETI	Quarter second resolution	Logs the total accumulated time the board has been powered, and the number of power cycles
JTAG Interface	VPX backplane JTAG to mezzanine sites	JTAG via Test Access Card for CPU debugger and boundary scan

A.3 Electrical Specifications

A.3.1 Voltage Supply Requirements

See the 3U VPX SBC Family manual.

LINK

3U VPX Single Board Computer Family Hardware Reference Manual, publication number VPX3USBC-HRM

The SBC314 does not use the VPX Vs1 supply. The SBC314 does not use the VPX ±12V Auxiliary supplies, but routes them to the mezzanine site.

The VBAT backplane signal may optionally be used to power the Real Time Clock when other supplies are removed.

Supply	Minimum	Nominal	Maximum
VBAT	1.8V	3.3V	5.5V

A.3.2 Current Consumption

Projected current consumption figures for the SBC314 are shown below. These are measured at the specified cold-wall temperatures in a conduction-cooled environment.

Supply	T1042 @ 1.4 GHz		T2081 @ 1.8 GHz	
	Current (A)		Current (A)	
	+25°C	+85°C	+25°C	+85°C
+3.3V (VS2)	1.0 (3.3W)	1.2 (3.96W)	1.0 (3.3W)	1.2 (3.96W)
+5V (VS3)	2.8 (14W)	4.6 (23W)	4.5 (22.5W)	7.7 (38.5W)
P3V3_AUX	0.3 (0.99W)	0.3 (0.99W)	0.3 (0.99W)	0.3 (0.99W)
Total Power	18.29 W	27.95W	26.79W	43.45W

NOTE

The above table is based on worst-case data sheet calculations. Use it to specify the external power system. Use the following table to estimate actual power consumption and thermal loading.

TIP

The I/O usage is a primary driver of the power consumption, so switching off in software any unused I/O, especially where connected via the PCIe Switch, can reduce power requirements.

Table A-1 Measured Current Consumption

Processor	T1042 @ 1.4 GHz		T2081 @ 1.8 GHz	
Whetstones (System)	3320		6768	
Whetstones (Core)	830		846	
Coremark	15551		40428	
Supply	+25°C	+85°C	+25°C	+85°C
+3.3V (VS2 and P3V3_AUX)	0.45A (1.5W)	0.48A (1.6W)	0.42A (1.4W)	0.45A (1.5W)
+5V (VS3)	2.64A (13.2W)	3.06A (15.3W)	4.06A (20.3W)	4.82A (24.1W)
Total Power	14.7W	17W	21.7W	25.6W

The SBC314 was configured with 4 GByte of SDRAM running at 1.6 GHz, and 256 MByte of Flash, and was tested with all cores (4 for the T1042 or 8 for the T2081) running VxWorks 6.9.4 with gnu-smp configuration. GbE links were active but idle.

A.4 Environmental Specifications

A.4.1 Air-cooled Boards

Table A-2 Air-cooled Environmental Specifications

Environment	Level 1	Level 2	Level 3
Cooling Method	Air	Air	Air
High/Low Temperature Operational	0 to +55 °C 300 ft/min airflow	-20 to +65 °C 300 ft/min airflow	-40 to +75 °C 600 ft/min airflow
Storage Temperature	-50 to +100 °C	-50 to +100 °C	-50 to +100 °C
Random Vibration	0.002g2/Hz 10-2000 Hz random 2g sinusoidal, 5-500 Hz	0.002g2/Hz 10-2000 Hz random 2g sinusoidal, 5-500 Hz	0.04g2/Hz 20-2000 Hz flat response to 1000 Hz, 6 dB/octave roll-off from 1000 to 2000 Hz
Shock	20g, peak sawtooth 11 ms duration	20g, peak sawtooth 11 ms duration	20g, peak sawtooth 11 ms duration
Humidity	Up to 95% RH	Up to 95% RH varying temperature 10 cycles, 240 hours	Up to 95% RH varying temperature 10 cycles, 240 hours

A.4.2 Conduction-cooled Boards

Table A-3 Conduction-cooled Environmental Specifications

Environment	Level 4	Level 5
Cooling Method	Conduction	Conduction
High/Low Temperature Operational	-40 to +75 °C at cold-wall	-40 to +85 °C at cold-wall
Storage Temperature	-50 to +100 °C	-50 to +100 °C
Random Vibration	0.01g2/Hz 15-2000 Hz random ~12g RMS	0.01g2/Hz 15-2000 Hz random ~12g RMS
Shock	40g, peak sawtooth 11 ms duration	40g, peak sawtooth 11 ms duration
Humidity	Up to 95% RH varying temperature 10 cycles, 240 hours	Up to 95% RH varying temperature 10 cycles, 240 hours



NOTE

As shown above, the build level dictates the maximum ambient temperature at which the board can operate. As the temperature affects the CPU operating frequency, this means that for a given build level, a maximum CPU operating frequency is achievable. For more details, contact Abaco Systems.

A.5 Reliability (MTBF)

The following table shows the predicted values for reliability as Mean Time between Failures (MTBF) and Failures Per Million Hours (FPMH) for an SBC314 as of 10th November 2014:

Environment	Temperature	FPMH	MTBF (Hours)
Ground Benign	30°C	1.93105	517 854
Ground Fixed	40°C	9.63354	103 804
Ground Mobile	45°C	23.76106	42 086
Naval Sheltered	40°C	13.10331	76 317
Naval Unsheltered	45°C	32.58030	30 693
Airborne Inhabited Cargo	55°C	25.21705	39 656
Airborne Inhabited Fighter	55°C	33.97892	29 430
Airborne Uninhabited Cargo	70°C	62.75683	15 935
Airborne Uninhabited Fighter	70°C	83.43083	11 986
Airborne Rotary Wing	55°C	69.59969	14 368
Space Flight	30°C	1.46060	684 651

The following table shows the predicted values for reliability as Mean Time between Failures (MTBF) and Failures Per Million Hours (FPMH) for an SBC314X as of 5th August 2015:

Environment	Temperature	FPMH	MTBF (Hours)
Ground Benign 30°C	30°C	1.36072	734 905
Ground Fixed 40°C	40°C	7.58348	131 866
Ground Mobile 45°C	45°C	17.92979	55 773
Naval Sheltered 40°C	40°C	9.82824	101 748
Naval Unsheltered 45°C	45°C	24.82848	40 276
Airborne Inhabited Cargo 55°C	55°C	19.83416	50 418
Airborne Inhabited Fighter 55°C	55°C	27.56198	36 282
Airborne Uninhabited Cargo 70°C	70°C	50.30824	19 877
Airborne Uninhabited Fighter 70°C	70°C	68.34318	14 623
Airborne Rotary Wing 55°C	55°C	54.26025	18 430
Space Flight 30°C	30°C	1.02459	976 000

The predictions are carried out using MIL-HDBK-217F Notice 2, Parts Count method. To complement the 217 failure rates, some manufacturers' data is included where appropriate; πQ values have been modified according to the ANSI/VITA51.1-2008 (R2013) Specification. These predictions relate only to the electronic components; mechanical components are not included.

These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user-fitted mezzanines.

A.6 Product Codes

SBC314 (X)-	A	B	C	D	E	F	G	H	Description
A	1[a]								Ruggedization Level 1, air-cooled
	2[a]								Ruggedization Level 2, air-cooled
	3[a]								Ruggedization Level 3, air-cooled
	4[b]								Ruggedization Level 4, conduction-cooled
	5[b]								Ruggedization Level 5, conduction-cooled
B		0							Reserved
		4							T1042 @ 1.4 GHz
		8							T2081 @ 2.1 GHz
C			0						Reserved
			4						4 GByte SDRAM
D				0					Reserved
				1					256 MByte Flash
E					0				NAND Flash Not Installed
					2				16 GByte NAND Flash
F						0			Reserved
						1			3x 1000BASE-T, 4x redundant GPIO, VITA 42
						2			2x 1000BASE-X + 1x 1000BASE-T, 4x redundant GPIO, 2x external SATA (or 1 external/1 internal), VITA 42
						3			2x 1000BASE-X + 1x 1000BASE-T, 8x standard GPIO, 1x external SATA, 1x internal SATA, VITA 42
						4			2x 1000BASE-T, 8x standard GPIO, 1x external SATA, 1x internal SATA, VITA 42
						A			3x 1000BASE-T, 4x redundant GPIO, VITA 61
						B			2x 1000BASE-X + 1x 1000BASE-T, 4x redundant GPIO, 2x external SATA (or 1 external/1 internal), VITA 61
						C			2x 1000BASE-X + 1x 1000BASE-T, 8x standard GPIO, 1x external SATA, 1x internal SATA, VITA 61
						D			2x 1000BASE-T, 8x standard GPIO, 1x external SATA, 1x internal SATA, VITA 61
G							0		Reserved
							3		VxWorks
							4		BIT / VxWorks
							5		U-Boot
							6		BIT / U-Boot
H								0	Reserved
								1	0.8” pitch, VITA 46
								6[c]	1” pitch, VITA 48
								B[d]	0.85” pitch, VITA 48 (2LM)

[a] Not available with H=B
[b] Not available with H=6
[c] Not available with A=4 or A=5
[d] Not available with A=1, A=2, or A=3



NOTES

The default product code is SBC314(X)-14412131.

See Table A-2 and Table A-3 for more information on Ruggedization levels.

Conformal coat type is 1B73AP. There is an option for Type UR (polyurethane) conformal coating.

A.7 Software Support

Abaco's software strategy allows fully integrated system-level solutions to be realized easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high level debug and run-time functionality of popular commercial operating systems and communications modules.

The software products described below build on those available for previous generations of products, so providing a common interface for technology inserts. The Abaco software strategy ensures that customers can develop market-leading products using the O/S and development environment best suited to their long term program requirements.

A.7.1 Boot Firmware

The Boot firmware provides a foundation layer to interface between the raw board hardware, with its highly programmable device set-ups and flexibility, and the supported operating systems, which require a straight-forward booting and device interface model.

The U-Boot Firmware includes comprehensive configuration facilities, interactive or auto-boot sequencing from a range of device types, automatic PCI resource allocation at initialization, PCI display/interrogation utilities and other valuable features for system integrators.

U-Boot seamlessly absorbs memory or other speed and feature enhancements, giving the same look and feel to the operating system and the user application as the Abaco hardware models advance. This allows the constant use of latest technology in required areas without system impact.

A.7.2 Built In Test

BIT probes from the lowest level of discrete onboard hardware up to Line Replaceable Unit level within a system, ensuring the highest degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialization tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

A.7.3 Continuous/Invocation BIT

CIBIT (which used to be called Background Condition Screening) supplements the BIT initialization test coverage with further health screening that can co-exist with a standard commercial Operating System.

In contrast to a traditional BIT-style test, the intensity and coverage of which makes it destructive to operating systems, the configurable BCS package allows functions such as periodic check-summing, memory scrubbing, and others to be tailored for operation alongside the application in online conditions. Results are stored in Flash in the same format as BIT results. Code is available for reading out BIT/BCS results under the operating system offerings.

A.8 I/O Modules

The recommended RTM for the SBC314 is the VPX3UX600A.

For 3U backplanes, use the VPX3UX300A.

More information about RTMs can be found in the VPX I/O Modules manual.



LINKS

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH

VPX3UX300A Hardware Reference Manual, publication number VPX3UX300A-HRM

VPX3UX600A Hardware Reference Manual, publication number VPX3UX600A-HRM

B • Statement of Volatility

B.1 Volatile Memory

The SBC314 contains volatile memory, i.e., memory in which the contents are lost when power is removed. None of this volatile memory is capable of write-protection.

Memory Type	Size	User Modifiable?	User Data Access?	Function	Process to Clear
DDR3 SDRAM	2 or 4 GByte	Yes	Yes	Main memory	Remove power
Unknown (inside CPU)	128 KByte x 8	Yes	No	CPU L2 cache	Remove power
Unknown (inside CPU)	2 MByte	Yes	No	CPU L3 cache	Remove power
SRAM	1536 bytes	Yes	No	BMM SRAM	Remove power

B.2 Non-Volatile Memory

The SBC314 contains non-volatile memory, i.e., memory in which the contents are retained when power is removed.

Memory Type	Size	User Modifiable?	User Data Access?	Function	Process to Clear
Flash	On-chip	Yes[a]	Yes[a]	PLDs for power management and glue logic	Erase via JTAG interface on TAC, or execute software erase routine
EEPROM	32 KByte	Yes	No	BMM firmware	Execute software erase routine
EEPROM	256 byte	Yes	No	BMM, FRU and configuration data (e.g., serial number)	Execute software erase routine
Flash	256 MByte	Yes	Yes	Boot code, User Flash, BIT results, MAC addresses and configuration data	Execute software erase routine
NVRAM	512 KByte	Yes	Yes	Boot parameters, environment variables and user memory	Execute software erase routine
Flash (SPI)	4 MByte	No	No	U-Boot recovery data	Not user erasable
Flash (SPI)	16 MByte	No	No	Ethernet 2 MAC and configuration data	Not user erasable
EEPROM	32 KByte	Yes	Yes	PCIe Switch configuration information	Execute software erase routine
EEPROM	32 KByte	Yes	Yes	Alternate RCW/user memory	Execute software erase routine
EEPROM	208 bytes	No	No	Clock synthesizer configuration	Not user erasable
EEPROM	10 bytes	Yes	Yes	User memory in ETI	Erase via software
EEPROM	12 bits	Yes	Yes	EEPROM DIP Switch	Erase via software

a. Only in Recovery mode.

B.3 Media

The SBC314 contains media storage capability (i.e., removable or non-removable disk drives, memory cards, etc.).

Memory Type	Removable?	Size	User Modifiable?	User Data Access?	Function	Process to Clear
SATA NAND drive onboard	No	8 or 16 GByte	Yes	Yes	Operating system and file storage (some OSs can implement a read-only file system)	Erase via software. Fast erase supported via software command

C • FPGA ROM Contents

This section defines the contents of the SBC314's RCWs. The terms used below relate to the manual content as follows:

RCW #0 = RCW A for T1042
RCW #1 = RCW B for T1042
RCW #2 = RCW A for T2081
RCW #3 = RCW B for T2081
RCW #4 = RCW for Avionics Application

C.1 RCW #0 SBC314-T1042 Rev 1.1 1400 MHz 2 UART Mode

RCW #0 with preamble and CRC checksum. GP_INFO set to 82 00 00 01

```
00000000:   aa55  aa55  010e  0100  0c10  000e  0800  0000
00000010:   0000  0000  0000  0000  0000  0000  0040  4002
00000020:   fc02  7000  2100  0400  0000  0000  8200  0001
00000030:   0000  0000  0003  303c  0000  0000  4001  5000
00000040:   0000  0000  0000  0000  0813  8040  4d97  1eaf
```

Decode as follows:

Bits	Description	Size'hvalue
0-1	SYS_PLL_CFG	2'h00
2-6	SYS_PLL_RAT	5'h06
7-7	RESERVED	1'h0
8-9	MEM_PLL_CFG	2'h00
10-15	MEM_PLL_RAT	6'h10
16-23	RESERVED	8'h0
24-25	CGA_PLL1_CFG	2'h00
26-31	CGA_PLL1_RAT	6'h0E
32-33	CGA_PLL2_CFG	2'h00
34-39	CGA_PLL2_RAT	6'h08
40-95	RESERVED	56'h0
96-99	C1_PLL_SEL	4'h00
100-103	C2_PLL_SEL	4'h00
104-107	C3_PLL_SEL	4'h00
108-111	C4_PLL_SEL	4'h00
112-127	RESERVED	16'h0
128-135	SRDS_PRTCL_S1	8'h00
136-157	RESERVED	22'h0
158-158	FM1_MAC_RAT	1'h00
159-159	RESERVED	1'h0
160-161	SRDS_PLL_REF_CLK_SEL_S1	2'h00
162-167	RESERVED	6'h0
168-169	SRDS_PLL_PD_S1	2'h01
170-175	RESERVED	6'h0
176-177	SRDS_DIV_PEX	2'h01

Bits	Description	Size'hvalue
178-179	RESERVED	2'h0
180-180	SRDS_DIV_AURORA	1'h00
181-182	RESERVED	2'h0
183-183	EMI1_MODE	1'h00
184-185	RESERVED	2'h0
186-187	DDR_REFCLK_SEL	2'h00
188-189	RESERVED	2'h0
190-191	DDR_FDBK_MUL	2'h02
192-195	PBI_SRC	4'h0F
196-200	BOOT_LOC	5'h18
201-201	BOOT_HO	1'h00
202-202	SB_EN	1'h00
203-211	IFC_MODE	9'h27
212-223	RESERVED	12'h0
224-226	HWA_CGA_M1_CLK_SEL	3'h01
227-229	RESERVED	3'h0
230-231	DRAM_LAT	2'h01
232-232	DDR_RATE	1'h00
233-233	RESERVED	1'h0
234-234	DDR_RSV0	1'h00
235-241	RESERVED	7'h0
242-242	SYS_PLL_SPD	1'h00
243-243	MEM_PLL_SPD	1'h00
244-244	CGA_PLL1_SPD	1'h00
245-245	CGA_PLL2_SPD	1'h01
246-263	RESERVED	18'h0
264-266	HOST_AGT_PEX	3'h00
267-287	RESERVED	21'h0
288-319	GP_INFO	32'h82000001
320-320	RESERVED	1'h0
321-321	UC1_CTSB_CDB_SEL	1'h00
322-322	UC3_CTSB_CDB_SEL	1'h00
323-356	RESERVED	34'h0
357-359	IRQ_EXT	3'h00
360-362	SPI_EXT	3'h00
363-365	RESERVED	3'h0
366-368	UART_BASE	3'h06
369-369	ASLEEP	1'h00
370-370	RTC	1'h01
371-371	SDHC_BASE	1'h01
372-372	IRQ_OUT	1'h00
373-381	IRQ_BASE	9'h0F
382-383	SPI_BASE	2'h00
384-404	RESERVED	21'h0
405-405	IFC_GRP_E1_BASE	1'h00
406-406	IFC_GRP_E2_BASE	1'h00
407-407	IFC_GRP_D_BASE	1'h00
408-408	RESERVED	1'h0
409-409	IFC_GRP_C_BASE	1'h00
410-411	IFC_GRP_B_BASE	2'h00
412-413	IFC_GRP_A_BASE	2'h00
414-415	RESERVED	2'h0

Bits	Description	Size'hvalue
416-416	1588	1'h00
417-417	SDHC	1'h01
418-419	EC1	2'h00
420-421	EC2	2'h00
422-423	I2C3	2'h00
424-425	I2C4	2'h00
426-427	QE_TDMA	2'h00
428-429	QE_TDMB	2'h00
430-431	DVDD_VSEL	2'h01
432-433	L1VDD_VSEL	2'h01
434-435	LVDD_VSEL	2'h01
436-437	CVDD_VSEL	2'h00
438-439	EVDD_VSEL	2'h00
440-440	MAC2_GMII_SEL	1'h00
441-441	HDLC1_MODE	1'h00
442-442	HDLC2_MODE	1'h00
443-443	MDIO_MDC1	1'h00
444-445	DMA1	2'h00
446-447	DMA2	2'h00
448-511	RESERVED	64'h0

C.2 RCW #1 SBC314-T1042 Rev 1.1 1400 MHz 4 UART Mode

RCW #1 with preamble and CRC checksum. GP_INFO set to 82 00 01 01

```
00000000: aa55 aa55 010e 0100 0c10 000e 0800 0000
00000010: 0000 0000 0000 0000 0000 0000 0040 4002
00000020: fc02 7000 2100 0400 0000 0000 8200 0101
00000030: 0000 0000 0003 b03c 0000 0000 4001 5000
00000040: 0000 0000 0000 0000 0813 8040 0786 cbcb
```

Decoded as follows:

Bits	Description	Size'hvalue
0-1	SYS_PLL_CFG	2'h00
2-6	SYS_PLL_RAT	5'h06
7-7	RESERVED	1'h0
8-9	MEM_PLL_CFG	2'h00
10-15	MEM_PLL_RAT	6'h10
16-23	RESERVED	8'h0
24-25	CGA_PLL1_CFG	2'h00
26-31	CGA_PLL1_RAT	6'h0E
32-33	CGA_PLL2_CFG	2'h00
34-39	CGA_PLL2_RAT	6'h08
40-95	RESERVED	56'h0
96-99	C1_PLL_SEL	4'h00
100-103	C2_PLL_SEL	4'h00
104-107	C3_PLL_SEL	4'h00
108-111	C4_PLL_SEL	4'h00
112-127	RESERVED	16'h0
128-135	SRDS_PRTCL_S1	8'h00
136-157	RESERVED	22'h0
158-158	FM1_MAC_RAT	1'h00
159-159	RESERVED	1'h0
160-161	SRDS_PLL_REF_CLK_SEL_S1	2'h00
162-167	RESERVED	6'h0
168-169	SRDS_PLL_PD_S1	2'h01
170-175	RESERVED	6'h0
176-177	SRDS_DIV_PEX	2'h01
178-179	RESERVED	2'h0
180-180	SRDS_DIV_AURORA	1'h00
181-182	RESERVED	2'h0
183-183	EMI1_MODE	1'h00
184-185	RESERVED	2'h0
186-187	DDR_REFCLK_SEL	2'h00
188-189	RESERVED	2'h0
190-191	DDR_FDBK_MUL	2'h02
192-195	PBI_SRC	4'h0F
196-200	BOOT_LOC	5'h18
201-201	BOOT_HO	1'h00
202-202	SB_EN	1'h00

Bits	Description	Size'hvalue
203-211	IFC_MODE	9'h27
212-223	RESERVED	12'h0
224-226	HWA_CGA_M1_CLK_SEL	3'h01
227-229	RESERVED	3'h0
230-231	DRAM_LAT	2'h01
232-232	DDR_RATE	1'h00
233-233	RESERVED	1'h0
234-234	DDR_RSV0	1'h00
235-241	RESERVED	7'h0
242-242	SYS_PLL_SPD	1'h00
243-243	MEM_PLL_SPD	1'h00
244-244	CGA_PLL1_SPD	1'h00
245-245	CGA_PLL2_SPD	1'h01
246-263	RESERVED	18'h0
264-266	HOST_AGT_PEX	3'h00
267-287	RESERVED	21'h0
288-319	GP_INFO	32'h82000101
320-320	RESERVED	1'h0
321-321	UC1_CTSB_CDB_SEL	1'h00
322-322	UC3_CTSB_CDB_SEL	1'h00
323-356	RESERVED	34'h0
357-359	IRQ_EXT	3'h00
360-362	SPI_EXT	3'h00
363-365	RESERVED	3'h0
366-368	UART_BASE	3'h07
369-369	ASLEEP	1'h00
370-370	RTC	1'h01
371-371	SDHC_BASE	1'h01
372-372	IRQ_OUT	1'h00
373-381	IRQ_BASE	9'h0F
382-383	SPI_BASE	2'h00
384-404	RESERVED	21'h0
405-405	IFC_GRP_E1_BASE	1'h00
406-406	IFC_GRP_E2_BASE	1'h00
407-407	IFC_GRP_D_BASE	1'h00
408-408	RESERVED	1'h0
409-409	IFC_GRP_C_BASE	1'h00
410-411	IFC_GRP_B_BASE	2'h00
412-413	IFC_GRP_A_BASE	2'h00
414-415	RESERVED	2'h0
416-416	1588	1'h00
417-417	SDHC	1'h01
418-419	EC1	2'h00
420-421	EC2	2'h00
422-423	I2C3	2'h00
424-425	I2C4	2'h00
426-427	QE_TDMA	2'h00
428-429	QE_TDMB	2'h00
430-431	DVDD_VSEL	2'h01
432-433	L1VDD_VSEL	2'h01

Bits	Description	Size'hvalue
434-435	LVDD_VSEL	2'h01
436-437	CVDD_VSEL	2'h00
438-439	EVDD_VSEL	2'h00
440-440	MAC2_GMII_SEL	1'h00
441-441	HDLC1_MODE	1'h00
442-442	HDLC2_MODE	1'h00
443-443	MDIO_MDC1	1'h00
444-445	DMA1	2'h00
446-447	DMA2	2'h00
448-511	RESERVED	64'h0

C.3 RCW #2 SBC314-T2081 Rev 1.1 1800 MHz 2 UART Mode

RCW #2 with preamble and CRC checksum. GP_INFO set to 82 00 02 00

```
00000000: aa55 aa55 010e 0100 0c08 1012 1000 0000
00000010: 0000 0000 0000 0000 aa00 0002 0040 4000
00000020: fc02 7000 c100 0000 0000 0000 8200 0200
00000030: 0000 0000 0003 3000 0000 0000 8800 0000
00000040: 0000 0000 0000 0001 0813 8040 528c a3ca
```

Decoded as follows:

Bits	Description	Size'hvalue
0-1	SYS_PLL_CFG	2'h00
2-6	SYS_PLL_RAT	5'h06
7-7	RESERVED	1'h0
8-9	MEM_PLL_CFG	2'h00
10-15	MEM_PLL_RAT	6'h08
16-17	RESERVED	2'h0
18-23	MEM_PLL_RAT_ERRATUM_7212	6'h10
24-25	CGA_PLL1_CFG	2'h00
26-31	CGA_PLL1_RAT	6'h12
32-33	CGA_PLL2_CFG	2'h00
34-39	CGA_PLL2_RAT	6'h10
40-95	RESERVED	56'h0
96-99	C1_PLL_SEL	4'h00
100-127	RESERVED	28'h0
128-135	SRDS_PRTCL_S1	8'hAA
136-157	RESERVED	22'h0
158-158	FM_MAC_RAT	1'h01
159-159	RESERVED	1'h0
160-161	SRDS_PLL_REF_CLK_SEL_S1	2'h00
162-167	RESERVED	6'h0
168-169	SRDS_PLL_PD_S1	2'h01
170-175	RESERVED	6'h0
176-177	SRDS_DIV_PEX_S1	2'h01
178-191	RESERVED	14'h0
192-195	PBI_SRC	4'h0F
196-200	BOOT_LOC	5'h18
201-201	BOOT_HO	1'h00
202-202	SB_EN	1'h00
203-211	IFC_MODE	9'h27
212-223	RESERVED	12'h0
224-226	HWA_CGA_M1_CLK_SEL	3'h06
227-229	RESERVED	3'h0
230-231	DRAM_LAT	2'h01
232-232	DDR_RATE	1'h00
233-263	RESERVED	31'h0

Bits	Description	Size'hvalue
264-266	HOST_AGT_PEX	3'h00
267-287	RESERVED	21'h0
288-319	GP_INFO	32'h82000200
320-356	RESERVED	37'h0
357-359	IRQ_EXT	3'h00
360-362	SPI_EXT	3'h00
363-365	RESERVED	3'h0
366-368	UART_BASE	3'h06
369-369	ASLEEP	1'h00
370-370	RTC	1'h01
371-371	SDHC_BASE	1'h01
372-372	IRQ_OUT	1'h00
373-381	IRQ_BASE	9'h00
382-383	SPI_BASE	2'h00
384-404	RESERVED	21'h0
405-405	IFC_GRP_E1_BASE	1'h00
406-406	IFC_GRP_E2_BASE	1'h00
407-407	IFC_GRP_D_BASE	1'h00
408-409	RESERVED	2'h0
410-411	IFC_GRP_B_BASE	2'h00
412-413	IFC_GRP_A_BASE	2'h00
414-415	RESERVED	2'h0
416-416	1588	1'h01
417-418	EC1	2'h00
419-420	EC2	2'h01
421-422	I2C3	2'h00
423-424	I2C4	2'h00
425-443	RESERVED	19'h0
444-444	DMA1	1'h00
445-445	SDHC	1'h00
446-447	DMA2	2'h00
448-508	RESERVED	61'h0
509-511	HWA_CGA_M2_CLK_SEL	3'h01

C.4 RCW #3 SBC314-T2081 Rev 1.1 1800 MHz 4 UART Mode

RCW #3 with preamble and CRC checksum. GP_INFO set to 82 00 03 00

```
00000000: aa55 aa55 010e 0100 0c08 1012 1000 0000
00000010: 0000 0000 0000 0000 aa00 0002 0040 4000
00000020: fc02 7000 c100 0000 0000 0000 8200 0300
00000030: 0000 0000 0003 b000 0000 0000 8800 0000
00000040: 0000 0000 0000 0001 0813 8040 189d 76ae
```

Decoded as follows:

Bits	Description	Size'hvalue
0-1	SYS_PLL_CFG	2'h00
2-6	SYS_PLL_RAT	5'h06
7-7	RESERVED	1'h0
8-9	MEM_PLL_CFG	2'h00
10-15	MEM_PLL_RAT	6'h08
16-17	RESERVED	2'h0
18-23	MEM_PLL_RAT_ERRATUM_7212	6'h10
24-25	CGA_PLL1_CFG	2'h00
26-31	CGA_PLL1_RAT	6'h12
32-33	CGA_PLL2_CFG	2'h00
34-39	CGA_PLL2_RAT	6'h10
40-95	RESERVED	56'h0
96-99	C1_PLL_SEL	4'h00
100-127	RESERVED	28'h0
128-135	SRDS_PRTCL_S1	8'hAA
136-157	RESERVED	22'h0
158-158	FM_MAC_RAT	1'h01
159-159	RESERVED	1'h0
160-161	SRDS_PLL_REF_CLK_SEL_S1	2'h00
162-167	RESERVED	6'h0
168-169	SRDS_PLL_PD_S1	2'h01
170-175	RESERVED	6'h0
176-177	SRDS_DIV_PEX_S1	2'h01
178-191	RESERVED	14'h0
192-195	PBI_SRC	4'h0F
196-200	BOOT_LOC	5'h18
201-201	BOOT_HO	1'h00
202-202	SB_EN	1'h00
203-211	IFC_MODE	9'h27
212-223	RESERVED	12'h0
224-226	HWA_CGA_M1_CLK_SEL	3'h06
227-229	RESERVED	3'h0
230-231	DRAM_LAT	2'h01
232-232	DDR_RATE	1'h00
233-263	RESERVED	31'h0
264-266	HOST_AGT_PEX	3'h00
267-287	RESERVED	21'h0

Bits	Description	Size'hvalue
288-319	GP_INFO	32'h82000300
320-356	RESERVED	37'h0
357-359	IRQ_EXT	3'h00
360-362	SPI_EXT	3'h00
363-365	RESERVED	3'h0
366-368	UART_BASE	3'h07
369-369	ASLEEP	1'h00
370-370	RTC	1'h01
371-371	SDHC_BASE	1'h01
372-372	IRQ_OUT	1'h00
373-381	IRQ_BASE	9'h00
382-383	SPI_BASE	2'h00
384-404	RESERVED	21'h0
405-405	IFC_GRP_E1_BASE	1'h00
406-406	IFC_GRP_E2_BASE	1'h00
407-407	IFC_GRP_D_BASE	1'h00
408-409	RESERVED	2'h0
410-411	IFC_GRP_B_BASE	2'h00
412-413	IFC_GRP_A_BASE	2'h00
414-415	RESERVED	2'h0
416-416	1588	1'h01
417-418	EC1	2'h00
419-420	EC2	2'h01
421-422	I2C3	2'h00
423-424	I2C4	2'h00
425-443	RESERVED	19'h0
444-444	DMA1	1'h00
445-445	SDHC	1'h00
446-447	DMA2	2'h00
448-508	RESERVED	61'h0
509-511	HWA_CGA_M2_CLK_SEL	3'h01

C.5 RCW #4 SBC314-T1042 Rev 1.1 1400 MHz 2 UART Mode

RCW #4 with preamble and CRC checksum GP_INFO set to 82 00 04 02

```
00000000: aa55 aa55 010e 0100 0c10 000e 0800 0000
00000010: 0000 0000 0000 0000 0000 0000 0040 4002
00000020: fc02 7000 2100 0400 0000 0000 8200 0402
00000030: 0000 0000 0003 303c 0000 0000 4001 5000
00000040: 0000 0000 0000 0000 0813 8040 f34b cef1
```

Decoded as follows:

Bits	Description	Size'hvalue
0-1	SYS_PLL_CFG	2'h00
2-6	SYS_PLL_RAT	5'h06
7-7	RESERVED	1'h0
8-9	MEM_PLL_CFG	2'h00
10-15	MEM_PLL_RAT	6'h10
16-23	RESERVED	8'h0
24-25	CGA_PLL1_CFG	2'h00
26-31	CGA_PLL1_RAT	6'h0E
32-33	CGA_PLL2_CFG	2'h00
34-39	CGA_PLL2_RAT	6'h08
40-95	RESERVED	56'h0
96-99	C1_PLL_SEL	4'h00
100-103	C2_PLL_SEL	4'h00
104-107	C3_PLL_SEL	4'h00
108-111	C4_PLL_SEL	4'h00
112-127	RESERVED	16'h0
128-135	SRDS_PRTCL_S1	8'h00
136-157	RESERVED	22'h0
158-158	FM1_MAC_RAT	1'h00
159-159	RESERVED	1'h0
160-161	SRDS_PLL_REF_CLK_SEL_S1	2'h00
162-167	RESERVED	6'h0
168-169	SRDS_PLL_PD_S1	2'h01
170-175	RESERVED	6'h0
176-177	SRDS_DIV_PEX	2'h01
178-179	RESERVED	2'h0
180-180	SRDS_DIV_AURORA	1'h00
181-182	RESERVED	2'h0
183-183	EMI1_MODE	1'h00
184-185	RESERVED	2'h0
186-187	DDR_REFCLK_SEL	2'h00
188-189	RESERVED	2'h0
190-191	DDR_FDBK_MUL	2'h02
192-195	PBI_SRC	4'h0F
196-200	BOOT_LOC	5'h18

Bits	Description	Size'hvalue
201-201	BOOT_HO	1'h00
202-202	SB_EN	1'h00
203-211	IFC_MODE	9'h27
212-223	RESERVED	12'h0
224-226	HWA_CGA_M1_CLK_SEL	3'h01
227-229	RESERVED	3'h0
230-231	DRAM_LAT	2'h01
232-232	DDR_RATE	1'h00
233-233	RESERVED	1'h0
234-234	DDR_RSV0	1'h00
235-241	RESERVED	7'h0
242-242	SYS_PLL_SPD	1'h00
243-243	MEM_PLL_SPD	1'h00
244-244	CGA_PLL1_SPD	1'h00
245-245	CGA_PLL2_SPD	1'h01
246-263	RESERVED	18'h0
264-266	HOST_AGT_PEX	3'h00
267-287	RESERVED	21'h0
288-319	GP_INFO	32'h82000402
320-320	RESERVED	1'h0
321-321	UC1_CTSB_CDB_SEL	1'h00
322-322	UC3_CTSB_CDB_SEL	1'h00
323-356	RESERVED	34'h0
357-359	IRQ_EXT	3'h00
360-362	SPI_EXT	3'h00
363-365	RESERVED	3'h0
366-368	UART_BASE	3'h06
369-369	ASLEEP	1'h00
370-370	RTC	1'h01
371-371	SDHC_BASE	1'h01
372-372	IRQ_OUT	1'h00
373-381	IRQ_BASE	9'h0F
382-383	SPI_BASE	2'h00
384-404	RESERVED	21'h0
405-405	IFC_GRP_E1_BASE	1'h00
406-406	IFC_GRP_E2_BASE	1'h00
407-407	IFC_GRP_D_BASE	1'h00
408-408	RESERVED	1'h0
409-409	IFC_GRP_C_BASE	1'h00
410-411	IFC_GRP_B_BASE	2'h00
412-413	IFC_GRP_A_BASE	2'h00
414-415	RESERVED	2'h0
416-416	1588	1'h00
417-417	SDHC	1'h01
418-419	EC1	2'h00
420-421	EC2	2'h00
422-423	I2C3	2'h00
424-425	I2C4	2'h00

Bits	Description	Size'hvalue
426-427	QE_TDMA	2'h00
428-429	QE_TDMB	2'h00
430-431	DVDD_VSEL	2'h01
432-433	L1VDD_VSEL	2'h01
434-435	LVDD_VSEL	2'h01
436-437	CVDD_VSEL	2'h00
438-439	EVDD_VSEL	2'h00
440-440	MAC2_GMII_SEL	1'h00
441-441	HDLC1_MODE	1'h00
442-442	HDLC2_MODE	1'h00
443-443	MDIO_MDC1	1'h00
444-445	DMA1	2'h00
446-447	DMA2	2'h00
448-511	RESERVED	64'h0

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