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INPUT TECHNICAL REPORTING FROM ICS

THE ICS-7002A FULL LENGTH DUAL PMC PCI CARRIER BOARD WITH PCI 2.2 64/66 BRIDGE, DUAL FPDP INTERFACES AND LVDS I/O

No. 51 Interactive Circuits and Systems Ltd.

INTRODUCTION

The ICS-7002A board is a full length PCI card capable of carrying two single-width PCI Mezzanine Card (PMC) modules. The board provides a PMC module carrier that allows the User I/O connectors of the two sites to be interconnected, or to be connected to external equipment in a flexible fashion.

It incorporates a PCI bridge capable of 64-bit 66 MHz operations on both its host and local sides. The bridge has the capability of asynchronous operation, i.e. local traffic (between PMC sites) can operate in 64-bit 66 MHz mode regardless of the host slot operating mode.

The ICS-7002A connects the Pn4 (User I/O) connectors of the two PMC sites independently to a 1 million gate FPGA. These connections support LVDS signals. Two 80-pin KEL cable connectors on the top surface of the board, provide ANSI/VITA 17 FPDP connections to the FPGA. One of these is configured as an input (FPDP/RM) while the other is configured as an output (FPDP/TM).

The ICS-7002A provides a cooling fan for each PMC site and engineering test points to the FPGA.

GENERAL DESCRIPTION

The PCI bridge used on the ICS-7002A is the PLX PCI 6154. This transparent host bridge can work asynchronously, so that the local side can operate using a local 66 MHz clock frequency even if the host side is operating at 33 MHz. Since the bridge is transparent, no software driver is required when using the board.

Fig. 2 shows a block diagram of the ICS-7002A.

All 64 wires of the PMC site Pn4 (User I/O) connectors are independently wired to the FPGA using LVDS paired and (optionally) terminated signals to allow for high speed parallel data path between the two sites, or between each site and the I/O connectors.

The I/O connectors are configured for use as FPDP ports on the standard board, but may be reconfigured for LVDS signals or for other purposes. Contact the factory for details.

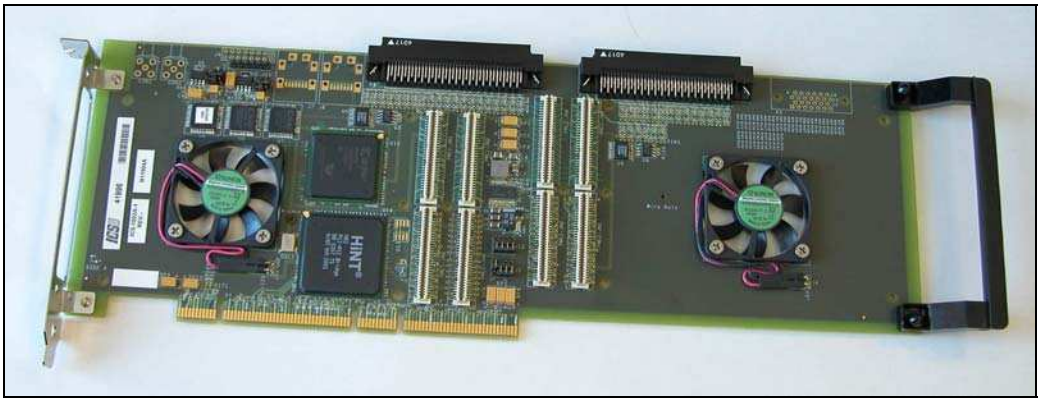


Figure 1 - ICS-7002A Dual PMC PCI Carrier

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Jumpers (wire links) on the board may be set to determine how data flow occurs on the board. The standard options available are as given in Table I below.

Table I – ICS-7002A I/O Modes

Mode	Pn4 Operation
1	PMC 1 to PMC 2
2	PMC 2 to PMC 1
3	PMC 1 to FPDP Out FPDP In to PMC 2
4	PMC 2 to FPDP Out FPDP In to PMC 1

The FPGA may be customized for changes of functionality to the Pn4 and FPDP connections. Contact the factory for details.

The standard board is configured for 3.3V signaling on both PMC sites. As an ordering option, the board may be configured for 5V signaling, for use with one or more PMC modules that support only 5V signaling. Contact the factory for details

The host PCI slot must provide +3.3V power to the board.

ORDERING CODES

The order code for the standard product is given below. Modified versions providing different functionality can be supplied on request. Contact the factory for details.

ICS-7002A-1 PMC to PCI Carrier with fans. Full length PCI, 66 MHz/64-bit PCI interface, 3.3V signalling. One FPDP input, one FPDP output.

ICS-7002A SPECIFICATIONS	
Format	PCI long card
PCI Bus Interface:	PCI 2.2 64-bit, 66MHz, universal signaling (PLX6154)
PMC Interface	PCI 2.2 64-bit, 66MHz 3.3V signaling (standard product) 5 V signaling option*
Other I/O	ANSI/VITA 17 Front Panel Data Port (FPDP), two connectors located on top edge of card FPDP/TM (one connector) FPDP/RM (one connector)
User Programmable I/O	64 I/Os (each) from Pn4 connectors of PMC sites to FPGA
User Programmable FPGA	1+ MGate
Environmental:	
Operating Temp:	0- 50 degreesC (at entry point of forced air)
Storage Temp:	-40 - +85 degrees C
Humidity:	95% non-condensing
Power:	+5V @ 0.4 Amps
	+3.3V @ 0.4 Amps
	(Requirement of PMC modules not included)

** Requires population of respective Key and Vio jumpers.*

Specifications are subject to change without notice

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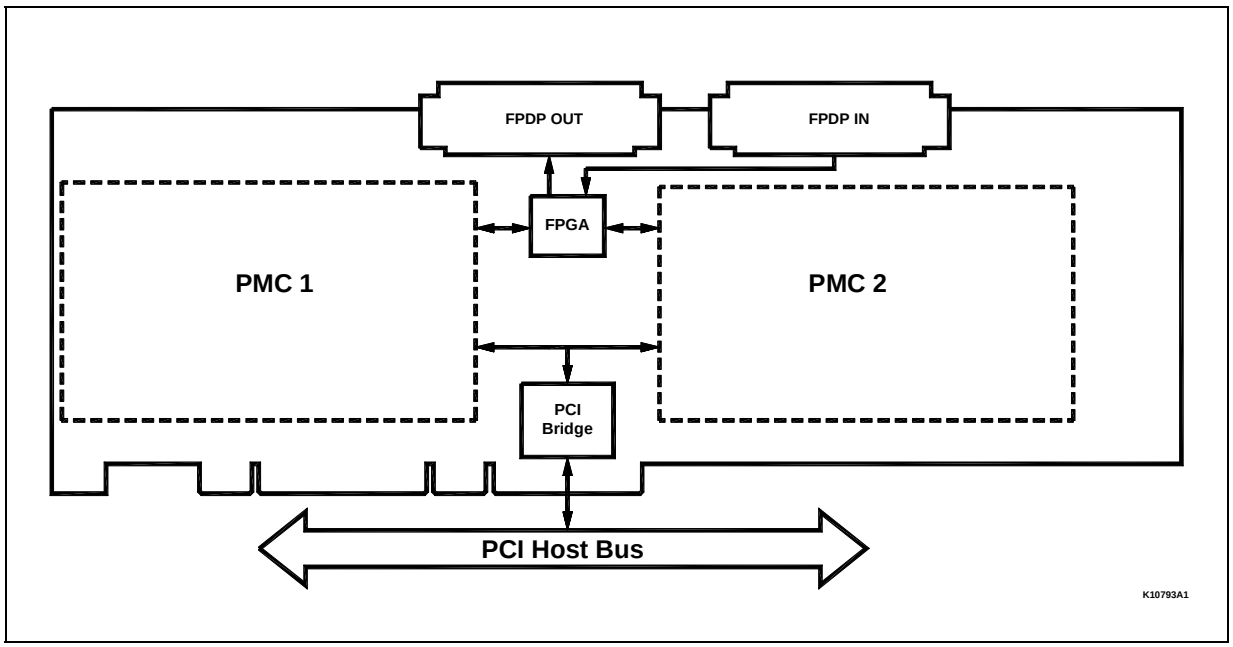


Figure 2 - ICS-7002A Block Diagram

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