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Hardware Reference Manual

PEX430

Edition 1QD

Publication No. PEX430-0HH/1QD



abaco SYSTEMS

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Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems Limited is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems Limited will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

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1 • Introduction

The Abaco Systems PEX430 is an XMC and PMC carrier-card based on the 3U VPX form factor. The PEX430 can also be used as a PCI Express switch.

Figure 1-1 PEX430



1.1 Features

- 16 lanes of external PCI express
- PMC carrier
- PCI Express to PCI bridge
- 4 lanes of PCI Express to PCI bridge
- Flexible lane options
- XMC carrier
- 8 lanes of PCI Express to XMC
- Configurable Non-Transparent port

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1.2 Conventions

This manual may use the following types of notice:



WARNING

Warnings alert you to the risk of personal injury.



CAUTION

Cautions alert you to system damage or loss of data.



NOTE

Notes call attention to important features or instructions.



TIP

Tips give guidance on procedures that may be tackled in a number of ways.



LINK

Links take you to other documents or websites. The purple link color may also be used within a body of text or paragraph to indicate a link (or hyperlink) to a different part of the same document.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$ respectively. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.



NOTE

When describing transfer rates, “k”, “M” and “G” mean $x10^3$, $x10^6$, and $x10^9$ - not $x2^{10}$, $x2^{20}$, and $x2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the LSB and n is the MSB.

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high.

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1.3 Safety Notices

1.3.1 Safety Summary

Observe the following general safety precautions during operation of this equipment. Failure to comply with these precautions or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Abaco Systems Inc. assumes no liability for the user's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Abaco is aware. Take note of these warnings and take all other safety precautions necessary for the safe operation of the equipment in your operating environment.

1.3.2 Power Supplies



WARNING

Do not exceed 7A supply current – a fuse or circuit breaker must be fitted.

Do not reverse bias the input supply.

Power supply problems should be dealt with only by qualified personnel.

1.3.3 Backplane Requirements



CAUTION

Only use the PEX430 in backplanes that supply power on both the J1 and J2 connectors.

1.3.4 Flammability

All Abaco circuit boards are manufactured by UL- recognized/approved manufacturers and have a flammability rating of 94V-1.

1.3.5 EMI/EMC Regulatory Compliance



CAUTION

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

Abaco Systems Ltd boards are designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

Abaco Systems Ltd boards also comply with EN60950 (product safety).

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1.3.6 Heatsink



CAUTION

Do not remove the heatsink.

There are ***no*** user-alterable components underneath the heatsink, so users should have no reason to remove it.

Users should not attempt reattachment of the heatsink, as this requires precise torque on the screws attaching the heatsink to the PCB. Over-tightening the screws may cause the heatsink to damage components beneath it (e.g. the main PowerPC processor). Removal and re-attachment of the heatsink should only be carried out by Abaco.

1.4 Abaco Systems Website

You can find information on Abaco products on the following website:



LINK

https://www.abaco.com

1.5 Abaco Documents

You may register for access to manuals via the website whose link is given above.

1.6 Technical Support

You can find technical assistance contact details on the website Embedded Support page.



LINK

https://www.abaco.com/embedded-support

Abaco will log your query on the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:



LINK

support@abaco.com

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1.7 Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.



LINK

https://www.abaco.com/embedded-support

Do not return products without first contacting the Abaco Repairs facility.

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2 • Identification and Inspection

2.1 Product Identification

The PEX430 is identified by labels at strategic positions. You can cross-check these against the Advice Note provided with your delivery.

Identification labels, similar to this, attached to the shipping box and the antistatic bag provide identical information: product code, product description, equipment number and board revision.



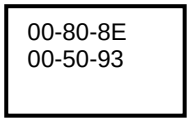
On the board within the antistatic bag, there is an identifying label similar to this attached to the printed wiring board.



On conduction-cooled versions of the board (build levels 4 and 5), there is also a label similar to this attached to the front panel.



A label, similar to this, giving the board's hardware Ethernet or MAC address is also attached to the printed wiring board.



See the Product Code Information section in Appendix A for more details

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2.2 Inspection

When handling the PEX430, observe antistatic precautions.



Visually examine the PEX430 for any physical damage.

If the PEX430 is not received in perfect physical condition, report this to Abaco immediately.

There are no user-alterable hardware configuration settings on the PEX430.

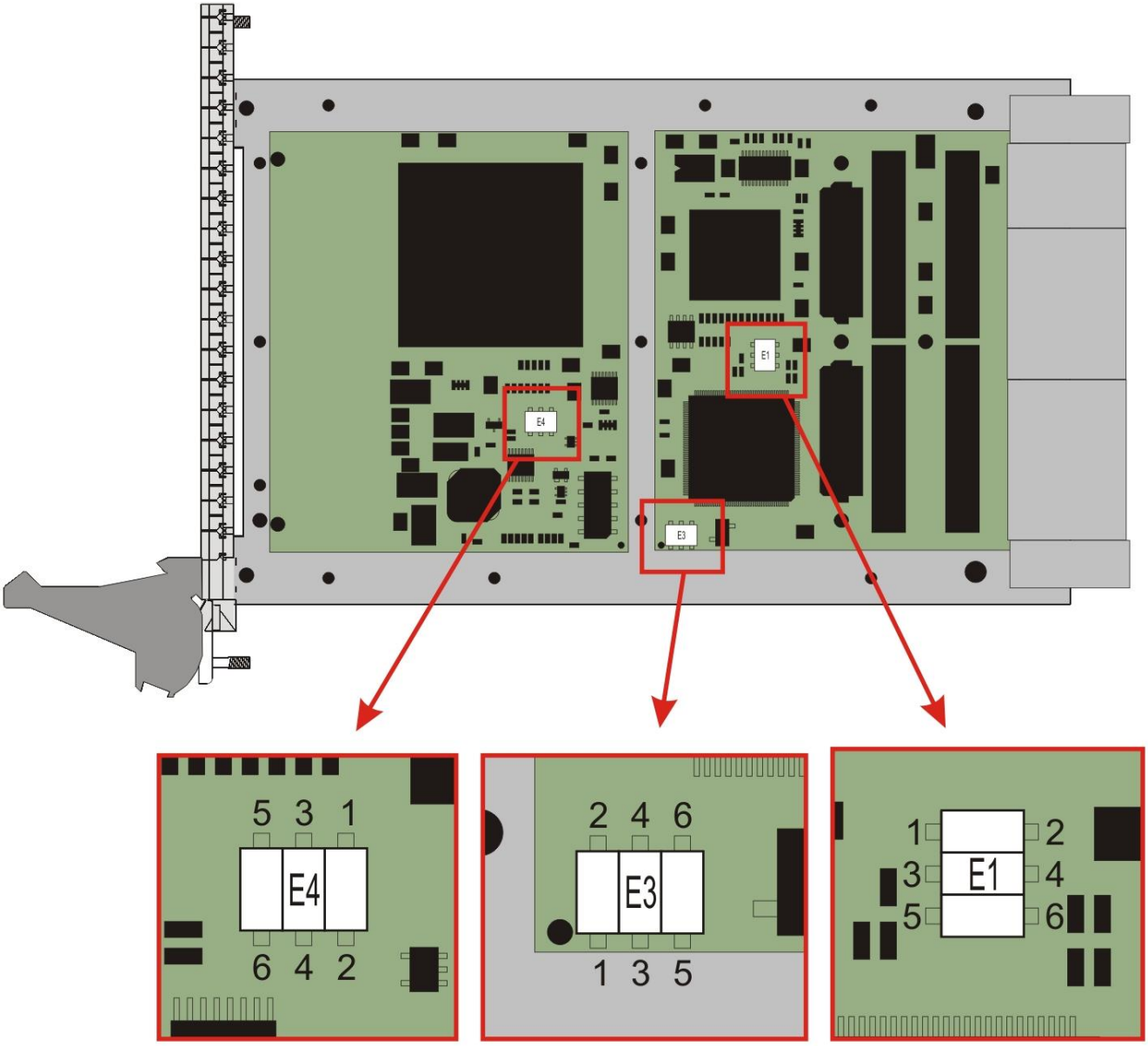
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3 • Configuration and Power-Up

3.1 Configuration

The PEX430 is highly configurable. Jumpers enable the board to be configured sufficiently to permit basic operation with *most* system configurations. More detailed configuration is possible by the use of in-system programming of on-board EEPROMs. Figure 3-1 shows the location of the configuration jumpers.

Figure 3-1 Configuration Links



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Table 3-1 shows that the PEX430 can be manually configured for a number of different operating conditions and that, in some cases, the jumpers can have more than one function; the operation of the jumpers being altered by the state of some external signals, for instance. The following sections describe the available functions and which jumpers are associated with each function.

Table 3-1

Link	Section for Information	Function(s)
E1	3.1.1 3.1.3 3.1.4	PMC Clock Over-ride PCI Express Upstream Port PMC X100 Selection
E3	3.1.2 3.1.4 3.1.5	PCI Express Port Lane configuration PMC X100 Selection PEX430 Switch and Bridge EEPROM Hold
E4	3.1.6	JTAG Chain

CAUTION

Unless specifically noted in this manual, jumpers should not be changed while the board is powered.

NOTE

The PEX430 can be configured for XMC I/O or PMC I/O. This configuration is a build time option and the appropriate PEX430 needs to be ordered.

3.1.1 PMC Clock Override (E1)

Normally, the PMC clock frequency will be selected automatically by the fitting of a PMC. However, it is possible to override this setting manually.

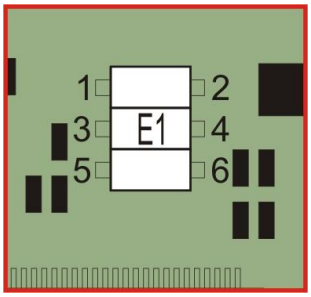


Table 3-2

E1 Pins 3-4	E1Pins 5-6	E1 Pins 1-2	Operation	Notes
Open	Don't Care	Don't Care	PMC determines the PMC clock frequency	Default configuration
Closed	Open	Open	Force 133 MHz operation	
Closed	Open	Closed	Force 100 MHz operation	
Closed	Close	Open	Force 66 MHz operation	
Closed	Closed	Closed	Force 33 MHz operation	

CAUTION

These jumpers are also used for setting the PCI Express upstream port configuration. It should be noted that even if these jumpers are being used for PCI Express upstream configuration the PMC clock frequency will also be changed (See 3.1.3).

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3.1.2 PCI Express Port Lane Configuration (E3)

The PEX430 has a number of different PCI Express lane options, the configuration of which is set up as shown in Table 3-3.

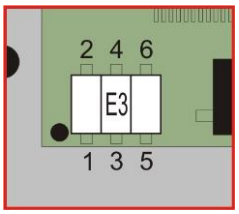
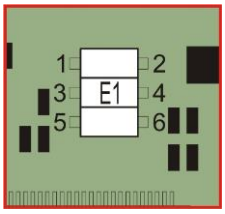


Table 3-3

E3 Pins 5-6	E3 Pins 3-4	PCI Express Lane Configuration				Notes
		Port 0	Port 1	Port 2	Port 3	
Open	Open	X4	X4	X4	X4	Default Configuration
Open	Closed	X8	X8	X0	X0	
Closed	Open	X8	X4	X4	X0	
Closed	Closed	X8	X4	X2	X2	

3.1.3 PCI Express Upstream Port Configuration (E1)

Using E1 to change the configuration of the upstream port enables the user to set the PEX430 into a basic mode that suits their application, and enables them to program the settings they require into the on-board EEPROM.



NOTE

It is not expected that jumpers will be used to permanently change the upstream port.
A user will normally configure the PEX430 to use another upstream port using the jumpers, and then this configuration will be programmed into the EEPROM.
Subsequently, the jumpers can be removed and the board will be set to boot using the values stored in the EEPROM. There is an option to ignore the EEPROM should the contents become corrupt or unsuitable for a particular application.
Programming the EEPROM requires an application to be run on the SBC that is connected to the PEX430.

Table 3-4

Backplane NVMRO	PEX430 E1 Pins 3-4	PEX430 E1 Pins 5-6	PEX430 E1 Pins 1-2	Description
1	Don't Care	Don't Care	Don't Care	Upstream port is the default Port 0
0	Open	Don't Care	Don't Care	Upstream port is set to Port 0
0	Closed	Open	Open	Upstream port is set to Port 0
0	Closed	Open	Closed	Upstream port is set to Port 1
0	Closed	Closed	Open	Upstream port is set to Port 2
0	Closed	Closed	Closed	Upstream port is set to Port 3

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CAUTIONS

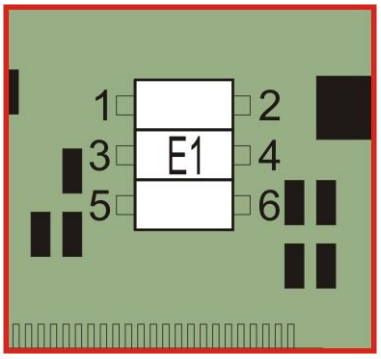
While these jumpers are fitted the PMC clock frequency will be over-ridden with the frequency selected by the jumpers (see 3.1.1). It is not expected that this will be an issue since the setting of the upstream port is expected to be done during a configuration operation on the PEX430 and not for normal operation.

Depending on how the NVMRO signal for the PEX430 is connected to the NVMRO signal for other VPX cards all the non-volatile memory devices in the system could be put into a writable state.

It is possible to set the upstream port to a port that is not configured. For example, if the ports are set up in x8 x8 x0 x0 mode then only Ports 0 and 1 are valid ports (the other two ports have a zero lane width). In this case, if the upstream port was set for Port 2 (or 3) then no upstream port will be enabled.

3.1.4 PMC X100 Selection (E1 and E3)

The PEX430 supports the operation of a PMC card with PCIX capability. It is possible to configure the operation of the PCIX PMC card for either 100 MHz or 133 MHz operation using Jumper E3 pins 1-2, as shown in Table 3-5.



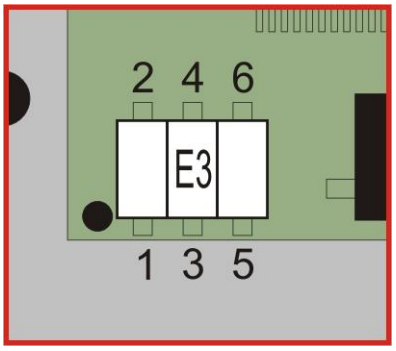


Table 3-5

PEX430 E1 Pins 3-4	PEX430 E3 Pins 1-2	Description
Open	Open	• PMC clock will be set to 100 MHz PCIX mode (if PMC supports PCIX operation)
Open	Closed	• PMC clock will be set to 133 MHz PCIX mode if PMC supports PCIX operation)
Closed	Don't Care	• PMC clock will be set manually by other E1 jumpers

NOTE

If a PMC card that does not have PCIX capability is fitted, then jumper E3 pins 1-2 has no effect.

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3.1.5 PEX430 Switch and Bridge EEPROM Hold (E3)

Jumper E3 pins 1-2 sets the switch and bridge EEPROMs into a hold mode so that the switch or bridge cannot access them.

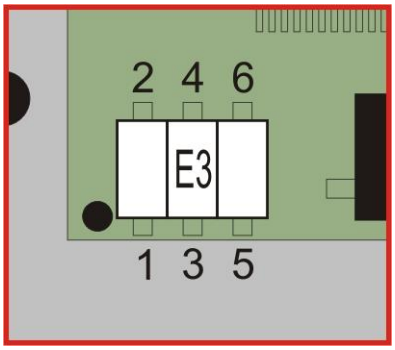


Table 3-6

Backplane NVMRO	PEX430 E3 Pins 1-2	Description
1	Don't Care	• EEPROMs not in Hold mode • EEPROMs read only
0	Closed	• EEPROMs in Hold mode • EEPROMS not writable • Stage 1 of recovery mode (see Note)
0	Open	• EEPROMs not in Hold mode • EEPROMs writable • Stage 2 of recovery mode (see Note)

If the VPX NVMRO signal is logic low – i.e. the on-board's non volatile memories are in the read/write mode, the jumper can be used to control the hold signal of the two EEPROMs. This one signal controls the hold state of both EEPROMs.

NOTE

Recovery mode is described in Section 4.2.1

CAUTIONS

Depending on how the NVMRO signal for the PEX430 is connected to the NVMRO signal for other VPX cards all the non-volatile memory devices in the system could be put into a writable state.

Jumper E3 pin 1-2 is also used for setting the PCIX PMC card (see Section 3.1.4).

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3.1.6 JTAG Chain (E4)

The PEX430 includes a JTAG test chain. There is an option either to use the full JTAG test chain or to reduce the chain to program the CPLD.

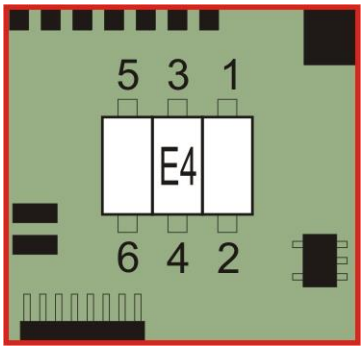


Table 3-7

PEX430 E4 Pins 1-2	PEX430 E4 Pins 3-4	Description
Open	Open	• JTAG Chain is incomplete
Open	Closed	• Short JTAG Chain – used for CPLD Programming
Closed	Open	• Full JTAG Chain – used for JTAG testing
Closed	Closed	• Invalid option – DO NOT USE

3.2 Power-Up

The PEX430 does not have any specific power supply start up sequence requirements.

The PEX430 requires a 5 volt DC supply to operate. The 5 volt supply is the main power supply and will need to be of sufficient power for the proper operation of the PEX430. The PEX430 produces all other supplies required for proper operation internally.

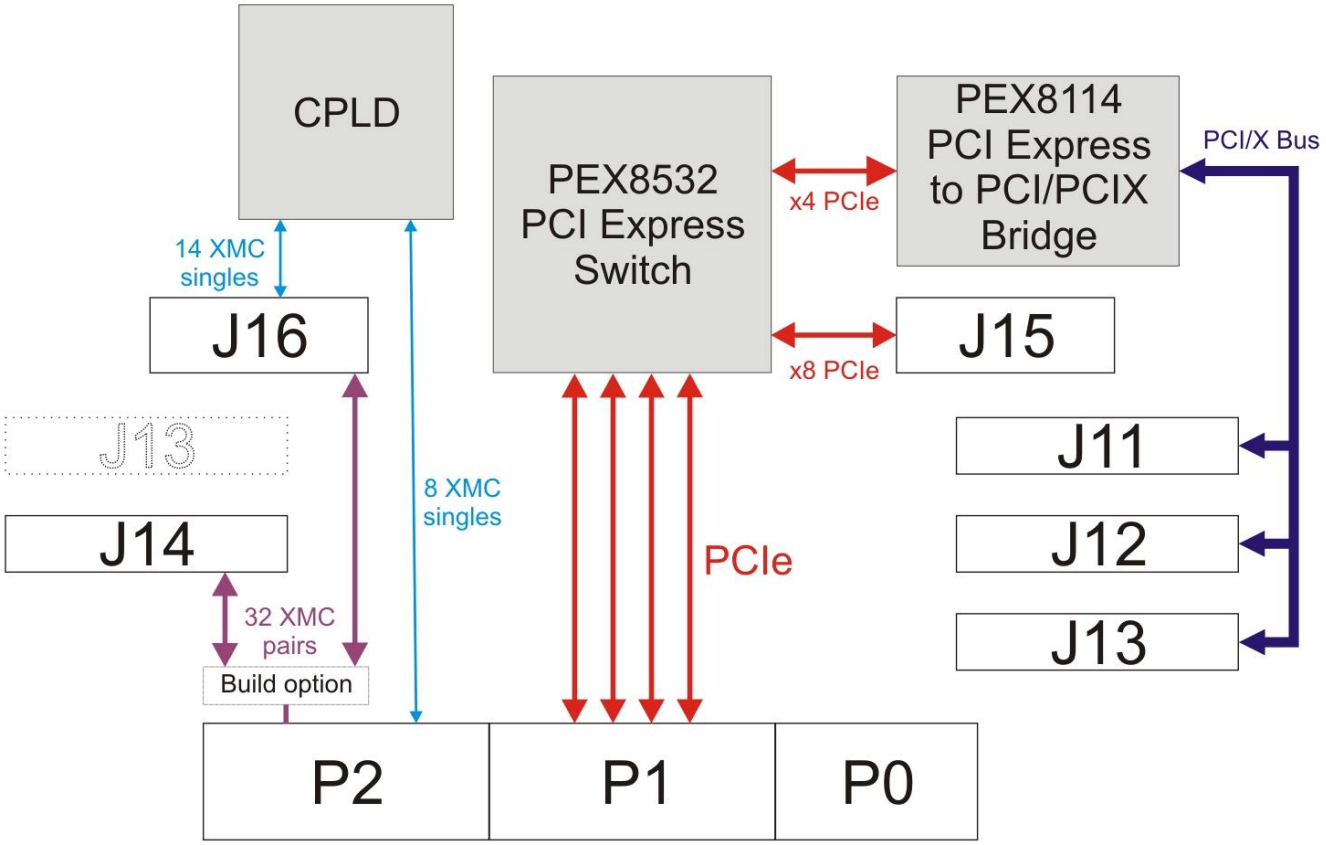
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4 • Functional Description

4.1 Functional Overview

The PEX430 is a PMC and XMC carrier and PCI Express (PCIe) switch card. It provides a PCIe switch function between devices connected to the VPX connector, the XMC connectors and a bridging function to PCI/PCIX devices connected to the PMC connectors.

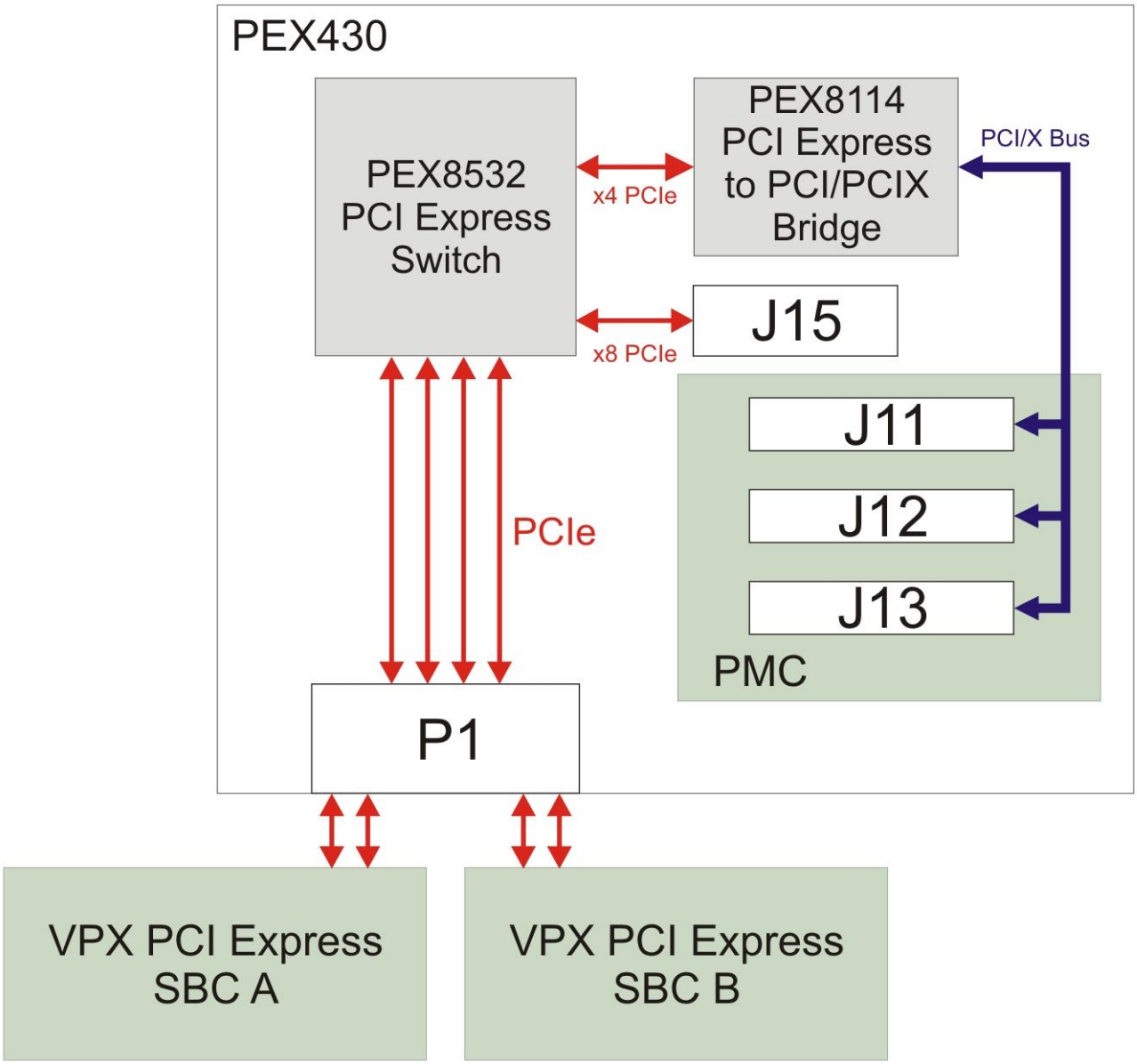
Figure 4-1 Functional Block Diagram



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4.1.1 System Example

Figure 4-2 System Block Diagram



In this example system, the PEX430 acts as a PCIe switch between the two VPX PCIe SBCs; thereby allowing the two SBCs to communicate with each other. In this example the SBCs will be connected to the PEX430 configured to have 2 ports with 8 lanes in each port. One of these ports would normally be expected to be set to Non-Transparent mode in this case. In addition, if the PEX430 has been configured for operation as an XMC carrier the PEX430 acts as a PCIe switch between the SBCs and any PCIe device fitted to the XMC site. If the PEX430 had been configured for operation as a PMC carrier the PEX430 would act as a PCIe switch and provide a bridging function to PCI/PCIX devices on the PMC site instead of acting as a switch to the XMC site.

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4.1.2 VPX PCI Express Port

The PEX430 has a PCI Express (PCIe) connection to the VPX connectors. This interface can be configured in a number of different ways as described in the table below. One of these ports in each case will be configured as the upstream port. One of these ports in each case can be configured as a Non-Transparent port. This allows the memory spaces of two connected systems to remain isolated by presenting the processor as an end point. If one of these ports is configured as a non-transparent port then there can be either a single upstream port or two upstream ports (one transparent port and one non-transparent).

Table 4-1

Port 0	Port 1	Port 2	Port 3
x16 lane	x0 lane	x0 lane	x0 lane
x8 lane	x8 lane	x0 lane	x0 lane
x8 lane	x4 lane	x4 lane	x0 lane
x8 lane	x4 lane	x2 lane	x2 lane
x4 lane	x4 lane	x4 lane	x4 lane

Ports can be configured as transparent or non transparent in the following combinations:

- Single transparent port
- Single non transparent port
- Single transparent port and single non transparent port

By default the PEX430 is configured as 4 ports each with 4 lanes with Port 0 as a transparent port. The setting of the PEX430 with a non-transparent port requires the use of configuration data stored in the associated EEPROM.

For a PEX430 set up for x4 x4 x4 x4 lane operation Port 0 corresponds to the 4 lanes described as Channel A. For a PEX430 set up for x8 x8 x0 x0 or x8 x4 x4 x0 or x8 x4 x2 x2 Port 0 corresponds to the 8 lanes described as Channel A and Channel B combined.

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4.1.3 PCI Express Switch

The PCI Express (PCIe) switch function is performed by a PLX PEX8532. This device provides 2.5 Gbps per lane (5 Gbps per lane full duplex) of aggregated bandwidth. The non-blocking internal crossbar architecture supports full wire speed, and provides a maximum payload size of 256 Bytes.

On the PEX430 the PEX8532 has 16 lanes connected to the VPX connector, 8 lanes connected to the XMC connector and 4 lanes connected to the PCIe to PCI/PCIX bridge. The 16 lanes connected to the VPX connector can be configured in several different ways as described earlier. One of the PEX8532 ports connected to the VPX connector can be configured for Non-Transparent mode. The setting of the PEX430 with a non-transparent switch port requires the use of configuration data stored in the associated EEPROM. All the ports connected to the VPX connector support lane reversal, and also support auto-width negotiation enabling the PEX430 to be connected to systems supporting lower lane widths.

It should be noted that if the PEX430 is connected so that for example two 4 lane ports are connected to a single 8 lane device the link may fail to negotiate. In this case the PEX430 should be reconfigured to present an 8 lane port or the second 4 lane port should be physically disconnected.

4.1.4 PCI Express to PCI/PCIX Bridge

The PCIe to PCI/PCIX bridge function is performed by a PLX PEX8114. The PEX8114 interfaces to the PCIe bus (via the PCIe switch) with up to 4 PCIe lanes, allowing a maximum 2.5 Gbps per lane bit rate. The other side of the bridge is either PCI or PCIX supporting a 32 bit or a 64-bit wide data path running at up to 133 MHz; giving bandwidths up to 8 Gbps.

The PEX430 supports the use of the PEX8114 in forward bridge mode. In this mode configuration accesses are sent from the PCI Express root complex.

The PEX8114 can operate in Transparent or Non-transparent mode. In Non-Transparent mode the bridge isolates the processor domains on each side. Data transfers between domains occurs using address translation. In Non-Transparent mode configuration accesses occur on both the PCI/PCIX bus and the PCIe port. There are two ‘hosts’ in this configuration and each can access or send data to devices on both sides of the bridge. Each host has its own memory map for the devices to which it has access. The setting of the PEX430 with a non-transparent bridge port requires the use of configuration data stored in the associated EEPROM.

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4.1.5 Differential I/O Signals

The PEX430 can be configured (at build time only) to connect 32 differential signal I/O to the XMC P16 connector or the PMC P14 connector. This configuration is done by populating different options of zero ohm links.

4.1.6 Single Ended I/O Signals

The PEX430 can be configured (at design time only) to connect up to 6 single ended I/O signals to any of up to 14 pins on the XMC P16 connector. This configuration is done using a CPLD.

4.2 Configuration EEPROMs

The PEX430 includes an EEPROM for configuration data for the PCI Express switch (PEX8532) and an EEPROM for configuration data for the PCI Express-to-PCI bridge (PEX8114). These EEPROMs can be programmed 'in-system' with suitable software running on an SBC that is connected to the upstream port.

The switch and bridge devices are configured either by 'strapping' options (see below) or at power up from data in the EEPROMs:

- If the EEPROMs are blank, or if they are in a Hold mode, the operation of the PEX8532 and PEX8114 is controlled by options set by the CPLD and jumpers, i.e. 'strapping'
- If the EEPROMs have valid configuration data and they are not in a Hold mode, the operation of the PEX8532 and PEX8114 is controlled by the data programmed into the EEPROMs

4.2.1 Recovery Mode

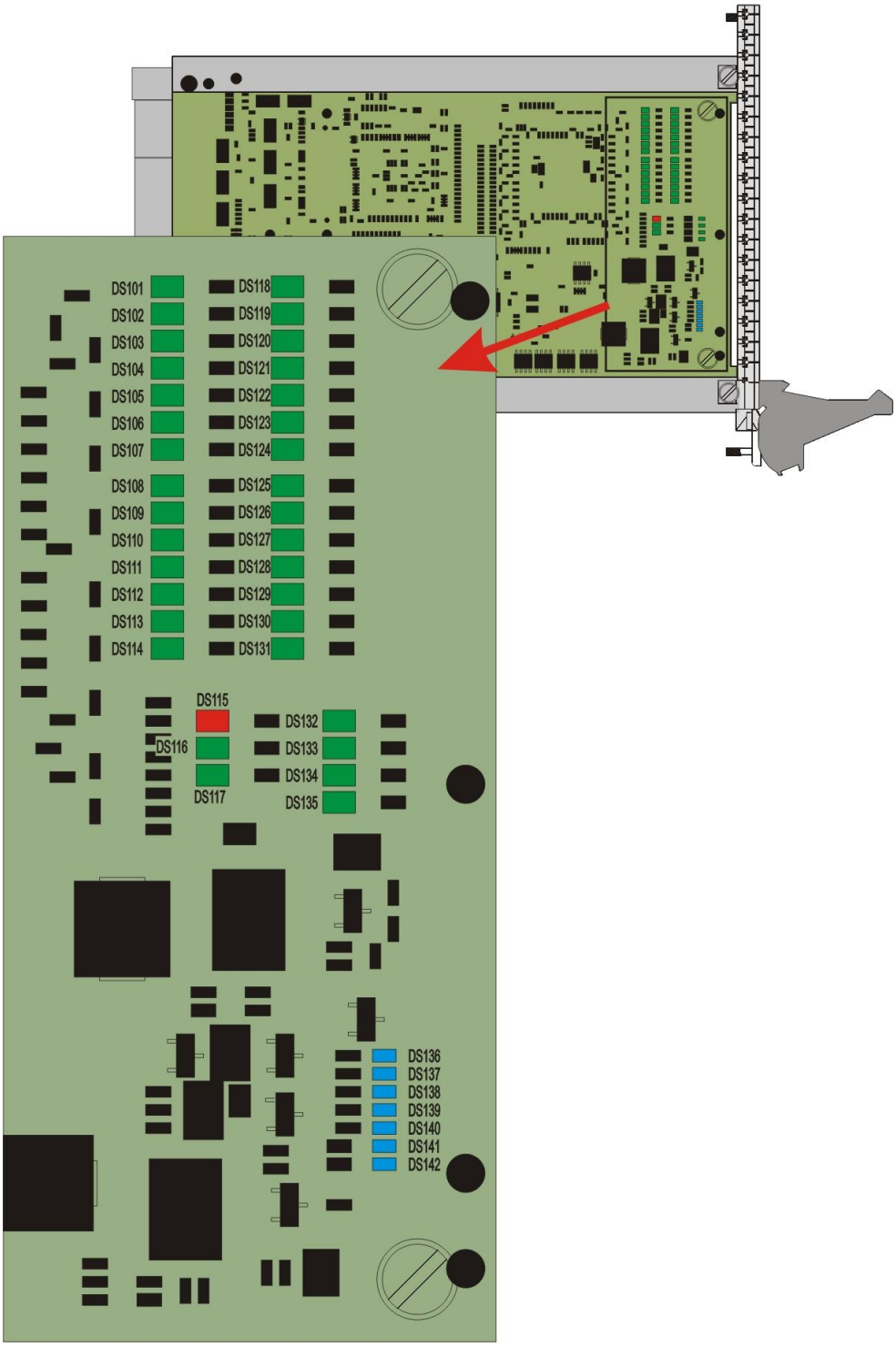
To recover a system with faulty or inappropriate EEPROM contents, the PEX430 should be powered up with the NVMRO signal from the backplane in a logic low state and jumper E3 pins 1-2 closed (see 3.1.5). This puts the EEPROMs into a hold condition during the boot up phase, which prevents the switch and bridge from using the EEPROM contents for configuration. Without cycling the power to the PEX430 remove the jumper form E3 pins 1-2. This removes the hold condition and allows the EEPROM to be over-written or erased.

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4.3 LEDs

The LEDs on the PEX430 are shown in Figure 4-3. The LEDs are highlighted on this diagram in the colour of the LED. Additional drawings are included to highlight the individual functions of the LEDs.

Figure 4-3 LEDs



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4.3.1 PCI Express Switch > PCI to PCI Express Bridge

These LEDs indicate the status of the PCI Express link between the PCI Express switch and the PCI to PCI Express bridge.

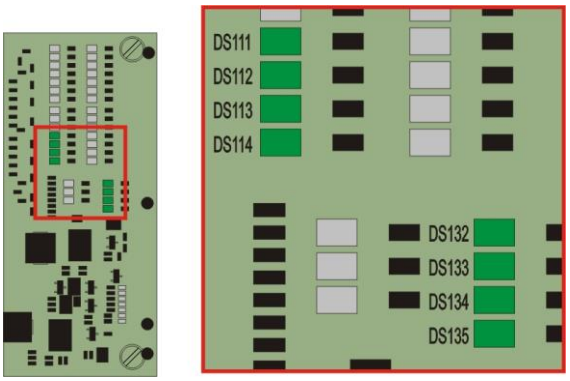


Table 4-2

PCI Express Switch				PCI-PCI Express Bridge				Width of Link (Lanes)
DS111	DS112	DS113	DS114	DS132	DS133	DS134	DS135	
On	On	On	On	On	On	On	On	4

4.3.2 PCI Express Switch > VPX Connectors – Channel A

These LEDs indicate the status of some of the PCI Express links between the PCI Express switch and the VPX connectors. The LEDs indicated in this diagram correspond to Channel A of the PEX430.

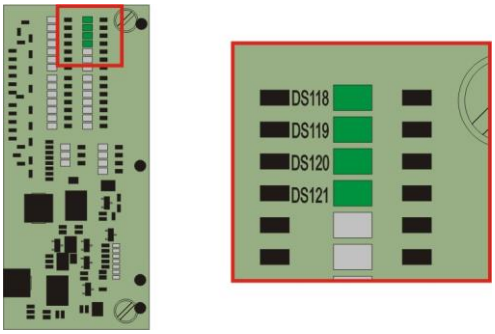


Table 4-3

Channel A				Width of Link (Lanes)
DS118	DS119	DS120	DS121	
On	On	On	On	4
On	On			2
On				1
		On	On	2 (with lane reversal)
			On	1 (with lane reversal)

NOTE

When the PEX430 is in a x4 x4 x4 x4 configuration, Channel A corresponds to Port 0.

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4.3.3 PCI Express Switch > VPX Connectors – Channel B

These LEDs indicate the status of some of the PCI Express links between the PCI Express switch and the VPX connectors. The LEDs indicated in this diagram correspond to Channel B of the PEX430.

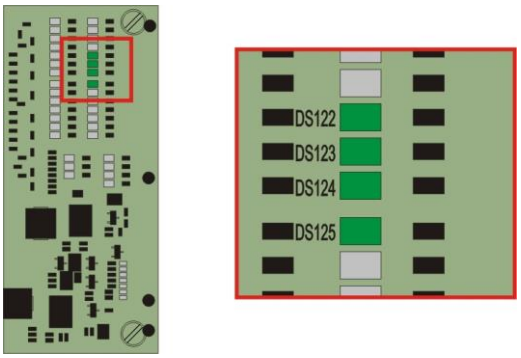


Table 4-4

Channel B				Width of Link (Lanes)
DS122	DS123	DS124	DS125	
On	On	On	On	4
On	On			2
On				1
		On	On	2 (with lane reversal)
			On	1 (with lane reversal)

NOTE

When the PEX430 is in a x4 x4 x4 x4 configuration Channel B corresponds to the Port 1.

When the PEX430 is in a x8 x8 x0 x0 or x8 x4 x2 x2 configuration Channel A and Channel B LEDs are combined to give an indication of the status of the link with a maximum width of 8.

NOTE

When the PEX430 is in a x8 x8 x0 x0, or a x8 x4 x2 x2, configuration Channel A combined with Channel B corresponds to the Port 0.

Table 4-5

Channel A				Channel B				Width of Link (Lanes)
DS118	DS119	DS120	DS121	DS122	DS123	DS124	DS125	
On	On	On	On	On	On	On	On	8
On	On	On	On					4
On	On							2
On								1
				On	On	On	On	4 (with lane reversal)
						On	On	2 (with lane reversal)
							On	1 (with lane reversal)

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4.3.4 PCI Express Switch > VPX Connectors – Channel C

These LEDs indicate the status of some of the PCI Express links between the PCI Express switch and the VPX connectors. The LEDs indicated in this diagram correspond to Channel C of the PEX430.

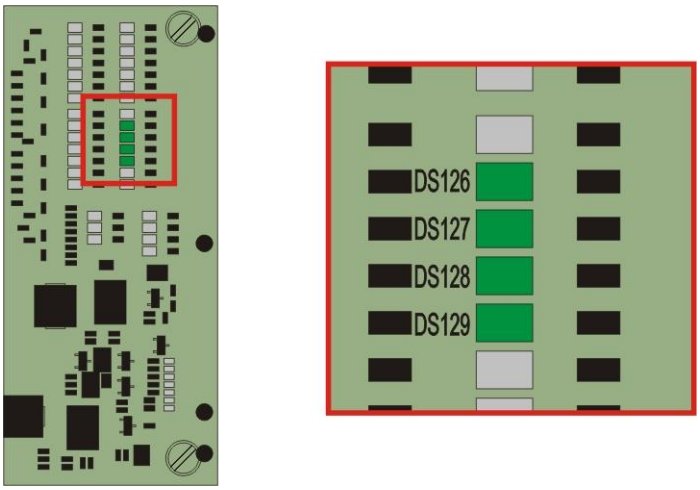


Table 4-6

Channel C				Width of Link (Lanes)
DS126	DS127	DS128	DS129	
On	On	On	On	4
On	On			2
On				1
		On	On	2 (with lane reversal)
			On	1 (with lane reversal)

NOTE

When the PEX430 is in a x4 x4 x4 x4 configuration Channel C corresponds to Port 2.

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4.3.5 PCI Express Switch > VPX Connectors – Channel D

These LEDs indicate the status of some of the PCI Express links between the PCI Express switch and the VPX connectors. The LEDs indicated in this diagram correspond to Channel D of the PEX430.

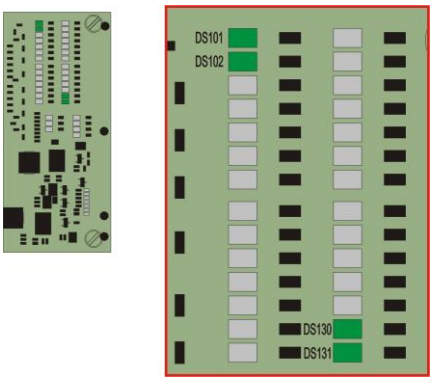


Table 4-7

Channel D				Width of Link (Lanes)
DS130	DS131	DS101	DS102	
On	On	On	On	4
On	On			2
On				1
		On	On	2 (with lane reversal)
			On	1 (with lane reversal)

NOTE

When the PEX430 is in a x4 x4 x4 x4 configuration Channel D corresponds to Port 3.

When the PEX430 is in a x8 x8 x0 x0 configuration Channel C and Channel D LEDs are combined to give an indication of the status of the link with a maximum width of 8.

NOTE

When the PEX430 is in a x8 x8 x0 x0 configuration, Channel C combined with Channel D corresponds to Port 1.

Table 4-8

Channel C				Channel D				Width of Link (Lanes)
DS126	DS127	DS128	DS129	DS130	DS131	DS101	DS102	
On	On	On	On	On	On	On	On	8
On	On	On	On					4
On	On							2
On								1
				On	On	On	On	4 (with lane reversal)
						On	On	2 (with lane reversal)
							On	1 (with lane reversal)

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When the PEX430 is in a x16 x0 x0 x0 configuration Channel A, Channel B, Channel C, and Channel D LEDs are combined to give an indication of the status of the link with a maximum width of 16.

NOTE

When the PEX430 is in a x16 x0 x0 x0 configuration, Channel A, combined with Channel B, combined with Channel C, combined with Channel D - corresponds to Port 0.

Table 4-9

Channel A				Channel B				Channel C				Channel D				Width of Link (Lanes)
DS118	DS119	DS120	DS121	DS122	DS123	DS124	DS125	DS126	DS127	DS128	DS129	DS130	DS131	DS101	DS102	
On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	16
On	On	On	On	On	On	On	On									8
On	On	On	On													4
On	On															2
On																1
								On	On	On	On	On	On	On	On	8 (with lane reversal)
												On	On	On	On	4 (with lane reversal)
														On	On	2 (with lane reversal)
															On	1 (with lane reversal)

4.3.6 PCI Express Switch > XMC Connectors

These LEDs indicate the status of the PCI Express links between the PCI Express switch and the XMC connectors.

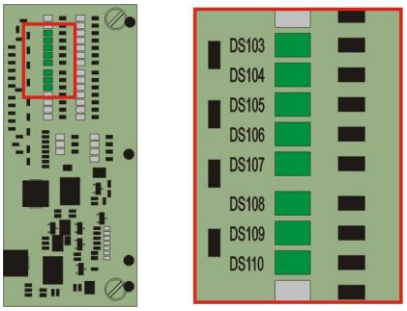


Table 4-10

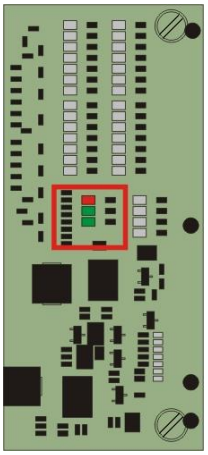
PCI Express Switch								Width of Link (Lanes)
DS103	DS104	DS105	DS106	DS107	DS108	DS109	DS110	
On	On	On	On	On	On	On	On	8
On	On	On	On					4
On	On							2
On								1
				On	On	On	On	4 (with lane reversal)
						On	On	2 (with lane reversal)
							On	1 (with lane reversal)

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4.3.7 PMC Clock Frequency

These LEDs have multiple functions as described below.

Normally, these LEDs indicate the clock frequency of the PMC. The PMC clock frequency can be set by the PMC or it can be manually over-ridden buy the use of jumpers on E1 (see 3.1.1).



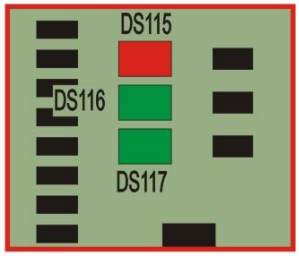


Table 4-11

DS115	DS116	DS117	Clock Frequency Operation
	On	On	133 MHz operation (PMC controlled)
		On	100 MHz operation (PMC controlled)
	On		66 MHz operation (PMC controlled)
			33 MHz operation (PMC controlled)
On	On	On	133 MHz operation (Configured control)
On		On	100 MHz operation (Configured control)
On	On		66 MHz operation (Configured control)
On			33 MHz operation (Configured control)

The alternative function of these LEDs is to indicate which port is being set as the upstream port when changes to the upstream port are enabled.

Table 4-12

DS115	DS116	DS117	Port Set as Upstream Port
On	On	On	Port 0
On		On	Port 1
On	On		Port 2
On			Port 3

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4.3.8 Power Supplies

These LEDs show the presence of the power supplies on the board, though the LED being on does not indicate that the associated power supply is within any specified tolerance.

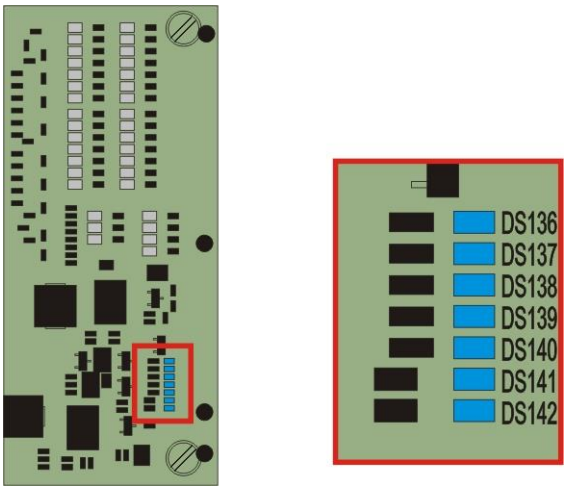


Table 4-13

LED	Power Supply Indicated	Source
DS136	P3V3_AUX	Backplane
DS137	P1V5	On-board
DS138	P1V	On-board
DS139	P3V3	On-board
DS140	Vcc (5V)	Backplane
DS141	P12V	Backplane (only if required by PMC/XMC)
DS142	N12V	Backplane (only if required by PMC/XMC)

4.4 Software

This board does not have any specific software. An associated SBC may require software to enable the in-system programming of the EEPROMs.

4.4.1 Operating Systems

This board does not have an operating system.

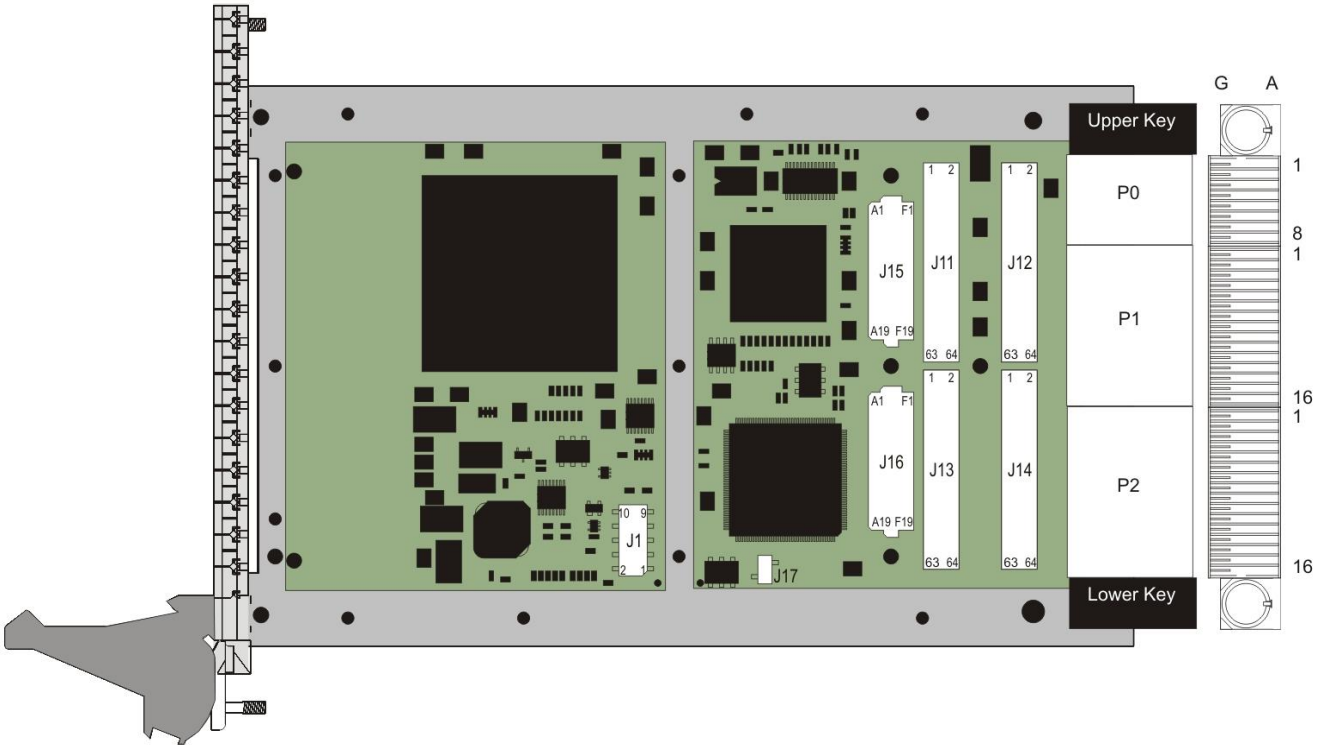
4.4.2 BIT

This board does not have any specific BIT. An associated SBC may include some BIT functionality for this board.

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5 • Connectors

Figure 5-1 Connector Positions and Numbering



The connector functions are designated as follows:

Table 5-1 Connector Designations

Connector	Function
P0	Power Supplies and JTAG
P1	Channel A-D, PMC Interrupts
P2	PMC/XMC I/O signals
J1	JTAG interface
J11	PMC Interface
J12	PMC Interface
J13	PMC Interface
J14	PMC Interface
J15	XMC interface
J16	XMC interface
J17	P3V3

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5.1 Pinouts

NOTE

Due to the pinouts of the board connector and the mating backplane connector being different, both are given for clarity.

5.1.1 P0 Connector

Table 5-2 P0 Pin Assignment

Pin	A	B	C	D	E	F	G
1	Not Used	Not Used	Not Used	NONE	Not Used	Not Used	Not Used
2	Not Used	Not Used	Not Used	NONE	Not Used	Not Used	Not Used
3	VCC(+5V)	VCC(+5V)	VCC(+5V)	NONE	VCC(+5V)	VCC(+5V)	VCC(+5V)
4	NVMRO	SYSRESET~	GND	N12V_AUX	GND	SM3	SM2
5	SM1	SM0	GND	P3V3_AUX	GND	GA4~	GAP~
6	GA0~	GA1~	GND	P12V_AUX	GND	GA2~	GA3~
7	JTAG_TRST~	JTAG_TMS	GND	JTAG_TDI	JTAG_TDO	GND	JTAG_TCK
8	GND	Not Used	Not Used	GND	Not Used	Not Used	GND

5.1.2 J0 (Backplane) Connector Pinout

Table 5-3 J0 Pin Assignment

Fin	A	B	C	D	E	F	G	H	I
1	Not Used by product	Not Used by product	Not Used by product	Not Used by product	NONE	Not Used by product	Not Used by product	Not Used by product	Not Used by product
2	Not Used by product	Not Used by product	Not Used by product	Not Used by product	NONE	Not Used by product	Not Used by product	Not Used by product	Not Used by product
3	VCC(+5V)	VCC(+5V)	VCC(+5V)	VCC(+5V)	NONE	VCC(+5V)	VCC(+5V)	VCC(+5V)	VCC(+5V)
4	GND	NVMRO	SYSRESET~	GND	N12V_AUX	GND	SM3	SM2	GND
5	GND	SM1	SM0	GND	P3V3_AUX	GND	GA4~	GAP~	GND
6	GND	GA0~	GA1~	GND	P12V_AUX	GND	GA2~	GA3~	GND
7	JTAG_TRST~	JTAG_TMS	GND	GND	JTAG_TDI	JTAG_TDO	GND	GND	JTAG_TCK
8	GND	GND	Not Used by product	Not Used by product	GND	GND	REF_CLK_P Not Used by product	REF_CLK_N Not Used by product	GND

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5.1.3 P1 Connector

Table 5-4 P1 Pin Assignment

Pin	A	B	C	D	E	F	G
1	CHA_RXOP	CHA_RXON	GND	CHA_TXOP	CHA_TXON	GND	NOT USED
2	GND	CHA_RX1P	CHA_RX1N	GND	CHA_TX1P	CHA_TX1N	GND
3	CHA_RX2P	CHA_RX2N	GND	CHA_TX2P	CHA_TX2N	GND	NOT USED
4	GND	CHA_RX3P	CHA_RX3N	GND	CHA_TX3P	CHA_TX3N	GND
5	CHB_RXOP	CHB_RXON	GND	CHB_TXOP	CHB_TXON	GND	SYS_CON~
6	GND	CHB_RX1P	CHB_RX1N	GND	CHB_TX1P	CHB_TX1N	GND
7	CHB_RX2P	CHB_RX2N	GND	CHB_TX2P	CHB_TX2N	GND	PMC_INT_OUTAB
8	GND	CHB_RX3P	CHB_RX3N	GND	CHB_TX3P	CHB_TX3N	GND
9	CHC_RXOP	CHC_RXON	GND	CHC_TXOP	CHC_TXON	GND	PMC_INT_OUTCD
10	GND	CHC_RX1P	CHC_RX1N	GND	CHC_TX1P	CHC_TX1N	GND
11	CHC_RX2P	CHC_RX2N	GND	CHC_TX2P	CHC_TX2N	GND	PMC_INT_OUTANY
12	GND	CHC_RX3P	CHC_RX3N	GND	CHC_TX3P	CHC_TX3N	GND
13	CHD_RXOP	CHD_RXON	GND	CHD_TXOP	CHD_TXON	GND	VPXP1_NOTUSED4
14	GND	CHD_RX1P	CHD_RX1N	GND	CHD_TX1P	CHD_TX1N	GND
15	CHD_RX2P	CHD_RX2N	GND	CHD_TX2P	CHD_TX2N	GND	VPXP1_NOTUSED5
16	GND	CHD_RX3P	CHD_RX3N	GND	CHD_TX3P	CHD_TX3N	GND

5.1.4 J1 (Backplane) Connector Pinout

Table 5-5 J1 Pin Assignment

Fin	A	B	C	D	E	F	G	H	I
1	CHA_RXOP	CHA_RXON	GND	GND	CHA_TXOP	CHA_TXON	GND	GND	NOT USED
2	GND	GND	CHA_RX1P	CHA_RX1N	GND	GND	CHA_TX1P	CHA_TX1N	GND
3	CHA_RX2P	CHA_RX2N	GND	GND	CHA_TX2P	CHA_TX2N	GND	GND	NOT USED
4	GND	GND	CHA_RX3P	CHA_RX3N	GND	GND	CHA_TX3P	CHA_TX3N	GND
5	CHB_RXOP	CHB_RXON	GND	GND	CHB_TXOP	CHB_TXON	GND	GND	SYS_CON~
6	GND	GND	CHB_RX1P	CHB_RX1N	GND	GND	CHB_TX1P	CHB_TX1N	GND
7	CHB_RX2P	CHB_RX2N	GND	GND	CHB_TX2P	CHB_TX2N	GND	GND	PMC_INT_OUTAB
8	GND	GND	CHB_RX3P	CHB_RX3N	GND	GND	CHB_TX3P	CHB_TX3N	GND
9	CHC_RXOP	CHC_RXON	GND	GND	CHC_TXOP	CHC_TXON	GND	GND	PMC_INT_OUTCD
10	GND	GND	CHC_RX1P	CHC_RX1N	GND	GND	CHC_TX1P	CHC_TX1N	GND
11	CHC_RX2P	CHC_RX2N	GND	GND	CHC_TX2P	CHC_TX2N	GND	GND	PMC_INT_OUTANY
12	GND	GND	CHC_RX3P	CHC_RX3N	GND	GND	CHC_TX3P	CHC_TX3N	GND
13	CHD_RXOP	CHD_RXON	GND	GND	CHD_TXOP	CHD_TXON	GND	GND	VPXP1_NOTUSED4
14	GND	GND	CHD_RX1P	CHD_RX1N	GND	GND	CHD_TX1P	CHD_TX1N	GND
15	CHD_RX2P	CHD_RX2N	GND	GND	CHD_TX2P	CHD_TX2N	GND	GND	VPXP1_NOTUSED5
16	GND	GND	CHD_RX3P	CHD_RX3N	GND	GND	CHD_TX3P	CHD_TX3N	GND

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5.1.5 P2 Connector

Table 5-6 P2 Pin Assignment

Pin	A	B	C	D	E	F	G
1	IO1N	IO1P	GND	IO0N	IO0P	GND	SINGIO0
2	GND	IO3N	IO3P	GND	IO2N	IO2P	GND
3	IO5N	IO5P	GND	IO4N	IO4P	GND	SINGIO1
4	GND	IO7N	IO7P	GND	IO6N	IO6P	GND
5	IO9N	IO9P	GND	IO8N	IO8P	GND	SINGIO2
6	GND	IO11N	IO11P	GND	IO10N	IO10P	GND
7	IO13N	IO13P	GND	IO12N	IO12P	GND	SINGIO3
8	GND	IO15N	IO15P	GND	IO14N	IO14P	GND
9	IO17N	IO17P	GND	IO16N	IO16P	GND	SINGIO4
10	GND	IO19N	IO19P	GND	IO18N	IO18P	GND
11	IO21N	IO21P	GND	IO20N	IO20P	GND	SINGIO5
12	GND	IO23N	IO23P	GND	IO22N	IO22P	GND
13	IO25N	IO25P	GND	IO24N	IO24P	GND	SEQ_IN
14	GND	IO27N	IO27P	GND	IO26N	IO26P	GND
15	IO29N	IO29P	GND	IO28N	IO28P	GND	SEQ_OUT
16	GND	IO31N	IO31P	GND	IO30N	IO30P	GND

5.1.6 J2 (Backplane) Connector Pinout

Table 5-7 J2 Pin Assignment

Fin	A	B	C	D	E	F	G	H	I
1	IO1N	IO1P	GND	GND	IO0N	IO0P	GND	GND	SINGIO0
2	GND	GND	IO3N	IO3P	GND	GND	IO2N	IO2P	GND
3	IO5N	IO5P	GND	GND	IO4N	IO4P	GND	GND	SINGIO1
4	GND	GND	IO7N	IO7P	GND	GND	IO6N	IO6P	GND
5	IO9N	IO9P	GND	GND	IO8N	IO8P	GND	GND	SINGIO2
6	GND	GND	IO11N	IO11P	GND	GND	IO10N	IO10P	GND
7	IO13N	IO13P	GND	GND	IO12N	IO12P	GND	GND	SINGIO3
8	GND	GND	IO15N	IO15P	GND	GND	IO14N	IO14P	GND
9	IO17N	IO17P	GND	GND	IO16N	IO16P	GND	GND	SINGIO4
10	GND	GND	IO19N	IO19P	GND	GND	IO18N	IO18P	GND
11	IO21N	IO21P	GND	GND	IO20N	IO20P	GND	GND	SINGIO5
12	GND	GND	IO23N	IO23P	GND	GND	IO22N	IO22P	GND
13	IO25N	IO25P	GND	GND	IO24N	IO24P	GND	GND	SEQ_IN
14	GND	GND	IO27N	IO27P	GND	GND	IO26N	IO26P	GND
15	IO29N	IO29P	GND	GND	IO28N	IO28P	GND	GND	SEQ_OUT
16	GND	GND	IO31N	IO31P	GND	GND	IO30N	IO30P	GND

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5.1.7 P0 VPX Signal Descriptions

Table 5-8 P0 Signal Descriptions

Signal	Description	Type
GA0/1~	Geographical Addressing bit 0/1	Input
GA2/3/4~	Geographical Addressing bit 2/3/4 - Reserved for future use	Input
GAP~	Geographical Addressing parity bit - Reserved for future use	Input
GND	Ground	Power
JTAG_TCK	JTAG TCK	Input
JTAG_TDI	JTAG TDI	Input
JTAG_TDO	JTAG TDO	Output
JTAG_TMS	JTAG TMS	Input
JTAG_TRST	JTAG TRST	Input
N12V (-12V)	-12V supply	Power
NVMRO	Non Volatile Memory Read Only control	Input
P12V (+12V)	+12V supply	power
P3V3_AUX (+3.3V)	3V3 Aux supply	Power
REF_CLK_N/P	PCI Express reference clock. This signal is not used by the PEX430 as an on-board clock is routed to the XMC site. Contact your local representative for other options.	Input
SM0-3	System management bus signal	Bi-directional
SYSRESET~	System Reset	Input
Vcc (+5V)	5V supply - main supply used by the PEX430	Power

5.1.8 P1 Signal Descriptions

Table 5-9 P1 Signal Descriptions

Signal	Description	Type
CHA-D_RX0-3N	PCI Express receive lane 0 of channel A-D - 'Negative' signal of differential pair	Input
CHA-D_RX0-3P	PCI Express receive lane 0 of channel A-D - 'Positive' signal of differential pair	Input
CHA-D_TX0-3N	PCI Express transmit lane 0 of channel A-D - 'Negative' signal of differential pair	Output
CHA-D_TX0-3P	PCI Express transmit lane 0 of channel A-D - 'Positive' signal of differential pair	Output
GND	Ground	Signal ground
NOTUSED	Spare	
PMC_INT_OUTAB	PMC interrupt - combined PMC INTA~ and INTB~	
PMC_INT_OUTANY	PMC interrupt - combined PMC INTA~ INTB~ INTC~ and INTD~	
PMC_INT_OUTCD	PMC interrupt - combined PMC INTC~ and INTD~	
SYS_CON~	Reserved for future use	

Erratum
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5.1.9 P2 Signal Descriptions

Table 5-10 P2 VPX Signal Descriptions

Signal	Description	Type
GND	Ground	Signal ground
IOnN	PMC or XMC I/O signal - 'Negative' signal of a differential pair	I/O
IOnP	PMC or XMC I/O signal - 'Positive' signal of a differential pair	I/O
SEQ_IN	Power Supply Sequence Input	Input
SEQ_OUT	Power Supply Sequence Output	Output
SINGIO0-5	XMC single ended I/O	I/O

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5.1.10 J1 (JTAG) Connector

Table 5-11 J1 Pin Assignment

Pin	Signal
1	VPX_JTAG_TRST~
2	GND
3	VPX_JTAG_TDO
4	GND
5	VPX_JTAG_TDI
6	GND
7	VPX_JTAG_TMS
8	GND
9	VPX_JTAG_TCK
10	GND

5.1.11 J17 Connector

Table 5-12 J17 Pin Assignment

Pin	A
1	P3V3
2	P3V3

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5.1.12 J11 (PMC) Connector

Table 5-13 J11 Pin Assignment

Pin	Signal	Pin	Signal
1	BUFFER_JTAG_TCK	2	N12V
3	GND	4	PMC_INTA~
5	PMC_INTB~	6	PMC_INTC~
7	PMC_BUSMODE1~	8	VCC
9	PMC_INTD~	10	NC
11	GND	12	NC
13	PMC_CLK	14	GND
15	GND	16	PMC_GNT~
17	PMC_REQ~	18	VCC
19	P3V3	20	PMC_AD(31)
21	PMC_AD(28)	22	PMC_AD(27)
23	PMC_AD(25)	24	GND
25	GND	26	PMC_C_BE3~
27	PMC_AD(22)	28	PMC_AD(21)
29	PMC_AD(19)	30	VCC
31	P3V3	32	PMC_AD(17)
33	PMC_FRAME~	34	GND
35	GND	36	PMC_IRDY~
37	PMC_DEVSEL~	38	VCC
39	PMC_PCIX_CAP	40	PMC_LOCK~
41	PMC_SDONE~	42	PMC_SBO~
43	PMC_PAR	44	GND
45	P3V3	46	PMC_AD(15)
47	PMC_AD(12)	48	PMC_AD(11)
49	PMC_AD(9)	50	VCC
51	GND	52	PMC_C_BE0~
53	PMC_AD(6)	54	PMC_AD(5)
55	PMC_AD(4)	56	GND
57	P3V3	58	PMC_AD(3)
59	PMC_AD(2)	60	PMC_AD(1)
61	PMC_AD(0)	62	VCC
63	GND	64	PMC_REQ64~

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5.1.13 J12 (PMC) Connector

Table 5-14 J12 Pin Assignment

Pin	Signal	Pin	Signal
1	P12V	2	BUFFER_JTAG_TRST~
3	BUFFER_JTAG_TMS	4	PMC_JTAG_TDO
5	CPLD_JTAG_TDO	6	GND
7	GND	8	Not Used
9	Not Used	10	Not Used
11	PMC_BUSMODE2~	12	P3V3
13	PMC_RESET~	14	PMC_BUSMODE3~
15	P3V3	16	PMC_BUSMODE4~
17	Not Used	18	GND
19	PMC_AD(30)	20	PMC_AD(29)
21	GND	22	PMC_AD(26)
23	PMC_AD(24)	24	P3V3
25	PMC_IDSEL	26	PMC_AD(23)
27	P3V3	28	PMC_AD(20)
29	PMC_AD(18)	30	GND
31	PMC_AD(16)	32	PMC_C_BE2~
33	GND	34	XSIG040596
35	PMC_TRDY~	36	P3V3
37	GND	38	PMC_STOP~
39	PMC_PERR~	40	GND
41	P3V3	42	PMC_SERR~
43	PMC_C_BE1~	44	GND
45	PMC_AD(14)	46	PMC_AD(13)
47	PMC_M66EN	48	PMC_AD(10)
49	PMC_AD(8)	50	P3V3
51	PMC_AD(7)	52	XSIG040598
53	P3V3	54	XSIG040600
55	PMC_MSCL_IPMI_CLK	56	GND
57	PMC_MSDA_IPMI_DATA	58	EREADY
59	GND	60	XSIG040606
61	PMC_ACK64~	62	P3V3
63	GND	64	XSIG040609

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5.1.14 J13 (PMC) Connector

Table 5-15 J13 Pin Assignment

Pin	Signal	Pin	Signal
1	Not Used	2	GND
3	GND	4	PMC_C_BE7~
5	PMC_C_BE6~	6	PMC_C_BE5~
7	PMC_C_BE4~	8	GND
9	P3V3	10	PMC_PAR64
11	PMC_AD(63)	12	PMC_AD(62)
13	PMC_AD(61)	14	GND
15	GND	16	PMC_AD(60)
17	PMC_AD(59)	18	PMC_AD(58)
19	PMC_AD(57)	20	GND
21	P3V3	22	PMC_AD(56)
23	PMC_AD(55)	24	PMC_AD(54)
25	PMC_AD(53)	26	GND
27	GND	28	PMC_AD(52)
29	PMC_AD(51)	30	PMC_AD(50)
31	PMC_AD(49)	32	GND
33	GND	34	PMC_AD(48)
35	PMC_AD(47)	36	PMC_AD(46)
37	PMC_AD(45)	38	GND
39	P3V3	40	PMC_AD(44)
41	PMC_AD(43)	42	PMC_AD(42)
43	PMC_AD(41)	44	GND
45	GND	46	PMC_AD(40)
47	PMC_AD(39)	48	PMC_AD(38)
49	PMC_AD(37)	50	GND
51	GND	52	PMC_AD(36)
53	PMC_AD(35)	54	PMC_AD(34)
55	PMC_AD(33)	56	GND
57	P3V3	58	PMC_AD(32)
59	Not Used	60	Not Used
61	Not used	62	GND
63	GND	64	Not Used

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5.1.15 J14 (PMC) Connector

Table 5-16 J14 Pin Assignment

Pin	Signal	Pin	Signal
1	PMC_IO0P	33	PMC_IO16P
2	PMC_IO1P	34	PMC_IO17P
3	PMC_IO0N	35	PMC_IO16N
4	PMC_IO1N	36	PMC_IO17N
5	PMC_IO2P	37	PMC_IO18P
6	PMC_IO3P	38	PMC_IO19P
7	PMC_IO2N	39	PMC_IO18N
8	PMC_IO3N	40	PMC_IO19N
9	PMC_IO4P	41	PMC_IO20P
10	PMC_IO5P	42	PMC_IO21P
11	PMC_IO4N	43	PMC_IO20N
12	PMC_IO5N	44	PMC_IO21N
13	PMC_IO6P	45	PMC_IO22P
14	PMC_IO7P	46	PMC_IO23P
15	PMC_IO6N	47	PMC_IO22N
16	PMC_IO7N	48	PMC_IO23N
17	PMC_IO8P	49	PMC_IO24P
18	PMC_IO9P	50	PMC_IO25P
19	PMC_IO8N	51	PMC_IO24N
20	PMC_IO9N	52	PMC_IO25N
21	PMC_IO10P	53	PMC_IO26P
22	PMC_IO11P	54	PMC_IO27P
23	PMC_IO10N	55	PMC_IO26N
24	PMC_IO11N	56	PMC_IO27N
25	PMC_IO12P	57	PMC_IO28P
26	PMC_IO13P	58	PMC_IO29P
27	PMC_IO12N	59	PMC_IO28N
28	PMC_IO13N	60	PMC_IO29N
29	PMC_IO14P	61	PMC_IO30P
30	PMC_IO15P	62	PMC_IO31P
31	PMC_IO14N	63	PMC_IO30N
32	PMC_IO15N	64	PMC_IO31N

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5.1.16 J14 (PMC) to J2 (Backplane) Mapping

Table 5-17 PMC to J2 Mapping

J14 Pin	Signal	J2 Pin	J14 Pin	Signal	J2 Pin
1	PMC_IO0P	F1	2	PMC_IO1P	B1
3	PMC_IO0N	E1	4	PMC_IO1N	A1
5	PMC_IO2P	H2	6	PMC_IO3P	D2
7	PMC_IO2N	G2	8	PMC_IO3N	C2
9	PMC_IO4P	F3	10	PMC_IO5P	B3
11	PMC_IO4N	E3	12	PMC_IO5N	A3
13	PMC_IO6P	H4	14	PMC_IO7P	D4
15	PMC_IO6N	G4	16	PMC_IO7N	C4
17	PMC_IO8P	F5	18	PMC_IO9P	B5
19	PMC_IO8N	E5	20	PMC_IO9N	A5
21	PMC_IO10P	H6	22	PMC_IO11P	D6
23	PMC_IO10N	G6	24	PMC_IO11N	C6
25	PMC_IO12P	F7	26	PMC_IO13P	B7
27	PMC_IO12N	E7	28	PMC_IO13N	A7
29	PMC_IO14P	H8	30	PMC_IO15P	D8
31	PMC_IO14N	G8	32	PMC_IO15N	C8
33	PMC_IO16P	F9	34	PMC_IO17P	B9
35	PMC_IO16N	E9	36	PMC_IO17N	A9
37	PMC_IO18P	H10	38	PMC_IO19P	D10
39	PMC_IO18N	G10	40	PMC_IO19N	C10
41	PMC_IO20P	F11	42	PMC_IO21P	B11
43	PMC_IO20N	E11	44	PMC_IO21N	A11
45	PMC_IO22P	H12	46	PMC_IO23P	D12
47	PMC_IO22N	G12	48	PMC_IO23N	C12
49	PMC_IO24P	F13	50	PMC_IO25P	B13
51	PMC_IO24N	E13	52	PMC_IO25N	A13
53	PMC_IO26P	H14	54	PMC_IO27P	D14
55	PMC_IO26N	G14	56	PMC_IO27N	C14
57	PMC_IO28P	F15	58	PMC_IO29P	B15
59	PMC_IO28N	E15	60	PMC_IO29N	A15
61	PMC_IO30P	H16	62	PMC_IO31P	D16
63	PMC_IO30N	G16	64	PMC_IO31N	C16

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5.1.17 J15 (XMC) Connector

Table 5-18 J15 Pin Assignment

Pin	A	B	C	D	E	F
1	XMC_CHA_TXOP	XMC_CHA_TXON	P3V3	XMC_CHA_TX1P	XMC_CHA_TX1N	XMC15_VPWR_12V5V
2	GND	GND	BUFFER_JTAG_TRST~	GND	GND	XMC15_MRSTI~
3	XMC_CHA_TX2P	XMC_CHA_TX2N	P3V3	XMC_CHA_TX3P	XMC_CHA_TX3N	XMC15_VPWR_12V5V
4	GND	GND	BUFFER_JTAG_TCK	GND	GND	XMC15_MRSTO~
5	XMC_CHA_TX4P	XMC_CHA_TX4N	P3V3	XMC_CHA_TX5P	XMC_CHA_TX5N	XMC15_VPWR_12V5V
6	GND	GND	BUFFER_JTAG_TMS	GND	GND	P12V
7	XMC_CHA_TX6P	XMC_CHA_TX6N	P3V3	XMC_CHA_TX7P	XMC_CHA_TX7N	XMC15_VPWR_12V5V
8	GND	GND	PMC_JTAG_TDO	GND	GND	N12V
9	Not Used	Not Used	Not Used	Not Used	Not Used	XMC15_VPWR_12V5V
10	GND	GND	XMC_JTAG_TDO	GND	GND	VPX_SMOOTH_XMC15_GA0~
11	XMC_CHA_RXOP	XMC_CHA_RXON	XMC15_MBIST~	XMC_CHA_RX1P	XMC_CHA_RX1N	XMC15_VPWR_12V5V
12	GND	GND	VPX_SMOOTH_XMC15_GA1~	GND	GND	XMC15_MPRESENT~
13	XMC_CHA_RX2P	XMC_CHA_RX2N	P3V3_AUX	XMC_CHA_RX3P	XMC_CHA_RX3N	XMC15_VPWR_12V5V
14	GND	GND	VPX_SMOOTH_XMC15_GA2~	GND	GND	XMC15_MSDA_IPMI_DATA
15	XMC_CHA_RX4P	XMC_CHA_RX4N	Not Used	XMC_CHA_RX5P	XMC_CHA_RX5N	XMC15_VPWR_12V5V
16	GND	GND	XMC15_MVMRO	GND	GND	XMC15_MSCL_IPMI_CLK
17	XMC_CHA_RX6P	XMC_CHA_RX6N	Not Used	XMC_CHA_RX7P	XMC_CHA_RX7N	Not Used
18	GND	GND	Not Used	GND	GND	Not Used
19	BP_REF_CLK_P	BP_REF_CLK_N	Not Used	XMC_WAKE~	XMC_ROOT0~	Not Used

5.1.18 J16 (XMC) Connector

Table 5-19 J16 Pin Assignment

Pin	A	B	C	D	E	F
1	XMC_IO0P	XMC_IO0N	XMC_IO20P	XMC_IO1P	XMC_IO1N	XMC_IO21P
2	GND	GND	XMC_IO20N	GND	GND	XMC_IO21N
3	XMC_IO2P	XMC_IO2N	XMC_IO22P	XMC_IO3P	XMC_IO3N	XMC_IO23P
4	GND	GND	XMC_IO22N	GND	GND	XMC_IO23N
5	XMC_IO4P	XMC_IO4N	XMC_IO24P	XMC_IO5P	XMC_IO5N	XMC_IO25P
6	GND	GND	XMC_IO24N	GND	GND	XMC_IO25N
7	XMC_IO6P	XMC_IO6N	XMC_IO26P	XMC_IO7P	XMC_IO7N	XMC_IO27P
8	GND	GND	XMC_IO26N	GND	GND	XMC_IO27N
9	XMC_IO8P	XMC_IO8N	XMC_IO28P	XMC_IO9P	XMC_IO9N	XMC_IO29P
10	GND	GND	XMC_IO28N	GND	GND	XMC_IO29N
11	XMC_IO10P	XMC_IO10N	XMC_IO30P	XMC_IO11P	XMC_IO11N	XMC_IO31P
12	GND	GND	XMC_IO30N	GND	GND	XMC_IO31N
13	XMC_IO12P	XMC_IO12N	XMC_SINGIO0	XMC_IO13P	XMC_IO13N	XMC_SINGIO1
14	GND	GND	XMC_SINGIO2	GND	GND	XMC_SINGIO3
15	XMC_IO14P	XMC_IO14N	XMC_SINGIO4	XMC_IO15P	XMC_IO15N	XMC_SINGIO5
16	GND	GND	XMC_SINGIO6	GND	GND	XMC_SINGIO7
17	XMC_IO16P	XMC_IO16N	XMC_SINGIO8	XMC_IO17P	XMC_IO17N	XMC_SINGIO9
18	GND	GND	XMC_SINGIO10	GND	GND	XMC_SINGIO11
19	XMC_IO18P	XMC_IO18N	XMC_SINGIO12	XMC_IO19P	XMC_IO19N	XMC_SINGIO13

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5.1.19 J16 (XMC) to J2 (Backplane) Mapping

Table 5-20 XMC to J2 Mapping

J16 Pin	Signal	J2 Pin	J16 Pin	Signal	J2 Pin	J16 Pin	Signal	J2 Pin
A1	XMC_IO0P	F1	C1	XMC_IO20P	F11	E1	XMC_IO1N	A1
A2	GND	GND	C2	XMC_IO20N	E11	E2	GND	GND
A3	XMC_IO2P	H2	C3	XMC_IO22P	H12	E3	XMC_IO3N	C2
A4	GND	GND	C4	XMC_IO22N	G12	E4	GND	GND
A5	XMC_IO4P	F3	C5	XMC_IO24P	F13	E5	XMC_IO5N	A3
A6	GND	GND	C6	XMC_IO24N	E13	E6	GND	GND
A7	XMC_IO6P	H4	C7	XMC_IO26P	H14	E7	XMC_IO7N	C4
A8	GND	GND	C8	XMC_IO26N	G14	E8	GND	GND
A9	XMC_IO8P	F5	C9	XMC_IO28P	F15	E9	XMC_IO9N	A5
A10	GND	GND	C10	XMC_IO28N	E15	E10	GND	GND
A11	XMC_IO10P	H6	C11	XMC_IO30P	H16	E11	XMC_IO11N	C6
A12	GND	GND	C12	XMC_IO30N	G16	E12	GND	GND
A13	XMC_IO12P	F7	C13	XMC_SINGIO0	RSVD	E13	XMC_IO13N	A7
A14	GND	GND	C14	XMC_SINGIO2	RSVD	E14	GND	GND
A15	XMC_IO14P	H8	C15	XMC_SINGIO4	RSVD	E15	XMC_IO15N	C8
A16	GND	GND	C16	XMC_SINGIO6	RSVD	E16	GND	GND
A17	XMC_IO16P	F9	C17	XMC_SINGIO8	RSVD	E17	XMC_IO17N	A9
A18	GND	GND	C18	XMC_SINGIO10	RSVD	E18	GND	GND
A19	XMC_IO18P	H10	C19	XMC_SINGIO12	RSVD	E19	XMC_IO19N	C10
B1	XMC_IO0N	E1	D1	XMC_IO1P	B1	F1	XMC_IO21P	B11
B2	GND	GND	D2	GND	GND	F2	XMC_IO21N	A11
B3	XMC_IO2N	G2	D3	XMC_IO3P	D2	F3	XMC_IO23P	D12
B4	GND	GND	D4	GND	GND	F4	XMC_IO23N	C12
B5	XMC_IO4N	E3	D5	XMC_IO5P	B3	F5	XMC_IO25P	B13
B6	GND	GND	D6	GND	GND	F6	XMC_IO25N	A13
B7	XMC_IO6N	G4	D7	XMC_IO7P	D4	F7	XMC_IO27P	D14
B8	GND	GND	D8	GND	GND	F8	XMC_IO27N	C14
B9	XMC_IO8N	E5	D9	XMC_IO9P	B5	F9	XMC_IO29P	B15
B10	GND	GND	D10	GND	GND	F10	XMC_IO29N	A15
B11	XMC_IO10N	G6	D11	XMC_IO11P	D6	F11	XMC_IO31P	D16
B12	GND	GND	D12	GND	GND	F12	XMC_IO31N	C16
B13	XMC_IO12N	E7	D13	XMC_IO13P	B7	F13	XMC_SINGIO1	RSVD
B14	GND	GND	D14	GND	GND	F14	XMC_SINGIO3	RSVD
B15	XMC_IO14N	G8	D15	XMC_IO15P	D8	F15	XMC_SINGIO5	RSVD
B16	GND	GND	D16	GND	GND	F16	XMC_SINGIO7	RSVD
B17	XMC_IO16N	E9	D17	XMC_IO17P	B9	F17	XMC_SINGIO9	RSVD
B18	GND	GND	D18	GND	GND	F18	XMC_SINGIO11	RSVD
B19	XMC_IO18N	G10	D19	XMC_IO19P	D10	F19	XMC_SINGIO13	RSVD

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A • Specifications

A.1 Power Requirements

A.1.1 Power Dissipation

Maximum 16.5 Watts

Typical 13 Watts

A.1.2 Input Voltage

+5V +5%/-2.5%
Vripple 50 mV (peak-to-peak) contained within the total excursion.



WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly.
If such conditions occur, toxic fumes may be produced due to the destruction of components.

A.1.3 Max Current

3.3 A

Meets MIL-STD-416D, CE101-4 and CE102

Transient suppression to MIL-STD-704D (option to meet MIL-STD-1275A available)

A.2 Interface Specifications

PEX430 meets the following interface specifications:

- VITA 46.0
- VITA 46.4

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A.3 Mechanical Specification

A.3.1 Weight

The approximate weight of the PEX430 is as follows:
Levels 1 to 3 ≈ 198 g
Levels 4 and 5 ≈ 224 g

A.3.2 Dimensions

The air-cooled PEX430 is constructed on a multi-layer single Eurocard and conforms to the dimensions specified in the VITA 46.0 and IEEE 1101.1 and IEEE 1101.2 specifications.

The Conduction-cooled PEX430 is constructed on a multi-layer single Eurocard and conforms to the dimensions specified in the VITA 46.0 and IEEE 1101.1 and IEEE 1101.2 specifications.

A.4 Reliability (MTBF)

The following table shows the predicted values for reliability as Mean Time Between Failures (MTBF) and Failures Per Million Hours (FPMH) as calculated for a PEX430-10000.
The predictions are carried out using MIL-HDBK-217F Notices 1 and 2, parts count method. To complement the 217 failure rates, some manufacturers' data is included where appropriate; πQ values have been modified according to industry practice.

Table A-1 Reliability (MTBF)

Environment	Fail Rate (FPMH)	MTBF (Hours)
Ground Benign 30°C	2.3247328	430,157
Ground Fixed 40°C	5.474254	182,673
Ground Mobile 45°C	13.57089	73,687
Naval Sheltered 40°C	9.435526	105,982
Naval Unsheltered 45°C	25.08919	39,858
Airborne Inhabited Cargo 55°C	11.41123	87,633
Airborne Inhabited Fighter 55°C	18.40739	54,326
Airborne Uninhabited Cargo 70°C	28.3698	35,249
Airborne Uninhabited Fighter 70°C	37.53781	26,640
Airborne Rotary Wing 55°C	30.31795	32,984
Space Flight 30°C	1.9830047	504,285
Missile Flight 45°C	21.23753	47,086
Missile Launch 55°C	52.51884	19,041

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A.5 Environmental Specifications

A.5.1 Convection-cooled Boards

Table A-2 Environmental Specifications - Convection-cooled Boards

Build Style	Temperature (°c)	Low pressure (feet)	Vibration	Shock	Humidity/ salt fog	Comments
Standard (Level 1)	Operating: 0 to +55 with airflow of 300 feet/minute. Storage: -40 to +85 Shock: 10°C/minute over range	Operating: 15,000 Storage: 50,000	Random: 0.002g2/Hz from 10 to 2000 Hz Sine: 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications. Optional conformal coating
Extended Temp (Level 2)	Operating: -20 to +65 with airflow of 300 feet/minute Storage: -40 to +85 Shock: 10°C/minute over range	Operating: 15,000 Storage: 50,000	Random: 0.002g2/Hz from 10 to 2000 Hz Sine: 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformal coated and temperature characterized.
Rugged Air-cooled (Level 3)	Operating: -40 to +75 with airflow of 600 feet/minute Storage: -50 to +100 Shock: 10°C/minute over range	Operating: 15,000 Storage: 50,000 Rapid Decompression: 0 to 50,000	Random: 0.04g2/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. Sine: 5g from 5 to 2000 Hz	20g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Wide temperature rugged, cooled by forced air. Conformal coated for additional protection.

A.5.2 Conduction-cooled Boards

Table A-3 Environmental Specifications - Conduction-cooled Boards

Build style	Temperature (°c)	Low pressure (feet)	Vibration	Shock	Humidity/ salt fog	Comments
Rugged Conduction-cooled (Level 4)	Operating: -40 to +75 at the thermal interface Storage: -50 to +100 Shock: 10°C/minute over range	Operating: 70,000 Storage: 70,000 Rapid Decompression: 0 to 70,000	Random: 0.1g2/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. Sine: 5g from 5 to 2000 Hz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformal-coated as standard. Optional ESS.
Rugged conduction-cooled (level 5)	Operating: -40 to +85 at the thermal interface Storage: -50 to +100 Shock: 10°C/minute over range	Operating: 70,000 Storage: 70,000 Rapid Decompression:0 to 70,000	Random: 0.1g2/Hz with a flat response to 1 kHz. 6db/Octave roll-off from 1 k to 2 kHz. Sine: 5g from 5 to 2 kHz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformal-coated as standard. Optional ESS.

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A.6 Product Code Information

Table A-4 Product Code Information

PEX430-	B	M	X	Y	
					Mechanics
				1	0.8” pitch, VITA 46
					Reserved
					Mezzanine
			P		PMC
			X		XMC
					Build level
	1				Build level 1
	2				Build level 2
	3				Build level 3
	4				Build level 4
	5				Build level 5

Erratum
December 2010

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