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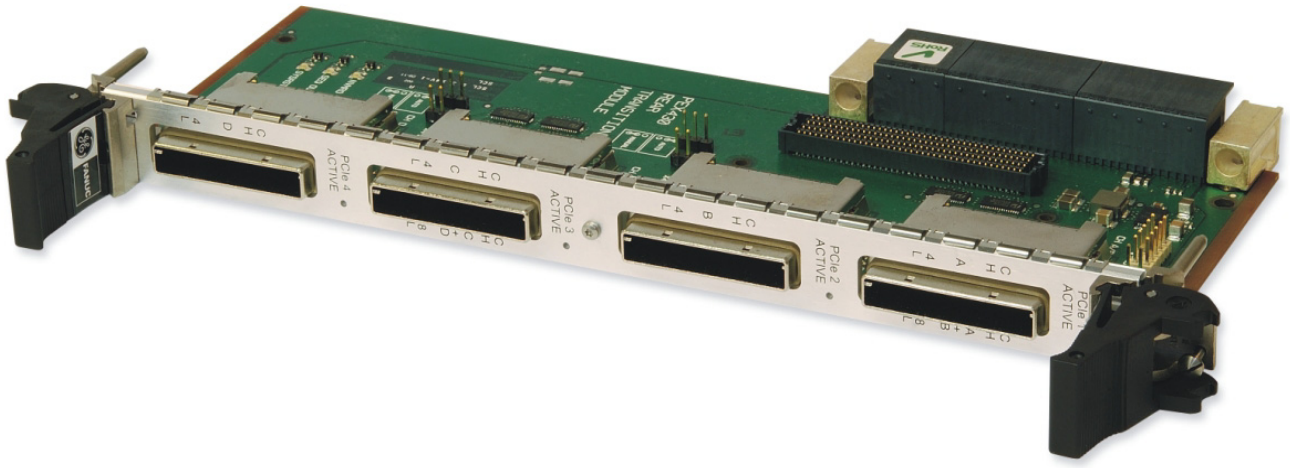
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Hardware Reference Manual

PEX430RTM

Edition 2DG

Publication No. PEX430RTM-0HH/2DG



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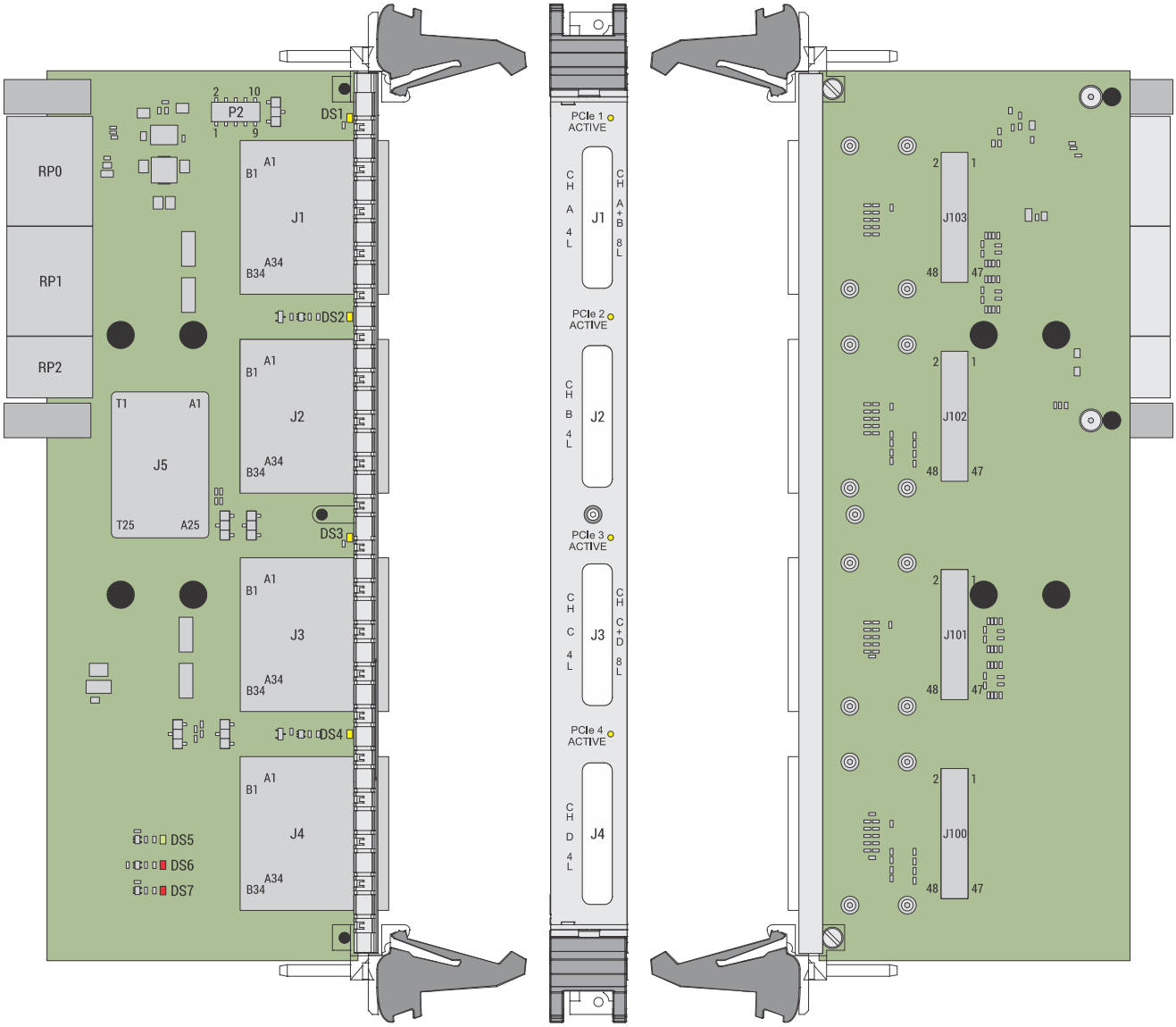
1 • PEX430RTM Layout

This document is intended to be read in conjunction with the VPX I/O Modules manual.

LINK
VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH/2.

The following diagram shows the front and side views of the PEX430RTM to illustrate the position of the various LEDs, connectors, and headers described in this document.

Figure 1-1 PEX430RTM Component Layout



For information on using the PEX430RTM with the MEZZIOP0 module, see section 3.3 Use of the PEX430RTM with the MEZZIOP0.

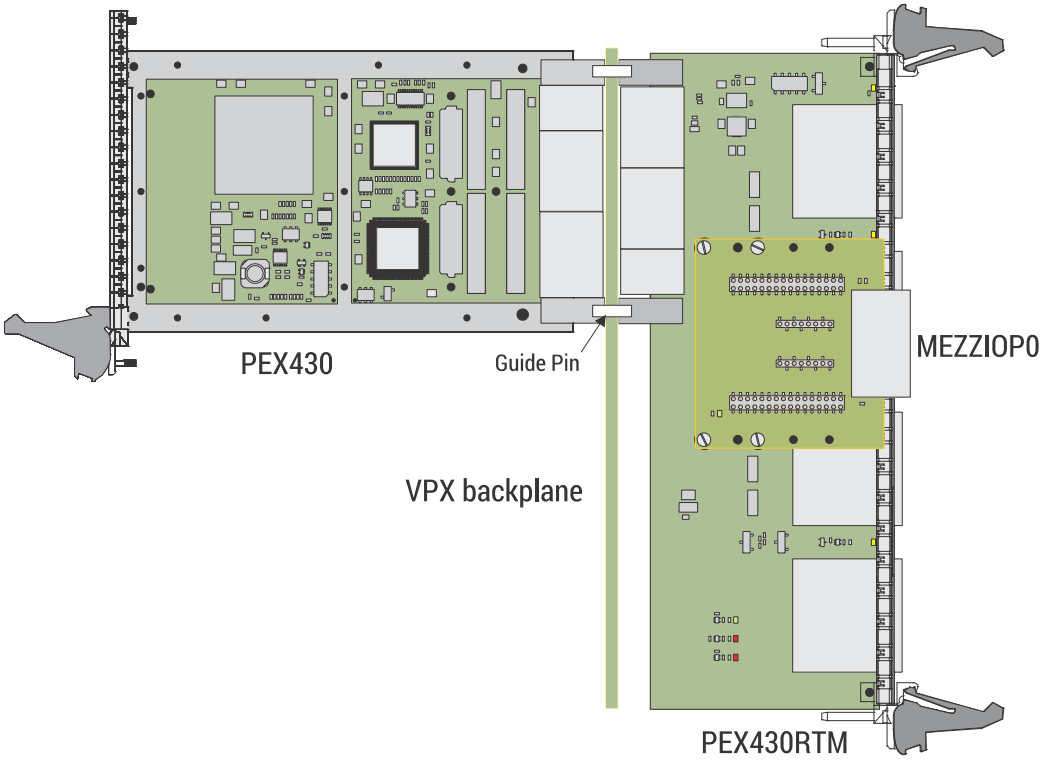
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2 • Installation and Operation

2.1 Fitting the PEX430RTM

The PEX430RTM is inserted into a rack with a backplane supporting VITA46.20. A suitable backplane will have back-to-back VPX connectors such that the RTM can be connected to the main board. The following diagram shows the arrangement for the PEX430RTM when used in combination with the MEZZIOP0 (see section 3.3 Use of the PEX430RTM with the MEZZIOP0).

Figure 2-1 Fitting the PEX430RTM



2.1.1 Guide Pins

The PEX430RTM, in its default build state, uses universally-keyed guide pin sockets. This allows the PEX430RTM to be mated with guide pins of any orientation. Users may change the guide pin sockets to match their requirements.

2.2 LEDs

See Figure 1-1 for the location of the LEDs.

Table 2-1 LED Functions

LED/Color	Function when lit
DS1 to DS4/Yellow	LEDs visible through the front panel indicate which sockets are active
DS5/Red	NVMRO - write enabled
DS6/Green	PEX430 power supplies have successfully completed their power-up sequence
DS7/Red	SYSRESET active

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2.3 Lane Configuration

2.3.1 Automatic Set-up by PCIe Connectors

The lane operation (e.g either x4 lane or x8 lane) of the PCIe ports is determined automatically by the insertion of the connectors into the front panel sockets, J1 to J4. The channels accessible via these sockets (see section 3.2.3 J1, J3 (PCIe) and section 3.2.4 J2, J4 (PCIe)) can each operate as independent x4 lane ports, or else J1 and J3 can be configured as x8 lane ports. For example, simply inserting a PCIe cable connector into each socket configures all ports as x4 lane ports. The following table describes the conditions for other configurations:

NOTE
X = connector is either in or out (don't care).

Table 2-2 Automatic Port Configurations

J1	J2	J3	J4	Port Set-up
In	In	In	In	Channels A to D = x4 lane
In	Out	X	X	Channel A + Channel B = x8 lane
In	In	X	X	Channel A, Channel B = x4 lane
X	X	In	Out	Channel C + Channel D = x8 lane
X	X	In	In	Channel C, Channel D = x4 lane

2.3.2 Channel Combining

The signal names used in the pinout tables reflect the situation that channels either operate separately as x4 lane ports or else may be combined to make x8 lane ports, e.g. signals in orange-shaded cells are combined with those in yellow-shaded cells (see Table 3-3). The following table illustrates this relationship between the connectors and the channels:

Table 2-3 Channel Combining

Connectors	CHA(0-3)	CHB(0-3)	CHC(0-3)	CHD(0-3)	Port Set-up
J1 In, J2 Out (J3/J4 don't care)	x8 (J1)				1 Port Channel A + Channel B = x8 lane
J1 In, J2 In (J3/4 don't care)	x4 (J1)	x4 (J2)			2 Ports Channel A, Channel B = x4 lane
J3 In, J4 Out (J1/J2 don't care)			x8 (J3)		1 Port Channel C + Channel D = x8 lane
J3 In, J4 In (J1/2 don't care)			x4 (J3)	x4 (J4)	2 Ports Channel C, Channel D = x4 lane

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2.3.3 Other Configurations

It is possible to connect to the four PCIe connector sockets in various combinations, and together with the set-up of the PCIe devices at the end of each link, derive diverse Lane/Port configurations. The following table summarizes some of these combinations:

NOTE

X = connector is either in or out (don't care)

Table 2-4 Other Configurations

J1	J2	J3	J4	Lanes	Port	Channels
In				x4	0	A
	In			x4	1	B
In	Out			x8	0	A+B
		In	In[1]	x4	1	C
In	Out			x8	0	A+B
		In	Out	x8	1	C+D
In	Out			x4[2]	0	A
		In	Out	x4[2]	1	C
In				x4	0	A
	In			x4	1	B
		In	In[1]	x4	2	C
In				x4	0	A
	In			x4	1	B
		In		x4	2	C
			In	x4	3	D
In	In			x8[3]	0	A+B
		In	In	x8[3]	1	C+D
In	In	In	In	x16[4]	0	A+B+C+D
In	Out	In	Out	x16[5]	0	A+B+C+D

NOTES

1. If a PCIe cable connector is inserted into J2 or J4 then the lane width of J1 or J3 will be automatically reduced to x4 lane or less. The other end of any such connection to J2 or J4 may be left unconnected.

2. Normally, this would automatically configure the J1 or J3 ports for x8 lane operation, however, in this case, PCIe devices at the end of the links should negotiate the unused lanes from J1 and J3 out of the connection.

3. Four cables, each carrying a x4 lane port, need to be terminated with a PCIe device that is x8 lane capable.

4. Four cables, each carrying a x4 lane port, need to be terminated with a PCIe device that is x16 lane capable.

5. Two cables, each carrying a x8 lane port, need to be terminated with a PCIe device that is x16 lane capable.

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3 • Connectors and Headers

3.1 Connector/Header Designations

See the layout diagram, Figure 1-1.

Table 3-1 Connector/Header Designations

Connector/Header	Functionality
J1	PCIe Channel A and B. See Note 1 below
J2	PCIe Channel B. See Note 1 below
J3	PCIe Channel C and D. See Note 1 below
J4	PCIe Channel D. See Note 1 below
J5	I/O interface
J100, J101, J102, J103	PCIe test points. See Note 2 below
P2	JTAG

NOTES

1. J1, J2, J3, and J4 - compatible cables are Molex 74546-0801 for 1m length (C-ASY000286-801) and Molex 74546-0813 for 0.5m length (C-ASY000286-813).

2. J100, J101, J102, and J103 are PCIe test points for the Agilent N4221A midbus connector. Details of the connectors' pinouts are not given. See http://cp.literature.agilent.com/litweb/pdf/5989-1172EN.pdf for further details.

3.2 Connector/Header Pinouts

3.2.1 Notes Regarding Colored Cells in Tables

The blue shaded signals are not connected to anything other than the PEX430RTM. All of these signals are terminated with a 10kΩ pull up to P3V3_AUX. An option exists to terminate these signals to GND if required.

The green shaded signals are connected to the PEX430RTM but the operation of these signals depends on the signal being sourced on the backplane; these signals are not generated by the PEX430 or the PEX430RTM. They have a differential 100 Ω termination between the P and N signal pair.
Since the PEX430RTM has four x8 lane PCIe Cable connectors, each connector has the green shaded signals available for connection to the reference clock signals on the backplane. However, to maintain a high level of signal integrity, only one of these pairs of signals can be connected at one time. Zero Ω resistor links can be used to select either the J1/J3 PCIe Cable connector or the J2/J4 PCIe Cable connector to connect these signals. In the default build state, the clock signals are connected through the J1/J3 PCIe Cable connector.

The purple shaded signals are not generated by the PEX430 or the PEX430RTM. They have a differential 100 Ω termination between the P and N signal pair.

Use orange-shade signals for x4 lane operation.
Signals with a _x4 suffix are not derived directly from the PEX430.

Use orange *and* yellow-shaded signals for x8 lane operation.
Signals are not derived directly from the PEX430.

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3.2.2 J1 to J4 Standard Pinout (PCIe)

See Table 3-3 and Table 3-4 for PEX430RTM pinouts

Table 3-2 J1 to J4 Standard Pin Assignments

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	PET0P	B2	PER0P
A3	PET0N	B3	PER0N
A4	GND	B4	GND
A5	PET1P	B5	PER1P
A6	PET1N	B6	PER1N
A7	GND	B7	GND
A8	PET2P	B8	PER2P
A9	PET2N	B9	PER2N
A10	GND	B10	GND
A11	PET3P	B11	PER3P
A12	PET3N	B12	PER3N
A13	GND	B13	GND
A14	CREFCLKP	B14	P3V3_AUX
A15	CREFCLKN	B15	P3V3_AUX
A16	GND	B16	P3V3_AUX
A17	NC	B17	GND
A18	NC	B18	GND
A19	CSB_RTN	B19	GND
A20	CPRSNT~	B20	CWAKE~
A21	CPWRON	B21	CPERST~
A22	GND	B22	GND
A23	PET4P	B23	PER4P
A24	PET4N	B24	PER4N
A25	GND	B25	GND
A26	PET5P	B26	PER5P
A27	PET5N	B27	PER5N
A28	NC	B28	GND
A29	PET6P	B29	PER6P
A30	PET6N	B30	PER6N
A31	GND	B31	GND
A32	PET7P	B32	PER7P
A33	PET7N	B33	PER7N
A34	GND	B34	GND

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3.2.3 J1, J3 (PCIe)

See section 3.2.1 Notes Regarding Colored Cells in Tables.

Table 3-3 Combined J1 and J3 Pin Assignments

Pin	J1 Signal	J3 Signal	Pin	J1 Signal	J3 Signal
A1	GND	GND	B1	GND	GND
A2	CHA_TX0P	CHC_TX0P	B2	CHA_RX0P	CHC_RX0P
A3	CHA_TX0N	CHC_TX0N	B3	CHA_RX0N	CHC_RX0N
A4	GND	GND	B4	GND	GND
A5	CHA_TX1P	CHC_TX1P	B5	CHA_RX1P	CHC_RX1P
A6	CHA_TX1N	CHC_TX1N	B6	CHA_RX1N	CHC_RX1N
A7	GND	GND	B7	GND	GND
A8	CHA_TX2P	CHC_TX2P	B8	CHA_RX2P	CHC_RX2P
A9	CHA_TX2N	CHC_TX2N	B9	CHA_RX2N	CHC_RX2N
A10	GND	GND	B10	GND	GND
A11	CHA_TX3P	CHC_TX3P	B11	CHA_RX3P	CHC_RX3P
A12	CHA_TX3N	CHC_TX3N	B12	CHA_RX3N	CHC_RX3N
A13	GND	GND	B13	GND	GND
A14	X8ABCREFCLKP	X8CDCREFCLKP	B14	P3V3_AUX	P3V3_AUX
A15	X8ABCREFCLKN	X8CDCREFCLKN	B15	P3V3_AUX	P3V3_AUX
A16	GND	GND	B16	P3V3_AUX	P3V3_AUX
A17	NC	NC	B17	GND	GND
A18	NC	NC	B18	GND	GND
A19	X8ABCSB_RTN	X8CDCSB_RTN	B19	GND	GND
A20	X8ABCPRSNT~	X8CDCPRSNT~	B20	X8ABCWAKE~	X8CDCWAKE~
A21	X8ABCPWRON	X8CDCPWRON	B21	X8ABCPERST~	X8CDCPERST~
A22	GND	GND	B22	GND	GND
A23	CHB_TX0P_x8	CHD_TX0P_x8	B23	CHB_RX0P_x8	CHD_RX0P_x8
A24	CHB_TX0N_x8	CHD_TX0N_x8	B24	CHB_RX0N_x8	CHD_RX0N_x8
A25	GND	GND	B25	GND	GND
A26	CHB_TX1P_x8	CHD_TX1P_x8	B26	CHB_RX1P_x8	CHD_RX1P_x8
A27	CHB_TX1N_x8	CHD_TX1N_x8	B27	CHB_RX1N_x8	CHD_RX1N_x8
A28	GND	GND	B28	GND	GND
A29	CHB_TX2P_x8	CHD_TX2P_x8	B29	CHB_RX2P_x8	CHD_RX2P_x8
A30	CHB_TX2N_x8	CHD_TX2N_x8	B30	CHB_RX2N_x8	CHD_RX2N_x8
A31	GND	GND	B31	GND	GND
A32	CHB_TX3P_x8	CHD_TX3P_x8	B32	CHB_RX3P_x8	CHD_RX3P_x8
A33	CHB_TX3N_x8	CHD_TX3N_x8	B33	CHB_RX3N_x8	CHD_RX3N_x8
A34	GND	GND	B34	GND	GND

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3.2.4 J2, J4 (PCIe)

See section 3.2.1 Notes Regarding Colored Cells in Tables.

Table 3-4 Combined J2 and J4 Pin Assignments

Pin	J2 Signal	J4 Signal	Pin	J2 Signal	J4 Signal
A1	GND	GND	B1	GND	GND
A2	CHB_TX0P_x4	CHD_TX0P_x4	B2	CHB_RX0P_x4	CHD_RX0P_x4
A3	CHB_TX0N_x4	CHD_TX0N_x4	B3	CHB_RX0N_x4	CHD_RX0N_x4
A4	GND	GND	B4	GND	GND
A5	CHB_TX1P_x4	CHD_TX1P_x4	B5	CHB_RX1P_x4	CHD_RX1P_x4
A6	CHB_TX1N_x4	CHD_TX1N_x4	B6	CHB_RX1N_x4	CHD_RX1N_x4
A7	GND	GND	B7	GND	GND
A8	CHB_TX2P_x4	CHD_TX2P_x4	B8	CHB_RX2P_x4	CHD_RX2P_x4
A9	CHB_TX2N_x4	CHD_TX2N_x4	B9	CHB_RX2N_x4	CHD_RX2N_x4
A10	GND	GND	B10	GND	GND
A11	CHB_TX3P_x4	CHD_TX3P_x4	B11	CHB_RX3P_x4	CHD_RX3P_x4
A12	CHB_TX3N_x4	CHD_TX3N_x4	B12	CHB_RX3N_x4	CHD_RX3N_x4
A13	GND	GND	B13	GND	GND
A14	X4BCREFCLKP	X4DCREFCLKP	B14	P3V3_AUX	P3V3_AUX
A15	X4BCREFCLKN	X4DCREFCLKN	B15	P3V3_AUX	P3V3_AUX
A16	GND	GND	B16	P3V3_AUX	P3V3_AUX
A17	NC	NC	B17	GND	GND
A18	NC	NC	B18	GND	GND
A19	X4BCSB_RTN	X4DCSB_RTN	B19	GND	GND
A20	X4BCPRSNT~	X4DCPRSNT~	B20	X4BCWAKE~	X4DCWAKE~
A21	X4BCPWRON	X4DCPWRON	B21	X4BCPERST~	X4DCPERST~
A22	GND	GND	B22	GND	GND
A23	PET4P	PER4P	B23	PET4P	PER4P
A24	PET4N	PER4N	B24	PET4N	PER4N
A25	GND	GND	B25	GND	GND
A26	PET5P	PER5P	B26	PET5P	PER5P
A27	PET5N	PER5N	B27	PET5N	PER5N
A28	NC	GND	B28	NC	GND
A29	PET6P	PER6P	B29	PET6P	PER6P
A30	PET6N	PER6N	B30	PET6N	PER6N
A31	GND	GND	B31	GND	GND
A32	PET7P	PER7P	B32	PET7P	PER7P
A33	PET7N	PER7N	B33	PET7N	PER7N
A34	P5, PIN2	P6, PIN2	B34	SEL_BX4~	SEL_DX4~

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3.2.5 J5 (PMC/XMC I/O)

A[25:1], C[25:1], E[25:1], G[25:1], J[25:1], K[25:1], M[25:1], P[25:1], R[25:1] and T[25:1] are all GND. There are no I[25:1] or O[25:1].

NOTE

Colors used in the table below indicate the following:
Grey = Ground; Red = Power; Orange = single-ended I/O;

Table 3-5 J5 Pin Assignments

Pin	B	D	F	H	L	N	Q	S
1	IO22P	NC	IO23P	IO21P	SYSRST~	P3V3	VCC	VCC
2	IO20N	NC	IO21N	IO20P	IO2N	IO0N	IO3N	IO1N
3	IO26P	IO24P	IO27P	IO25P	IO2P	IO0P	IO3P	IO1P
4	IO24N	IO22N	IO25N	IO23N	GND	GND	GND	GND
5	IO30P	IO28P	IO31P	IO29P	IO6N	IO4N	IO7N	IO5N
6	IO28N	IO26N	IO29N	IO27N	IO6P	IO4P	IO7P	IO5P
7	SINGIO4	SINGIO0	SINGIO5	SINGIO1	GND	GND	GND	GND
8	SINGIO2	IO30N	SINGIO3	IO31N	IO10N	IO8N	IO11N	IO9N
9	SINGIO12	SINGIO8	SINGIO13	SINGIO9	IO10P	IO8P	IO11P	IO9P
10	SINGIO10	SINGIO6	SINGIO11	SINGIO7	GND	GND	GND	GND
11	GND	GND	GND	GND	IO14N	IO12N	IO15N	IO13N
12	IO2N	IO0N	IO3N	IO1N	IO14P	IO12P	IO15P	IO13P
13	IO2P	IO0P	IO3P	IO1P	GND	GND	GND	GND
14	GND	GND	GND	GND	IO18N	IO16N	IO19N	IO17N
15	IO12N	IO10N	IO13N	IO11N	IO18P	IO16P	IO19P	IO17P
16	IO12P	IO10P	IO13P	IO11P	GND	GND	GND	GND
17	GND	GND	GND	GND	IO22N	IO20N	IO23N	IO21N
18	IO6N	IO4N	IO7N	IO5N	IO22P	IO20P	IO23P	IO21P
19	IO6P	IO4P	IO7P	IO5P	GND	GND	GND	GND
20	GND	GND	GND	GND	IO26N	IO24N	IO27N	IO25N
21	IO14N	IO8N	IO15N	IO9N	IO26P	IO24P	IO27P	IO25P
22	IO14P	IO8P	IO15P	IO9P	GND	GND	GND	GND
23	GND	GND	GND	GND	IO30N	IO28N	IO31N	IO29N
24	IO18N	IO16N	IO19N	IO17N	IO30P	IO28P	IO31P	IO29P
25	IO18P	IO16P	IO19P	IO17P	GND	GND	N12V	P12V

3.2.6 P2 (JTAG)

The JTAG connector is used for programming the CPLD devices on the PEX430.

Table 3-6 P2 Pin Assignments

Pin	Signal	Pin	Signal
1	TRST~	2	GND
3	TDO	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCLK	10	GND

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3.3 Use of the PEX430RTM with the MEZZIOP0

PEX430 may be used with either a PMC or an XMC fitted, and in each case the I/O signals from the mezzanines are routed to the PEX430 P2 connector. Access to these I/O signals is facilitated by using the PEX430RTM in combination with the MEZZIOP0, which, when mounted onto the PEX430RTM J5 connector (see Figure 2-1), presents the PMC/XMC signals to a P0-type connector (P0) and to two board-mounted headers (P2/P3). For more information, see the manual.

LINK
MEZZIOP0 Hardware Reference Manual, publication number MEZZIOP0-HRM.

The following three tables illustrate the distribution of the PMC/XMC I/O differential signals on the MEZZIOP0 P0, P2, and P3 connectors.

NOTE
Colors used in the tables below indicate the following:
Blue = differential signal negative; Red = differential signal positive

3.3.1 MEZZIOP0 P0 Pinout Showing PEX430 PMC/XMC I/O

Table 3-7 MEZZIOP0 P0 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	NC	NC	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	GND
3	NC	NC	NC	VCC	VCC	GND
4	IO2P	IO1N	IO0N	IO1P	IO0P	GND
5	IO5P	IO4P	IO3N	IO2N	IO3P	GND
6	IO6N	IO7P	IO6P	IO5N	IO4N	GND
7	IO9N	IO8N	IO9P	IO8P	IO7N	GND
8	IO12P	IO11N	IO10N	IO11P	IO10P	GND
9	NC	NC	NC	NC	NC	GND
10	NC	NC	NC	NC	NC	GND
11	NC	NC	NC	NC	NC	GND
12	IO15P	IO14P	IO13N	IO12N	IO13P	GND
13	IO16N	IO17P	IO16P	IO15N	IO14N	GND
14	IO19N	IO18N	IO19P	IO18P	IO17N	GND
15	IO22P	IO21N	IO20N	IO21P	IO20P	GND
16	IO25P	IO24P	IO23N	IO22N	IO23P	GND
17	IO26N	IO27P	IO26P	IO25N	IO24N	GND
18	IO29N	IO28N	IO29P	IO28P	IO27N	GND
19	VCC	IO31N	IO30N	IO31P	IO30P	GND

NOTE
All signals are tracked as 50 Ω, single-ended, with matched lengths between pairs, e.g. IO26P with IO26N

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3.3.2 MEZZIOP0 P2 Pinout Showing PEX430 PMC/XMC I/O

Table 3-8 MEZZIOP0 P2 Pinout

Pin	PEX430 PMC/ XMC I/O Signal	Pin	PEX430 PMC/ XMC I/O Signal
1	IO0P	2	IO1P
3	IO0N	4	IO1N
5	IO2P	6	IO3P
7	IO2N	8	IO3N
9	IO4P	10	IO5P
11	IO4N	12	IO5N
13	IO6P	14	IO7P
15	IO6N	16	IO7N
17	IO8P	18	IO9P
19	IO8N	20	IO9N
21	IO10P	22	IO11P
23	IO10N	24	IO11N
25	IO12P	26	IO13P
27	IO12N	28	IO13N
29	IO14P	30	IO15P
31	IO14N	32	IO15N

3.3.3 MEZZIOP0 P3 Pinout Showing PEX430 PMC/XMC I/O

Table 3-9 MEZZIOP0 P3 Pinout

Pin	PEX430 PMC/ XMC I/O Signal	Pin	PEX430 PMC/ XMC I/O Signal
1	IO16P	2	IO17P
3	IO16N	4	IO17N
5	IO18P	6	IO19P
7	IO18N	8	IO19N
9	IO20P	10	IO21P
11	IO20N	12	IO21N
13	IO22P	14	IO23P
15	IO22N	16	IO23N
17	IO24P	18	IO25P
19	IO24N	20	IO25N
21	IO26P	22	IO27P
23	IO26N	24	IO27N
25	IO28P	26	IO29P
27	IO28N	28	IO29N
29	IO30P	30	IO31P
31	IO30N	32	IO31N

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