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ICS-8552B

OPERATING MANUAL

Radstone Sensor Processing

December 2006

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1 INTRODUCTION

The ICS-8552B is a rugged 2-channel, 14-bit A/D module in PCI Mezzanine Card (PMC) format. This product is available in five levels of ruggedization, as defined by Radstone Technology, ranging from benign environment convection-cooled to severe environment conduction-cooled versions. For all ruggedization levels, this board has a nominal signal input impedance of 50 Ohms, conforms to the PCI 2.2 (64-bit, 66 MHz) standard, and is optionally available with Graychip DDC modules. This board supports ADC sample rates from 30 to 105 MHz over the entire -40˚C to +85˚C temperature range. For details on ruggedization levels, refer to Section 2.2.

The ICS-8552B includes a three million gate user programmable FPGA, or User FPGA, that provides flexible signal processing capability for software digital radio and radar applications. It has connections to a user-defined Pn4 connector (User I/O Pn4) to allow high-speed serial and parallel data to be passed via this port, and to enable customer specific signals to be connected to the User FPGA.

This product offers a wide range of operating modes and features; its design has been optimized for applications that demand high speed, precision and ease of integration. A Built-In-Test (BIT) feature is not implemented with this version of the ICS-8552B board, but will be implemented on future versions.

Radstone Sensor Processing offers software drivers for the ICS-8552B for a number of platforms, including Windows, Linux, and the VxWorks real-time operating system. These drivers greatly simplify control and operation of the ICS-8552B, and are strongly recommended. Using one of these drivers will generally save the programmer a significant amount of time since they are relieved of the requirement of understanding the complexities of the ICS-8552B board.

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2 GENERAL DESCRIPTION

A simplified block diagram of the ICS-8552B is shown in Figure 1. The ICS-8552B uses two 14-bit ADCs (Texas Instruments ADS5424) providing a sampling rate of up to 105 MHz (100 MHz maximum sampling rate with the optional use of the DDCs).

The ICS-8552B includes a 66 MHz/64-bit PCI bus interface conforming to the PCI 2.2 specification. The PCI interface uses the QuickLogic QL5064 chip to support a master burst transfer (DMA) interface. The ICS-8552B can generate PCI bus interrupts at any user-programmed interval (number of samples acquired).

The sampling clock and the trigger can be either internal or external. The internal ADC clock for the ICS-8552B is a high stability temperature compensated crystal oscillator (TCXO) with a fixed frequency of 94.4 MHz. The external clock signal may be either a TTL-level or sine wave signal with a frequency in the range 30 - 105 MHz.

The ADCs can be operated in a number of different modes. In the continuous mode, data is continuously converted on all selected channels and supplied to the PCI bus interface upon application of a trigger signal, until the acquisition is disabled. In capture mode, a fixed number of samples are acquired upon each application of the trigger. The number of samples acquired at each application of the trigger is programmable with a resolution of four samples per channel or less, up to the maximum capacity of the buffer. The programmable ADC output decimator can reduce the output data rate by a factor of up to thirty-two.

The outputs of the ADCs are applied directly to a 3 million gate Xilinx Virtex II FPGA for routing and processing of data. A pair of Graychip GC4016 quad digital down-converter (DDC) modules is also connected to the User FPGA. A crossbar switch is supplied as standard firmware in the User FPGA to enable the user to select either the ADC output or the DDC output, under software control. Refer to Section 4.1 for more information on DDC outputs.

The output of the User FPGA is buffered into two 128K x 64 FIFO memories (see Reference [7] for more information), that are designed to accommodate two different channels with two different data rates. PCI Bus interrupts may be generated based on a user programmed threshold level and overflow conditions of the FIFOs. The FIFO outputs are applied to the PCI Bus interface, which is implemented using a QuickLogic QL5064 part. This provides a PCI 2.2 compliant 64-bit/66 MHz PCI interface with Master/Target DMA supporting chain-mode (scatter-gather) DMA.

All power requirements of the ICS-8552B are satisfied with PCI Bus or PMC standard voltages.

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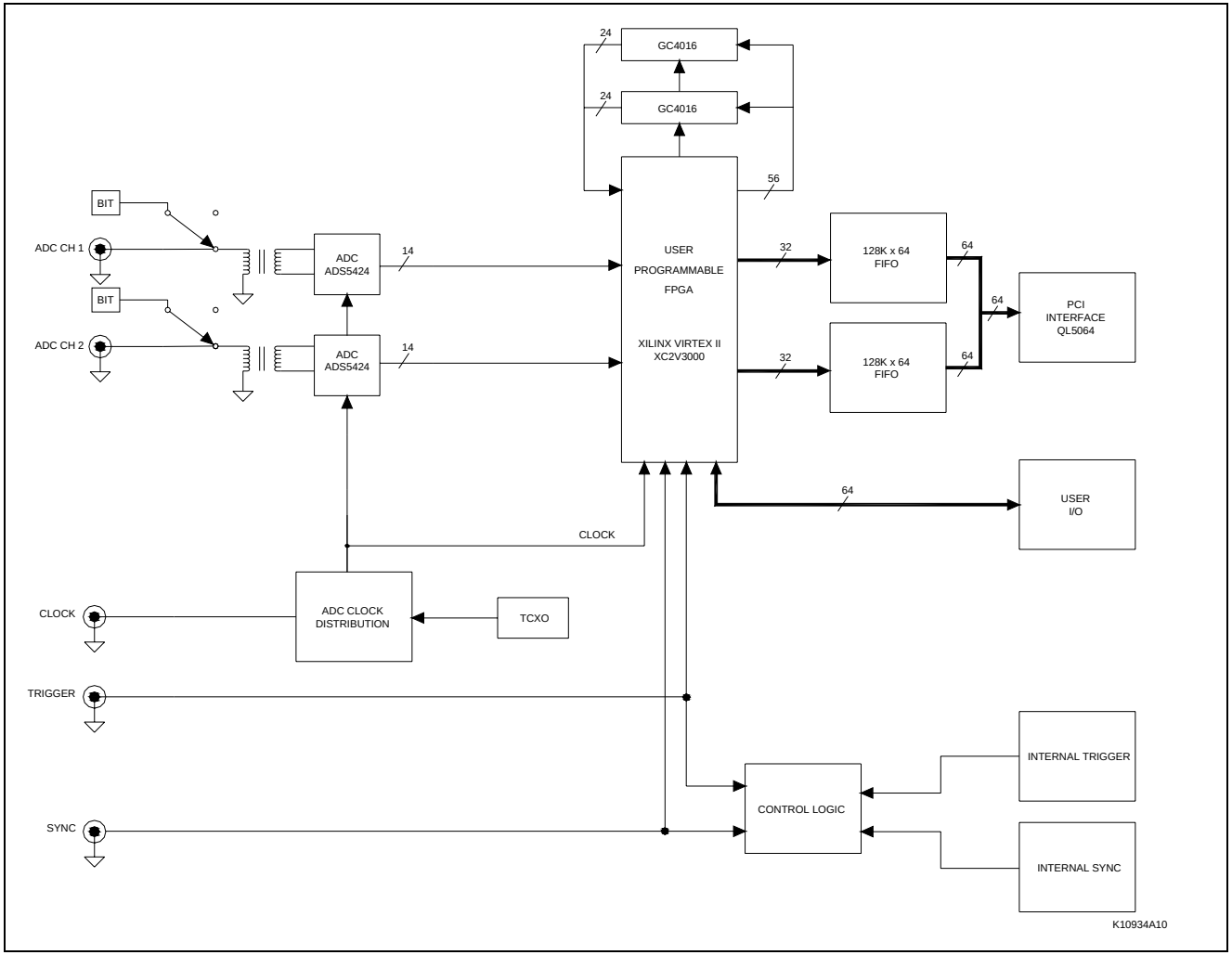


Figure 1 - ICS-8552B Block Diagram

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2.1 ICS-8552B Specifications

Versions: ICS-8552B-**xyy**

00	= 2 DDCs
01	= no DDCs

1 - 5	= Ruggedization Level

ANALOG INPUT	
Number of Analog Input Channels:	2
Analog Connector Type:	MMCX
Input Impedance:	50 Ohm
Full Scale Input:	1.2 V peak-to-peak (+5.5 dBm) into 50 Ohms
Max. Safe Input Voltage:	± 2.5 Volts into 50 Ohms
Input Signal Bandwidth:	2 MHz – 570 MHz (-3 dB point)
Max. Sampling Rate:	105 MHz/channel
Min. Sampling Rate:[1]	30 MHz/channel
Internal Sample Clock Oscillator:	94.4 MHz fixed frequency TCXO, 1 PPM
ADC Resolution:	14 bits
Sampling:	Rising edge of internal or external sample clock
External Clock Connector Type:	MMCX
External Clock:	LVTTL or Sinewave compatible, -3 dBm min., +13 dBm max.
External Trigger Connector Type:	MMCX
External Trigger:	LVTTL compatible, programmable rising or falling edge
External Sync Connector Type:	MMCX
External Sync:	LVTTL compatible, programmable rising or falling edge
Signal-to-Noise Ratio (S/(N+D)):	> 70 dB @ 80 MSPS
SFDR:[2]	> 80 dBc @ 80 MSPS, excluding signal harmonics
Inter-channel Cross-talk:	< -72 dBc

GENERAL	
PCI Bus Interface:	PCI 2.2 64-bit 66 MHz, Master Burst Mode (DMA) capable
User Programmable I/O:	64 I/Os
User Programmable FPGA:	XC2V3000, package: FG676
Onboard storage:	2 MBytes total
Board Size:	CMC single width form factor (see Reference [2])
Board Weight:	98 g
Environmental: Operating Temp	Per ruggedization level
Storage Temp	Per ruggedization level
Humidity	Per ruggedization level
Cooling	Per ruggedization level
Power:	+5V @ 1.03 A (with DDCs, Fs = 100 MHz)
	+3.3V @ 0.93 A (with DDCs, Fs = 100 MHz)

Specifications subject to change without notice

[1] The specified minimum sample rate is 30 MHz. The product can be operated at sample rates down to 5 MHz, but the performance is not guaranteed in this case.
[2] The SFDR & SNR specification is set-up dependent. Please refer to Application Note AN-SR-14. For best results ICS recommends the use of the external clock.

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2.2 Ruggedization Levels

The ICS-8552B is available in five build levels, each associated with a particular set of environmental specifications. These build levels are shown in Table 2.1.

Table 2.1 - ICS-8552B Build Levels

Level 1 Standard	
Operating Temperature	0 to 55˚C with 300 ft./min. airflow
Storage Temperature	-50 to + 100˚C
Vibration	$0.002g^2$/Hz from 10 to 2000 Hz random and 2g sinusoidal from 5 to 500 Hz
Shock	20g peak sawtooth, 11mS duration
Humidity	Up to 95% RH
Notes	Commercial grade, cooled by blown air; for use in benign environments and software development applications.
Level 2 Extended Temperature	
Operating Temperature	-20 to +65˚C with 300 ft./min. airflow
Storage Temperature	-50 to + 100˚C
Vibration	$0.002g^2$/Hz from 10 to 2000 Hz random and 2g sinusoidal from 5 to 500 Hz
Shock	20g peak sawtooth, 11mS duration
Humidity	Up to 95% RH with varying temperature, 10 cycles, 240 hours
Notes	Similar to Standard but conformally-coated and temperature characterized.
Level 3 Rugged Air-cooled	
Operating Temperature	-40 to +75˚C with 600 ft./min. airflow
Storage Temperature	-50 to + 100˚C
Vibration	$0.04g^2$/Hz from 10 to 2000 Hz, with a flat response to 1000 Hz, 6 dB/Octave roll-off from 1000 to 2000 Hz
Shock	20g peak sawtooth, 11mS duration
Humidity	Up to 95% RH with varying temperature, 10 cycles, 240 hours
Notes	Wide temperature rugged, cooled by blown air, conformally-coated for additional protection. Optional Environmental Stress Screening (ESS).
Level 4 Rugged Conduction-cooled	
Operating Temperature	-40 to +75˚C at the thermal interface
Storage Temperature	-50 to + 100˚C
Vibration	Random, $0.1g^2$/Hz from 5 to 2000 Hz per MIL-STD-810E
Shock	40g peak sawtooth, 11mS duration
Humidity	Up to 95% RH with varying temperature, 10 cycles, 240 hours
Notes	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling. Optional Environmental Stress Screening (ESS).
Level 5 Rugged Conduction-cooled	
Operating Temperature	-40 to +85˚C at the thermal interface
Storage Temperature	-50 to + 100˚C
Vibration	Random, $0.1g^2$/Hz from 5 to 2000 Hz per MIL-STD-810E
Shock	40g peak sawtooth, 11mS duration
Humidity	Up to 95% RH with varying temperature, 10 cycles, 240 hours
Notes	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling. Optional Environmental Stress Screening (ESS).

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2.3 Cooling of Convection-Cooled Boards

It is essential that the user provide adequate cooling air to the ICS-8552B when it is installed in the target system. Achieving high levels of analog performance at high speed requires the use of A/D converter products with substantial power consumption requirements. Higher power requirements translate to a greater requirement for heat dissipation. Build levels one through three are applicable to situations where a laminar flow of cooling air over each surface of the board is available, with the warm air being removed to the external environment. Build levels four and five are applicable to situations where no cooling air flow is expected, and the thermal/mechanical interface to the chassis metalwork will provide the path to sink heat to the outside environment.

Although the ICS-8552B can be operated in a commercial desktop type PC, the user should take careful precautions to ensure that overheating will not occur. Many PCI backplane/enclosure systems are not designed to provide a flow of cooling air to the boards. In some cases, a flow of air is provided through the case, but this may not directly cool the boards. In other situations, no cooling arrangements exist, apart from a fan in the power supply unit and a separate one for the CPU. However, this may not be possible to achieve at all times. We recommend that the user consider the following approaches:

1. If using a PCI backplane/enclosure system, select one that has been designed to provide a laminar flow of cooling air to the boards.
2. If using a PCI backplane/enclosure system, use a ‘fan card’ in a slot adjacent to the component side of the ICS-8552B. Examples of such products are listed in Reference [8] and [9].
3. If using a VME or cPCI backplane/enclosure system, use one that is generously designed with regard to the flow of cooling air, and use blanking plates in unused slots in order to ensure adequate flow of air to the board.

2.4 Power

As previously mentioned, achieving high levels of analog performance at high speed requires the use of A/D converter products with substantial power consumption requirements. Many backplane/enclosure products do not measure or limit the power consumption of each PCI slot; however, some products are now adding these limitations. When using a PCI backplane/enclosure/system, we therefore recommend that the user verify that the selected product will supply adequate power to the ICS-8552B, with a generous margin to allow for a surge when power is applied, and for variation with temperature.

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3 FUNCTIONAL DESCRIPTION

3.1 ADC Section

The ICS-8552B uses two 14-bit ADCs (TI ADS5424), which sample synchronously at frequencies of up to 105 MHz using either a 94.4 MHz fixed frequency on-board oscillator or an external frequency source. The specified minimum sampling rate for the converters is 30 MHz. The ICS-8552B operates at sampling rates as low as 5 MHz, however, the signal/noise performance is not guaranteed in this case. This board also provides programmable decimation of the ADC data stream by a factor of up to 32, making the effective minimum sampling rate 937.5 kHz. Decimation is accomplished by storing one out of every N samples where N is programmable from 1 to 32. Note that no filtering is performed prior to decimation when the optional DDC is bypassed. The full-scale input signal level is approximately 1.2 V peak-to-peak (+5.5 dBm) into 50 Ohms. The inputs to the converters are transformer coupled. The transformers have a lower cut-off frequency of approximately 2 MHz and an upper cut-off frequency that exceeds the bandwidth of the converter part. MMCX coaxial connectors are provided on the front panel for connecting the single-ended analog input signals. The connectors are marked as CH1 and CH2.

The outputs of the ADCs are passed to the User FPGA and to the digital downconverters (ICS-8552B-x00 version only). The selection of whether data is taken from the converters or from the DDC outputs is made within the User FPGA. When ADC output is selected, the data is presented as 2's complement (signed) 14-bit samples; these are justified to the most significant 14 bits of each 16-bit word within the 128K x 64-bit FIFO memories. When DDC output is selected, the standard User FPGA firmware stores the DDC output data as 2's complement (signed) 24-bit samples justified to the most significant 24 bits of each 32-bit word.

The ICS-8552B module may be configured to store data from a single ADC channel or from two channels. In either of these cases, the 14-bit or 16-bit data is packed so that the full capacity of the FIFO memories is used. The FIFO provides a bus matching feature so that data can be read out as 64-bit values at the maximum PCI 2.2 bus clock speed of 66 MHz regardless of the number of channels enabled. Thus, the ICS-8552B can be operated continuously without data loss when one channel is enabled.

3.2 Clock, Trigger and Sync Options

The ICS-8552B offers a number of options for selection of the clock, trigger and DDC synchronization signals.

The sampling clock may be either internal or external. The ICS-8552B has an on board temperature compensated crystal oscillator that provides a sample clock with a fixed frequency of 94.4 MHz.

The internal sampling clock has sufficient power to drive a total of four boards.

When using an external clock, a signal of the desired frequency must be applied before configuring the board. The signal is connected via the front panel MMCX connector marked CLK and is terminated on the board with a 50 Ohm resistive termination. When driving multiple boards, a power splitter should be used in order to maintain 50 Ohm characteristic impedance of all paths. The external clock signal must have a frequency between 30 and 105 MHz, and must be a continuous signal. It may be either a sinusoidal waveform with a level in the range –3 to +6 dBm into 50 Ohms, or a signal with TTL levels and drive capability. The drive should not exceed +13 dBm (2.85 Vpp) to avoid possible damage to the board. Sampling occurs on the rising edge of the external clock.

Due to the nature of the PLL clock generation circuitry used for generation of clocks for some parts of the digital circuitry, care should be taken to ensure that the PLL is locked before the ICS-8552B module is used. The user should therefore allow a delay of at least 1 microsecond after a stable clock signal has been supplied to the external clock input.

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The trigger can also be programmed to be internal or external. Internal triggering is effected by writing to the Trigger register. The internal trigger signal is output to the front panel TRIG connector to allow triggering of one or more of the ICS-8552B boards.

The external trigger signal is connected at the front panel MMCX TRIG connector, and may be programmed to be active on either the rising edge or falling edge using UCR1<01>. Sampling starts on the first rising edge of clock following the active transition of the trigger signal. The signal must remain in the state following the active edge for at least one clock cycle. The external trigger signal input will accept a low voltage TTL input (3.3V), but is tolerant of 5V TTL signals. The signal must conform to standard TTL drive capability.

The trigger signal is not terminated on the board. It is recommended that a source series termination of 50 Ohms be used.

Synchronization of the Digital Downconverters (DDCs), if installed, can also be programmed to be internal or external. In multiple board configurations, one board must be configured as the master, the others are slaves. The master board generates the DDC Sync signal and supplies it to the slaves by means of cables connected to the SYNC connectors. For a single board, it must be configured for internal sync. The GC4016 Sync Mode registers must be programmed to generate Sync on the master board, and to receive it on the slave boards.

3.3 Channel Allocation

The ICS-8552B provides the ability to select the number of channels to be used under software control. One or two channels may be selected. Table 3.1 summarizes the operation of the module with different numbers of channels enabled.

When one ADC channel is enabled, the ICS-8552B stores the data from ADC channel 1 into the FIFO1 memory. The maximum acquisition count is 512 Ksamples. The other channel is unused. When data is read over PCI Bus, only the data for channel 1 is read. The data output format over 64-bit PCI bus for one ADC channel mode is shown in Table 3.2.

When two ADC channels are enabled, the ICS-8552B stores the data from both ADC channels into both FIFO memories. The maximum acquisition count for either channel is 512 Ksamples. The data output format over 64-bit PCI bus for two ADC channels mode is shown in Table 3.2 and Table 3.3.

Table 3.1 - ICS-8552B ADC Channel Configuration without DDCs

Number of Channels	ADCs Used	FIFO1 Number of Channels	FIFO2 Number of Channels	ADC1 Acquisition Count	ADC2 Acquisition Count	UCR<10> Acq1 En	UCR<15> Acq2 En	Check ADC1 Interrupt	Check ADC2 Interrupt
1	1	1	Not used	Not used	Not used	Enable	Disable	YES	NO
2	1, 2	1	1	16 - 524287	16 - 524287	Enable	Enable	YES	YES

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Table 3.2 - Data Output Format for FIFO 1 (1 or 2 Channels Enabled, without DDCs)

Bit 63 48	**Bit 47 32**	**Bit 31 16**	**Bit 15 0**	**Sequence**
ADC1 Sample 1	ADC1 Sample 2	ADC1 Sample 3	ADC1 Sample 4	1
ADC1 Sample 5	ADC1 Sample 6	ADC1 Sample 7	ADC1 Sample 8	2
ADC1 Sample 9	ADC1 Sample 10	ADC1 Sample 11	ADC1 Sample 12	3
ADC1 Sample 13	ADC1 Sample 14	ADC1 Sample 15	ADC1 Sample 16	4
…	…	…	…	…
ADC1 Sample (AcqCount1 –3)	ADC1 Sample (AcqCount1 –2)	ADC1 Sample (AcqCount1 –1)	ADC1 Sample AcqCount1	AcqCount1/4

Table 3.3 - Data Output Format for FIFO 2 (2 Channels Enabled, without DDCs)

Bit 63 48	**Bit 47 32**	**Bit 31 16**	**Bit 15 0**	**Sequence**
ADC2 Sample 1	ADC2 Sample 2	ADC2 Sample 3	ADC2 Sample 4	1
ADC2 Sample 5	ADC2 Sample 6	ADC2 Sample 7	ADC2 Sample 8	2
ADC2 Sample 9	ADC2 Sample 10	ADC2 Sample 11	ADC2 Sample 12	3
ADC2 Sample 13	ADC2 Sample 14	ADC2 Sample 15	ADC2 Sample 16	4
…	…	…	…	…
ADC2 Sample (AcqCount2 –3)	ADC2 Sample (AcqCount2 –2)	ADC2 Sample (AcqCount2-1)	ADC2 Sample AcqCount2	AcqCount2/4

The format of the output data varies depending on which of the optional Digital Downconverters (DDCs) is used, if any. The data, whether 14-bit or greater resolution, is provided as a 2's-complement signed value justified to the most significant bits of each 16-bit part of the 64-bit word. For more information on DDC data output format, refer to Section 4.15.

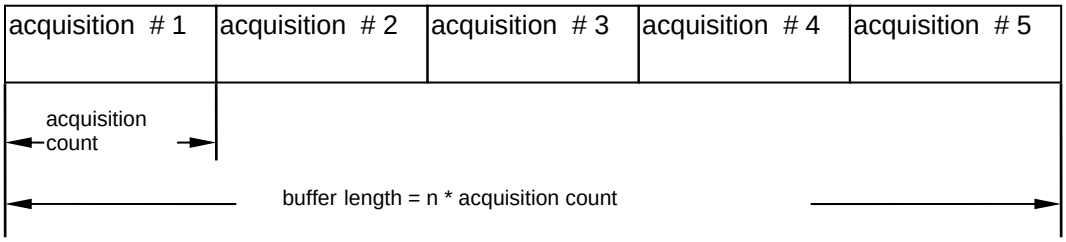
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3.4 Modes of Operation

Two modes of operation are provided by the ICS-8552B:

- Capture mode
- Continuous mode

In the Capture mode, data is acquired for a programmable number of samples following each application of the trigger. Because the size of the memory buffer and the count of samples acquired are both programmable, multiple capture acquisitions may be stored in the ICS-8552B memory before data is read from the board. Note that when using Capture mode, the memory buffer length programmed must always be an integral number of acquisition counts. If enabled, an interrupt (ADC interrupt) will occur after the number of samples acquired is equal to the programmed buffer length.



In the Continuous mode of operation, acquisition begins upon application of the trigger and continues until the board is disabled. If enabled, an interrupt (ADC interrupt) will occur each time the number of samples acquired since the trigger or since the last interrupt is equal to the programmed buffer length. The host processor must be capable of transferring data at a rate greater than or equal to the rate at which it is generated by the ADCs, or else data received by the host will not be continuous. The use of large programmed buffer lengths will help to ensure that data loss does not occur.

3.5 Digital Downconverters and the User FPGA

The ICS-8552B-x00 version of the product includes two Graychip GC4016 digital downconverter chips (DDCs). All versions of the product include a user-programmable Xilinx XC2V3000 Field Programmable Gate Array (FPGA). Figure 1 illustrates how these parts are connected.

A description of the functionality of the DDCs is given in Section 4. Programming details are given in the Graychip data sheet, Reference [5].

The ICS-8552B is shipped with a data crossbar switch loaded in the User FPGA. This enables the data input source for the FIFO memories to be selected as either the A/D converter outputs or the GC4016 outputs outputs, if installed. It also provides control over the data output format. It can be reprogrammed for other functions by the user. Approximately 95% of the logic slices of the three million gates part are still available for use by the user. There are 256 32-bit PCI Bus registers allocated within the ICS-8552B address map for access to the User FPGA in the case that programmable functions need to be implemented.

In order to program the User FPGA for user-defined functions, the user will need to purchase the ICS-8552B Hardware Development Kit (HDK) and the necessary Xilinx tools. The ICS-8552B HDK contains details of the User FPGA connections, signal functions and timing diagrams as well as the VHDL source code design file and Constraints file for the default code included in the User FPGA. A good understanding of the capabilities of the User FPGA is required in order to be able to successfully reprogram the device. The required functionality will need to be coded in VHDL, synthesized, simulated, compiled and loaded to the board by means of the JTAG port or via PCI bus.

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3.6 Buffer Length

The buffer almost full length (number of samples acquired) at which an ADC interrupt will occur is user programmable. In Capture mode, an interrupt will occur when the programmed almost full level has been acquired; this may be as a result of more than one trigger, if the Acquisition Count has been programmed to be a sub-multiple of the buffer length. In Continuous mode, an interrupt will occur every time the total number of samples in the buffer reaches the programmed almost full level. The relationship between the programmed acquisition count and buffer length depends on the output data format, which depends on the operating mode used. This relationship is described in Section 6.15. The buffer length is programmed using the FIFO Level Control register. The value must be programmed serially, one bit at a time (see Section 6.9).

3.7 PCI Bus Interface

The ICS-8552B implements a 64-bit, 66 MHz PCI bus Master/Slave interface compliant with the PCI 2.2 specification. It uses the QuickLogic QuickPCI™ QL5064 PCI Bus interface chip. The QL5064 includes a PCI core and a field-programmable gate array (FPGA). The PCI core implements the PCI protocol while the User FPGA contains a controller for the ICS-8552B local bus. This implementation enables the PCI bus and the internal local bus to operate at rates up to the full PCI bandwidth (528 MBytes/sec). The board uses the chain mode DMA channel in the QL5064 to read data from the board memory.

At power on, the operating system must set the PCI base addresses for the board using the standard PCI configuration procedure.

The ICS-8552B will operate in 64-bit mode and at 66 MHz clock speed on busses that support these options. The board accepts either 3.3V or 5V signaling and is keyed in accordance with Reference [3].

As shipped, the ICS-8552B uses PCI interrupts to indicate buffer almost full (i.e. data available to be read), ADC over range, and DMA transfer completion. The board also includes the capability to generate an interrupt based on the users coding of the User FPGA. Three bits in the ICS-8552B Interrupt Mask register allow the user to enable the interrupts for buffer almost full (ADC Interrupt), ADC over range (Over range Interrupt), and the User FPGA interrupt. Corresponding bits in the Status register indicate the status of these conditions. A PCI interrupt will occur when one of the IMR bits is set and the condition occurs. The interrupt handler must then clear the corresponding IMR bit to prevent a further interrupt from occurring. The ADC interrupt will occur, if enabled, when the number of samples acquired is equivalent to the value programmed to the Buffer Length register. In Continuous mode, the user must read data from the buffer in order to avoid data loss.

Target mode access to the ICS-8552B bus interface for transfer of data is not supported. The DMA engine on the board should always be used for data transfers.

Important Note: The ICS-855B orders data in 'Little-Endian' format, i.e. ascending Byte address read from LSB to MSB of the data. For Big-Endian host systems, endian conversion can be enabled within the QL5064 chip. The programmable feature allows the user to select the type of endian conversion to be applied to data transferred from the ICS-8552B to the PCI bus. This conversion is applied to data transferred by single cycle bus transfers and by DMA transfers. However, when using the linked-list (chain memory, scatter-gather) DMA capability of the QL5064, the chain memory data is located on host memory and must be reordered by the user using the appropriate endian conversion when it is written. Radstone Sensor Processing supplied software device drivers provide this conversion, except for that for Windows operating systems.

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3.8 Cascading Multiple Boards

The ICS-8552B provides simultaneous sampling across all channels on multiple boards. In order to achieve multiple board synchronization, one board is designated as the sampling Master, while the other boards are configured as Slave boards. An external sample clock must be used when simultaneous sampling is required across multiple boards. The user must supply the same clock signal to Master and Slave boards. The Master board provides a trigger and timing signals to the Slaves. All boards to be synchronized must be located in the same chassis in order not to violate signal timing requirements.

The ICS-8552B clock circuitry allows multiple board systems to have simultaneous triggering (+/- 0 samples) and less than 1.5 ns board to board sampling skew.

3.9 Light-Emitting Diodes

The ICS-8552B contains four light-emitting diodes (LEDs) which indicate board operation and error conditions. The LEDs are described in Table 3.4 and the location on the board is shown in Figure 2.

Table 3.4 - Light Emitting Diodes

	LED Function	**Color**	**Description**
DS1	ADC Running	Green	Illuminated for each ADC sample acquired
DS2	ADC Over range	Red	Illuminated when a ADC over range condition occurs (resulting in over range analog input)
DS3	FIFO Overflow	Red	Illuminates when the FIFO overflow condition occurs (resulting in lost data)
DS4	PCI access (local bus busy)	Green	Illuminated at each valid PCI Bus access to ICS-8552B

Note: The LED state is not latched. Therefore, the illumination level may not be sufficient to be visible for intermittent events.

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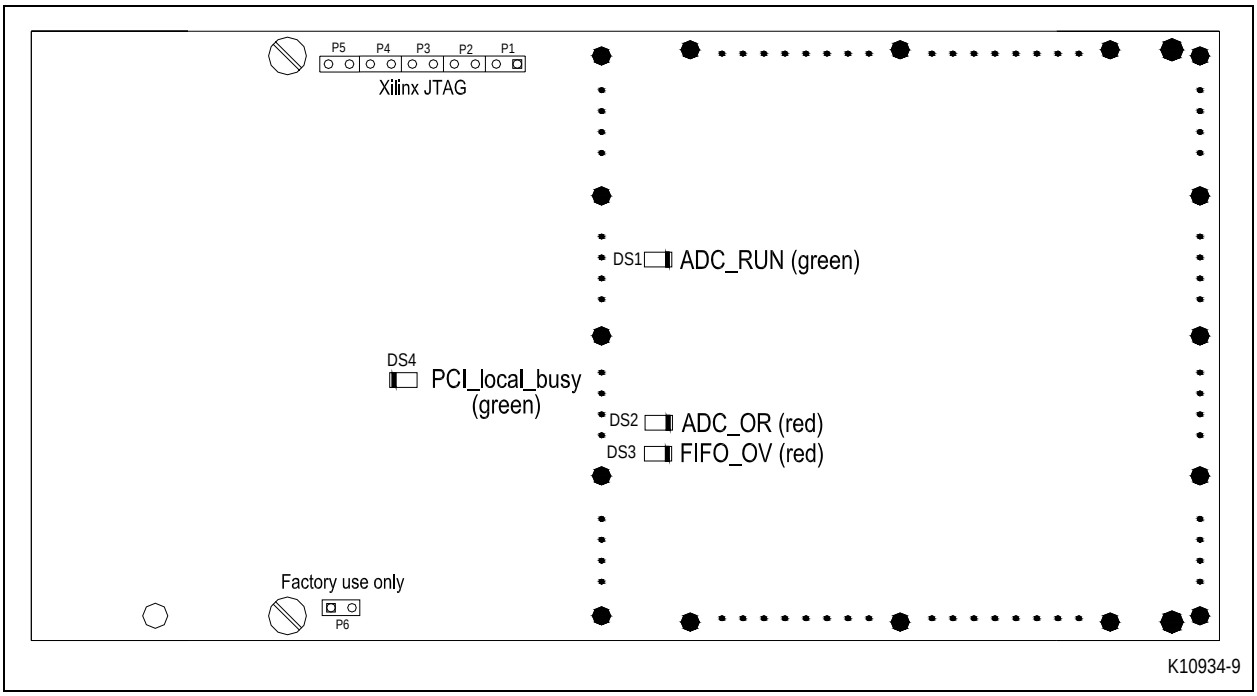


Figure 2 - Position of LEDs and JTAG Ports on ICS-8552B (Bottom View)

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4 OPTIONAL DDC FUNCTIONAL DESCRIPTION

4.1 General Description

The user should consult the Graychip documentation for a complete description of the GC4016 product, Reference [5]. This section provides an overview of the chip functionality and describes the data output formats available from the ICS-8552B.

The ICS-8552B-x00 version of the product includes up to two Graychip GC4016 Digital Down Converter (DDC) chips, each containing four identical down-conversion circuits, giving a total of up to 8 individual output channels. A block diagram of a single GC4016 device is shown in Figure 3.

The data inputs to each of the GC4016 chips consist of four independent 14-bit data buses routed from the User FPGA. Any of the output channels from the GC4016 chips may use either of the A/D input channels as its data source, or use digital data received from outside the card via the User I/O Pn4 interface (see the ICS-8552B HDK, Reference [10], for more information). Each GC4016 output channel can be configured to select and downconvert a signal band from the input data stream centered on a specific input frequency (the IF or carrier frequency).

Each of the four identical down-converters on the DDC chip accepts a real sample rate up to 100 MHz, down-converts a selected IF frequency to zero, filters the signal, decimates the signal rate by a programmable factor ranging from 32 to 16,384 and then optionally resamples the channel to adjust the sample rate up or down by an arbitrary factor. The GC4016 output data is usually presented in complex (I & Q) format, where the output spectrum is centered on DC. The chips also provide a real output mode where the output sample rate is doubled and the signal is output as a real signal centered at frequency Fout/4. The output channels on a DDC may be combined to produce wider band and/or oversampled outputs or to process complex input data. The chip contains two user programmable output filters per path which can be used to arbitrarily shape the received data's spectrum. These filters can be used as Nyquist receive filters for digital data transmission. The chip also contains a resampling filter to provide additional filtering and to allow the user complete flexibility in the selection of input and output sample rates.

Within a single chip, two downconverter paths can be merged to be used as a single complex input down-conversion circuit. Two paths may also be combined to support wider band output rates or oversampled outputs. Four paths may be combined to support both wider band output and oversampling, again, if the paths are located within the same chip. The downconverters are designed to maintain over 115 dB of spur free dynamic range and over 100 dB of out of band rejection. A five stage CIC and 20 bit internal data paths support this high dynamic range signal processing requirement. Each downconverter circuit accepts 14-bit inputs and produces 24-bit outputs. The ICS-8552B provides a feature to optionally truncate the 24-bit samples to 16 bits. The frequencies and phase offsets of the four sine/cosine sequence generators can be independently specified, as can the decimation and filter parameters of each circuit.

Since two DDC outputs feed into two FIFO memories, they may use different bandwidth (i.e. a different decimation factor). Each channel can be programmed independently for filter coefficients and input selection, centre (IF) frequency, phase and gain. Each downconverter channel contains three filters in sequence to lowpass filter and isolate the downconverted signal(s). Users have the option to download filter coefficient sets provided by Radstone Sensor Processing with the software device drivers for the ICS-8552B, or to use their own custom filter coefficients.

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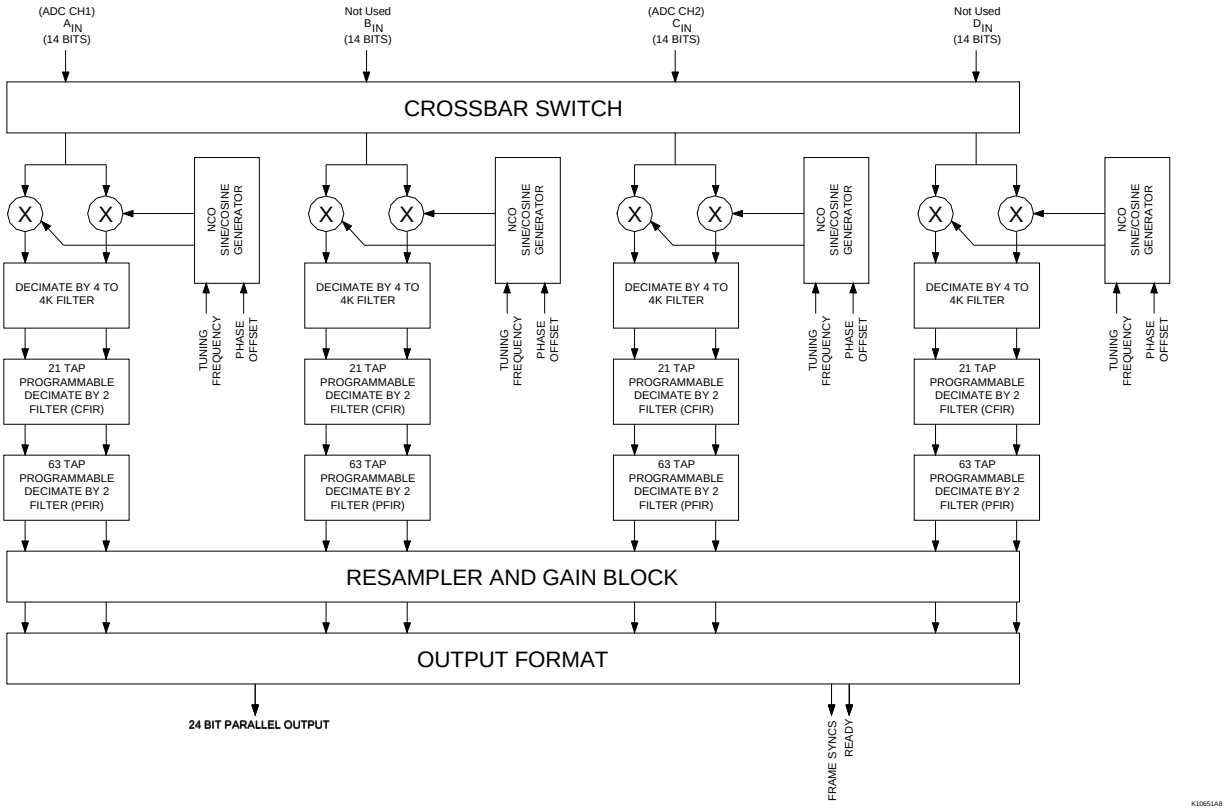


Figure 3 – GC4016 Block Diagram

4.2 Channel Configuration

The maximum signal bandwidth that can be processed by a single channel is dependant upon the clock frequency, the decimation ratio and the type of filter, or the filter coefficients. By combining channels, the signal bandwidth can be increased, as described below. The GC4016 provides a number of options for combining channels and converting the standard complex data output format to real data.

The DDCs in the Graychips contain multichannel mode functionality. The maximum single channel output bandwidth is approximately 2.5 MHz. This output bandwidth can be doubled by combining two channels using the Split-I/Q mode. Four channels may be combined to provide three to four times the single channel output bandwidth. Two channels can be combined to process complex input data, doubling the input bandwidth. Four channels can be combined to both process complex input data and to double the output bandwidth of the chip. Two or four multichannel modes may also be used in the complex to real mode.

Table 4.1 gives a summary of the channel output formats for each GC4016 mode. DDC output data formats are given in Section 4.15. A detailed description of the Channel Count register programming is given in Section 6.17. See Reference [5] for more information on GC4016 functionality.

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Table 4.1 – DDC operating modes

DDC Mode	**Signal bands stored in FIFO memory.**
Narrowband complex output	2,4,6,8
Narrowband real output	4,8
Split-I/Q complex output	2,4
Split-I/Q real output	2,4
Wideband complex output	1,2
Wideband real output	1,2
Narrowband pairs of complex input & complex output	2,4
Narrowband pairs of complex input & real output	2,4
Split-I/Q complex input & complex output	1,2
Split-I/Q complex input & real output	1,2

4.3 Detailed Description

Figure 4 illustrates the structure of a single downconverter channel; there are four such downconverters in each of the two DDC chips. A Numerically Controlled Oscillator (NCO) and mixer are used to quadrature downconvert a signal from the tuning frequency to baseband. The tuning frequency is specified as a 32-bit word and the phase as a 16-bit word. The tuning word TW is based on the formula:

$$TW=2^{32} \times F/Fck$$

where F is the desired tuning frequency and Fck is the input data rate (= programmed ADC sampling frequency).

A positive tuning frequency is normally used to downconvert the signal; however, a negative tuning frequency can be used to invert the output spectrum. Phase is set according to the following formula:

$$PH=2^{16} \times P/(2\pi)$$

where P specifies the desired phase in radians between 0 and 2π. The spur level of the NCO can be reduced when dithering is turned on, resulting in a significant improvement in SFDR of the output.

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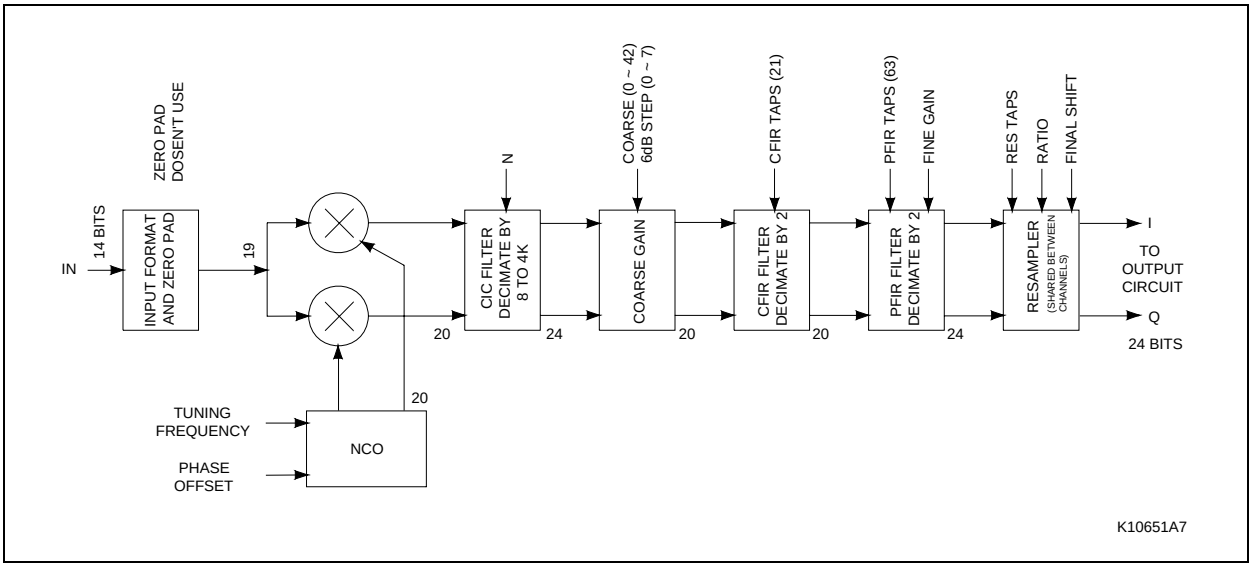


Figure 4 – GC4016 Block Diagram (Single Channel)

4.4 Input CrossBar

The crossbar switch allows the user to route any input source to any downconverter channel.

4.5 Input Scaling and CIC Filter

The CIC filter decimates the inputs from the NCO by a factor of N, where N is from 8 to 4K, and has a gain equal to N^5. The inputs have to be scaled before this filter to prevent overflow. This scaling is done in the shift down block indicated in Figure 4.

The shift down circuit has a gain equal to:

$$2^{(SHIFT+SCALE+6xBIG_SCALE-62)},$$

where the values for SHIFT, SCALE and BIG_SCALE are set in the Channel Reset and CIC Scale register and are common for all channels of the module. The overall gain of the shift down and CIC filter is given by the following formula:

$$GAIN = N^5 * 2^{(SHIFT+SCALE+6xBIG_SCALE-62)}$$

The user must select the values for SHIFT, SCALE and BIG_SCALE such that the overall gain (GAIN) is less than or equal one. Therefore (SHIFT+SCALE+6xBIG_SCALE) has to be less than or equal to (62-5xlog2(N)) otherwise the resulting overflow will go undetected.

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4.6 Coarse Gain

Coarse gain is set for each channel in the CFIR register (bits 4-6) and it can be used to boost the channel's gain by up to 42 dB. This is accomplished by shifting up the output of the CIC filter by 0 to 7 bits before rounding to 24 bits. The coarse gain is equal to 2^{COARSE}, where COARSE is the 3 register bits mentioned above. It is not recommended to change the coarse gain. See Section 4.10 for a description of the effect of this register on the overall gain of the chip.

4.7 Compensating FIR Filter

The output of the coarse gain circuit is filtered in the CFIR filter stage. This stage is a 21-tap decimate by 2 filters with programmable 16-bit coefficients. Since this filter decimates by two, a stopband must be created in that portion of the spectrum that would alias into the signal of interest. This filter has very lax transition band specifications so 21 taps is sufficient to both provide the required anti-aliasing stopband, and to provide compensation for the droop in the CIC filter's passband. The CFIR is also used, in some cases, to provide additional stopband rejection for the second stage PFIR filter.

The user downloaded filter coefficients are 16-bit 2's complement numbers. Unity gain will be achieved through the filter if the sum of the 21 coefficients is equal to 65536. If the sum is not 65536, then CFIR will introduce a gain equal to: CFIR_GAIN = CFIR_SUM/65536, where CFIR_SUM is the sum of the 21 coefficients.

The 21 coefficients are identified as coefficients h0 through h20, where h10 is the center tap. The coefficients are assumed to be symmetric, so only the first 11 coefficients (h0 through h10) are loaded into the chip. A non-symmetric mode (NO_SYM_CFIR) allows the user to download a 21-tap non-symmetric filter as taps h0 through h20. The newest sample is multiplied by h0 and the oldest is multiplied by h10.

Note: Filters normally multiply h0 by the oldest data; hence one may wish to reverse the tap order in the non-symmetric mode.

The CFIR has a programmable delay of one CFIR input sample. This delay is used in a multichannel mode to alter the decimation-by-two phasing in order to generate oversampled or wider bandwidth output data. This delay is independently programmable for each channel and is also independent for I and Q (QDLY_CFIR and IDLY_CFIR). A special mode (Split-I/Q) is also available where the CFIR generates two I outputs rather than one I and one Q.

Table 4.2 describes the CFIR coefficient sets included with Radstone Sensor Processing software device drivers. Users can also design their own CFIR coefficient sets and download them to the GC4016 chips. Note: Radstone Sensor Processing supplied device drivers compensate for the varying CFIR gain in the final gain stage, to within ±0.5 dB.

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Table 4.2 - CFIR Coefficient Sets included with Radstone Sensor Processing SDKs

Filter type	Descriptions	CFIR_GAIN (dB)
CFIR_80	80% usable output bandwidth (default setting)	-0.0882
CFIR_17	17% usable output bandwidth	6.1981
CFIR_34	34% usable output bandwidth	3.7668
CFIR_68	68% usable output bandwidth	2.0521
CFIR_100	100% usable output bandwidth	-0.8106
CFIR_150	150% usable output bandwidth (used for Wideband converter mode)	-0.7679
CFIR_GSM	GSM usable output bandwidth	-0.0001
CFIR_is95	IS-95 (NB-CDMA) usable output bandwidth	5.4309
CFIR_UMTS	UMTS (WB-CDMA) usable output bandwidth	-0.9381
CFIR_4014	GC4014 usable output bandwidth	-0.0012

4.8 Programmable FIR Filter

The second stage decimate by two filter is a 63-tap decimate-by-2 filter with programmable 16-bit coefficients. Fine gain is applied at the output of the PFIR and rounded to 24 bits. Overflows are detected and hard limited. Overflows can be directed to the channel overflow detection block. The PFIR filter passband must be flat in the region of the signal of interest, and have the desired out of band rejection in the region that will alias into the signal's bandwidth after decimation. The externally downloaded coefficients can be used to tailor the spectral response to the user's needs. For example, it can be programmed as a Nyquist (typically a root-raised-cosine) filter for matched filtering of digital data. The user downloaded filter coefficients are 16 bit 2's complement numbers. Unity gain will be achieved through the filter if the sum of the 63 coefficients is equal to 65536. If the sum is not 65536, then PFIR will introduce a gain equal to: PFIR_GAIN = PFIR_SUM/65536, where PFIR_SUM is the sum of the 63 coefficients.

The 63 coefficients are identified as coefficients h0 through h62, where h31 is the center tap. The coefficients are assumed to be symmetric, so only the first 32 coefficients (h0 through h31) are loaded into the chip. A non-symmetric mode (NO_SYM_PFIR) allows the user to download a 63 tap non-symmetric filter as taps h0 through h62. The newest sample is multiplied by h0 and the oldest is multiplied by h31. NOTE: Filters normally multiply h0 by the oldest data, hence one may wish to reverse the tap order in the non-symmetric mode.

PFIR also contains a one PFIR sample input delay that is independently programmable for the I and Q paths and for the four channels (QDLY_PFIR and IDLY_PFIR). The delay is used when combining channels to allow wider output bandwidth and/or more oversampling. It is also used for complex to real conversion in PFIR.

A fine gain is applied to the data after filtering and negation. The fine gain is a positive 14-bit integer (FINE) ranging from 0 to 16383. Fine gain is equal to: FINE_GAIN = FINE/1024. Setting FINE to zero will clear the channel.

Table 4.3 describes the PFIR coefficient sets included with Radstone Sensor Processing software device drivers. Users can also design their own PFIR coefficient sets and download them to the GC4016 chips. Note: Radstone Sensor Processing supplied SDKs compensate for the varying PFIR gain in the final gain stage, to within ±0.5 dB.

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Table 4.3 - PFIR Coefficient Sets included with Radstone Sensor Processing SDKs

Filter type	Description	PFIR_GAIN (dB)
PFIR_80	80% usable output bandwidth (default setting)	1.2094
PFIR_17	17% usable output bandwidth	9.9003
PFIR_34	34% usable output bandwidth	6.9933
PFIR_68	68% usable output bandwidth	1.6844
PFIR_100	100% usable output bandwidth	-0.7346
PFIR_150	150% usable output bandwidth (used for Wideband converter mode)	-3.9857
PFIR_GSM	GSM usable output bandwidth	3.3409
PFIR_is95	IS-95 (NB-CDMA) usable output bandwidth	2.6945
PFIR_UMTS	UMTS (WB-CDMA) usable output bandwidth	-0.5069
PFIR_UMTS_24x	UMTS (WB-CDMA) usable output bandwidth	3.0149
PFIR_DAMPS	IS-136 DAMPS usable output bandwidth	5.2095

4.9 Resampler

The resampler will independently filter and change the data rate of each channel. The most common application of the resampler is to increase the sample rate of the data so that it will match a desired symbol or bit rate. Demodulators for digital modulation schemes, such as GMSK, QPSK, QAM or CDMA, for example, require sample rates which are 1X, 2X, 4X or 8X times the bit or symbol rate of the modulation. In these cases, the maximum down converter filter performance is achieved when the PFIR output rate is around 1.5 to 2 times the signal's bandwidth. The resampler is then used to increase the sample rate up to the required 2X, 4X or 8X rate. The resampler can also be used as an additional filter to optimize the passband or stopband response of the channel.

An application example that uses the resampler is included with those supplied with Radstone Sensor Processing software drivers. For more information about resampler functionality refer to the GC4016 datasheet, Reference [5].

4.10 Optimal Gain Settings

The overall gain of each downconverter chip consists of the product of the CIC gain, coarse gain, CFIR gain, PFIR gain, final gain, resampler gain and final shift gain. The following is a summary of the contributions to the overall gain of each channel:

$$GAIN = \{N^5 2^{(SHIFT + SCALE + 6*BIG_SCALE - 62)}\}(2^{COARSE})(\frac{CFIR_SUM}{65536})(\frac{PFIR_SUM}{65536})(\frac{FINE_GAIN}{65536})(\frac{RES_SUM}{32768 * NDELAY})(2^{FINAL_SHIFT})$$

or

$$GAIN(dB) = 20*\lg(N^5 2^{(SHIFT+SCALE+6*BIG_SCALE-62)}) +$$
$$20*\lg(2^{COARSE}) + 20*\lg(\frac{CFIR_SUM}{65536}) + 20*\lg(\frac{PFIR_SUM}{65536}) + 20*\lg(\frac{RES_SUM}{32768*NDELAY}) + 20*\lg(2^{FINAL_SHIFT});$$

CIC gain = N^5 x $2^{(SHIFT+SCALE+6*BIG_SCALE-62)}$
This is the gain up to and including the CIC filter and is described in Section 4.5. This gain setting can be different to all 16 channels of the DDC chip.

Coarse Gain = 2^{COARSE}
This component is unique to each channel; it is described in Section 4.6.

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CFIR Gain = CFIR_SUM/65536
This is the gain introduced by the user-downloadable filter taps if their sum is not 65536.

PFIR Gain = PFIR_SUM/65536
This is the gain introduced by the user-downloadable filter taps if their sum is not 65536.

Fine Gain = FINE_GAIN/1024
The default setting of FINE_GAIN is Fine_Gain = 1024 which gives a gain of 0.0 dB. The adjustable range of Fine Gain is from -60.206 dB to 24.0819 dB (from 1 to 16384). It is recommended to change this value to match input and output gain.

Resampler Gain = RES_SUM/(32768*NDELAY)
Final Shift Gain = 2^{FINAL_SHIFT}
If bypassing the resampler and if Final Shift = 5, (resampler gain + Final Shift gain) should be set to unity in the gain equation. For more information refer to the GC4016 datasheet, Reference [5].

The signal data flows through these gain sections in the order given above. To optimize the dynamic range of the chip, each of these gain stages should be set so as to maximize the signal amplitude without clipping. Another factor that has to be taken into consideration is the tuning loss; this effectively halves the input amplitude. The tuning loss occurs after the CIC filter. To compensate for this loss, the product of the individual gain stages after the CIC filter should equal 2 for optimal performance.

4.11 DDC Module Configurations

Each GC4016 chip contains four independent channels and each channel can output complex data at sample rates up to Fck/32. Depending on the filter coefficients and the clock rate, the maximum single channel output bandwidth is just under 2 MHz. This output bandwidth can be doubled by combining two channels using the Split-I/Q mode. Four channels may be combined to provide 3 to 4 times the single channel output bandwidth (with reduced out of band rejection). The two or four multi-channel modes may also be used in the complex-to-real mode. Two channels can also be combined to process complex input data, thereby doubling the input bandwidth going into the chip. Four channels can be combined to both process complex input data and to double the output bandwidth of the chip.

4.11.1 8-Channel Narrow Band Configuration

Since each GC4016 chip contains four downconverter paths, the ICS-8552B can be configured for up to 8 downconverter channels in this mode. Each downconverter channel has individual input selection, tuning frequency, tuning phase, CFIR coefficients, PFIR coefficients and gain settings. The decimation of each channel is from 32 to 16384 and CIC decimation factor is from 8 to 4096. The outputs are normally complex sample pairs. Double rate real output can also be generated by using complex to real conversion. The output data format for complex data is as shown in Table 4.4. The output format for real data is shown in Table 4.5.

4.11.2 4-Channel Split-I/Q Configuration

Two channels work together in the Split-I/Q mode to double the output bandwidth of the downconverter. In the Split-I/Q mode, the real half of the complex output data is processed in one channel and the imaginary half in the other. The CIC has a minimum decimation of 4 instead of 8, which allows channel output at sample rates up to Fck/16. The two channels being combined in the Split-I/Q mode should be programmed identically, including the tuning frequency, except that the imaginary channel should have a +90 degree phase shift. The IONLY bit in the real channel should be set and the QONLY bit in the imaginary channel should be set. The decimation of each channel is from 16 to 8192 and CIC decimation factor is from 4 to 2048.

Typically the chip is configured in the Split-I/Q mode so that channels A and B are combined as one downconverter and C and D are combined as the other. Double rate real output can be generated by

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combining Split-I/Q and complex to real conversion. Note: in Split-I/Q and real output mode, the minimal CIC decimation factor is 5, while the minimal CIC decimation factor is 4 in Split-I/Q and complex output mode.

The ICS-8552B provide up to 4 Split-I/Q downconverter channels. The output data format for complex data is as shown in Table 4.6. The output format for real data is shown in Table 4.7.

4.11.3 2-Channel Wideband Configuration

Even wider output bandwidth is possible than is available using the modes described previously, by combining all four channels of a DDC. This is done by noticing that PFIR decimates the signal by two. If one pair of channels in the Split-I/Q mode are used to generate even time sample outputs and the other pair are used to generate odd time sample outputs, then the PFIR filter effectively does not decimate the signal. This allows a wider bandwidth filter to be used in the CFIR and PFIR. Adjacent channel rejection, however, will be reduced due to the increase in the output bandwidth relative to the CIC's stopbands. Also the increase in output bandwidth makes it harder for the CFIR and PFIR to achieve deep stop bands. The wide output mode uses the chip in the Split-I/Q mode. In addition the QDLY_PFIR bits are set in channels A and B. The delay of one input sample into the PFIR will offset the decimate by two operation so that the channel A and B outputs are the real and imaginary parts of the even time samples and the C and D outputs are the real and imaginary parts of the odd time samples. Double rate real output can be generated by combining wideband and complex to real conversion. The decimation of each channel is from 8 to 4094 and CIC decimation factor is from 4 to 2048. Note: in wideband and real output mode, the minimal CIC decimation factor is 5, while the minimal CIC decimation factor is 4 in wideband and complex output mode.

The ICS-8552B provide up to 2 wideband downconverter channels. The output data format for complex data is as shown in Table 4.8. The output format for real data is shown in Table 4.9.

4.11.4 4-Channel Complex Input Configuration

Complex input data can be processed using two channels. The real portion of the input (I_{IN}) is processed in one channel while the imaginary portion (Q_{IN}) is processed in the next channel. Channels A and B are described here, channels C and D can be combined as well. The desired mixer output is $I_{out} = (I_{IN}*\cos - Q_{IN}*\sin)$ and $Q_{out} = (I_{IN}*\sin + Q_{IN}*\cos)$. Channel A is used in the normal mode and will output ($I_{IN}*\cos$) and ($I_{IN}*\sin$). A 90 degree offset in channel B will cause channel B to output ($-Q_{IN}*\sin$) and ($Q_{IN}*\cos$). The desired result is achieved by adding the channel A outputs to the channel B outputs. The complex to real mode can be used in conjunction with the complex input mode. If both channels are configured as described, then the combined complex input downconverter will be in the complex to real mode. The decimation of each channel is from 32 to 16384 and CIC decimation factor is from 8 to 4096.

The ICS-8552B provide up to 4 pairs of complex input channels. The output data format is similar to the 8-channel Split-I/Q mode, shown in Table 4.6 for complex output and Table 4.7 for real output.

4.11.5 2-Channel Complex Input with Split-I/Q Configuration

The complex input and Split-I/Q modes can be combined. In this mode, channels A and D of each chip process the (I_{IN}) inputs, while channels B and C process the (Q_{IN}) input data. Channel A will output ($I_{IN}*\cos$) and channel B will output ($-Q_{IN}*\sin$), if its phase is set to 90 degrees. Channel C will output ($Q_{IN}*\cos$) and channel D will output ($I_{IN}*\sin$) if its phase is set to -90 degrees. The I_{out} output is formed by adding channel A to channel B, and the Q_{OUT} output is formed by adding channel C to channel D. The IONLY bits must be set for channels A and B, and the QONLY bits must be set for channels C and D. The complex to real mode can be added to this mode by delaying the I word by half (set QDLY_PFIR in channels A and B) and mixing by Fs/4. The decimation of each channel is from 16 to 8192 and the CIC decimation factor is from 4 to 2048. Note: When real output is selected in this mode, the minimum CIC decimation factor is 5, while the minimum CIC decimation factor for complex output is 4.

The ICS-8552B provide up to 2 Complex input channel pairs. The output data format is the same as for the 4-Channel Wideband mode shown in Table 4.8 for complex output and Table 4.9 for real output.

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4.12 DDC Decimation Setting

The total decimation through each GC4016 channel is the product of the CIC, CFIR and PFIR decimations. The CIC decimation ratio is programmable (=N), while the CFIR decimation is fixed at 2, and the PFIR decimation is either 2 or 1, depending on whether complex or real output is selected. The decimation is therefore equal to 4N for complex output, or 2N for real output. The output rate, and therefore the decimation, must be the same for all channels.

For a given bandwidth, the decimation factor should be as high as possible in order to avoid undesired frequency components within the passband. This is because the cut-off frequency of the low-pass filters is a function of the decimated output rate. The decimation should always be computed in relation to complex output data (output rate > bandwidth), bearing in mind that the output rate is doubled for real data.

The decimation (D) must be chosen according to the bandwidth (B) of interest:

$$D = INT [Fs/B]$$

and $D = 4N$

For complex output data, the output rate is given as follows:

$$Fo = Fs/D$$
$$= Fs/4N$$

and the output signal bandwidth is Fo.

For real output data, the output rate is given as follows:

$$Fo = Fs/D$$
$$= Fs/2N$$

and the output signal bandwidth is Fo/2.

Example:

Assume that the downconverters are clocked at 64 MHz and the decimation value is set to 16 in the CIC Decimation register of each chip. This gives a decimation factor of 64 overall, assuming the PFIR filter stage is set to decimate by 2 (complex output data). The CIC Decimation register must be set to D-1, in this case 15 for a decimation of 16. (This is automatically done if the Radstone Sensor Processing SDK is used). Also assume that the signal of interest is centered at 30 MHz and the aim is to tune to this signal.

With this tuning frequency the tuning word is equal to:

2^{32} x 30 MHz/64 MHz = 4,294,967,296 = 0x78000000

The 2's complement of this value (0x88000000) is loaded into the channels' frequency registers. The decimated output sample rate is 64 MHz/64 = 1 MHz. Assuming an 80% filter, the bandwidth is 1 MHz and usable bandwidth is 800 kHz. The complex output spectrum extends from -400 kHz to +400 kHz and it is represented as a sequence of I and Q sample pairs.

If real mode is selected with the same value programmed to the CIC Decimation register, the overall decimation will be 32. The output sample rate is 2 MHz.

The output spectrum (real) is now centered on 500 kHz and extends from 100 kHz to 900 kHz. The output data consists of a sequence of I samples.

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4.13 DDC Synchronization

All two GC4016 downconverter circuits must be synchronized for changes in decimation. Tuning frequency, phase, CFIR, PFIR and gain are also synchronized. This is accomplished by generating a sync pulse on one of the chips, and receiving it on the other three. Two registers must be correctly programmed to achieve this, the General Sync register and the Count Sync register.

The ICS-8552B requires that downconverter chip 1 is used to generate sync. Chips 1 and 2 must be programmed to receive sync from chip 1. The correct programming of the General Sync register and the Count Sync register is described in the section relating to those registers.

The design of the ICS-8552B also allows synchronization of DDCs on multiple modules. Cable/s must be connected between the Sync connectors of the modules to achieve this, and the modules must be configured as master/slave configuration, as described in Section 5 and 6 below.

4.14 DDC Module Output Spectrum

The organization of the DDC module output spectrum depends on the output mode, real or complex and on whether the tuning frequency is entered as a positive or negative number.

In Figure 4, the sampling frequency is represented as Fs and the tuning or centre frequency as F_T. The output rate will be:

Fo = Fs/Decimation,

where Decimation is the overall decimation of the downconverter.

In complex output mode, the tuning frequency, F_T, is translated to zero frequency at the output, and either the upper or lower sideband is located on the positive side of the frequency axis, depending on whether a negative or positive tuning frequency is programmed. The other sideband is present on the positive frequency axis, located above half the output frequency.

In real output mode, F_T is translated to F_C, where:

$F_C = 0.25Fo$

and the spectrum is centred on this frequency. It is either inverted or in original orientation depending on whether a positive or negative tuning frequency is programmed.

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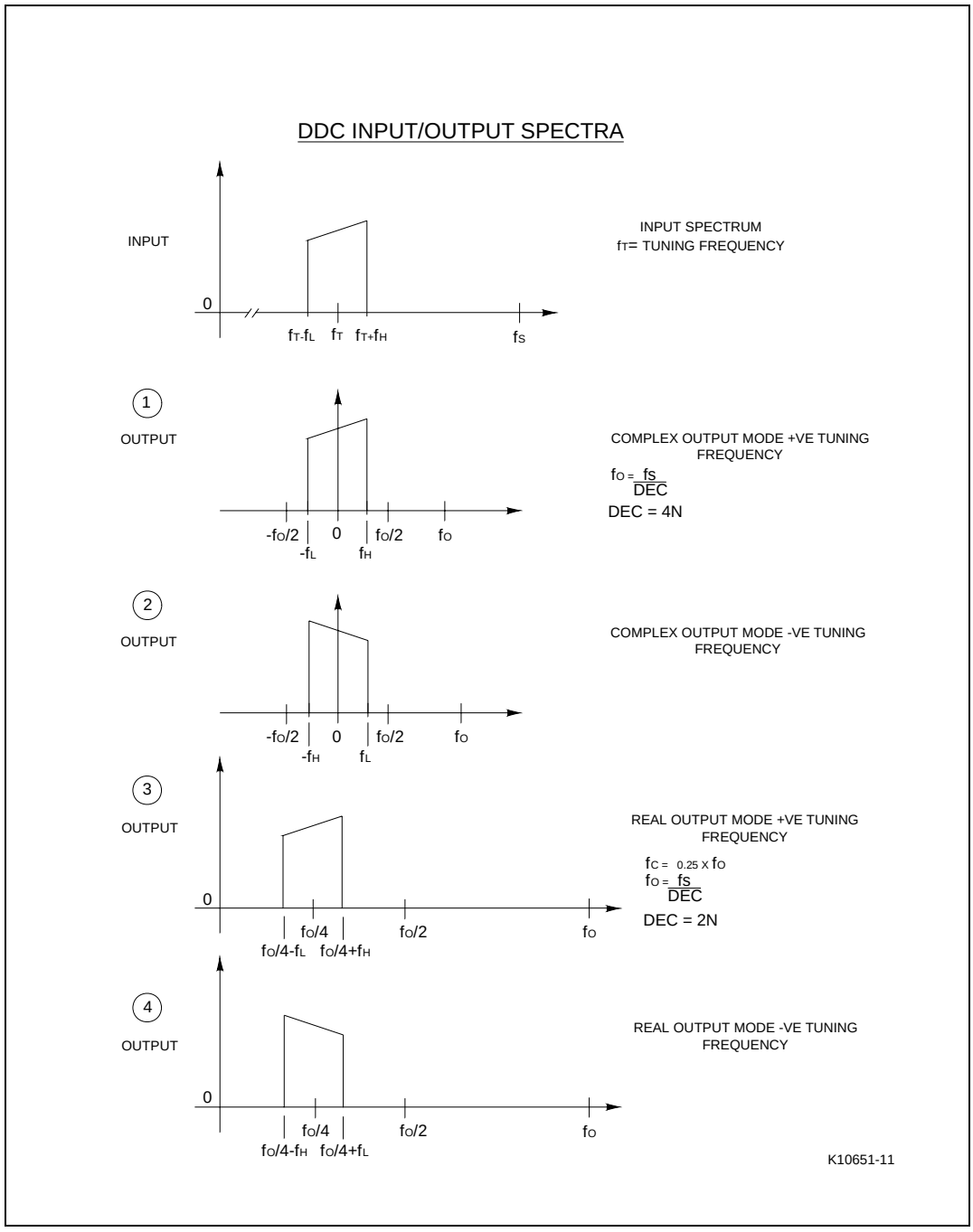


Figure 6 – ICS-8552B-x00 DDC Output Spectra

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4.15 DDC Data Output Format

The DDC output data is 24-bit 2's complement data. It is justified to the most significant 24 bits of each 32-bit part of the 64-bit PCI Bus word. The least significant eight bits of each 32-bit part are all set to ones. The ICS-8552B provide a feature to optionally truncate the 24-bit samples to 16 bits (see Section 6.14.11); 16-bit data may be rounded by setting the appropriate rounding control within the GC4016 devices, Reference [5].

The format of the data output varies depending on the GC4016 mode of operation, with regard to complex or real output data, mode of DDC operation (Narrow band, Split-I/Q, etc.) and number of output channels selected.

The following tables show the data format for the FIFO memory, when N DDC channels have been selected for output in the Channel Count register (see Section 6.17). Data is generated in frames, where a frame contains a defined format of samples from each active DDC channel (sometimes one sample for each channel, sometimes more than one sample). The number of output channels that can be selected depend on the mode of operation (Narrow band, Split-I/Q or Wide band); each table shows the output format for the maximum number of channels available in that mode. The number of channels supported in that mode is given beneath each table. When fewer than the maximum number are selected, channels are dropped from the end of the frame (i.e. Chip 2 Channel C is the first to be dropped when selecting 7 channels rather than the maximum 8, in Narrow band mode).

Table 4.4 – Data Output Format over 64-bit PCI Bus (32-bit Complex DDC Output, Narrow Band)

63 40	39 32	31 8	7 0	Frame Number	Sequence
Chip 1 Chan A I1	11111111	Chip 1 Chan A Q1	11111111	1	1
Chip 1 Chan B I1	11111111	Chip 1 Chan B Q1	11111111	1	2
Chip 1 Chan C I1	11111111	Chip 1 Chan C Q1	11111111	1	3
Chip 1 Chan D I1	11111111	Chip 1 Chan D Q1	11111111	1	4
Chip 1 Chan A I2	11111111	Chip 1 Chan A Q2	11111111	2	5
Chip 1 Chan B I2	11111111	Chip 1 Chan B Q2	11111111	2	6
Chip 1 Chan C I2	11111111	Chip 1 Chan C Q2	11111111	2	7
Chip 1 Chan D I2	11111111	Chip 1 Chan D Q2	11111111	2	8

N = 2, 4, 6, 8
Frame length = N/2 64-bit words

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Table 4.5 – Data Output Format over 64-bit PCI Bus (32-bit Real DDC Output, Narrow Band)

63 40	39 32	31 8	7 0	Frame Number	Sequence
Chip 1 Chan A I1	11111111	Chip 1 Chan B I1	11111111	1	1
Chip 1 Chan C I1	11111111	Chip 1 Chan D I1	11111111	1	2
Chip 1 Chan A I2	11111111	Chip 1 Chan B I2	11111111	2	3
Chip 1 Chan C I2	11111111	Chip 1 Chan D I2	11111111	2	4
Chip 1 Chan A I3	11111111	Chip 1 Chan B I3	11111111	3	5
Chip 1 Chan C I3	11111111	Chip 1 Chan D I3	11111111	3	6
Chip 1 Chan A I4	11111111	Chip 1 Chan B I4	11111111	4	7
Chip 1 Chan C I4	11111111	Chip 1 Chan D I4	11111111	4	8

N = 2, 4
Frame length = N/2 64-bit words

Table 4.6 – Data Output Format over 64-bit PCI Bus (32-bit Complex DDC Output, Split-I/Q)

63 40	39 32	31 8	7 0	Frame Number	Sequence
Chip 1 Chan A I1	11111111	Chip 1 Chan A Q1	11111111	1	1
Chip 1 Chan B I1	11111111	Chip 1 Chan B Q1	11111111	1	2
Chip 1 Chan A I2	11111111	Chip 1 Chan A Q2	11111111	1	3
Chip 1 Chan B I2	11111111	Chip 1 Chan B Q2	11111111	1	4
Chip 1 Chan A I3	11111111	Chip 1 Chan A Q3	11111111	2	5
Chip 1 Chan B I3	11111111	Chip 1 Chan B Q3	11111111	2	6
Chip 1 Chan A I4	11111111	Chip 1 Chan A Q4	11111111	2	7
Chip 1 Chan B I4	11111111	Chip 1 Chan B Q4	11111111	2	8

N = 8
Frame length = N/2 64-bit words

Table 4.7 – Data Output Format over 64-bit PCI Bus (32-bit Real DDC Output, Split-I/Q)

63 40	39 32	31 8	7 0	Frame Number	Sequence
Chip 1 Chan A I1	11111111	Chip 1 Chan A I2	11111111	1	1
Chip 1 Chan B I1	11111111	Chip 1 Chan B I2	11111111	1	2
Chip 1 Chan A I3	11111111	Chip 1 Chan A I4	11111111	2	3
Chip 1 Chan B I3	11111111	Chip 1 Chan B I4	11111111	2	4

N = 4
Frame length = N/2 64-bit words

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Table 4.8– Data Output Format over 64-bit PCI Bus (32-bit Complex DDC Output, Wide Band)

63 40	39 32	31 8	7 0	Frame Number	Sequence
Chip 1 I1	11111111	Chip 1 Q1	11111111	1	1
Chip 1 I2	11111111	Chip 1 Q2	11111111	1	2
Chip 1 I3	11111111	Chip 1 Q3	11111111	1	3
Chip 1 I4	11111111	Chip 1 Q4	11111111	1	4
Chip 1 I5	11111111	Chip 1 Q5	11111111	2	5
Chip 1 I6	11111111	Chip 1 Q6	11111111	2	6
Chip 1 I7	11111111	Chip 1 Q7	11111111	2	7
Chip 1 I8	11111111	Chip 1 Q8	11111111	2	8

N = 8
Frame length = N/2 64-bit words

Table 4.9 – Data Output Format over 64-bit PCI Bus (32-bit Real DDC Output, Wide Band)

63 40	39 32	31 8	7 0	Frame Number	Sequence
Chip 1 I1	11111111	Chip 1 I2	11111111	1	1
Chip 1 I3	11111111	Chip 1 I4	11111111	1	2
Chip 1 I5	11111111	Chip 1 I6	11111111	2	3
Chip 1 I7	11111111	Chip 1 I8	11111111	2	4

N = 4
Frame length = N/2 64-bit words

Table 4.10 – Data Output Format over 64-bit PCI Bus (16-bit Complex DDC Output, Narrow band)

63 48	47 32	31 16	15 0	Frame Number	Sequence
Chip 1 Chan A I1	Chip 1 Chan A Q1	Chip 1 Chan B I1	Chip 1 Chan B Q1	1	1
Chip 1 Chan C I1	Chip 1 Chan C Q1	Chip 1 Chan D I1	Chip 1 Chan D Q1	1	2
Chip 1 Chan A I2	Chip 1 Chan A Q2	Chip 1 Chan B I2	Chip 1 Chan B Q2	2	3
Chip 1 Chan C I2	Chip 1 Chan C Q2	Chip 1 Chan D I2	Chip 1 Chan D Q2	2	4

N = 2, 4, 6, 8
Frame length = N/2 64-bit words

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Table 4.11 – Data Output Format over 64-bit PCI Bus (16-bit Real DDC Output, Narrow Band)

63 8	47 32	31 8	7 0	Frame Number	Sequence
Chip 1 Chan A I1	Chip 1 Chan B I1	Chip 1 Chan C I1	Chip 1 Chan D I1	1	1
Chip 1 Chan A I2	Chip 1 Chan B I2	Chip 1 Chan C I2	Chip 1 Chan D I2	2	2
Chip 1 Chan A I3	Chip 1 Chan B I3	Chip 1 Chan C I3	Chip 1 Chan D I3	3	3
Chip 1 Chan A I4	Chip 1 Chan B I4	Chip 1 Chan C I4	Chip 1 Chan D I4	4	4

N = 2, 4
Frame length = N/2 64-bit words

Table 4.12 – Data Output Format over 64-bit PCI Bus (16-bit Complex DDC Output, Split-I/Q)

63 48	47 32	31 16	15 0	Frame Number	Sequence
Chip 1 Chan A I1	Chip 1 Chan A Q1	Chip 1 Chan B I1	Chip 1 Chan B Q1	1	1
Chip 1 Chan A I2	Chip 1 Chan A Q2	Chip 1 Chan B I2	Chip 1 Chan B Q2	1	2
Chip 1 Chan A I3	Chip 1 Chan A Q3	Chip 1 Chan B I3	Chip 1 Chan B Q3	2	3
Chip 1 Chan A I4	Chip 1 Chan A Q4	Chip 1 Chan B I4	Chip 1 Chan B Q4	2	4

N = 8
Frame length = N/2 64-bit words

Table 4.13 – Data Output Format over 64-bit PCI Bus (16-bit Real DDC Output, Split-I/Q)

63 48	47 32	31 16	15 0	Frame Number	Sequence
Chip 1 Chan A I1	Chip 1 Chan A I2	Chip 1 Chan B I1	Chip 1 Chan B I2	1	1
Chip 1 Chan A I3	Chip 1 Chan A I4	Chip 1 Chan B I3	Chip 1 Chan B I4	2	2
Chip 1 Chan A I5	Chip 1 Chan A I6	Chip 1 Chan B I5	Chip 1 Chan B I6	3	3
Chip 1 Chan A I7	Chip 1 Chan A I8	Chip 1 Chan B I7	Chip 1 Chan B I8	4	4

N = 4
Frame length = N/2 64-bit words

Table 4.14 – Data Output Format over 64-bit PCI Bus (16-bit Complex DDC Output, Wide Band)

63 48	47 32	31 16	7 0	Frame Number	Sequence
Chip 1 I1	Chip 1 Q1	Chip 1 I2	Chip 1 Q2	1	1
Chip 1 I3	Chip 1 Q3	Chip 1 I4	Chip 1 Q4	1	2
Chip 1 I5	Chip 1 Q5	Chip 1 I6	Chip 1 Q6	2	3
Chip 1 I7	Chip 1 Q7	Chip 1 I8	Chip 1 Q8	2	4

N = 8
Frame length = N/2 64-bit words

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Table 4.15 – Data Output Format over 64-bit PCI Bus (16-bit Real DDC Output, Wide Band)

63 48	47 32	31 16	15 0	Frame Number	Sequence
Chip 1 I1	Chip 1 I2	Chip 1 I3	Chip 1 I4	1	1
Chip 1 I5	Chip 1 I6	Chip 1 I7	Chip 1 I8	2	2
Chip 1 I9	Chip 1 I10	Chip 1 I11	Chip 1 I12	3	3
Chip 1 I13	Chip 1 I14	Chip 1 I15	Chip 1 I16	4	4

N = 4
Frame length = N/2 64-bit words

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5 HARDWARE CONFIGURATION

All clock, trigger, and sync source configuration of the ICS-8552B are accomplished through the use of FET switches, under software control. The user is not required to move wire links, or set jumpers in order to configure the control inputs of the card. The only feature controlled by a switch setting is the selection of signaling levels used on the User I/O Pn4 connection of the ICS-8552B. These are determined by setting the switches as shown in Figure 5.

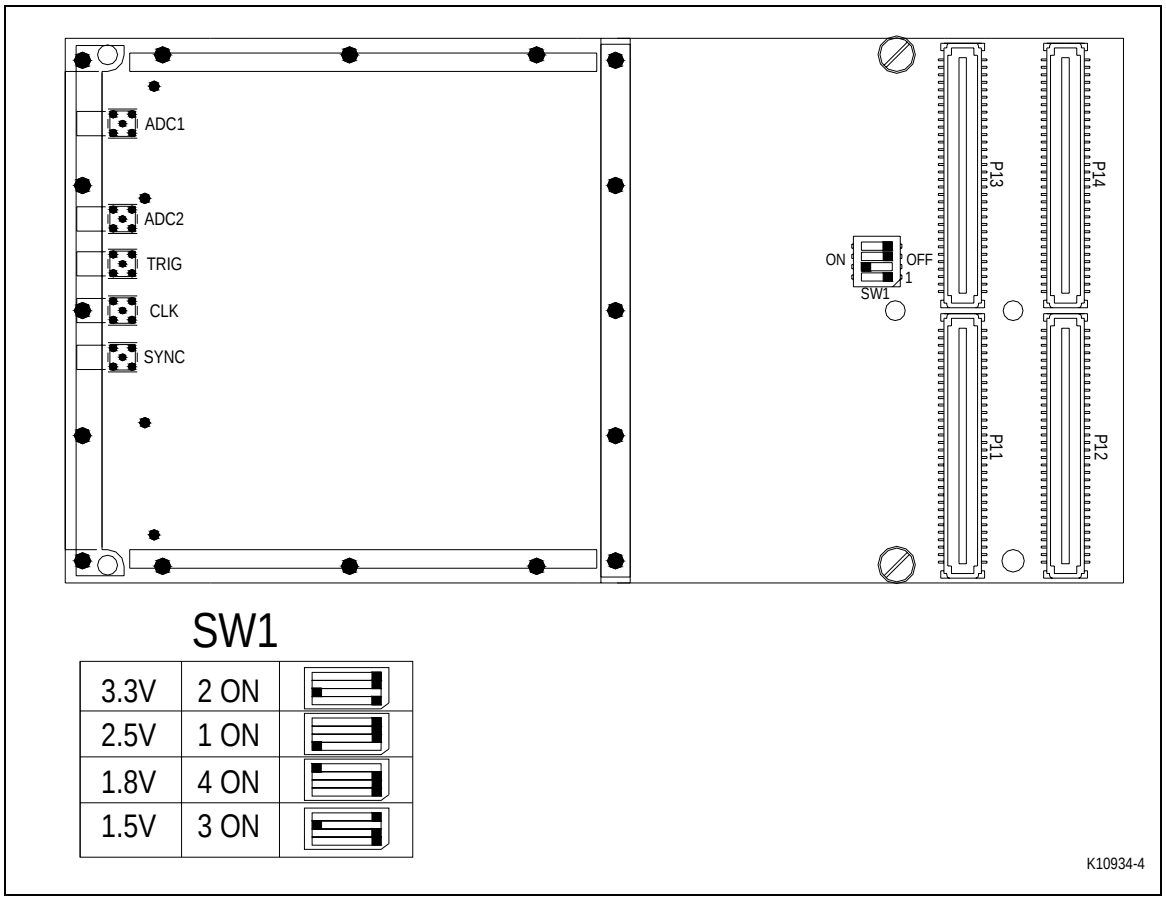


Figure 5 - ICS-8552B Switch Location and Default Setting

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6 PROGRAMMING MODEL

The ICS-8552B is controlled by means of memory-mapped registers accessed through the PCI bus interface. The PCI address map is summarized in Table 6.1. The ICS-8552B register set is listed in Table 6.2 and the register bit allocations are given in Figure 6.

Data should be read from the PCI Bus interface using the chain mode DMA controller of the QL5064, as described in Section 6.2. However, it is also possible to read data by means of target mode access to the memory space of the board.

A detailed description of the QL5064 register and bit allocations is given in Reference [4].

Note: All programming and control of the ICS-8552B is accomplished through the PCI Bus interface using 64-bit or 32-bit transfers. All control register bits that are not defined have no effect on the operation of the boards. All undefined bits may be read as zero or one.

Table 6.1 - PCI Address Map (Summary)

Name	PCI address	Description	Size
QL5064 Internal registers	PCI_BASE0		4 KBytes
QL5064 Configuration Space 1	PCI_BASE0+ 0x00-0xFF	QL5064 control registers. Memory space, 32-bit addressing	256 Bytes
QL5064 Configuration Space 2	PCI_BASE0+ 0x1000-0x10FF	QL5064 control registers (User FPGA side). Memory space, 32-bit addressing	256 Bytes
ICS-8552B Register Set	PCI_BASE1+ 0x000-0xFFF	ICS-8552B register access. Memory space, 32-bit addressing	4 KBytes
ICS-8552B Memory Space	PCI_BASE2+ 0x0000000-0x3FFFFFF	ICS-8552B buffer memory access	16 MBytes

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Table 6.2 - ICS-8552B Address Map

Register	PCI Bus Address	Type
ICS-8552B Register Set	PCI_BASE1	
Status Register	PCI_BASE1 + 0x000	Read/Write
Interrupt Mask Register	PCI_BASE1 + 0x008	Read/Write
Control Register 1	PCI_BASE1 + 0x010	Read/Write
Control Register 2	PCI_BASE1 + 0x018	Read/Write
JTAG Program Register	PCI_BASE1 + 0x020	Read/Write
FIFO Level Control Register	PCI_BASE1 + 0x0D8	Write Only
Trigger Register	PCI_BASE1 + 0x0E0	Write Only
ADC Reset Register	PCI_BASE1 + 0x0F0	Write Only
Board Reset Register	PCI_BASE1 + 0x0F8	Write Only
GC4016 Configuration Registers	PCI_BASE1 + 0x100 - 0x1F8	Read/Write
User Programmable FPGA Registers	PCI_BASE1 + 0x800 - 0xFF8	Read/Write
User Status Register	PCI_BASE1 + 0x810	Read Only
User Control Register	PCI_BASE1 + 0x818	Read/Write
ADC1 Acquisition Count Register	PCI_BASE1 + 0x820	Read/Write
ADC1 Decimation Register	PCI_BASE1 + 0x830	Read/Write
Channel Count Register	PCI_BASE1 + 0x838	Read/Write
ADC2 Acquisition Count Register	PCI_BASE1 + 0x840	Read/Write
ADC2 Decimation Register	PCI_BASE1 + 0x850	Read/Write
ICS-8552B Memory Space		
DATA FIFO1	PCI_BASE2 + 0x00000000	Read Only
DATA FIFO2	PCI_BASE2 + 0x00800000	Read Only

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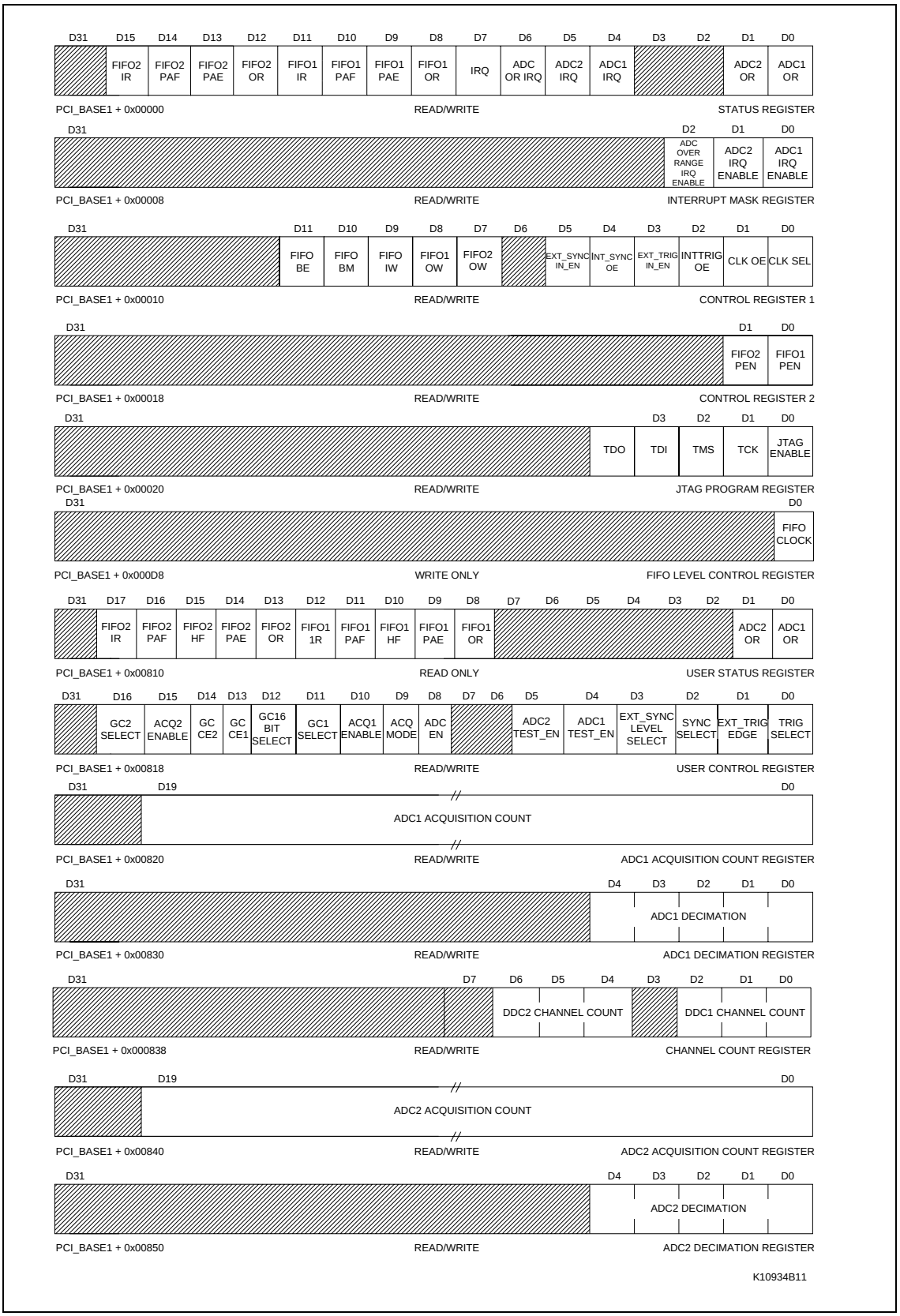


Figure 6 - ICS-8552B Register Map

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6.1 QL5064 Registers

The ICS-8552B uses the QuickLogic QL5064 PCI Bus interface chip. The QL5064 is an FPGA containing a PCI interface core. The QL5064 register set is complex, and a complete description is not given here. Details of the QL5064 may be found in the QL5064 data sheet, Reference [4].

As with any PCI Bus device, the QL5064 has a unique 256 Byte region called the Configuration Header Space, or just Configuration Space (see References [3] and [4]). It is mandatory that portions of this configuration header are addressable in order for a PCI agent to be in full compliance with the PCI specification. For ICS-8552B device registers to be addressable, it is necessary that information in the configuration space is read. Base address values and lengths must then be written to registers also in configuration space. This is normally done by the operating system.

The ICS-8552B use three of the available base address registers defined by the PCI specification for access the module. These base address registers, and the lengths assigned to the corresponding mapped areas of PCI address space are given in Table 6.1. The space addressed by PCI_BASE1 is split into two areas of 256 Bytes, with an unused area between them.

The QL5064 registers are described in Table 6.3.

The vendor and sub-vendor information contained in the PCI configuration space is as follows:

Vendor ID: 0x11E3
Device ID: 0x0006
Sub-vendor ID: 0x1464
Sub-system ID: 0x8552

6.2 Endian Conversion

Endian ordering refers to the significance with which data is ordered within a computer system. The ICS-8552B implements ‘Little-Endian’ ordering of data within larger data widths. When operating the boards within a PC or Intel-based system, no endian conversion will be required, since these are little-endian systems. In Little-Endian systems, the highest address is applied to the most significant byte (or word) of data of a given size; in Big-Endian systems (e.g. most Unix-based systems such as Sparc and PowerPC), the lowest address is applied to the most significant bytes (or word) of data in an element of data of a given size. The QL5064 interface provides ‘endian’ conversion for Big-Endian systems for a variety of data types. This feature results in 8-bit, 16-bit or 32-bit word order being reversed within larger word sizes (16-bit, 32-bit or 64-bit). The selection of endian function is made in the QL5064 Control register, address offset 0x1008 (see Table 6.3). Table 6.4 describes the effects of the various settings of this register.

The endian ordering should be set according to the type of system in which the ICS-8552B is installed and the bus width employed (32-bit or 64-bit). The most commonly used settings are shown in bold type in Table 6.4.

Note: When using chain-mode DMA (see Section 6.3), the linked list data must be reordered by the user before being written to host memory, when using a Big-endian host. This is because the data is read directly by the DMA controller without being passed through the endian conversion hardware.

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6.3 Performing DMA Transfers

When reading data from the board through the PCI interface, the DMA controller in the QL5064 is used. The controller can be used with or without chain mode (scatter-gather) operation. The QL5064 should normally be the PCI bus master (initiator) for transfers. When using chain mode DMA, the DMA controller requires the chain mode descriptor tables to be located in PCI addressable memory. This is usually located in the host processor. Please note that the starting PCI target address must be quadword (8 Byte or 64-bit) aligned for correct DMA mode operation.

The QL5064 PCI core uses the Transmit 0 DMA channel to move data from the ICS-554 to PCI Bus. The DMA engine supports both transmit and receive functions, but the ICS-554 does not use the receive function.

6.3.1 Non-Chain Mode DMA operation

To use DMA without scatter-gather, the QL5064 DMA controller must be programmed with the PCI Bus starting address for the target data, the source (ICS-8552B local memory) starting address, which is 0x000000 for FIFO 1, and 0x800000 for FIFO 2, and the length of the transfer. The length programmed should not exceed the amount of data available in the FIFO.

The steps required to start Transmit 0 DMA operation for writing data to the ICS-8552B are as follows:

1. Write the starting PCI target address to QL5064 control register "Master Write Address 0" (offset 0x00).
2. Write the transfer count (in bytes) to QL5064 control register "Master Write Transfer Count 0" (offset 0x08, bits [31:0]. The minimum transfer count is 8 Bytes (8 Bytes or 1 Quadword). The maximum transfer count is equal to the FIFO programmed almost full level. Transfers must always be in multiples of 8 Bytes. The transfer must be Quadword (8 Byte) aligned.
3. Write the transfer count and starting Local address to the ICS Local Bus control register LOC_XMT0_CNT_ADDR (offset 0x1010). The transfer count written to this register must be the same as that written to the Master Write Transfer Count 0 register (offset 0x08). The starting local address must be quad word (8 Byte) aligned.
4. To start the DMA transfer, write a "1" to the QL5064 control register DMA Control register Start/Done bit (offset 0x90, bit 16).
5. The transfer will continue until the transfer count expires or is cancelled.

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Table 6.3 - QL5064 Control Registers

Register	Offset (PCI_BASE0)	Type	Width (bits)	Description
Master Write Address 0	0x00	R/W	64	PCI address for write to PCI target
Master Write Transfer Count 0	0x08	R/W	32	Write transfer count in Bytes
Master Read Address 0 / Chain Descriptor Start Address	0x48	R/W	64	PCI address for read from PCI target / pointer to first chain descriptor PCI start address
Master Read Transfer Count 0	0x50	R/W	32	Read transfer count in Bytes
FIFO Level Controls	0x68	R/W	64	Almost full and almost empty levels for 6 FIFOs Recommended setting is 0x0008.0020.0020.001B
DMA Control	0x90	R/W	64	Set Bit 16 to start Transmit 0 DMA transfer Set Bit 18 to start Receive 0 DMA transfer Set Bit 20 to start Chain Mode DMA transfer
Board Reset	0xE8	W	1 (bit 0)	Write 1 - perform a Host Total Reset Write 0 - no effect
Control Register	0x1008	R/W	8	[01:00] must be 00
LOC_XMT0_CNT_ADDR	0x1010	R/W	64	[31:00] Local Start Address for DMA Transmit 0 [63:32] Transfer count in Bytes
LOC_RCV0_CNT_ADDR	0x1020	R/W	64	[31:00] Local Start Address for DMA Receive 0 [63:32] Transfer count in Bytes
LOC_DMA_CANCEL	0x1030	W	8	Write 1 to this register to cancel unfinished DMA

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Table 6.4 - Endian Conversion when Transferring Data from ICS-8552B Local Bus to PCI Bus

PCI Bus		**AD[63:56]**	**AD[55:48]**	**AD[47:40]**	**AD[39:32]**	**AD[31:24]**	**AD[23:16]**	**AD[15:8]**	**AD[7:0]**
	CR<5:2>								
ICS Local Data Bus	**0000**	**LD[63:56]**	**LD[55:48]**	**LD[47:40]**	**LD[39:32]**	**LD[31:24]**	**LD[23:16]**	**LD[15:8]**	**LD[7:0]**
	0001	**LD[31:24]**	**LD[23:16]**	**LD[15:8]**	**LD[7:0]**	**LD[63:56]**	**LD[55:48]**	**LD[47:40]**	**LD[39:32]**
	0010	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]
	0011	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]
	0100	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]
	0101	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]
	0110	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]
	0111	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]
	1000	**LD[7:0]**	**LD[15:8]**	**LD[23:16]**	**LD[31:24]**	**LD[39:32]**	**LD[47:40]**	**LD[55:48]**	**LD[63:56]**
	1001	**LD[39:32]**	**LD[47:40]**	**LD[55:48]**	**LD[63:56]**	**LD[7:0]**	**LD[15:8]**	**LD[23:16]**	**LD[31:24]**

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6.3.2 Chain Mode DMA Operation

The following steps are required to use chain mode DMA:

1. Write the chain mode DMA descriptor tables to PCI memory. The format of the Chain Mode DMA descriptor tables is given in Figure 7. The requirements for Local Starting Address and Transfer Count in the chain descriptors are the same as for non-chain mode DMA. If the host is a 'Big-Endian' machine, it will be necessary to reorder the descriptor data, as described in Section 6.2. The usual reordering required is byte order within 64-bit words. However, this may vary depending on the details of the system implementation.
2. Write the PCI address of the first descriptor pointer to QL5064 control register 'Master Read Address/Chain Descriptor Start Address' (PCI offset 0x48).
3. Start execution of the instructions in the descriptor tables by writing '1' to 'Chain Enable' (PCI offset 0x90, bit [20]).
4. The chain mode DMA will run until the end-of-chain flag is encountered or until the DMA transfer is cancelled.

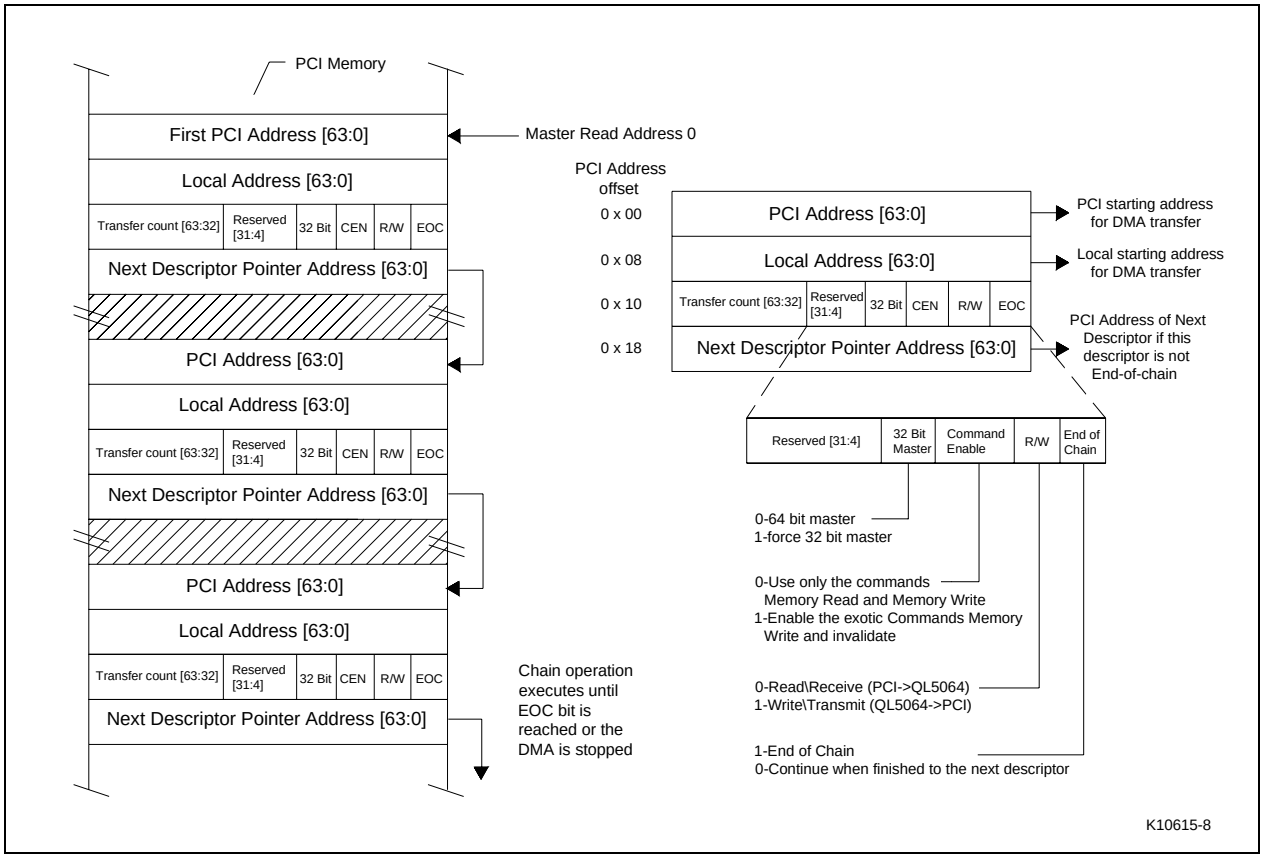


Figure 7 – DMA Chain Mode Descriptors

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6.3.3 Canceling a DMA Transfer

It may become necessary to cancel a DMA transfer that is in progress, for example if a time out has occurred. The procedure for doing this is as follows:

1. Cancel DMA in QL5064 core (see Reference [4]).
2. Write 1 to the LOC_DMA_CANCEL register (see Table 6.3).

The order of operations shown above must be observed.

6.3.4 PCI Target Mode

The ADC data area is mapped to PCI Base Address 2 (PCI_BASE2 – see Table 6.3). The host may read data from this area as a PCI slave device rather than use the ICS-8552B DMA engine. However, the transfer rate achievable is very limited. The ICS-8552B do not support target mode DMA, so a DMA engine on the host device may not be used; only single cycle reads are supported. The maximum length read must not exceed the programmed buffer length.

This area of the memory map is not configured to be pre-fetchable. In one PCI read transaction, only one word is read from the board. If the transaction is in 32-bit PCI bus mode, a 32-bit word is read. If the transaction is in 64-bit PCI bus mode, a 64-bit word is read.

6.4 Status Register (SR)

Some bits Read Only, Some bits Read/Write

The Status Register contains information about the state of the ICS-8552B. It is used to determine the interrupt status of the ICS-8552B, and the source of the interrupt. It also contains error condition information.

6.4.1 SR<00> - ADC1 OR

This bit indicates that an analog input over range condition has occurred on ADC channel 1. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the ADC Over Range bits to determine on which channel the over range occurred. This bit is latched; to clear it, a 1 must be written to it.

SR<00>	**ADC1 Over Range**
READ/WRITE	
0	No over range has been detected at ADC channel 1
1	Over range has been detected at ADC channel 1

6.4.2 SR<01> - ADC2 OR

This bit indicates that an analog input over range condition has occurred on ADC channel 2. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the ADC Over Range bits to determine on which channel the over range occurred. This bit is latched; to clear it, a one must be written to it.

SR<01>	**ADC2 Over Range**
READ/WRITE	
0	No over range has been detected at ADC channel 2
1	Over range has been detected at ADC channel 2

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6.4.3 SR<04> - ADC1 IRQ

This bit will be set when the quantity of data acquired in FIFO1 reaches the almost full level programmed by the user to the FIFO1 Level Control register for FIFO1. If ADC1 interrupts have been enabled by setting bit 0 of the IMR register, an interrupt request will occur.

SR<04>	**ADC 1 Interrupt Request**
READ ONLY	
0	ADC IRQ not asserted
1	ADC IRQ asserted

6.4.4 SR<05> - ADC2 IRQ

This bit will be set when the quantity of data acquired in FIFO2 reaches the almost full level programmed by the user to the FIFO2 Level Control register for FIFO2. If ADC2 interrupts have been enabled by setting bit 0 of the IMR register, an interrupt request will occur.

SR<05>	**ADC 2 Interrupt Request**
READ ONLY	
0	ADC IRQ not asserted
1	ADC IRQ asserted

6.4.5 SR<06> - ADC OR IRQ

This bit indicates that an analog input over range condition has occurred on either of the ADC channels. If the ADC over range interrupt is enabled, an interrupt request will occur. The user should first check this bit and the ADC IRQ and User IRQ bits to determine which type of interrupt has occurred. If this bit is set, the user should then check the ADC1 and 2 Over Range bits to determine on which channel/s the overflow occurred. The interrupt must be cleared by clearing the ADC*x* Over Range bit(s) responsible for the interrupt (see Section 6.4.1 or Section 6.4.2).

SR<06>	**ADC Over Range IRQ**
READ ONLY	
0	No overflow IRQ has occurred on any channel
1	An overflow IRQ has occurred on one or more channel/s

6.4.6 SR<07> - IRQ

This bit indicates that the ICS-8552B is asserting a PCI bus interrupt from one of the three available sources (i.e. ADC1, ADC2, or Over Range). It will therefore be set if any of bits 4, 5 and 6 of this register are set.

SR<07>	**PCI Bus Interrupt Request**
READ ONLY	
0	PCI Bus interrupt is not asserted
1	PCI Bus interrupt is asserted

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6.4.7 SR<08> - FIFO1 OR

This bit indicates that data buffer FIFO1 has data available for reading. When any amount of data is written into the FIFO1 this bit will be asserted low.

SR<08>	FIFO1 Output Ready
READ ONLY	
0	FIFO1 has data available (FIFO1 is not empty)
1	FIFO1 does not have data available (FIFO1 is empty)

6.4.8 SR<09> - FIFO1 PAE

This bit, when asserted low, indicates that the amount of data in FIFO1 has fallen to (or below) the value programmed to the FIFO Level Control register for the FIFO1 Almost Empty level.

SR<09>	FIFO1 Programmable Almost Empty
READ ONLY	
0	FIFO1 Programmable Almost Empty is asserted
1	FIFO1 Programmable Almost Empty is not asserted

6.4.9 SR<10> - FIFO1 PAF

This bit, when asserted low, indicates that the amount of data in the FIFO1 buffer has reached or exceeded the buffer length value programmed to the FIFO Level Control register. The ADC1 IRQ will also be set. An interrupt will occur if the ADC1 IRQ enable bit in the IMR register is set.

SR<10>	FIFO1 Programmable Almost Full
READ ONLY	
0	FIFO1 Programmable Almost Full is asserted
1	FIFO1 Programmable Almost Full is not asserted

6.4.10 SR<11> - FIFO1 IR

This bit, when asserted low, indicates that data buffer FIFO1 has space available to accept either ADC or DDC data. In normal operation the input ready bit should always be asserted low. If the Input Ready bit is de-asserted (high) FIFO1 has filled, and data has been lost. The FIFO1 IR flag is latched, and must be proactively cleared by writing a ‘1’ to it. They are also cleared on Board reset and ADC reset.

SR<11>	FIFO1 Input Ready
READ ONLY	
0	FIFO1 is ready to accept ADC1 or DDC data. (FIFO1 is not full)
1	FIFO1 is not ready to accept ADC1 or DDC data. (FIFO1 is full – data has been lost)

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6.4.11 SR<12> - FIFO2 OR

This bit indicates that data buffer FIFO2 has data available for reading. When any amount of data is written into the FIFO2 this bit will be asserted low.

SR<12>	FIFO2 Output Ready
READ ONLY	
0	FIFO2 has data available (FIFO2 is not empty)
1	FIFO2 does not have data available (FIFO2 is empty)

6.4.12 SR<13> - FIFO2 PAE

This bit, when asserted low, indicates that the amount of data in FIFO2 has fallen to (or below) the value programmed to the FIFO Level Control register for the FIFO2 Almost Empty level.

SR<13>	FIFO2 Programmable Almost Empty
READ ONLY	
0	FIFO2 Programmable Almost Empty is asserted
1	FIFO2 Programmable Almost Empty is not asserted

6.4.13 SR<14> - FIFO2 PAF

This bit, when asserted low, indicates that the amount of data in the FIFO2 buffer has reached or exceeded the buffer length value programmed to the FIFO Level Control register. The ADC2 IRQ will also be set. An interrupt will occur if the ADC2 IRQ enable bit in the IMR register is set.

SR<14>	FIFO2 Programmable Almost Full
READ ONLY	
0	FIFO2 Programmable Almost Full is asserted
1	FIFO2 Programmable Almost Full is not asserted

6.4.14 SR<15> - FIFO2 IR

This bit, when asserted low, indicates that data buffer FIFO2 has space available to accept either ADC or DDC data. In normal operation the input ready bit should always be asserted low. If the Input Ready bit is de-asserted (high) FIFO2 has filled, and data has been lost. The FIFO2 IR flag is latched, and must be proactively cleared by writing a ‘1’ to it. They are also cleared on Board reset and ADC reset.

SR<15>	FIFO2 Input Ready
READ ONLY	
0	FIFO2 is ready to accept ADC2 or DDC data. (FIFO2 is not full)
1	FIFO2 is not ready to accept ADC2 or DDC data. (FIFO2 is full – data has been lost)

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6.5 Interrupt Mask Register (IMR)

Read/Write

This register is used to enable PCI bus interrupts for ADC buffer almost full and ADC analog input over range conditions. Masked interrupts are still seen in the corresponding bits of the status register, but do not cause an interrupt to occur.

6.5.1 IMR<00> - ADC1 IRQ Enable

This register is used to enable PCI bus interrupts for the ADC buffer almost full condition. If the interrupt is masked, the ADC1 IRQ bit of the Status register will still indicate the occurrence of this condition, but no interrupt will occur. This bit must be cleared by the interrupt handler in order to prevent the possibility of a further interrupt before data has been read from FIFO 1.

IMR<00>	**ADC1 IRQ Mask**
READ/WRITE	
0	ADC1 interrupt is disabled
1	ADC1 interrupt is enabled

6.5.2 IMR<01> - ADC2 IRQ Enable

This register is used to enable PCI bus interrupts for the ADC buffer almost full condition. If the interrupt is masked, the ADC2 IRQ bit of the Status register will still indicate the occurrence of this condition, but no interrupt will occur. This bit must be cleared by the interrupt handler in order to prevent the possibility of a further interrupt before data has been read from FIFO 2.

IMR<01>	**ADC2 IRQ Mask**
READ/WRITE	
0	ADC2 interrupt is disabled
1	ADC2 interrupt is enabled

6.5.3 IMR<02> - ADC Over Range IRQ Enable

This bit enables the ADC analog input over range PCI bus interrupts. An analog signal over range condition occurring on any input channel will cause this condition to be asserted. If the over range condition has not been corrected, setting this bit again will immediately cause a further interrupt.

IMR<02>	**ADC Over Range IRQ Enable**
READ/WRITE	
0	ADC over range interrupts are disabled
1	ADC over range interrupts are enabled

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6.6 Control Register 1 (CR1)

Read/Write

The control register allows the user to configure the following operating parameters:

- internal/external clock selection
- internal clock output enable
- internal trigger output enable
- external trigger input enable
- internal Sync output enable
- external Sync input enable
- FIFO OW (output width)
- FIFO IW (input width)
- FIFO BM (bus match)
- FIFO BE (Big-Endian)

The register bits are discussed in detail below. The reset default for each bit describes the state of the bit after a hardware PCI Bus reset or software reset via the Board Reset register.

6.6.1 CR1<00> - CLK Sel

This bit selects internal or external sampling clock.

CR1<00>	ADC Sampling Clock Select
0	Internal Sampling Clock
1	External Sampling Clock

6.6.2 CR1<01> - CLK OE

This bit enables internal clock output to external.

CR1<01>	Internal Clock Output Enable
0	Internal Clock Output disabled
1	Internal Clock Output enabled

6.6.3 CR1<02> - IntTrig OE

This bit enables the internal trigger output for use as a trigger source.

CR1<02>	Internal Trigger Output Enable
0	Internal Trigger Output disabled
1	Internal Trigger Output enabled

6.6.4 CR1<03> - Ext_Trig IN_EN

This bit enables external trigger input to the User FPGA.

CR1<03>	External Trigger Input Enable
0	External Trigger Input Disabled
1	External Trigger Input enabled

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6.6.5 CR1<04> - Int_Sync OE

This bit enables the internal trigger output for use as a trigger source.

CR1<04>	**Internal Sync Output Enable**
0	Internal Sync Output disabled
1	Internal Sync Output enabled

6.6.6 CR1<05> - Ext_Sync IN_EN

This bit enables the external sync input to the User FPGA.

CR1<05>	**External Sync Input Enable**
0	External Sync Input disabled
1	External Sync Input enabled

6.6.7 CR1<10~07> FIFO BM, FIFO IW, FIFO1 OW and FIFO2 OW

Bits 7 to 10 of CR1 control the FIFO data input and output width and FIFO bus matching for both FIFOs. During Board reset, these FIFO configuration values will be latched into the FIFO. For detailed information, refer to the IDT72T72115 datasheet (2.5 Volt High-speed TeraSync FIFO). The write port width is controlled by bits 8 and 7 for FIFO1 and FIFO2 respectively. The read port width is 64-bits.

CR1<10, 9, **8**> BM, IW, FIFO1 OW	FIFO1 Data Input and Output Width	
	Write Port Width FIFO1	**Read Port Width FIFO1**
1 1 1	X16	X64
1 1 0	X32	X64
Other combinations	Not available	Not available

CR1<10, 9, **7**> BM, IW, FIFO2 OW	FIFO2 Data Input and Output Width	
	Write Port Width FIFO2	**Read Port Width FIFO2**
1 1 1	X16	X64
1 1 0	X32	X64
Other combinations	Not available	Not available

6.6.8 CR1<11> FIFO BE

This bit controls FIFO Big-Endian/Little-Endian. For detail information, refer to the IDT72T72115 datasheet (2.5 Volt High-speed TeraSync FIFO 36-Bit Configuration.)

CR1<11>	**FIFO Big-Endian**
0	FIFO is Little-Endian mode.
1	FIFO is Big-Endian mode.

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6.7 Control Register 2 (CR2)

Read/Write

The control register allows the user to configure the FIFO level programming enable operating parameter.

The control register bits are discussed in detail below. The reset default for each CR2 bit reflects the bit's state after a hardware PCI Bus reset or software reset via the Board Reset register.

6.7.1 CR2<00> FIFO1 PEN

This bit enables the FIFO1 almost full / almost empty threshold levels to be programmed. After setting this bit, the levels may be programmed using the FIFO Level Control register. This bit must be cleared after the levels have been programmed.

CR2<00>	FIFO1 Programming Enable
0	FIFO1 Programming Disable
1	FIFO1 Programming Enable

6.7.2 CR2<01> FIFO2 PEN

This bit enables FIFO2 almost full / almost empty threshold levels to be programmed. After setting this bit, the levels may be programmed using the FIFO Level Control register. This bit must be cleared after the levels have been programmed.

CR2<01>	FIFO2 Programming Enable
0	FIFO2 Programming Disable
1	FIFO2 Programming Enable

6.8 JTAG Program Register (JTAG_Pro)

Read/Write

This register programs the ICS-8552B User FPGA over PCI Bus rather than using the P6 JTAG port. The register allows the user to configure the following operating parameters:

- Enable programming of the User FPGA or the EEPROM from PCI bus
- Generation of the JTAG signals TCK, TMS and TDI
- Read JTAG signal TDO

The control register bits are discussed in detail below. The reset default for each JTAG_Pro bit reflects the bits state after a hardware PCI Bus reset or software reset via the Board Reset register. Before software programs the User FPGA or EEPROM, set the JTAG Programming Enable bit to ‘1’. During programming the User FPGA or EEPROM, it is recommended that application software only read or write to the JTAG Program Register. After programming the User FPGA or EEPROM, the JTAG Programming Enable bit must be set back to the default value of ‘0’.

6.8.1 JTAG_PRO<00> JTAG Enable

This bit enables generation of the JTAG programming signals and read back of TDO over PCI bus. After setting this bit, the User FPGA or EEPROM may be programmed over PCI bus. The bit must be cleared after programming is complete. The default value of this bit is ‘0’, JTAG Programming Disable.

JTAG_PRO<00>	JTAG Programming Enable
0	JTAG Programming Disable
1	JTAG Programming Enable

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6.8.2 JTAG_PRO<01:03> TCK, TMS, TDI

Application software generates TCK, TMS and TDI signals by writing these bits through PCI bus to program the User FPGA or EEPROM.

6.8.3 JTAG_PRO<04> TDO

Application software reads the JTAG TDO signal by reading this bit through PCI bus to verify JTAG commands and programming results. This bit is read only.

6.9 FIFO Level Control Register

Write Only

This register allows the user to program the levels for the FIFO 1 and FIFO 2 programmable almost full (PAF) and programmable almost empty (PAE) flags. The values assigned to these levels determine the FIFO data levels at which the Status register PAF and PAE flags will be set or cleared. They also determine the levels at which the ADC IRQ interrupts occur, since these are triggered from the PAF flag.
The level values are programmed by writing a 34-bit programming word to this register. The PAE value is contained in the least significant 17 bits in the 34-bit word, while the PAF value is contained in the most significant 17 bits. The range of values that can be programmed for each parameter is therefore 0 – 131070, corresponding to the number of 64-bit words in the FIFO at which the level is set, less two. The value programmed to the PAF level sets the length of free space below the full state of the FIFO (i.e. the difference between the full and almost full levels), while the value programmed to the PAE level sets the length of filled space above the empty state of the FIFO (i.e. the difference between the empty and almost empty levels). Data is written serially to the FIFO, least significant bit first. One write must occur for each bit of data to be written to the FIFO, with the data to be programmed in bit 0 of the FIFO level control register. The PAF/PAE buffer is shown in Figure 8.

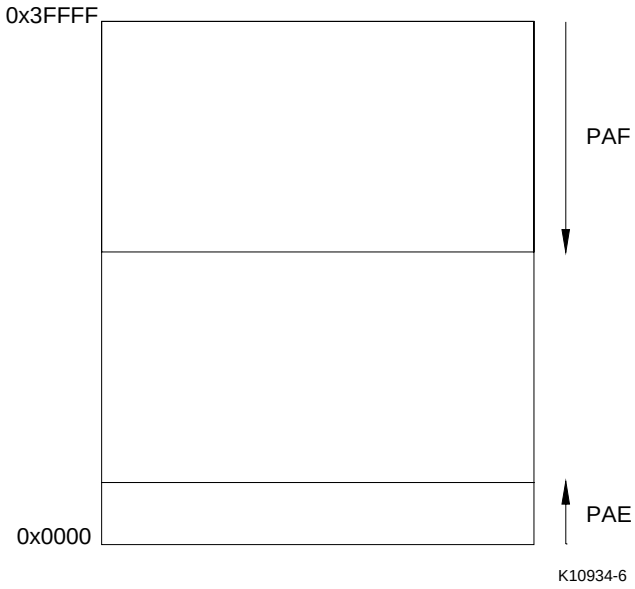


Figure 8 – PAF/PAE Buffer

Since the almost empty condition is not usually of interest to the user, and can not generate an interrupt, the value programmed is not important. However, the almost full level must be carefully selected, since the optimum setting will be determined by several factors. The PAF level must be programmed with the number of 64-bit words to be acquired in the FIFO buffer prior to each interrupt or to completion of acquisition. The ADC

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interrupt request will occur each time the FIFO fills to the PAF level. When operating in Capture mode, the value programmed must be an integral multiple of the Acquisition Count (see Section 6.15). When the ADC interrupt occurs, the user may read data to the programmed length (= PAF level), but not more.

In general, the PAF level should be set as high as possible, since it determines the length of data that can be read from the module in each DMA transfer. Increasing the size will result in more efficient transfers and greater throughput. However, setting the PAF level too near to the FIFO full condition (i.e. 0x1FFFF) may result in FIFO overflow on systems that have poor or variable interrupt latency. In particular, this applies to non-real time systems such as Windows. Note that data is written to the FIFO in frames; the frame size is determined by the mode of operation (DDCs enabled or disabled, DDC mode, number of channels of output, complex or real data). In general, for maximum efficiency, the PAF level should be set to a multiple of the frame size, less two. The frame size can be as small as one quarter of a 64-bit word, for one channel output without DDC, or as large as 8 x 64-bit words for 8 channels of complex data.

Example: Program the FIFO programmable full (i.e. the ADC buffer length) level to 90% of the FIFO size, and the programmable empty flag to 2 (minimum value possible). Calculate 90% of the FIFO size:

131072 64-bit words x (1 - .90) = 13107.2

Round this up to the nearest integer multiple of 8 (to allow for 8-channel complex output) for a value of 12288. The value to be programmed is two less than this for a value of 12288.

The hexadecimal equivalent of this number is 0x2FFE. The programming word required is therefore 0x05FFC0000. To program the data, set CR2<00> to select the FIFO chip, and write 0x05FFC0000 to the register. This is performed by a one bit write, 34 times, shifting the data right by one bit after each write.

The user must perform an ADC Reset (by writing to the ADC Reset register) after writing to the FIFO Level Control, Acquisition Count and Decimation registers in order for the new values to take effect.
Please note that the Buffer Length Set functions of the API (see Reference [1]) automatically set the PAE and PAF levels based on the desired buffer length.

6.10 Trigger Register

Write only

A write to this register causes acquisition to start if the internal trigger is selected (by clearing UCR<00>). The data written to the register is unimportant.

When Capture mode has been selected (UCR<09>), writing to this register will cause data acquisition to begin, and continue until the programmed acquisition count value has been reached. The board may be triggered multiple times in this way, until the total amount of data acquired is equal to the programmed buffer length. When this occurs, an ADC interrupt will occur, if enabled.

When Continuous mode has been selected (UCR<09>), writing to this register will cause data acquisition to begin, and continue until the module is disabled by clearing UCR<10>.

6.11 ADC Reset Register

Write only

A write to this register initializes memory pointers. It does not alter memory contents or the values of control registers. The data written to the register is unimportant. The register should be written to after the board is configured and before acquisition is started.

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After writing to this register, a delay of at least one microsecond is required before the ICS-8552B is triggered, to allow time for the DLL clock manager located in the User FPGA to lock, otherwise the data read from the board may be corrupted. The user may perform other board configuration activities immediately after writing to this register.

6.12 Board Reset Register

Write only

A write to this register masks all interrupts, resets all control register bits to their power-up defaults (zero) and resets all on-board memory except CR1<11> (FIFO Big-Endian), CR1<10> (FIFO bus match), CR1<09> (FIFO Input Width) and CR1<08> (FIFO Output Width). The QL5064 registers and status are unaffected. The data written to the register is unimportant. The register should only be written in order to perform a complete reset of the board prior to changing the board configuration.

Note: CR1<11> (FIFO Big-Endian), CR1<10> (FIFO bus match), CR1<09> (FIFO Input Width) and CR1<08:07> (FIFO Output Width) must be configured before writing to this register. Board Reset and ADC Reset do not clear these four bits, and a board reset is required to load the values programmed to these bits to the FIFOs.

6.13 User Status Register (USR)

Read Only

The Status Register contains information about the state of the ICS-8552B ADCs and FIFO memory. It also contains error condition information.

6.13.1 USR<00> - ADC1 OR

This bit indicates that an analog input over range condition has occurred on ADC1 channel 1. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the ADC Over Range bits to determine on which channel the over range occurred.

USR<00>	**ADC1 Over Range**
READ ONLY	
0	No over range has been detected at ADC1 channel 1
1	Over range has been detected at ADC1 channel 1

6.13.2 USR<1> - ADC2 OR

This bit indicates that an analog input over range condition has occurred on ADC2 channel 2. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the ADC Over Range bits to determine on which channel the over range occurred.

USR<01>	**ADC2 Over Range**
READ ONLY	
0	No over range has been detected at ADC2 channel 2
1	Over range has been detected at ADC2 channel 2

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6.13.3 USR<08> - FIFO1 OR

This bit indicates that data buffer FIFO1 has data available for reading. When any amount of data is written into FIFO1, this bit will be asserted low.

USR<08>	**FIFO1 Output Ready**
READ ONLY	
0	FIFO1 has data available (FIFO1 is not empty)
1	FIFO1 does not have data available (FIFO1 is empty)

6.13.4 USR<09> - FIFO1 PAE

This bit, when asserted low, indicates that the amount of data in FIFO1 has fallen to (or below) the value programmed to the FIFO Level Control register for the FIFO Almost Empty level.

USR<09>	**FIFO1 Programmable Almost Empty**
READ ONLY	
0	FIFO1 Programmable Almost Empty is asserted
1	FIFO1 Programmable Almost Empty is not asserted

6.13.5 USR<10> - FIFO1 HF

This bit, when asserted low, indicates that the amount of data in FIFO1 is equal to or more than half full.

USR<10>	**FIFO1 Half Full**
READ ONLY	
0	FIFO1 less than half full
1	FIFO1 more than half full

6.13.6 USR<11> - FIFO1 PAF

This bit, when asserted low, indicates that the amount of data in the FIFO1 buffer has reached or exceeded the buffer length value programmed to the FIFO Level Control register. The ADC IRQ will also be set. An interrupt will occur if the ADC1 IRQ enable bit in the IMR register is set.

USR<11>	**FIFO1 Programmable Almost Full**
READ ONLY	
0	FIFO1 Programmable Almost Full is asserted
1	FIFO1 Programmable Almost Full is not asserted

6.13.7 USR<12> - FIFO1 IR

This bit, when asserted low, indicates that data buffer FIFO1 has space available to accept either ADC or DDC data. In normal operation the Input Ready (IR) bit should always be asserted low. If the Input Ready bit is de-asserted (high) FIFO1 has filled, and data has been lost. This bit is cleared on Board reset and ADC reset.

USR<12>	**FIFO1 Input Ready**
READ ONLY	
0	FIFO1 is ready to accept ADC or DDC data. (FIFO1 is not full)
1	FIFO1 is not ready to accept ADC or DDC data. (FIFO1 is full – data has been lost)

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6.13.8 USR<13> - FIFO2 OR

This bit indicates that data buffer FIFO2 has data available for reading. When any amount of data is written into FIFO2, this bit will be asserted low.

USR<13>	**FIFO2 Output Ready**
READ ONLY	
0	FIFO2 has data available (FIFO2 is not empty)
1	FIFO2 does not have data available (FIFO2 is empty)

6.13.9 USR<14> - FIFO2 PAE

This bit, when asserted low, indicates that the amount of data in FIFO2 has fallen to (or below) the value programmed to the FIFO Level Control register for the FIFO2 Almost Empty level.

USR<14>	**FIFO2 Programmable Almost Empty**
READ ONLY	
0	FIFO2 Programmable Almost Empty is asserted
1	FIFO2 Programmable Almost Empty is not asserted

6.13.10 USR<15> - FIFO2 HF

This bit, when asserted low, indicates that the amount of data in FIFO2 is equal to or more than half full.

USR<15>	**FIFO2 Half Full**
READ ONLY	
0	FIFO2 less than half full
1	FIFO2 more than half full

6.13.11 USR<16> - FIFO2 PAF

This bit, when asserted low, indicates that the amount of data in the FIFO2 buffer has reached or exceeded the buffer length value programmed to the FIFO Level Control register. The ADC IRQ will also be set. An interrupt will occur if the ADC2 IRQ enable bit in the IMR register is set.

USR<16>	**FIFO2 Programmable Almost Full**
READ ONLY	
0	FIFO2 Programmable Almost Full is asserted
1	FIFO2 Programmable Almost Full is not asserted

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6.13.12 USR<17> - FIFO2 IR

This bit, when asserted low, indicates that data buffer FIFO2 has space available to accept either ADC or DDC data. In normal operation the Input Ready (IR) bit should always be asserted low. If the Input Ready bit is de-asserted (high) FIFO2 has filled, and data has been lost. This bit is also cleared on Board reset and ADC reset.

USR<17>	**FIFO2 Input Ready**
READ ONLY	
0	FIFO2 is ready to accept ADC or DDC data. (FIFO2 is not full)
1	FIFO2 is not ready to accept ADC or DDC data. (FIFO2 is full – data has been lost)

6.14 User Control Register (UCR)

Read/Write

The control register allows the user to configure the following operating parameters:

- internal/external trigger selection
- external trigger edge selection
- internal/external sync selection
- external sync edge selection
- ADC channel 1 Built-in-test enable (not implemented with this version of the ICS-8552B board)
- ADC channel 2 Built-in-test enable (not implemented with this version of the ICS-8552B board)
- ADC data output enable
- Acquisition Enable
- GC4016 selection
- GC4016 output data 16-bit or 24-bit selection
- GC4016 chip 1 configuration enable
- GC4016 chip 2 configuration enable

The register bits are discussed in detail below. The reset default for each bit describes the state of the bit after a hardware PCI Bus reset or software reset via the Board Reset register.

6.14.1 UCR<00> - Trig Select

This bit selects either internal or external Trigger source.

UCR<00>	**Trigger Select**
0	Internal Trigger
1	External Trigger

6.14.2 UCR<01> - Ext_Trig Edge

This bit selects the external Trigger active edge.

UCR<01>	**External Trigger Edge Select**
0	Rising edge
1	Falling edge

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6.14.3 UCR<02> - Sync Select

This bit selects the internal or external Sync source.

UCR<02>	GC4016 Sync Select
0	Internal Sync
1	External Sync

6.14.4 UCR<03> - Ext_Sync Level Select

This bit selects the external Sync active level.

UCR<03>	External Sync Level Select
0	External Sync active low
1	External Sync active high

6.14.5 UCR<04> - ADC1 Test_En

This bit enables ADC channel 1 Built-In-Test (BIT). BIT is not implemented with this version of the ICS-8552B board.

UCR<04>	ADC Channel 1 Built-In-Test Enable
0	Built-In-Test disable
1	Built-In-Test enable

6.14.6 UCR<05> - ADC2 Test_En

This bit enables ADC channel 2 Built-In-Test (BIT). BIT is not implemented with this version of the ICS-8552B board.

UCR<05>	ADC Channel 2 Built-In-Test Enable
0	Built-In-Test disable
1	Built-In-Test enable

6.14.7 UCR<08> - ADC_En

This bit enables ADC data output.

UCR<08>	ADC Data Output Enable
0	ADC data output enabled
1	ADC data output disabled

6.14.8 UCR<09> - Acq Mode

This bit controls the ICS-8552B data acquisition mode.

UCR<09>	Acquisition Mode
0	Continuous mode
1	Capture mode

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6.14.9 UCR<10> Acq1 Enable

This bit enables data acquisition to FIFO1.

UCR<10>	Acquisition Enable FIFO1
0	Acquisition disabled
1	Acquisition Enabled

6.14.10 UCR<11> GC1 Select

This bit selects the GC4016 data for writing to the FIFO1 buffer, otherwise ADC data will be written into the buffer.

UCR<11>	GC4016 Chip 1 Select
0	ADC data flow
1	GC4016 data flow

6.14.11 UCR<12> GC16 Bit Select

This bit selects GC4016 16-bit or 24-bit data format.

UCR<12>	GC4016 16-bit or 24-bit Data Format Select
0	24-bit data format
1	16-bit data format

6.14.12 UCR<13> GC CE1

This bit must be enabled to configure GC4016 chip 1.

UCR<13>	GC4016 Chip 1 Configuration Enable
0	Disabled
1	Enabled

6.14.13 UCR<14> GC CE2

This bit must be enabled to configure GC4016 chip 2.

UCR<14>	GC4016 Chip 2 Configuration Enable
0	Disabled
1	Enabled

6.14.14 UCR<15> Acq2 Enable

This bit must be enabled for FIFO 2 to receive data.

UCR<15>	Acquisition Enable FIFO2
0	Acquisition disabled
1	Acquisition Enabled

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6.14.15 UCR<16> GC2 Select

This bit selects GC4016 data for writing to the FIFO2 buffer, otherwise ADC data will be written into the buffer.

UCR<16>	GC4016 Chip 2 Select
0	ADC data flow
1	GC4016 data flow

6.15 ADC1 Acquisition Count Register

Read/Write

The ADC1 Acquisition Count register determines the number of frames of data to be stored in the FIFO buffers following each application of the trigger when operating in Capture mode. The value to be programmed to the register is one less than the required number of data frames. A frame is defined as a block of data containing one or more sample(s) or one or more complex sample(s) from each active channel at a single point in time. When the DDCs are disabled, each frame contains only one ADC sample per channel, as described in Section 3.3. Data from one channel is stored in FIFO 1. Data from two channels is stored in FIFO 1 and FIFO 2.

When the DDCs are enabled (if installed), each frame will be formatted as described in Section 4.15; the format varies depending on the DDC operating mode (Wide band, Split-I/Q or Narrow band), and on the number of channels selected for output (see Channel Count register description, Section 6.17 below). When the DDCs are enabled (if installed) by setting UCR<11> or UCR<16>, up to 8 output channels may be selected. The rules for programming this register are given below.

When operating in Continuous mode, the Acquisition Count must be set to a non-zero value.

The following expressions show the relationship between the value programmed to the Acquisition Count registers, the operating mode, the frame size and the buffer length.

Frame Size (16-bit words) = No_Chan x DDC_Mode x Data_Type,

where:

No_Chan = number of channels of output to each FIFO
(1, 2 or 4 when DDCs disabled, up to 8 when DDCs enabled)

DDC_Mode:

1 Disabled
2 Narrow
4 Split-I/Q (or complex input)
8 Wide (or Split-I/Q with complex input)

Data_Type:

1 Real Data (DDC enabled or disabled)
2 Complex Data (DDC enabled only)

Note: Some combinations are not allowed, such as 1-channel real output when the DDCs are enabled. Legal combinations are described in Section 4.2. For some combinations when the DDCs are enabled, data frames contain more than one sample for each output channel (see the DDC data frame format descriptions in Section 4.15).

The minimum Acquisition Count value that may be programmed is given by:

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Min Acq Cnt = 3 for DDC disabled, one ADC enabled;
= 1, all other cases

Step size = 4 for one channel operation, DDC disabled;
= 2 for two channel operation, DDC enabled or disabled
= 1 for DDC enabled with more than two channels of output

The maximum Acquisition Count that may be programmed is given by:

Max Acq Cnt = 131072 / Frame Size

The relationship between the Buffer Length or FIFO level value programmed to the FIFO Level Control register (see Section 6.9) is given by:

BL (64-bit words) = Acq Cnt x Frame size (16-bit words) / 4

6.16 ADC1 Decimation Register (DECR)

Read/Write

The control register allows the user to configure the ADC decimation operating parameter.

6.16.1 DECR<04:00> - ADC Decimation

The ICS-8552B includes a programmable decimation feature independent of the DDCs. This feature may be used to decimate the output data stream by a factor of N. No filtering is applied to the decimated data stream. The feature should not be used when the DDCs are enabled.

This register is used to set the decimation factor for each ADC channel. Decimation is done by periodically discarding a specified number of samples from each channel at the output of the converters, before the samples are written to their respective FIFOs.

The register allows the user to specify the decimation factor in the range 1 to 32. If a value (N-1) is programmed to the register, the board will reject (N-1) out of every N samples before placing them in their respective FIFOs. This effectively reduces the output rate by a factor of N. the range of values that may be programmed is therefore 0 – 31, inclusive.

For example, when the value 0 is programmed, no decimation takes place. When the value 1 is programmed, every second data frame is discarded.

The Decimation register must be programmed with the value 0 when the DDCs are enabled.

6.17 Channel Count Register (CCR)

Read / Write

The channel count register allows the user to configure the DDC Number of Channels selection operating parameter.

6.17.1 CCR<02:00> - DDC 1 Number of Channels

This register is used to specify the output data format when the optional DDCs are used. It is not necessary to program the register if the DDCs are not enabled. Table 6.5 outlines the number of channels stored in the FIFOs. The FIFOs can be used separately or together for channel storage.

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When DDC1 is enabled (UCR<11>), this field selects the output data format. The value to be programmed must be one less than the number of output channels required. Depending on the operating mode, only certain values are allowed, as shown in Table 6.5. The output data formats are as shown in Section 4.15.

6.17.2 CCR<06~04> - DDC 2 Number of Channels

This register is used to specify the output data format when the optional DDCs are used. It is not necessary to program the register if the DDCs are not enabled. Table 6.5 discusses the number of channels stored in the FIFOs. The FIFOs can be used separately or together for channel storage.

When DDC2 is enabled (UCR<16>), this field selects the output data format. The value to be programmed must be one less than the number of output channels required. Depending on the operating mode, only certain values are allowed, as shown in Table 6.5. The output data formats are as shown in Section 4.15.

Table 6.5 - Programming of Channel Count Values

DDC Mode	Channel Count (N)	Data Stored in FIFO
Narrowband complex output	2,4,6,8	N channels complex data.
Narrowband real output	2,4	2N channels real data.
Split-I/Q complex output	8	N/2 channels complex data.
Split-I/Q real output	4	N channels real data.
Wideband complex output	8	N/4 channels complex data.
Wideband real output	4	N/2 channels real data.
Narrowband pairs of complex input & complex output	8	N/2 channels complex data.
Narrowband pairs of complex input & real output	4	N channels real data.
Split-I/Q complex input & complex output	8	N/4 channels complex data.
Split-I/Q complex input & real output	4	N/2 channels real data.

6.18 ADC2 Acquisition Count Register

The details of this register are outlined in Section 6.15. References to ADC1 should be replaced with ADC2.

6.19 ADC2 Decimation Register

The details of this register are outlined in Section 6.16. References to ADC1 should be replaced with ADC2.

6.20 Programming the DDC Modules

As an option, the ICS-8552B is available with two GC4016 DDC devices installed, one for each A/D channel (models ICS-8552B-x00). Each of the devices has an identical register set, and is independently programmed. The registers for programming these devices are located at PCI Bus address PCI_BASE1 + 0x0100 (see Table 6.2); the same register set is used for programming each of the two devices. The device to be programmed (ADC channel 1 or 2) must be selected using UCR<14:13> before programming. After the device has been programmed, UCR<14:13> must be cleared.

The user should not attempt to operate the versions of ICS-8552B that include DDCs without configuring both of the GC4016 down converters since the results may be unpredictable.

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The GC4016 register set is divided into global registers and paged registers. Global registers apply to all four channels of each chip, and are accessible regardless of which page has been selected for access. Access to any of the paged register set requires that the page number be programmed to the Page register of the Global register set before any access is made to a paged register, in order to select the required page.

The programming details are not described here, since they are fully described in the Graychip data sheet, Reference [5], available from the Graychip web site. Users should follow the recommendations given there for the values to be programmed to each register. However, notes are given below on required programming with respect to the ICS-8552B implementation, and where the default programming values given in the Graychip documentation should be modified.

In the Graychip documentation, the registers are given an address value ranging from 0 – 31. Each register is a single byte, and is mapped to the least significant 8 bits of a single 64-bit PCI Bus address. The required offset for any register in PCI address space is therefore computed by multiplying the GC4016 register address by 8 and adding it to PCI_BASE1 + 0x100. Registers 0 –15 are the global registers, while registers 16 – 31 are the paged registers, accessible on 98 different pages. The required page must be selected before attempting to read or write to the paged registers.

The output data from the GC4016 DDCs is formatted in the User FPGA. The formatting applied depends on the number of output channels required. A single register located in the User FPGA, the Channel Count register must be programmed to select the data output format when the DDCs are enabled.

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7 TECHNICAL SUPPORT

Technical support for this product is available through Radstone Sensor Processing using the contact information given below.

When requesting technical support, please provide the following information:

- Product name - ICS-8552B specific model and custom core (HDK-8552B/xxx number), if applicable.
- Equipment Number (Equ No. of the form 10987654, given on the board equipment number label)
- Software device driver used, if any (e.g. Windows, Linux or VxWorks driver).
- Installation environment – type of chassis, type of CPU, and other boards installed.
- Nature of problem.

You may contact Radstone Sensor Processing Technical Support at:

Address: Radstone Sensor Processing
Attn. Technical Support
5430 Canotek Road
Ottawa, Ontario
K1J 9G2

Phone: 613-749-9241 or (USA) 800-267-9794
Fax: 613-749-9461
Web: http://www.ics-ltd.com
E-mail: support@ics-ltd.com

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8 REFERENCES

1. ICS-8552B Windows Software Development Kit User's Manual, Document Number E11323, Radstone Sensor Processing, Ottawa, ON

2. IEEE 1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, IEEE, 2001.

3. PCI Local Bus Specification Revision 2.2 December 18, 1998

4. QL5064 Production Information, QuickLogic, http://www.quicklogic.com

5. GC4016 Multi-Standard Quad DDC Chip Data Sheet Rev 1.0 August 27, 2001 (SLWS133A), http://www.ti.com/

6. Xilinx Virtex-II product documentation, http://www.xilinx.com

7. 72T72115 128K x 72 TeraSync FIFO datasheet, http://www.idt.com.

8. Antec cooling products, http://www.antec-inc.com/

9. The Card Cooler products, http://www.thecardcooler.com/

10. ICS-8552B Hardware Development Kit User’s Manual, Document Number E11331, Radstone Sensor Processing, Ottawa, ON

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APPENDICES

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APPENDIX A

A.1 Typical Order of Operations for Simple Acquisition

1. Configure jumpers to desired master/slave and internal/external clock and trigger configuration. Install ICS-8552B in chassis.
2. Set FIFO bus match CR1<11:07>.
3. Reset board; clears control registers except CR1<11:07>.
4. Set control register:
   4.1. Select clock source (internal or external).
   4.2. Select trigger source (internal or external).
   4.3. Select external trigger edge if external trigger used.
   4.4. Select Sync source (if use Tuner).
   4.5. Select operation mode (capture or continuous).
5. Enable Tuners (if use Tuner).
6. Set Number of Channels register.
7. Configure tuner module if use tuners.
8. Set decimation.
9. Set acquisition count.
10. Set buffer length.
11. Reset ADC (loads acquisition count, FIFO reset)
12. Set enable bit in control register.
13. If using internal trigger, writing trigger register, or wait for external trigger to occur.
14. Wait for interrupt from ICS-8552B ADC.
15. Read back acquired data.
16. If using continuous mode:
17. IF enough data acquired, disable acquisition.
18. ELSE repeat steps 13…15.
19. If using capture mode:
20. IF enough data acquired, disable acquisition.
21. ELSE repeat steps 10…18.

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Fruchey, Nicole

From: Operach, Paula (GE EntSol, Intelligent Platforms, US) [paula.operach@ge.com]
Sent: Wednesday, September 23, 2009 10:36 AM
To: Fruchey, Nicole
Cc: Tallent, Allison; Norwood, Rossana (GE EntSol, Intelligent Platforms)
Subject: Aeroflex: GE
Attachments: SKMBT_C25309082414410.pdf

Hi Nichole,

I am trying to update an order that you currently have with us.

Based on our history with the Loral Project, Aeroflex needs the SMA connectors incorporated onto the ICS-8552 boards.
This is something that we do at the factory since it is more customized rather than just sending our customers out the SMA connector to incorporate themselves.

I would like to verify the following;

Short term:

1) PO attached: 34229. We are shipping out this week. We would like to go ahead and put the connectors on for you before they ship. This would mean that we would need to add a second line item: for 2 each of the SA-8552-SMA at $0. This will allow us to go ahead and put the connectors on other board for this order. Can you please confirm that you would like the connectors on the board so that we can update the PO ?

Long Term:

2) We have a specific part # "ICS-8552B-102". This part # is for our ICS-8552B-100 with our SA-8552-SMA all in one.

I understand from talking ot Allison that to make a change to the part # would require some time and an ECN. In the long term it would be safer to call out all inclusive part# so that we wont' have units coming back.. If this is too difficult, then we should make sure that each po has both the ICS-8552B-100 and a line item for SA-8552-SMA (one for one call out). We will have to make sure the factory knows that they should be incoporated together on each po.

I will be at your facitlty the week of October 5th. We can talk about the long term fix then as well if we just want to take care of the short term fix on the attached order for now.

Just let me know..

Please let us know if you need anything further or if you need addtianl clarification!

Thank you for your help!

Regards,
Paula

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Eastern Regional Manager
National Sales Director - Sensor Processing
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