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IMP1A

PowerPact™ CompactPCI

3U CompactPCI Processor with Certifiable BSP to DO-178B Level A

- High Performance 3U CompactPCI Processor
- CompactPCI System Slot or Peripheral Slot
- PowerPC 7410 to 500 MHz and beyond
- On-board PMC site
- Up to 2 Megabyte (MB) L2 Cache
- Up to 128 MB SDRAM
- 64 MB FLASH
- Two fast Sync/Async serial ports
- Two 10/100 BASE-T Ethernet ports
- Up to 12 bits GPIO



Designed for demanding applications with restrictive dimensional requirements, IMP1A packs a powerful SBC into an extremely space efficient 3U form factor. Radstone's 40 years of experience in the defense electronics market have been coupled with their continued investment in PowerPC technology to produce a highly effective solution for the most rigorous of requirements.

Available with either PowerPC 7410 processor IMP1A is based around a Marvell Discovery Integrated System Controller which combines high-performance system control with multiple communication peripherals including high-speed serial and Ethernet ports, all on a single chip.

A range of I/O options are offered including up to 2 Ethernet channels, up to 12 bits of discrete digital I/O, and up to 2 serial channels capable of high-speed operation in either asynchronous or synchronous mode and software programmable as RS232/422 or 485.

In addition to deployed test software and a range of BSP support for standard (non certifiable) COTS operating systems, the IMP1A is supported by a BSP for the certifiable VxWorksAE653 operating system from Wind River Systems.

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Features

System or Peripheral slot	Support for up to 7 peripheral slots	IMP1A detects a backplane signal to configure in System Slot or Peripheral Slot mode
Processor	PowerPC 755 at 400 MHz	The 755 is Freescale's long term supported part from its well established and performant G3 family of processors (SPECInt95 = 18.1, SPECfp95 = 12.3) Typical power consumption for SBC = 11.0 Watts
	PowerPC 7410 at 500 MHz	The 7410 is Freescale's long term supported part from its well established and AltiVec enabled G4 family of processors (SPECInt95 = 22.8, SPECfp95 = 17.0) Typical power consumption for SBC = 13.5 Watts
System Controller	Marvell 'Discovery' GT-64260	The Marvell Discovery Integrated System Controller (ISC) combines a high bandwidth memory controller, two PCI interfaces and a range of communications peripherals, all on a single chip
L2 Cache	1 MB (with 755) or 2 MB (with 7410)	Dependant on processor choice, either 1 MB or 2 MB of SRAM with parity error detection is supported on a 64 bit wide 200 MHz L2 bus
Main Memory	64 MB or 128 MB SDRAM with ECC	The CPU is interfaced to the main memory via a 64 bit data bus running at 100 MHz. Up to 128 MB SDRAM with ECC can be supported, with 64 MB being fitted as standard
FLASH Memory	64 MB FLASH	The CPU is interfaced to the FLASH memory via a 32 bit data bus running at 100 MHz. 8 MB are allocated to Boot FLASH and 56 MB to User FLASH
Non-volatile RAM	32 Kilobyte (KB) NVRAM	NON-VOLATILE RAM combines the advantages of SRAM (fast read and write) and EPROM (non-volatility and in-circuit programmability) providing non-volatile storage for data which must not be lost when power is removed
Serial EEPROM	2 KB EEPROM	EEPROM is provided on the I2C bus as an optional location for Discovery ISC configuration data
Real-Time Clock	1 sec. resolution	The RTC provides TOD/calendar with 1 sec resolution. 5V Standby must be connected to maintain data during power down
Ethernet Interfaces	10/100 BASE-T 1 or 2 ports	1 or 2 Ethernet Channels are provided from the Discovery ISC and can be accessed through the J2 connector (See Fig. 2 for I/O options)
Serial ports	RS232/422/485 2 ports Async/Sync	2 serial channels are provided from the Discovery ISC. Both channels are software selectable to be RS232/422 or 485 (See Fig. 2 for I/O options)
Discrete Digital I/O	12 bits	Up to 12 bits of TTL compatible Discrete Digital I/O are provided from the Discovery ISC, each bit being capable of generating an interrupt. (See Fig. 2 for I/O options)
Timers	8 x 32 bit timers	Timers are provided from the Discovery ISC
Watchdog Timer	1.6 sec time-out	The Watchdog timer has a fixed 1.6 second time-out period
CompactPCI Interface	32 bit/33 MHz 3.3 Volts	A 32 bit/33 MHz cPCI interface is provided conforming to the mechanical definitions of VITA 30.1
DMA controllers	8 available	8 DMA controllers are available in the Discovery ISC for efficiently moving large blocks of data
JTAG Interface	On-card connector	A JTAG header is accessible for both factory test and software de-bug purposes - (IMP1A JTAG-11 Adaptor card required for easy access)

Software Support

VxWorks provision includes a Board Support Package (BSP) designed to strict WindRiver definitions and supporting all defined features, plus an Enhanced Support Package (ESP), providing extra hardware-related support that is not defined by the O/S vendor (therefore possesses Radstone interfaces). The BSP initialization includes a full PCIbus scan, which will configure the Memory and I/O space of all PCI devices, including any PMC plugged into IMP1A, or any further PMCs on IMPCC1 carriers.

The ESP includes a software DMA engine, therefore allowing users to avoid direct and complex hardware programming of this function, plus Synchronous Serial support, also BCS (see below).

Two Deployed Test Software modules are available, together providing an overall test philosophy adapted to COTS silicon and COTS O/Ss that we believe is unbeaten in the industry.

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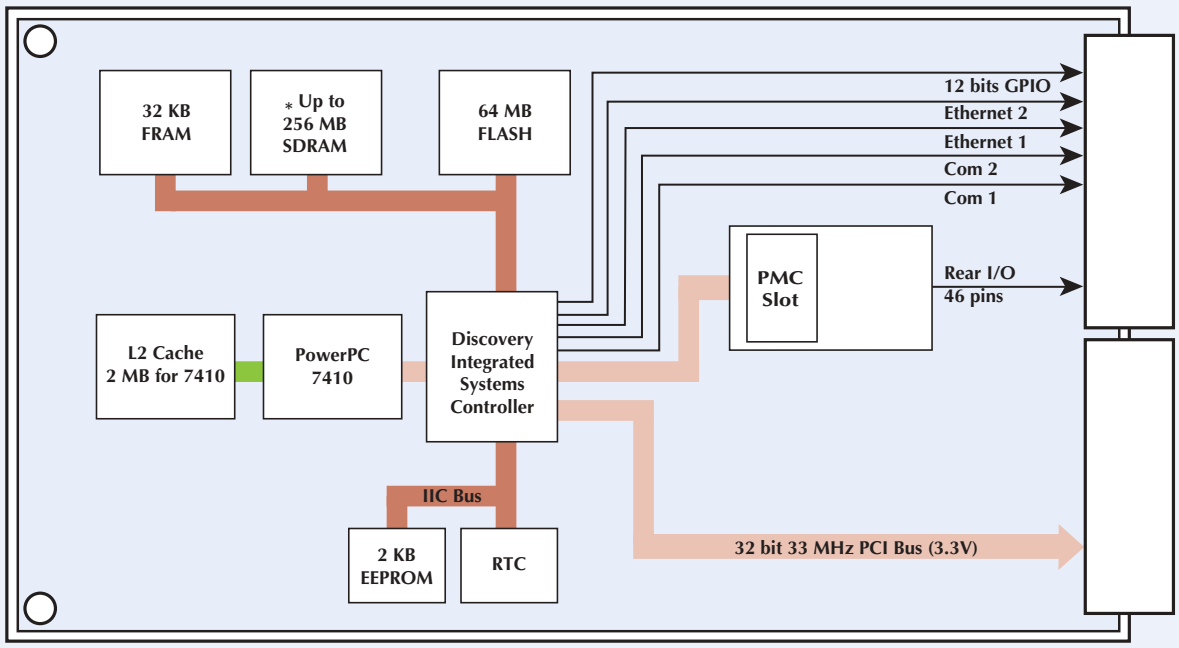
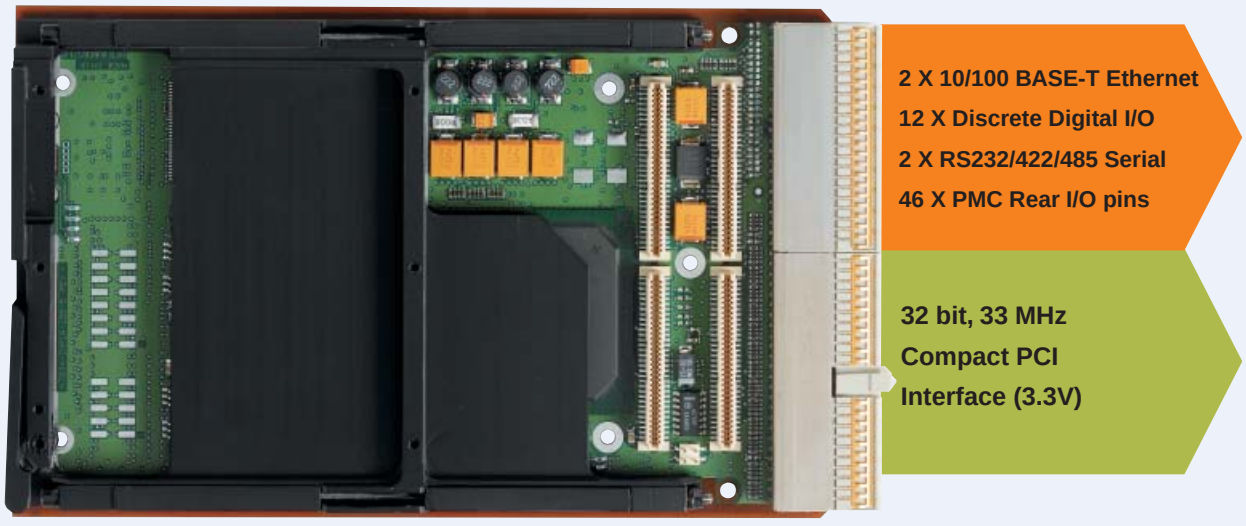


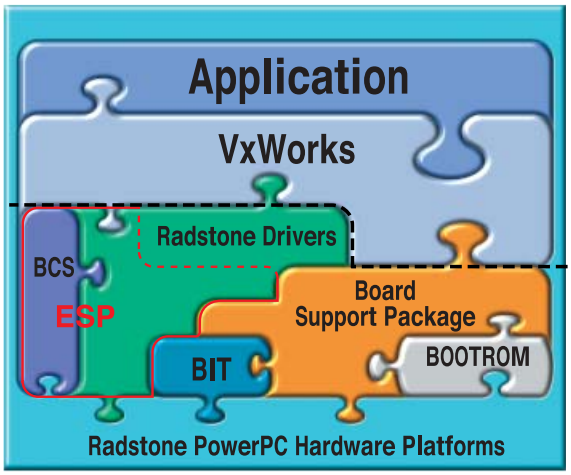
Figure 1: IMP1A Functional Block Diagram



	Ethernet 1	Ethernet 2	Serial 1	Serial 2	Discrete Digital I/O
Option 1	Yes	Yes	RS232	RS232/422/485. Async only	12 bits
Option 2	Yes	No	RS232/422/485. Async/Sync	RS232/422/485. Async/Sync	None
Option 3	Yes	No	RS232	RS232/422/485. Async/Sync	8 bit

Figure 2: IMP1A Input/Output Options

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BIT is supplied as an independent module that runs at initialization, achieving the highest possible coverage by the use of destructive (in system state terms) testing, before passing control to the O/S. In addition to visual failure indication, the application can read BIT results from FLASH.

Background Condition Screening (BCS) is supplied as part of the ESP, providing continuous, non-destructive testing for early warning of problems while the application is actually running. BCS runs as a task thread and is specifically designed for co-operation with the VxWorks Operating System. Both Deployed Test Software modules have a broad range of configuration options.

Support for the INTEGRITY RTOS on IMP1A is also available direct from our technology partner Green Hills Software Inc. INTEGRITY is a Real-Time O/S providing secure, maximum reliability operation for use in mission-critical embedded systems.

The royalty-free INTEGRITY RTOS uses hardware memory protection to isolate and protect itself, and user tasks, from incorrect operation caused by accidental errors or malicious tampering. Without the burden of compatibility with 1980's vintage products, INTEGRITY was designed from the ground up for 32 bit and 64 bit embedded processors, and employs the latest in RTOS technology.

Standard Ordering Information

Sales Code	PowerPact Processor (500 MHz PowerPC 7410)
IMP1A-7410-1C100X	500 MHz PowerPC 7410 3U cPCI SBC, Level 1; 128 MB SDRAM, 2 MB L2 Cache, 128 MB FLASH, 2x10/100 BASE-T 1 x RS232, 1 x RS232/422/485 async port, 12 bits GPIO, 1 PMC slot
IMP1A-7410-2C100X	Air-cooled Level 2 as above with conformal coating
IMP1A-7410-3C100X	Air-cooled Level 3 as above with conformal coating
IMP1A-7410-4C100X	Conduction-cooled Level 4 as above
IMP1A-7410-5C100X	Conduction-cooled Level 5 as above

X= software option

Note: For ordering information, further options and accessories please contact your local Radstone sales office

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