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Radstone P0CC1 Manual

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Document History

Note: The revision state refers to the manual *only*, ***not*** the board.

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Chapter 1 - Introduction

Radstone's P0CC1 is a PMC carrier card, and forms part of an expansion board range complementing Radstone's latest generation of PMC-compatible PowerPC-based single board computers.

The P0CC1 forms part of a set of cards that includes the PMCPCI and backplane component cards, e.g. the P0BP1. Using this combination of cards with a PowerPC card, e.g. the PPC4, provides the user with access to a high performance PowerPC processor plus a PCI backplane system with PMC carrier cards and an expanded host PCI bus.

Each P0CC1 allows an extra two single (or one double) width PMC modules to be fitted to the backplane PCI bus. The PCI to PCI bridge on the P0CC1 enables the PowerPC card to maintain concurrent bus operation. This allows applications using PMCs for routing and communications to operate efficiently and in parallel without being blocked.

The I/O on the P0CC1 is routed through the P2 VMEbus connector. For access to a wider range of I/O signals, 5-row connectors are used for the P1 and P2 connectors.

Two single (or one double) width PMC modules may be fitted onto the P0CC1. The PMC slots are compliant with the 32-bit, 33 MHz PCI Specification Revision 2.1, and are normally powered at 5V. 3.3V power may be obtained by additional connections to the P0 backplane. A range of PMCs are available from Radstone, including high-performance graphics, MIL-STD-1553, multi-channel communications, FDDI and ATM. These all fully comply with the IEEE P1386.1 standard.

Documentation Objectives

This manual provides the user with sufficient information to install and use Radstone's P0CC1.

Documentation Scope

This manual describes all build standards and variants of the P0CC1. The Radstone host cards are described in separate manuals. The PMC modules are also described in separate manuals.

Documentation Audience

This manual is written to cover, as far as possible, the range of people who will handle or use the P0CC1, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, grounding, VME and PCI. There is a glossary provided at the back of this manual that explains some of the terms used and expands all abbreviations.

Documentation Structure

This manual is structured in a way that will reflect the sequence of operations from receipt of your P0CC1 up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

Chapter 1 (this chapter) - gives a brief introduction, this manual's objectives, audience and scope, the documentation structure, some warnings, conventions and related documentation.

Chapter 2 - contains unpacking and inspection instructions.

Chapter 3 - describes the P0CC1's connectors.

Chapter 4 - describes the P0CC1's front panel.

Chapter 5 - describes installation of the P0CC1 and PMCs onto the P0CC1.

Chapter 6 - is a functional description.

Chapter 7 - gives Technical Support details.

Appendix A - is a board specification.

There are also a glossary and an index provided.

Documentation Conventions

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a 'D' subscript and binary numbers have a 'b' subscript. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

'**Note:**' highlights information of particular importance.

The multipliers 'k' and 'M' have their conventional scientific and engineering meanings of $*10^3$ and $*10^6$ respectively. The only exception to this is in the description of the size of memory areas, when 'K' and 'M' mean $*2^{10}$ and $*2^{20}$ respectively.

When describing transfer rates, 'k' and 'M' mean $*10^3$ and $*10^6$ *not* $*2^{10}$ and $*2^{20}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI and VMEbus terminology follow the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending in a tilde (~) denote active low signals; all other signals are active high.

Warnings

Only use the P0CC1 in backplanes that supply power on both the J1 and J2 connectors. Failure to observe this warning may result in damage to the board.

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components.



Build Styles

The P0CC1 is available in five electrically compatible build styles. These have two basic mechanical configurations: convection-cooled in accordance with ANSI/VITA 1-1994 spec., and conduction-cooled in accordance with IEEE Std 1101.2-1992.

Convection-cooled boards include:

Level 1
Level 2
Level 3

Conduction-cooled boards include:

Level 4
Level 5

A brief description of each build style follows:

Level 1

Intended for use in benign environments, Level 1 also provides the ideal cost effective method of complete system development. The Level 1 assembly comprises a double-Eurocard size PCB with high quality commercial (plastic encapsulated) components. As software compatibility throughout the build styles is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to target style only in the final stages of system integration.

Level 2

As Level 1, but conformally coated and 100% tested in manufacture to provide an extended operating range.

Level 3

Level 3 boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional, forced-air-cooled, racking systems. These rugged boards comprise a double-Eurocard size printed wiring board fitted with wide temperature range, industrial grade components and are conformally coated as standard.

Level 4

Designed primarily for use in sealed ATR chassis and other conduction-cooled environments the Level 4 board features wide temperature range, industrial grade devices, an integral thermal management layer and incorporates a central stiffening bar for additional strength. Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack to which the boards are secured by screw driven wedgelocks. Level 4 boards are 100% temperature characterised and conformally coated during manufacture. Level 4 is mechanically compliant with IEEE Std. 1101.2-1992.

Level 5

As Level 4, but 100% tested in manufacture to provide an extended operating range.

All five styles fully support the power and versatility of the VMEbus, so no matter how large or diversified your project, absolute compatibility is assured at all stages of development.

Related Documents

Radstone PPC4/PPC4A Manual, publication number PPC4-0HH.

Radstone PMCPCI Manual, publication number PMCPCI-0HH.

ANSI/VITA 1-1994 VME64 Specification.

PCI Local Bus Specification Revision 2.1, PCI Special Interest Group.

PCI System Design Guide Rev 1.0 9/93, PCI Special Interest Group.

EC-QPLDB-TE Digital Semiconductor 21150 PCI to PCI Bridge Maynard, California.

IEEE P1386 Draft Standard for a Common Mezzanine Card Family: CMC.

IEEE P1386.1 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC.

IEEE 1101.2 Conduction-cooled VME Mechanics

IEEE 1014-1987 VMEbus Specification.

Radstone on the Web

Radstone's web site can be found at:

http://www.radstone.co.uk

or

http://www.radstone.com

Chapter 2 - Unpacking and Inspection

This chapter gives guidelines on unpacking and inspecting the P0CC1.



Unpacking

Radstone boards are protected by a static-protective envelope**. Observe antistatic precautions when handling the board (always wear a grounded anti-static wrist strap and work at an approved grounded, static-protected work station).** Keep the board in its static envelope until it is ready to be installed.

The P0CC1 is shipped in an individual, reusable shipping box. When you receive the shipping container, inspect it for any evidence of physical damage. If there is any damage, request that the carrier's agent is present when you open the carton. Keep the contents and packing materials for the agent's inspection and notify Radstone's customer service department of the incident. Retain the packing list for reference.

Assuming that there is no obvious damage, you may still want to keep the shipping carton in case you want to ship the P0CC1 on elsewhere.

Board Identification

Radstone boards are identified by a label fitted to the component side of the board. This label gives the board's material number, revision state, and equipment number. An example follows:

MADE IN UK	P0CC1	Base Rev
10233351	Rev	Rev -

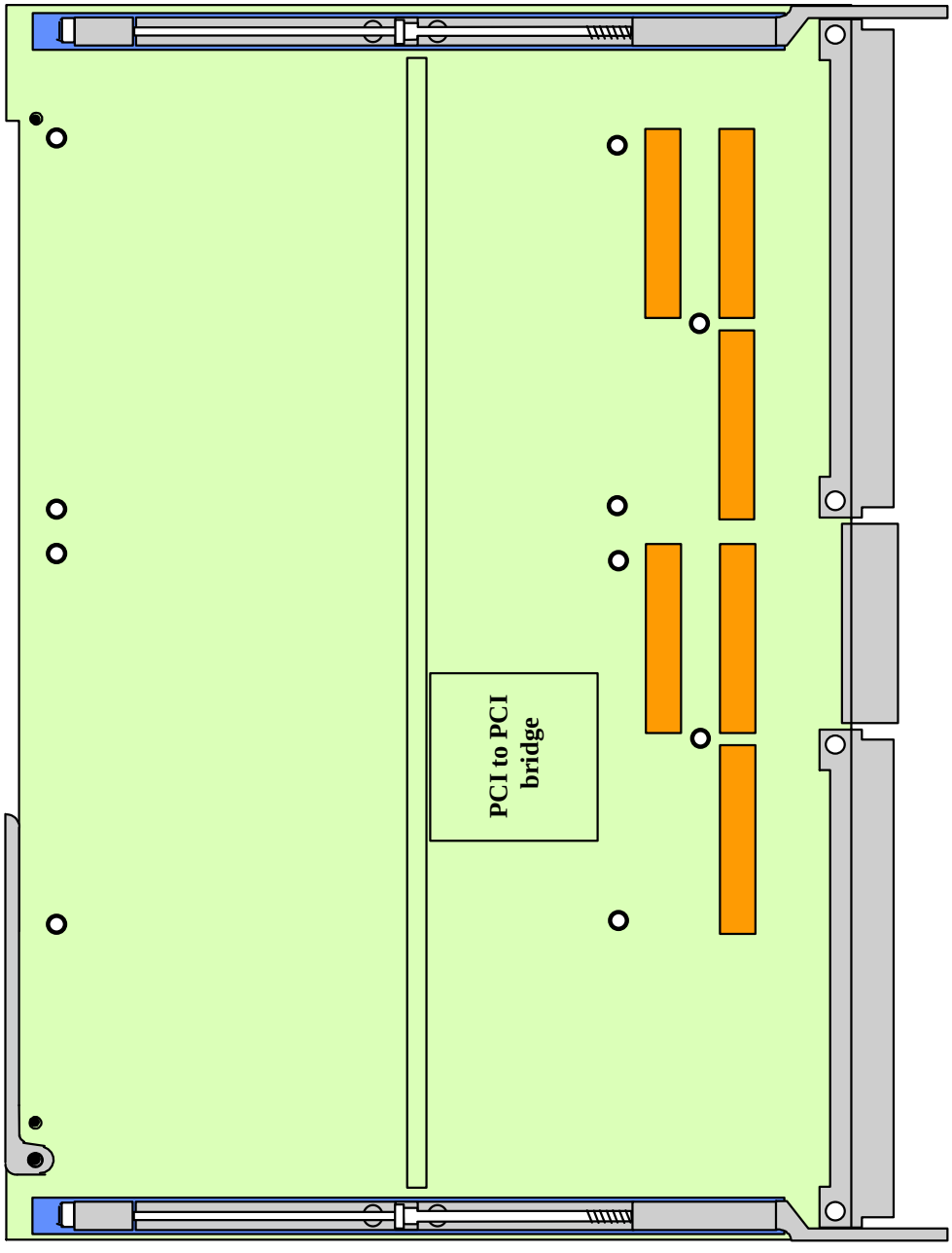
Inspection

Assuming that the P0CC1 is not obviously damaged, you can now go on to inspect it. It is possible for components (connectors, socketed chips etc.) to work loose or be dislodged in transit or in the process of unpacking, although this is extremely unlikely. A quick visual inspection should reveal any obviously loose components. Report any defects you detect to Radstone.

The P0CC1 has no user configurable links.

The following diagram shows the main component layout of the top side of the board:

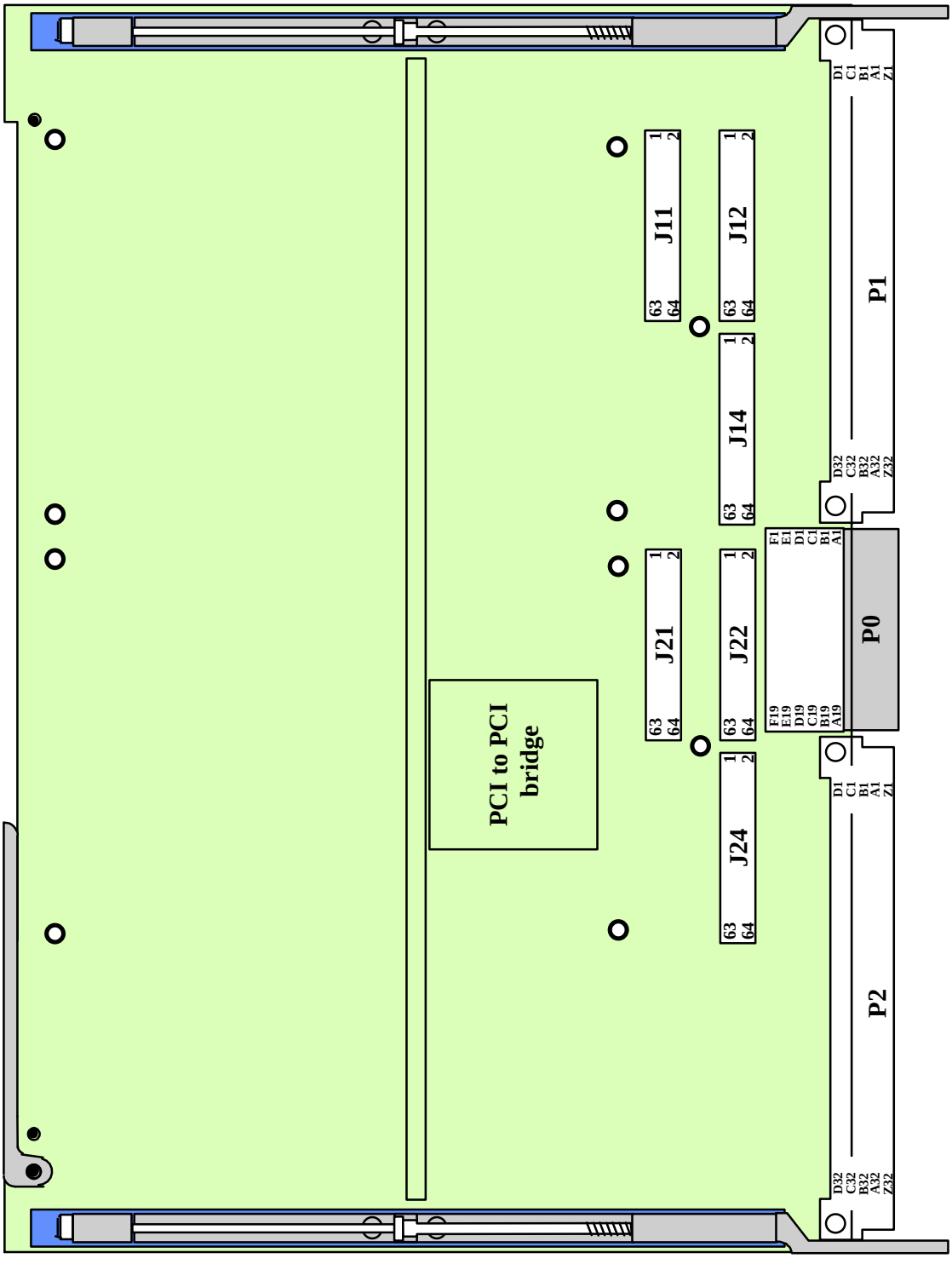
Figure 2-1. General Layout of the P0CC1



Chapter 3 - Connectors

This chapter gives the pinouts for the connectors on the P0CC1. The following diagram shows the connector positions on the top side of the board:

Figure 3-1 Connector Positions and Numbering.



P0 Connector

P0 is the primary PCIbus connector.

Pin Number	Row A	Row B	Row C	Row D	Row E	Row F
1	TCK	TMS	TDI	TDO	TRST~	GND
2	IDSEL	GNT~	REQ~	-	-	GND
3	3.3V†	3.3V†	3.3V†	+5V	+5V	GND
4	PRESENT1~	-	-	-	CLK	GND
5	-	-	-	-	-	GND
6	CBE1	-	-	-	-	GND
7	RESET~	FRAME~	CBE2	CBE3	CBE0	GND
8	PAR	TRDY~	IRDY~	DEVSEL~	LOCK~	GND
9						GND
10						GND
11						GND
12	AD0	AD1	PERR~	SERR~	STOP~	GND
13	AD5	AD2	AD3	IRQW~	IRQX~	GND
14	AD8	AD9	AD6	AD7	AD4	GND
15	AD15	AD12	AD13	AD10	AD11	GND
16	AD18	AD19	AD16	AD17	AD14	GND
17	AD25	AD22	AD23	AD20	AD21	GND
18	IRQZ~	IRQY~	AD26	AD27	AD24	GND
19	+5V	AD30	AD31	AD28	AD29	GND

† The 3.3V pins are NOT connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on PMC connectors and capacitively decoupled to ground.

PRESENT1~ is connected to ground on the P0CC1 to indicate to the master (PMCPCI) card that there are other cards present in the P0 backplane.

PMC Connectors J11 and J21

Pin	Signal	Signal	Pin
1	NO_CONNECT	-12V	2
3	GND	INTA~	4
5	INTB~	INTC~	6
7	BUSMODE1~	+5V	8
9	INTD~	NO_CONNECT	10
11	GND	NO_CONNECT	12
13	CLK	GND	14
15	GND	GNT~	16
17	REQ~	+5V	18
19	+5V	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3~	26
27	AD22	AD21	28
29	AD19	+5V	30
31	+5V	AD17	32
33	FRAME~	GND	34
35	GND	IRDY~	36
37	DEVSEL~	+5V	38
39	GND	LOCK~	40
41	NO_CONNECT	NO_CONNECT	42
43	PAR	GND	44
45	+5V	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0~	52
53	AD06	AD05	54
55	AD04	GND	56
57	+5V	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64~	64

Note: REQ64~ is only connected to a 4k7 pull-up.

PMC Connectors J12 and J22

Pin	Signal	Signal	Pin
1	+12V	NO_CONNECT	2
3	NO_CONNECT	NO_CONNECT	4
5	NO_CONNECT	GND	6
7	GND	NO_CONNECT	8
9	NO_CONNECT	NO_CONNECT	10
11	BUSMODE2~	3.3V **	12
13	RST~	BUSMODE3~	14
15	3.3V **	BUSMODE4~	16
17	NO_CONNECT	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	3.3V **	24
25	IDSEL	AD23	26
27	3.3V **	AD20	28
29	AD18	GND	30
31	AD16	C/BE2~	32
33	GND	NO_CONNECT	34
35	TRDY~	3.3V **	36
37	GND	STOP~	38
39	PERR~	GND	40
41	3.3V **	SERR~	42
43	C/BE1~	GND	44
45	AD14	AD13	46
47	GND	AD10	48
49	AD8	3.3V **	50
51	AD7	NO_CONNECT	52
53	3.3V **	NO_CONNECT	54
55	NO_CONNECT	GND	56
57	NO_CONNECT	NO_CONNECT	58
59	GND	NO_CONNECT	60
61	ACK64~	3.3V **	62
63	GND	NO_CONNECT	64

Notes:

1. ** - The 3.3V pins are *not* connected to a 3.3V supply, they are merely bussed together with the 3.3V pins on connector P0 and capacitively decoupled to ground.
2. BUSMODE2~, ACK64~ are only connected to a 4k7 pull-ups.
3. BUSMODE3~, BUSMODE4~ are only connected to ground.

PMC I/O Connectors J14 and J24

Pin	Signal	Signal	Pin
1	PMCx_IO_01	PMCx_IO_02	2
3	PMCx_IO_03	PMCx_IO_04	4
5	PMCx_IO_05	PMCx_IO_06	6
7	PMCx_IO_07	PMCx_IO_08	8
9	PMCx_IO_09	PMCx_IO_10	10
11	PMCx_IO_11	PMCx_IO_12	12
13	PMCx_IO_13	PMCx_IO_14	14
15	PMCx_IO_15	PMCx_IO_16	16
17	PMCx_IO_17	PMCx_IO_18	18
19	PMCx_IO_19	PMCx_IO_20	20
21	PMCx_IO_21	PMCx_IO_22	22
23	PMCx_IO_23	PMCx_IO_24	24
25	PMCx_IO_25	PMCx_IO_26	26
27	PMCx_IO_27	PMCx_IO_28	28
29	PMCx_IO_29	PMCx_IO_30	30
31	PMCx_IO_31	PMCx_IO_32	32
33	PMCx_IO_33	PMCx_IO_34	34
35	PMCx_IO_35	PMCx_IO_36	36
37	PMCx_IO_37	PMCx_IO_38	38
39	PMCx_IO_39	PMCx_IO_40	40
41	PMCx_IO_41	PMCx_IO_42	42
43	PMCx_IO_43	PMCx_IO_44	44
45	PMCx_IO_45	PMCx_IO_46	46
47	PMCx_IO_47	PMCx_IO_48	48
49	PMCx_IO_49	PMCx_IO_50	50
51	PMCx_IO_51	PMCx_IO_52	52
53	PMCx_IO_53	PMCx_IO_54	54
55	PMCx_IO_55	PMCx_IO_56	56
57	PMCx_IO_57	PMCx_IO_58	58
59	PMCx_IO_59	PMCx_IO_60	60
61	PMCx_IO_61	PMCx_IO_62	62
63	PMCx_IO_63	PMCx_IO_64	64

Where: x = 1 for J14 (PMC site 1)

x = 2 for J24 (PMC site 2)

VMEbus P1 Connector Pin-out

Pin	row Z	row A	row B	row C	row D
1	-	-	-	-	+5V
2	GND	-	-	-	GND
3	-	-	-	-	-
4	GND	-	BG0IN~	-	-
5	-	-	BG0OUT~	-	-
6	GND	-	BG1IN~	-	-
7	-	-	BG1OUT~	-	-
8	GND	-	BG2IN~	-	-
9	-	GND	BG2OUT~	GND	-
10	GND	-	BG3IN~	-	-
11	-	GND	BG3OUT~	-	-
12	GND	-	-	-	-
13	-	-	-	-	-
14	GND	-	-	-	-
15	-	GND	-	-	-
16	GND	-	-	-	-
17	-	GND	-	-	-
18	GND	-	-	-	-
19	-	GND	-	-	-
20	GND	-	GND	-	-
21	-	IACKIN~	-	-	-
22	GND	IACKOUT~	-	-	-
23	-	-	GND	-	-
24	GND	-	-	-	-
25	-	-	-	-	-
26	GND	-	-	-	-
27	-	-	-	-	-
28	GND	-	-	-	-
29	-	-	-	-	-
30	GND	-	-	-	-
31	-	-12V	+5VSTDBY	+12V	GND
32	GND	+5V	+5V	+5V	+5V

Notes:

1. - = Not connected.
2. xxxIN~ is connected to xxxOUT~.

VMEbus P2 Connector Pin-out (Standard)

Pin	row Z	row A	row B	row C	row D
1	PMC1_IO_2	PMC2_IO_2	+5V	PMC2_IO_1	PMC1_IO_1
2	GND	PMC2_IO_4	GND	PMC2_IO_3	PMC1_IO_3
3	PMC1_IO_5	PMC2_IO_6	-	PMC2_IO_5	PMC1_IO_4
4	GND	PMC2_IO_8	-	PMC2_IO_7	PMC1_IO_6
5	PMC1_IO_8	PMC2_IO_10	-	PMC2_IO_9	PMC1_IO_7
6	GND	PMC2_IO_12	-	PMC2_IO_11	PMC1_IO_9
7	PMC1_IO_11	PMC2_IO_14	-	PMC2_IO_13	PMC1_IO_10
8	GND	PMC2_IO_16	-	PMC2_IO_15	PMC1_IO_12
9	PMC1_IO_14	PMC2_IO_18	-	PMC2_IO_17	PMC1_IO_13
10	GND	PMC2_IO_20	-	PMC2_IO_19	PMC1_IO_15
11	PMC1_IO_17	PMC2_IO_22	-	PMC2_IO_21	PMC1_IO_16
12	GND	PMC2_IO_24	GND	PMC2_IO_23	PMC1_IO_18
13	PMC1_IO_20	PMC2_IO_26	+5V	PMC2_IO_25	PMC1_IO_19
14	GND	PMC2_IO_28	-	PMC2_IO_27	PMC1_IO_21
15	PMC1_IO_23	PMC2_IO_30	-	PMC2_IO_29	PMC1_IO_22
16	GND	PMC2_IO_32	-	PMC2_IO_31	PMC1_IO_24
17	PMC1_IO_26	PMC2_IO_34	-	PMC2_IO_33	PMC1_IO_25
18	GND	PMC2_IO_36	-	PMC2_IO_35	PMC1_IO_27
19	PMC1_IO_29	PMC2_IO_38	-	PMC2_IO_37	PMC1_IO_28
20	GND	PMC2_IO_40	-	PMC2_IO_39	PMC1_IO_30
21	PMC1_IO_32	PMC2_IO_42	-	PMC2_IO_41	PMC1_IO_31
22	GND	PMC2_IO_44	GND	PMC2_IO_43	PMC1_IO_33
23	PMC1_IO_35	PMC2_IO_46	-	PMC2_IO_45	PMC1_IO_34
24	GND	PMC2_IO_48	-	PMC2_IO_47	PMC1_IO_36
25	PMC1_IO_38	PMC2_IO_50	-	PMC2_IO_49	PMC1_IO_37
26	GND	PMC2_IO_52	-	PMC2_IO_51	PMC1_IO_39
27	PMC1_IO_41	PMC2_IO_54	-	PMC2_IO_53	PMC1_IO_40
28	GND	PMC2_IO_56	-	PMC2_IO_55	PMC1_IO_42
29	PMC1_IO_44	PMC2_IO_58	-	PMC2_IO_57	PMC1_IO_43
30	GND	PMC2_IO_60	-	PMC2_IO_59	PMC1_IO_45
31	PMC1_IO_46	PMC2_IO_62	GND	PMC2_IO_61	GND
32	GND	PMC2_IO_64	+5V	PMC2_IO_63	+5V

Notes:

1. - = Not connected.
2. xxxIN~ is connected to xxxOUT~.

VMEbus P2 Connector Pin-out (Optional)

To allow the I/O of both PMC sites to come out on rows A and C of P2, a build option is provided that routes the first 32-bits of the PMC I/O of each site into rows A and C (differences from the standard pinout are shown in bold). The original I/O routing to rows Z and D remains unchanged (in italics):

Pin	row Z	row A	row B	row C	row D
1	*PMC1_IO_2*	PMC2_IO_2	+5V	PMC2_IO_1	*PMC1_IO_1*
2	GND	PMC2_IO_4	GND	PMC2_IO_3	*PMC1_IO_3*
3	*PMC1_IO_5*	PMC2_IO_6	-	PMC2_IO_5	*PMC1_IO_4*
4	GND	PMC2_IO_8	-	PMC2_IO_7	*PMC1_IO_6*
5	*PMC1_IO_8*	PMC2_IO_10	-	PMC2_IO_9	*PMC1_IO_7*
6	GND	PMC2_IO_12	-	PMC2_IO_11	*PMC1_IO_9*
7	*PMC1_IO_11*	PMC2_IO_14	-	PMC2_IO_13	*PMC1_IO_10*
8	GND	PMC2_IO_16	-	PMC2_IO_15	*PMC1_IO_12*
9	*PMC1_IO_14*	PMC2_IO_18	-	PMC2_IO_17	*PMC1_IO_13*
10	GND	PMC2_IO_20	-	PMC2_IO_19	*PMC1_IO_15*
11	*PMC1_IO_17*	PMC2_IO_22	-	PMC2_IO_21	*PMC1_IO_16*
12	GND	PMC2_IO_24	GND	PMC2_IO_23	*PMC1_IO_18*
13	*PMC1_IO_20*	PMC2_IO_26	+5V	PMC2_IO_25	*PMC1_IO_19*
14	GND	PMC2_IO_28	-	PMC2_IO_27	*PMC1_IO_21*
15	*PMC1_IO_23*	PMC2_IO_30	-	PMC2_IO_29	*PMC1_IO_22*
16	GND	PMC2_IO_32	-	PMC2_IO_31	*PMC1_IO_24*
17	*PMC1_IO_26*	**PMC1_IO_2**	-	**PMC1_IO_1**	*PMC1_IO_25*
18	GND	**PMC1_IO_4**	-	**PMC1_IO_3**	*PMC1_IO_27*
19	*PMC1_IO_29*	**PMC1_IO_6**	-	**PMC1_IO_5**	*PMC1_IO_28*
20	GND	**PMC1_IO_8**	-	**PMC1_IO_7**	*PMC1_IO_30*
21	*PMC1_IO_32*	**PMC1_IO_10**	-	**PMC1_IO_9**	*PMC1_IO_31*
22	GND	**PMC1_IO_12**	GND	**PMC1_IO_11**	*PMC1_IO_33*
23	*PMC1_IO_35*	**PMC1_IO_14**	-	**PMC1_IO_13**	*PMC1_IO_34*
24	GND	**PMC1_IO_16**	-	**PMC1_IO_15**	*PMC1_IO_36*
25	*PMC1_IO_38*	**PMC1_IO_18**	-	**PMC1_IO_17**	*PMC1_IO_37*
26	GND	**PMC1_IO_20**	-	**PMC1_IO_19**	*PMC1_IO_39*
27	*PMC1_IO_41*	**PMC1_IO_22**	-	**PMC1_IO_21**	*PMC1_IO_40*
28	GND	**PMC1_IO_24**	-	**PMC1_IO_23**	*PMC1_IO_42*
29	*PMC1_IO_44*	**PMC1_IO_26**	-	**PMC1_IO_25**	*PMC1_IO_43*
30	GND	**PMC1_IO_28**	-	**PMC1_IO_27**	*PMC1_IO_45*
31	*PMC1_IO_46*	**PMC1_IO_30**	GND	**PMC1_IO_29**	GND
32	GND	**PMC1_IO_32**	+5V	**PMC1_IO_31**	+5V

Chapter 4 - Front Panel

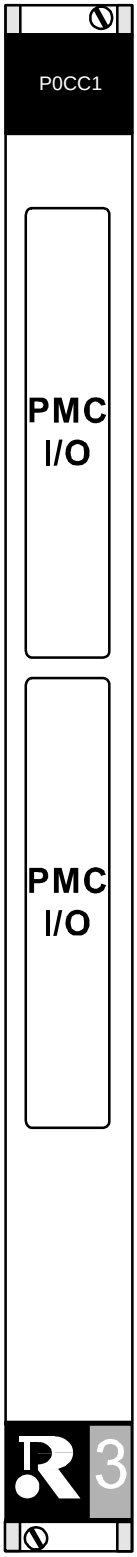
This chapter describes the features found on the P0CC1 front panel.

Front Panel I/O

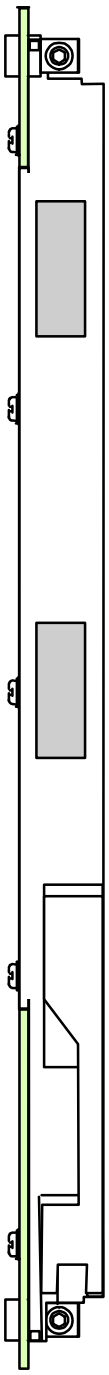
On air-cooled versions of the P0CC1, I/O can be brought out through the front panel. There are two PMC slots for two single (or one double) width PMCs.

On the conduction-cooled version of the P0CC1, I/O through the front panel is limited to those PMCs that have suitably placed connectors (e.g. Radstone's PMC2-9100 graphics accelerator PMC).

Figure 4-1 P0CC1 Front Panels



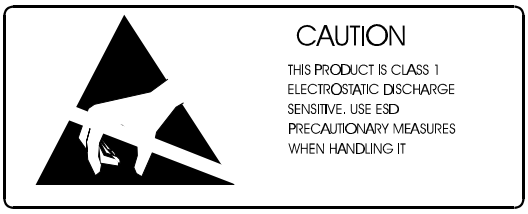
Air-cooled
Build Levels 1, 2 and 3



Conduction-cooled
Build levels 4 and 5

Chapter 5 - Installation

This chapter describes the installation of the P0CC1 board in a system.



Caution

When using a conduction-cooled board in a commercial backplane, please ensure that the wedgelocks do not interfere with any backplane connection points such as the Ground or Vcc points near the P1 and P2 connectors.

System Backplane Configuration Links

The P0CC1 carries out VME Bus Grant and IACK daisy chaining via tracking on the board. It is therefore unaffected by any backplane links governing daisy chaining for the slot occupied.

Chassis Ground

To ensure optimum operation of the air-cooled P0CC1 with regard to EMC, when taking I/O connections from the front panel connectors, there should always be a connection from the front panel to the chassis ground of the system.

The P0CC1 is unlikely to operate on a VME bus extender due to the extra tracking the extender would add to the P0-based PCI bus.

P0 PCI Backplane

Ensure that the P0CC1 is plugged into a P0 PCI backplane slot that conforms to the P0 connections as detailed on page 3-2, for instance one of Radstone's P0BP1 range of backplanes. These are a series of PCBs for attaching to a system backplane that has J0 connectors fitted. The following variants are available:

P0BP1-502	Two slot PCI backplane. One master slot and one P0CC1 slot.
P0BP1-503	Three slot PCI backplane. One master slot and two P0CC1 slots.
P0BP1-504	Four slot PCI backplane. One master slot and three P0CC1 slots.
P0BP1-505	Five slot PCI backplane. One master slot and four P0CC1 slots.

The P0BP1 backplane must be soldered onto the J0 system backplane, and can be used with either type A or type B J0. These backplanes are intended to have a host SBC with PMCPCI card plugged into the master slot, which is the left-most slot of the P0 PCI backplane.

PMC Installation

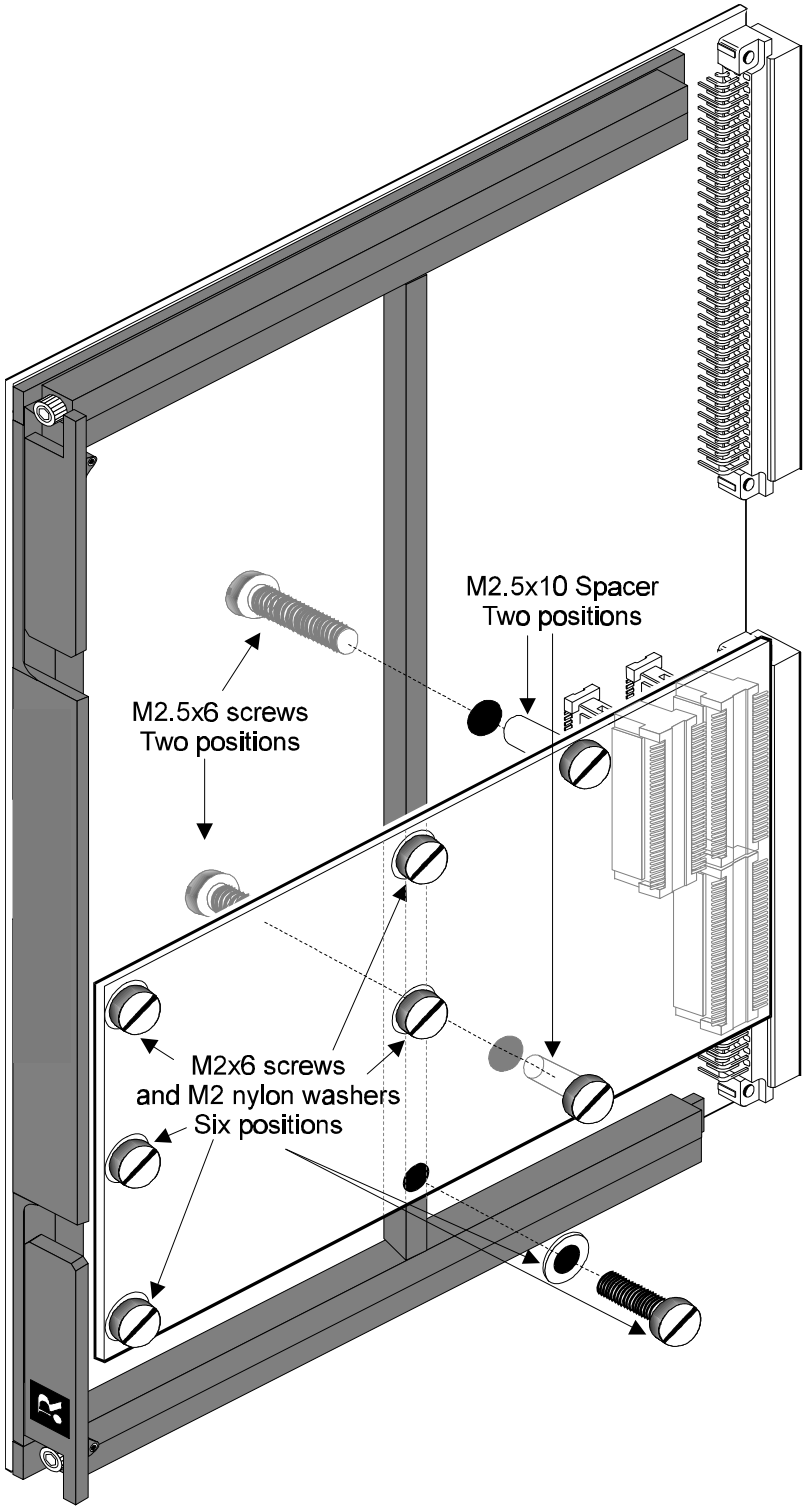
Two single width (or one double width) PMC modules may be fitted to the P0CC1 as shown in Figure 5-1. The P0CC1 is keyed to accept only 5V PMC modules.

Each PMC module is supplied with a full kit of parts for mounting it, full fitting instructions and a manual (which also normally contains instructions on how to fit the module). The installation of driver software or other firmware configuration may be required to achieve full functionality of a PMC module (see the specific PMC manual for the exact procedure). PMC modules ordered with a P0CC1 are supplied factory fitted by Radstone.

If the PMC is an air-cooled module from Radstone's rugged PMC range, a half-height central stiffening bar should be fitted to the PMC before installation. If this type of PMC module is ordered with a P0CC1, this will be done by Radstone.

Before fitting your own PMC module, remove the blanking plate from the PMC slot in the front panel. The PMC's bezel will fill the slot and usually provides connection to the module.

Figure 5-1. PMC Installation

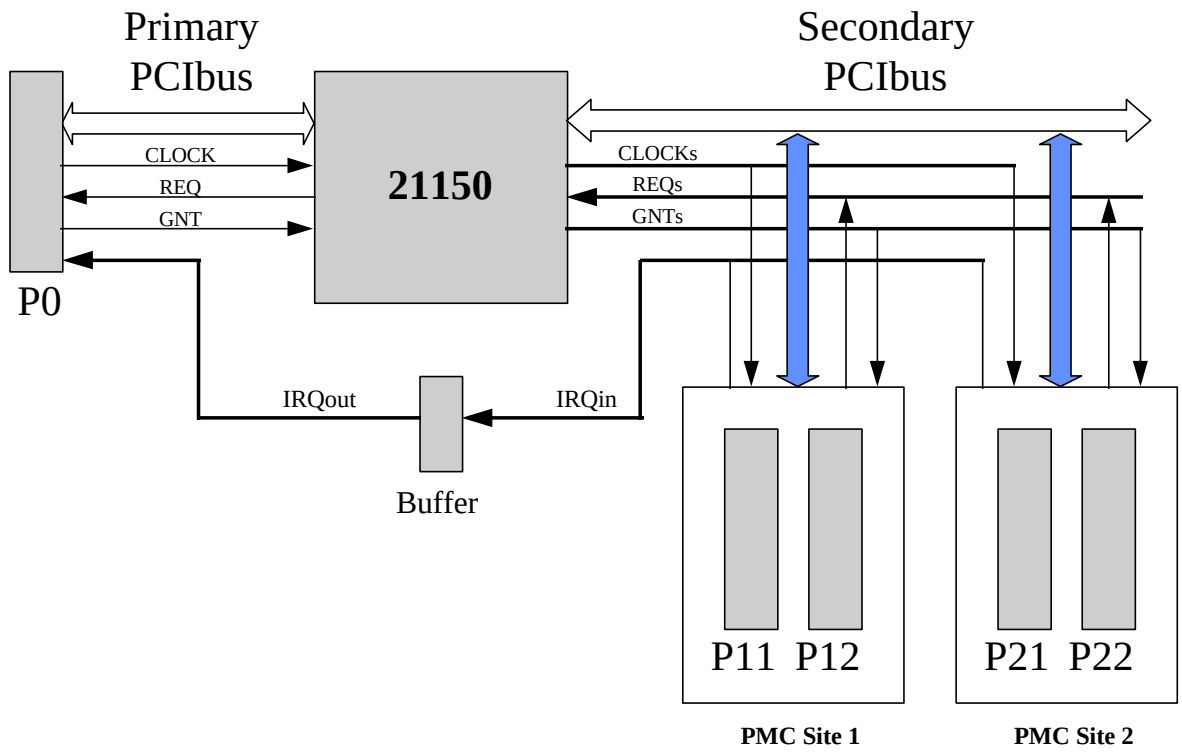


Chapter 6 - Functional Description

This chapter describes the P0CC1's main functional blocks.

The P0CC1 is a PCI to PCI bridge that takes the primary PCI bus from the P0 connector and bridges it to an on-board secondary PCI bus, as shown in the diagram below. On the secondary PCI bus there are two PMC sites.

Figure 6-1. Block Diagram



The P0CC1 card receives unique primary IDSEL, clock, and PCI request and grant line signals from the P0 PCI backplane. The backplane must also provide rotation for the interrupt request lines, which are buffered down to the primary PCI bus (P0). There is no facility for generating PCI interrupts on the secondary PCI bus.

Power Supply

The P0CC1 contains a 3.3V regulator to provide power to the core of the 21150 PCI to PCI bridge chip. There is no on-board 3.3V supply for the PMC sites, although there is provision for 3.3V to be fed to the PMC sites via the P0 backplane.

The primary and secondary PCI busses are configured for 5V signalling only.

Hard Reset

The 21150 bridge chip takes in the primary PCI bus reset and generates the secondary PCI bus reset from it. The primary reset also resets the PCI to PCI Bridge chip.

There is also a ***Chip Reset*** bit in the **Diagnostic Control** register that can be used to reset the 21150 bridge chip and the secondary PCI bus. When the ***Chip Reset*** bit is set, all the registers and the state of the chip are reset, and all signals are tri-stated. In addition, the secondary PCI bus reset is asserted, and the ***Secondary Reset*** bit is set. The ***Chip Reset*** bit self-clears within 20 PCI clock cycles after completion of the write cycle that set it. After this period, the 21150 bridge is ready for configuration. The secondary PCI bus reset signal remains asserted until a configuration write operation clears the ***Secondary Reset*** bit and the serial clock mask has been shifted in.

During chip reset, the 21150 bridge chip is inaccessible.

PCI to PCI Bridge Chip

The 21150 PCI to PCI bridge chip provides the P0CC1 with the following features:

- Complies fully with Revision 2.1 of the PCI Local Bus Specification
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands - up to three transactions simultaneously in each direction
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction - up to five posted write transactions simultaneously in each direction
- Allows 72 bytes of read data buffering in each direction
- Concurrent primary and secondary bus operation, to isolate traffic
- A programmable 2-level arbiter for secondary bus arbitration
- Enhanced address decoding:
  - A 32-bit I/O address range
  - A 32-bit memory-mapped I/O address range
  - A 64-bit prefetchable memory address range
  - ISA-aware mode for legacy support in the first 64 Kbytes of the I/O address range
  - VGA addressing and VGA palette snooping support
- Supports PCI transaction forwarding for the following commands:
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration commands
- Includes downstream lock support
- An IEEE standard 1149.1 JTAG interface

PMC Sites

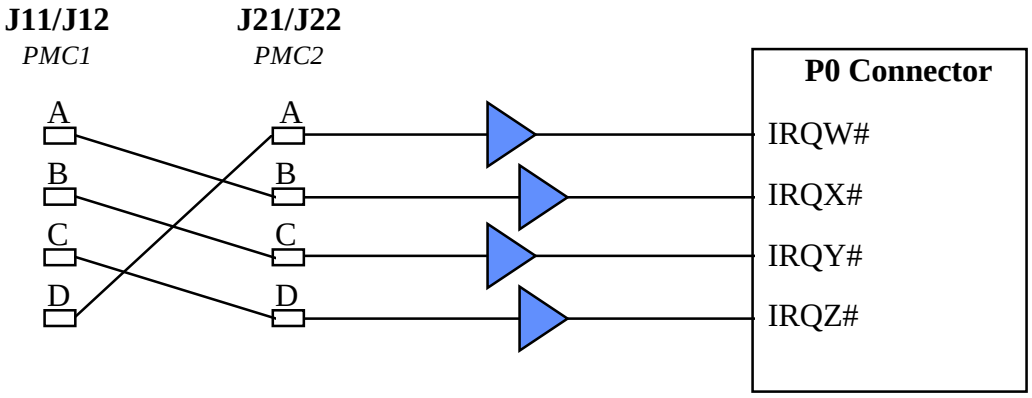
One or two PMCs, conforming to the conduction-cooled PMC draft standard for level 4 boards or IEEE P1386 for level 1, 2, and 3 boards, may be connected to the P0CC1 through the PMC expansion slots. I/O connections to such modules are through the P2 connector (and P0, if fitted) for all build levels. On levels 1, 2 and 3 direct connection to the PMCs through the front panel is also possible. The PMCs may be +5V, ±12V or 3.3V powered (if 3.3V is supplied via the P0 backplane).

The primary and secondary PCI busses only support 32-bit PCI communications with 5V signalling.

PCI Interrupts

There are 4 interrupt lines for the PMC expansion slots on the P0CC1. These are connected together and buffered down to the backplane via the P0 connector. The interrupt routing follows the recommendations in the PCI specification and the PCI system design guide with a ‘rotation’ between each slot.

The interrupt lines for the two on-board PMC slots are routed as shown below:



Two single function PMCs (which always use INTA~) are able to use unique IRQs with appropriate programming of the interrupt controller.

Notes:

1. Further rotation normally occurs in the P0 backplane and on the host board that contains the PMCPCI card.
2. When using a PPC4 with a PMCPCI card in PMC site 1, with this assembly plugged into a P0BP1 backplane and the P0CC1 connected in the next slot, IRQW~ of the P0CC1 will arrive on the PPC4 as **A** on **PMC1** and undergo a further rotation to become PIRQ1~ on the ISA bridge of the PPC4, (see the PPC4 manual for information regarding the PCI interrupts).

I/O Registers

Several I/O registers exist on the P0CC1 for controlling or reading the status of the PCI bus, as listed below:

PCI to PCI Bridge Standard Configuration Registers

Register	Offset (Hex)
Vendor ID	0x00
Device ID	0x02
Command	0x04
Status	0x06
Revision ID	0x08
Programming Interface	0x09
Subclass Code	0x0A
Base Class Code	0x0B
Cache Line Size	0x0C
Primary Latency Timer	0x0D
Header Type	0x0E
Primary Bus Number	0x18
Secondary Bus Number	0x19
Subordinate Bus Number	0x1A
Secondary Latency Timer	0x1B
I/O Base Address	0x1C
I/O Limit Address	0x1D
Secondary Status	0x1E
Memory Base Address	0x20
Memory Limit Address	0x22
Prefetchable Memory Base Address	0x24
Prefetchable Memory Limit Address	0x26
Prefetchable Memory Base Address Upper 32 Bits	0x28
Prefetchable Memory Limit Address Upper 32 Bits	0x2C
I/O Base Address Upper 16 Bits	0x30
I/O Limit Address Upper 16 Bits	0x32
Subsystem Vendor ID	0x34
Subsystem ID	0x36
Interrupt Pin	0x3D
Bridge Control	0x3E

Device-Specific Configuration Registers

Register	Offset (Hex)
Chip Control	0x40
Diagnostic Control	0x41
Arbiter Control	0x42
p_serr_l Event Disable	0x64
gpio Output Data	0x65
gpio Output Enable Control	0x66
gpio Input Data	0x67
Secondary Clock Control	0x68
p_serr_l Status	0x6A

JTAG

The P0CC1 has a JTAG chain, which is ***intended for factory use only***.

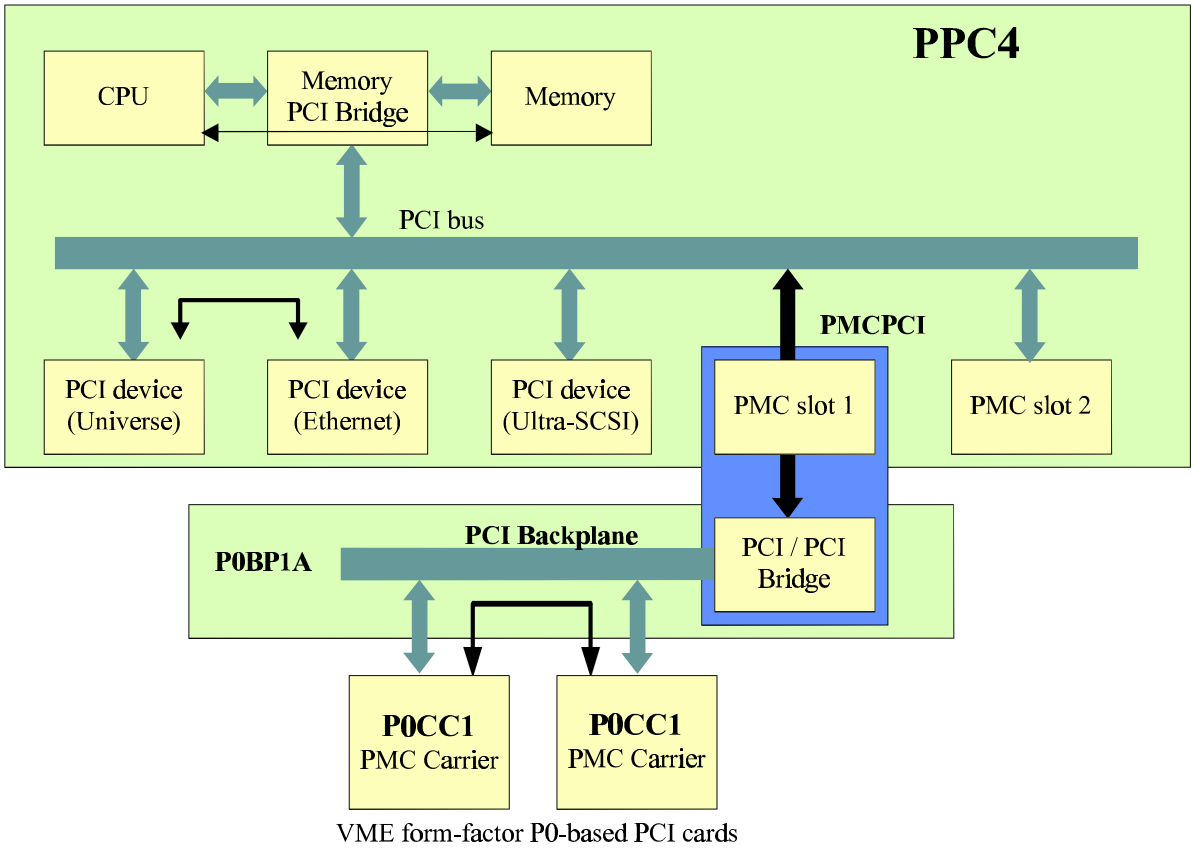
The JTAG chain connects the 21150 to PMC site 1 and then to PMC site 2. If a site is unpopulated, then it is automatically bypassed. The JTAG chain connections appear on the P0 connector (see Chapter 3).

PCI

PCI has become a highly desirable local interface bus, due to its high bandwidth, glueless interface and low cost. PCI provides a synchronous 32-bit multiplexed address and data bus (with future expansion capability to 64-bit), allowing burst data transfers to 132 Mbytes/second. The PCI mezzanine format also provides 64 I/O pins for user definition.

Using a PPC4 as a PowerPC host card, a PCI to PCI bridge on the PMCPCI card connecting to a P0 backplane, the P0CC1 carrier card and other P0 PCI based cards may look like the following:

Figure 6-1. PCI Connectivity



In this configuration, the CPU to Memory bus, two devices on the PPC4 PCI bus and two cards on the P0 PCI backplane may all operate concurrently. If there are more P0CC1 cards on the backplane, then their PMC sites may communicate with each other concurrently within this configuration, as the P0CC1 has the PMC sites on a secondary side of a PCI to PCI bridge.

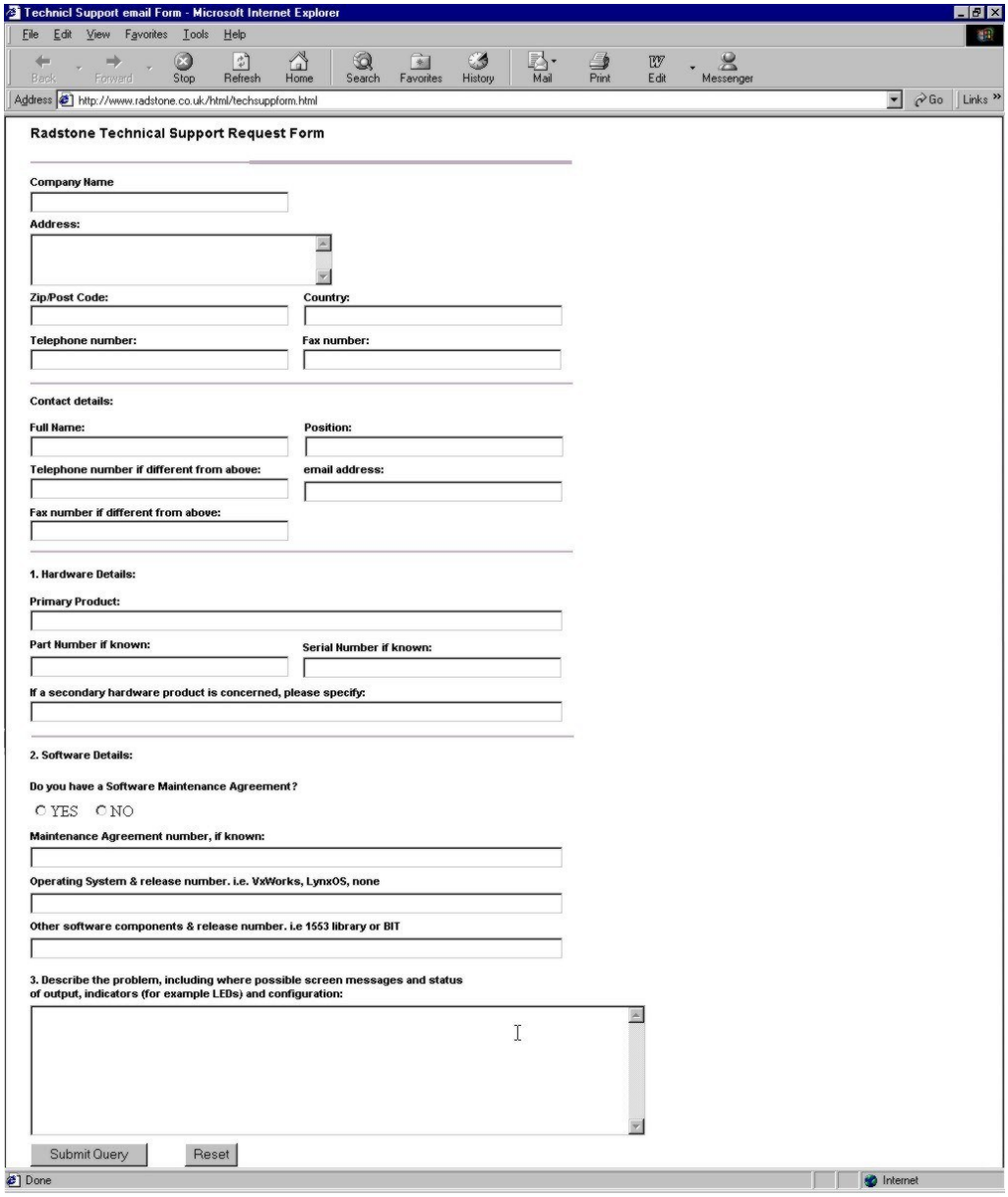
Chapter 7 - Technical Support

Radstone Contact Information

In the unlikely event that you experience problems with your P0CC1, for assistance please contact Radstone's Technical Help Line on:

+44 1327 359804 outside the UK
01327 359804 in the UK

Alternatively, you may also register support requests using the Technical Support Request Form available through the Radstone web site at http://www.radstone.co.uk. This form looks like:



Your query will be logged on Radstone's Technical Support database and allocated a unique Call Reference Number (CRN) for use in future correspondence.

If you telephone for technical support, please be prepared to provide the above details.

Helpful Hints

If you *are* experiencing a problem with your P0CC1 and are awaiting a response from Radstone's technical support, there follow some rudimentary suggestions that you may also like to try to get your P0CC1 operational.

First make sure that the P0CC1 is correctly positioned in a P0 backplane and that there is a P0 controller card taking care of the P0 backplane (e.g. a PMCPCI card fitted to a PPC4 in the left-most slot of a P0BP1 and the P0CC1 is correctly fitted into the same P0BP1).

To make sure that it is not the host CPU card causing the problem, if you have not already done so, ensure that the host operates successfully in isolation (i.e. without the P0CC1 fitted). Troubleshooting suggestions for hosts like the PPC2A or PPC4 can be found in the corresponding manuals. By doing this, you can eliminate the host as being the source of the problem, and narrow the scope to the P0CC1 or the PMC(s).

Similarly, by ensuring that the PMCs work successfully when fitted straight onto a host like the PPC4, rather than via the P0CC1, you can reduce the possibility of the PMC/host combination as being the source of the problem as well.

Having narrowed the scope to the P0CC1, the problem is most likely to be caused by a faulty connection somewhere, as the P0CC1 is mainly a mechanical PCI bus expander, with virtually no software components. If you have two PMCs fitted on the P0CC1, and find that one PMC operates successfully while the other doesn't, this suggests a connection problem between the non-working PMC and the P0CC1. Try removing and reattaching the PMC, as described in the PMC's manual. You could also try rearranging the order of the PMCs on the P0CC1.

The P0CC1 is intended only to be used with a PMCPCI card fitted to a Radstone host card and Radstone P0BP1 or P0BP3 backplane, so any problems you may encounter in trying to use the P0CC1 with any other host board or backplane may be beyond the scope of Radstone's assistance.

Appendix A - Specifications

Mechanical Specification

Levels 1, 2 and 3. Are double Eurocard sized, conformally coated for levels 2 and 3, and occupy a single VMEbus card slot, with mechanics complying with IEEE 1014-1987. The card has five row P1 and P2 connectors, in line with the VME64 Extensions draft standard. There is a P0 connector and there are two PCI expansion slots. I/O access is available through the front panel, and PMC I/O is also mapped to P2.

Levels 4 and 5. Are double Eurocard sized, conformally coated, and occupy a single VMEbus card slot, with mechanics complying with IEEE 1101.2-1992 for conduction cooling. The card has five row P1 and P2 connectors, in line with the VME64 Extensions draft standard. There is a P0 connector and there are two PCI expansion slots with P2 access, plus limited access via the front panel.

Power Requirements

Power supply requirements for the P0CC1 with no PMC cards fitted are:

	No PMCs fitted
+5 V (+5 %,-2.5 %)	100 mA

The ±12 V supply lines are not used by the board, but they do feed the PMC sites.

WARNING
The P0CC1 must only be used in backplanes that supply power on both the J1 and J2 connectors. Failure to observe this warning may result in damage to the board.

The P0CC1 uses the undefined pins (rows a, c, d and z) of the VMEbus P2 connector for I/O and power/ground connections, as shown in Chapter 3.

Environmental Specifications

The P0CC1 is available in build levels 1 to 5 to meet a variety of environmental requirements from commercial air-cooled to rugged conduction-cooled. The exact test methods used to verify these environmental requirements are detailed in Radstone's test methods specification.

Convection-cooled Boards

Build Style	Operating Temp (°C)	Storage Temp (°C)	Vibration	Shock	Humidity	Comments
Standard (Level 1)	0 to +55 with airflow of 300 feet/minute	-50 to +100	$0.002g^2$/Hz from 10 to 2000 Hz random, and 2g sinusoidal from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications.
Extended Temp (Level 2)	-20 to +65 with airflow of 300 feet/minute	-50 to +100	$0.002g^2$/Hz from 10 to 2000 Hz random, and 2g sinusoidal from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformally coated and temperature characterised.
Rugged Air-cooled (Level 3)	-40 to +75 with airflow of 600 feet/minute	-50 to +100	$0.04g^2$/Hz from 10 to 2000 Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection.

Conduction-cooled Boards

Build Style	Operating Temp (°C)	Storage Temp (°C)	Vibration	Shock	Humidity	Comments
Rugged Conduction-cooled (Level 4)	-40 to +75 at the thermal interface	-50 to +100	Random $0.1g^2$/Hz from 5 to 2000 Hz per MIL-STD-810E	40g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.
Rugged Conduction-cooled (Level 5)	-40 to +85 at the thermal interface	-50 to +100	Random $0.1g^2$/Hz from 5 to 2000 Hz per MIL-STD-810E	40g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.

Mean Time Between Failures

The following table shows the calculated MTBFs for some example configurations of the P0CC1. The failure rates are based only on the components and connectors fitted to the P0CC1 at delivery and take no account of user-fitted PMC modules. The failure rates are calculated using MIL-HDBK-217F Notice 1 and field data for the Naval Sheltered environment, plus Bellcore data for the Ground Benign and Ground Fixed environments. Where a component does not comply with the MIL-HDBK (commercial or non-military quality level), the closest equivalent, compliant component is used.

Configuration		Ground Benign (30°C)	Ground Fixed (40°C)	Naval Sheltered (40°C)
P0CC1-1000A	Failures/million hours	0.463594	1.27457	2.25281
	MTBF	2,157,060	784,578	443,890
P0CC1-1100A	Failures/million hours	0.463594	1.27457	2.25281
	MTBF	2,157,060	784,578	443,890

See the Ordering Information section for an explanation of the above configurations.

EMC Regulatory Compliance and Safety

Air-cooled versions of P0CC1 are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

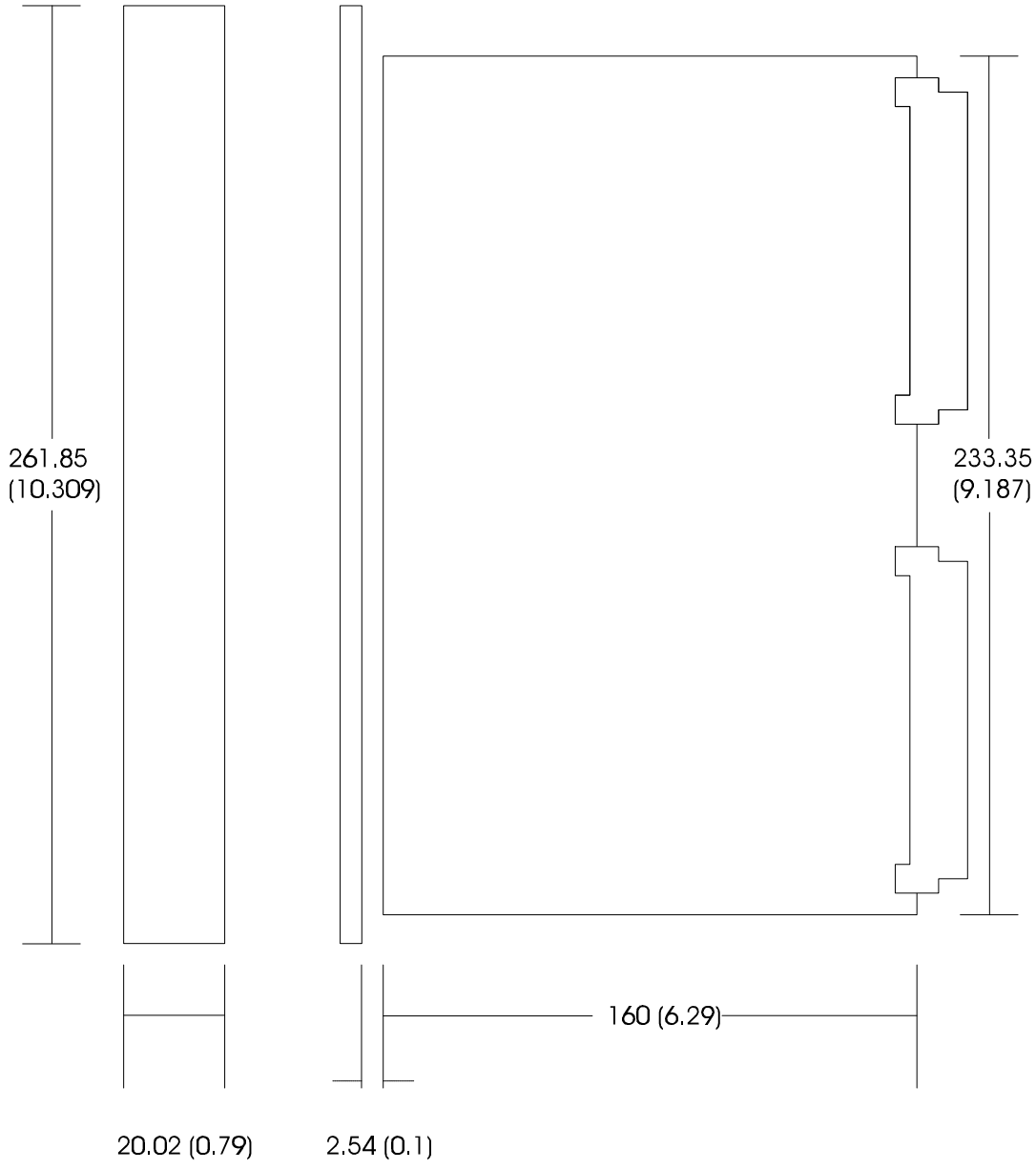
Conduction-cooled versions are designed for integration into EMC hardened cabinets/boxes.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

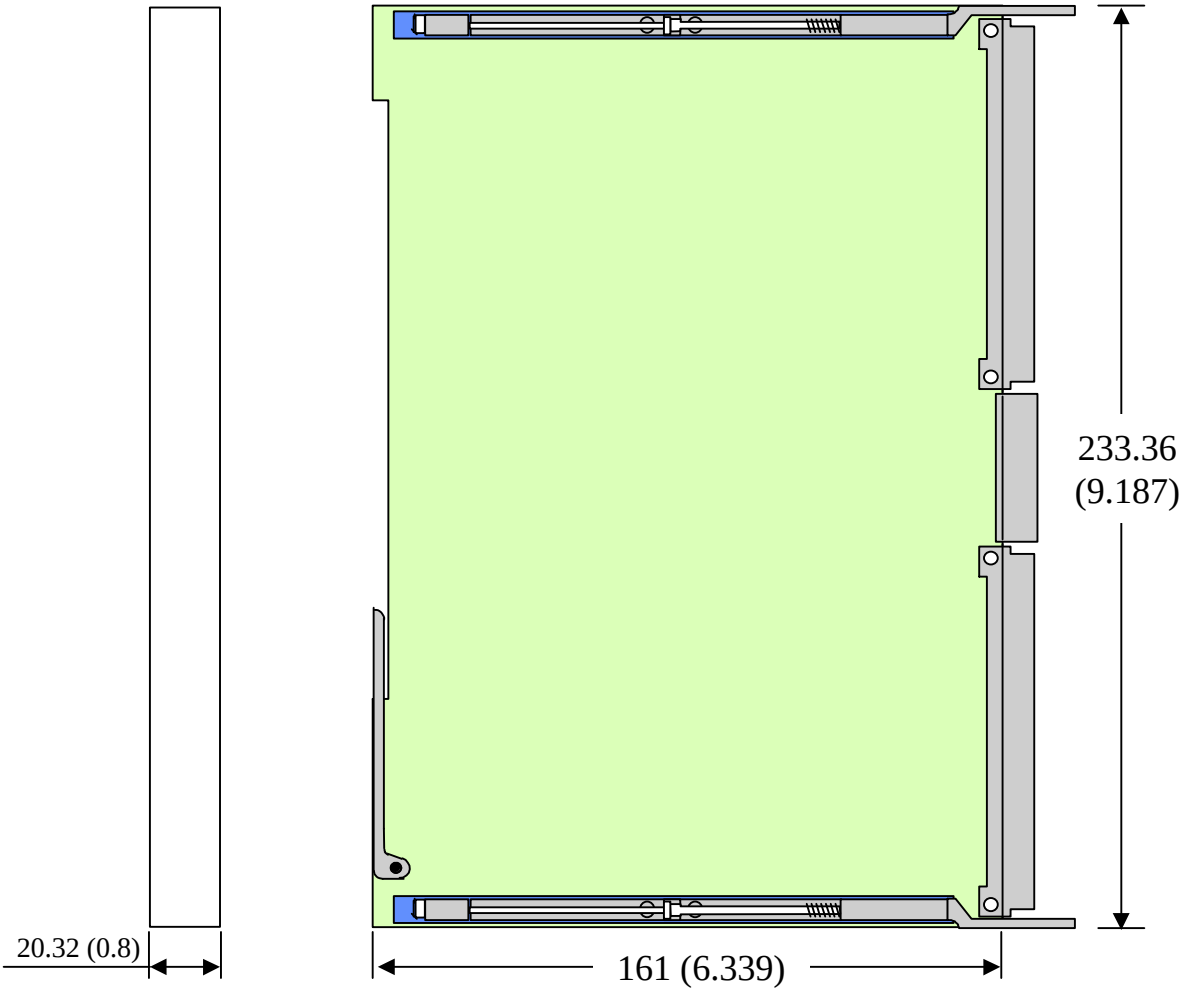
Mechanical Construction

Dimensions

The air-cooled P0CC1 is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.



The Conduction-cooled P0CC1 is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the IEEE 1101.2. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.



Weight

The weight of the P0CC1 without PMCs fitted is as follows:

Level 1/2 (S/X) = 330g

Level 3 (RA) = 400g

Level 4/5 (RC) = 430g

Ordering Information

The order code is specified as **P0CC1-vwxyz**, where **vwxyz** are explained in the following table:

v **(Build Level)**	**w** **(*P2 Routing*)**		**x** **(*reserved*)**		**y** **(*reserved*)**		**z** **(P0 Type)**	
1	0	Standard 5 row I/O†	0		0		A	Type A
2	1	32-bit I/O from each PMC site‡					B	Type B
3								
4								
5								

† PMC1 has 46 pins to rows z and d, PMC2 has 64 pins to rows a and c (see page 3-7).

‡ PMC1 has 46 pins to rows z and d and 32 pins to rows a and c, PMC2 has 32 pins to rows a and c (see page 3-8).

PMC Modules

A range of PMCs are available both from Radstone and third parties. PMCs available from Radstone, in various build standards including Radstone's state-of-the-art rugged conduction-cooled PMCs, include:

- PMCMMA graphics and/or audio accelerator. Levels 1 to 4. 4 or 8 Mbytes graphics RAM and front panel or rear I/O options
- PMC2-9100 graphics accelerator, Levels 1 to 4. 4 Mbytes VRAM. Front panel or rear I/O and analogue or digital video output options
- PMCFDAS FDDI interface, Level 1 only. Dual attach
- PMC1553 MIL-STD-1553B interface, Levels 1 to 4. Front panel or rear I/O, single or dual channel, and RT-only or RT/BC/MT options
- PMX1553 single MIL-STD-1553B channel and 4 channels of serial I/O. RT-only or RT/BC/MT and RS232/RS422 options. Level 4 preferred
- PMCEXT 100BaseTX Fast Ethernet interface, Levels 1 and 2 only
- PMCATMF 155 Mbps ATM adapter for OC-3 fiber networks. Levels 1 to 4
- PMCF1 High capacity FLASH. 32, 64, 96 or 128 Mbytes options. Levels 1 to 5
- PMCF2 Solid state hard disk using 40 Mbyte CompactFLASH. Levels 1 to 5

These products are backed-up by data sheets and manuals giving more information and details on the different options (some of this may also be available via Radstone's web site - see Chapter 1). For more details on any of these or forthcoming products, or for copies of the literature, please contact Radstone directly or your nearest Sales Office.

Note: Level 1 PMCs (both from Radstone and third parties) may be used on all air-cooled versions (Levels 1, 2 and 3) of the P0CC1, even if the PMC does not meet the extended temperature and environmental requirements of Levels 2 and 3. However, the conduction-cooled variant of the P0CC1 can only accept conduction cooled PMCs.

Glossary

ANSI
American National Standards Institute.

ATM
Asynchronous Transfer Mode.

ATR
Air Transportable Racking.

Big-endian
Refers to the way in which multi-byte data is stored in memory. Big-endian data is stored with the *most* significant byte at the lowest address (68XXX style). See also Little-endian.

Byte
An 8-bit data structure.

CMC
Common Mezzanine Card.

DEC
Digital Equipment Corporation. An OEM.

Double-word
A 64-bit data structure.

ECC
Error Correction Code.

EMC
Electro-Magnetic Conduction.

EN
European Norm.

ESD
Electro-Static Discharge.

ESS
Environmental Stress Screening.

FCC
Federal Communications Commission.

FDDI

Fiber Distributed Data Interface. A standard for fiber-optic cable data transmission.

GND

The Ground (0V) signal or supply rail.

Half-word

A 16-bit data structure.

ID

Identity or Identifier.

IEEE

Institute of Electrical and Electronic Engineers.

I/O

Input/Output.

ISA

Industry Standard Architecture.

JTAG

Joint Test Action Group. A standard for board-level testing.

LED

Light Emitting Diode. A semiconductor diode that radiates light. LEDs that emit in the visible region are used as indicators or warnings.

Little-endian

Refers to the way in which multi-byte data is stored in memory. Little-endian data is stored with the *least* significant byte at the lowest address. See also Big-endian**.**

Longword

A 32-bit data structure.

LSB

Least Significant Bit

MSB

Most Significant Bit

MTBF

Mean Time Between Failures.

NC
No Connection or Not Connected.

OEM
Original Equipment Manufacturer.

PCB
Printed Circuit Board.

PCI
Peripheral Component Interconnect.

PMC
PCI Mezzanine Card.

POR
Power On Reset.

RAM
Random Access Memory. Memory that can be read from or written to in any order.

RH
Relative Humidity.

RT/BC/MT
Remote Terminal/Bus Controller/Bus Monitor. The various modes in which a MIL-STD-1553B node can operate.

SBC
Single Board Computer.

TBA
To Be Announced.

U
The U is a standard unit of height measurement (e.g. 3U). One U is 4.445 centimetres (1.75 inches).

UL
Underwriter's Laboratories.

VCC
The 5 Volt supply rail.

VDE
Verband Deutscher Elektrotechniker. The German Safety Regulations specification.

VGA

Video Graphics Array.

VITA

VFEA (VMEbus and Futurebus Extended Architecture) International Trade Association.

VME

Versa Module Europe. Often used as an abbreviation for **VMEbus**.

VMEbus

An ANSI/**VITA** standard (1-1994) for a versatile backplane bus based on the Eurocard mechanical standard.

VRAM

Video RAM.

Word

In PowerPC terminology, a 32-bit data structure. Also often refers to a 16-bit data structure in **VME** systems. See Halfword, Longword.

Write Posting

This is a pipelining technique that can be used by the VME interface chip to increase system performance.

In *Master Write Posting*, when a local bus master writes to the **VMEbus**, instead of requesting and arbitrating for the bus, transferring data to the slave and waiting for the acknowledgement, the VME interface chip acknowledges the local bus master immediately and captures the address and data to write. The local bus master can then continue with its processing while the VME interface chip requests the VMEbus and transfers the data for the host.

Slave Write Posting works in a similar way. Write operations to the VME interface chip as a VME slave do not wait for the chip to become local bus master, write the data to the host memory and wait for its acknowledgement. The VME interface chip acknowledges immediately and captures the address and data to write. Another transfer can then take place on the VMEbus while the VME interface chip writes the data from the previous one.

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