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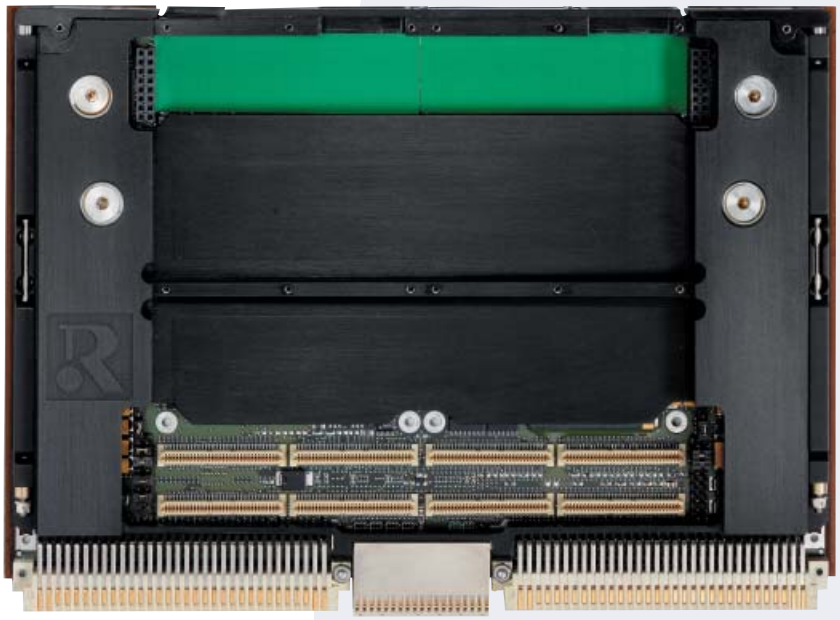
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PPCM1

7457 Dual Processor SBC

XtraPower™
POWER PC PROCESSOR

- **High performance** processing
  - Two 7457 PowerPC processors
- **High performance** architecture
  - Two independent processor nodes
- **High bandwidth** memory
  - Two Discovery's with SDRAM
- **High bandwidth** PMCs
  - Two 64-bit / 66 MHz PMC sites
- **High bandwidth** inter-board data
  - On-board PPzero
- **Full rugged operation**
  - 5 ruggedization levels
- **Full product support**
  - Comprehensive software & services



RADSTONE
DIGITAL PROCESSING

PPCM1, the founding member of Radstone's XtraPower product family, provides dual processing solutions for defense and aerospace applications. Now updated to Freescale 7457 processors, PPCM1 harnesses the processing power of two state-of-the-art Single Board Computers within a single 6U VME slot.

The architecture of PPCM1 loosely couples two fully independent processor nodes across a 64-bit PCI bus, providing the system architect with cost effective, high bandwidth processing units. PPCM1's architecture is also optimized for Real-Time Operating Systems, each node supporting its own entirely standard kernel.

For multi-slot processing solutions, PPCM1 provides an opportunity for reducing system slot count, or for dramatically boosting the processing power within each slot. Each of the processing nodes features a Freescale 7457 processor with 512 KBytes on-chip L2 Cache, its own private L3 Cache and high bandwidth access to its own FLASH and SDRAM, plus non-competing access to its own PMC site via a 64-bit/66 MHz PCI bus.

Features

Processor	2 x MPC7457 PowerPC processors up to 1 GHz and beyond	High performance, low power consumption implementation of 32-bit PowerPC RISC architecture with full 128-bit vector processing using AltiVec technology – ideal for mixed high end computing and signal processing applications SPECInt95 = 43.79 @ 1 GHz, SPECfp95 = 31.61 @ 1 GHz SBC Typical Power Consumption when fitted with 7457 & 256 MBytes SDRAM = 32W
L3 Cache	2 x 2 MBytes	Parity error detection, 64-bit wide at 200 MHz
L2 Cache	2 x 512 KBytes	On-chip running at core frequency
Main Memory bus	2 x 100 MHz	Facilitates high data/instruction bandwidth between processors and main memory
Main Memory	2 x 256 MBytes to 512 MBytes SDRAM with EDC	The CPU is interfaced to the main memory via a 64-bit data bus running at 100 MHz. Up to 512 MBytes SDRAM with EDC supported, 256 MBytes being fitted as standard
FLASH Memory	2 x 64 MBytes FLASH	64 MBytes per processor fitted as standard, split as follows: 55 MBytes User FLASH, 4 MBytes Boot FLASH, 1 MByte reserved for BIT results etc. 4 MBytes BANC (See below)
BANC	Boot Area, Non-Corruptible	Factory write access only. This contains a firmware monitor that can re-boot the board, should all other loaded programs be corrupted
PCI bus to PMC sites	2 x 64-bit 66 MHz	Easy incremental system expansion using air or conduction-cooled single or double width PMCs, accommodates very high bandwidth communication or I/O path or custom function
PCI bus between nodes	64-bit 33 MHz	Provides a high speed inter-node communication path, also using a standard software interface
PPzero on-board	32-bit 33 MHz	Provides a performant inter-board communication path, also using a standard software interface, in addition to VME path
EEPROM	2 x 32 KBytes	Serial
Real-Time Clock	1 sec. resolution	The RTC provides TOD/calendar with 1 sec. resolution
Ethernet	10/100 BASE-T	On CPU0
Serial ports	COM 1,2	COM1 for CPU0, COM2 for CPU1
Timers	8 x 32-bit timer / counters	Configurable as either timer or counter per CPU
Watchdog	2 off	Programmable
DMA engines	8 available	8 DMA controllers are available in the Discovery ISC for efficiently moving large blocks of data
VME	Tundra Universe IIB	64-bit VME, 32-bit 33 MHz PCI bus interface, Integral FIFOs, Programmable DMA controller, 70 MBps burst data transfer
Software	Full Radstone software support	Radstone's Deployed test strategy is fully implemented with a combination of BIT (comprehensive power-up Built-in-Test firmware) and BCS (Background Condition Screening for non-destructive, continuous on-line testing). Also included in Radstone's COTS software support are BSPs (Board Support Packages) and ESPs (Enhanced Support Packages) for WindRiver's VxWorks

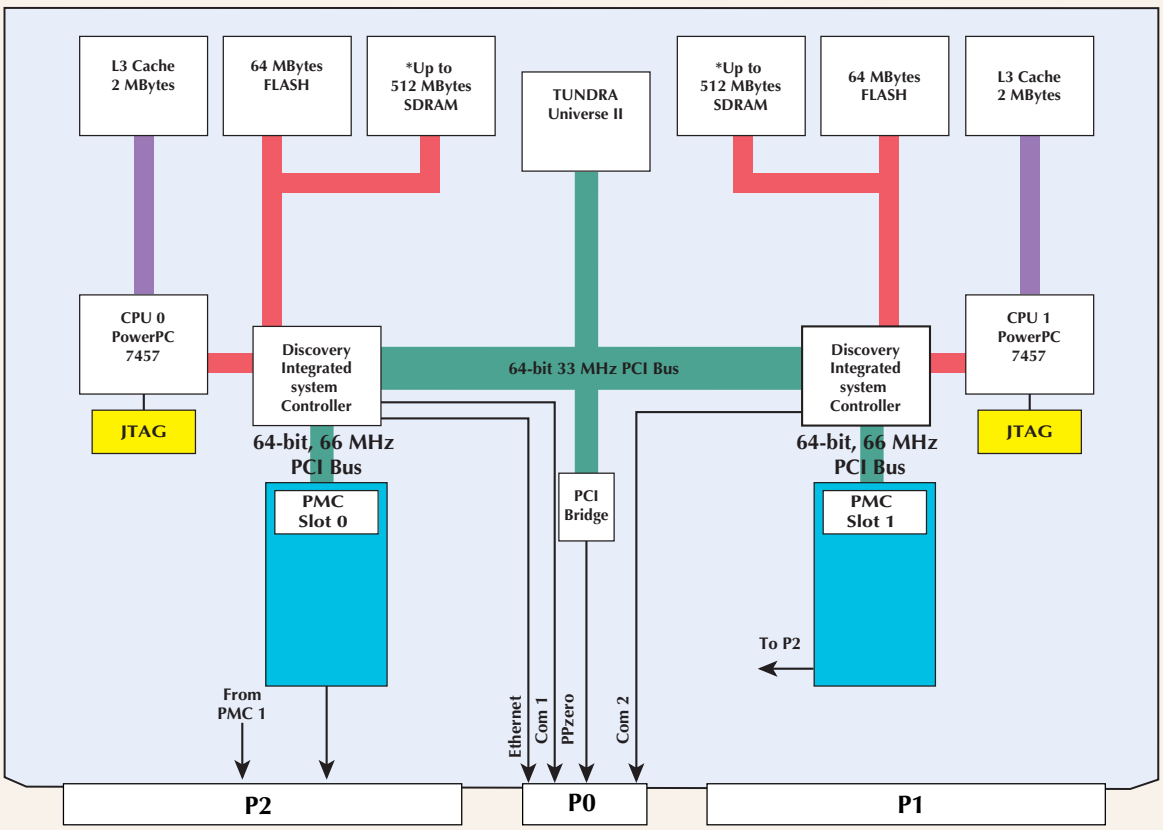


Figure 1: PPCM1 Functional Block Diagram (**256 MBytes SDRAM fitted as standard. 512 MBytes can be fitted as a build option).*

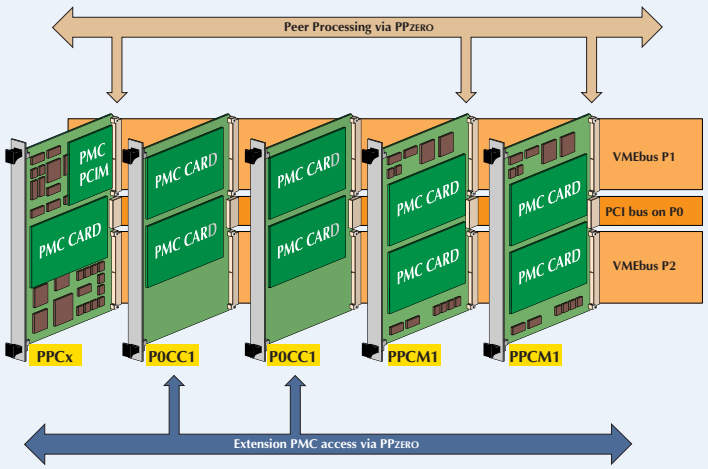
PPzero (PCI over PO)

PPCM1 supports PPzero, a Radstone solution providing for both high bandwidth peer multi-processing and extension PMCs, using a PCI bus routed over standard P0 capable VME backplanes.

Extension PMCs - PPCM1 includes an on-board PCI-PCI bridge which can be used to extend the on-board PCI bus through the P0 connector onto a P0 backplane. The PCI bus can then be picked up by P0CC1 carrier cards, each of which can support 2 PMC cards. Up to 10 PMCs can be supported in this way by a combination of one PPCM1 and four P0CC1s.

Peer multi-processing – the on-board PCI-PCI bridge can also be used to extend the on-board PCI bus to be picked up by further PPCM1s (or any other Radstone PPzero enabled processor boards), facilitating multi-processing over PCI for maximum system flexibility.

See the PPzero/P0CC1 data sheets for more details.



- High bandwidth access to peer processing across PCI on a P0 backplane
  - Supported on-board by PPCM1 (and by PPzero adapter cards on any Radstone PowerX board)
  - Genuine Multi-processing, peers see the others main memory
  - Standard O/S backplane driver model supported for VxWorks
- Access to up to 10 standard PMC cards within 5 VME slots
- Easy system expansion at low incremental cost

Figure 2: PPzero Diagram

Input/Output

PPCM1 is designed to provide high density rear I/O utilizing 5 row VME64 connectors. The Rear I/O tracking is matched for compatibility with all Radstone's high data rate PMCs such as Fibre Channel and Graphics. Additional matched tracking is also provided to take Fibre Channel output from PMC1 to the center rows of the P0 connector. Type B 95 way P0 connectors are offered as standard.

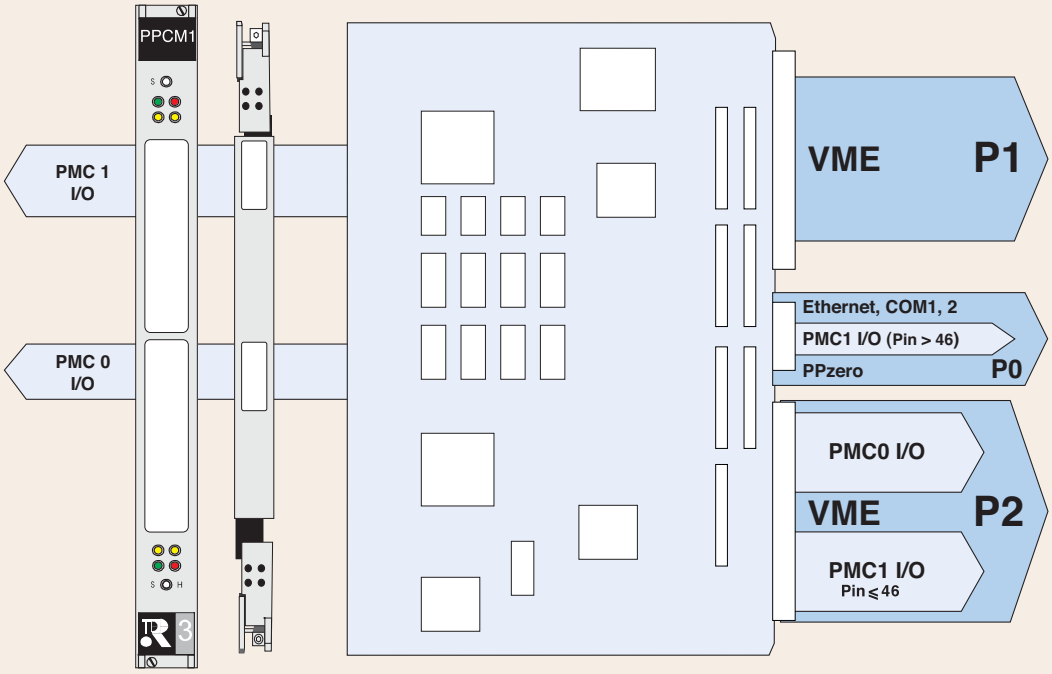


Figure 3: PPCM1 I/O Diagram

Ruggedization Levels

PPCM1 is available in Radstone's 5 environmental ruggedization levels (see Table 1). Air- cooled variants are designed to be used in standard industrial VME chassis. Conduction-cooled builds are for use in Radstone or third-party ATR style enclosures.

Radstone uses advanced thermal and mechanical design in the printed circuit board, metal work and assembly process in order to build in the required levels of ruggedness. Ruggedization Level 2 and higher circuit card assemblies include Conformal Coating as standard.

Ruggedization Level	**1**	**2**	**3**	**4**	**5**
Cooling Method	Convection			Conduction	
Conformal Coat	Optional	Standard	Standard	Standard	
Low Pressure Operationial	15,000 Ft	15,000 Ft	15,000 Ft	70,000 Ft	
Low Pressure Storage	50,000 Ft	50,000 Ft	50,000 Ft	70,000 Ft	
Rapid Decompression	-	-	0-50,000 Ft	0-70,000 Ft	
High Temp Operationial	55°C@ 300Ft/min	65°C@ 300Ft/min	75°C@ 300Ft/min	75°C	85°C
				At card edge	
Low Temp Operationial	0°C	-20°C	-40°C	-40°C	
High Temp Storage	85°C	85°C	100°C	100°C	
Low Temp Storage	-40°C	-40°C	-50°C	-50°C	
Temperature Shock	10°C/min over Ts	10°C/min over Ts	10°C/min over Ts	10°C/min over Ts	
Humidity	95% non-condensing	95% 10 cycles 240hrs	95% 10 cycles 240hrs	95% 10 cycles 240hrs	
Salt Fog	-	-	5% Salt 48 Hrs	5% Salt 48 Hrs	
Acceleration	13.5g	13.5g	13.5g	13.5g	
Vibration Sine	10-500Hz 2g	10-500Hz 2g	5-2000Hz 5g	5-2000Hz 5g	
Vibration Random	0.002g^2H^z from 10-2000H^z	0.002g^2H^z from 10-2000H^z	0.04g^2/Hz with a flat response to 1000Hz. 6dB/Oct roll off from 1000-2000Hz	0.1g^2/Hz with a flat response to 1000Hz. 6dB/Oct roll off from 1000-2000Hz	
Shock	20g PEAK Sawtooth 11mSec duration	20g PEAK Sawtooth 11mSec duration	20g PEAK Sawtooth 11mSec duration bench handling	20g PEAK Sawtooth 11mSec duration bench handling	

Table 1: Ruggedization Levels Table

Software Model

PPCM1 is optimized for running real-time applications based upon non-SMP embedded Operating Systems such as VxWorks. As each PPCM1 processing cell (node) is hardware independent, a fully standard BSP and kernel based upon a normal, single-processor memory map can be ported to each. Non-standard porting arrangements, typically needed to fit such O/Ss onto an SMP style board, are eliminated by the exceptional design of the PPCM1.

There are further advantages to PPCM1 architecture. Increased memory performance has been mentioned above, but this is particularly relevant to real-time. Large, complex real-time applications can be subject to high context switch rates, which on average result in a greater reliance upon code in memory rather than in cache. Typical 'linear', non real-time applications do not suffer so much from this. On PPCM1, processors do not compete for memory through the same bridge, so maximum possible performance is maintained, despite the imposition of real-time context switching. On SMP architecture boards memory competition in the single bridge chip can degrade performance in this type of situation.

Standard Task Partitioning – Standard Inter-Node Communications

Arrays of PPCM1s can be built up very simply to scale the required processing power to application needs. VxWorks tasks are partitioned across multiple nodes exactly as though each node were an independent board. Communication between nodes and between multiple PPCM1 boards is accomplished in an identical manner, and complies to industry standard VxWorks methodology.

Peripheral functions added via use of PMCs are supported by entirely standard VxWorks drivers, PPCM1 architecture does not impose any special memory-map or interrupt needs. Hence PPCM1 is ideally suited to immediate use for standard, embedded applications on VxWorks, requiring multiple generic processing elements, or (utilizing the AltiVec processor capabilities), those applications requiring mixed generic processing and DSP activity.

Many third-party packages, e.g. those to support AltiVec math's algorithms, are available for VxWorks, and these will run on PPCM1. Any hardware dependencies are supplied by the Radstone BSP.

Control Communication and Bulk Data Transfer

The provision of a standard VxWorks backplane interface on VME and PPzero, allows all legacy code to operate unchanged on PPCM1. This includes any use of the WindRiver layered multi-processor options like VxMP or VxFusion. However, because the WindRiver backplane protocol uses a TCP/IP stack, splitting all traffic down to highly manipulated/verified packets at its lowest level of communication, it has inherently very limited performance. This limit applies to all layered products such as those quoted above that sit above the backplane protocol. Radstone's recommendation is to use the backplane protocol for all control and co-ordination messages, plus legacy/layered code, where performance is not an issue, but to use raw DMA for bulk data transfers where speed is important. We supply a PCI DMA engine for inter-node and also inter-board traffic on PPzero, and a VME DMA engine too, in our ESP package. The two engines share a common interface and allow transfers to proceed at the full rate defined by bus hardware.

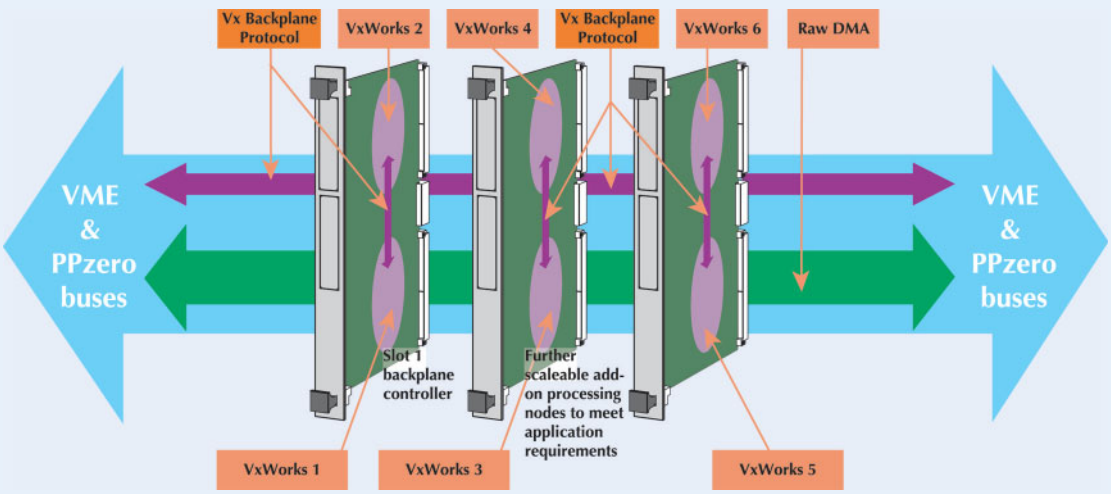


Figure 4: PPCM1 Software Models

Legacy Upgrades

PPCM1 is very well suited to the replacement of older, single-processor SBCs in legacy multi-processing systems. This technology insertion can reduce the slot count, increase performance, or both. Figure 5 below depicts a typical system constructed from three single processor SBCs. A VxWorks kernel sits on each board and they all communicate across the VMEbus via the VxWorks backplane protocol.

A replacement system is shown in Figure 6. In addition to what would be a typical processing power upgrade (to use the latest frequency and style of processors), two of the SBCs have been compacted into one unit. Processing power has been increased, the slot-count reduced, cost significantly reduced, but the software model remains exactly the same!

In this case a single processor 'workstation' board (such as one from Radstone's PowerX range) has been maintained in slot one, as typically one board in the system is often required to run a variety of interfaces, such as SCSI or keyboard/mouse, or other control/MMI functions, and these may also require unchanged backplane connections. However the other SBCs not using these peripheral interfaces, and typically present for just processing power and memory capacity, are both replaced by PPCM1.

The distribution of the application tasks across processing nodes, and the communication method, both remain exactly the same as in the original system. No re-arrangement of these is required. In the upgraded system the backplane protocol may still be run over true VME, or can be configured across PPzero, i.e. PCI over the VME backplane on P0. This leaves the VMEbus free for transfers to legacy equipment, which can improve overall throughput, but also determines if slower equipment attached to this bus might impose latency delays on inter-processor traffic. Raw DMA for bulk data transfers can be accomplished over VME or PPzero.

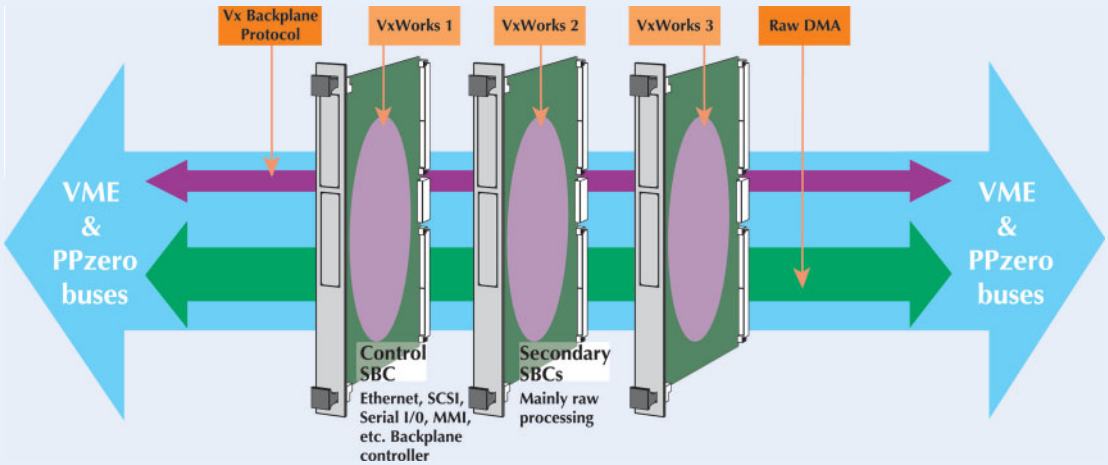


Figure 5: Legacy Multi-processor implementation

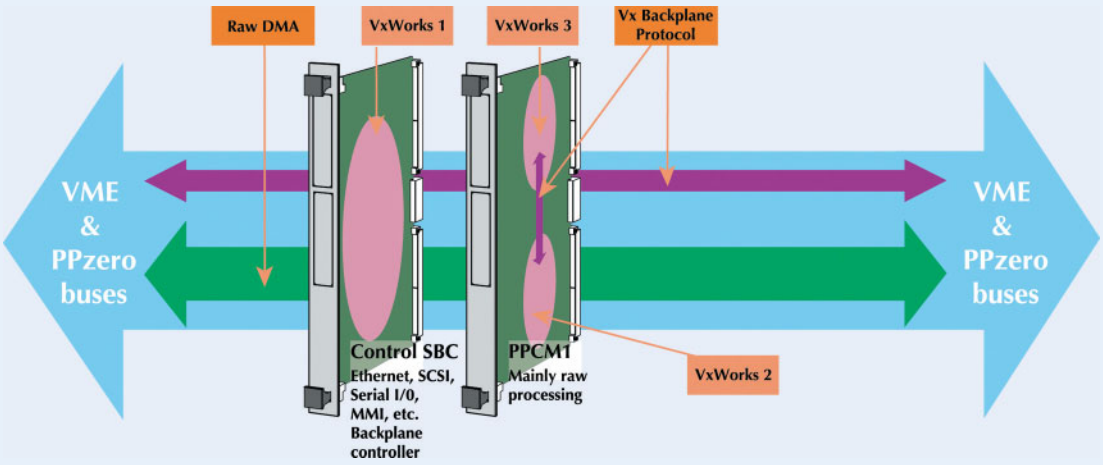


Figure 6: Multi-processor implementation with PPCM1

Standard Ordering Information

Sales Code	Description
	Dual 1 GHz PowerPC 7457 – 256 MBytes SDRAM per processor
PPCM1-7457-1E20DBx	Dual 1 GHz PowerPC 7457 6U VME SBC, level 1; 256 MBytes SDRAM per processor, 2 MBytes L3 Cache per processor, 64 MBytes FLASH per processor, 10/100 BASE-T, PPzero Interface, 2 PMC slots, 5 Row P1 & P2, Type B P0
PPCM1-7457-2E20DBx	Air-cooled level 2 as above with conformal coating
PPCM1-7457-3E20DBx	Air-cooled level 3 as above with conformal coating
PPCM1-7457-4E20DBx	Conduction-cooled level 4 as above
PPCM1-7457-5E20DBx	Conduction-cooled level 5 as above

x=software option

NOTE: The standard ordering information (above) defines the standard build variant. Consult your local Radstone sales office for availability of further build options.

RADSTONE
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USA
Telephone: +1 (800) 368-2738
E-mail: sales@radstone.com

EUROPE
Telephone: +44 (0) 1327 359444
E-mail: sales@radstone.co.uk

Visit www.radstone.com for a full list of regional offices and contact details

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