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Appendix A - PPCM1

This appendix contains hardware information for PPCM1 boards - rev 5 and upward. The information contained in this document must be used in conjunction with the XtraPower Family Product Manual.

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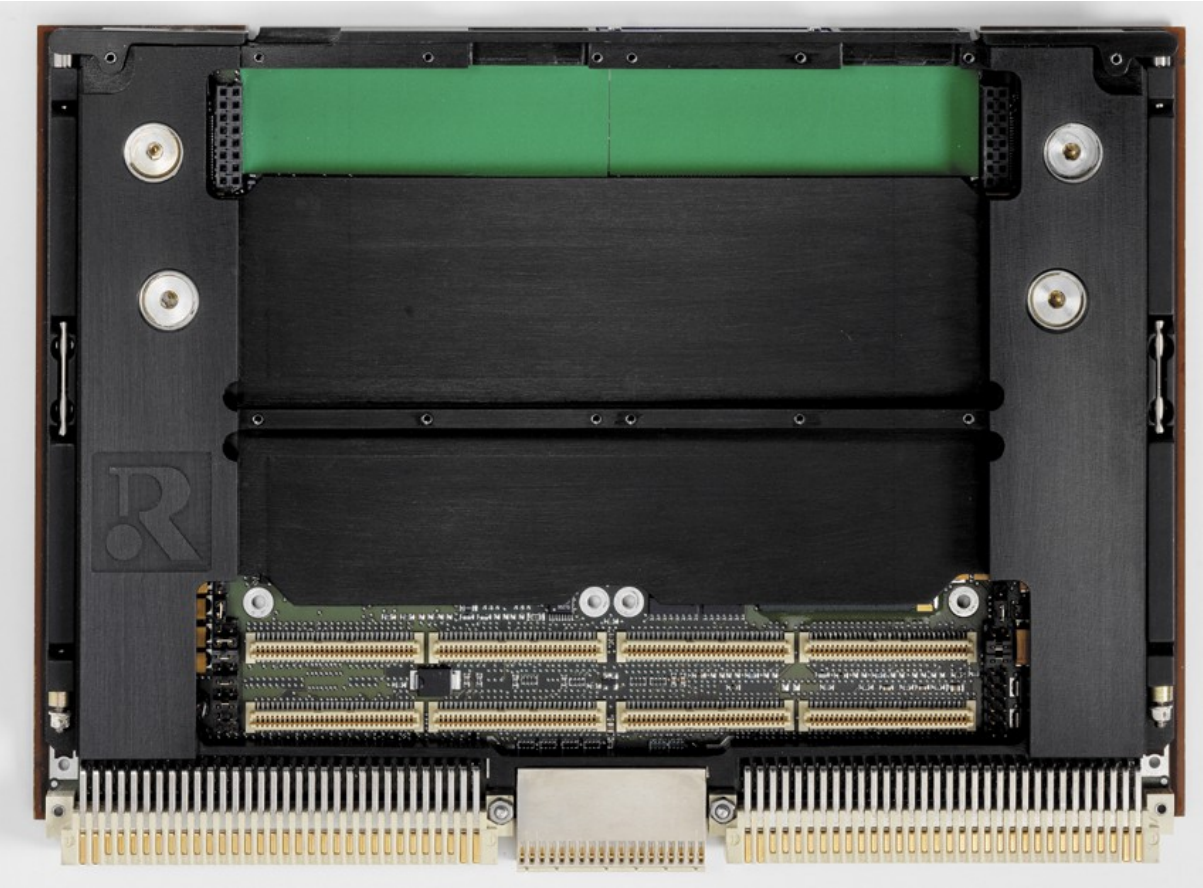
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Overview

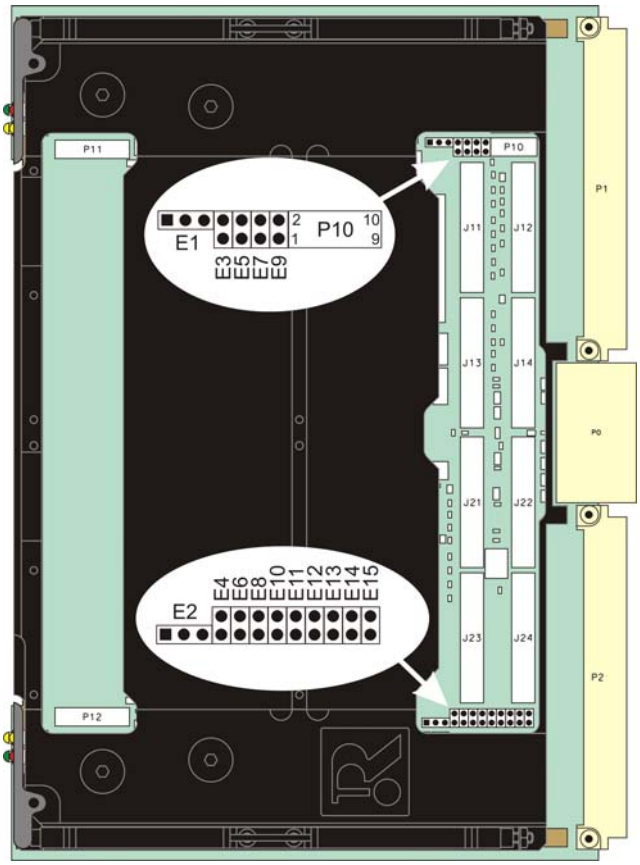
The PPCM1 features two fully independent processor nodes loosely coupled across a 64-bit PCI bus. Each of the processing nodes features a Motorola PowerPC 7410 processor, supported by its own local memory resources - private L2 cache, FLASH and SDRAM, and a PCI bridge. Each node has non-competing access to its own IEEE P1386.1 PMC site via a 64-bit/66 MHz PCI bus, and can access the other node's PMC site if required.

Figure A-1. View of Conduction-Cooled PPCM1



Configuration

Link Positions



Notes:

Boards are delivered with push-on jumper links, but for rugged or military applications, it is recommended that wire wraps be used to connect the posts.

This document refers to link settings as In or Out, meanings are as follows:

In = jumper fitted -

Out = jumper not fitted -

Before changing any of these link options, refer to the appropriate section(s) in the following pages.

Pin one of link blocks is shown by a square pad in the diagram alongside.

CAUTION

Links E1, E2 and E13 must be correctly configured before operation

CAUTIONS

If your PPCM1 has no PMCs fitted, E1 and E2 can be linked either for 3.3V (pin 1 to pin 2), or 5V (pin 2 to pin 3) signaling, but you must fit the links one way or the other; not fitting links may cause damage to the PPCM1.

If PMCs are fitted, incorrect linking of E1 or E2 may cause damage to the PMCs or the PPCM1.

If there is no PPzero backplane fitted in your system, E13 must be fitted.

If your PPCM1 is fitted in the leftmost slot of a PPzero backplane, E13 must be fitted.

If your PPCM1 is fitted in any other slot of a PPzero backplane, E13 must not be fitted and a PPzero Master must be fitted to the leftmost slot of the PPzero backplane.

Delivered Link Settings

The PPCM1 is delivered with no links fitted.

PMC1 Signalling Voltage Selection Link (E1) and PMC0 Signalling Voltage Selection Link (E2)

These 3-pin links select the VIO (signalling) voltage on the PCI bus to the corresponding PMC site, as follows:

SETTING	MEANING
Out	Not a valid setting
Pin 2 to pin 1	3.3V signaling
Pin 2 to pin 3	5V signaling
Pin 1 to pin 3	Not a valid setting

CAUTION

If your PPCM1 has no PMCs fitted, E1 and E2 can be linked either pin 1 to pin 2 or pin 2 to pin 3, but you must fit the links one way or the other; not fitting links may cause damage to the PPCM1.

If PMCs are fitted, incorrect linking of E1 or E2 may cause damage to the PMCs or the PPCM1.

CPU1 FLASH Swap Link (E3) and CPU0 FLASH Swap Link (E4)

If the processor is booting from FLASH (see the CPU1 Bootmode Link (E9) or CPU0 Bootmode Link (E10) description), it uses address 0xFFF0 0000. These links determine whether this corresponds to the BANC or the Boot area of FLASH, as follows:

SETTING	MEANING
Out	Boot FLASH at 0xFFF0 0000
In	BANC FLASH at 0xFFF0 0000

CPU1 User FLASH Write Enable Link (E5), CPU0 User FLASH Write Enable Link (E6), CPU1 Boot FLASH Write Enable Link (E7) and CPU0 Boot FLASH Write Enable Link (E8)

These links enable or disable writes to the appropriate areas of FLASH for the appropriate processor, as follows:

SETTING	MEANING
In	FLASH writes to appropriate area/processor enabled
Out	FLASH writes to appropriate area/processor disabled

The Global FLASH Write Enable link (E11) also needs to be fitted before these FLASH areas can be written to.

CPU1 Bootmode Link (E9) and CPU0 Bootmode Link (E10)

Link E9 determines whether CPU1 boots normally from FLASH or is held in reset, as follows:

SETTING	MEANING
Out	CPU1 boots from FLASH
In	CPU1 held in reset†

† In this mode, CPU1 is actually configured to boot from VME, but is held in reset after configuration until instructed to proceed by CPU0 or another processor, allowing "Master-Slave" type operation. See the CPU-PCI Bridge and Memory Controller section for more details.

Link E10 determines whether CPU0 boots from FLASH or over the VMEbus, as follows:

SETTING	MEANING
Out	CPU0 boots from FLASH
In	CPU0 boots over VME (see also link E12)

Global FLASH Write Enable Link (E11)

This link must be fitted (or the P0 FLPRGEN~ signal pulled low) to enable writes to any areas of FLASH except the Scratch area.

SETTING	MEANING
Out	FLASH writes globally disabled
In	FLASH writes globally enabled

Universe II Register VME Access Link (E12)

This link determines whether the Universe II registers can be accessed over the VMEbus (at 0x8000 0000 in A32 space or 0x80 0000 in A24 space), as follows:

SETTING	MEANING
Out	No VME access to Universe II registers
In	Universe II registers can be accessed over VME

Fitting this link (E12) and the CPU0 Bootmode link (E10) allows an external processor to access the PPCM1's Universe II registers via the VMEbus and so alter some of the PPCM1's internal settings. In this mode, CPU0 is held in reset until an LINT7 interrupt from the Universe II is generated, giving the external processor time to change the configuration. Once the external processor has carried out any required reconfiguration, it can generate the LINT7 trigger from the Universe II, and CPU0 will then boot over the VMEbus.

Note: Before the on-board firmware configures the Universe VME interface, the Universe II registers are at the same address on every PPCM1, so only one PPCM1 in a system should be configured for CPU0 controlled VME boot mode (i.e. links E10 and E12 fitted).

PPzero Master/Slave Link (E13)

On boards with no PPzero option, this link is not used. On boards with the PPzero option, this link determines whether the PPCM1 is PPzero interface master or slave, as follows:

SETTING	MEANING
In	PPzero master
Out	PPzero slave

CAUTION

If there is no PPzero backplane fitted in your system, E13 must be fitted.

If your PPCM1 is fitted in the leftmost slot of a PPzero backplane, E13 must be fitted.

If your PPCM1 is fitted in any other slot of a PPzero backplane, E13 must not be fitted and a PPzero Master must be fitted to the leftmost slot of the PPzero backplane.

P3V3PCI Monitor Link (E14)

Although the PCI +3.3V voltage is not used internally, it may be a system supply voltage on the P0 and P1 connectors. The level of the +3.3V voltage rail can optionally be monitored by power-up circuitry such that the PPCM1 is held in reset until this rail reaches a suitable level. This prevents the PPCM1 attempting to access devices that may be connected to this power rail before the rail is operational. If no power supply is connected to this rail, configure the PPCM1 not to monitor it.

SETTING	MEANING
Out	PPCM1 does not wait for PCI +3.3V
In	PPCM1 waits for PCI +3.3V

Test Link (E15)

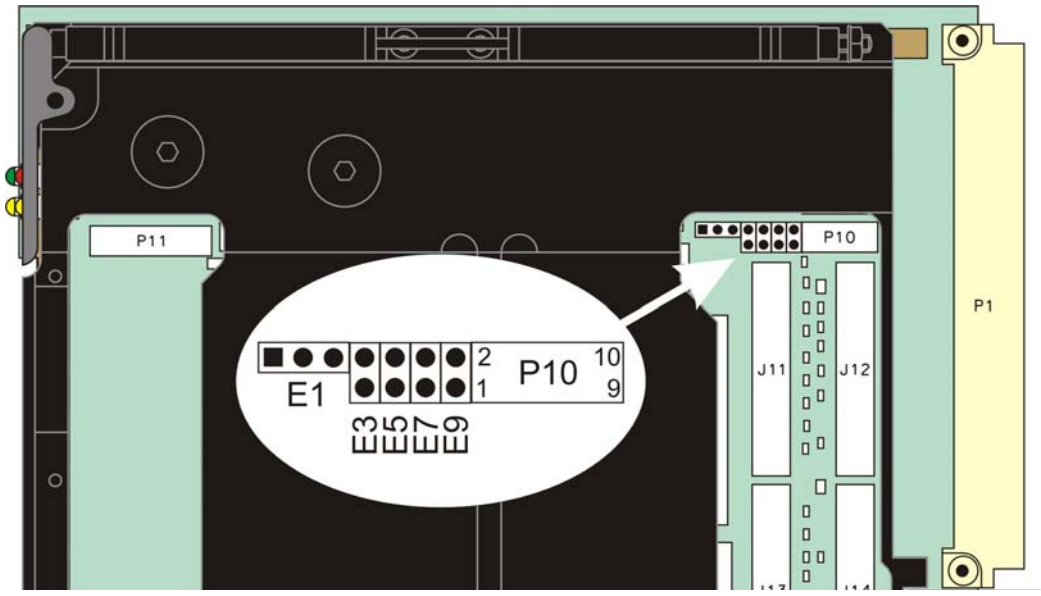
This is a factory test/upgrade link. Do not alter the default setting (out) in normal use.

Note: Only use this link as and when instructed.

Board ID (P10)

The pins on P10 form a 5-bit board ID that may be read from the PLD register. The pins are decoded as follows:

Board ID	Pin 9 to Pin 10	Pin 7 to Pin 8	Pin 5 to Pin 6	Pin 3 to Pin 4	Pin 1 to Pin 2
0	VCC/Out	GND/In	GND/In	GND/In	GND/In
1	VCC/Out	GND/In	GND/In	GND/In	VCC/Out
2	VCC/Out	GND/In	GND/In	VCC/Out	GND/In
3	VCC/Out	GND/In	GND/In	VCC/Out	VCC/Out
4	VCC/Out	GND/In	VCC/Out	GND/In	GND/In
5	VCC/Out	GND/In	VCC/Out	GND/In	VCC/Out
6	VCC/Out	GND/In	VCC/Out	VCC/Out	GND/In
7	VCC/Out	GND/In	VCC/Out	VCC/Out	VCC/Out
8	VCC/Out	VCC/Out	GND/In	GND/In	GND/In
9	VCC/Out	VCC/Out	GND/In	GND/In	VCC/Out
10	VCC/Out	VCC/Out	GND/In	VCC/Out	GND/In
11	VCC/Out	VCC/Out	GND/In	VCC/Out	VCC/Out
12	VCC/Out	VCC/Out	VCC/Out	GND/In	GND/In
13	VCC/Out	VCC/Out	VCC/Out	GND/In	VCC/Out
14	VCC/Out	VCC/Out	VCC/Out	VCC/Out	GND/In
15 (default)	VCC/Out	VCC/Out	VCC/Out	VCC/Out	VCC/Out
16	GND/In	VCC/Out	GND/In	VCC/Out	GND/In
17	GND/In	VCC/Out	GND/In	VCC/Out	VCC/Out
18	GND/In	VCC/Out	VCC/Out	GND/In	GND/In
19	GND/In	VCC/Out	VCC/Out	GND/In	VCC/Out
20	GND/In	VCC/Out	VCC/Out	VCC/Out	GND/In
21	GND/In	VCC/Out	VCC/Out	VCC/Out	VCC/Out



Geographical Addressing/VME Slave Address Configuration

Chassis with VME64x-compliant backplanes provide Geographical Addressing facilities, i.e. the backplane slot position provides the board ID, as shown in the following table:

Slot	Slot 1 Functions	Board ID	A32 Address	A24 Address
1	Yes	0	0x0000 0000	0x00 0000
2	No	1	0x1000 0000	0x40 0000
3	No	2	0x2000 0000	0x80 0000
4	No	3	0x3000 0000	0xC0 0000
5	No	4	0x4000 0000	None
6	No	5	0x5000 0000	None
7	No	6	0x6000 0000	None
8	No	7	0x7000 0000	None
9	No	8	0x8000 0000	None
10	No	9	0x9000 0000	None
11	No	A	0xA000 0000	None
12	No	B	0xB000 0000	None
13	No	C	0xC000 0000	None
14	No	D	0xD000 0000	None
15	No	E	0xE000 0000	None
16	No	F	0xF000 0000	None

P10 is connected to the VME64x geographical addressing signals on P1 row D (see the P1 connector description) as follows:

P10 Pin	Signal	P10 Pin	Signal
1	GND	2	GA0~
3	GND	4	GA1~
5	GND	6	GA2~
7	GND	8	GA3~
9	GND	10	GA4~

If you wish to read the status of the P1 Geographical Address signals, do not fit links across the corresponding P10 pins.

The board ID also sets the board's VME slave addresses, as shown in the above table, so take care to avoid an address clash with other boards in the system. This is set up by software and so is only applicable once the system is 'operational'.

Suggested Configuration

Although the default link configuration is for no links to be fitted, the options selected may not suit your system, and you will need to fit links to configure your PPCM1 before plugging it into your system. The following suggested link settings are suitable in many cases:

LINK	SETTING	ACTION
E1	Pin 2 to pin 3	PMC1 VIO = +5V
E2	Pin 2 to pin 3	PMC0 VIO = +5V
E3	Out	CPU1 boots from Boot FLASH area
E4	Out	CPU0 boots from Boot FLASH area
E5	Out	User FLASH write disabled for CPU1
E6	Out	User FLASH write disabled for CPU0
E7	Out	Boot FLASH write disabled for CPU1
E8	Out	Boot FLASH write disabled for CPU0
E9	Out	CPU1 boots from FLASH
E10	Out	CPU0 boots from FLASH
E11	Out	Global FLASH writes disabled
E12	Out	No VME access to Universe II registers
E13	In	PPCM1 is PPzero master
E14	Out	PPCM1 does not wait for PCI +3.3V
E15	Out	Test (do not alter)
P10	1-2, 3-4, 5-6, 7-8	Board ID = 0 (System Controller)

CAUTIONS

If your PPCM1 has no PMCs fitted, E1 and E2 may be linked either pin 1 to pin 2, or pin 2 to pin 3, but you must fit the links one way or the other; not fitting links may cause damage to the board.

If PMCs are fitted, incorrect linking of E1 or E2 may cause damage to the PMCs or the If there is no PPzero backplane fitted in your system, E13 must be fitted.

If your PPCM1 is fitted in the leftmost slot of a PPzero backplane, E13 must be fitted.

If your PPCM1 is fitted in any other slot of a PPzero backplane, E13 must not be fitted and a PPzero Master must be fitted to the leftmost slot of the PPzero backplane.PPCM1.

Power to the Real Time Clock on the PPCM1 is fed from +5VSTDBY and +5V on the VMEbus. Whichever of these two supplies has the greater voltage provides the supply in normal operation (i.e. current may be drawn from the +5VSTDBY line even when +5V is powered). The supply is provided by +5VSTDBY when the +5V supply is not present. VME compliance requires the +5VSTDBY supply to be 5V +5% -2.5%, however the PPCM1 can operate with a standby voltage in the range 2.5 to 5.25V. This allows the standby voltage to be supplied by a battery, although in this case it is a safety requirement of the user to make sure that that battery cannot be charged from the +5VSTDBY rail. If operation of the Real Time Clock is not required when the main supplies are powered down, no connection is required on +5VSTDY.

VMEbus Interface Configuration

Several operating features of the Universe VME interface are set at power-up or reset by surface mount jumper links. All of these, except local register access, may be overridden by software. The default settings are:

Operating Feature	Setting
Register access slave image from VMEbus:	Enabled in A32 space at 0x8000 0000 or 0x80 0000 in A24 space, depending on link E12
VME CR/CSR slave image:	Disabled
PCI slave image 0:	Enabled in PCI memory space at 0xF000 0000 to 0xFFFF FFFF
Local register access:	PCI I/O space
Auto-ID scheme:	Disabled

Changing the default power-up options requires surface-mount rework tools and would normally only be done at the factory. Further details are available from technical support at Radstone.

Functional Description

Booting

Configuration is independent between the two CPUs, e.g. CPU0 could boot from VME while CPU1 boots from FLASH.

Note: If both CPUs are configured to boot over VME, they will both boot from the same image on VME (at address 0xFFF0 0000).

CPU0

Link E10 determines whether CPU0 boots from FLASH (link out) or over the VMEbus (link fitted). The default is CPU0 boots from FLASH.

CPU0 boots from FLASH at 0xFFF0 0000. Link E4 determines whether this corresponds to the Boot (link out) or the BANC (link fitted) area of FLASH. The default is CPU0 boots from the Boot area.

When booting over the VMEbus, CPU0 can be configured, using link E12, either to boot immediately (link out) or be held in reset until an LINT7 interrupt from the Universe II is generated (link fitted). This option allows an external processor to access the PPCM1's Universe II registers via the VMEbus (at 0x80000 000 in A32 space or 0x80 0000 in A24 space) and so alter some of the PPCM1's internal settings. Once the external processor has carried out any required reconfiguration, it can generate the LINT7 trigger from the Universe II, and CPU0 then boots over the VMEbus.

Note: Before the on-board firmware configures the Universe VME interface, the Universe II registers are at the same address on every PPCM1, so only one PPCM1 in a system should be configured for CPU0 controlled VME boot mode (i.e. links E10 and E12 fitted).

CPU1

Link E9 determines whether CPU1 is configured to boot from FLASH (link out) or over VME (but held in reset [link fitted]). The default is CPU1 boots from FLASH.

CPU1 boots from FLASH at 0xFFF0 0000. Link E3 determines whether this corresponds to the Boot (link out) or the BANC (link fitted) area of FLASH. The default is CPU1 boots from the Boot area.

When booting over the VMEbus, CPU1 always operates in a controlled boot manner. CPU1 is held in reset until released using MPP31 on Disco1. Taking this line low releases CPU1 from reset. This allows either CPU0 or an external processor to carry out other configuration before CPU1 is booted.

Resets

The CPU0 reset switch (below the PMC0 slot) on the front panel generates a hard reset to the whole board when moved to the “H” position, or generates a soft reset to CPU0 when moved to the “S” position. The CPU0 reset switch is only fitted on build levels 1 to 3.

The CPU1 reset switch (above the PMC1 slot) on the front panel generates a soft reset to CPU1 when moved to the “S” position. It has no hard reset capability; moving the switch to the other position has no effect. The CPU1 reset switch is only fitted on build levels 1 to 3.

There are two types of reset that may be applied to the PPCM1: ‘Hard’ and ‘Soft’.

Hard Reset

This causes the CPU to begin executing code from address 0xFFF0 0000 in FLASH. By fitting a hardware jumper (E10 for CPU0, E9 for CPU1), the CPU can execute code from a VME source instead.

The following table summarises events that may cause a hard reset:

Source		Action	SYSRESET~ Generation
Hardware Events	Power-on	Hard reset all devices	Yes
	Received SYSRESET~		No
	Watchdog time-out		If System Controller
	Front-panel hard reset (build levels 1 to 3)		
Hardware Events	P0 hard reset signal (EXTRESET†)	Hard reset all devices	If System Controller
	P2 hard reset signal (EXTRESET†)		
Software Events	SW_LRST bit	Hard reset excluding VMEbus interface	No
	VCSR bit		
	SW_SYSRESET bit	Hard reset if System Controller	If System Controller

† External availability depends on the pinout option selected.

The SW_LRST, VCSR and SW_SYSRESET bits are located in the Universe II control registers. Another VME master may use these to reset the PPCM1

There is one watchdog per CPU. The watchdog timer has a software selectable period and can generate an interrupt close to expiry of the timer to warn the processor that the timer needs retriggering. Expiry of either watchdog timer provides a hard reset to the whole of the PPCM1, and potentially the rest of the system depending on whether the board is the VME System Controller or PPzero Master.

The front panel hard reset may be disabled under software control (bit D24 of the CPU0 PLD Register; there is no hard reset capability for CPU1).

Note: Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled. Similarly, integrity of FLASH or EEPROM data cannot be guaranteed if a hard reset occurs during a FLASH or EEPROM write cycle, respectively.

Soft Reset

This causes the CPU to reach a recoverable state and then branch to either 0x0000 0100 or 0xFFF0 0100, depending on the state of the IP bit in the processor's Machine State Register.

The following table summarises events that may cause a soft reset:

SOURCE	
Hardware Events	Front-panel soft reset (build levels 1 to 3)
	P0 soft reset signal (EXTABORT0, EXTABORT1)†
	P2 soft reset signal (EXTABORT0, EXTABORT1)†

† External availability depends on the pinout option selected.

The front panel soft reset switch may be disabled under software control (bit D24 of the appropriate PLD Register for the CPU).

Soft reset is falling-edge triggered.

Architecture

Notes:

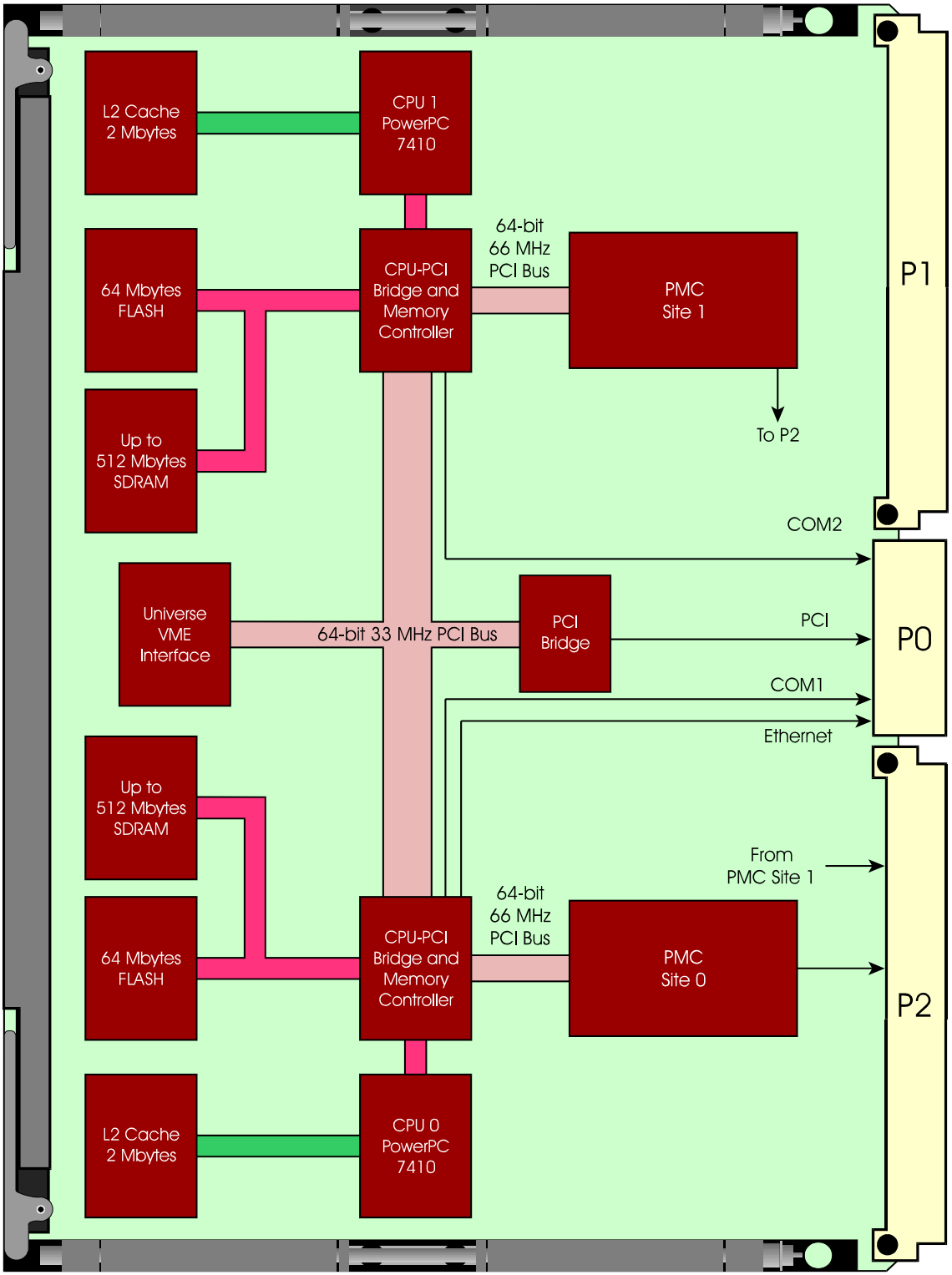
1) Due to the increasingly short lifetimes of system components, the I/O devices used on the PPCM1 are not guaranteed to remain fixed in the future.

2) Hardware should be accessed only through mechanisms provided by the Operating System's "Hardware Independence" mechanism (BSP, HAL, residual data, etc.), and not directly by application software.

3) If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimise direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.

4) Radstone supported Operating Systems guarantee compatibility at the application level through the Hardware Independence mechanisms mentioned above.

Figure A-2. Block Diagram



Memory

Level 2 Cache

The PPCM1 provides 2 Mbytes of L2 cache per processor, connected to a private L2 cache bus. Full snooping is supported.

User EEPROM

The PPCM1 has 32 Kbytes of User EEPROM per processor, provided by 24LC256 devices. The User EEPROM is always readable, but writes are protected by bit D22 of the appropriate PLD Register for the CPU, as follows:

D22: User EEPROM Write Enable.
0 = Writes enabled.
1 = Writes disabled (default at power-up).

Configuration EEPROM

The PPCM1 has two 32 Kbyte Configuration EEPROMs per processor, provided by 24LC256 devices. For each processor:

- The lower part of the EEPROM contains Discovery hardware configuration data
  - One device holds the data for FLASH boot
  - The other device holds the data for VME boot
- The upper part of the EEPROM contains board description data

The appropriate FLASH or VME boot device is selected by the address put out on the I^2C bus.

Both areas in each EEPROM are always readable, but writes are protected by bit D23 of the appropriate PLD Register for the CPU, as follows:

D23: Configuration EEPROM Write Enable.
0 = Writes enabled.
1 = Writes disabled (default at power-up).

An appropriate link must be fitted before bit D23 of the PLD register can be set to 0.

System RAM (SDRAM)

Up to 512 Mbytes of SDRAM with EDC per processor (up to 1 Gbyte total) can be fitted directly to the PPCM1. 256 Mbytes per processor are fitted by default (512 Mbytes total).

FLASH

64 Mbytes of FLASH per processor (128 Mbytes total) are fitted directly to the PPCM1. The FLASH is organised as 4 devices, each 8 bits wide to make up the 32-bit device bus. Writes are only allowed to the full 32-bit width.

The FLASH is burst mode capable, however, this depends on whether the area is cacheable, and so is not applicable to writes, due to the register mechanism. Care should also be taken, as reprogramming the Boot area at 0xExxx xxxx will affect caching at 0xFFCx xxxx.

For each processor, the FLASH is divided into the following areas:

- User (55 Mbytes)
- Boot (4 Mbytes)
- BANC (Boot Area Non-Configurable) - a non-alterable copy of the boot code (4 Mbytes)
- Scratch - a non write-protected area to which e.g. BIT fail data can be written while the User area remains write protected. This area also provides an address range where FLASH device Identify commands (which require write operations, and the write signal is used as a write protect mechanism for the FLASH) can be carried out (1 Mbyte)

Writing to the FLASH (User and Boot areas only, as explained above) is a 2-stage process:

1) Links must be fitted appropriately to enable writes to the Write Enable bits in the PLD Register for the required CPU.
2) The PLD Register Write Enable bits must then be set appropriately to enable writes to the required area of FLASH.

Links E5 to E8 and E11 control the writes to the PLD Registers for CPU0 and CPU1. Firstly, the global FLASH write enable link E11 must be inserted. This controls writes to all areas of FLASH except the Scratch area and is out by default. Alternatively, the FLPRGEN~ signal on the P0 connector can be pulled low, which has the same effect. The state of this link/signal is reflected in bit D16 of the PLD Register (0 = write enable).

Next, links E5 to E8 must be fitted according to whether the Boot or User FLASH area of CPU0 or CPU 1 is required to be write enabled, as follows:

FLASH AREA	CPU0	CPU1
Boot	E8	E7
User	E6	E5

The link(s) must be inserted to enable writes to the corresponding PLD Register write enable bit. The links are out by default.

Finally, bits D17 and D19 of the PLD Register for the CPU actually enable writes to the appropriate area of FLASH, as follows:

D17: User FLASH Area Write Enable.
0 = Writes enabled.
1 = Writes disabled (default at power-up).

D19: Boot FLASH Area Write Enable.
0 = Writes enabled.
1 = Writes disabled (default at power-up).

Notes:

1) Bits D17 and D19 can be written to to disable writes whatever the state of the links.
2) The FLPRGEN~ signal can be used to control writes even after the appropriate PLD bit has enabled the write. However, changing this signal during a write/erase operation may have an undetermined effect on the operation.

The following tabulates the above to show the conditions for writing to the different areas of FLASH:

PLD Reg. Bit	E7/FLPRGEN~	E6 (CPU0)/ E5 (CPU1)	E8 (CPU0)/ E7 (CPU1)
D17	Fitted/low	Fitted	x
D19	Fitted/low	x	Fitted

FLASH Area	E11/FLPRGEN~	PLD Reg. D17	PLD Reg. D19
Scratch	Can always be written to		
User	Fitted/low	0	x
Boot	Fitted/low	x	0
BANC	Can never be written to		

Note: Once the area of FLASH has been written to as required, don't forget to remove links to prevent further inadvertent writes.

See the Booting section for more details on FLASH usage when booting.

NVRAM

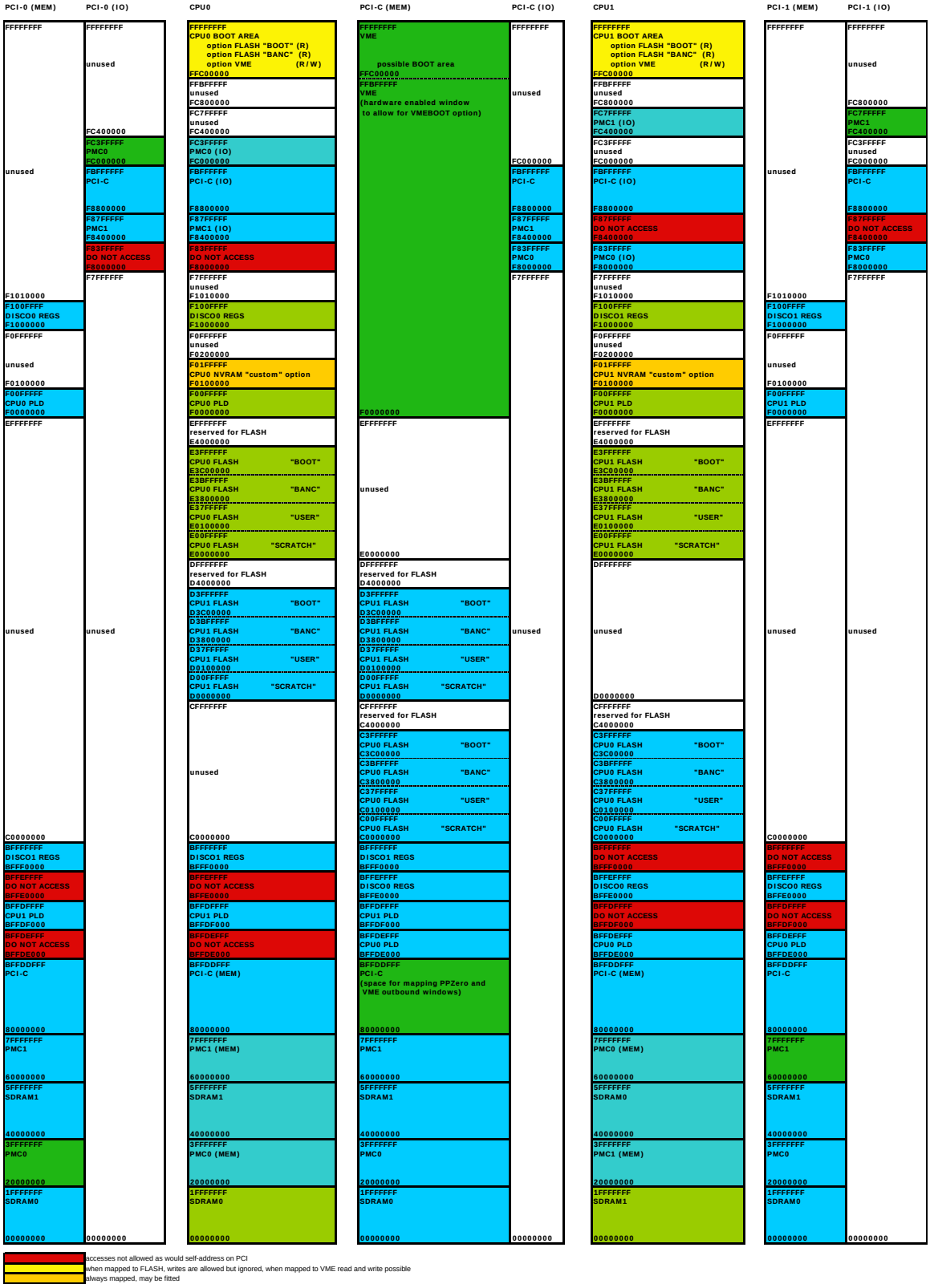
Note: This is a non-standard option to special order.

Custom options allow a 32 Kbyte NVRAM device to be fitted for either CPU0 or CPU1or both. These devices are fitted in the PMC front panel connector area and so are not compatible with all PMC cards. However, they are compatible with Radstone's PMC1553 card specifically.

The devices are Simtek STK14C88 Autostore NVRAMs. See the memory map for addressing information. They are only accessible (as standard) from the local processor.

The devices consist of 32 Kbytes of SRAM, which shadows 32 Kbytes of EEPROM. Data is restored from EEPROM to SRAM on power-up or under software instruction. SRAM can then be modified as many times as required by the processor. The SRAM is stored to EEPROM on power-down or under software instruction.

Memory Maps



The illustration above shows the memory map for each processor (CPU0 and CPU1), with the PCI buses that the processors can 'see' directly (PCI0 and PCIC for CPU0, and PCI1 and PCIC for CPU1). The PCI bus memory maps are sub-divided into memory and I/O space versions.

PCI Bus Architecture

Each of the two GT-62460A ("Discovery") CPU-PCI Bridge chips provides 2 PCI buses. These are termed PCI-0 and PCI-1 in the Discovery Documentation.

The PPCM1 architecture has 3 PCI buses:

- PCI0, which connects the PMC0 site to CPU0
- PCI1, which connects the PMC1 site to CPU1
- PCIC (common), which connects CPU0 to CPU1

The Discovery PCI buses map to the PPCM1 PCI buses as follows:

Discovery PCI Bus		PPCM1 PCI Bus	Comments
0	PCI-0	PCIC	64-bits wide, 33 MHz
	PCI-1	PCI0/PMC0	2 possible devices (A or B)
1	PCI-0	PCIC	64-bits wide, 33 MHz
	PCI-1	PCI1/PMC1	2 possible devices (A or B)

The IDSEL connections are as follows:

Device	PPCM1 Bus	Capability	IDSEL	Interrupts	INTA	INTB	INTC	INTD
Discovery 0, PCI-0	PCIC	64-bit, 33 MHz	PCIC_AD12		Discovery 1			
Discovery 1, PCI-0	PCIC	64-bit, 33 MHz	PCIC_AD13		Discovery 0			
Universe II	PCIC	64-bit, 33 MHz	PCIC_AD17	LINT0 → Discovery 0 LINT1 → CPU0 SMI LINT2 → Discovery 1 LINT3 → CPU1 SMI LINT7 → CPU0 Trigger				
PPzero (21555)	PCIC	64-bit, 33 MHz	PCIC_AD18	INT → Discovery 0	Discovery 0	Discovery 0	Discovery 0	Discovery 0
Discovery 0, PCI-1	PCI0	64-bit, 66 MHz	PCI0_AD23					PMC0 INTD[2]
PMC0 A	PCI0	64-bit, 66 MHz	PCI0_AD20		PMC0 INTA[1]	PMC0 INTB[1]	PMC0 INTC[1]	PMC0 INTD[1]
PMC0 B	PCI0	64-bit, 66 MHz	PCI0_AD21		PMC0 INTB[1]	PMC0 INTC[1]	PMC0 INTD[1]	PMC0 INTA[1]
Discovery 1, PCI-1	PCI1	64-bit, 66 MHz	PCI1_AD27					PMC1 INTD[2]
PMC1 A	PCI1	64-bit, 66 MHz	PCI1_AD24		PMC1 INTA[1]	PMC1 INTB[1]	PMC1 INTC[1]	PMC1 INTD[1]
PMC1 B	PCI1	64-bit, 66 MHz	PCI1_AD25		PMC1 INTB[1]	PMC1 INTC[1]	PMC1 INTD[1]	PMC1 INTA[1]

1 = Connected to both Discovery 0 and Discovery 1.

2 = Currently unused, but could be output to INTD to give interrupts in both directions between the PMC card and the corresponding Discovery.

At boot-up or reset, CPU0 configures all of the PCI buses, including PCI1.

Ethernet

The CPU0 node provides a 10/100BaseT Ethernet connection, usually through P0 (although depending on the I/O configuration, may be P2 – see the I/O Options section).

JTAG

The P12 connector provides a JTAG connection for CPU0.
The P11 connector provides a JTAG connection for CPU1.

Serial Ports

Each node provides a simple 2-wire (Tx and Rx) RS232 serial console port, usually through P0 (although depending on the I/O configuration, may be P2 – see the I/O Options section). CPU0 provides COM1 and CPU1 provides COM2.

Real Time Clock

There is one RTC. This has a resolution of 1 second and is provided by a PCF8563. It is available on the I^2C bus for CPU0 at address 1010001_b. The RTC has its own 32.768 kHz crystal for timing.

LEDs

There are 4 LEDs per processor visible through the front panel. The LEDs are controlled by bits D28 to D31 of the PLD Register for the appropriate CPU. During power-up the LEDs indicate progress through the boot sequence, as described in the LED Boot Sequences section.

On CPU0 after boot:

- If the green LED is not on, then OFFLINE~ is driven low
- If the red LED is on, then the SYSFAIL~ is also driven low

The external availability of these signals depends on the pinout option selected.

Discovery Counter/Timers

Each Discovery device has eight independent 32-bit wide registers that can be configured as either timers or counters. These have a resolution of 10ns with a 100 MHz bus speed. There are options for interconnecting certain timers to allow them to be cascaded (giving 64-bit operation) and to give synchronous timers between the two processors. The timer/counters are as follows:

Timer/ Counter	CPU	Function	Comments
TC0	CPU0	32-bit timer/counter with carry in connected to TC1 (CPU0) carry out	Each timer/counter can be used as an individual 32-bit timer/counter or TC0 in both of the Discovery devices can be run synchronously using TC1 (CPU0) as a prescaler
TC0	CPU1	32-bit timer/counter with carry in connected to TC1 (CPU0) carry out	
TC1	CPU0	32-bit timer/counter with carry out connected to TC0 (CPU0) and TC0 (CPU1) carry in	
TC1	CPU1	32-bit timer/counter	
TC2	CPU0/CPU1	32-bit timer/counters	
TC3	CPU0/CPU1	32-bit timer/counters	
TC4	CPU0/CPU1	32-bit timer/counters	
TC5	CPU0	32-bit timer/counter with carry out connected to TC6 (CPU0) carry in	Each timer/counter can be used as an individual 32-bit timer/counter or TC5 and TC6 in each Discovery device can be cascaded to provide a 64-bit timer/counter
TC5	CPU1	32-bit timer/counter with carry out connected to TC6 (CPU1) carry in	
TC6	CPU0	32-bit timer/counter with carry in connected to TC5 (CPU0) carry in	
TC6	CPU1	32-bit timer/counter with carry in connected to TC5 (CPU1) carry in	
TC7	CPU0/CPU1	32-bit timer/counters	

I²C Bus

The I²C bus is a bi-directional, two-wire (Serial Clock and Serial Data) bus for inter-IC control. On the PPCM1, it connects the CPU with the RTC, User EEPROM and Configuration EEPROM.

Address Map

The I²C bus has a 7-bit address map with the Read/Write bit as the eighth bit.

Address Bits								Device
A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	1	0	0	0	0	†	User EEPROM
1	0	1	0	0	0	1	R/W	RTC (CPU0 only)
1	0	1	0	0	1	0	R	VME Boot Config. EEPROM
1	0	1	0	0	1	1	R	FLASH Boot Config. EEPROM

† Always readable. Writeable only when bit D22 in the PLD Register is set to 0.

Configuring the CPU to boot from FLASH (using link E10 for CPU0 and E9 for CPU1, link not fitted) selects the 'FLASH Boot Config. EEPROM' address. In this mode, the Discovery configures from the FLASH Boot Configuration EEPROM.

Configuring the CPU to boot from the VMEbus (using link E10 for CPU0 and E9 for CPU1, link fitted) selects the 'VME Boot Config. EEPROM' address. In this mode, the Discovery configures from the VME Boot Configuration EEPROM.

Watchdog Timer

The MPP25 line on each Discovery is the Watchdog Expiry (WDE) signal, and is connected to a hard reset input that will reset the whole PPCM1. MPP24 is the Watchdog Interrupt Out (WDNMI) signal, which goes active shortly before watchdog expiry to warn the processor that this is about to happen. This is linked to MPP2 (a general purpose line that can be used as an interrupt input), which can then be routed to the processor.

CPU-PCI Bridge and Memory Controller

Each of the nodes on the PPCM1 features a 'Discovery' GT-62460 Integrated System Controller. The Discovery provides 8 independent DMA engines for high-speed data access on a 64-bit main memory bus running at speeds up to 100 MHz.

The Discoveries also implement a 64-bit, 33 MHz PCI bus (PCIC) that connects the two nodes with each other, the Universe II VME interface and a further PCI bridge that provides the on-board PPzero interface. See the PCI Bus Architecture and PPzero Interface sections for more details.

The following table shows the functions provided by the Discovery:

Line	CPU0		CPU1	
	Signal	Function	Signal	Function
MPP0	PPzero INTA	Interrupt input	DISCO0 GNT	Disco PCI0 arbiter (PCIC)
MPP1	PPzero INTB	Interrupt input	DISCO0 REQ	Disco PCI0 arbiter (PCIC)
MPP2	PPzero INTC	Interrupt input	Universe GNT	Disco PCI0 arbiter (PCIC)
MPP3	PPzero INTD	Interrupt input	Universe REQ	Disco PCI0 arbiter (PCIC)
MPP4	PPzero INT	Interrupt input	PPzero GNT	Disco PCI0 arbiter (PCIC)
MPP5	Linked to MPP6 (CPU0/1)	Timer 1 carry out	PPzero REQ	Disco PCI0 arbiter (PCIC)
MPP6	Linked to MPP5 (CPU0)	Common Timer 0 carry in	Linked to MPP5 (CPU0)	Common Timer 0 carry in
MPP7	NC		NC	
MPP8	PMC0 INTA	Interrupt input	PMC0 INTA	Interrupt input
MPP9	PMC0 INTB	Interrupt input	PMC0 INTB	Interrupt input
MPP10	PMC0 INTC	Interrupt input	PMC0 INTC	Interrupt input
MPP11	PMC0 INTD	Interrupt input	PMC0 INTD	Interrupt input
MPP12	PMC1 INTA	Interrupt input	PMC1 INTA	Interrupt input
MPP13	PMC1 INTB	Interrupt input	PMC1 INTB	Interrupt input
MPP14	PMC1 INTC	Interrupt input	PMC1 INTC	Interrupt input
MPP15	PMC1 INTD	Interrupt input	PMC1 INTD	Interrupt input
MPP16	PMC0 GNTA	Disco PCI1 arbiter (PCI0)	PMC1 GNTA	Disco PCI1 arbiter (PCI1)
MPP17	PMC0 REQA	Disco PCI1 arbiter (PCI0)	PMC1 REQA	Disco PCI1 arbiter (PCI1)
MPP18	PMC0 GNTB	Disco PCI1 arbiter (PCI0)	PMC1 GNTB	Disco PCI1 arbiter (PCI1)
MPP19	PMC0 REQB	Disco PCI1 arbiter (PCI0)	PMC1 REQB	Disco PCI1 arbiter (PCI1)
MPP20	Universe INT	Interrupt input	Universe INT	Interrupt input
MPP21	Other Disco PCI0 (PCIC) INT	Interrupt input	Other Discovery PCI0 (PCIC) INT	Interrupt input
MPP22	Linked to MPP24 WDNMI (CPU0)	Interrupt input	Linked to MPP24 WDNMI (CPU1)	Interrupt input
MPP23	MCP (CPU0)	Interrupt output	MCP (CPU1)	Interrupt output
MPP24	Linked to MPP22 WDNMI (CPU0)	Watchdog interrupt output	Linked to MPP22 WDNMI (CPU1)	Watchdog interrupt output
MPP25	WDE (CPU0)	Watchdog reset output	WDE (CPU1)	Watchdog reset output
MPP26	Linked to MPP29[1] (CPU0)	Timer 6 carry in	Linked to MPP29[1] (CPU1)	Timer 6 carry in
MPP27	RTC INT (shared)	Interrupt input	RTC INT (shared)	Interrupt input
MPP28	INITACT (CPU0)	Hardware use[3]	INITACT	Hardware use[3]
MPP29	Linked to MPP26[1] (CPU0)	Timer 5 carry out	Linked to MPP26[1] (CPU1)	Timer 5 carry out
MPP30	BCLKIN	14.7456 MHz baud rate clock source	BCLKIN	14.7456 MHz baud rate clock source
MPP31	CPU HRESET[2]	0 = No reset 1 = Reset	CPU HRESET[2]	0 = No reset 1 = Reset

1) Allows 2 timers to be linked for 64-bit operation.

2) For CPU1 in Controlled VME Boot mode, this needs to be set as an output and taken low to release the CPU from reset (or push the front panel switch to the 'Soft Reset' position). It is not used for CPU0 in Controlled VME Boot mode.

3) An indication to the hardware that the Discovery is configuring from serial EEPROM. This holds the CPU in reset until configuration is complete.

PPzero Interface

The PPCM1 implements an on-board (rather than via a PMC) PPzero interface (see the PPzero data sheet for more details). This is similar to Radstone's PMCPCI interface, but uses a Intel 21555 PCI to PCI bridge to provide either a Master or a Slave interface (selectable using link E13) with the same hardware. The PPzero PCI bus runs at 33 MHz. The primary interface of the 21555 bridge is connected to the PPZero bus and the secondary interface is connected to the internal PCI-C bus.

Certain PCI Bridge parameters, plus other additional information, can be read from the parallel PROM interface (using any address), as shown in the table below. The parallel PROM space can be accessed using register accesses rather than by enabling a decode in PCI memory space.

BIT	VALUE	COMMENTS
D7	**0 = No secondary bus arbiter**	Power-up configuration
D6	**1 = No central functions**	Power-up configuration
D5	**0 = Disable sclk_0 output**	Power-up configuration
D4	0 = Synchronous clocking 1 = Asynchronous clocking	Power-up configuration
D3	**1 = Primary lockout**	Power-up configuration
D2	Reads as 1	Power-up configuration
D1	1 = 32-bit capable	PPCM1 PPzero configuration
D0	0 = PPzero Master† 1 = PPzero Slave	PPCM1 PPzero configuration

Bold text indicates fixed settings.

† Indicates the state of link E13, which must be fitted to correspond to the slot in the PPzero backplane into which the PPCM1 is fitted:

CAUTION

If there is no PPzero backplane fitted in your system, E13 must be fitted.

If your PPCM1 is fitted in the first (leftmost) slot of a PPzero backplane, E13 must be fitted (PPCM1 is PPzero Master, D0 = 0).

If your PPCM1 is fitted in any other slot of a PPzero backplane, E13 must not be fitted and a PPzero Master must be fitted to the leftmost slot of the PPzero backplane (PPCM1 is PPzero Slave, D0 = 1).

PLD Registers

CPU0

The 32-bit CPU0 PLD register can be read from or written to as individual bytes or as a 32-bit value (see the Memory Maps section for register accessibility regions). It has the following bit allocation:

Bits	Read/Write	Description	Power-up/Reset
D0 to D4	Read only	Processor ID from P10 or backplane. D0 to D4 correspond to GA0 to GA4 respectively	As link/backplane (latched at end of reset)
D5	Read only	0 = CPU0	
D6	Read only	Reads 0	0
D7	Read only	Reflects level of BITFAST~ signal.[7] 0 = Skip BIT 1 = Run BIT	
D8	Read only	PMC0 speed (latched at end of reset) 0 = 33 MHz 1 = 66 MHz	
D9	Read only	PMC0 fitted (latched at end of reset) 0 = Fitted 1 = Not fitted	
D10	Read only	PMC1 speed (latched at end of reset) 0 = 33 MHz 1 = 66 MHz	
D11	Read only	PMC1 fitted (latched at end of reset) 0 = Fitted 1 = Not fitted	
D12 to D15	Read only	Reserved. Read as 0	0
D16	Read only	Reflects level of FLPRGEN~ signal/E11 0 = Writes enabled 1 = Writes disabled	
D17	Read/write	User FLASH write enable[1] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D18	Read/write	BANC FLASH write enable[3] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D19	Read/write	Boot FLASH write enable[2] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D20	Read only	Reflects state of link E4 0 = Boot and BANC FLASH areas swapped 1 = Boot and BANC areas not swapped	As link
D21	Read only	Reflects state of link E10 0 = Boot from VME 1 = Boot from FLASH	As link
D22	Read/write	User EEPROM write enable 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D23	Read/write	Configuration EEPROM write enable[4] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D24	Read/write	Reset switch enable (switch only fitted on build levels 1 to 3) 0 = Reset switch enabled 1 = Reset switch disabled	Set to 0 at power-up
D25	Read/write	PHY reset 0 = Reset 1 = Operational	Set to 0 at power-up
D26 and D27	Read only	Reserved. Read as 0	0

BITS	READ/WRITE	DESCRIPTION	POWER-UP/RESET
D28	Read/write	Green LED 0 = On 1 = Off Also drives OFFLINE~ signal (OFFLINE~ low when LED off)	Set to 1 at power-up[6]
D29	Read/write	Amber (by Green) LED 0 = On 1 = Off	Set to 1 at power-up[6]
D30	Read/write	Amber (by Red) LED 0 = On 1 = Off	Set to 1 at power-up[6]
D31	Read/write[5]	Red LED 0 = On 1 = Off Also drives SYSFAIL~ signal (SYSFAIL~ low when LED lit)	Set to 0 at power-up[6]

1) To enable this bit (D17) to be set to 0 requires link E6 to be fitted and FLPRGEN~ to be low (see the FLASH section). The bit can be set to 1 regardless of link settings. FLPRGEN~ can be used to control writes after the bit is set to 0.

2) To enable this bit (D19) to be set to 0 requires link E8 to be fitted and FLPRGEN~ to be low (see the FLASH section). The bit can be set to 1 regardless of link settings. FLPRGEN~ can be used to control writes after the bit is set to 0.

3) To enable this bit (D18) to be set to 0 requires an appropriate link to be fitted and FLPRGEN~ to be low (see the FLASH section). The bit can be set to 1 regardless of link settings. FLPRGEN~ can be used to control writes after the bit is set to 0.

4) An appropriate link must be fitted to enable this bit (D23) to be set to 0.

Note: The BANC FLASH and Configuration EEPROM Write Enable bits (D18 and D23 respectively) are not normally accessible. The mechanism to allow writes to these areas will be provided by Radstone if necessary.

5) If the green LED is off (bit D28 = 1), then this bit (D31) is read/write, but writing to it will not change the state of the red LED.

6) See the LED Boot Sequences section.

7) The BITFAST~ input signal tells the processor whether to run or skip BIT (if installed). Both CPU0 and CPU1 use the same signal, which is high (run BIT) by default. If the signal is pulled low, BIT is skipped.

CPU1

The 32-bit CPU1 PLD register can be read from or written to as individual bytes or as a 32-bit value (see the Memory Maps section for register accessibility regions). It has the following bit allocation:

BITS	READ/WRITE	DESCRIPTION	POWER-UP/RESET
D0 to D4	Read only	Processor ID from P10 or backplane. D0 to D4 correspond to GA0 to GA4 respectively	As link/backplane (latched at end of reset)
D5	Read only	1 = CPU1	
D6	Read only	Reads 0	0
D7	Read only	Reflects level of BITFAST~ signal.[7] 0 = Skip BIT 1 = Run BIT	
D8	Read only	PMC0 speed (latched at end of reset) 0 = 33 MHz 1 = 66 MHz	
D9	Read only	PMC0 fitted (latched at end of reset) 0 = Fitted 1 = Not fitted	
D10	Read only	PMC1 speed (latched at end of reset) 0 = 33 MHz 1 = 66 MHz	
D11	Read only	PMC1 fitted (latched at end of reset) 0 = Fitted 1 = Not fitted	
D12 to D15	Read only	Reserved. Read as 0	0
D16	Read only	Reflects level of FLPRGEN~ signal/E11 0 = Writes enabled 1 = Writes disabled	
D17	Read/write	User FLASH write enable[1] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D18	Read/write	BANC FLASH write enable[3] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D19	Read/write	Boot FLASH write enable[2] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D20	Read only	Reflects state of link E3 0 = Boot and BANC FLASH areas swapped 1 = Boot and BANC areas not swapped	As link
D21	Read only	Reflects state of link E9 0 = Controlled boot 1 = Boot from FLASH	As link
D22	Read/write	User EEPROM write enable 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D23	Read/write	Configuration EEPROM write enable[4] 0 = Writes enabled 1 = Writes disabled	Reads 1 at power-up
D24	Read/write	Reset switch enable (switch only fitted on build levels 1 to 3) 0 = Reset switch enabled 1 = Reset switch disabled	Set to 0 at power-up
D25	Read only	Reserved. Read as 0	0
D26 and D27	Read only	Reserved. Read as 0	0

BITS	READ/WRITE	DESCRIPTION	POWER-UP/RESET
D28	Read/write	Green LED 0 = On 1 = Off	Set to 1 at power-up[6]
D29	Read/write	Amber (by Green) LED 0 = On 1 = Off	Set to 1 at power-up[6]
D30	Read/write	Amber (by Red) LED 0 = On 1 = Off	Set to 1 at power-up[6]
D31	Read/write[5]	Red LED 0 = On 1 = Off	Set to 0 at power-up[6]

1) To enable this bit (D17) to be set to 0 requires link E5 to be fitted and FLPRGEN~ to be low (see the FLASH section). The bit can be set to 1 regardless of link settings. FLPRGEN~ can be used to control writes after the bit is set to 0.

2) To enable this bit (D19) to be set to 0 requires link E7 to be fitted and FLPRGEN~ to be low (see the FLASH section). The bit can be set to 1 regardless of link settings. FLPRGEN~ can be used to control writes after the bit is set to 0.

3) To enable this bit (D18) to be set to 0 requires an appropriate link to be fitted and FLPRGEN~ to be low (see the FLASH section). The bit can be set to 1 regardless of link settings. FLPRGEN~ can be used to control writes after the bit is set to 0.

4) An appropriate link must be fitted to enable this bit (D23) to be set to 0.

Note: The BANC FLASH and Configuration EEPROM Write Enable bits (D18 and D23 respectively) are not normally accessible. The mechanism to allow writes to these areas will be provided by Radstone if necessary.

5) If the green LED is off (bit D28 = 1), then this bit (D31) is read/write, but writing to it will not change the state of the red LED.

6) See the LED Boot Sequences section.

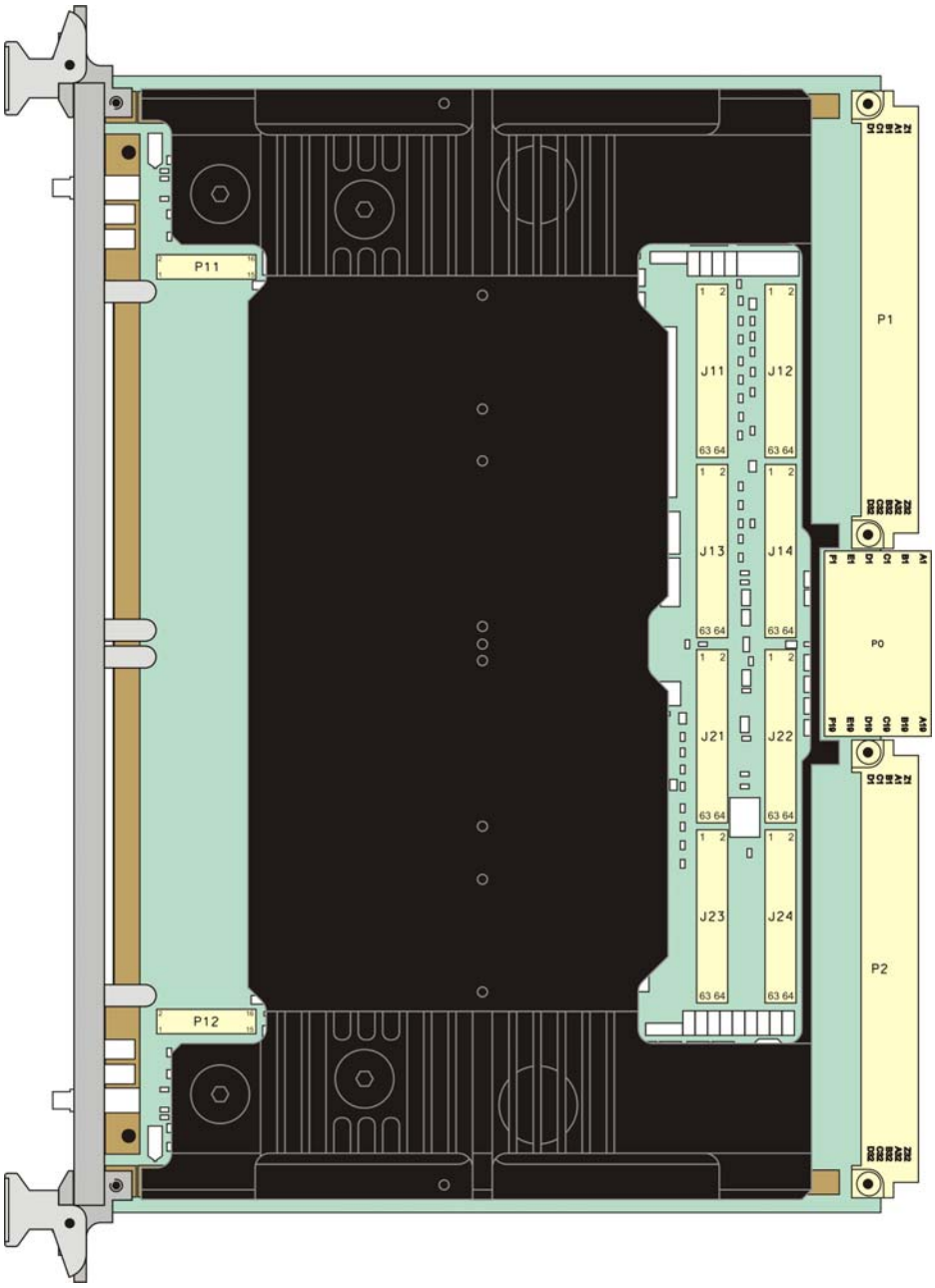
7) The BITFAST~ input signal tells the processor whether to run or skip BIT (if installed). Both CPU0 and CPU1 use the same signal, which is high (run BIT) by default. If the signal is pulled low, BIT is skipped.

Connectors

The following table shows the function of the connectors on the PPCM1:

CONNECTOR	FUNCTION
P1	VMEbus (see general description)
P2	VMEbus and I/O
P0	PCI
J11, J12, J13, J14	PMC1 site (see general description)
J21, J22, J23, J24	PMC0 site (see general description)
P11	EST VisionProbe connector for CPU1
P12	EST VisionProbe connector for CPU0

Figure A-3. Connector Positions and Pin Numbering



I/O Options

There are several variants for I/O through P2 (rows z, a, c and d) and P0 (rows A to E), as shown below (see the Product Codes section for more details on variant numbering).

'XtraPower pinout' is a new Radstone pinout standard, specific to boards in the XtraPower range. 'Compatibility pinout' maintains some pinout compatibility with Radstone's established PowerX processors. In particular, COM1, COM2, Ethernet and BIT Fast Start are maintained at the same pin locations.

VARIANT	DESCRIPTION	P0	P2	
			ROW A/C	ROW Z/D
xxx0By	PPzero32 with XtraPower pinout and BIT Master signals	COM1, COM2, Ethernet, BITFAST, FLPRGEN, PMC1_FC, PPzero32	PMC0 (64)	PMC1 (40), BITFAST, OFFLINE, SYSFAIL, EXTRESET, EXTABORT0, EXTABORT1
xxx0Dy	PPzero32 with XtraPower pinout and full PMC I/O	COM1, COM2, Ethernet, BITFAST, FLPRGEN, PMC1_FC, PPzero32	PMC0 (64)	PMC1 (46)
xxx0F[1]y	PPzero32 with compatibility pinout and BIT Master signals	PMC1_FC, PPzero32, FLPRGEN, OFFLINE, SYSFAIL, EXTRESET, EXTABORT0, EXTABORT1	COM1, COM2, Ethernet, BITFAST	PMC1 (40)
xxx2By	XtraPower pinout and BIT Master signals (no PPzero32)	COM1, COM2, Ethernet, BITFAST, FLPRGEN, PMC1_FC	PMC0 (64)	PMC1 (40), BITFAST, OFFLINE, SYSFAIL, EXTRESET, EXTABORT0, EXTABORT1
xxx2Dy	XtraPower pinout and full PMC I/O (no PPzero32)	COM1, COM2, Ethernet, BITFAST, FLPRGEN, PMC1_FC	PMC0 (64)	PMC1 (46)
xxx2F[1]y	Compatibility pinout and BIT Master signals (no PPzero32)	PMC1_FC, FLPRGEN, OFFLINE, SYSFAIL, EXTRESET, EXTABORT0, EXTABORT1	COM1, COM2, Ethernet, BITFAST	PMC1 (40)

COM1, Ethernet, SYSFAIL, OFFLINE, PCI and PMC0 are associated with CPU0

COM2 and PMC1 are associated with CPU1

Notes:

1) The above table, in electronic form, is hyperlinked on the 'Variant', 'P0' and 'P2' columns to jump to the relevant pinout table(s).
2) There is no rear I/O from PMC0 with options 0F and 2F.
3) Variant '0D', as highlighted above, is the default pinout.
4) Although the PMC1_IO47 to PMC1_IO52, PMC1_IO55 to PMC1_IO59 and PMC1_IO61 to PMC1_IO64 signals routed through the P0 connector are general purpose PMC I/O signals, and not tied to any particular functionality, they are mainly intended for use by a Fibre Channel PMC, and so are shown as 'PMC1_FC' above. These PMC1_FC signals are only available when Type B (95-way) P0 connectors are fitted.
5) In the table above, y = 0 or B for a Type B (95-way) P0 connector.
   y = A for a Type A (80-way) P0 connector.
   Due to the large amount of I/O required to be handled by the PPCM1, Type B (95-way) P0 connectors are always fitted unless specified otherwise.

Variant xxx0By

P0 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	ETH_TXP	ETH_RXP	BITFAST~	COM1_TX	COM2_TX	GND
2	ETH_TXN	ETH_RXN	FLPRGEN~	COM1_RX	COM2_RX	GND
3	3.3V	3.3V	3.3V	5V	5V	GND
4	GND	IDSEL/CLK4	GNT~/CLK3	REQ~/CLK2	CLK/CLK1	GND
5	NC/GNT2~	NC/REQ2~	NC/GNT1~	NC/REQ1~	GND	GND
6	C/BE1	NC/GNT4~	NC/REQ4~	NC/GNT3~	NC/REQ3	GND
7	RESET~	FRAME~	C/BE2	C/BE3	C/BE0	GND
8	PAR	TRDY~	IRDY~	DEVSEL~	LOCK~	GND
9	PMC1_IO50	PMC1_IO49	PMC1_IO62	PMC1_IO56	PMC1_IO55	GND
10	PMC1_IO48	PMC1_IO47	PMC1_IO59	PMC1_IO64	PMC1_IO63	GND
11	PMC1_IO52	PMC1_IO51	PMC1_IO61	PMC1_IO58	PMC1_IO57	GND
12	AD0	AD1	PERR~	SERR~	STOP~	GND
13	AD5	AD2	AD3	INTA~	INTB~	GND
14	AD8	AD9	AD6	AD7	AD4	GND
15	AD15	AD12	AD13	AD10	AD11	GND
16	AD18	AD19	AD16	AD17	AD14	GND
17	AD25	AD22	AD23	AD20	AD21	GND
18	INTD~	INTC~	AD26	AD27	AD24	GND
19	5V	AD30	AD31	AD28	AD29	GND

Key

Power	PPzero32	Comms	BIT Master/misc	PMC1 I/O

Notes:

1) Pins B4, C4, D4, E4, A5, B5, C5, D5, B6, C6, D6, E6 are shown as x/y, where x is the signal for a PPzero Slave and y is the signal for a PPzero Master.
2) If a type A P0 connector is fitted, then connections on rows 9, 10 and 11 are not available.

P2 Pinout

Pin	Row z	Row a	Row c	Row d
1	PMC1_IO2	PMC0_IO2	PMC0_IO1	PMC1_IO1
2	GND	PMC0_IO4	PMC0_IO3	PMC1_IO3
3	PMC1_IO5	PMC0_IO6	PMC0_IO5	PMC1_IO4
4	GND	PMC0_IO8	PMC0_IO7	PMC1_IO6
5	PMC1_IO8	PMC0_IO10	PMC0_IO9	PMC1_IO7
6	GND	PMC0_IO12	PMC0_IO11	PMC1_IO9
7	PMC1_IO11	PMC0_IO14	PMC0_IO13	PMC1_IO10
8	GND	PMC0_IO16	PMC0_IO15	PMC1_IO12
9	PMC1_IO14	PMC0_IO18	PMC0_IO17	PMC1_IO13
10	GND	PMC0_IO20	PMC0_IO19	PMC1_IO15
11	PMC1_IO17	PMC0_IO22	PMC0_IO21	PMC1_IO16
12	GND	PMC0_IO24	PMC0_IO23	PMC1_IO18
13	PMC1_IO20	PMC0_IO26	PMC0_IO25	PMC1_IO19
14	GND	PMC0_IO28	PMC0_IO27	PMC1_IO21
15	PMC1_IO23	PMC0_IO30	PMC0_IO29	PMC1_IO22
16	GND	PMC0_IO32	PMC0_IO31	PMC1_IO24
17	PMC1_IO26	PMC0_IO34	PMC0_IO33	PMC1_IO25
18	GND	PMC0_IO36	PMC0_IO35	PMC1_IO27
19	PMC1_IO29	PMC0_IO38	PMC0_IO37	PMC1_IO28
20	GND	PMC0_IO40	PMC0_IO39	PMC1_IO30
21	PMC1_IO32	PMC0_IO42	PMC0_IO41	PMC1_IO31
22	GND	PMC0_IO44	PMC0_IO43	PMC1_IO33
23	PMC1_IO35	PMC0_IO46	PMC0_IO45	PMC1_IO34
24	GND	PMC0_IO48	PMC0_IO47	PMC1_IO36
25	PMC1_IO38	PMC0_IO50	PMC0_IO49	PMC1_IO37
26	GND	PMC0_IO52	PMC0_IO51	PMC1_IO39
27	BITFAST~	PMC0_IO54	PMC0_IO53	PMC1_IO40
28	GND	PMC0_IO56	PMC0_IO55	EXTRESET~
29	OFFLINE~	PMC0_IO58	PMC0_IO57	EXTABORT0~
30	GND	PMC0_IO60	PMC0_IO59	EXTABORT1~
31	SYSFAIL~	PMC0_IO62	PMC0_IO61	GND
32	GND	PMC0_IO64	PMC0_IO63	5V

Key

Power	BIT Master/misc	PMC1 I/O	PMC0 I/O

Variant xxx0Dy

P0 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	ETH_TXP	ETH_RXP	BITFAST~	COM1_TX	COM2_TX	GND
2	ETH_TXN	ETH_RXN	FLPRGEN~	COM1_RX	COM2_RX	GND
3	3.3V	3.3V	3.3V	5V	5V	GND
4	GND	IDSEL/CLK4	GNT~/CLK3	REQ~/CLK2	CLK/CLK1	GND
5	NC/GNT2~	NC/REQ2~	NC/GNT1~	NC/REQ1~	GND	GND
6	C/BE1	NC/GNT4~	NC/REQ4~	NC/GNT3~	NC/REQ3	GND
7	RESET~	FRAME~	C/BE2	C/BE3	C/BE0	GND
8	PAR	TRDY~	IRDY~	DEVSEL~	LOCK~	GND
9	PMC1_IO50	PMC1_IO49	PMC1_IO62	PMC1_IO56	PMC1_IO55	GND
10	PMC1_IO48	PMC1_IO47	PMC1_IO59	PMC1_IO64	PMC1_IO63	GND
11	PMC1_IO52	PMC1_IO51	PMC1_IO61	PMC1_IO58	PMC1_IO57	GND
12	AD0	AD1	PERR~	SERR~	STOP~	GND
13	AD5	AD2	AD3	INTA~	INTB~	GND
14	AD8	AD9	AD6	AD7	AD4	GND
15	AD15	AD12	AD13	AD10	AD11	GND
16	AD18	AD19	AD16	AD17	AD14	GND
17	AD25	AD22	AD23	AD20	AD21	GND
18	INTD~	INTC~	AD26	AD27	AD24	GND
19	5V	AD30	AD31	AD28	AD29	GND

Key

Power	PPzero32	Comms	BIT Master/misc	PMC1 I/O

Notes:

1) Pins B4, C4, D4, E4, A5, B5, C5, D5, B6, C6, D6, E6 are shown as x/y, where x is the signal for a PPzero Slave and y is the signal for a PPzero Master.
2) If a type A P0 connector is fitted, then connections on rows 9, 10 and 11 are not available.

P2 Pinout

Pin	Row z	Row a	Row c	Row d
1	PMC1_IO2	PMC0_IO2	PMC0_IO1	PMC1_IO1
2	GND	PMC0_IO4	PMC0_IO3	PMC1_IO3
3	PMC1_IO5	PMC0_IO6	PMC0_IO5	PMC1_IO4
4	GND	PMC0_IO8	PMC0_IO7	PMC1_IO6
5	PMC1_IO8	PMC0_IO10	PMC0_IO9	PMC1_IO7
6	GND	PMC0_IO12	PMC0_IO11	PMC1_IO9
7	PMC1_IO11	PMC0_IO14	PMC0_IO13	PMC1_IO10
8	GND	PMC0_IO16	PMC0_IO15	PMC1_IO12
9	PMC1_IO14	PMC0_IO18	PMC0_IO17	PMC1_IO13
10	GND	PMC0_IO20	PMC0_IO19	PMC1_IO15
11	PMC1_IO17	PMC0_IO22	PMC0_IO21	PMC1_IO16
12	GND	PMC0_IO24	PMC0_IO23	PMC1_IO18
13	PMC1_IO20	PMC0_IO26	PMC0_IO25	PMC1_IO19
14	GND	PMC0_IO28	PMC0_IO27	PMC1_IO21
15	PMC1_IO23	PMC0_IO30	PMC0_IO29	PMC1_IO22
16	GND	PMC0_IO32	PMC0_IO31	PMC1_IO24
17	PMC1_IO26	PMC0_IO34	PMC0_IO33	PMC1_IO25
18	GND	PMC0_IO36	PMC0_IO35	PMC1_IO27
19	PMC1_IO29	PMC0_IO38	PMC0_IO37	PMC1_IO28
20	GND	PMC0_IO40	PMC0_IO39	PMC1_IO30
21	PMC1_IO32	PMC0_IO42	PMC0_IO41	PMC1_IO31
22	GND	PMC0_IO44	PMC0_IO43	PMC1_IO33
23	PMC1_IO35	PMC0_IO46	PMC0_IO45	PMC1_IO34
24	GND	PMC0_IO48	PMC0_IO47	PMC1_IO36
25	PMC1_IO38	PMC0_IO50	PMC0_IO49	PMC1_IO37
26	GND	PMC0_IO52	PMC0_IO51	PMC1_IO39
27	PMC1_IO41	PMC0_IO54	PMC0_IO53	PMC1_IO40
28	GND	PMC0_IO56	PMC0_IO55	PMC1_IO42
29	PMC1_IO44	PMC0_IO58	PMC0_IO57	PMC1_IO43
30	GND	PMC0_IO60	PMC0_IO59	PMC1_IO45
31	PMC1_IO46	PMC0_IO62	PMC0_IO61	GND
32	GND	PMC0_IO64	PMC0_IO63	5V

Key

Power	PMC1 I/O	PMC0 I/O

Variant xxx0Fy

P0 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	NC	SYSFAIL~	EXTRESET~	NC	NC	GND
2	FLPRGEN~	OFFLINE~	EXTABORT0~	EXTABORT1~	NC	GND
3	3.3V	3.3V	3.3V	5V	5V	GND
4	GND	IDSEL/CLK4	GNT~/CLK3	REQ~/CLK2	CLK/CLK1	GND
5	NC/GNT2~	NC/REQ2~	NC/GNT1~	NC/REQ1~	GND	GND
6	C/BE1	NC/GNT4~	NC/REQ4~	NC/GNT3~	NC/REQ3	GND
7	RESET~	FRAME~	C/BE2	C/BE3	C/BE0	GND
8	PAR	TRDY~	IRDY~	DEVSEL~	LOCK~	GND
9	PMC1_IO50	PMC1_IO49	PMC1_IO62	PMC1_IO56	PMC1_IO55	GND
10	PMC1_IO48	PMC1_IO47	PMC1_IO59	PMC1_IO64	PMC1_IO63	GND
11	PMC1_IO52	PMC1_IO51	PMC1_IO61	PMC1_IO58	PMC1_IO57	GND
12	AD0	AD1	PERR~	SERR~	STOP~	GND
13	AD5	AD2	AD3	INTA~	INTB~	GND
14	AD8	AD9	AD6	AD7	AD4	GND
15	AD15	AD12	AD13	AD10	AD11	GND
16	AD18	AD19	AD16	AD17	AD14	GND
17	AD25	AD22	AD23	AD20	AD21	GND
18	INTD~	INTC~	AD26	AD27	AD24	GND
19	5V	AD30	AD31	AD28	AD29	GND

Key

Power	PPzero32	BIT Master/misc	PMC1 I/O

Notes:

1) Pins B4, C4, D4, E4, A5, B5, C5, D5, B6, C6, D6, E6 are shown as x/y, where x is the signal for a PPzero Slave and y is the signal for a PPzero Master.
2) If a type A P0 connector is fitted, then connections on rows 9, 10 and 11 are not available.

P2 Pinout

Pin	Row z	Row a	Row c	Row d
1	PMC1_IO2	NC	ETH_RXP	PMC1_IO1
2	GND	NC	ETH_RXN	PMC1_IO3
3	PMC1_IO5	NC	ETH_TXP	PMC1_IO4
4	GND	NC	ETH_TXN	PMC1_IO6
5	PMC1_IO8	NC	NC	PMC1_IO7
6	GND	NC	NC	PMC1_IO9
7	PMC1_IO11	NC	NC	PMC1_IO10
8	GND	NC	NC	PMC1_IO12
9	PMC1_IO14	NC	NC	PMC1_IO13
10	GND	NC	NC	PMC1_IO15
11	PMC1_IO17	NC	NC	PMC1_IO16
12	GND	NC	NC	PMC1_IO18
13	PMC1_IO20	NC	NC	PMC1_IO19
14	GND	NC	NC	PMC1_IO21
15	PMC1_IO23	NC	NC	PMC1_IO22
16	GND	NC	NC	PMC1_IO24
17	PMC1_IO26	NC	NC	PMC1_IO25
18	GND	NC	NC	PMC1_IO27
19	PMC1_IO29	NC	NC	PMC1_IO28
20	GND	NC	NC	PMC1_IO30
21	PMC1_IO32	NC	NC	PMC1_IO31
22	GND	NC	NC	PMC1_IO33
23	PMC1_IO35	NC	NC	PMC1_IO34
24	GND	NC	NC	PMC1_IO36
25	PMC1_IO38	COM2_TX	NC	PMC1_IO37
26	GND	COM2_RX	BITFAST~	PMC1_IO39
27	NC	NC	COM1_TX	PMC1_IO40
28	GND	NC	COM1_RX	NC
29	NC	NC	NC	NC
30	GND	NC	NC	NC
31	NC	NC	NC	GND
32	GND	NC	NC	5V

Key

Power	BIT Master/misc	PMC1 I/O	Comms

Variant xxx2By

P0 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	ETH_TXP	ETH_RXP	BITFAST~	COM1_TX	COM2_TX	GND
2	ETH_TXN	ETH_RXN	FLPRGEN~	COM1_RX	COM2_RX	GND
3	3.3V	3.3V	3.3V	5V	5V	GND
4	GND	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	GND	GND
6	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	GND
9	PMC1_IO50	PMC1_IO49	PMC1_IO62	PMC1_IO56	PMC1_IO55	GND
10	PMC1_IO48	PMC1_IO47	PMC1_IO59	PMC1_IO64	PMC1_IO63	GND
11	PMC1_IO52	PMC1_IO51	PMC1_IO61	PMC1_IO58	PMC1_IO57	GND
12	NC	NC	NC	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
14	NC	NC	NC	NC	NC	GND
15	NC	NC	NC	NC	NC	GND
16	NC	NC	NC	NC	NC	GND
17	NC	NC	NC	NC	NC	GND
18	NC	NC	NC	NC	NC	GND
19	5V	NC	NC	NC	NC	GND

Key

Power	Comms	BIT Master/misc	PMC1 I/O

Notes:

1) Pins B4, C4, D4, E4, A5, B5, C5, D5, B6, C6, D6, E6 are shown as x/y, where x is the signal for a PPzero Slave and y is the signal for a PPzero Master.
2) If a type A P0 connector is fitted, then connections on rows 9, 10 and 11 are not available.

P2 Pinout

Pin	Row z	Row a	Row c	Row d
1	PMC1_IO2	PMC0_IO2	PMC0_IO1	PMC1_IO1
2	GND	PMC0_IO4	PMC0_IO3	PMC1_IO3
3	PMC1_IO5	PMC0_IO6	PMC0_IO5	PMC1_IO4
4	GND	PMC0_IO8	PMC0_IO7	PMC1_IO6
5	PMC1_IO8	PMC0_IO10	PMC0_IO9	PMC1_IO7
6	GND	PMC0_IO12	PMC0_IO11	PMC1_IO9
7	PMC1_IO11	PMC0_IO14	PMC0_IO13	PMC1_IO10
8	GND	PMC0_IO16	PMC0_IO15	PMC1_IO12
9	PMC1_IO14	PMC0_IO18	PMC0_IO17	PMC1_IO13
10	GND	PMC0_IO20	PMC0_IO19	PMC1_IO15
11	PMC1_IO17	PMC0_IO22	PMC0_IO21	PMC1_IO16
12	GND	PMC0_IO24	PMC0_IO23	PMC1_IO18
13	PMC1_IO20	PMC0_IO26	PMC0_IO25	PMC1_IO19
14	GND	PMC0_IO28	PMC0_IO27	PMC1_IO21
15	PMC1_IO23	PMC0_IO30	PMC0_IO29	PMC1_IO22
16	GND	PMC0_IO32	PMC0_IO31	PMC1_IO24
17	PMC1_IO26	PMC0_IO34	PMC0_IO33	PMC1_IO25
18	GND	PMC0_IO36	PMC0_IO35	PMC1_IO27
19	PMC1_IO29	PMC0_IO38	PMC0_IO37	PMC1_IO28
20	GND	PMC0_IO40	PMC0_IO39	PMC1_IO30
21	PMC1_IO32	PMC0_IO42	PMC0_IO41	PMC1_IO31
22	GND	PMC0_IO44	PMC0_IO43	PMC1_IO33
23	PMC1_IO35	PMC0_IO46	PMC0_IO45	PMC1_IO34
24	GND	PMC0_IO48	PMC0_IO47	PMC1_IO36
25	PMC1_IO38	PMC0_IO50	PMC0_IO49	PMC1_IO37
26	GND	PMC0_IO52	PMC0_IO51	PMC1_IO39
27	BITFAST~	PMC0_IO54	PMC0_IO53	PMC1_IO40
28	GND	PMC0_IO56	PMC0_IO55	EXTRESET~
29	OFFLINE~	PMC0_IO58	PMC0_IO57	EXTABORT0~
30	GND	PMC0_IO60	PMC0_IO59	EXTABORT1~
31	SYSFAIL~	PMC0_IO62	PMC0_IO61	GND
32	GND	PMC0_IO64	PMC0_IO63	5V

Key

Power	BIT Master/misc	PMC1 I/O	PMC0 I/O

Variant xxx2Dy

P0 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	ETH_TXP	ETH_RXP	BITFAST~	COM1_TX	COM2_TX	GND
2	ETH_TXN	ETH_RXN	FLPRGEN~	COM1_RX	COM2_RX	GND
3	3.3V	3.3V	3.3V	5V	5V	GND
4	GND	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	GND	GND
6	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	GND
9	PMC1_IO50	PMC1_IO49	PMC1_IO62	PMC1_IO56	PMC1_IO55	GND
10	PMC1_IO48	PMC1_IO47	PMC1_IO59	PMC1_IO64	PMC1_IO63	GND
11	PMC1_IO52	PMC1_IO51	PMC1_IO61	PMC1_IO58	PMC1_IO57	GND
12	NC	NC	NC	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
14	NC	NC	NC	NC	NC	GND
15	NC	NC	NC	NC	NC	GND
16	NC	NC	NC	NC	NC	GND
17	NC	NC	NC	NC	NC	GND
18	NC	NC	NC	NC	NC	GND
19	5V	NC	NC	NC	NC	GND

Key

Power	Comms	BIT Master/misc	PMC1 I/O

Notes:

1) Pins B4, C4, D4, E4, A5, B5, C5, D5, B6, C6, D6, E6 are shown as x/y, where x is the signal for a PPzero Slave and y is the signal for a PPzero Master.
2) If a type A P0 connector is fitted, then connections on rows 9, 10 and 11 are not available.

P2 Pinout

Pin	Row z	Row a	Row c	Row d
1	PMC1_IO2	PMC0_IO2	PMC0_IO1	PMC1_IO1
2	GND	PMC0_IO4	PMC0_IO3	PMC1_IO3
3	PMC1_IO5	PMC0_IO6	PMC0_IO5	PMC1_IO4
4	GND	PMC0_IO8	PMC0_IO7	PMC1_IO6
5	PMC1_IO8	PMC0_IO10	PMC0_IO9	PMC1_IO7
6	GND	PMC0_IO12	PMC0_IO11	PMC1_IO9
7	PMC1_IO11	PMC0_IO14	PMC0_IO13	PMC1_IO10
8	GND	PMC0_IO16	PMC0_IO15	PMC1_IO12
9	PMC1_IO14	PMC0_IO18	PMC0_IO17	PMC1_IO13
10	GND	PMC0_IO20	PMC0_IO19	PMC1_IO15
11	PMC1_IO17	PMC0_IO22	PMC0_IO21	PMC1_IO16
12	GND	PMC0_IO24	PMC0_IO23	PMC1_IO18
13	PMC1_IO20	PMC0_IO26	PMC0_IO25	PMC1_IO19
14	GND	PMC0_IO28	PMC0_IO27	PMC1_IO21
15	PMC1_IO23	PMC0_IO30	PMC0_IO29	PMC1_IO22
16	GND	PMC0_IO32	PMC0_IO31	PMC1_IO24
17	PMC1_IO26	PMC0_IO34	PMC0_IO33	PMC1_IO25
18	GND	PMC0_IO36	PMC0_IO35	PMC1_IO27
19	PMC1_IO29	PMC0_IO38	PMC0_IO37	PMC1_IO28
20	GND	PMC0_IO40	PMC0_IO39	PMC1_IO30
21	PMC1_IO32	PMC0_IO42	PMC0_IO41	PMC1_IO31
22	GND	PMC0_IO44	PMC0_IO43	PMC1_IO33
23	PMC1_IO35	PMC0_IO46	PMC0_IO45	PMC1_IO34
24	GND	PMC0_IO48	PMC0_IO47	PMC1_IO36
25	PMC1_IO38	PMC0_IO50	PMC0_IO49	PMC1_IO37
26	GND	PMC0_IO52	PMC0_IO51	PMC1_IO39
27	PMC1_IO41	PMC0_IO54	PMC0_IO53	PMC1_IO40
28	GND	PMC0_IO56	PMC0_IO55	PMC1_IO42
29	PMC1_IO44	PMC0_IO58	PMC0_IO57	PMC1_IO43
30	GND	PMC0_IO60	PMC0_IO59	PMC1_IO45
31	PMC1_IO46	PMC0_IO62	PMC0_IO61	GND
32	GND	PMC0_IO64	PMC0_IO63	5V

Key

Power	PMC1 I/O	PMC0 I/O

Variant xxx2Fy

P0 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	NC	SYSFAIL~	EXTRESET~	NC	NC	GND
2	FLPRGEN~	OFFLINE~	EXTABORT0~	EXTABORT1~	NC	GND
3	3.3V	3.3V	3.3V	5V	5V	GND
4	GND	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	GND	GND
6	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	GND
9	PMC1_IO50	PMC1_IO49	PMC1_IO62	PMC1_IO56	PMC1_IO55	GND
10	PMC1_IO48	PMC1_IO47	PMC1_IO59	PMC1_IO64	PMC1_IO63	GND
11	PMC1_IO52	PMC1_IO51	PMC1_IO61	PMC1_IO58	PMC1_IO57	GND
12	NC	NC	NC	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
14	NC	NC	NC	NC	NC	GND
15	NC	NC	NC	NC	NC	GND
16	NC	NC	NC	NC	NC	GND
17	NC	NC	NC	NC	NC	GND
18	NC	NC	NC	NC	NC	GND
19	5V	NC	NC	NC	NC	GND

Key

Power	BIT Master/misc	PMC1 I/O

Notes:

1) Pins B4, C4, D4, E4, A5, B5, C5, D5, B6, C6, D6, E6 are shown as x/y, where x is the signal for a PPzero Slave and y is the signal for a PPzero Master.
2) If a type A P0 connector is fitted, then connections on rows 9, 10 and 11 are not available.

P2 Pinout

Pin	Row z	Row a	Row c	Row d
1	PMC1_IO2	NC	ETH_RXP	PMC1_IO1
2	GND	NC	ETH_RXN	PMC1_IO3
3	PMC1_IO5	NC	ETH_TXP	PMC1_IO4
4	GND	NC	ETH_TXN	PMC1_IO6
5	PMC1_IO8	NC	NC	PMC1_IO7
6	GND	NC	NC	PMC1_IO9
7	PMC1_IO11	NC	NC	PMC1_IO10
8	GND	NC	NC	PMC1_IO12
9	PMC1_IO14	NC	NC	PMC1_IO13
10	GND	NC	NC	PMC1_IO15
11	PMC1_IO17	NC	NC	PMC1_IO16
12	GND	NC	NC	PMC1_IO18
13	PMC1_IO20	NC	NC	PMC1_IO19
14	GND	NC	NC	PMC1_IO21
15	PMC1_IO23	NC	NC	PMC1_IO22
16	GND	NC	NC	PMC1_IO24
17	PMC1_IO26	NC	NC	PMC1_IO25
18	GND	NC	NC	PMC1_IO27
19	PMC1_IO29	NC	NC	PMC1_IO28
20	GND	NC	NC	PMC1_IO30
21	PMC1_IO32	NC	NC	PMC1_IO31
22	GND	NC	NC	PMC1_IO33
23	PMC1_IO35	NC	NC	PMC1_IO34
24	GND	NC	NC	PMC1_IO36
25	PMC1_IO38	COM2_TX	NC	PMC1_IO37
26	GND	COM2_RX	BITFAST~	PMC1_IO39
27	NC	NC	COM1_TX	PMC1_IO40
28	GND	NC	COM1_RX	NC
29	NC	NC	NC	NC
30	GND	NC	NC	NC
31	NC	NC	NC	GND
32	GND	NC	NC	5V

Key

Power	BIT Master/misc	PMC1 I/O	Comms

P0/P2 Signal Descriptions

MNEMONIC	DESCRIPTION
3.3V	**+3.3V PCI supply pins**. These pins are not connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on P1, and capacitively decoupled to ground
5V	+5 Volts DC power
EXTRESET~	**External reset**. Generates a Hard Reset. See the Resets section for more details
EXTABORT0~, EXTABORT1~	**External abort**. Generate a Soft Reset to the corresponding CPU. See the Resets section for more details
ETH_TXP, ETH_TXN, ETH_RXP, ETH_RXN	Ethernet transmit and receive differential signals
BITFAST~	BIT fast start signal
COM1_TX, COM1_RX, COM2_TX, COM2_RX	2-wire (transmit and receive) serial Communications ports
FLPRGEN~	FLASH Program Enable signal
AD0 to AD31	**Address/Data bits.** Multiplexed address and data bus
C_BE0 to C_BE3	**Command/Byte Enables.** During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase, the signals are byte enables that specify the active bytes on the bus
FRAME~	**FRAME.** Driven low by the current master to signal the start and duration of an access
DEVSEL~	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	**Parity.** Parity protection bit for AD0 to AD31 and BE0 to BE3
IRDY~	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase
LOCK~	**LOCK.** Driven low to indicate an atomic operation that may require multiple transactions to complete
RESET~	**Reset.** Driven low to reset the PCI bus
TRDY~	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase
PERR~	**Parity Error.** Driven low by a PCI agent to signal a parity error
SERR~	**System Error.** Driven low by a PCI agent to signal a system error
STOP~	**STOP.** Driven low by a PCI target to signal a disconnect or target-abort
INTA~ to INTD~	**Interrupt lines.** Level-sensitive, active-low interrupt requests
CLK	**Clock.** All PCI bus signals except RESET~ are synchronous to this clock
REQ~	**Request.** Driven low by a PCI agent to request ownership of the PCI bus
GNT~	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	**Initialisation Device Select.** Device chip select during configuration cycles
NC	**No connection**
GND	The DC voltage reference for the system
CLK1 to CLK4	Backplane clocks provided by PPzero Master
REQ1~ to REQ4~	Backplane bus requests to PPzero Master arbiter
GNT1~ to GNT4~	Backplane bus grants from PPzero Master arbiter

JTAG CPU Emulator Connectors (P11 and P12)

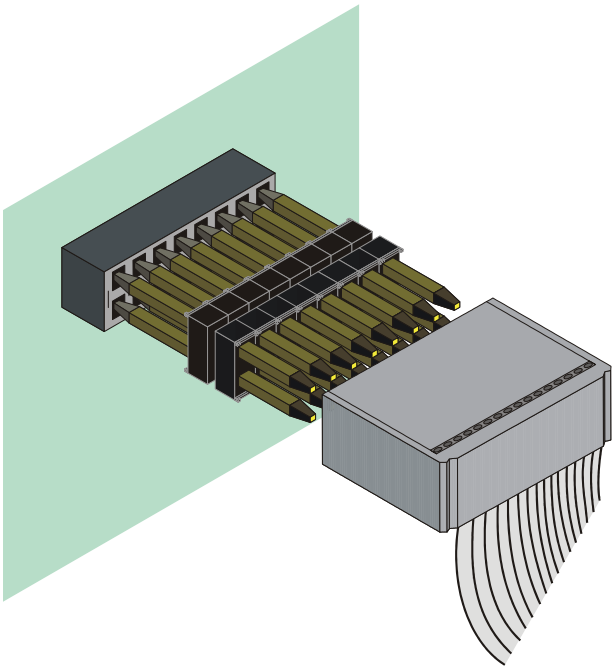
P11 provides connection between CPU1 and a JTAG CPU emulator. P12 provides a similar connection for CPU0. P11 and P12 both have the following pinout:

Pin	Signal	Pin	Signal
1	TDO	2	QACK~
3	TDI	4	TRST~
5	QREQ~	6	VIO
7	TCK	8	CHECKSTOP_IN~
9	TMS	10	No Connection
11	SRESET~	12	GND
13	HRESET~	14	No Connection
15	CHECKSTOP_OUT~	16	GND

An example of a suitable JTAG CPU emulator is a WindRiver VisionProbe supporting 2.5V signaling. HRESET~ generation must be set for open collector.

If 2 VisionProbes are being used, HRESET~ on one of the units must be disabled, as a falling edge on either HRESET~ resets the whole board.

Note: The PPCM1 is shipped with loose headers suitable for connecting P11/P12 to a JTAG CPU emulator as shown below.



Transition Modules

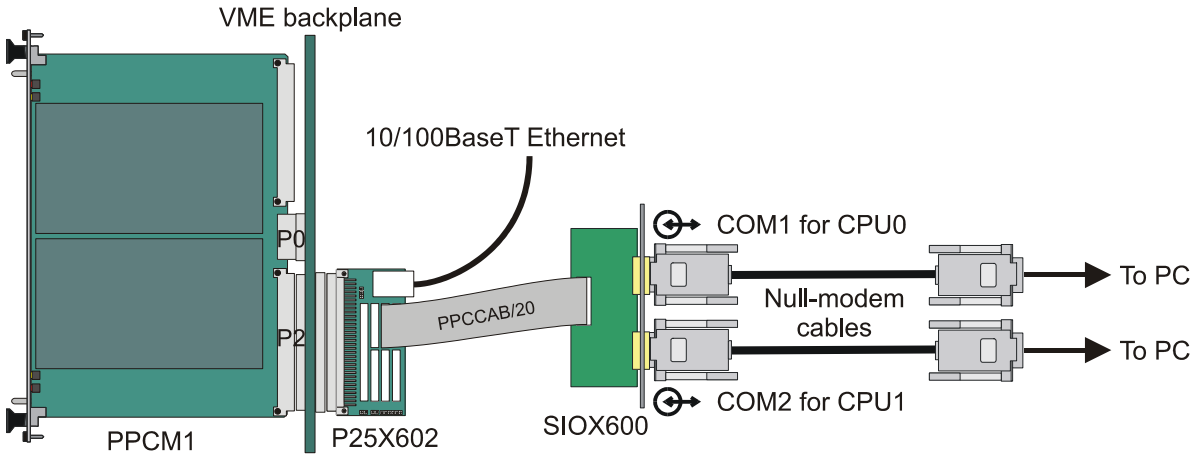
This section describes the available transition modules for the PPCM1. It should be read in conjunction with the I/O Module Installation Guide, publication number RT5154.

There are three transition modules for the PPCM1:

- For the 'Compatibility' pinout (see I/O Options)
  - P25X602 is the transition module for use with P2
- For the 'XtraPower' pinout (see I/O Options)
  - P25X603 is the transition module for use with P2
  - P0M1 is the transition module for use with P0

These modules are described in more detail in the following sections.

Compatibility Pinout

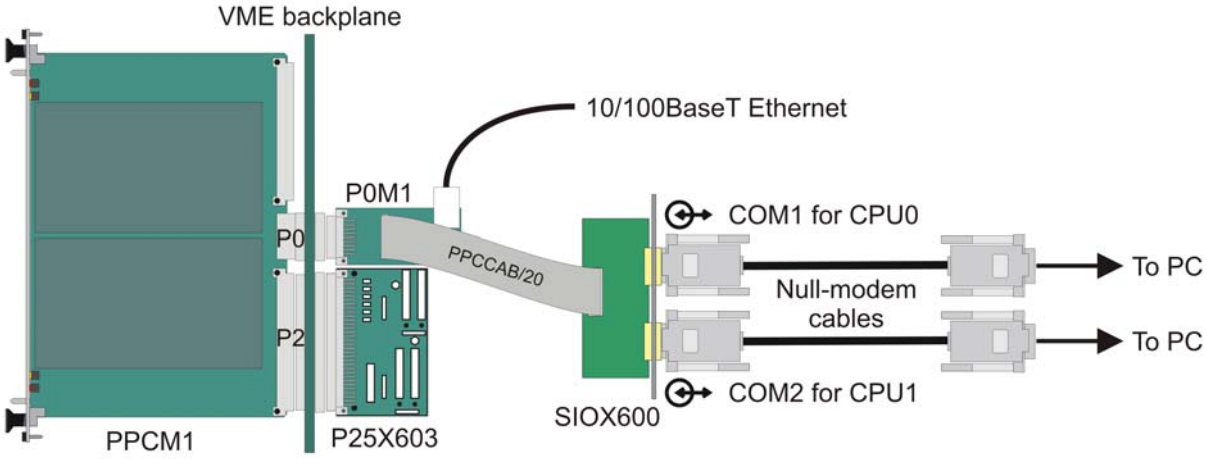


P25X602 provides

- 10/100BaseT Ethernet (RJ45 connector)
- COM1 and COM2
- Pins for P2 rows z and d PMC I/O signals

See the I/O Module Installation Guide, publication number RT5154, for more details.

XtraPower Pinout



P0M1 provides:

- 10/100BaseT Ethernet (RJ45 connector)
- COM1 and COM2
- BITFASTSTART~ and FLASHPROGENABLE~ links/headers
- Pins for P0 PMC I/O signals

See the P0M1 section for more details.

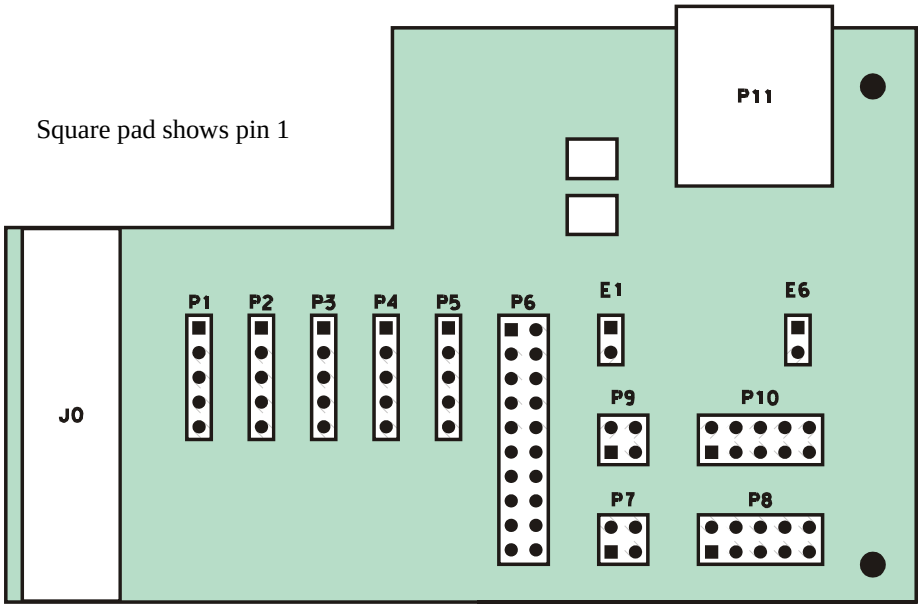
P25X603 provides (depending on the pinout option selected):

- Pins for P2 rows z and d PMC I/O signals
- Pins for P2 rows a and c PMC I/O signals
- BITFASTSTART~, OFFLINE~, SYSFAIL~, EXTRESET~, EXTABORT0~ and EXTABORT1~ signal links/headers

See the P25X603 section for more details.

P0M1

P0M1 is available with sales code P0M1-11 (level 1 build style) or P0M1-21 (level 2 build style). It has the following layout:



P11 is an RJ45 connector that provides 10/100BaseT Ethernet.

E1 provides the BITFASTSTART~ signal (on pin 1, GND on pin 2). Fit the link to make the signal active (low).

E6 provides the FLASHPROGENABLE~ signal (on pin 1, GND on pin 2). Fit the link to make the signal active (low).

P1 to P5 provide the PMC1_IO 47 to 52, 55 to 59 and 61 to 64 (Fibre Channel) signals as follows:

Pin	P1	P2	P3	P4	P5
1	0V	PMC1_IO50	PMC1_IO48	PMC1_IO52	+5V
2	0V	PMC1_IO49	PMC1_IO47	PMC1_IO51	No Connection
3	0V	PMC1_IO62	PMC1_IO59	PMC1_IO61	+3.3VPCI
4	0V	PMC1_IO56	PMC1_IO64	PMC1_IO58	No Connection
5	0V	PMC1_IO55	PMC1_IO63	PMC1_IO57	0V

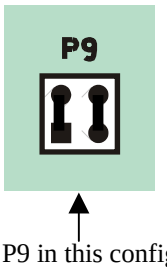
P6 provides a connector compatible with P25X602 (and associated cabling) to give connections for COM1 and COM2, as follows:

Pin	Signal	Pin	Signal
1	No Connection	2	No Connection
3	No Connection	4	No Connection
5	COM1TX	6	COM1RX
7	No Connection	8	No Connection
9	No Connection	10	No Connection
11	No Connection	12	No Connection
13	COM2TX	14	No Connection
15	No Connection	16	COM2RX
17	No Connection	18	No Connection
19	0V	20	0V

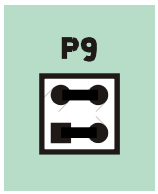
Note: The above pinout requires a null modem cable.

To allow a 1:1 cable to be used for connection to a PC, the P0M1 should be configured to provide a null modem on-board. P7 and P9 allow the COM2 and COM1 Rx/Tx signals respectively to be swapped, with the swapped signals being available on P8/P10 or P6.

P9 allows COM1 Tx and Rx to be swapped, as follows (the square pad shows pin 1):



P0M1 provides null modem



Normal connection (requires null modem cable)

With P9 in this configuration, COM1 is available as follows:

P10

PIN	SIGNAL	PIN	SIGNAL
1	No Connection	2	No Connection
3	COM1RX	4	No Connection
5	COM1TX	6	No Connection
7	No Connection	8	No Connection
9	0V	10	No Connection

P6

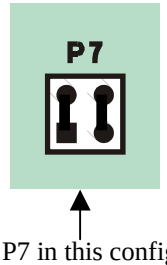
PIN	SIGNAL	PIN	SIGNAL
1	No Connection	2	No Connection
3	No Connection	4	No Connection
5	COM1RX	6	COM1TX
7	No Connection	8	No Connection
:	:	:	:

This allows a 1:1 cable to be used to connect to a 9-way D-type connector for connection to a PC.

Notes:

1) Use P10 *or* P6, **not** both.
2) If no links are fitted to P9, serial interface connections will not be available on P10 or P6.

P7 allows COM2 Tx and Rx to be swapped, as follows (the square pad shows pin 1):



P0M1 provides null modem



Normal connection (requires null modem cable)

With P7 in this configuration, COM2 is available as follows:

P8

PIN	SIGNAL	PIN	SIGNAL
1	No Connection	2	No Connection
3	COM2RX	4	No Connection
5	COM2TX	6	No Connection
7	No Connection	8	No Connection
9	0V	10	No Connection

P6

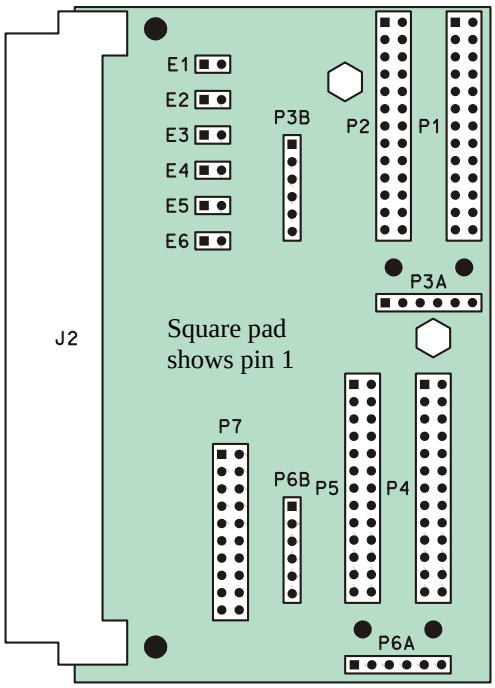
PIN	SIGNAL	PIN	SIGNAL
9	No Connection	10	No Connection
11	No Connection	12	No Connection
13	COM2RX	14	No Connection
15	No Connection	16	COM2TX
:	:	:	:

This allows a 1:1 cable to be used to connect to a 9-way D-type connector for connection to a PC.

Notes:

1) Use P8 *or* P6, **not** both.
2) If no links are fitted to P7, serial interface connections will not be available on P8 or P6.

P25X603



Links E1 to E6 provide connection to various signals on P2 rows z and d, as follows:

Link	Pin 1		Pin 2
	CPU Signals	PMC1 I/O	
E1	BITFASTSTART~	PMC1_IO41	GND
E2	OFFLINE~	PMC1_IO44	5V
E3	SYSFAIL~	PMC1_IO46	5V
E4	EXTRESET~	PMC1_IO42	GND
E5	EXTABORT0~	PMC1_IO43	GND
E6	EXTABORT1~	PMC1_IO45	GND

Note: Take care when fitting links, as the signal available at pin 1 of the link depends on the P2 pinout option.

OFFLINE~ and SYSFAIL~ are driven low via 220Ω resistors to drive LEDs connected between the signal and +5V.

P1

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PMC1_IO40	4	PMC1_IO42
5	PMC1_IO38	6	PMC1_IO41
7	PMC1_IO44	8	PMC1_IO46
9	NC	10	NC
11	PMC1_IO34	12	PMC1_IO36
13	PMC1_IO37	14	PMC1_IO39
15	PMC1_IO32	16	PMC1_IO35
17	PMC1_IO20	18	PMC1_IO23
19	PMC1_IO14	20	PMC1_IO17
21	PMC1_IO26	22	PMC1_IO29
23	PMC1_IO31	24	PMC1_IO33
25	GND	26	GND

P2

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PMC1_IO22	4	PMC1_IO24
5	PMC1_IO25	6	PMC1_IO27
7	PMC1_IO28	8	PMC1_IO30
9	NC	10	NC
11	PMC1_IO13	12	PMC1_IO15
13	PMC1_IO19	14	PMC1_IO21
15	PMC1_IO16	16	PMC1_IO18
17	PMC1_IO4	18	PMC1_IO6
19	PMC1_IO1	20	PMC1_IO3
21	PMC1_IO10	22	PMC1_IO12
23	PMC1_IO7	24	PMC1_IO9
25	GND	26	GND

P3A and P3B

Pin	Signal
1	PMC1_IO2
2	PMC1_IO5
3	PMC1_IO8
4	PMC1_IO1
5	PMC1_IO43
6	PMC1_IO45

P4

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PMC0_IO40	4	PMC0_IO42
5	PMC0_IO38	6	PMC0_IO41
7	PMC0_IO44	8	PMC0_IO46
9	NC	10	NC
11	PMC0_IO34	12	PMC0_IO36
13	PMC0_IO37	14	PMC0_IO39
15	PMC0_IO32	16	PMC0_IO35
17	PMC0_IO20	18	PMC0_IO23
19	PMC0_IO14	20	PMC0_IO17
21	PMC0_IO26	22	PMC0_IO29
23	PMC0_IO31	24	PMC0_IO33
25	GND	26	GND

P5

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PMC0_IO22	4	PMC0_IO24
5	PMC0_IO25	6	PMC0_IO27
7	PMC0_IO28	8	PMC0_IO30
9	NC	10	NC
11	PMC0_IO13	12	PMC0_IO15
13	PMC0_IO19	14	PMC0_IO21
15	PMC0_IO16	16	PMC0_IO18
17	PMC0_IO4	18	PMC0_IO6
19	PMC0_IO1	20	PMC0_IO3
21	PMC0_IO10	22	PMC0_IO12
23	PMC0_IO7	24	PMC0_IO9
25	GND	26	GND

P6A and P6B

Pin	Signal
1	PMC0_IO2
2	PMC0_IO5
3	PMC0_IO8
4	PMC0_IO1
5	PMC0_IO43
6	PMC0_IO45

P7

Pin	Signal	Pin	Signal
1	PMC_IO47	2	PMC_IO48
3	PMC_IO49	4	PMC_IO50
5	PMC_IO51	6	PMC_IO52
7	PMC_IO53	8	PMC_IO54
9	PMC_IO55	10	PMC_IO56
11	PMC_IO57	12	PMC_IO58
13	PMC_IO59	14	PMC_IO60
15	PMC_IO61	16	PMC_IO62
17	PMC_IO63	18	PMC_IO64
19	GND	20	GND

Front Panel

Air-cooled Versions

PMC Slots

There are two PMC slots in the front panel. However, if you have not ordered PMCs for the sites, then Radstone will fit a blanking plate in the slot(s) for EMC protection.

If you are fitting a non-Radstone PMC, it must comply with the P1386.1 standard for air-cooled PMCs to ensure that it mates correctly with the PPCM1 mechanics. Radstone PMCs comply with the standard.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel should fill the slot and may provide front panel connection to the module. Radstone PMCs are delivered with a full kit of parts for mounting them plus fitting instructions.

LEDs

There are 8 LEDs mounted on the front panel, in two groups of four (one group per node). Each group has one red, one green and two amber LEDs. See the LEDs section for more details.

Switches

There are two momentary action toggle switches fitted - one per node. These allow generation of a hard reset or aborts to the corresponding processor. With the board in the orientation as shown in Figure A-4, moving the bottom switch to the left ("S" position) causes an abort to CPU0, and moving the switch to the right ("H" position) causes a hard reset. Moving the top switch to the left ("S" position) causes an abort to CPU1.

The switches may be disabled under software control, via bit D24 of the appropriate PLD Register for the CPU. Software control is enabled following power-up.

Additional reset sources (both hard and soft) may be found on the P0 or P2 connector (depending on the I/O options).

Conduction-cooled Versions

PMC Slots

There are two conduction-cooled PMC slots in the front panel, allowing limited access to PCI signals.

If you are fitting a non-Radstone PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the PPCM1 mechanics. This will be the case for Radstone PMCs.

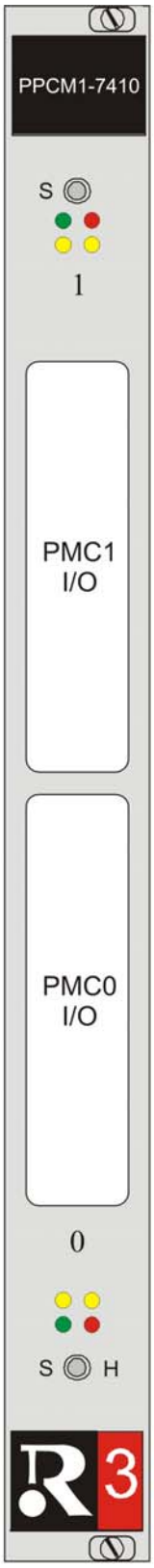
LEDs

There are 8 LEDs mounted on the front panel, in two groups of four (one group per node). Each group has one red, one green and two amber LEDs. See the LEDs section for more details.

Switches

There are no switches on the conduction-cooled front panel, although external reset inputs are available on the P0 or P2 connector (depending on the I/O options).

Figure A-4. Front Panels



Air-cooled
front panel



Conduction-cooled
front panel

Troubleshooting

As well as the general troubleshooting suggestions, there follow some suggestions that are specific to the PPCM1:

- The suggested link configuration gives operation as system controller, so if you are using the PPCM1 in its suggested configuration, ensure that the board is the leftmost position in the rack (usually slot 1) and that no other boards are also configured as system controllers
- If you are having problems programming the FLASH, then check that the appropriate area write enable links (E5, E6, E7 or E8) are fitted, the global write enable link (E11) is fitted (or the FLPRGEN~ signal on the P0 connector is pulled low), and the appropriate bit of the PLD Register for the CPU is set. See the FLASH section and the E5, E6, E7, E8 and E11 descriptions for more details

Note: The BANC area of FLASH is not writeable.

Specifications

Processors:	2 x PowerPC 7410s at 500 MHz.
SDRAM:	Up to 512 Mbytes with EDC per processor (up to 1 Gbyte total) on board.
L2 Cache:	2 Mbytes per processor (4 Mbytes total). Private L2 cache bus.
FLASH:	64 Mbytes of 32-bit wide, on-board programmable FLASH per processor.
RTC:	Backed up by connection to VMEbus 5VSTDBY pin.
User EEPROM:	32 Kbytes.
PCI:	64-bit, 33 MHz internal bus; two 64-bit, 66 MHz PMC buses.
Ethernet:	10/100BaseT via the P0/P2 connector.
PMC Sites:	Air-cooled: Two 3.3V or 5V, 64-bit, 66 MHz IEEE P1386.1 compliant slots with front panel and P0 I/O, and restricted P2 I/O. Conduction-cooled: Two 3.3V or 5V, 64-bit, 66 MHz rugged PMC compliant slots with P0 I/O, restricted P2 I/O and limited front panel I/O. User selectable 3.3V or 5V signaling voltage to PMCs. 3.3V power generated on-board
Serial I/O:	Two PC-style COM ports via the P0/P2 connector.
Counter/Timers:	Eight independent 32-bit counter/timers with a resolution of 10ns at 100 MHz bus speed. Two timers may be linked to form a 64-bit counter/timer.
Front Panel I/O:	PMC I/O for Levels 1 to 3. Levels 4 and 5 have limited front panel I/O for PMCs with the appropriate layout, and connector size and location.
Status LEDs:	Two groups of 4 LEDs, front panel mounted on all levels.
Reset switches:	Two, front panel mounted on levels 1 to 3. Not present on levels 4 or 5.
Operating Systems:	VxWorks/Tornado
PCI Expansion:	PCI through P0 using Radstone PPzero technology.
Weight:	700g for levels 1 to 3 and 800g for levels 4 and 5

Power Requirements

Main Power

The PPCM1-7410 with 512 Mbytes of SDRAM, 64 Mbytes of FLASH and 2 Mbytes of L2 cache typically requires 6A from the +5V +5%, -2.5% supply.

As the current trend for processors is for the core voltage and power consumption to drop with successive generations, the overall PPCM1 power consumption will change as the CPU power consumption changes.

The PPCM1 does not use the ±12V supply lines, but they do feed the PMC sites.

Note: When using PMCs, ensure that they do not cause the specified maximum supply current to be exceeded, especially from the +5V and +3.3V supplies. The VME specification allows a maximum of 1 Amp to be drawn from each +5V supply pin (9 pins in total) in a single slot over the PPCM1's specified operating temperature range. It may not be possible to support all combinations of SDRAM and PMCs within this limit.

The PPCM1 uses the undefined pins (rows a, c, d and z) of the VMEbus P2 connector for I/O and power/ground connections.

WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components

CAUTION

Only use the PPCM1 in backplanes that supply power on both the J1 and J2 connectors

Real Time Clock Backup

Power to the Real Time Clock on the PPCM1 is fed from +5VSTDBY and +5V on the VMEbus. Whichever of these two supplies has the greater voltage provides the supply in normal operation (i.e. current may be drawn from the +5VSTDBY line even when +5V is powered). The supply is provided by +5VSTDBY when the +5V supply is not present. VME compliance requires the +5VSTDBY supply to be 5V +5% -2.5%, however the PPCM1 can operate with a standby voltage in the range 2.5 to 5.25V. This allows the standby voltage to be supplied by a battery, although in this case it is a safety requirement of the user to make sure that that battery cannot be charged from the +5VSTDBY rail. If operation of the Real Time Clock is not required when the main supplies are powered down, no connection is required on +5VSTDY.

On power-down, the RTC circuit may draw up to 800 µA for 1 second. After that it typically draws <100 µA.

Reliability (MTBF)

The following table shows the calculated Mean Time Between Failures for the PPCM1-7410-xC10D0x:

Environment	Fail Rate (Failures Per Million Hours)	Mean Time Between Failures (Hours)
Ground Benign 30°C	5.3441	187,122
Ground Fixed 40°C	13.85487	72,177
Ground Mobile 45°C	25.65703	38,976
Naval Sheltered 40°C	22.63474	44,180
Naval Unsheltered 45°C	36.8356	27,148
Airborne Inhabited Cargo 55°C	33.1116	30,201
Airborne Inhabited Fighter 55°C	39.38783	25,389
Airborne Uninhabited Cargo 70°C	52.82361	18,931
Airborne Uninhabited Fighter 70°C	77.59914	12,887
Airborne Rotary Wing 55°C	54.08244	18,490
Space Flight 30°C	5.120218	195,304
Missile Flight 45°C	33.46993	29,878
Missile Launch 55°C	74.63196	13,399

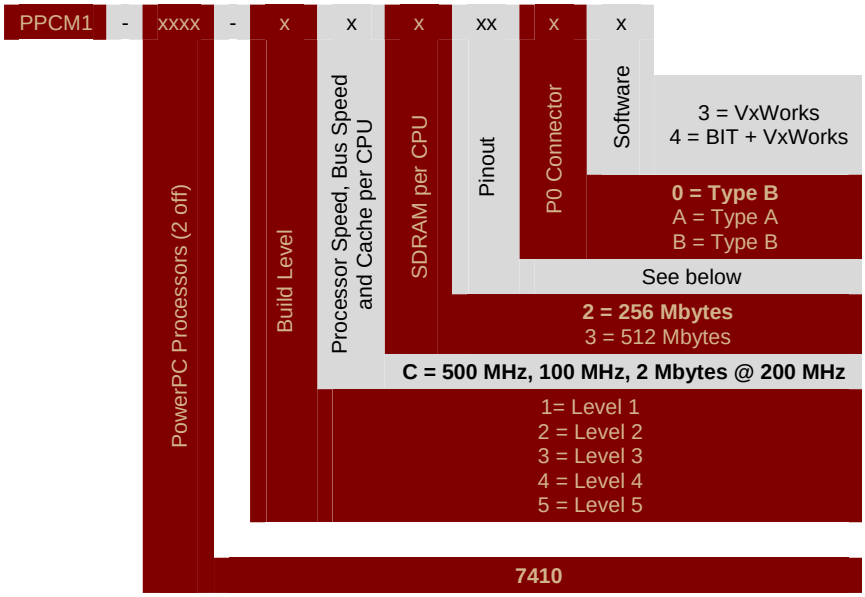
These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted PMCs.

The failure rates used in this calculation are based on MIL-HDBK-217F Notice 1 with commercial or non-military quality level. Where a component did not comply with the MIL-HDBK, the closest equivalent, compliant component was used.

See the Product Codes section for more details on the meaning of the product code.

Product Codes

The product code is specified as follows:



xx	PPzero	PMC0 I/O	PMC1 I/O	Comms Signals	BIT Master Signals	Pinout
0B	32	64	40	P0	P2 z/d	XtraPower
0D	32	64	46	P0		XtraPower
0F	32		40	P2 a/c	P0	Compatible
2B		64	40	P0	P2 z/d	XtraPower
2D		64	46	P0		XtraPower
2F			40	P2 a/c	P0	Compatible

All other items, such as 64 Mbytes of FLASH per CPU, 10/100BaseT Ethernet, 2 x RS232 serial ports, 2 PMC slots, 5-row P1 and P2 connectors etc. are standard.

The default product code is PPCM1-7410-xC20D0x (where x = any), as highlighted above.

Software Support

A VxWorks/Tornado BSP (XPBSP-TORxxx) is available as standard. A VxWorks ESP with PPzero support (XPESPZ-TORxxx) will be available soon.

BIT for the XtraPower range is available (XPBIT-xxx).

Please contact Radstone for more details on these or availability of support for other operating systems.

I/O Modules (3U)

For use with chassis, Radstone offers backplane transition modules to convert the condensed P2 and P0 pinouts to industry-standard formats, plus 3U breakout panels offering a variety of industry standard connectors such as Serial I/O and 10/100BaseT. Internal cables and a basic set of external cables are available. These transition and I/O modules are intended for development use in a benign environment, and so are only available in level 1 or 2 build standards.

For more details see the Transition Modules section and the I/O Module Installation Guide, publication number RT5154.

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