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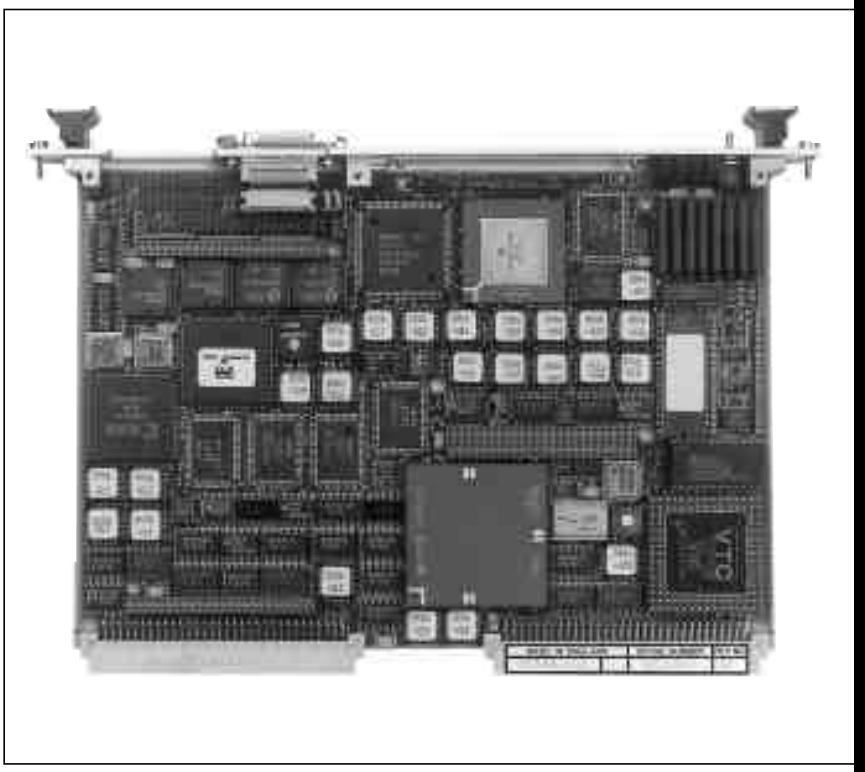
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68-41/68-42

68040/68020 Dual Processor Single Board Computers



Radstone's 68-41 and 68-42 are 68040-based single board computers that maximize real-time performance in VMEbus systems through the use of a dual processor architecture. 68-41 and 42 fully utilize the RISC-like performance of the 68040 processor, while integrating the high level of I/O functionality demanded for high performance real-time systems. Software investment is guaranteed by maintaining code compatibility throughout the 68000 family of processor devices.

Both boards combine the processing power of Motorola's 68040, with up to 36 Mbytes of RAM, on-board SCSI, Ethernet and APEX interfaces, plus four serial ports, all under the control of a dedicated 68020 acting as an intelligent I/O processor.

The 68-41 features a VSB interface, allowing concurrent data transfers over VME and VSB. For systems not requiring VSB, the 68-42 provides a software compatible platform that uses the P2 user-defined pins for I/O connections. A range of transition modules is available to convert P2 inputs/outputs to industry standard connectors.

Extensive software support includes UNIX System V, VRTX32, Velocity, VxWorks, OS-9 and other leading real-time operating systems and kernels. On-board firmware includes hardware drivers and I/O management functions in a BIOS PROM, providing system developers with a comprehensive software environment.

The highly segmented "Freeflow" architecture of the 68-41/42 uses multiple internal and external data paths under the control of independent processors, thereby avoiding the I/O and bus transfer conflicts often found in I/O intensive single board designs. This multiple data path architecture allows real-time transfers across the VMEbus and, in the case of the 68-41, VSB to run concurrently with on-board I/O operations, without adversely affecting the performance of the main processor.

Real-time performance is maximized by offloading the management of peripheral interfaces such as SCSI, Ethernet and serial ports (plus additional user defined functions via the built in APEX interface), to the on-board 68020 I/O processor. Up to 4 Mbytes of dedicated local RAM is available to the 68020 for I/O operations and buffer space.

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Key Features

- 68040 based SBCs for VME/VSB systems (VSB on 68-41 only)
- 68040 processor at up to 40 MHz
- Up to 36 Mbytes of distributed multi-port RAM
- 68020-based I/O subsystem
- SCSI and Ethernet interfaces with built-in DMA
- Four RS232C serial ports with RS422/RS485 options
- Technology independent memory module with byte parity
- Advanced Processor Extension (APEX) interface
- Six 16 bit timers
- Real-time clock
- 2 Kbytes of battery backed SRAM
- Two 32 pin JEDEC sites for EPROM
- VIC068 VMEbus interface at up to 40 Mbytes/sec
- VSB master/slave interface with DMA at up to 30 Mbytes/sec (68-41 only)
- BIOS firmware
- Freeflow architecture for maximum data throughput

68040

The 68040 is a virtual memory 32 bit microprocessor employing multiple concurrent execution units. Its highly integrated architecture provides an exceptional level of performance from a monolithic HCMOS device. In performance terms, this equates to up to 20 MIPS and over 3.5 MFLOPS at 25 MHz. 33MHz devices enable even higher levels of performance to be achieved.

The 68040 consists of multiple execution units that operate autonomously. Multiple internal buses and execution pipelines allow integer unit, FPU, MMU and bus controller operations to occur concurrently, enabling maximum throughput to be achieved.

Central to this is an integer unit that provides single cycle execution of a set of commonly used instructions, and results in an average of 1.3 clocks per instruction.

Independent 4 Kbyte instruction and data caches allow the processor to operate at maximum performance using fast, high capacity DRAM. Cache burst fill allows a fast access DRAM mode, such as static column, to be used. Information is fetched in bursts of 4 longwords, i.e. 16 bytes, which requires only a single processor bus (Pbus) arbitration cycle.

Memory Module

A technology independent memory interface on the 68-41/42 board accepts a plug-in module providing DRAM, SRAM or EEPROM. This memory is directly accessible by the 68040 processor, I/O subsystem, VMEbus and VSB (68-41) via the board's 57 Mbytes/sec synchronous bus. Memory capacities from 4 to 32 Mbytes are available as standard, with battery backup and parity options available. This modular approach enables the price/performance of the board's main memory to be matched to the requirements of a particular application, by allowing selection of the optimum memory technology, capacity and speed. Field upgrades allow new memory devices to be adopted as they become available.

Cache burst fill mode, essential for maximum 68040 performance, is fully supported by Radstone's memory modules. This gives a performance of (4,1,1,1) clock cycles for a fully populated DRAM array.

EPROM

Two 32 pin JEDEC sites accept standard 8 bit wide PROM or EPROM devices up to 2 Mbytes total capacity. Custom Datapath ASICs enable the 68040 to access 8 bit devices. The 68-41/42 can automatically transfer EPROM code to the 68040 DRAM module for optimum performance.

One JEDEC site is always available for user firmware; the second site is normally reserved for system firmware such as CIOS or PLUM.

Gateway ASIC

Fabricated using 1.5 micron CMOS technology, the Gateway ASIC couples the synchronous 68040 bus to the asynchronous I/O and VME buses. The ASIC is clocked synchronously with the processor clock and is capable of speeds of up to 40 MHz. The Gateway ASIC enables the 68040 to snoop synchronous local bus accesses as well as VME or VSB transfers to Pbus memory. This is essential for multiprocessor systems that communicate using VME or VSB shared memory locations.

Datapath ASIC

Two Datapath ASICs each provide 32 bit bi-directional latching buffers to handle byte alignment and byte swapping functions. The ASIC translates unaligned 8 and 16 bit accesses into transfers suitable for the 68040. This allows the 68040 to directly address 8 or 16 bit I/O devices and to support D08 and D16 VMEbus cycles.

Configuration

Hardware links are used only where essential on the 68-41/42. Many functions, including VME and VSB addressing, are software configurable. The 68-41/42 includes 512 bytes of EEPROM to retain board configuration details.

68-41/42 I/O System

A 68020 processor at 20 MHz and 1 or 4 Mbytes of local memory is provided on the 68-41/42 to interface with SCSI, Ethernet, serial and APEX interfaces directly. Acting as a dedicated I/O processor, the 68020 relieves the 68040 of many time-critical local interrupt and data manipulation overheads.

68020

The 68020 I/O processor significantly reduces the number of interrupts reaching the 68040. Local interrupt processing can represent a very large overhead; four serial channels alone can easily represent 5000 interrupts per second at peak rate. Off-loading interrupt handling to the 68020 and allowing the 68040 to process blocks of characters can reduce this overhead to less than 1% overall.

Complex tasks such as Ethernet protocol handling or serial bit-oriented operations can also be offloaded from the 68040, freeing up the main CPU for applications processing.

Ethernet

The on-board Ethernet interface uses the AM79C900 ILACC device, which combines the functionality of the industry-standard LANCE controller and its Serial Interface Adaptor in a single package. The interface is fully compatible with Ethernet 2.0 and IEEE 802.3 10Base5 specifications.

A second Ethernet interface can be added using an APEX-100 plug-in module to support dual-redundant networking.

The on-board CIOS firmware provides full support for Ethernet, including TCP/IP protocols.

SCSI Interface

The on-board SCSI interface is provided by the NCR 53C700 SCSI controller, which incorporates a SCSI SCRIPTS processor. The controller handles the phase-by-phase management of the SCSI bus directly, and results in a significant reduction in latency. The device carries out complex SCSI bus sequences without interrupts. The interface adopts the same high level command interface as used on Radstone's range of stand-alone SCSI controllers.

The single-ended interface executes synchronous transfers at up to 6.25 Mbytes/sec or asynchronous transfers at up to 5 Mbytes/sec.

An on-chip 32 byte FIFO and DMA controller supports burst mode transfers to memory.

The on-board CIOS firmware provides full SCSI Common Command Set (CCS) support and SCSI-2 features such as command tagging and queuing.

Serial I/O

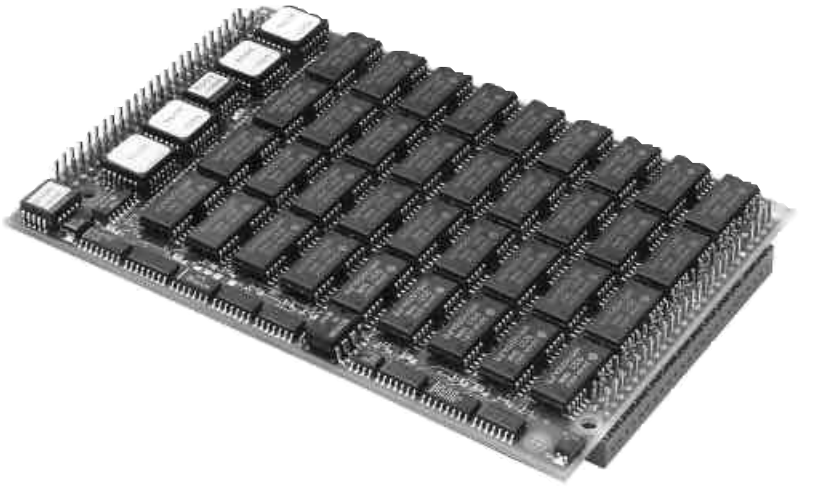
Four serial ports are provided, driven by two Z85C30 Enhanced Serial Communications Controllers. Two ports support RS232C or asynchronous operation with data rates of up to 2.048 Mbits/sec. HDLC, SDLC, X.25 or BISYNC operations can also be supported with appropriate software. The other two ports support RS232C asynchronous mode only. Each port can be individually configured, with custom serial protocols or line discipline routines handled by the 68040 or 68020 as required.

Real-time Clock

This has year, month, day, hours, minutes and seconds. There is integral battery backup with automatic fail write protection, plus 2 Kbytes of battery-backed SRAM.

Counter/Timers

Two 85C36 Counter/Timer and I/O (CIO) devices provide six independent software programmable 16 bit timers with 400ns resolution.



Technology independent memory module

These can be programmed to operate as six 16 bit timers, or two 16 bit and two 32 bit timers.

APEX

The 32 bit Advanced Processor Extension (APEX) interface enables easy tailoring of the 68-41/42 to meet application specific requirements. Extra functionality can be added using plug-in modules, while still occupying a single VME backplane slot. A range of standard modules are available including SCSI, floppy disk controller, IEEE-488, parallel I/O and Ethernet.

Interrupts

Interrupts from the serial channels, SCSI, Ethernet and APEX are routed to the 68020 processor. This allows autonomous operation of the I/O subsystem, and enables it to work on behalf of either the 68040 or an external VMEbus master. All other interrupts are routed to the 68040. Mailbox interrupts may be used to allow communication between the 68020 and 68040 processors.

The I/O Subsystem bus (IObus) has many potential bus masters. Arbitration for the bus is done on a priority basis in the order VMEbus (highest priority), Ethernet, SCSI, APEX, 68040 gateway and 68020. This resolves deadlock situations and provides optimum performance with this mix of bus masters. A Release When Done (RWD) mechanism is employed, returning control to the 68020 after another master has used the IObus.

Multiple DMA

The 68-41/42 board has multiple DMA controllers - the VIC068, the VSIC (68-41 VSB interface), the Ethernet controller, the SCSI controller, the 68020 and potentially, an APEX-based controller. The Gateway ASIC also enables the 68020 to DMA data at up to 10 Mbytes/sec.

Front Panel LEDs

Eight LEDs, visible through the board's front panel, provide the systems integrator (or user) with a convenient overview of the board's current mode of operation. Four of the LEDs indicate:

- Pbus Halt
- Power OK
- VMEbus master/slave status
- VSB master/slave status

The remaining four LEDs are software programmable.

VMEbus Interface

A VIC068 VMEbus interface controller provides a complete VMEbus interface with block transfer DMA at up to 40 Mbytes/sec, VMEbus requester with fairness option, interrupter, four level arbiter, seven level interrupt handler and interprocessor communication registers. The device fully conforms to the IEEE 1014 and VMEbus Revision D specifications.

The VIC068 provides eight interprocessor communication registers, four location monitors (mailboxes), four broadcast location monitors and remote reset. These enable specific processors to be addressed or a message to be passed simultaneously to a group of processors.

Efficient bus arbitration and minimal latency are key features of the VIC068 and are particularly important when building high performance multiprocessor systems.

The 68-41/42 includes a full master/slave interface to the VMEbus, supporting read and write operations to both on-board memory areas. The board's address range for slave mode VME accesses is software programmable. The 68040 processor provides VME interrupt services.

VME Subsystem Bus (VSB)

(68-41 only)
The VME Subsystem Bus (VSB) provides a full 32 bit expansion bus, and can be used for multiprocessing, for memory expansion or to increase total available bus bandwidth. It can also be used to connect intelligent I/O controllers, freeing the VMEbus for higher level inter-processor or global transfers within a multiprocessor implementation.

The 68-41 provides a direct interface to the VSB for the 68040 processor and its memory module. The interface uses Radstone's VSIC (VSB Interface Controller) incorporating the following features:

- VSB master/slave interface with block transfer support
- Software programmable address map
- ROR Bus requester for reduced bus arbitration overhead
- DMA controller up to 30 Mbytes/sec

Multiprocessing Support

The 68-41/42 is ideally suited to high performance, real-time multiprocessing configurations, with its dual processor, dual bus architecture, VME and VSB interfaces and the VIC068 controller.

SOFTWARE

The 68-41/42 is widely supported with a broad range of real-time and development software available both from Radstone and from independent software vendors.

Industry-standard software support includes OS-9, VRTX32, Velocity, VxWorks, pSOS and ADA. For real-time development under UNIX, Radstone has developed VXCEL, an integrated UNIX/VRTX environment. Further details on operating systems and software can be found in Radstone's Commercial and Industrial products shortform catalogue.

Software portability is a key feature of the 68-41/42, with the on-board CIOS firmware providing complete device driver and software interface support. This ensures that any necessary software or porting is very straightforward, yet still takes full advantage of the advanced architecture of the 68-41/42 board.

Concurrent I/O Server (CIOS)

The 68-41/42 is supplied with a modular BIOS-style firmware package that provides I/O services, Ethernet protocols, SCSI management and all software driver interfaces for the board. These facilities are provided by the Concurrent I/O Server (CIOS), which runs on the 68020 processor. CIOS operates concurrently with any other software or operating system on the 68040.

68-41/42 CIOS is software compatible with existing Radstone VME processor and I/O designs such as the ENET-1 and SCSI-11, so existing software and development effort is preserved. As a completely independent subsystem running on the 68020, CIOS can be driven not only from the on-board 68040 processor, but also by other VME boards over VME or VSB buses.

For real-time systems, CIOS can be used to relieve the 68040 from the overhead of I/O operations, allowing the 68040 to be dedicated to time-critical processing and control functions.

CIOS allows individual firmware modules to be enabled or disabled, and additional modules to be downloaded, for example, to support the APEX interface. The required configuration is permanently retained in non-volatile memory. CIOS is supplied together with the PLUM monitor in a single EPROM device.

CIOS provides both link-level access and TCP/IP protocols for the 68-41/42 board. Compliant with the US DoD TCP/IP open communications standards CIOS provides TCP, UDP, IP, ICMP, ARP, TFTP, SLIP and link-level access protocols with both BSD 4.3 sockets and UNIX streams libraries.

Built in TFTP and BOOTP services mean that compiled object code can be simply downloaded over Ethernet from any suitable networked host computer.

The 68-41/42 CIOS is fully compatible with T-Stream TCP/IP on Radstone's ENET-1 and EMPP-1 VME Ethernet controllers. An additional source code package is available to provide Telnet, FTP, rlogin and Berkeley utilities.

PLUM

PLUM is the resident EPROM-based universal monitor for Radstone VME processors. It provides monitor, debugger and bootstrap facilities, and enables memory and local resources to be accessed directly from a terminal connected to one of the board's serial ports. PLUM is written in C, and the extensive range of PLUM functions can be called from the user's application.

PLUM for the 68-41/42 runs on both the 68040 and 68020 processors.

Diagnostics

Comprehensive on-board diagnostics provide power-on self test for the 68-41/42 and can also be run from the PLUM monitor.

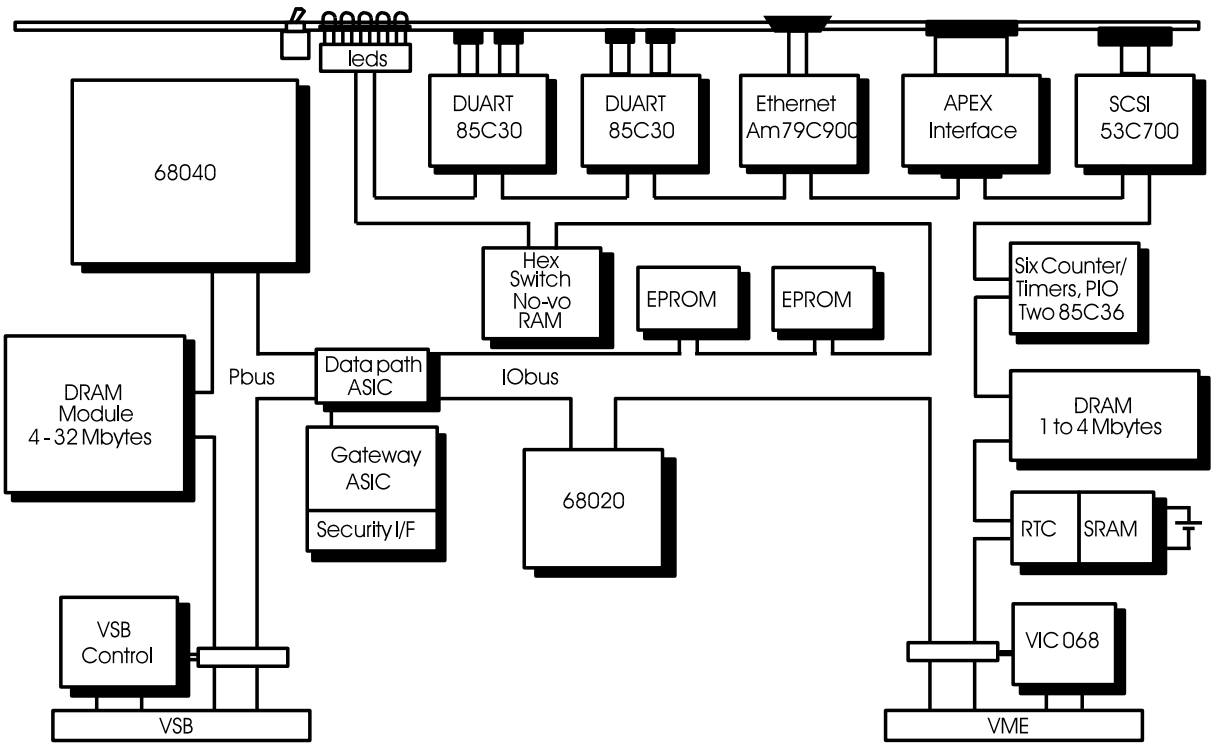
X42 Transition Module

(68-42 only)
The ability to attach I/O devices to the P2 backplane connector instead of using front panel connections, can be an advantage for some applications in terms of simplified system enclosure design, installation, upgrades and aesthetic appeal.

The X42 Transition Modules are available as an option for the 68-42. These convert the P2 pinout to a range of industry-standard connectors.

Documentation

A complete Technical Manual is available for the 68-41/42 This provides full specifications of VLSI devices, programming examples and full technical information.



68-41 Block Diagram

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